TI Designs

LMG5200: 48 to 1 V or 40 A Single-Stage Converter Reference Design

Description

The PMP4497 is a gallium nitride (GaN) based solution for 1.0-V and 40-A core, field programmable array (FPGA), and application specific integrated circuit (ASIC) applications. With high integration and low switching loss, the GaN module LMG5200 enables a high-efficiency, single stage from the 48 to 1.0 V solution to replace the traditional two-stage solution. This design shows the GaN performance and the system advantages compared with the 2-stages solution. A low-cost ER18 planar printed circuit board (PCB) transformer is embedded on the board. The design was achieved in a compact form factor (45 mm × 26 mm × 11 mm). The size could be further reduced by optimizing frequency and components. A design guide with complete test data is provided to facilitate new designs.

Resources

PMP4497	Design Folder
LMG5200	Product Folder
TPS53632	Product Folder
ISO7420FE	Product Folder
UCC27512DRSR	Product Folder
TLV70450DBVR	Product Folder
TLV70433DBVR	Product Folder
PMP4435	Tools Folder

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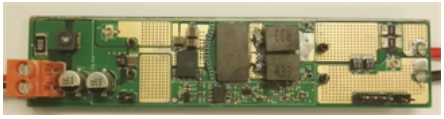
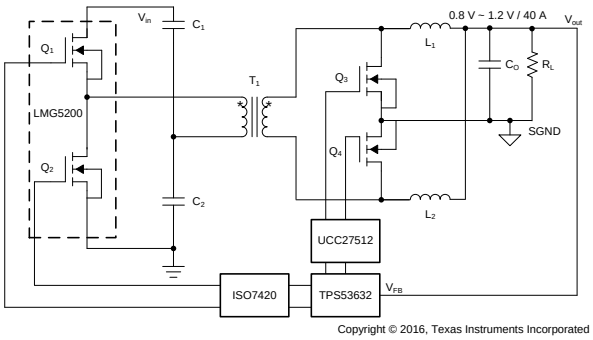
Features

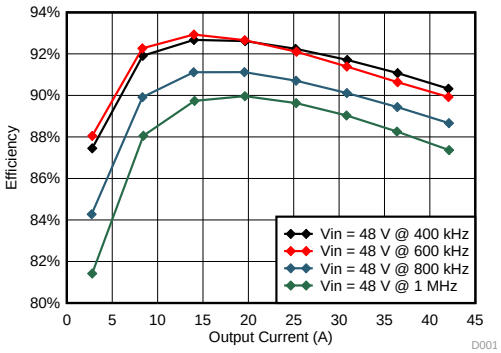
- Input Voltage From 36 to 60 V
- Single Stage Half-Bridge and Current Doubler
- Peak Efficiency up to 93.7% at 48 V, 1.0 V, and 600 kHz
- LMG5200 GaN FET Module
- DCAP+ Control With the TPS53632
- 400-kHz to 1-MHz Operation Frequency
- I²C Configurable From 0.8 to 1.2 V
- Optional Resistor-Configurable Load-Line
- Output Over Voltage Protection (OVP), Overcurrent Protection (OCP), and Output Under Voltage Protection (UVP)

Applications

- Servers and High-Performance Computing
- Telecom DC-DC Module
- Industrial Board Computer, Field Programmable Gate Array (FPGA), and Application Specific Integrated Circuit (ASIC)







1 System Overview

1.1 System Description

The PMP4497 implements the 48- to 1-V single-stage power conversion using a hard-switching half-bridge converter with the current-doubler synchronize rectifier. Figure 1 shows the topology implemented in this board. A LMG5200 and EPC2023 GaN FETs are used on the primary side and secondary side respectively. With the GaN MOSFET advantages, such as the zero-reverse recovery, low capacitance, and low Rds-on, the converter could achieve a smaller size and a higher efficiency compared with a traditional two-stage solution (for example, an eighth brick and the 12-V POL module).

Because the half-bridge converter is transformer-based, the converter can be isolated. The TPS53632 controller can support an isolated converter by using a digital isolator, for example, the ISO7420, to drive the primary-side LMG5200. The PMP4497 supports input voltage from 36 to 60 V and output voltage from 0.8 to 1.2 V; the default output voltage is 1.0 V. The output current supports up to 40 A; fan cooling is recommended to help dissipate the heat when operating above 20 A. The output voltage is programmable through an I²C interface. See the TPS53632 data sheet (SLUSBW8) for the details of the I²C program command and the data format.

1.2 Key System Specifications

Table 1. Key System Specifications

PARAMETER	TEST CONDITIONS	MINIMUM	TYP	MAXIMUM	UNIT
INPUT AND OUTPUT CHARACTERISTICS					
Input voltage range		36	48	60	V
Input current	V_{IN}= 36 V, V_{OUT}= 1.2 V, I_{OUT}= 40 A	—	—	1.4	A
Output voltage	I²C programmable	0.8	1.0	1.2	V
Output voltage tolerance	I_{OUT}= 0A	—	—	10	mV
Output current	—	—	—	40	A
Over-current protection	—	—	60		A
SYSTEM CHARACTERISTICS					
Switching frequency		400	600	1000	kHz
Peak efficiency	V_{IN}= 48 V, V_{OUT}= 1.0 V, I_{OUT}= 15 A, @600kHz without controller and driver losses	—	92.9	—	%
Full-load efficiency	V_{IN}= 48 V, V_{OUT}= 1.0 V, I_{OUT}= 40 A, at 600kHz without controller and driver losses	—	89.9	—	%
Transient load voltage variation	Transient at the 25% full load (10 A), the ELoad slew rate is 2.5 A/µs	—	±3	—	%

1.3 Block Diagram

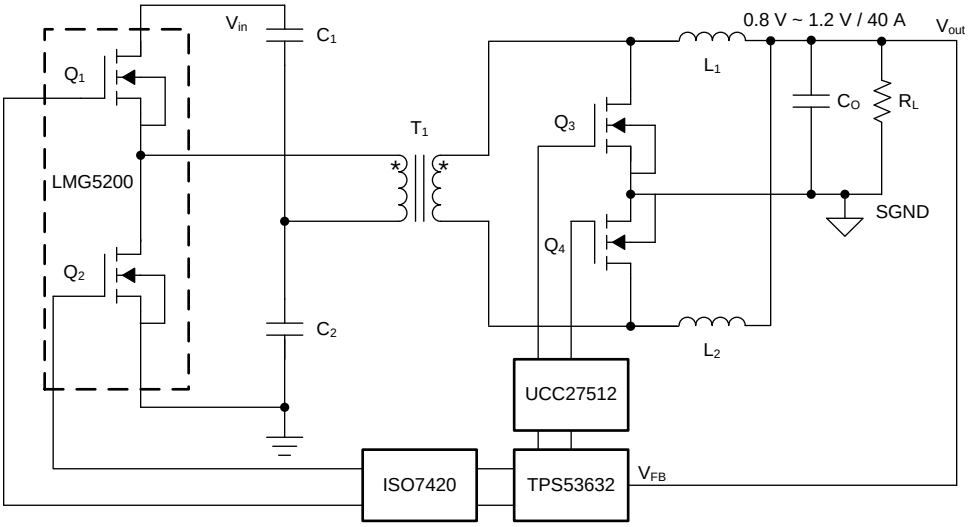


Figure 1. PMP4497 Block Diagram

1.4 Highlighted Products

1.4.1 LMG5200

The LMG5200 device integrates an enhancement-mode GaN FET half-bridge power stage with a 100-V driver, which provides a compact solution.

The device extends the advantages of discrete GaN FETs by offering a more user-friendly interface. The device is an ideal solution for the applications requiring high-frequency and high-efficiency operation in a small form factor. Integration reduces the board clearance and creepage needed for a discrete solution while minimizing the loop inductances to ensure fast switching and low ringing.

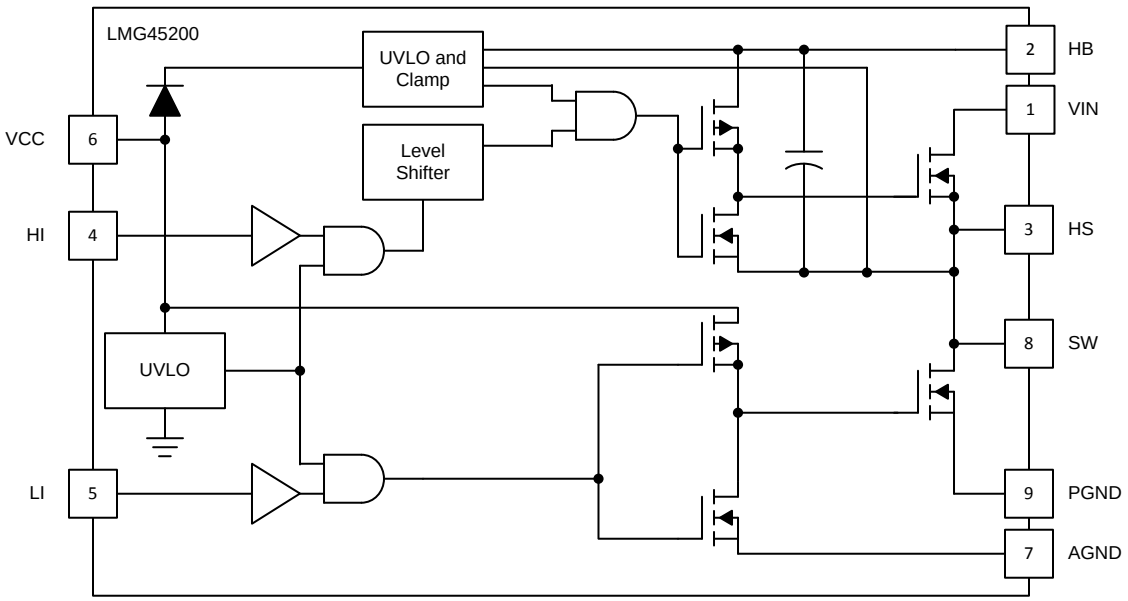


Figure 2. LMG5200 Functional Block Diagram

1.4.2 TPS53632

The TPS53632 device is a driverless step-down controller with I²C control. Its advanced features, such as D-CAP+ architecture, provide fast transient response, and high-efficiency operation with minimized output capacitance. The TPS53632 device supports the standard I²C revision 3.0 interface for dynamic control of the output voltage and current monitor telemetry. The device also has dynamic phase adding and shedding control and is able to enter single-phase, discontinuous-current mode operation to maximize light-load efficiency.

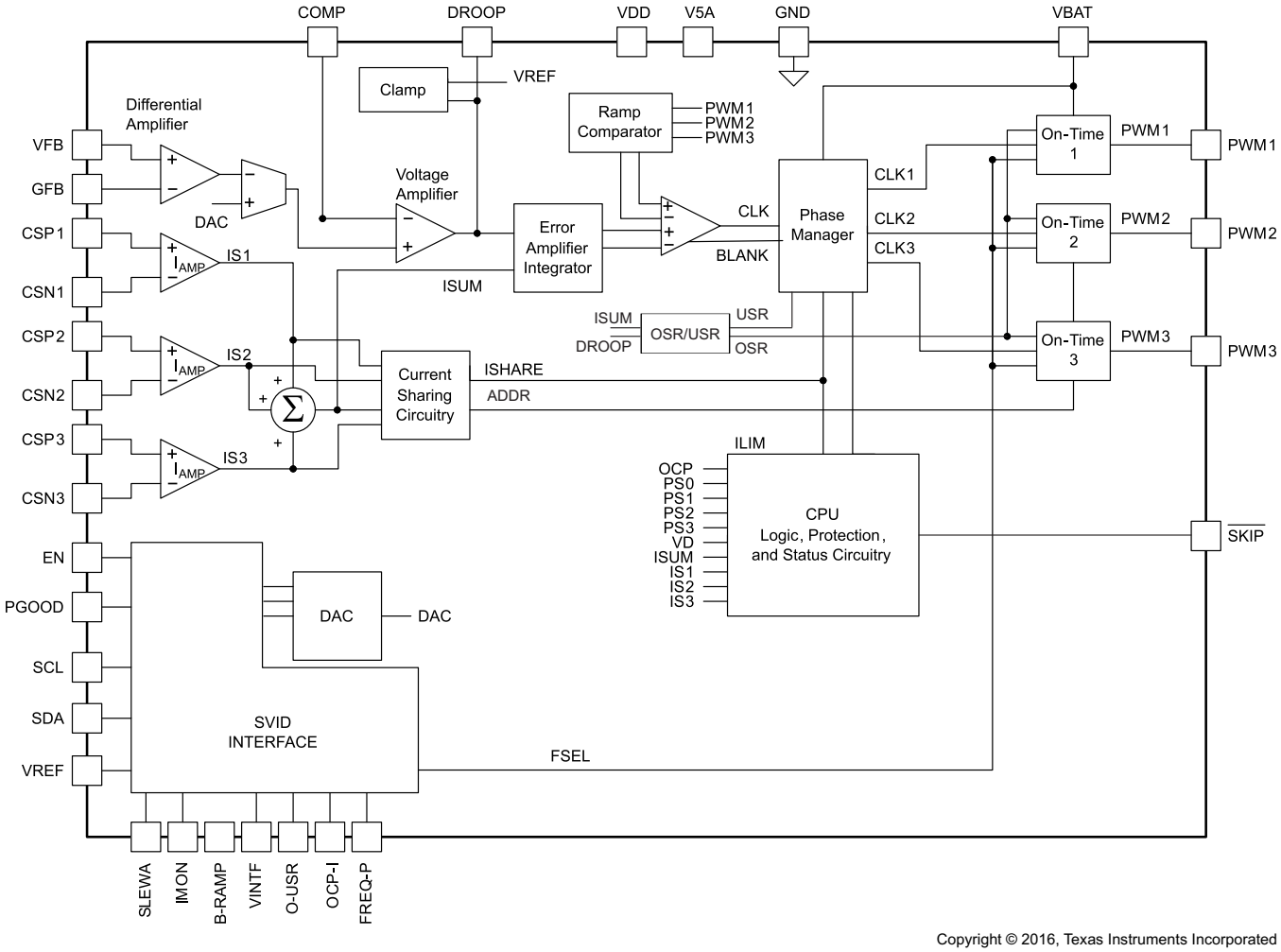


Figure 3. TPS53632 Functional Block Diagram

1.4.3 ISO7420

The ISO7420 is a low-power, dual-channel digital isolator. The device is used in the design to deliver isolated control signals from the secondary side to the LMG5200 on the primary side. The ISO7420 provides galvanic isolation up to 2500 V RMS for 1 minute per UL and 4242 VPK per VDE. This device has two isolated channels. Each channel has a logic input and output buffer separated by an insulation barrier. Used in conjunction with an isolated power supply, the device prevents noise current from entering the local ground and interfering with or damaging sensitive circuitry.

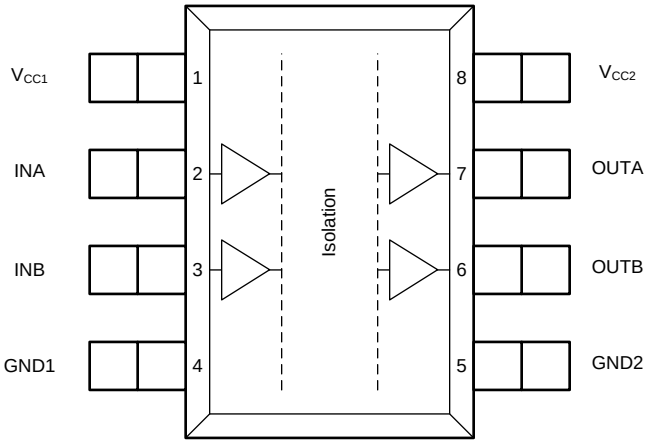


Figure 4. ISO7420 Block Diagram

1.4.4 UCC27512

The UCC27512 is a single-channel, high speed, low-side gate-driver device. The device can effectively drive the MOSFET and insulated gate bipolar translator (IGBT) power switches with 4-A peak source and 8-A peak sink asymmetrical drive capability. Using TI intellectual property (IP) that inherently minimizes shoot-through current, the UCC27512 is capable of sourcing and sinking high peak-current pulses into capacitive loads and offering rail-to-rail drive capability with small propagation delay, typically 13 ns. In the PMP4497 design, a duty signal to IN- of the driver to drive the synchronous rectifier MOSFET. IN+ is bypassed by connecting it to VDD directly.

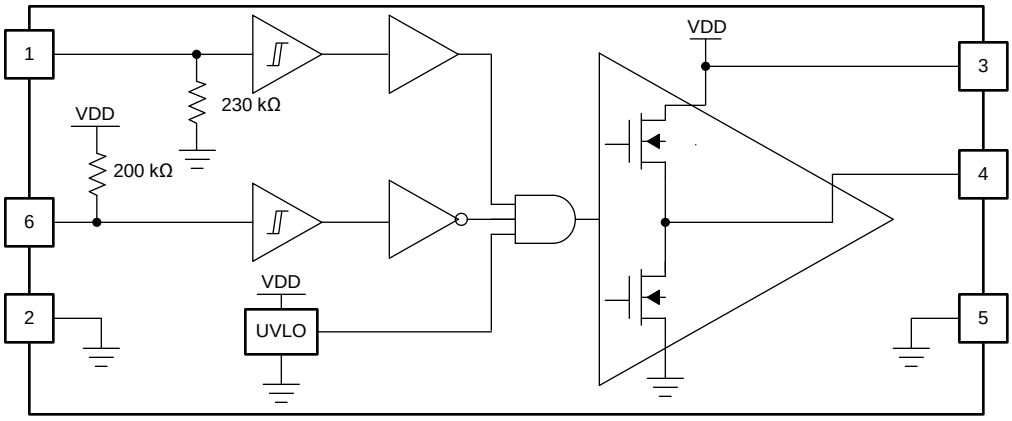


Figure 5. UCC27512 Block Diagram

2 System Design Theory

Benefitting from the output ripple current cancellation technique, a half-bridge converter with a current doubler rectifier circuit is suitable for low-profile, high-voltage input and large output current applications and provides higher efficiency. The converter key theoretical waveforms are shown in Figure 6.

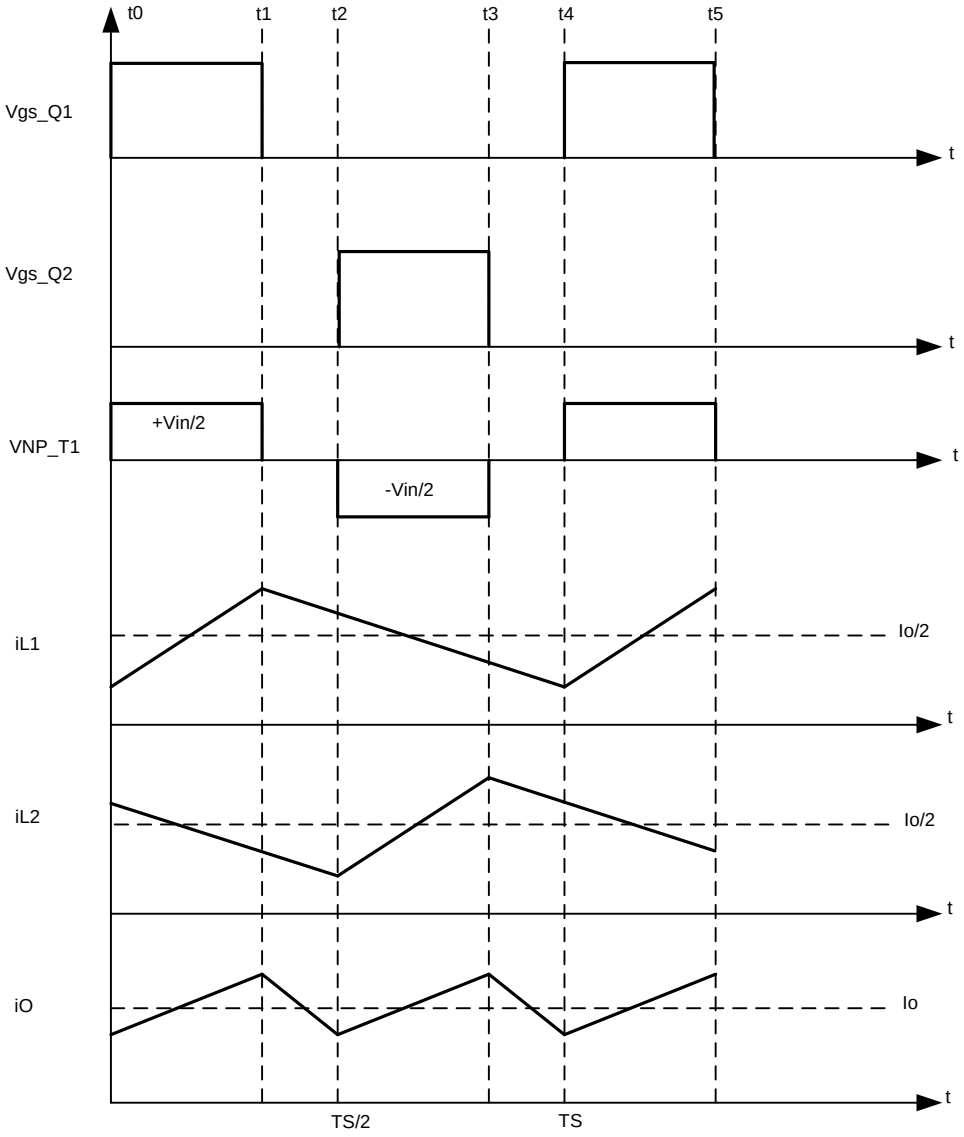


Figure 6. Half-Bridge with Current Doubler Timing Diagram

2.1 Operation Modes of the Converter With Current Flow

The converter in the continuous current mode (CCM) mode has four operation modes during one full switching period as shown in Figure 7.

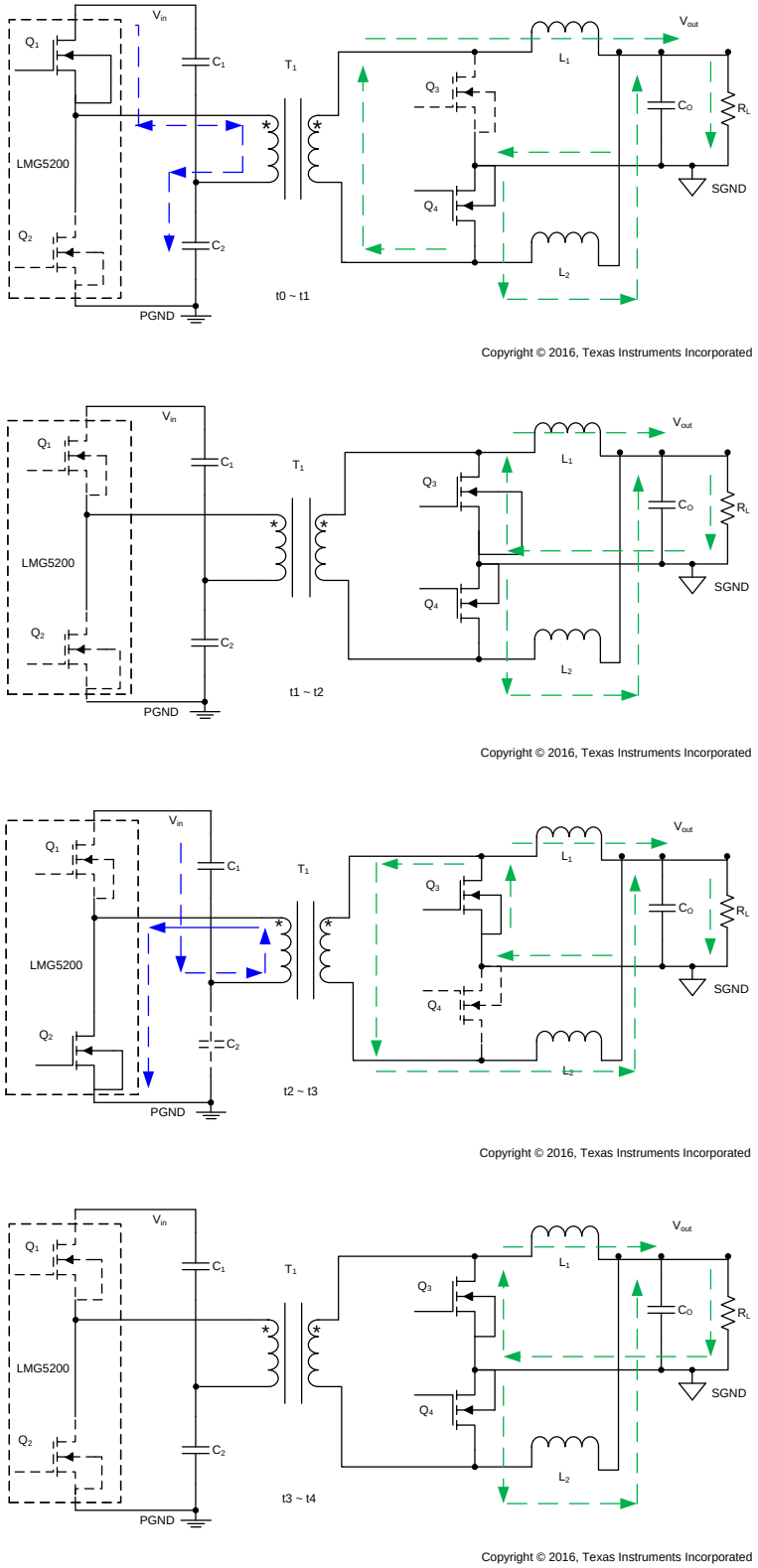


Figure 7. Operation Modes With Current Flow

2.2 Circuit Operation and Description

Time interval $t_0 \rightarrow t_1$:
During the $t_0 \rightarrow t_1$, Q_1 and Q_4 are on, and Q_2 and Q_3 are off. The transformer T_1 secondary winding begins to charge the output inductor L_1, and the L_2 is discharged to the output capacitor and the load.

$$\frac{V_{in}}{2} \times \frac{N_S}{N_P} - V_O = L_1 \times \frac{di_1}{dt}$$

$$0 - V_0 = L_2 \times \frac{di_2}{dt}$$

Time interval $t_1 \rightarrow t_2$:
During the $t_1 \rightarrow t_2$, Q_1 and Q_2 are off, and Q_3 and Q_4 are on. Both L_1 and L_2 discharges the current to the output; the inductor current is discharged linearly.

$$0 - V_0 = L_1 \times \frac{di_1}{dt}$$

$$0 - V_0 = L_2 \times \frac{di_2}{dt}$$

Time interval $t_2 \rightarrow t_3$:
During the $t_2 \rightarrow t_3$, Q_1 and Q_4 are off, and Q_2 and Q_3 are on. The transformer T_1 secondary winding inverses the polarity and begins to charge the output inductor L_2, and the current in L_1 is discharged to the output capacitor and the load.

$$0 - V_0 = L_1 \times \frac{di_1}{dt}$$

$$\frac{V_{in}}{2} \times \frac{N_S}{N_P} - V_0 = L_2 \times \frac{di_2}{dt}$$

Time interval $t_3 \rightarrow t_4$:
During the $t_3 \rightarrow t_4$, Q_1 and Q_2 are off, and Q_3 and Q_4 are on. Both the L_1 and L_2 are discharged to the output; the inductor current is decreased linearly.

$$0 - V_0 = L_1 \times \frac{di_1}{dt}$$

$$0 - V_0 = L_2 \times \frac{di_2}{dt}$$

According to the simplified operation models, during the $t_0 \rightarrow t_1$ (DT_s) the winding begins to charge the inductor L_1 with the voltage $\left(\frac{V_{in}}{2} \times \frac{N_S}{N_P} - V_0\right)$, and the current i_1 increases linearly. Within the $t_1 \rightarrow t_4$ (1-D), the current i_1 decreases with the voltage $(0 - V_0)$. The inductors ripple current is as follows:

$$\Delta i_1 = \frac{V_0 \times (1-D) \times T_S}{L_1}$$

Based on the voltage-second balance of the inductor, the CCM voltage transfer ratio is

$$\left(\frac{Vin}{2} \times \frac{NS}{NP} - V_0\right) \times D \times T_S = V_0 \times (1-D) \times T_S$$

$$M = \frac{V_O}{V_{in}} = \frac{N_S}{2 \times N_P} \times D$$

3 Getting Started Hardware

3.1 Hardware

The converter output range is from 0.8 to 1.2 V, and the input voltage range is from 36 to 60 V. Operation should be within the input/output voltage ranges.

If the converter shuts off due to UVP or OCP, the controller IC must be rested to re-enable the converter. To change the output voltage, the I²C bus should be used to set the TPS53632. Consult the user guide for the TPS53632 for the necessary VID protocol (SNVU520). The TPS53632 controller's switching frequency, voltage ramp rate, load line, and OCP could be changed by modifying resistor values on the board. The TPS53632 data sheet (SLUSCJ3) includes the detailed procedures to choose these components.

3.1.1 Test Equipment

- DC voltage source: supplies the EVM from 36 V to 60 V, output current >2A
- DC bias source: 6 to approximately 9V or 0.5 A, two outputs for the primary and secondary
- Oscilloscope: >200-MHz operation, use oscilloscope probes with a pigtail spring ground clip instead of the standard alligator clip
- DC multimeter: capable of 100-V measurement, suitable for efficiency
- DC load: supports 1-V operation at up to 50 A in current-mode operation
- Fan cooling: 200-LFM minimum airflow is recommended to cool the PCB when operating over 20-A output current

3.1.2 Measurement Procedure

The following procedure is used to measure the board.

1. Connect the input and output supplies as shown in Figure 8.
2. Connect the oscilloscope to the board to measure input/output voltage. Use a bayonet nut connector (BNC) to a subminiature version A (SMA) cable or differential probe for the noise immunity.
3. Connect the bias supply. The onboard LDO provides 5 and 3.3 V to the power and control circuitry.
4. Power up the input supply. Operation below 36 V may result in the output voltage range out of regulation.
5. Power up the bias supply to start the converter. The output voltage will ramp up and the output voltage should be in regulation.
6. Enable the electronic load and set to a desired load current.
7. Test and measure the input/output voltage response, efficiency, and so forth.

3.1.3 Shutdown Procedure

After the measurements have been completed, shut down the board by the following steps:

1. Disable the input voltage supply.
2. Disable the electronic load.
3. Disable the bias supply.

4 Testing and Results

4.1 Test Setup

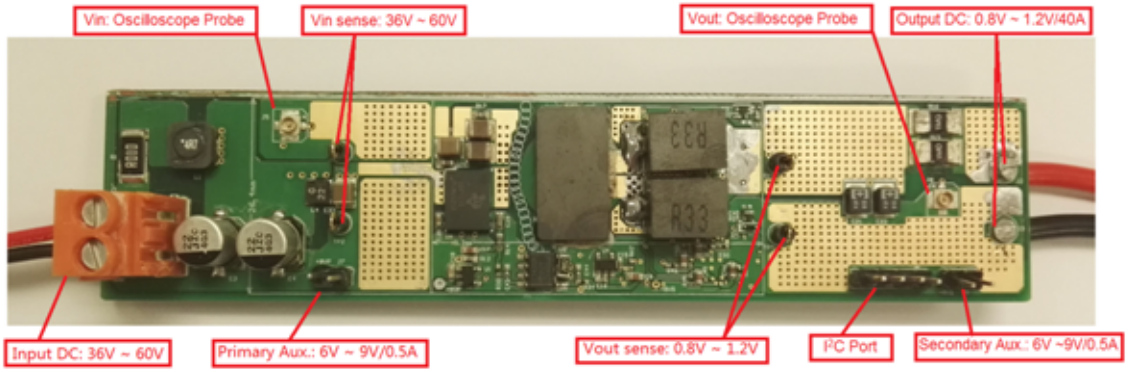


Figure 8. Connection Points

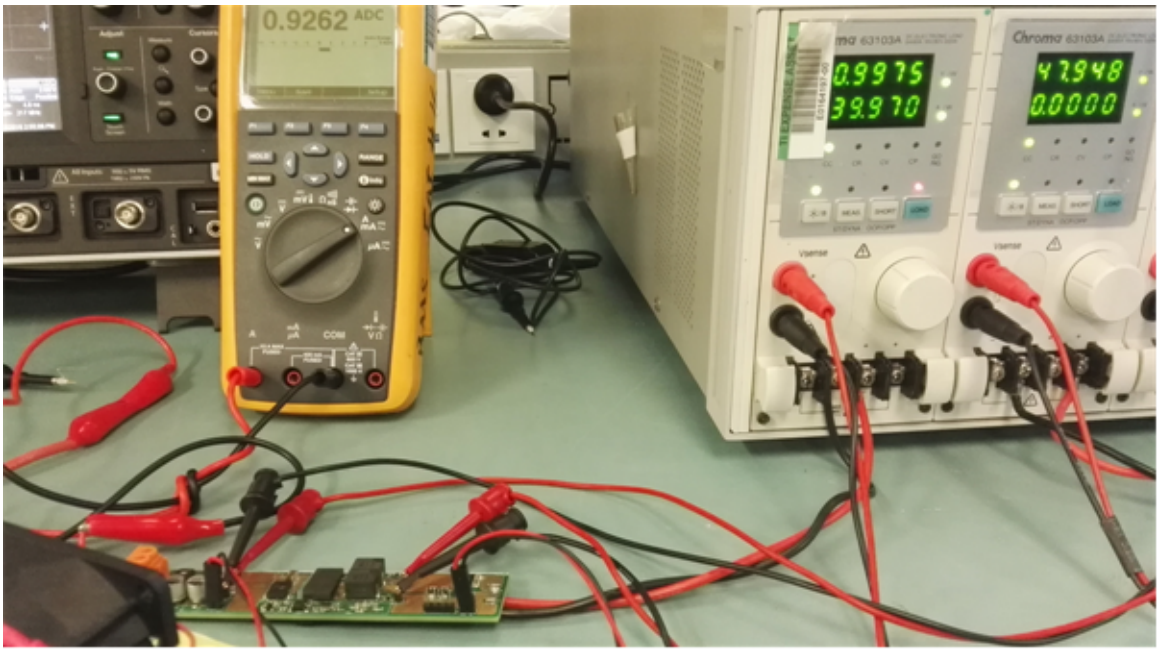


Figure 9. Testing Setup With Full Load

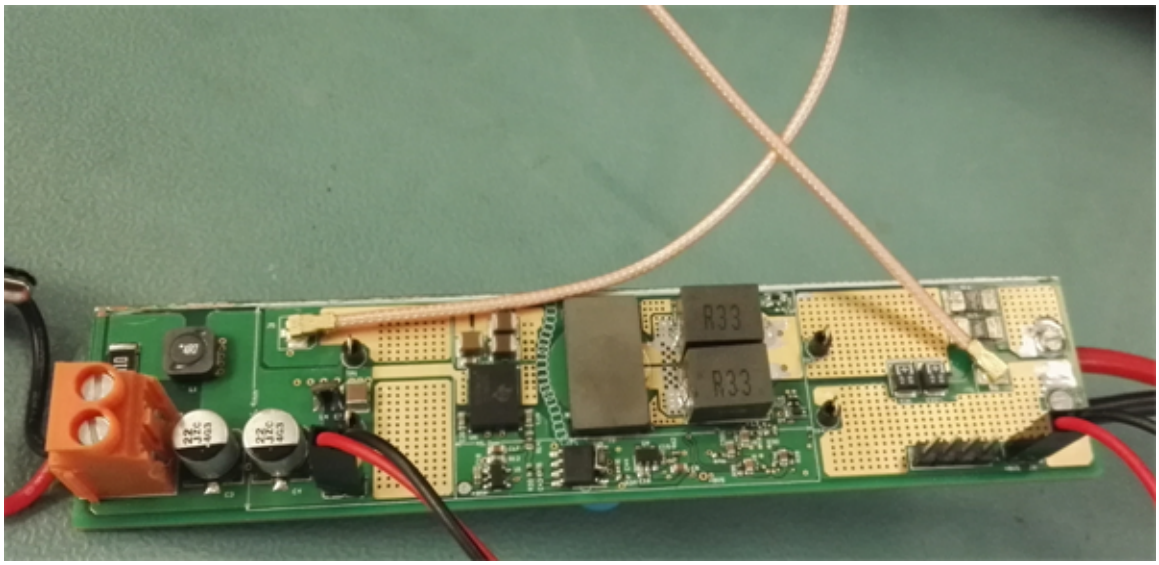


Figure 10. Oscilloscope Probe Connections

4.2 Test Data

The following sections detail the typical performance curves and waveforms of the PMP4497.

4.2.1 Efficiency

Note that most of the efficiency results in this section do not include the controller losses (aside from Figure 14). The default output voltage is 1.0 V.

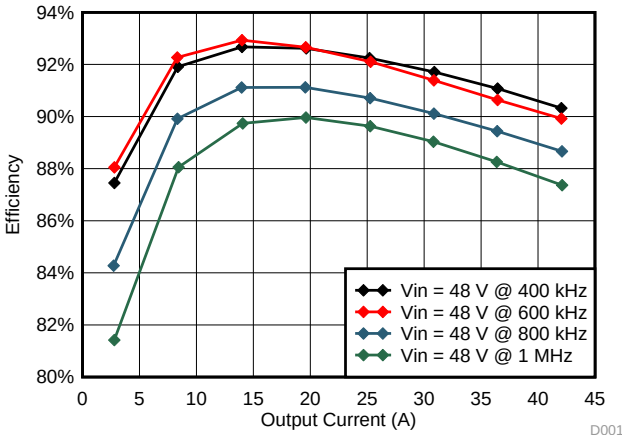


Figure 11. Efficiency Curve Without Controller Loss Versus Switching Frequency

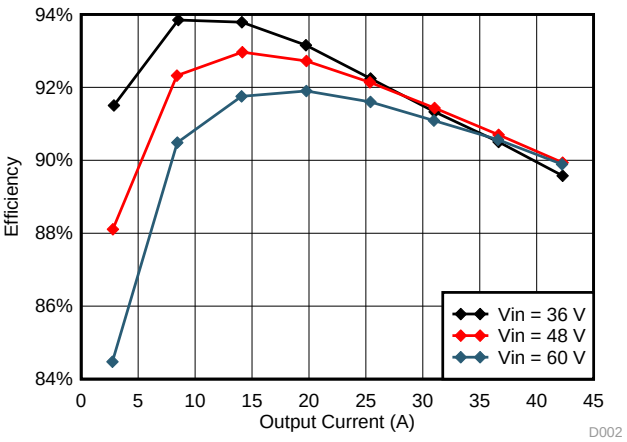


Figure 12. Efficiency Curve Without Controller Loss Versus Output Current

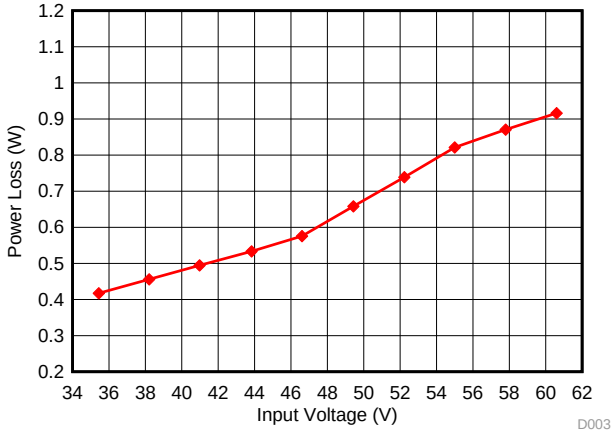


Figure 13. Power Loss (No Load) Versus Input Voltage

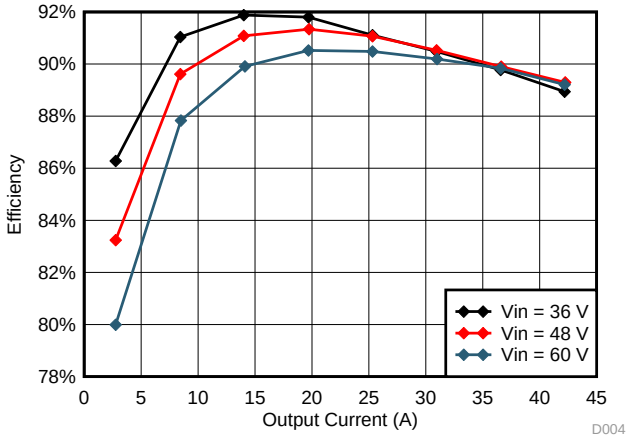


Figure 14. Efficiency Curve with Controller Loss Versus Output Current

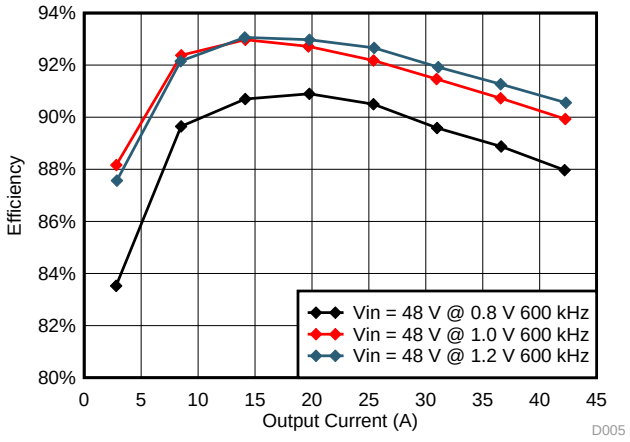
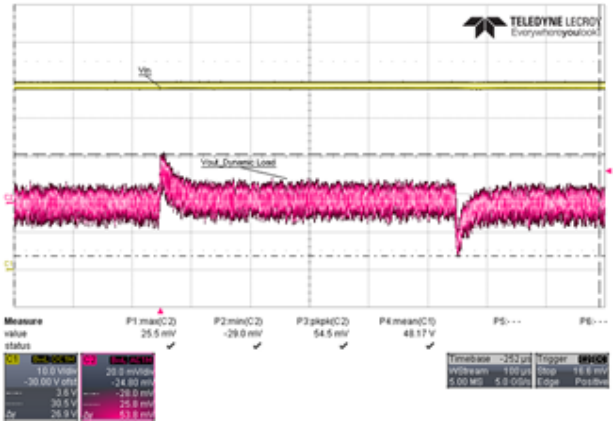
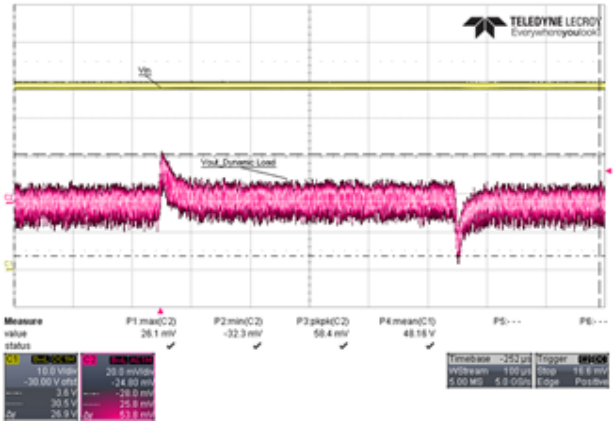


Figure 15. Efficiency Curve without Controller Loss Versus Vout Change (Through I²C)

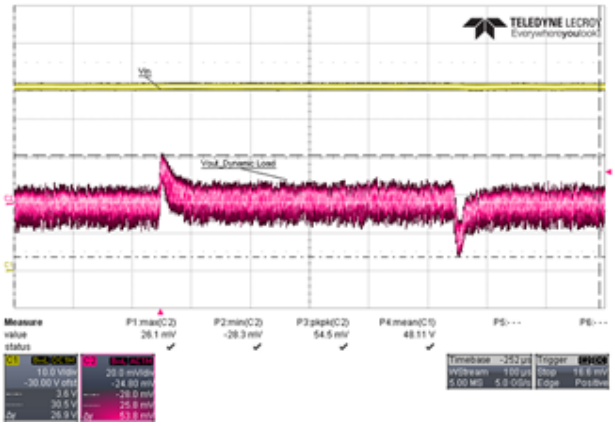
4.2.2 Transient Load Waveforms



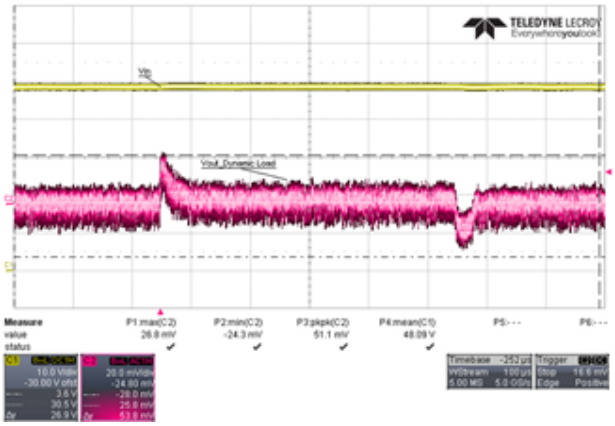
Transient load (0 to 25%)
C1: 48-V input voltage 10.0 V/Div
C2: 1.0-V output voltage 20.0 mV/Div



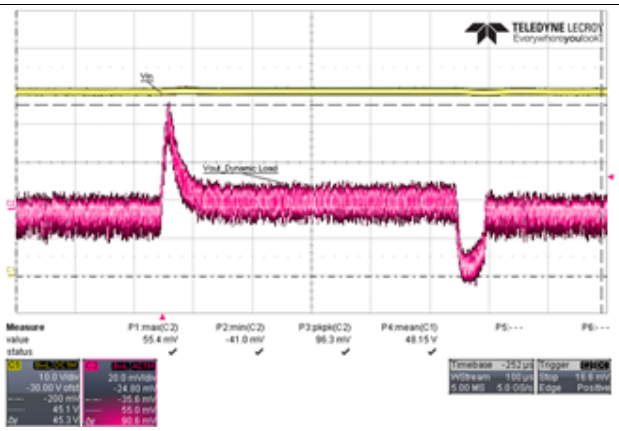
Transient load (25 to 50%)
C1: 48-V input voltage 10.0 V/Div
C2: 1.0-V output voltage 20.0 mV/Div



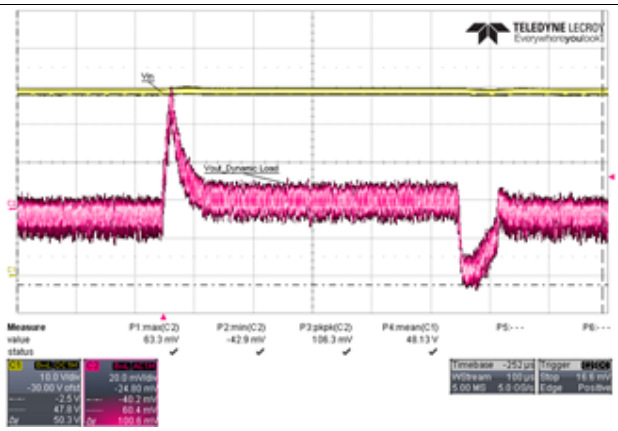
Transient load (50 to 75%)
C1: 48-V input voltage 10.0 V/Div
C2: 1.0-V output voltage 20.0 mV/Div



Transient load (75 to 100%)
C1: 48-V input voltage 10.0 V/Div
C2: 1.0-V output voltage 20.0 mV/Div

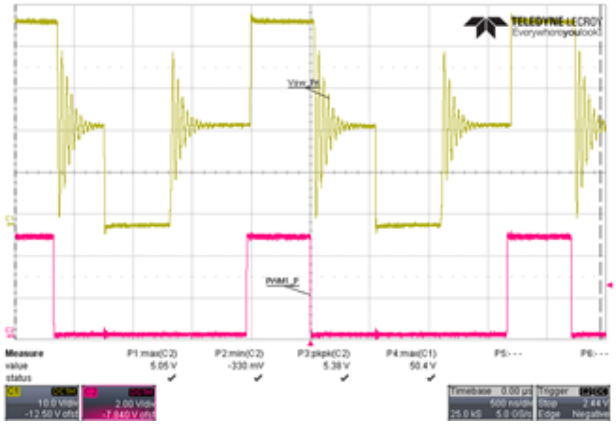


Transient load (10 to 90%)
C1: 48-V input voltage 10.0 V/Div
C2: 1.0-V output voltage 20.0 mV/Div

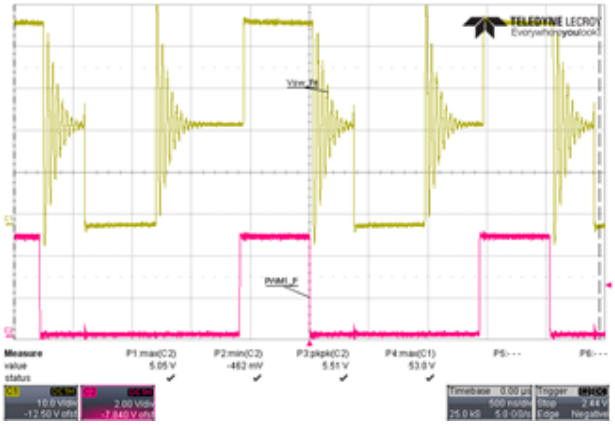


Transient load (0 to 100%)
C1: 48-V input voltage 10.0 V/Div
C2: 1.0-V output voltage 20.0 mV/Div

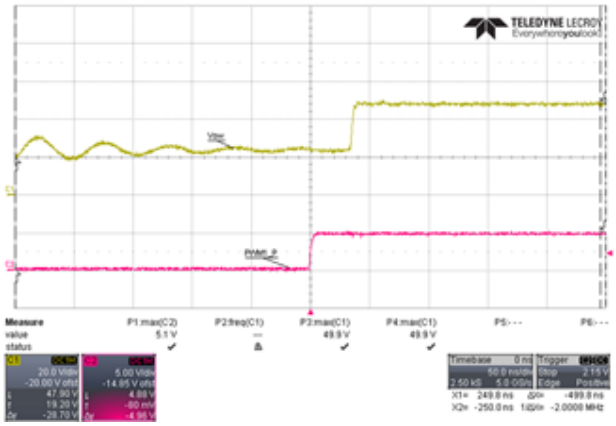
4.2.3 Switching Node Waveforms (Full Bandwidth)



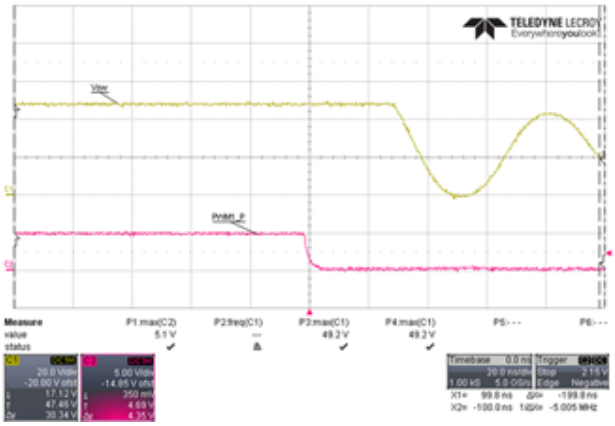
Primary Vsw versus PWM1_P no load
C1: Vsw switching node 10 V/Div
C2: PWM1_P driver signal 2.0 V/Div



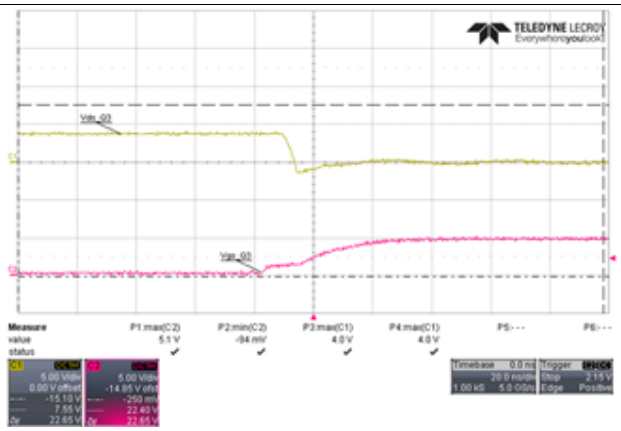
Primary Vsw versus PWM1_P full load
C1: Vsw switching node 10 V/Div
C2: PWM1_P driver signal 2.0 V/Div



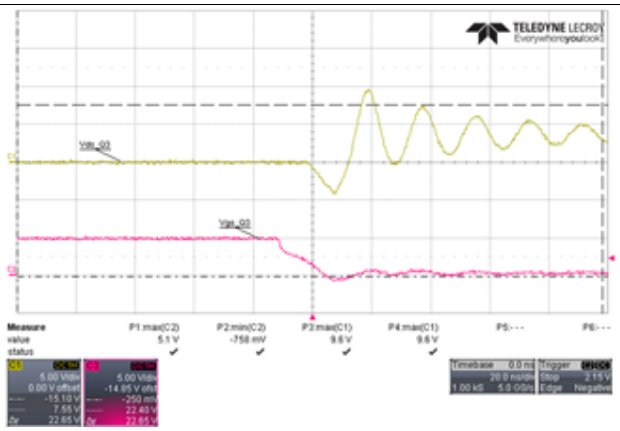
Primary Vsw versus PWM1_P full load
C1: Vsw switching node 20 V/Div
C2: PWM1_P driver signal 5.0 V/Div



Primary Vsw versus PWM1_P full load
C1: Vsw switching node 20 V/Div
C2: PWM1_P driver signal 5.0 V/Div



Secondary Vds_Q3 versus Vgs_Q3 at 40 A
C1: Vds_Q3 5.0 V/Div
C2: Vgs_Q3 5.0 V/Div



Secondary Vds_Q3 versus Vgs_Q3 at 40 A
C1: Vds_Q3 5.0 V/Div
C2: Vgs_Q3 5.0 V/Div

4.2.4 IR Scan Thermal Gradient (With Fan Cooling)

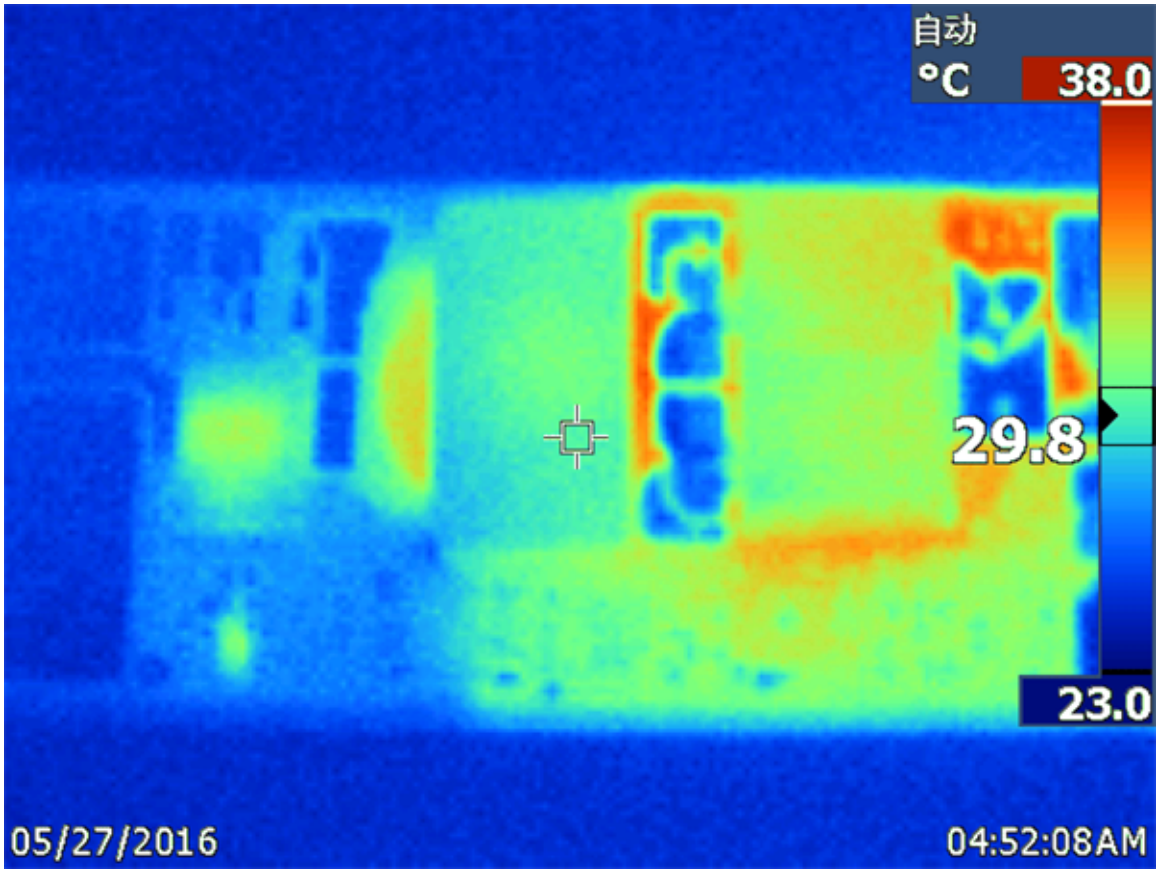


Figure 16. 48-V Input at Full Load (1.0 V and 40 A)

5 Design Files

5.1 Schematics

To download the schematics, see the design files at PMP4497.

5.2 Bill of Materials

To download the bill of materials (BOM), see the design files at PMP4497.

5.3 PCB Layout Recommendations

High-switching speed is important in a high-efficiency design. Optimizing the PCB layout to minimize the power loop impedance and parasitic inductance is a necessary measure to achieve the goal.

It is recommended to use a multilayer board. Power loop parasitic impedance should be minimized by having the input capacitor return path (between VIN and PGND) directly underneath the first layer as shown in the below Figure 17. Loop inductance is reduced due to inductance cancellation as the return current is directly underneath and flowing in the opposite direction. The VCC capacitors and the bootstrap capacitors are placed in the first layer and should be as close to the device as possible.

The AGND of LMG5200 should *not* be directly connected to PGND in order to avoid the PGND noise and not to cause spurious switching events due to noise coupling to HI and LI signals. Reducing the impedance and the inductances on the board and the PCB layout should comply with the clearance and creepage distance requirements.

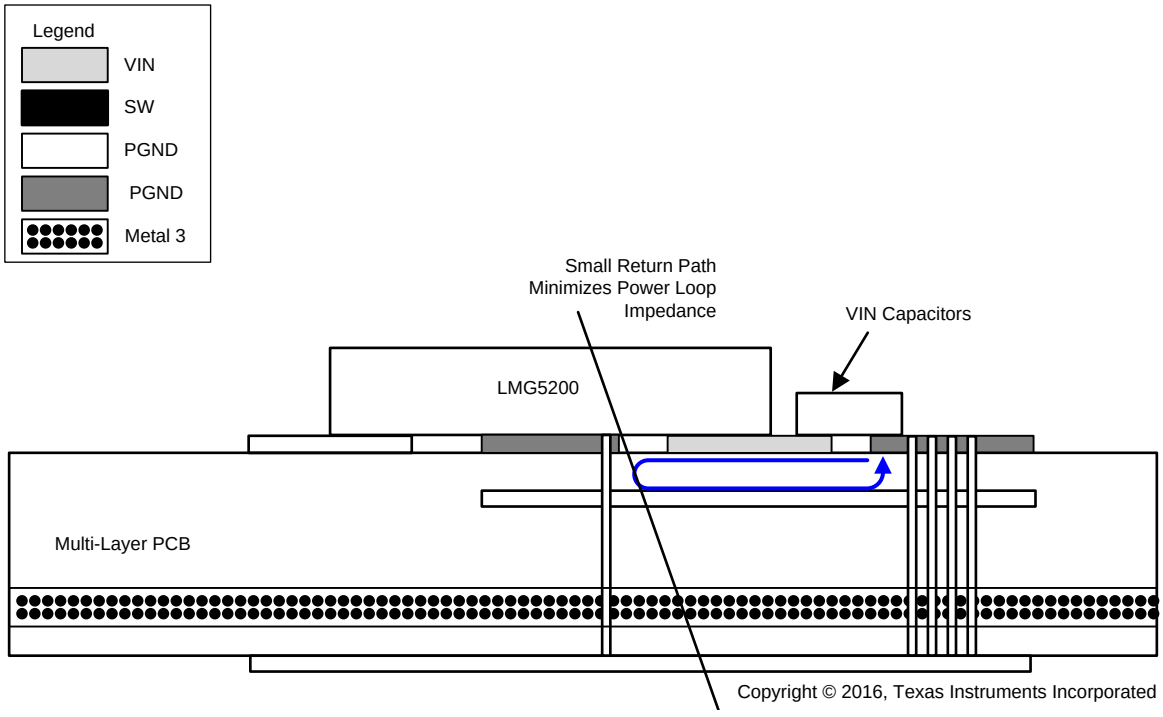


Figure 17. Multilayer Board Cross Section With Return Path Directly Underneath for Power Loop

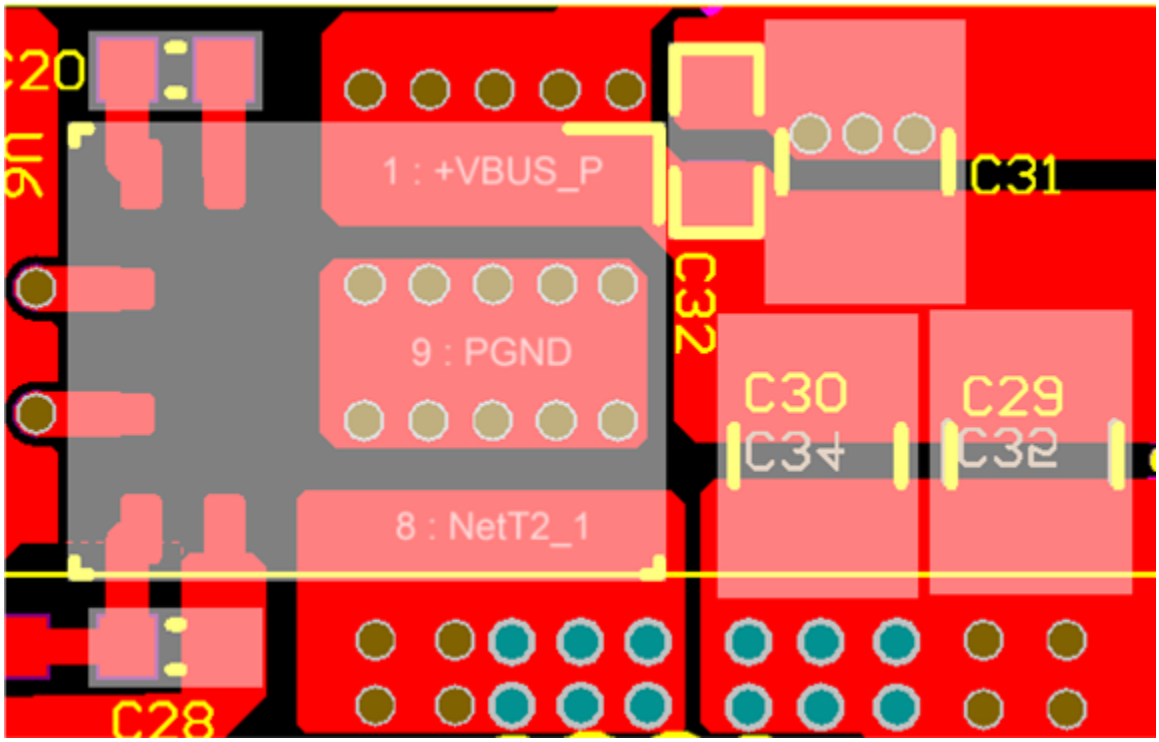


Figure 18. LMG5200 Top Layer Placement

5.3.1 Layout Prints

To download the layer plots, see the design files at PMP4497.

5.4 Altium Project

To download the Altium project files, see the design files at PMP4497.

5.5 Gerber Files

To download the Gerber files, see the design files at PMP4497.

5.6 Assembly Drawings

To download the assembly drawings, see the design files at PMP4497.

6 Software Files

To download the software files, see the design files at PMP4497.

7 References

1. Texas Instruments, *Using the LMG5200POLEVM-10A GaN 48V-1V Point-of-Load EVM*, User's Guide (SNVU520)
2. Texas Instruments, *GaN TECHNOLOGY PREVIEW LMG5200 80-V, GaN Half-Bridge Power Stage*, Data Sheet (SNOSCY4)
3. Texas Instruments, *Current Doubler Rectifier Offers Ripple Current Cancellation*, Application Note (SLUA323)
4. Texas Instruments, *Control Driven Synchronous Rectifiers In Phase Shifted Full Bridge Converters*, Application Note (SLUA287)

8 About the Author

JASON YU is a senior application engineer at Texas Instruments where he is responsible for developing reference design solutions for power systems. Jason brings his extensive experience in high frequency, high density, and digital power design to this role. Jason holds a master's degree in power electronics from South China University of Science and Technology. He has over ten years of experience in power design.

Revision A History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (September 2016) to A Revision	Page
• Changed from preview draft	1

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