*TI Designs*

# *36-W, Universal Input, >90% Efficiency, Dual Output, Auxiliary Supply Reference Design for Server PSU*

## Description

The TIDA-00709 is a 36-W, dual output, auxiliary power supply with provision to accept both wide ranges of DC as well as AC input. Based on the input, this TI Design can be used as an adapter or auxiliary power supply designed for use in power converters targeted for server, telecom, and industrial system applications. This reference design is a quasi-resonant (QR) flyback converter implemented using the UCC28740 constant voltage-constant current (CV-CC) flyback controller with optocoupled feedback for voltage and primary-side regulation (PSR) for current. For improved efficiency, the TIDA-00709 uses synchronous rectification with sync controller UCC24636 and low $R_{DS(on)}$ MOSFET for main 12-V_ISO/2.75-A output. Hardware is designed and tested to pass conducted emissions, surge and EFT requirements. Additionally, the design has a built-in eFuse for multiple faults isolation for main output rail without effecting any other output.

## Resources

| | |
|---|---|
| TIDA-00709 | Design Folder |
| UCC28740 | Product Folder |
| UCC24636 | Product Folder |
| CSD19531 | Product Folder |
| ATL431 | Product Folder |
| TPS259241 | Product Folder |

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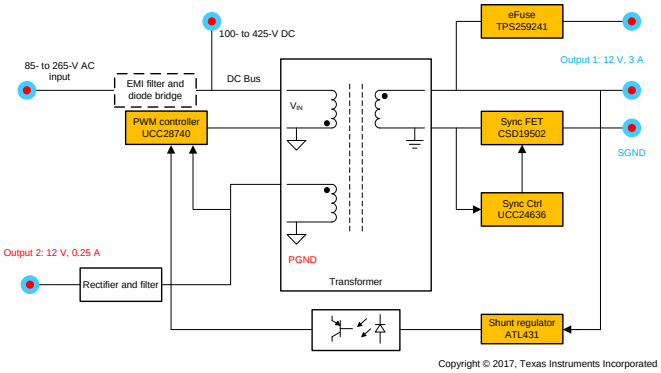
## Features

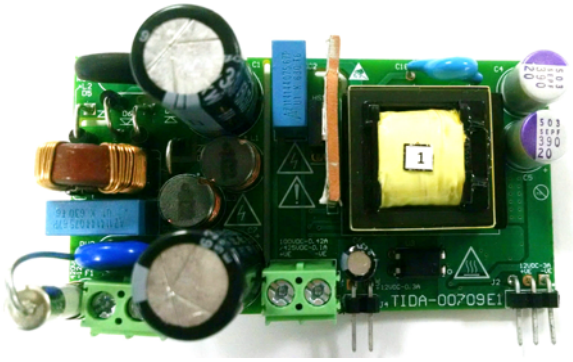
- High Efficiency of > 90% With AC Input and > 92% With DC Input
- Minimum Efficiency > 86.5% at 10% Load Aids to Meet 80Plus Titanium Standard of Server PSUs
- Designed for Wide Operating Input Voltage Range from 100- to 425-V DC or 85- to 265-V AC
- Delivers Full Power of 36 W Over Entire Operating Voltage Range
- Low Standby Power (≈ 120 mW) Aids to Meet No-Load Condition Limits of DoE Level VI and EU CoC Tier-I
- Dual Output: 12 V/0.25 A and 12 V_ISO/2.75 A
- Compact Form-Factor to Achieve High Power Density Solutions:
  - DC/DC: 40 mm × 45 mm
  - AC/DC: 70 mm × 45 mm
- eFuse for Multiple Fault Isolation of Main Output
- Robust Supply Protected for Input Brownout, Output Overcurrent, Short-Circuit, and Output Overvoltage Conditions

## Applications

- Auxiliary Power for Server PSU and Telecom Rectifiers
- AC-DC Adapters
- Housekeeping PSU for UPS
- Battery Chargers





# 1 System Overview

## 1.1 System Description

High-power converters used in server, telecom, and industrial systems need auxiliary power supplies to support housekeeping needs of the power supply unit (PSU). An auxiliary power supply is commonly used to power the internal control electronics and voltage and current feedback sensing electronics of the PSU. It is an isolated DC-DC converter generating multiple outputs to power primary and secondary side control devices. The typical usage of an auxiliary power supply of a server PSU is shown in Figure 1.

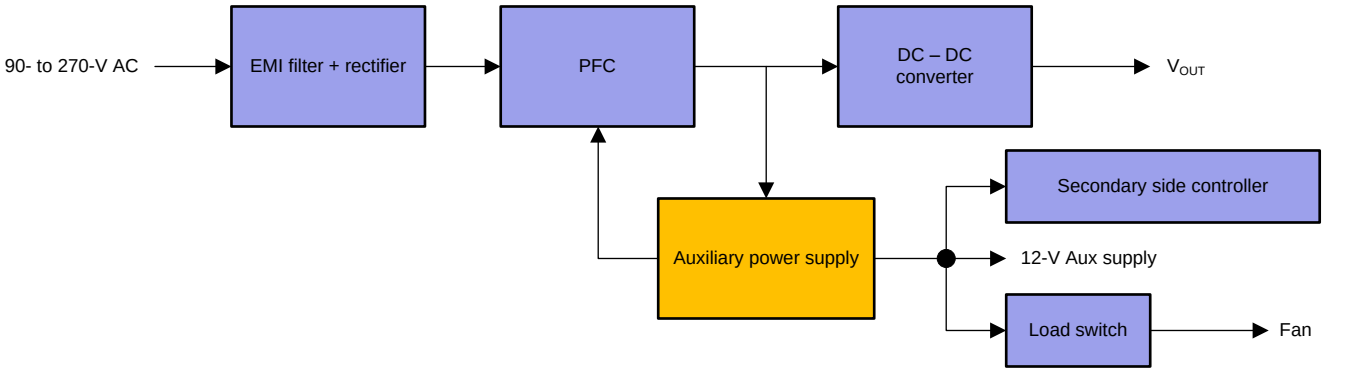





**Figure 1. Typical Block Diagram of Server Power Supply**

The auxiliary power supplies are independent isolated DC-DC converters because PSUs have an EMI filter, a diode-bridge rectifier, and a bulk capacitor present in the system, generating a rectified DC bus. These supplies operate over a wide input range from 100- to 450-V DC and need to keep system electronics powered under all conditions to detect faults such as undervoltage, overvoltage, and overcurrent. Typically, auxiliary power supplies generate multiple outputs delivering power from 5 to 40 W, supporting system fans and auxiliary output. These supplies need to have low standby power to meet the stringent norms such as the Department of Energy (DoE) and Code of Conduct (CoC). In addition, these need to have high efficiency form 10% to 100% loads, ensuring low system power loss under all operating conditions.

This reference design is a 36-W auxiliary power supply, designed specifically to meet low standby power needs of < 100 mW with DC input, high DC average efficiency of > 91% for a wide load range from 25% to 100%, over entire input operating voltage range. This reference design is a simple, low component, low-cost primary side regulated (PSR) flyback converter implemented using the device UCC28740 that regulates constant voltage (CV) and constant current (CC) output and uses quasi-resonant (QR) valley switching, and secondary-side rectification implemented using the UCC24636 synchronous rectification controller for higher efficiency. The design operates over wide input range of 100- to 425-V DC, delivering a total power of 36 W.

In addition, there is also a provision for wide AC input ranging from 85- to 265-V AC, enabling this design to be used as standard AC-DC power supply and adapter. Figure 2 shows a block diagram for a typical adapter system. The TIDA-00709 meets the stringent norms such as the Department of Energy (DoE) Level VI and Code of Conduct (CoC) Tier-I. Their requirements of active average efficiency for a 36-W adapter are 82.98% and 87.03%, respectively. The minimum active average efficiency met with the TIDA-00709 with AC input is approximately 88%. The EU CoC Tier-I minimum efficiency requirement at a 10% load for a 36-W adapter is 77.03% while the minimum efficiency at a 10% load with this TI Design is approximately 88%. Also, DoE Level VI and CoC Tier-I no-load power requirements for multiple output power supply are 300 mW and 150 mW, respectively. The EMI filter and rectifier have been designed such that the total standby power is < 150 mW, efficiency is > 90% with 230-V AC and > 88% with a 115-V AC input, and meets class-B conducted emission level.

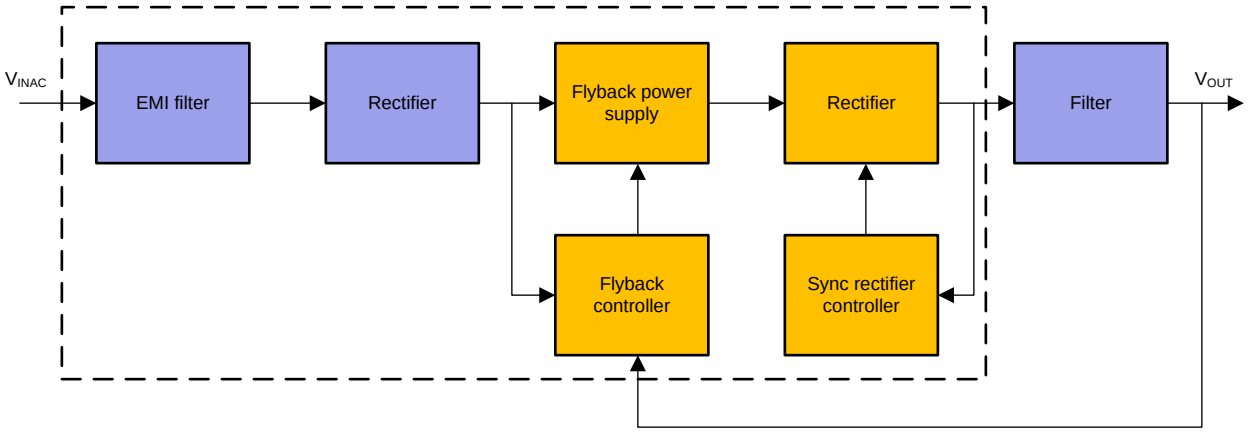





**Figure 2. Adapter System Block Diagram**

## 1.2 Key System Specifications

**Table 1. Key System Specifications**

| PARAMETER | TEST CONDITIONS | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| **INPUT CONDITIONS** | | | | | | |
| Input voltage ($V_{IN}$) | — | | 100 | 160/325 | 425 | VDC |
| | | | 85 | 115/230 | 260 | VAC |
| No load power ($P_{NL}$) | $V_{INDC}$ = 400 V, $I_{OUT}$ = 0 A | | — | 0.1 | — | W |
| | $V_{INAC}$ = 230 V, $I_{OUT}$ = 0 A | | — | 0.15 | — | W |
| Brownout voltage ($V_{IN\_UVLO}$) | — | | — | 70 | — | V |
| **OUTPUT CONDITIONS** | | | | | | |
| $V_{OUT\_1}$(isolated) | — | | 11.4 | 12.0 | 12.6 | VDC |
| $I_{OUT\_1}$ (isolated) | — | | — | 2.75 | — | A |
| $V_{OUT\_2}$(non-isolated) | — | | 11.4 | 12 | 12.6 | VDC |
| $I_{OUT\_2}$(non-isolated) | — | | — | 0.25 | — | A |
| Line regulation | At full load, $V_{IN}$ = 100- to 400-V DC | | — | — | 5 | % |
| Load regulation | $V_{IN}$ = 100- to 400-V DC, Load: 10% to 100% | | — | — | 5 | % |
| Output voltage ripple ($V_{RIPPLE}$) | At full load | 12 V | — | — | 500 | mV |
| | | 12 V_ISO | — | — | 500 | |
| Output power ($P_{OUT}$) | — | | — | 36 | — | W |
| Primary to secondary insulation | — | | — | 3.75 | — | kV |
| **SYSTEM CHARACTERISTICS** | | | | | | |
| Efficiency (η) | $V_{INDC}$ = $V_{NOM}$, $I_{OUT}$= 25%, 50%, 75% and 100% | | — | — | 92.2 | % |
| | $V_{INAC}$ = $V_{NOM}$, $I_{OUT}$= 25%, 50%, 75% and 100% | | — | — | 90.2 | % |
| Protections | Output overvoltage | | | | | |
| | Input undervoltage | | | | | |
| | Overcurrent | | | | | |
| | Short-circuit and power limit | | | | | |
| | Open loop protection | | | | | |
| Operating ambient | Open frame | | –45 | 25 | 60 | °C |
| Conducted emissions | — | | As per EN55022/11 Class-B | | | |
| EFT | — | | As per IEC 61000-4-4, Level-4 | | | |
| Surge | — | | As per IEC-61000-4-5, Level-4 | | | |
| Dimensions | Length × Width × Height | DC-DC | 40 × 45 × 17 | | | mm |
| | | AC-DC | 70 x 45 x 30 | | | |

## 1.3 Block Diagram

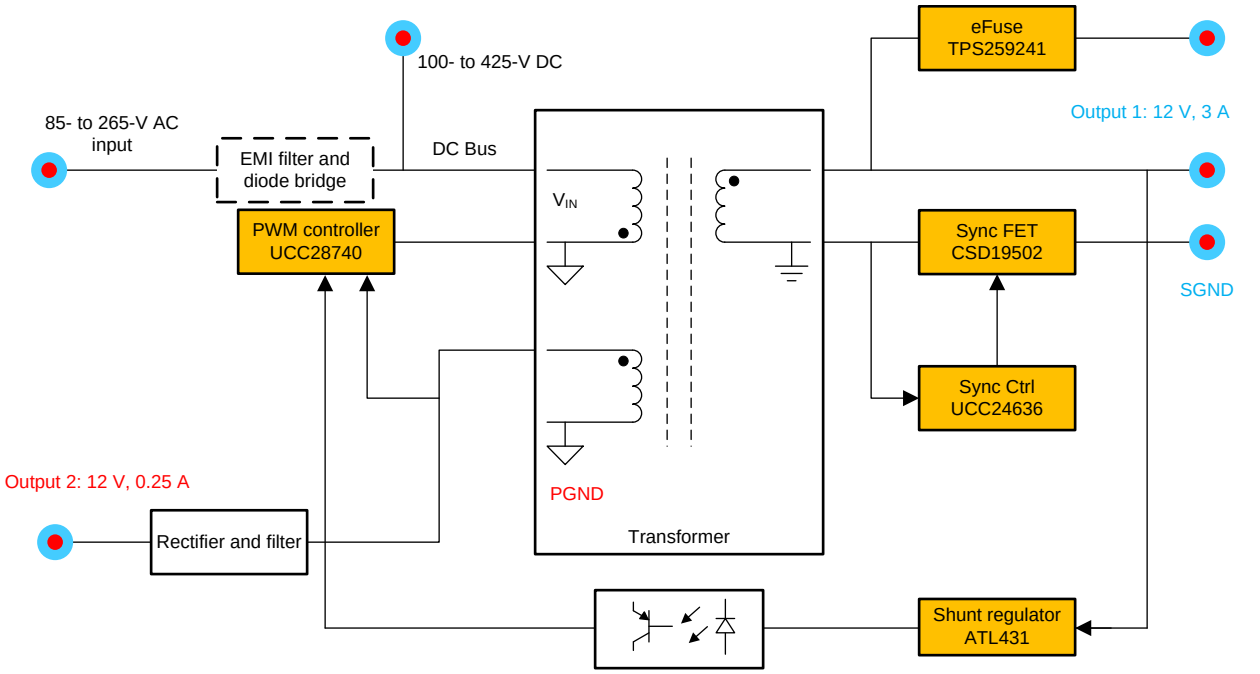





**Figure 3. Block Diagram of 36-W Auxiliary Power Supply**

## 1.4 Highlighted Products

The following are the highlighted products used in this reference design. Key features for selecting the devices for this reference design are explained in the following subsections. Find complete details of the highlighted devices in their respective product datasheets.

### 1.4.1 UCC28740 CV-CC Flyback Controller

To implement the high-performance, small form factor flyback design less than 100 W, the UCC28740 is the preferred controller as it offers a series of benefits to address the needs of very compact DC-DC converters. The device has a reduced number of feedback loops for precision current and power limits, which eliminates the need of current sensing on secondary-side and multiple optocoupler feedback loops for open-loop detection and power limiting.

The UCC28740 isolated flyback power supply controller provides CV output regulation using an optical coupler to improve transient response under large load steps. CC regulation is accomplished through the PSR technique. This device processes information from optocoupled feedback and from an auxiliary flyback winding for precise high-performance control of output voltage and current. An internal 700-V start-up switch, dynamically-controlled operating states and a tailored modulation profile support ultra-low standby power without sacrificing start-up time or output transient response. The drive output interfaces to a MOSFET power switch. Discontinuous conduction mode (DCM) with valley-switching reduces switching losses. Modulation of switching frequency and primary current peak amplitude (FM and AM) keeps the conversion efficiency high across the entire load and line ranges.

Key features that make this device unique are:

- Optocoupled feedback regulation for CV and PSR for CC
- Enables ±1% voltage regulation and ±5% current regulation across line and load
- 100-kHz max switching frequency enables high-power density designs
- QR valley switching operation for highest overall efficiency
- Frequency jitter scheme to ease EMI compliance
- Wide VDD range (35 V) allows small bias capacitor
- Drive output for MOSFET
- Enables <10-mW system standby power
- Protection functions: Overvoltage, low line, and overcurrent
- SOIC-7 package

### 1.4.2 UCC24636 Synchronous Rectifier (SR) Controller With Ultra-Low Standby Current

High-efficiency designs need synchronous rectification to optimize the power loss. The UCC24636 offers great benefits and simplicity in design, offering near-ideal diode rectifier function.

The UCC24636 SR is a compact, 6-pin secondary-side synchronous rectifier MOSFET controller and driver for high efficiency flyback converters operating in DCM and Transition Mode (TM). Unlike traditional SR controllers that measure the SR MOSFET drain voltage, the UCC24636 implements a volt-second balance control method to determine the turn-off transition of the SR MOSFET, hence SR conduction time is independent of the MOSFET $R_{DS(on)}$, parasitic inductance or ringing allowing flexibility to designers in component selection and PCB layout. This control method enables maximum SR conduction time and highest rectifier efficiency for a given MOSFET.

The controller's built-in intelligence to detect converter no load and automatically entry in the standby mode operation helps achieve low standby power. The wide VDD operating range for the controller allows direct bias from the converter output for fixed or variable output voltage designs eliminating the need for an auxiliary winding on the main transformer which simplifies the circuit design and reduces the cost.

Key features that make this device unique are:

- Volt-second balance control enables highest rectifier efficiency
- Secondary-side SR controller optimized for 5- to 24-V output DCM and TM flyback converters
- Compatible with PSR and SSR flyback controller
- Ultra-low 110-µA standby current consumption
- Auto-Detect standby mode disables SR switching for lower no-load power consumption
- SR turn-off independent of $R_{DS(on)}$ and parasitic inductance
- Operating frequency up to 130 kHz
- Wide VDD range from 3.6 to 28 V
- Adaptive gate drive clamp
- Open and short pin fault protection

### 1.4.3 CSD19531Q5A 100-V N-Channel NexFET™ Power MOSFETs

To achieve good efficiency, select a MOSFET with very low $R_{DS(on)}$. Keeping and cost of total solution in mind, the CSD19531 was chosen for this design. This is a 100-V, 5.3-mΩ, SON 5-mm×6-mm NexFET power MOSFET designed to minimize losses in power conversion.

Key features that make this device unique are:

- Ultra-low $Q_G$ and $Q_{GD}$
- Low thermal resistance
- Avalanche rated
- RoHS compliant
- Halogen free
- SON 5-mm×6-mm plastic package

### 1.4.4 ATL431B Precision Programmable Reference

The ATL431 devices are three-terminal adjustable shunt regulators, with specified thermal stability over applicable automotive, commercial, and industrial temperature ranges. The output voltage can be set to any value between $V_{REF}$ (approximately 2.5 V) and 36 V, with two external resistors. These devices have a typical output impedance of 0.05 Ω. Active output circuitry provides a very sharp turn-on characteristic, making this device excellent replacements for Zener diodes.

Key features that make this device unique are:

- Adjustable regulated output voltage: 2.5 to 36 V
- Very low operating current:
  - $I_{KA(min)}$ = 35 µA (max)
  - $I_{REF}$ = 150 nA (max)
- Internally compensated for stability
  - Stable with no capacitive load
- Reference voltage tolerances at 25°C:
  - 0.5% for ATL431B
  - 1% for ATL431A
- Typical temperature drift:
  - 5 mV (–40°C to 85°C); I Version
  - 6 mV (–40°C to 125°C); Q Version
- Extended cathode current range: –35 µA to 100 mA
- Low output impedance: 0.3 Ω (max)

### 1.4.5 TPS259241 12-V eFuse With Overvoltage Protection and Blocking FET Control

The TPS259241 eFuse is a highly integrated circuit protection and power management solution in a tiny package. The device uses few external components and provide multiple protection modes. The TPS259241 is a robust defense against overloads, shorts circuits, voltage surges, excessive inrush current, and reverse current.

The current limit level can be set with a single external resistor. Overvoltage events are limited by internal clamping circuits to a safe fixed maximum with no external components required.

Key features that make this device unique are:

- $V_{OPERATING}$ = 4.5 to 13.8 V, $V_{ABSMAX}$ = 20 V
- Integrated 28-mΩ pass MOSFET
- Fixed 15-V overvoltage clamp
- 1- to 5-A adjustable $I_{LIMIT}$
- ±8% $I_{LIMIT}$ accuracy at 3.7 A
- Reverse current blocking support
- Programmable OUT slew rate, UVLO
- Built-in thermal shutdown
- Safe during single-point failure test (UL60950)
- Small footprint: 10L (3-mm×3-mm) VSON

# 2 System Design Theory

This reference design provides 36 W of continuous power over a wide DC input range from 100- to 400-V DC with a provision for wide AC input as well. The design has a flyback power stage implemented using the UCC28740 QR PSR CC-CV flyback controller to deliver dual outputs: 12 V_ISO/2.75 A and 12 V/0.25 A. The total system efficiency with DC input is ≈ 92% for 165-V DC and ≈ 91.8% for 325-V DC and with AC input, it is over 90% for 230VAC and >88% for 115VAC. The design has precise current limit and limits the power to ≤ 40 W under all fault conditions. In addition, several protections are embedded into this TI Design, which includes input undervoltage protection and output short-circuit protection.

Overall, the main focus of this design is to achieve high efficiency and low standby power to help meet 80Plus (Titanium) standard for Server PSU, DoE Level VI and EU CoC Tier-2 norms in very compact form-factor to address high power density.

## *2.1 QR Flyback Converter With PSR*

Flyback converters provide a cost effective solution for AC-DC and DC-DC conversion needs. They are widely used for converters up to 150 W. There are three modes of operation, namely DCM, QR mode, and continuous conduction mode (CCM). For lower power applications, DCM or QR mode is preferred as they have reduced power losses and optimal peak currents. As the output wattage increases, the CCM becomes more efficient due to the reduced peak and RMS currents.

Flyback converters designed with PSR flyback controllers eliminate the use of conventional optocoupler based feedback. The PSR flyback controllers sense the voltage feedback through auxiliary winding and current feedback through the current sense resistor used in series with switching FET. In addition, Texas Instruments PSR flyback controllers provide a wide range of protections and accurate limiting of both current and power. The UCC28740 controller has both PSR feedback and opto-feedback, enhancing the reliability of the system.

## *2.2 Flyback Circuit Component Design*

The UCC28740 is a flyback controller that provides both CV mode and CC mode control for precise output regulation. While in CV operating range, the controller uses an optocoupler for tight voltage regulation and improved transient response to large load steps. Accurate regulation while in CC mode is provided by primary-side control. The UCC28740 uses frequency modulation, peak primary current modulation, valley switching, and valley hopping in its control algorithm to maximize efficiency over the entire operating range.

The design process and component selection for this design are illustrated in the following sections. All design calculations are available in the TIDA-00709 Design Calculator.

### 2.2.1 Design Goal Parameters

Table 2 lists the design goal parameters for this TI Design. These parameters will be used in further calculations to select components.

**Table 2. Design Goal Parameters**

| PARAMETER | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| **INPUT** | | | | | |
| $V_{IN}$ | Input voltage | 100 | 162/325 | 400 | VDC |
| | | 85 | 115/230 | 265 | VAC |
| $f_{LINE}$ | Input Frequency | 47 | 50/60 | 63 | Hz |
| | Brownout voltage | — | 70 | — | VAC |
| **OUTPUT** | | | | | |
| $V_{OUT\_1}$ | Output voltage (Isolated) | 11.4 | 12.0 | 12.6 | VDC |
| $I_{OUT\_1}$ | Output current (Isolated) | — | 2.75 | — | A |
| $V_{OUT\_2}$ | Output voltage (non-isolated) | 11.4 | 12 | 12.6 | VDC |
| $I_{OUT\_2}$ | Output current (non-isolated) | — | 0.25 | — | A |
| $P_{OUT}$ | Output power | — | 36 | — | W |
| — | Line regulation | — | — | 5 | % |
| — | Load regulation | — | — | 5 | % |
| $F_{MAX}$ | Maximum desired switching frequency | — | — | 100 | kHz |
| η | Targeted efficiency | — | 90 | — | % |

The main application for this design is auxiliary power supply for Telecom and Server PSU where the input for this design is the output from the front-end PFC. Thus all the parameters are designed keeping DC input in mind.

### 2.2.2 Transformer Parameter Calculations: Turns Ratio, Primary Inductance, and Peak Primary Current

The target maximum switching frequency at full load, the minimum input voltage, and the estimated DCM QR time determine the maximum primary-to-secondary turns ratio of the transformer.

First determine the maximum available total duty cycle of the on-time and secondary conduction time based on the target switching frequency, $F_{MAX}$, and DCM resonant time. For DCM resonant frequency, assume 500 kHz if an estimate from previous designs is not available. At the transition-mode operation limit of DCM, the interval required from the end of secondary current conduction to the first valley of the $V_{DS}$ voltage is half of the DCM resonant period ($t_R$), or 1 µs assuming a 500-kHz resonant frequency. The maximum allowable MOSFET on-time $D_{MAX}$ is determined using Equation 1:

$$D_{MAX} = 1 - D_{MAGCC} - F_{MAX} \times \frac{t_R}{2} \quad (1)$$

where:

- $t_R$ is the estimated period of the LC resonant frequency at the switch node
- $D_{MAG\_CC}$ is defined as the secondary-diode conduction duty-cycle during CC operation and is fixed internally by the UCC28740 at 0.425
- $t_R$ = 2 µs

$$D_{MAX} = 1 - 0.425 - 100\ \text{kHz} \times \frac{2\ \mu\text{s}}{2} = 0.475$$

When $D_{MAX}$ is known, the maximum primary-to-secondary turns ratio is determined with Equation 2. Calculate the total voltage on the secondary winding by adding $V_{OCV}$, $V_F$, and $V_{OBC}$.

$$N_{PS(max)} = \frac{D_{MAX} \times V_{DC(min)}}{D_{MAGCC} \times \left(V_{OCV} + V_F + V_{OCBC}\right)} \quad (2)$$

$V_{OBC}$ is the additional voltage drop of post filter inductor and any other target cable-compensation voltage added to $V_{OCV}$ (provided by an external adjustment circuit applied to the shunt regulator). Set $V_{OCV}$ equal to 0 V if not used.

$$N_{PS(max)} = \frac{0.475 \times 100\ V}{0.425 \times \left(12\ V + 0.4\ V\right)} = 9.0133$$

A higher turns ratio generally improves efficiency, but may limit operation at low input voltage.

The transformer turns ratio selected affects the MOSFET $V_{DS}$ and secondary rectifier reverse voltage, so these must be reviewed. The UCC28740 requires a minimum on-time of the MOSFET ($t_{ON(min)}$) and minimum secondary rectifier conduction time ($t_{DM(min)}$) in the high line and minimum load condition. The selection of $F_{MAX}$, $L_P$ and $R_{CS}$ affects the minimum $t_{ON(min)}$ and $t_{DM(min)}$.

The secondary rectifier and MOSFET voltage stress can be determined by Equation 3 and Equation 4, respectively.

$$V_{REV} = \frac{V_{IN(max)}}{N_{PS}} + V_{OCV} + V_{OCBC} \quad (3)$$

For the MOSFET $V_{DS}$ voltage stress, include an estimated leakage inductance voltage spike ($V_{LK}$).

$$V_{DSPK} = V_{IN(max)} + \left(V_{OCV} + V_{OCBC} + V_F\right) \times N_{PS} + V_{LK} \quad (4)$$

Equation 5 determines if $t_{ON(min)}$ exceeds the minimum $t_{ON}$ target of 280 ns (maximum $t_{CSLEB}$). Equation 6 verifies that $t_{DM(min)}$ exceeds the minimum $t_{DM}$ target of 1.2 µs.

$$t_{ON(min)} = \frac{L_P}{V_{IN(max)}} \times \frac{I_{PP(max)}}{K_{AM}} \quad (5)$$

where:

- $K_{AM}$ denotes the AM control ratio

$$t_{DM(min)} = \frac{t_{ON(min)} \times V_{IN(max)}}{N_{PS} \times \left(V_{OCV} + V_F\right)} \quad (6)$$

To determine the optimum turns ratio $N_{PS}$, design iterations are generally necessary to optimize and evaluate system-level performance trade-offs and parameters mentioned in Equation 3 through Equation 6. The design spreadsheet provides an easy way to iterate and arrive at the optimum value for $N_{PS}$.

When the optimum turns ratio $N_{PS}$ is determined from a detailed transformer design, use this ratio for the following parameters. For this design, $N_{PS}$ = 9.5 is selected on optimization.

The UCC28740 CC regulation is achieved by maintaining $D_{MAGCC}$ at the maximum primary peak current setting. The product of $D_{MAGCC}$ and $V_{CST(max)}$ defines a CC-regulating voltage factor $V_{CCR}$, which is used with $N_{PS}$ to determine the current sense resistor value necessary to achieve the regulated CC target, $I_{OCC}$ (see Equation 7).

$$R_{CS} = \frac{V_{CCR} \times N_{PS}}{2 \times I_{OCC}} \times \sqrt{\eta_{XFMR}} \tag{7}$$

Because a small portion of the energy stored in the transformer does not transfer to the output, a transformer efficiency term is included in Equation 7. This efficiency number includes the core and winding losses, the leakage-inductance ratio, and a bias-power to maximum-output-power ratio. For example, an overall transformer efficiency of 0.9 is a good estimate based on 3.5% leakage inductance, 5% core and winding loss, and 0.5% bias power. Adjust these estimates as needed based on each specific application.

$$R_{CS} = \frac{0.33\ V \times 9.5 \times \sqrt{0.9}}{2 \times 3\ A} = 0.496\ \Omega$$

$V_{CCR(min)}$ is the minimum CC regulation factor and device parameter = 0.318 V.

The standard value of the current sense resistor selected is $R_{CS}$ = 0.5 Ω; a series combination of resistors is used to easily adjust values and pass single point failure test.

For primary inductance calculation, determine the transformer primary peak current using Equation 8. Peak primary current is the maximum current-sense threshold divided by the current-sense resistance.

$$I_{PP(max)} = \frac{V_{CST(max)}}{R_{CS}} \tag{8}$$

$$I_{PP(max)} = \frac{0.81\ V}{0.5\ \Omega} = 1.62\ A$$

$$I_{PP(nom)} = \frac{0.773\ V}{0.5\ \Omega} = 1.546\ A$$

Based on the primary peak current, the actual output current during constant current output can be calculated using Equation 9:

$$I_{OCC\_act} = \frac{I_{PP(nom)} \times N_{PS} \times D_{MAGCC}}{2} \tag{9}$$

$$I_{OCC\_act} = \frac{1.546\ A \times 9.5 \times 0.425}{2} = 3.121\ A$$

The primary transformer inductance is calculated using the standard energy storage equation for flyback transformers. Primary current, maximum switching frequency, output voltage, current targets, and transformer power losses are included in Equation 10:

$$L_P = \frac{2 \times \left(V_{OCV} + V_F + V_{OCBC}\right) \times I_{OCC\_act}}{\eta_{XFMR} \times I_{PP(nom)}^2 \times f_{MAX}} \tag{10}$$

$$L_P = \frac{2 \times (12\ V + 0.4\ V + 0\ V) \times 3.121}{0.9 \times 1.546\ A^2 \times 100\ kHz} = 359.82\ \mu H$$

The actual primary inductance selected is $L_P$ = 360 µH.

$N_{AS}$ is determined by the lowest target operating output voltage while in CC regulation and by the VDD UVLO turn-off threshold of the UCC28740. For this design, both the output rails are rated for a 12-V output. Thus, transformer auxiliary to secondary turns ratio, $N_{AS}$ = 1.

### 2.2.3 Transformer Parameter Calculations: Primary and Secondary RMS Currents

With the primary inductance selected, the actual maximum nominal switching frequency is determined by Equation 11:

$$f_{MAX} = \frac{N_{PS} \times D_{MAGCC} \times \left(V_{OCV} + V_F\right)}{L_P \times I_{PP(nom)}} \tag{11}$$

$$f_{MAX} = \frac{9.5 \times 0.425 \times \left(12 + 0.4\right)}{360\ \mu H \times 1.546} = 89.95\ kHz$$

The maximum switching period is given by Equation 12:

$$t_{SW} = \frac{1}{f_{MAX}} = \frac{1}{89.95\ kHz} = 11.117\ \mu s \tag{12}$$

The actual maximum on-time is given by Equation 13:

$$t_{ON(max)} = \frac{I_{PP(nom)} \times L_P}{V_{IN(min)}} \tag{13}$$

$$t_{ON(max)} = \frac{1.546 \times 360\ \mu H}{100} = 5.566\ \mu s$$

The maximum duty cycle of operation $D_{MAX}$ is calculated using Equation 14:

$$D_{MAX} = \frac{t_{ON(max)}}{t_{SW}} = \frac{5.566\ \mu s}{11.117\ \mu s} = 0.501 \tag{14}$$

Once peak primary current is known, the transformer primary RMS current ($I_{PRMS}$) is calculated using Equation 15:

$$I_{PRI\_RMS} = I_{PP(nom)} \times \sqrt{\frac{D_{MAX}}{3}} \tag{15}$$

$$I_{PRI\_RMS} = 1.546\ A \times \sqrt{\frac{0.501}{3}} = 0.632\ A$$

The transformer secondary peak current and RMS current are given by Equation 16 and Equation 17, respectively:

$$I_{SP(max)} = I_{PP(nom)} \times N_{PS} = 1.546\ A \times 9.5 = 14.687\ A \tag{16}$$

$$I_{SEC\_RMS} = I_{SP(max)} \times \sqrt{\frac{D_{MAG}}{3}} \tag{17}$$

$$I_{SEC\_RMS} = 14.687\ A \times \sqrt{\frac{0.425}{3}} = 5.528\ A$$

Based on these calculations, a Würth Electronik transformer was designed for this application (part number 750343306), which has the following specifications:

- $N_{PS}$ = 9.5
- $N_{PA}$ = 9.5
- $L_P$ = 360 µH
- $L_{LK}$ = 8 µH ($L_{LK}$ denotes the leakage inductance)

### 2.2.4 Main Switching Power MOSFET Selection

The drain-to-source RMS current, $I_{DS\_RMS}$, through switching FET is calculated as Equation 18:

$$I_{DS\_RMS} = \frac{I_{PP(max)}}{\sqrt{3}} \times \sqrt{D_{MAX}} \tag{18}$$

$$I_{DS\_RMS} = \frac{1.62}{\sqrt{3}} \times \sqrt{0.501} = 0.662 \text{ A}$$

It is recommended to select a MOSFET with at least five times the calculated value. So, ideal $I_{DS\_RMS}$ = 3.31 A. Estimate the maximum voltage across with FET using Equation 4. Considering a derating of 10%, the voltage rating of MOSFET should be 800-V DC. The IPU80R1K0CE MOSFET of 800 V and 5.7 A is selected for this design.

For thermal dissipation, a standard TO-220 vertical heat sink from "Advanced Thermal Solutions Inc." with part number ATS-PCBT1093, is used. The heat sink is cut at 16mm height from board level so that the total height of the TIDA-00709 board does not exceed 17 mm. It is further attached to the MOSFET with a thermally conductive, electrically insulating double sided tape. Board temperature is measured with this arrangement and shown in Figure 24 and Figure 25.

The recommended clamping voltage on the drain is calculated using Equation 19:

$$V_{DRAIN\_CLAMP} = 0.95 \times V_{DS} - \left(V_{IN(max)} + N_{PS} \times \left(V_{OCV} + V_F + V_{OCBC}\right)\right) \tag{19}$$

$$V_{DRAIN\_CLAMP} = 0.9 \times 800 \text{ V} - \left(400 \text{ V} + 9.5 \times \left(12 + 0.4 \text{ V}\right)\right) = 202.2 \text{ V}$$

### 2.2.5 Rectifying Diode and Synchronous Rectification MOSFET Selection

Calculate the secondary output diode or synchronous rectifier FET reverse voltage or blocking voltage needed ($V_{DIODE\_BLOCKING}$) with Equation 20:

$$V_{DIODE\_BLOCKING} = \frac{V_{IN(max)}}{N_{PS}} + V_{OCV} + V_{OCBC} + V_F \tag{20}$$

$$V_{DIODE\_BLOCKING} = \frac{400 \text{ V}}{9.5} + 12 \text{ V} + 0 \text{ V} + 0.4 = 54.51 \text{ V}$$

The required minimum output current is $I_{DOUT} = I_{DS\_RMS}$ = 3.31 A.

A synchronous rectifier FET is recommended for low-power loss and high-efficiency needs. This TI Design uses the CSD19531 by TI to optimize the on-state losses.

### 2.2.6 Select Output Capacitors

For this design, the output capacitor ($C_{OUT}$) is selected to have ≤1% ripple of all the outputs with an operating frequency of 100 kHz. Calculate the value of the output capacitor for both the outputs using Equation 21:

$$C_{OUT} > \frac{I_{OUT}}{f \times V_{RIPPLE}} \tag{21}$$

$$C_{OUT} > \frac{3 \text{ A}}{100 \text{ kHz} \times 0.1 \text{ V}} = 300 \text{ µF}$$

Considering the allowable output ripple of 100 mV, the ESR of the capacitor must be as per Equation 22:

$$ESR = \frac{V_{OUT\_RIPPLE}}{I_{SEC(max)}} = \frac{100 \text{ mW}}{14.687 \text{ A}} = 6.81 \text{ m}\Omega \tag{22}$$

$$I_{COUT\_RMS} = \sqrt{\left(I_{SEC\_RMS}\right)^2 - \left(I_{OUT}\right)^2} \tag{23}$$

$$I_{COUT\_RMS} = \sqrt{(5.528\ A)^2 - (I_{OUT})^2} = 4.643\ A$$

A 470-µF×2, 25-V capacitor was selected on the output.

### 2.2.7 Capacitance on VDD Pin

The capacitance on VDD needs to supply the device operating current until the output of the converter reaches the target minimum operating voltage in CC regulation.

The capacitance on VDD must supply the primary-side operating current used during start-up. Equation 24 determines the value of $C_{VDD}$:

$$C_{VDD} > \frac{\left(I_{RUN} + Q_G \times f_{SW(max)}\right) \times \left(\frac{C_{OUT} \times V_{OCC}}{I_{OCC}}\right)}{V_{VDD(on)} - \left(V_{VDD(off)} + 1\ V\right)} \quad (24)$$

$$C_{VDD} > \frac{(2.65\ mA + 31\ nC \times 89.95\ kHz) \times \left(\frac{940\ \mu F \times 12\ V}{3\ A}\right)}{23\ V - (8.15\ V + 1\ V)} = 2.2\ \mu F$$

To address the start-up of the converter for heavy capacitive loads (which is around 8000 to 10,000 µF), a higher value of $C_{VDD}$ is needed. This TI Design uses a 10-µF capacitor.

### 2.2.8 Open-Loop Voltage Regulation VS Pin Resistor Divider, Line Compensation Resistor

The resistor divider at the VS pin determines the output voltage regulation point of the flyback converter. The high-side divider resistor ($R_{S1}$) determines the line voltage at which the controller enables continuous DRV operation. $R_{S1}$ is initially determined based on the transformer auxiliary-to-primary turns ratio and desired input voltage operating threshold as per Equation 25:

$$R_{S1} = \frac{V_{IN(run)}}{N_{PA} \times I_{VSL(run)}} \quad (25)$$

where:

- $N_{PA}$ is the transformer primary to auxiliary turns ratio
- $V_{IN(run)}$ is the DC voltage to enable turnon of the controller
- $I_{VSL(run)}$ is the run threshold for the current pulled out of the VS pin during the switch on-time [see Electrical Characteristics of the UCC28740 datasheet (SLUSBF3)]

$$R_{S1} = \frac{100\ V}{9.5 \times 225\ \mu A} = 46.78\ k\Omega$$

A standard resistor of 46.4 kΩ is selected for this design.

The low-side VS pin resistor is selected based on the desired $V_{OUT}$ regulation voltage in open-loop conditions and sets the maximum allowable voltage during open-loop conditions. Use Equation 26 to determine its value:

$$R_{S2} = \frac{R_{S1} \times V_{OVPTH}}{N_{AS} \times \left((V_{OCV} + V_F) - V_{OVPTH}\right)} \quad (26)$$

where:

- $V_{OV}$ is the maximum allowable peak voltage at the converter output
- $V_F$ is the output-rectifier forward drop at near-zero current
- $N_{AS}$ is the transformer auxiliary-to-secondary turns ratio
- $R_{S1}$ is the VS divider high-side resistance
- $V_{OVPTH}$ is the overvoltage detection threshold at the VS input [see Electrical Characteristics of the UCC28740 datasheet (SLUSBF3)]

$$R_{S2} = \frac{46.4\ k\Omega \times 4.6}{1 \times \left((12.6\ V + 0.4\ V) - 4.6\right)} = 25.41\ k\Omega$$

A standard resistor of 24.9 kΩ is selected.

The UCC28740 maintains a tight CC regulation over varying input lines by using the line-compensation feature. The line-compensation resistor ($R_{LC}$) value is determined by current flowing in $R_{S1}$ and the total internal gate drive and external MOSFET turnoff delay. Assuming an internal delay of 50 ns in the UCC28740, the value of $R_{LC}$ is calculated with Equation 27:

$$R_{LC} = \frac{K_{LC} \times R_{S1} \times R_{CS} \times T_D \times N_{PA}}{L_P} \quad (27)$$

where:

- $R_{CS}$ is the current-sense resistor value
- $t_D$ is the current-sense delay including MOSFET turnoff delay, add ≈ 50 ns to MOSFET delay
- $N_{PA}$ is the transformer primary-to-auxiliary turns ratio
- $L_P$ is the transformer primary inductance
- $K_{LC}$ is a current-scaling constant [see Electrical Characteristics of the UCC28740 datasheet (SLUSBF3)]

$$R_{LC} = \frac{25 \times 46.4\ k\Omega \times 0.5\ \Omega \times (72 + 50)\ ns \times 9.5}{360\ \mu H} = 1.867\ k\Omega$$

A standard 1.87-kΩ resistor is selected for this design.

### 2.2.9 Feedback Elements

The output voltage is set through the sense-network resistors $R_{FB1}$ and $R_{FB2}$. The design spreadsheet has all relevant equations to characterize the optocoupler and its adjustments of the initial values to accommodate variations of the UCC28740. Also using the design sheet, the shunt-regulator parameters can be optimized for overall system performance. The shunt-regulator compensation network, ZFB, is determined using well-established design techniques for control-loop stability. Typically, a type-II compensation network is used.

## *2.3 Synchronous Rectifier Controller Component Design*

The UCC24636 SR controller is targeted for flyback converters operating in DCM and TM. The control method to determine SR on-time is based on the volt-second balance principle of primary and secondary conduction volt-second product. In converters operating in DCM and TM, the secondary current always returns to zero in each cycle. The inductor charge voltage and time product is equal to the discharge voltage and time product. The device uses internal current ramp emulators to predict the proper SR on-time based on voltage and time information on the VPC and VSC pins.

The design procedure for selecting the component circuitry for use with the UCC24636 is detailed in the following sections.

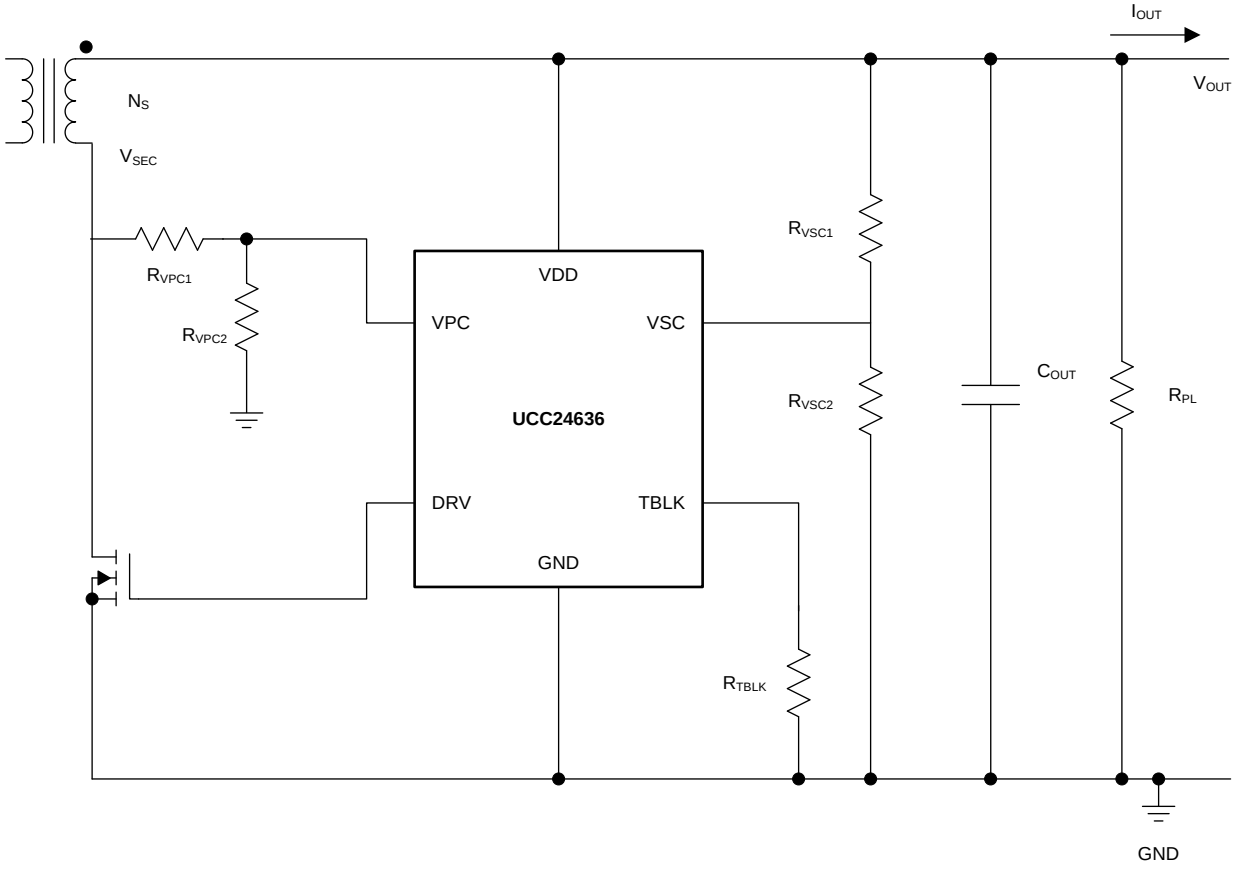





**Figure 4. UCC24636 Circuit Component Design**

### 2.3.1 VPC Pin Elements

Determining the VPC and VSC divider resistors is based on the operating voltage ranges of the converter and $Ratio_{VPC-VSC}$ gain ratio. Referring to Figure 4, Equation 28 determines the VPC divider values. For R2, a value of 10 kΩ is recommended for minimal impact on time delay and low-resistor dissipation. A higher R2 value reduces resistor divider dissipation but may increase the DRV turnon delay due to the time constant of ≈2-pF pin capacitance and divider resistance. A lower R2 value can be used with the trade-off of higher dissipation in the resistor divider. A factor of 10% over the VPC threshold, $V_{VPCEN}$, is shown in Equation 28 for the design margin.

For minimal power dissipation: R2 = 10 kΩ

$$R_{VPC1} = \frac{\left[\left(\frac{V_{IN(min)}}{N_{PS}} + V_{OUT(min)}\right) - V_{VPCEN} \times 1.1\right] \times R_{VPC2}}{V_{VPCEN} \times 1.1} \quad (28)$$

where:

- $V_{IN(min)}$ is the converter minimum primary bulk capacitor voltage
- $V_{OUT(min)}$ is the minimum converter output voltage in normal operation
- $V_{VPCEN}$ is the VPC enable threshold, use the specified maximum value
- $N_{PS}$ is the transformer primary-to-secondary turns ratio

$$R_{VPC1} = \frac{\left[\left(\frac{100}{9.5} + 11.4\right) - 0.4 \times 1.1\right] \times 10\ k\Omega}{0.4 \times 1.1} = 488.325\ k\Omega$$

In order to satisfy the $V_{VPC}$ limits, a standard resistor of 464 kΩ is selected.

The operating voltage range on the VPC pin should be within 0.45 to 2.2 V. Referring to Figure 4, if $V_{VPC}$ is greater than 2.3 V, the dynamic range is exceeded and $Ratio_{VPC\_VSC}$ is reduced; in this condition, the DRV on-time is less than expected. If $V_{VPC}$ is greater than 2.6 V for 500 ns, a fault is generated and DRV is disabled for the cycle. To ensure the maximum voltage is within range, confirm with Equation 29:

$$V_{VPC(max)} = \frac{\left(\frac{V_{IN(max)}}{N_{PS}} + V_{OUT(max)}\right) \times R_{VPC2}}{R_{VPC1} + R_{VPC2}} \quad (29)$$

where:

- $V_{IN(max)}$ is the converter maximum primary bulk capacitor voltage
- $V_{OUT(max)}$ is the maximum converter output voltage at OVP
- $N_{PS}$ is the transformer primary-to-secondary turns ratio

$$V_{VPC(max)} = \frac{\left(\frac{400}{9.5} + 12.6\right) \times 10\ k\Omega}{10\ k\Omega + 464\ k\Omega}$$

$$V_{VPC(min)} = \frac{\left(\frac{400}{9.5} + 11.4\right) \times 10\ k\Omega}{10\ k\Omega + 464\ k\Omega} = 0.463\ V$$

Therefore, $V_{VPC}$ is within the recommended range of 0.45 to 2.2 V.

### 2.3.2 VSC Pin Elements

The program voltage on the VSC pin is determined by the VPC divider ratio and the device's parameter, $Ratio_{VPC\_VSC}$. The current emulator ramp gain is higher on the VPC pin by the multiple $Ratio_{VPC\_VSC}$, so the VSC resistor divider ratio is reduced by the same $Ratio_{VPC\_VSC}$ accordingly. Determine the VSC divider resistors using Equation 30 . To minimize resistor divider dissipation, the recommended range for $R_{VSC2}$ is 25 to 50 kΩ. Higher $R_{VSC2}$ values results in increasing offset due to VSC input current, $I_{VSC}$. Lower $R_{VSC2}$ values increases the resistor divider dissipation. To ensure DRV turns off slightly before the secondary current reaches zero, 10% margin is shown for initial values.

A standard resistor of 37.4 kΩ is selected for $R_{VSC2}$.

$$R_{VSC1} = \left[ \left( \frac{\frac{R_{VPC1} + R_{VPC2}}{R_{VPC2}}}{Ratio_{VPC\_VSC} \times 1.1} \right) - 1 \right] \times R_{VSC2} \tag{30}$$

where:

- $Ratio_{VPC\_VSC}$ is the device parameter VPC and VSC gain ratio, use a value of 4.15

$$R_{VSC1} = \left[ \left( \frac{\frac{464\ k\Omega + 10\ k\Omega}{10\ k\Omega}}{4.15 \times 1.1} \right) - 1 \right] \times 37.4\ k\Omega = 350.94\ k\Omega$$

A standard resistor of 348 kΩ is selected for $R_{VSC1}$.

The operating voltage range on the VSC pin should be from 0.3 to 2.2 V. Referring to Figure 4, if $V_{VSC}$ is greater than 2.3 V, the dynamic range is exceeded and $Ratio_{VPC\_VSC}$ is increased; in this condition, the DRV on-time is more than expected. To ensure the VSC voltage is within range, confirm with Equation 31 and Equation 32.

$$\frac{R_{VSC2}}{R_{VSC1} + R_{VSC2}} \times V_{OUT(max)} \leq 2.2\ V \tag{31}$$

$$\frac{R_{VSC2}}{R_{VSC1} + R_{VSC2}} \times V_{OUT(min)} \geq 0.3\ V \tag{32}$$

where:

- $V_{OUT(max)}$ is the maximum converter output operating voltage of the voltage at OVP
- $V_{OUT(min)}$ is the maximum converter output operating voltage of the SR controller

$$V_{SC(max)} = \frac{37.4\ k\Omega}{37.4\ k\Omega + 348\ k\Omega} \times 12.6 = 1.223\ V$$

$$V_{SC(min)} = \frac{37.4\ k\Omega}{37.4\ k\Omega + 348\ k\Omega} \times 11.4 = 1.106\ V$$

Therefore, $V_{VSC}$ is within the recommended range of 0.3 to 2.2 V.

### 2.3.3 tBLK Input

The blanking time is set with resistor $R_{TBLK}$. Select the blanking time to meet the following criteria based on minimum primary on-time at high line as per Equation 33

$$t_{VPC-BLK} = \left(t_{PRI} \times 0.85\right) - 120\ ns \tag{33}$$

where:

- $t_{VPC\_BLK}$ is the target blanking time

$$t_{VPC-BLK} = \left(660\ ns \times 0.85\right) - 120\ ns = 441\ ns$$

To determine the resistor value for $t_{VPC\_BLK}$, use Equation 34 to select from a range of 200 ns to 1 µs.

$$R_{TBLK} = \frac{t_{VPC-BLK} - 100\ ns}{18\ pF} \tag{34}$$

$$R_{TBLK} = \frac{441\ ns - 100\ ns}{18\ nF} = 18.94\ k\Omega$$

A standard resistor of 18 kΩ is selected.

## 2.4 Input Bulk Capacitance and Minimum Bulk Voltage

The value of the bulk capacitor used determines the minimum input voltage for the flyback converter. This in turn determines the primary-to-secondary turn determines the primary-to-secondary turns ratio of the transformer.

The input capacitance value, $C_{BULK}$, is based on the maximum load power, converter efficiency, minimum operational input voltage, and minimal operational input frequency.

The maximum AC input power is determined by the $V_{OCV}$, $I_{OCC}$, and full load efficiency targets.

The primary output is:

$$V_{OUT} = V_{OCV} = 12\ V$$

The converter is for 3 A of maximum output current on the primary output and is designed to limit the current at 3 A for overload conditions. So, $I_{OCC}$ = 3 A.

The total maximum output power needed is:

$$P_{OUT} = V_{OUT} \times I_{OCC} \tag{35}$$

$$P_{OUT} = 12 \times 3 = 36\ W$$

To calculate component specifications, the minimum targeted efficiency is considered 90%. For input power:

$$P_{IN} = \left(\frac{P_{OUT}}{Efficiency}\right) = \frac{36}{0.9} = 40\ W \tag{36}$$

Equation 37 provides an accurate solution for input capacitance needed to achieve a minimum bulk valley voltage target, $V_{BULK(min)}$. Alternately, if a given capacitance value is prescribed, one can calculate the $V_{BULK(min)}$ expected for that capacitance.

$$C_{BULK} = \frac{2 \times P_{IN} \times \left(0.25 + \frac{1}{2\pi} \times \arcsin\left(\frac{V_{BULK(min)}}{\sqrt{2} \times V_{IN(min)}}\right)\right)}{\left(2 \times V_{IN(min)}^{2} - V_{BULK(min)}^{2}\right) \times f_{LINE}} \tag{37}$$

The minimum recommended valley voltage on the input bulk capacitor is taken as 60% of the peak of the minimum AC voltage.

$$V_{BULK(min)} = V_{IN(min)} \times \sqrt{2} \times 0.6 \tag{38}$$

$$V_{BULK(min)} = 85 \times \sqrt{2} \times 0.6 = 72.14 \text{ V}$$

$$C_{BULK} \geq \frac{2 \times 40 \text{ W} \times \left(0.25 + \frac{1}{2\pi} \times \arcsin\left(\frac{72.14 \text{ V}}{\sqrt{2} \times 85 \text{ V}}\right)\right)}{\left(2 \times 85 \text{ V}^2 - 72.14 \text{ V}^2\right) \times 50} \geq 60.99 \text{ µF}$$

To meet the needs of hold-up time, bulk capacitance is selected higher than the calculated value. The bulk capacitor selected for this TI Design is 56 µF × 2 = 112 µF.

Using Equation 37 and $C_{BULK}$ = 112 µF, $V_{BULK(min)}$ = 94 V.

To calculate input capacitor charge time, ($t_{CH}$), based on $V_{BULK(min)}$:

$$t_{CH} = \frac{1 - \sin^{-1}\left(\frac{\sqrt{2} \times V_{IN(min)} - V_{BULK(min)}}{\sqrt{2} \times V_{IN(min)}}\right)}{4 \times 50} \tag{39}$$

$$t_{CH} = \frac{1 - \sin^{-1}\left(\frac{\sqrt{2} \times 85 \text{ V} - 94 \text{ V}}{\sqrt{2} \times 85 \text{ V}}\right)}{4 \times 50} = 3.9 \text{ ms}$$

To calculate the longest period of the rectified line voltage (full bridge rectification):

$$t_{RL} = \frac{1}{2 \times 47} = 10.6 \text{ ms} \tag{40}$$

The minimum input capacitor RMS ripple current rating is given by Equation 41:

$$I_{CINripple} = \frac{C_{BULK} \times \left(\sqrt{2} \times V_{IN(min)} - V_{BULK(min)}\right)}{t_{RL} - t_{CH}} \times \sqrt{3} \tag{41}$$

$$I_{CINripple} = \frac{112 \text{ µF} \times \left(\sqrt{2} \times 85 \text{ V} - 94 \text{ V}\right)}{10.6 \text{ ms} - 3.9 \text{ ms}} \times \sqrt{3} = 758.8 \text{ mA}$$

This TI Design uses two capacitors (400BXW56MEFR12.5X30) with a 400-V rating and 12000 hours of life at 105°C.

## 2.5 Bridge Rectifier and Fuse Selection

To calculate peak AC input current:

$$I_{PKAC} = \left( \frac{2 \times \frac{P_{IN}}{V_{BULK(min)}}}{\sqrt{\frac{t_{CH}}{t_{RL}}}} \right) \quad (42)$$

$$I_{PKAC} = \left( \frac{2 \times \frac{40\ W}{94\ W}}{\sqrt{\frac{3.9\ ms}{21.27\ ms}}} \right) = 1.987\ A$$

The bridge rectifier current rating is determined by current at minimum bulk voltage:

$$I_{DAPK} = \left( \frac{2 \times P_{IN}}{V_{BULK(min)}} \right) \quad (43)$$

$$I_{DAPK} = \left( \frac{2 \times 40\ W}{94\ V} \right) = 0.851\ A$$

In order to reduce the overall cost, this TI Design uses four 1N4007 diodes to construct the bridge rectifier. The bridge rectifier losses are determined by the average bridge rectifier current. The average bridge rectifier current is highest at the minimum AC line voltage and is determined by:

$$I_{DA} = \left( \frac{P_{IN}}{\frac{2}{\pi} \times \sqrt{2} \times V_{IN(min)}} \right) \quad (44)$$

$$I_{DA} = \left( \frac{40\ W}{\frac{2}{\pi} \times \sqrt{2} \times 85\ V} \right) = 0.52\ A$$

Forward voltage drop of bridge rectifier diode, VFDA = 1.1 V.

The estimated power dissipated in bridge rectifier diode ($P_{DA}$) is:

$$P_{DA} = V_{DA} \times I_{DA} = 2 \times 1.1 \times 0.52 = 1.144\ W \quad (45)$$

# 3 Getting Started Hardware

## 3.1 Test Equipment Needed to Validate Board

- Isolated AC source - 85- to 265-V / DC source: 0- to 450-V DC rated
- Digital oscilloscope
- 6 ½ digit multimeter (×4)
- Electronic or resistive load (×2)

## 3.2 Test Conditions

### Input voltage range

The source must be capable of varying between a $V_{INDC}$ of 100- to 450-V DC or 85- to 265-V AC. Set the input current limit to 0.8 A.

### Output

Connect an electronic load capable of 20 V to both outputs. The load must be variable and capable of 3 A for $V_{OUT1}$ and 0.3 A for $V_{OUT2}$. A rheostat or resistive decade box can also be used in place of an electronic load.

## 3.3 Test Procedure

1. For DC input, connect the source at the input terminal (Pin 1 and Pin 2 of connector J1) of the reference board with Pin 2 being the primary ground reference. For AC input, connect the source at input terminal ,connector J5.
2. Connect the following output terminals:
   - Connector J2 details: Pin 1,2 for 12 V/2.75 A, Pin 1 is the isolated secondary reference. This output is split into two—one independently overload protected through an eFuse and another directly without independent overload protection. Load the rail through eFuse (max load 12 V/1.5 A) with Pin 3 being the output of eFuse.
   - Connector J4 details: Pin 1,2 for 12 V/0.25 A, Pin 1 is primary referred ground.
3. Set and maintain a minimum load of about 10 mA.
4. Gradually increase the input voltage from 0 V to a turnon voltage of 100 V.
5. Turn on the load to draw current from the output terminals of the converter.
6. Observe the startup conditions and smooth switching waveforms.

# 4 Test Results

The test results are divided into multiple sections that cover the steady state performance measurements, functional performance waveforms and test data, transient performance waveforms and thermal measurements.

## 4.1 Performance Data

### 4.1.1 Efficiency and Regulation With Load Variation (DC Input)

Table 3 shows the efficiency and regulation performance data at 120-V DC.

**Table 3. Efficiency and Regulation at 120-V DC**

| LOAD % | $I_{INDC}$ (A) | $P_{INDC}$ (W) | $V_{OUT1}$ (V) | $I_{OUT1}$ (A) | $V_{OUT2}$ (V) | $I_{OUT2}$ (A) | $P_{OUT}$ (W) | EFF (%) | % REG $V_{OUT1}$ | % REG $V_{OUT2}$ | PWR LOSS (W) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0.000786 | 0.0943 | 12.42 | — | 13.53 | — | 0.00 | 0.00 | 2.44 | 13.13 | 0.09 |
| 10 | 0.03 | 3.9800 | 12.14 | 0.27 | 11.90 | 0.03 | 3.60 | 90.60 | 0.09 | –0.50 | 0.37 |
| 25 | 0.08 | 9.9200 | 12.14 | 0.68 | 11.94 | 0.07 | 9.06 | 91.38 | 0.06 | –0.19 | 0.85 |
| 50 | 0.17 | 20.1400 | 12.13 | 1.38 | 11.96 | 0.13 | 18.38 | 91.24 | 0.00 | 0.04 | 1.76 |
| 75 | 0.25 | 30.1200 | 12.12 | 2.06 | 11.98 | 0.21 | 27.51 | 91.33 | –0.05 | 0.21 | 2.61 |
| 100 | 0.33 | 39.2700 | 12.12 | 2.73 | 12.01 | 0.24 | 35.94 | 91.53 | –0.10 | 0.44 | 3.33 |

Table 4 shows the efficiency and regulation performance data at a 165-V DC input.

**Table 4. Efficiency and Regulation at 165-V DC**

| LOAD % | $I_{INDC}$ (A) | $P_{INDC}$ (W) | $V_{OUT1}$ (V) | $I_{OUT1}$ (A) | $V_{OUT2}$ (V) | $I_{OUT2}$ (A) | $P_{OUT}$ (W) | EFF (%) | % REG $V_{OUT1}$ | % REG $V_{OUT2}$ | PWR LOSS (W) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0.00058 | 0.0957 | 12.43 | — | 13.54 | — | 0.00 | 0.00 | 2.49 | 13.61 | 0.10 |
| 10 | 0.02 | 4.0000 | 12.14 | 0.27 | 11.87 | 0.03 | 3.60 | 90.13 | 0.09 | –0.48 | 0.39 |
| 25 | 0.06 | 9.8900 | 12.13 | 0.68 | 11.90 | 0.07 | 9.05 | 91.52 | 0.06 | –0.17 | 0.84 |
| 50 | 0.12 | 20.0100 | 12.13 | 1.38 | 11.93 | 0.13 | 18.34 | 91.66 | 0.00 | 0.05 | 1.67 |
| 75 | 0.18 | 29.9500 | 12.12 | 2.06 | 11.95 | 0.21 | 27.50 | 91.81 | –0.05 | 0.22 | 2.45 |
| 100 | 0.24 | 39.1200 | 12.12 | 2.70 | 11.97 | 0.27 | 35.97 | 91.95 | –0.09 | 0.38 | 3.15 |

Table 5 shows the efficiency and regulation performance data at a 250-V DC input voltage.

**Table 5. Efficiency and Regulation at 250-V DC**

| LOAD % | $I_{INDC}$ (A) | $P_{INDC}$ (W) | $V_{OUT1}$ (V) | $I_{OUT1}$ (A) | $V_{OUT2}$ (V) | $I_{OUT2}$ (A) | $P_{OUT}$ (W) | EFF (%) | % REG $V_{OUT1}$ | % REG $V_{OUT2}$ | PWR LOSS (W) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0.000387 | 0.0968 | 12.41 | — | 13.60 | — | 0.00 | 0.00 | 2.32 | 14.38 | 0.10 |
| 10 | 0.02 | 4.0500 | 12.14 | 0.27 | 11.85 | 0.03 | 3.61 | 89.15 | 0.09 | –0.31 | 0.44 |
| 25 | 0.04 | 9.9100 | 12.13 | 0.68 | 11.87 | 0.07 | 9.05 | 91.39 | 0.06 | –0.20 | 0.85 |
| 50 | 0.08 | 19.9600 | 12.13 | 1.38 | 11.88 | 0.13 | 18.33 | 91.82 | 0.01 | –0.07 | 1.63 |
| 75 | 0.12 | 29.8800 | 12.12 | 2.06 | 11.91 | 0.21 | 27.48 | 91.99 | –0.06 | 0.19 | 2.39 |
| 100 | 0.16 | 39.4500 | 12.11 | 2.73 | 11.94 | 0.27 | 36.37 | 92.20 | –0.11 | 0.39 | 3.08 |

Table 6 shows the efficiency and regulation performance data at 325-VDC input voltage.

**Table 6. Efficiency and Regulation at 325-V DC**

| LOAD % | $I_{INDC}$ (A) | $P_{INDC}$ (W) | $V_{OUT1}$ (V) | $I_{OUT1}$ (A) | $V_{OUT2}$ (V) | $I_{OUT2}$ (A) | $P_{OUT}$ (W) | EFF (%) | % REG $V_{OUT1}$ | % REG $V_{OUT2}$ | PWR LOSS (W) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0.000303 | 0.0985 | 12.41 | — | 13.64 | — | 0.00 | 0.00 | 2.35 | 14.82 | 0.10 |
| 10 | 0.01 | 4.1100 | 12.14 | 0.27 | 11.85 | 0.03 | 3.61 | 87.83 | 0.09 | –0.26 | 0.50 |
| 25 | 0.03 | 9.9600 | 12.14 | 0.68 | 11.85 | 0.07 | 9.05 | 90.90 | 0.06 | –019 | 0.91 |
| 50 | 0.06 | 20.0000 | 12.13 | 1.38 | 11.88 | 0.13 | 18.33 | 91.65 | 0.00 | 0.00 | 1.67 |
| 75 | 0.09 | 29.9700 | 12.12 | 2.07 | 11.89 | 0.21 | 27.50 | 91.78 | –0.05 | 0.15 | 2.46 |
| 100 | 0.12 | 39.6100 | 12.12 | 2.73 | 11.91 | 0.27 | 36.38 | 91.83 | –0.10 | 0.30 | 3.24 |

Table 7 shows the efficiency and regulation performance data at a 400-V DC input voltage.

**Table 7. Efficiency and Regulation at 400-V DC**

| LOAD % | $I_{INDC}$ (A) | $P_{INDC}$ (W) | $V_{OUT1}$ (V) | $I_{OUT1}$ (A) | $V_{OUT2}$ (V) | $I_{OUT2}$ (A) | $P_{OUT}$ (W) | EFF (%) | % REG $V_{OUT1}$ | % REG $V_{OUT2}$ | PWR LOSS (W) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0.0002526 | 0.101 | 12.42 | — | 13.67 | — | 0.00 | 0.00 | 2.44 | 15.02 | 0.10 |
| 10 | 0.01 | 4.160 | 12.14 | 0.27 | 11.84 | 0.03 | 3.60 | 86.65 | 0.07 | –0.32 | 0.56 |
| 25 | 0.03 | 10.040 | 12.14 | 0.68 | 11.86 | 0.07 | 9.06 | 90.24 | 0.07 | –0.15 | 0.98 |
| 50 | 0.05 | 20.080 | 12.13 | 1.38 | 11.88 | 0.13 | 18.34 | 91.33 | 0.01 | 0.02 | 1.74 |
| 75 | 0.08 | 30.100 | 12.12 | 2.07 | 11.90 | 0.21 | 27.51 | 91.41 | –0.04 | 0.12 | 2.58 |
| 100 | 0.10 | 39.760 | 12.12 | 2.73 | 11.92 | 0.27 | 36.38 | 91.51 | –0.10 | 0.34 | 3.38 |

Table 8 shows the efficiency and regulation performance at a 430-V DC input voltage.

**Table 8. Efficiency and Regulation at 430-V DC**

| LOAD % | $I_{INDC}$ (A) | $P_{INDC}$ (W) | $V_{OUT1}$ (V) | $I_{OUT1}$ (A) | $V_{OUT2}$ (V) | $I_{OUT2}$ (A) | $P_{OUT}$ (W) | EFF (%) | % REG $V_{OUT1}$ | % REG $V_{OUT2}$ | PWR LOSS (W) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0.000245 | 0.105 | 12.43 | — | 13.67 | — | 0.00 | 0.00 | 2.50 | 15.00 | 0.11 |
| 10 | 0.01 | 4.360 | 12.14 | 0.28 | 11.85 | 0.03 | 3.79 | 86.88 | 0.08 | –0.29 | 0.57 |
| 25 | 0.02 | 10.060 | 12.14 | 0.68 | 11.87 | 0.07 | 9.07 | 90.18 | 0.06 | –0.16 | 0.99 |
| 50 | 0.05 | 20.170 | 12.13 | 1.39 | 11.88 | 0.13 | 18.39 | 91.18 | 0.01 | –0.06 | 1.78 |
| 75 | 0.07 | 30.140 | 12.12 | 2.07 | 11.91 | 0.21 | 27.51 | 91.27 | –0.04 | 0.21 | 2.63 |
| 100 | 0.09 | 39.710 | 12.12 | 2.73 | 11.92 | 0.27 | 36.30 | 91.42 | –0.11 | 0.30 | 3.41 |

Table 9 shows the line regulation of both the outputs over the input voltage range for full load.

**Table 9. Line Regulation at Full Load**

| $V_{INDC}$ (V) | $V_{OUT1}$ (V) | $V_{OUT2}$ (V) | % REG $V_{OUT1}$ | % REG $V_{OUT2}$ |
|---|---|---|---|---|
| 120 | 12.115 | 12.012 | 0.000 | 0.568 |
| 165 | 12.116 | 11.967 | 0.008 | 0.191 |
| 250 | 12.114 | 11.935 | –0.008 | –0.077 |
| 325 | 12.115 | 11.911 | 0.000 | –0.278 |
| 400 | 12.115 | 11.920 | 0.000 | –0.202 |
| 430 | 12.115 | 11.920 | 0.000 | –0.202 |

Table 10 and Table 11 show the cross reference data for the 12-V_ISO/2.75-A rail and 12-V/0.25-A rail, respectively. The cross reference data for each rail was noted while the other output was at full load with a 400-V DC input voltage.

**Table 10. Cross Regulation for $V_{OUT1}$ (12 V_ISO/2.75 A) With Full Load on $V_{OUT2}$ (12 V/0.25 A)**

| LOAD % ON $V_{OUT1}$ | $V_{OUT1}$ (V) | $I_{OUT1}$ (A) | % REG $V_{OUT1}$ |
|---|---|---|---|
| 10 | 12.16 | 0.28 | 1.33 |
| 25 | 12.13 | 0.68 | 1.11 |
| 50 | 12.12 | 1.39 | 1.03 |
| 75 | 12.12 | 2.07 | 0.97 |
| 100 | 12.11 | 2.73 | 0.92 |

**Table 11. Cross Regulation for $V_{OUT2}$ (12 V_ISO/0.25 A) With Full Load on $V_{OUT1}$ (12 V/2.75 A)**

| LOAD % ON $V_{OUT1}$ | $V_{OUT1}$ (V) | $I_{OUT1}$ (A) | % REG $V_{OUT1}$ |
|---|---|---|---|
| 10 | 14.29 | 0.03 | 19.08 |
| 25 | 12.71 | 0.07 | 5.92 |
| 50 | 12.19 | 0.13 | 1.56 |
| 75 | 11.98 | 0.21 | –0.16 |
| 100 | 11.90 | 0.27 | –0.87 |

### 4.1.2 Efficiency and Regulation With Load Variation (AC Input)

Table 12 and Table 13 show the efficiency and regulation performance data at a 115-V and 230-V AC input voltage, respectively.

**Table 12. Efficiency and Regulation at 115-V AC**

| LOAD % | $I_{INDC}$ (A) | $P_{INDC}$ (W) | $V_{OUT1}$ (V) | $I_{OUT1}$ (A) | $V_{OUT2}$ (V) | $I_{OUT2}$ (A) | $P_{OUT}$ (W) | EFF (%) | % REG $V_{OUT1}$ | % REG $V_{OUT2}$ | PWR LOSS (W) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 10 | 0.08 | 3.70 | 12.14 | 0.24 | 11.89 | 0.02 | 3.26 | 87.99 | 0.14 | –0.74 | 0.44 |
| 25 | 0.18 | 10.26 | 12.14 | 0.69 | 11.92 | 0.06 | 9.08 | 88.43 | 0.09 | –0.52 | 1.19 |
| 50 | 0.34 | 20.60 | 12.13 | 1.38 | 12.00 | 0.12 | 18.10 | 87.86 | 0.01 | 0.11 | 2.50 |
| 75 | 0.49 | 30.97 | 12.12 | 2.06 | 12.03 | 0.18 | 27.17 | 87.74 | –0.07 | 0.36 | 3.80 |
| 100 | 0.63 | 41.34 | 12.11 | 2.75 | 12.08 | 0.25 | 36.23 | 87.64 | –0.16 | 0.80 | 5.11 |

**Table 13. Efficiency and Regulation at 230-V AC**

| LOAD % | $I_{INDC}$ (A) | $P_{INDC}$ (W) | $V_{OUT1}$ (V) | $I_{OUT1}$ (A) | $V_{OUT2}$ (V) | $I_{OUT2}$ (A) | $P_{OUT}$ (W) | EFF (%) | % REG $V_{OUT1}$ | % REG $V_{OUT2}$ | PWR LOSS (W) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 10 | 0.09 | 4.14 | 12.14 | 0.28 | 12.00 | 0.02 | 3.64 | 88.04 | 0.14 | –0.38 | 0.49 |
| 25 | 0.13 | 9.99 | 12.13 | 0.68 | 12.02 | 0.06 | 9.01 | 90.21 | 0.08 | –0.22 | 0.98 |
| 50 | 0.21 | 20.30 | 12.12 | 1.39 | 12.04 | 0.12 | 18.31 | 90.17 | 0.00 | –0.07 | 2.00 |
| 75 | 0.30 | 30.27 | 12.11 | 2.07 | 12.08 | 0.18 | 27.27 | 90.11 | –0.08 | 0.30 | 2.99 |
| 100 | 0.38 | 40.13 | 12.10 | 2.74 | 12.09 | 0.25 | 36.16 | 90.10 | –0.14 | 0.36 | 3.97 |

### 4.1.3 Standby Power

The standby power was noted at multiple DC input voltages and 230V AC input voltage with no load on the output DC bus. Standby power for 230VAC was measured to be around 150mW. The results for DC input voltages are shown in Table 14.

**Table 14. No Load Power Across Input**

| $V_{INDC}$ (VDC) | $I_{INDC}$ (mA) | $P_{INDC}$ (mW) |
|---|---|---|
| 120 | 0.7860 | 94.3 |
| 165 | 0.5800 | 95.7 |
| 250 | 0.3870 | 96.8 |
| 325 | 0.3030 | 98.5 |
| 400 | 0.2526 | 101.0 |
| 430 | 0.2450 | 105.4 |

## 4.2 Performance Curves

### 4.2.1 Efficiency With Load Variation

Figure 5 and Figure 6 show the measured efficiency of the system with DC input voltage and AC input voltage variation respectively.

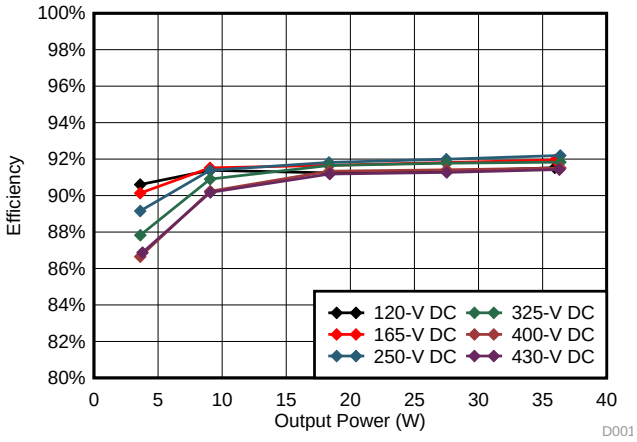



**Figure 5. DC Efficiency versus Output Power**

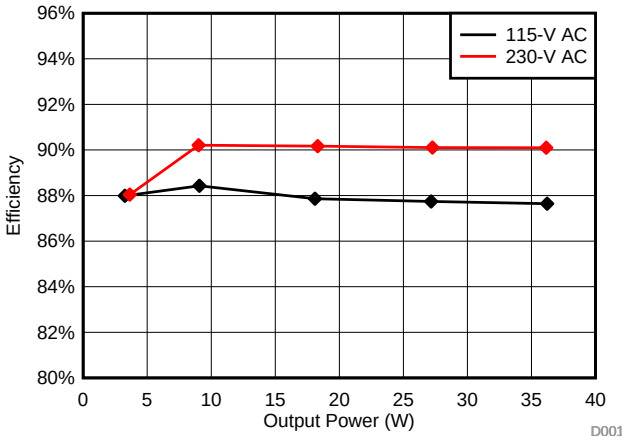



**Figure 6. AC Efficiency versus Output Power**

### 4.2.2 Load and Line Regulation in CV Mode

Figure 7 shows the measured load regulation of the 12-V_ISO/2.75-A output.

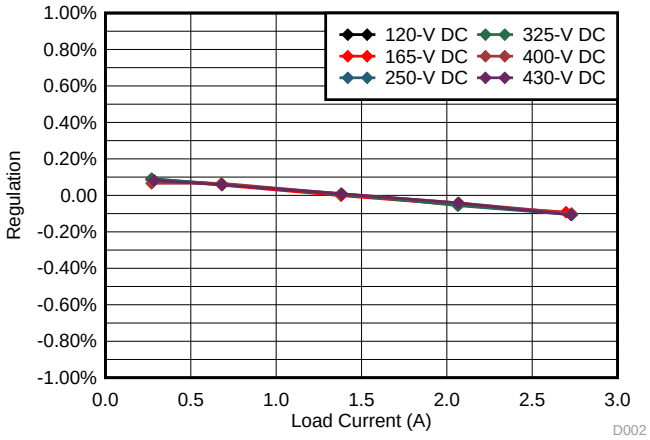



**Figure 7. 12-V_ISO Output Voltage Regulation With Load Current in CV Mode**

Figure 8 shows the measured load regulation of the 12-V/0.25-A output.

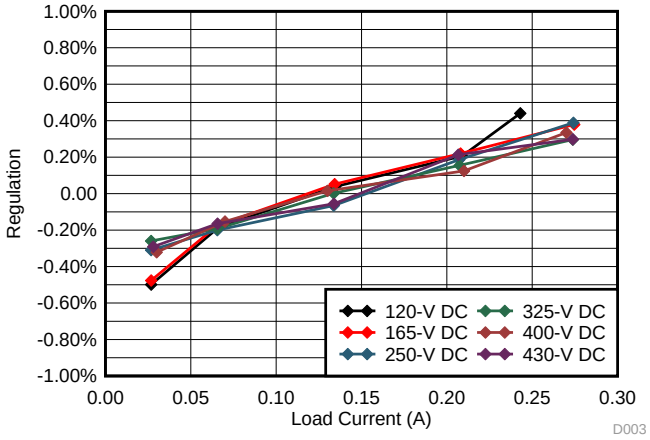



**Figure 8. 12-V Output Voltage Regulation With Load Current in CV Mode**

Figure 9 shows the measured line regulation of both the outputs at full load.

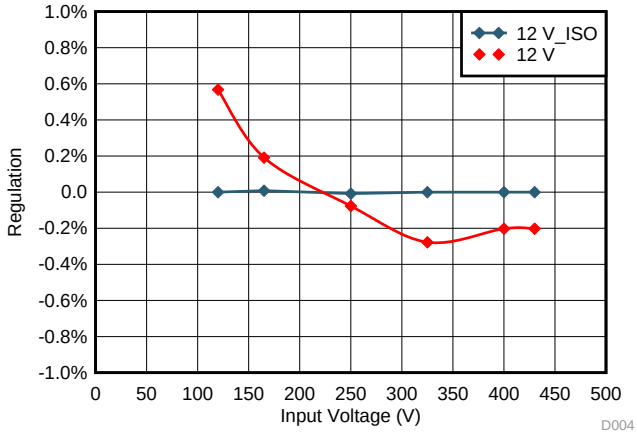



**Figure 9. Line Regulation With Full Load**

## 4.3 Functional Waveforms

### 4.3.1 Flyback MOSFET Switching Node Waveforms

Waveforms at the flyback switching (SW) node were observed along with the MOSFET current for 165-V DC and 400-V DC under full load condition.

Figure 10 and Figure 11 show the SW node waveform along with MOSFET current for a 165-V DC input and a 400-V DC input, respectively, with all the rails loaded fully.

**NOTE:** Red trace: Drain-to-source voltage, 200 V/div; Green trace: Drain current, 2 A/div

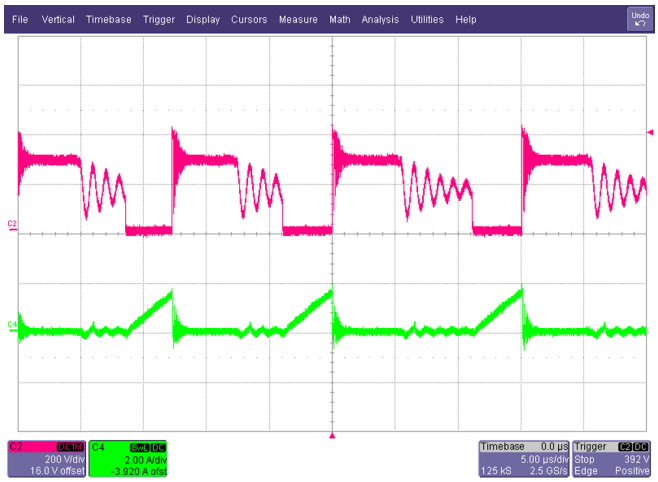


**Figure 10. SW Node Waveform and MOSFET Current at $V_{INDC}$ = 165-V, Full Load**

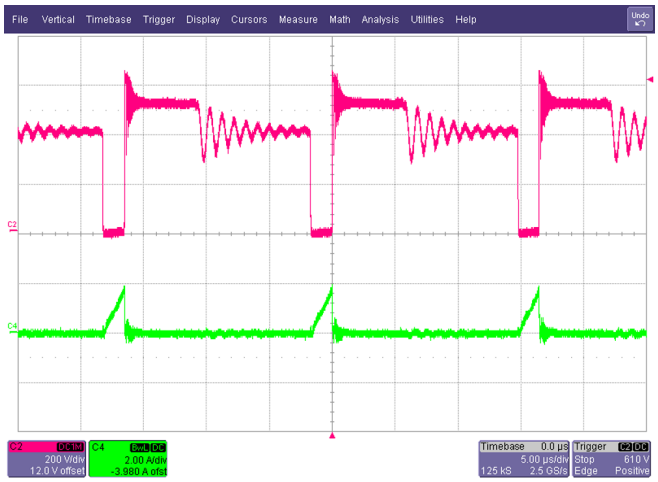


**Figure 11. SW Node Waveform and MOSFET Current at $V_{INDC}$ = 400-V, Full Load**

Figure 12 and Figure 13 show the $V_{DS}$ turnon and turnoff waveforms at 400-V DC input voltage and full load.

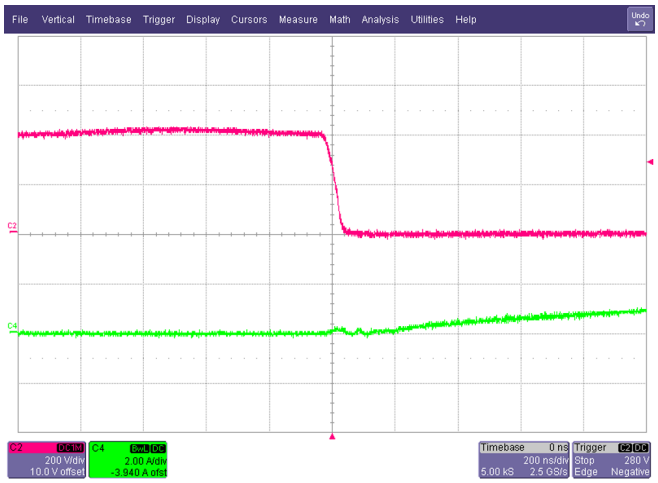


**Figure 12. $V_{DS}$ Turnon Waveform**

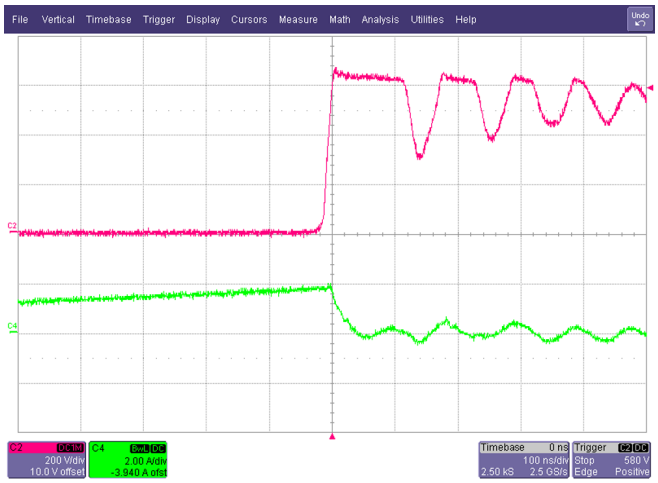


**Figure 13. $V_{DS}$ Turnoff Waveform**

### 4.3.2 Synchronous Rectifier $V_{DS}$ Waveform

The $V_{DS}$ waveform was observed with a 400-V DC input voltage under full load condition. The maximum voltage across the synchronous FET is below 60 V. To have a sufficient margin, a 100-V TI FET (CSD19531) has been used for this TI Design. Based on user requirement, an 80-V FET can also be used for synchronous rectification. Figure 14 shows the $V_{DS}$ waveform of the synchronous FET.

**NOTE:** Red trace : Drain-to-source voltage, 10 V/div


**Figure 14. Synchronous FET $V_{DS}$ Waveform at $V_{INDC}$ = 400 V, Full Load**

### 4.3.3 Output Ripple

For the following figures, the ripple is observed at both the outputs at full load with a 400-V DC input voltage without any post LC filtering.

The peak-to-peak ripple voltage is around 500 mV for both the outputs. Figure 15 and Figure 16 show the ripple for 12-V_ISO/2.75-A rail and 12-V/0.25-A rail, respectively.

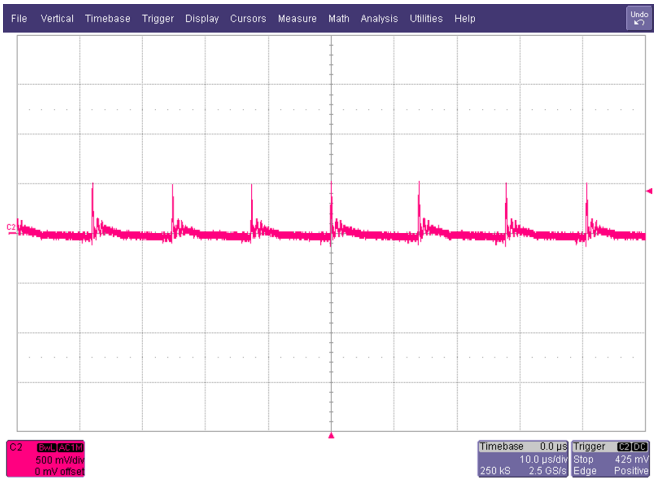



**Figure 15. 12-V_ISO Output Ripple at $V_{INDC}$ = 400-V and Full Load**

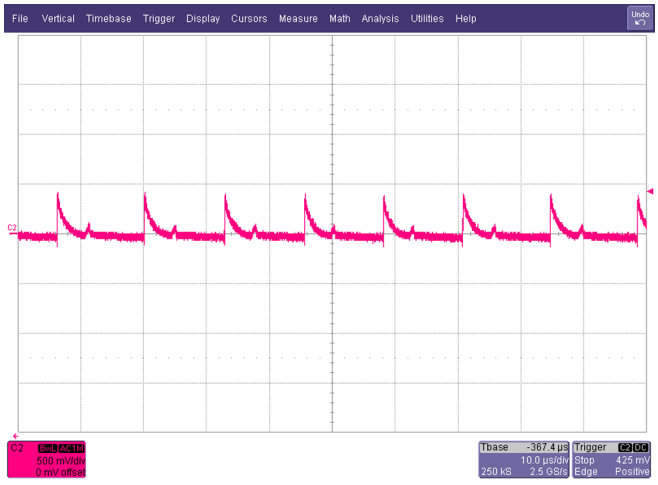



**Figure 16. 12-V Output Ripple at $V_{INDC}$ = 400-V and Full Load**

## 4.4 Transient Waveforms

### 4.4.1 Turnon Characteristics

The output turnon waveforms are observed with a resistive load. Figure 17 and Figure 18 show the turnon waveform at the 12-V_ISO/2.7-5A and 12-V/0.25-A outputs at 400-VDC input voltage and full load, respectively.

**NOTE:** Red trace : Output voltage, 5 V/div; Green trace: Output current, 1 A/div

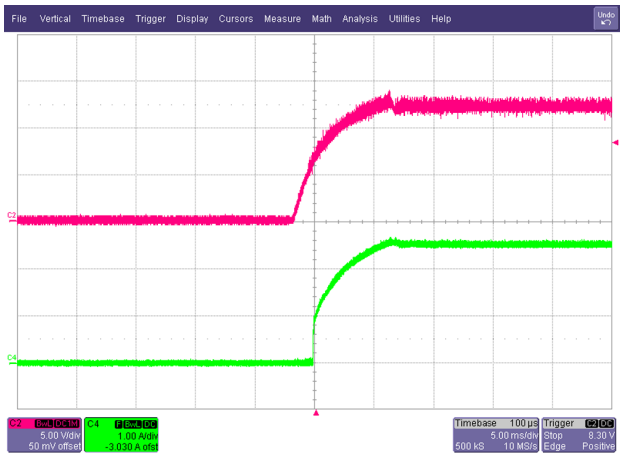



**Figure 17. 12-V_ISO/2.75-A Output Turnon Waveform at 400-V DC**

**NOTE:** Red trace: Output voltage, 5 V/div; Green trace: Output current, 100 mA/div

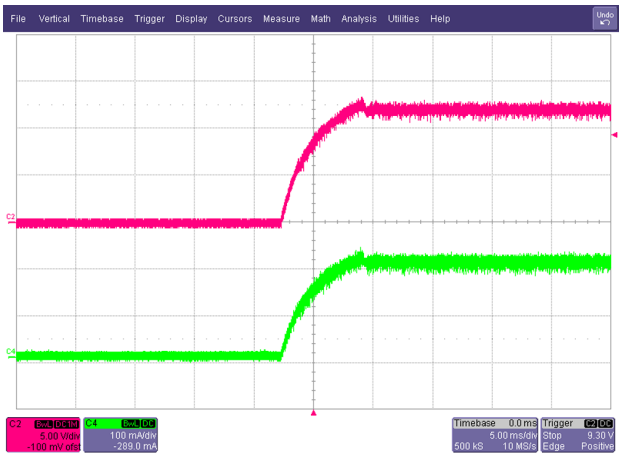



**Figure 18. 12-V/0.25-A Output Turnon Waveform at 400-V DC**

### 4.4.2 Transient Load Response

Load transient performance is observed for both the rails with the load switched at a 0.2-m wire length. The load transient is observed for output switched on from 10% to 100% and switched off back to 10% load.

Figure 19 and Figure 20 depict the transient load response for the 12-V_ISO output at an input voltage of 400-V DC with a load transient from 0.275 to 2.75 A and vice versa.

**NOTE:** Red trace: Output voltage, 500 mV/div; Green trace: Output current, 2 A/div

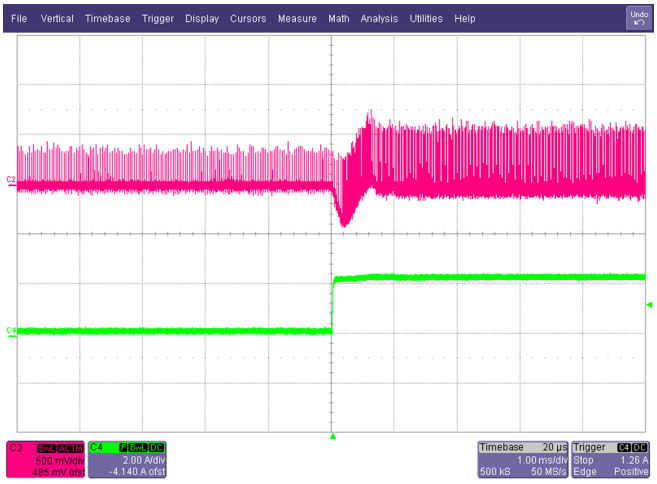



**Figure 19. 12-V_ISO Output Waveform, Load Transient From 0.275 to 2.75 A**

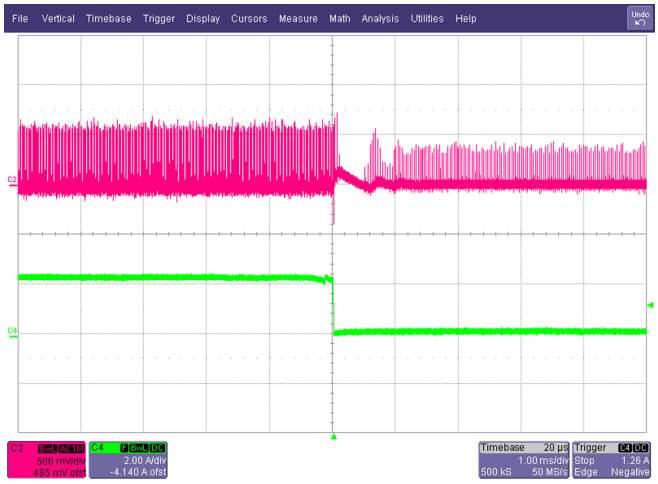



**Figure 20. 12-V_ISO Output Waveform, Load Transient From 2.75 to 0.275 A**

Figure 21 and Figure 22 depict the transient load response for the 12-V output at an input voltage of 400-V DC with a load transient from 25 to 250 mA and vice versa.

**NOTE:** Red trace: Output voltage, 2 V/div; Green trace: Output current, 200 mA/div

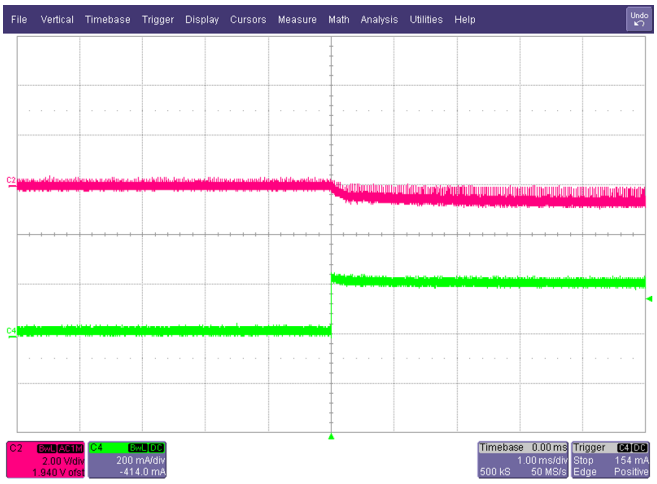



**Figure 21. 12-V Output Waveform, Load Transient From 25 to 250 mA**

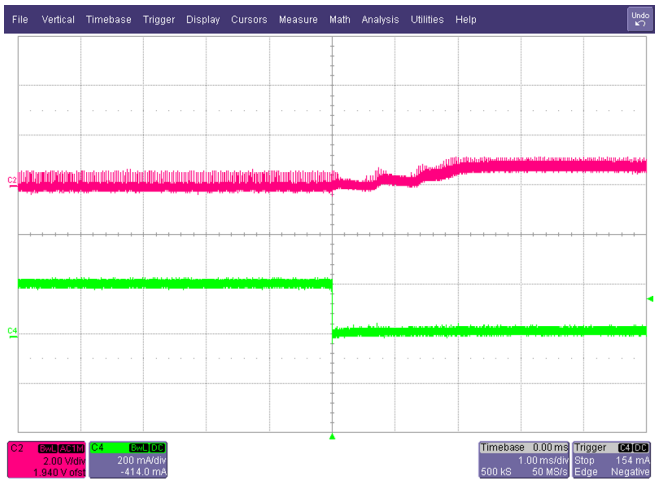



**Figure 22. 12-V Output Waveform, Load Transient from 250 to 25 mA**

### 4.4.3 Short-Circuit Response

The short-circuit response was recorded by applying a short at the 12-V_ISO/2.75-A output during full load operation. Figure 23 shows that during the interval when the short is present, the converter goes into hiccup mode; when the short is removed, the converter recovers back to the normal operation.

**NOTE:** Red trace: Output voltage, 10 V/div; Green trace: Output current, 2 A/div


**Figure 23. Response During Short-Circuit and Auto-Recovery After Removal of Short**

## 4.5 Thermal Measurements

The thermal measurements are taken at room temperature (25°C) with a 400-V DC input voltage, full load, after letting the board run for half an hour and without any external cooling.

Figure 24 and Figure 25 show the top and bottom side thermal images of TIDA-00709, respectively.

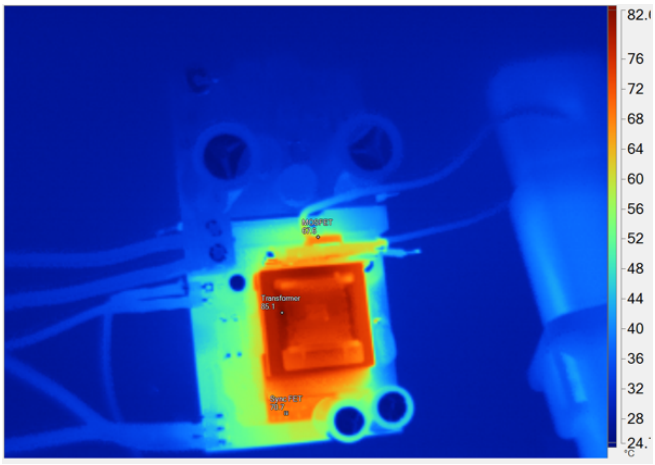



**Figure 24. Top-Side Thermal Image at 400-VDC Input, Full Load, Without Fan**

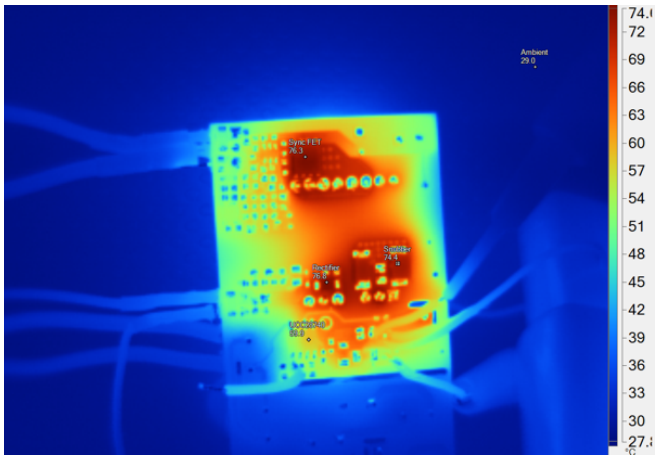



**Figure 25. Bottom-Side Thermal Image at 400-V DC Input, Full Load, Without Fan**

**Table 15. Highlighted Image Markers**

| COMPONENT | TEMPERATURE |
|---|---|
| Transformer | 85.1°C |
| MOSFET | 67.6°C |
| Synchronous FET | 76.3°C |
| Snubber | 74.4°C |

These temperatures are at an ambient of 25°C. For higher ambient temperatures (typically, 60°C for server PSUs), a 200LFM Fan must be used while operating the board.

## 4.6 Conducted Emissions

The conducted emissions were measured with 230-VAC input voltage at full load in a standard setup and were compared against EN55011 Class-B limits. The CE signature was found to meet the class-B limits. Figure 26, Figure 27, Figure 28 and Figure 29 show the CE data for peak on positive line, peak on negative line, average on positive line and average on negative line respectively. Table 16 gives the measured peak and average margin limits at some specific frequencies.

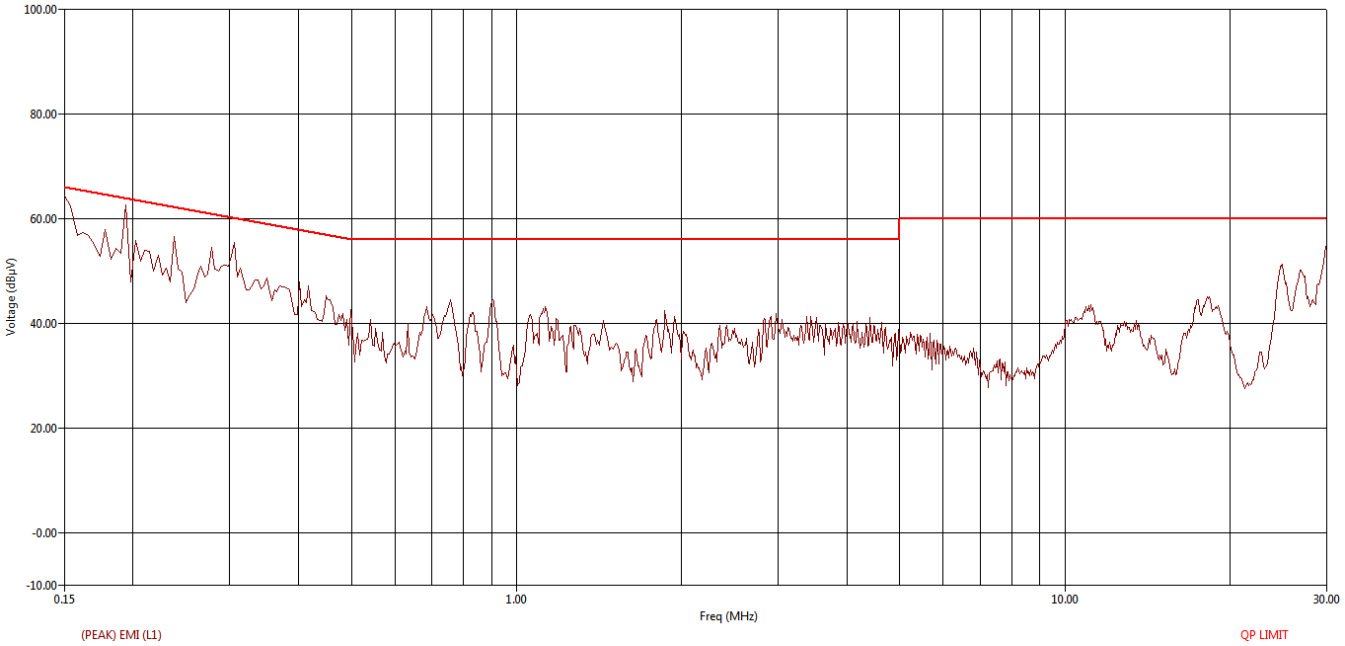



**Figure 26. CE as per EN55011 Class B, Peak on Positive Line**

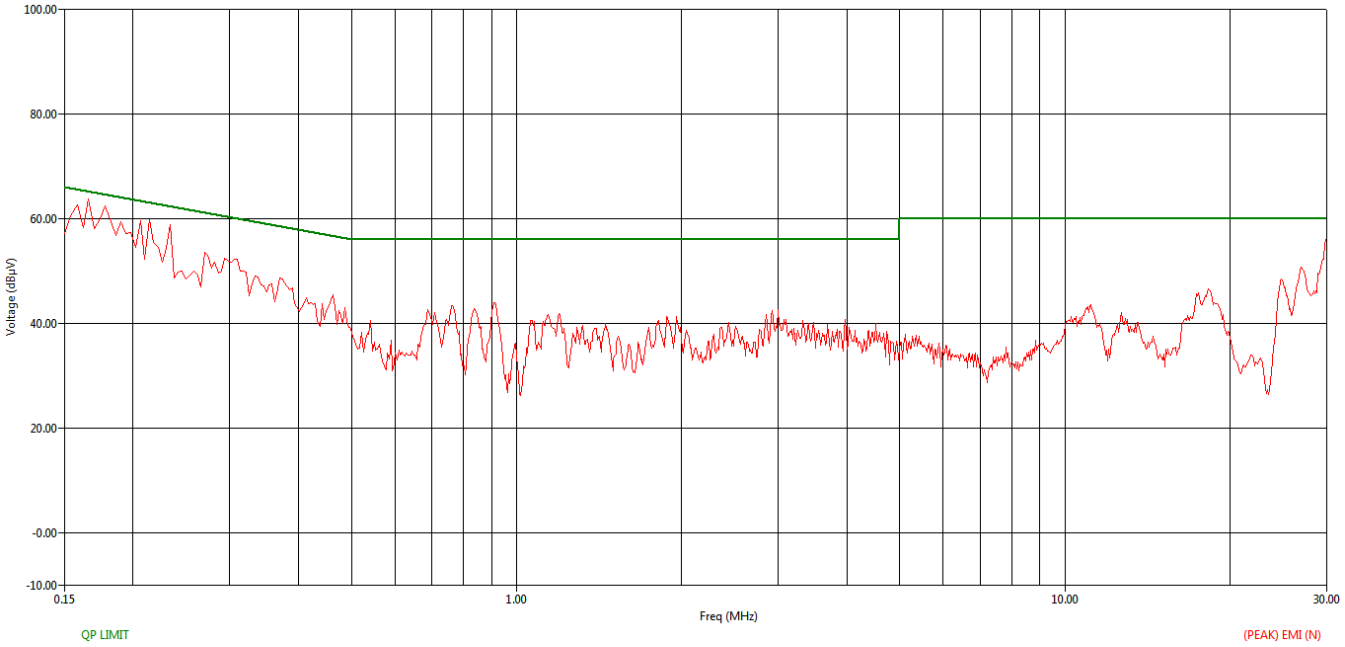



**Figure 27. CE as per EN55011 Class B, Peak on Negative Line**

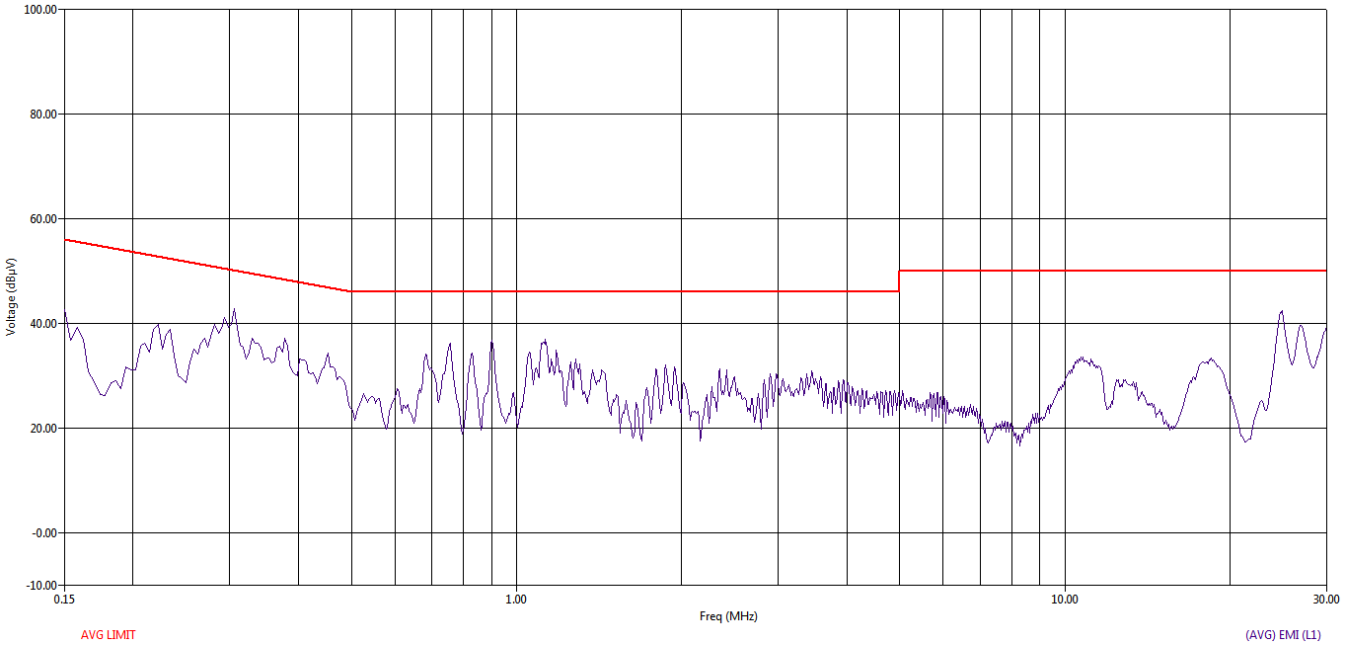



**Figure 28. CE as per EN55011 Class B, Average on Positive Line**

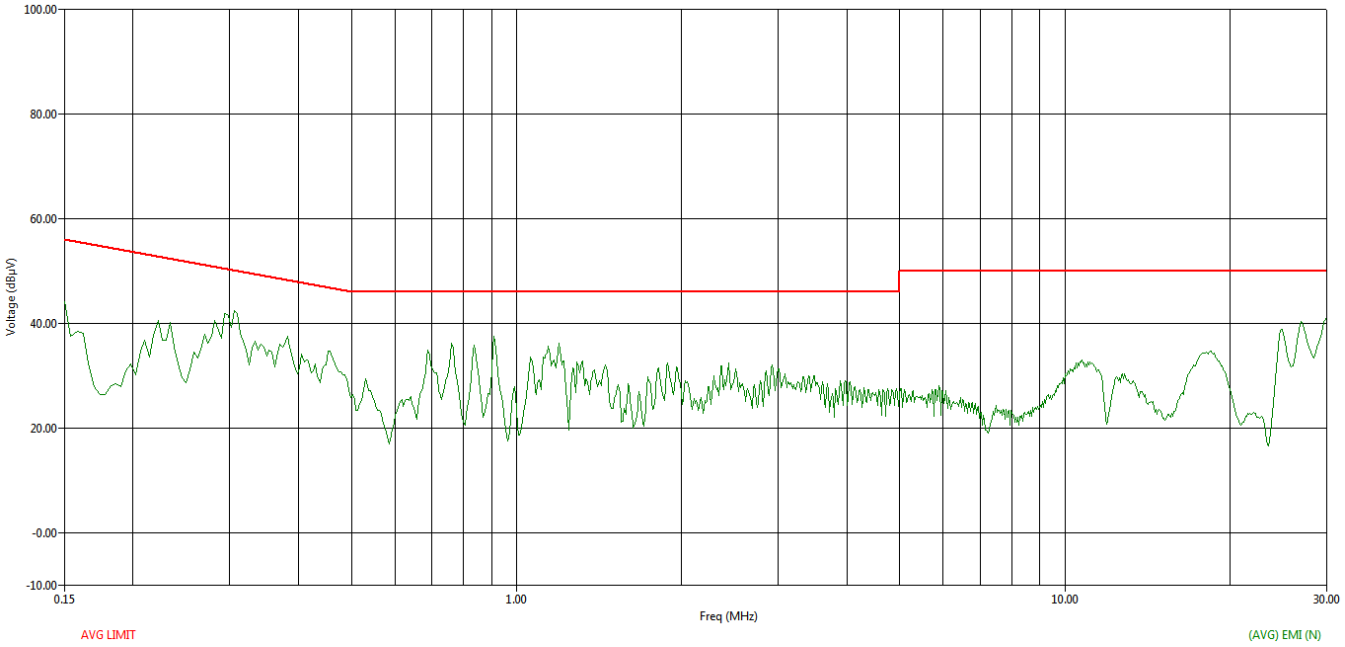



**Figure 29. CE as per EN55011 Class B, Average on Negative Line**

**Table 16. Conducted Emissions Quasi-Peak And Average Margins as per EN55011 Limits**

| FREQUENCY (MHz) | LINE | (QP) MARGIN QPL (dB) | (AVG) MARGIN AVL (dB) |
|---|---|---|---|
| 0.1500 | L1 | –10.99 | –17.20 |
| 0.1660 | N | –12.18 | –15.47 |
| 0.1940 | L1 | –15.29 | –23.75 |
| 0.2380 | L1 | –14.35 | –11.02 |
| 0.3060 | L1 | –9.63 | –6.91 |
| 0.9100 | N | –12.47 | –8.95 |
| 11.1680 | N | –19.33 | –16.31 |
| 18.2640 | N | –15.93 | –14.61 |
| 24.8120 | N | –15.43 | –11.01 |
| 24.8600 | L1 | –12.72 | –8.25 |
| 26.9080 | N | –13.97 | –10.23 |
| 26.9680 | L1 | –14.48 | –10.61 |
| 29.9080 | N | –10.46 | –10.70 |
| 29.9680 | L1 | –11.52 | –11.51 |

## 4.7 Surge and EFT Test

Surge and EFT testing is done on the boards as per EN55014. The test condition and test results are listed in Table 17.

**Table 17. Surge and EFT Test Results**

| BASIC STANDARD | PORT | REQUIREMENTS OF IEC 61000-6-2/EN 50082-2: IMMUNITY STANDARD FOR INDUSTRIAL ENVIRONMENTS | TEST RESULT |
|---|---|---|---|
| IEC/EN 61000-4-4: EFT, Level-4 | AC input line | ±4 kV, 5 kHz | Passed with performance criterion A(1) |
| IEC/EN 61000-4-5: Surge, Level-4 | AC input line | ±4 kV line to line | Passed with performance criterion A(1) |

(1) Normal performance within limits specified by the design or manufacturer

# 5 Design Files

## 5.1 Schematics

To download the schematics, see the design files at TIDA-00709.

## 5.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00709.

## 5.3 PCB Layout Recommendations

A careful PCB layout is critical and extremely important in a fast-switching circuit involving magnetics to provide appropriate device operation and design robustness.

### 5.3.1 Power Stage Specific Guidelines

Follow these guidelines to route power stage components:

- Minimize the loop area and trace length of the power path circuits, which contain high-frequency switching currents. This helps to reduce EMI and improve converter overall performance.
- Keep the switch node as short as possible. A compact switch node reduces common mode noise associated with the high dV/dt.
- Keep traces with high dV/dt and high di/dt away or shielded from sensitive signal traces with adequate clearance and/or ground shielding.
- For each power supply stage, keep power ground and control ground separate. Tie them together (if they are electrically connected) at single point to a stable potential.
- Place protection devices such as TVS, snubbers, capacitors, or diodes physically close to the device they are intended to protect, and route them with short traces to reduce inductance.
- Choose the width of PCB traces based on acceptable temperature rise at the rated current as per IPC2152 as well as acceptable DC and AC impedances. Also, the traces should withstand the fault currents (such as short-circuit current) before the activation of electronic protection such as fuse or circuit breaker.
- Determine the distances between various traces of the circuit according to the requirements of applicable standards. For this design, follow the UL 60950-1 safety standard to maintain the creepage and clearance from live line to neutral line and to safety ground as defined in the Tables 2K through 2N of this standard.
- Adapt thermal management to fit the end-equipment requirements.
- Place bulk capacitors close to the transformer and to the ground.

### 5.3.2 Controller Specific Guidelines

Follow the key guidelines for routing controller components and signal circuits:

- Place VS resistors as close to VS pin as possible.
- For the VDD decoupling capacitor, put multiple vias in parallel from the VDD capacitor to the ground plane and from the ground plane to the GND pin of the controller. Put as many vias in parallel as possible.
- Place current sense components as close to the CS pin as possible.
- See the placement and routing guidelines and layout examples presented in UCC28740 datasheet (SLUSBF3).

### 5.3.3 Layout Prints

To download the layer plots, see the design files at TIDA-00709.

### 5.4 Altium Project

To download the Altium project files, see the design files at TIDA-00709.

### 5.5 Gerber Files

To download the Gerber files, see the design files at TIDA-00709.

### 5.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-00709.

### 5.7 Design Calculator Spreadsheet

To download the design spreadsheet calculator for this reference design, see the link at TIDA-00709.

## 6 References

1. Texas Instruments, *Control Challenges for Low Power AC/DC Converters*, Unitrode Power Supply Design Seminar SEM2100 (SLUP325)
2. Texas Instruments, *Snubber Circuits: Theory, Design and Applications* , Seminar 900 Topic 2 (SLUP100)
3. Texas Instruments, *Choosing Standard Recovery Diode or Ultra-Fast Diode in Snubber*, Snubber Application Note (SNVA744)
4. Texas Instruments, *Choosing Standard Recovery Diode or Ultra-Fast Diode in Snubber* UCC28740 User's Guide (SLUUAL8)

### 6.1 Trademarks



## 7 About the Authors

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## Revision A History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**Changes from Original (October 2016) to A Revision** **Page**

- Changed title from *36-W, 100- to 425-V DC, >92% Efficiency, Dual Output, Auxiliary Supply Reference Design for Server PSU* ..... 1
- Changed block diagram ..... 1
- Deleted "High Average Efficiency of >91% and Peak Efficiency of > 92%" from Features ..... 1
- Added "High Efficiency of > 90% With AC Input and > 92% With DC Input" to Features ..... 1
- Added "85- to 265-V AC" to operating input voltage range ..... 1
- Changed standby power from ≈ 100 mW to ≈ 120 mW ..... 1
- Added AC/DC form factor size ..... 1
- Changed final paragraph of Section 1.1 ..... 3
- Added Figure 2 ..... 3
- Changed block diagram ..... 5
- Added Section 2.4 ..... 20
- Added Section 2.5 ..... 22
- Added Section 4.1.2 ..... 28
- Changed Section 4.1.3 (was previously Section 4.1.2) ..... 29
- Changed Figure 6 ..... 30
- Added Section 4.6 ..... 37
- Added Section 4.7 ..... 40

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