TI Designs

Automotive Wide V_{IN} Front-End Power Reference Design With Cold Crank Operation and Transient Protections

Description

This reference design is an automotive front-end power supply that able to supply a 30-W maximum output for the 12-V car battery. The first stage is a buck-boost DC/DC converter, which maintains a stable output voltage over the full DC range of the 12-V battery conditions specified in ISO 7637-2 and ISO 16750-2 standards. Then a low-cost, compact buck converter is connected to the buck-boost converter and enables up to a 20-W output. The system consists of reverse battery protection, electrical transient protections, and EMI filters. The EMI filter consists of DM and CM respectively and is designed for complying conducted EMI standards per CISPR25.

Resources

TIDA-01179	Design Folder
LM5118-Q1	Product Folder
LM74610-Q1	Product Folder
TPS54540-Q1	Product Folder

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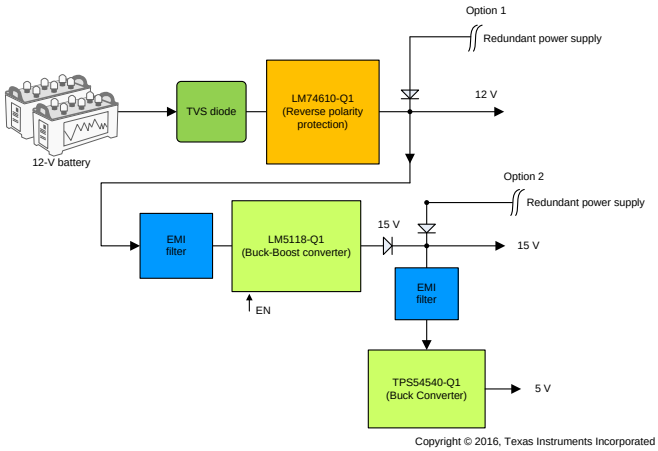
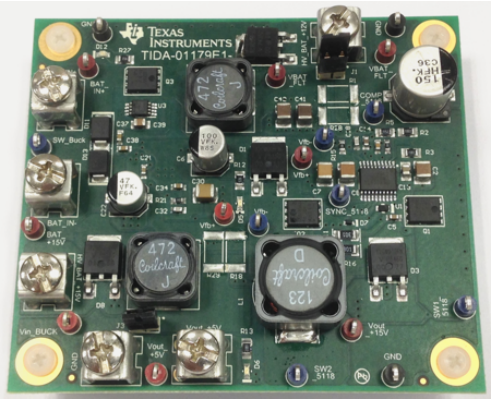
Features

- Wide-V_{IN} Buck-Boost Converter During Very Low Dips in Input Voltage of 3- to 36-V DC, 42-V Transient
- Low-Cost Buck Operates After the Buck-Boost With 5-V and 4.5-A maximum output
- Reverse Battery Protection With Fast Shutdown
- Designed and Tested for Severe Battery Cold Crank Operations (ISO 16750-2 Level III)
- Designed and Tested for ISO 7637-2:2004 Pulse 1, 2a, and 3a/b Severe Conditions (Level IV)
- Tested for CISPR25 Conducted EMI (Class 5)

Applications

- HEV/EV Traction Inverter
- Dry Double Clutch Transmission
- Electronic Control Units
- Battery Front-End Power





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1 System Overview

1.1 System Description

This reference design is a wide input 30-W front-end power supply for a 12-V car battery in the HEV/EV traction inverter system (see Figure 1). It consists of two DC/DC converters. The first converter is a buck-boost converter, which handles a wide input range from the car battery and provides 15 V of constant output voltage at a 2-A output current. This 15-V rail can be used to power the system basis chip (SBC), the resolver, and the primary of the IGBT bias supply. Then a buck converter connected to the output of buck-boost converts the 15 V down to 5 V at 4.5 A. This 5 V can power the microcontrollers, AD converters, safety diagnostic circuits, the primary sides of the current sensing, voltage sensing, and so on. The TIDA-01179 is able to handle all battery conditions, which includes:

- The system maintains a constant output voltage over the full DC range of battery conditions specified in ISO 16750-2:
  - Input $V_{IN(min)}$ down to 3.0 V simulating a severe cold cranking condition
  - Input $V_{IN(max)}$ up to 28 V simulating the upper range of normal battery operation
- The system must clamp and filter high-voltage electrical fast transients and maintain operation through them:
  - These pulses include clamped load dump (up to 38 V) and other transients outlined in ISO 7637-2:2004.
- The system must properly respond to a reverse battery polarity event and shut down appropriately.
- Filter design targets at the CISPR 25 automotive EMI standard for conducted emission suppression.
- The layout of the board must be done in such a way to minimize the footprint of the solution while maintaining high performance.

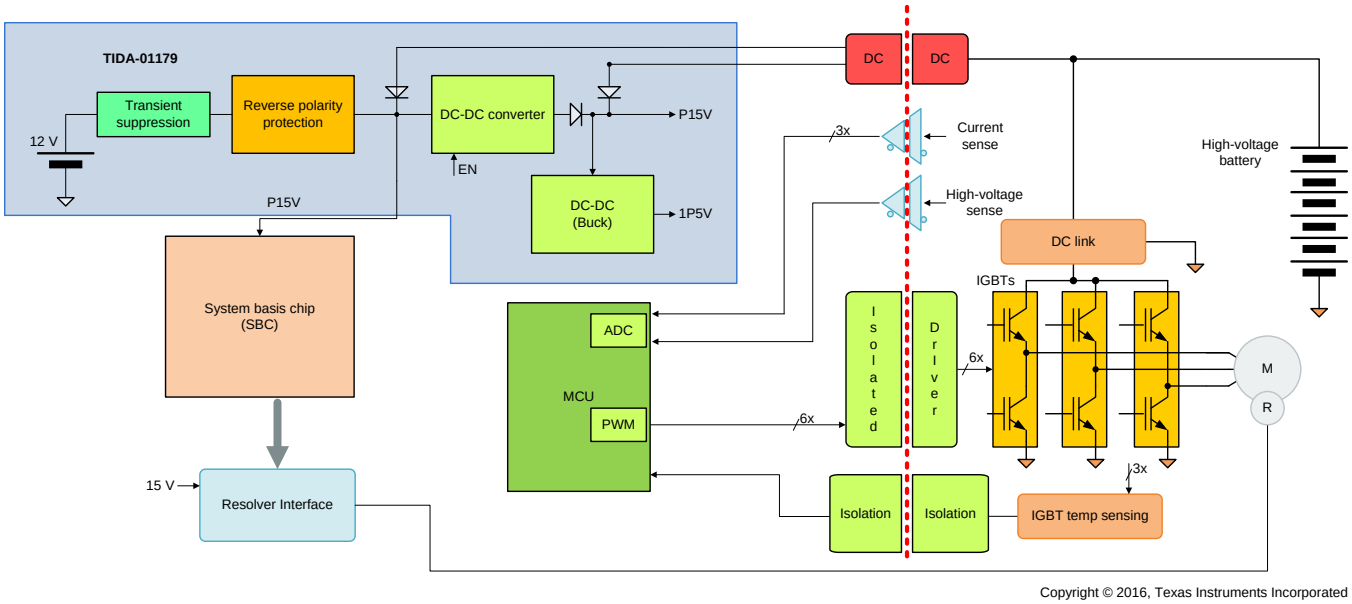


Figure 1. HEV/EV Traction Inverter System Block Diagram and Position of TIDA-01179

1.2 Key System Specifications

The key specifications of TIDA-01179 are shown in Table 1.

Table 1. Key System Specifications

PARAMETER		COMMENTS	MIN	TYP	MAX	UNIT
SYSTEM INPUT						
V_{IN}	Input voltage	Battery voltage range (DC)	3.00	13	28.00	V
V_{CLAMP+}	Positive clamping voltage	Positive input protection TVS clamping range	28.90	—	42.10	V
$V_{CLAMP–}$	Negative clamping voltage	Negative input protection TVS clamping range	15.60	—	25.80	V
P_{PK}	Peak pulse power dissipation	Maximum TVS power dissipation		600		W
OUTPUT VOLTAGE						
V_{OUT1}	V_{SYS1}	System output voltage, across load	14.70	15	15.30	V
V_{OUT2}	V_{SYS2}	System output voltage, across load	4.97	5	5.03	V
OUTPUT CURRENTS						
I_{OUT1}	I_{SYS1}	Max output current. Drawing more than 2.2 A is not recommended for thermal reasons. See the Thermal Images testing to see the temperature rise at different load levels	—	2	2.20	A
I_{OUT2}	I_{SYS2}	Max output current. Drawing more than 4.5 A is not recommended for thermal reasons. See the Thermal Images testing to see the temperature rise at different load levels	—	4	4.50	A

1.3 Block Diagram

The system block diagram is shown in Figure 2. The design consists of two DC/DC converters:

1. Buck-boost converter based on the LM5118-Q1. It converts the wide input battery voltage to a 15-V constant output voltage and supplies up to a 2-A output current.
2. Buck converter based on the TPS54540-Q1. It is connected to the buck-boost converter and generates a 5-V output voltage and up to a 4-A output current.

Prior to all the circuits, TVS diodes are connected to the 12-V battery for electrical transient suppression. Then the LM74610-Q1 is implemented for battery reverse polarity protection. Two EMI filters, which are implemented in front of the buck-boost converter and the buck converter respectively, are implemented for suppressing the conducted emission.

This TI Design option for connecting the redundant power supply is included in case the 12-V car battery is depleted or absent. The connection has two options and it is down through the oring diodes. The first path (option 1) is connected to the output of LM74610-Q1, which requires 12 V. The second path (option 2) is connected to the output of the buck-boost converter, which requires 15 V.

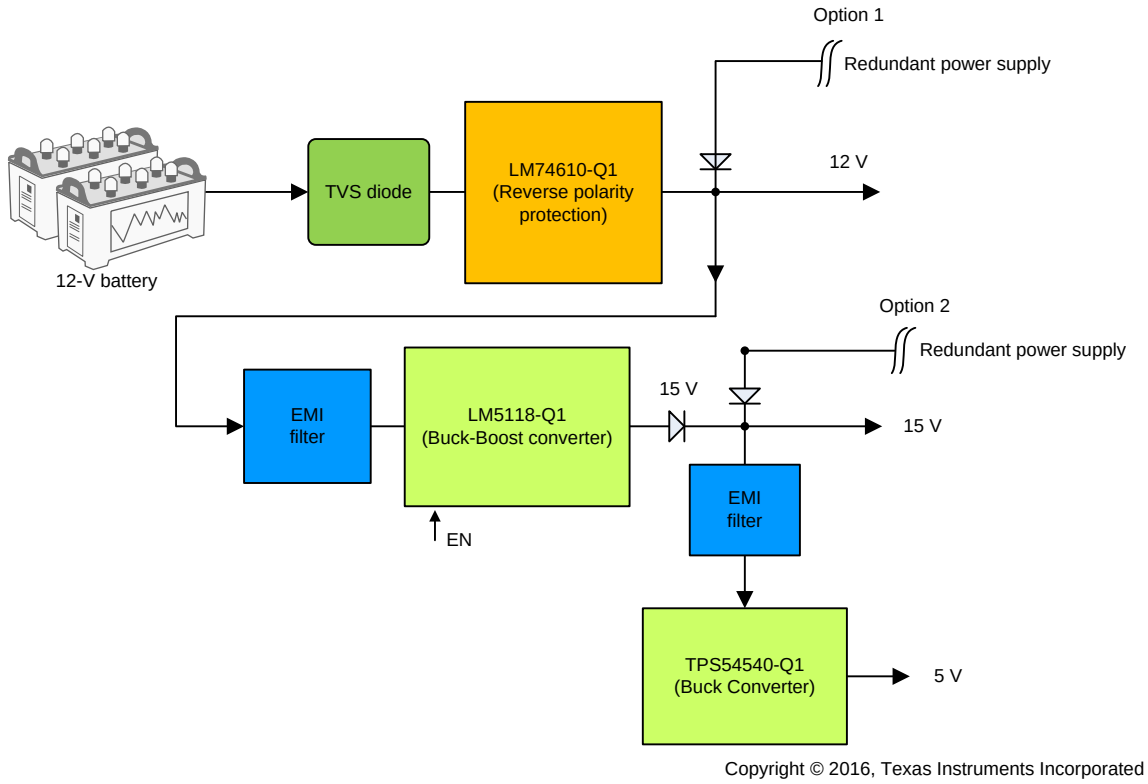


Figure 2. TIDA-01179 Block Diagram

1.4 Highlighted Products

The TIDA-01179 reference design features the following Texas Instruments devices.

1.4.1 LM5118-Q1

The LM5118-Q1 is an automotive grade buck-boost controller with 3- to 75-V input voltage range that is ideal for handling large electrical transients' conditions. The regulator switches smoothly from buck to buck-boost operation as the input voltage approaches the output voltage. It integrates high-side and low-side MOSFET drives capable of supplying peak currents of 2 A. The regulator control method is based on current mode control using an emulated current ramp. Peak current mode control provides inherent line feed-forward, cycle-by-cycle current limiting, and ease of loop compensation.

1.4.2 LM74610-Q1

The LM74610-Q1 is a controller device that can be used with an N-channel MOSFET in a reverse polarity protection circuitry. It is designed to drive an external MOSFET to emulate an ideal diode rectifier when connected in series with a power source. It provides a gate drive for an external N-channel MOSFET and a fast response internal comparator to discharge the MOSFET gate in the event of reverse polarity.

1.4.3 TPS54540-Q1

The TPS54540-Q1 is a 42-V, 5-A, step-down regulator with an integrated high side MOSFET. The device survives load dump pulses up to 65 V per ISO 7637. A low-ripple, pulse-skip mode reduces the no load supply current to 146 μA. It integrated a 92-mΩ high-side MOSFET.

2 System Design Theory

2.1 Input Protection

Figure 3 shows a schematic of the input transient protection and battery reverse polarity protection.

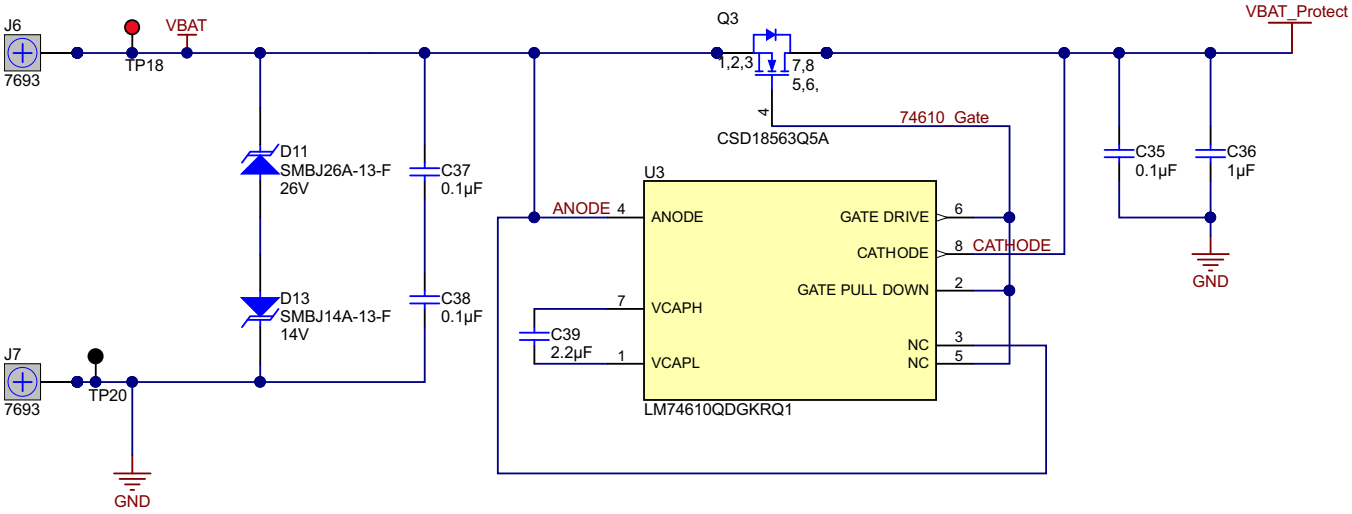


Figure 3. Schematic of Input Transient Protection and Reverse Polarity Protection

2.1.1 Reverse Battery Protection

Reverse battery protection is required in every electronic subsystem of a vehicle, both by OEM standards, as well as ISO 16750-2, an international standard pertaining to supply quality. The goal is to prevent reverse-biasing components, which are sensitive to polarity, like polarized capacitors and most integrated circuits.

The circuit consists of a N-channel MOSFET (Q3), which is driven by the LM74610-Q1 smart diode controller. Traditional methods that implement blocking diodes result in large power dissipation due to the typical 400- to 700-mV forward voltage drop. The smart diode solution decreases the losses as per the $R_{DS(ON)}$ of the MOSFET. The LM74610-Q1 controller provides a gate drive for an external N-channel MOSFET and a fast response internal comparator to discharge the MOSFET gate in the event of reverse polarity. A unique advantage of this scheme is that it is not referenced to ground and thus has zero I_Q. The N-channel MOSFET is selected according to the following criteria:

- Continuous current rating higher than 10 A, which is the maximum input current at minimum input voltage in this design
- V_{GS} threshold must be 2.5 V maximum
- Source-to-drain voltage (V_{SD}) must be at least 0.48 V at 2 A

2.1.2 Electrical Transient Protection

TVS diodes are implemented on the supply input of the system to protection against both positive and negative electrical transients as per prescribed in ISO 7637-2:2004 pulses 1, 2a and 3a/b. OEM specifications will define a "class of operation" for each test, which defines the required operational status during and after the event. The TVS diodes are placed aiming at shut the transients while maintaining the downstream circuits operation.

The TVS diode is selected based on the following criteria:

- The diode breakdown voltage is lower than the breakdown voltage of the downstream circuits.
- The positive clamping voltage is above twice of the input battery voltage (for jump start) and clamped load dump voltages.
- The negative clamping voltage is slightly lower than the battery voltage is reverse connection so that it will clamp all negative voltages while does not create short circuit during a reverse battery condition.
- The power rating of the TVS diode is higher than the power dissipation during the transient clamping.

The important parameters for calculating the TVS diode power rating are: the clamping voltage, the voltage of the pulse it is clamping, and the source impedance of the pulse. One severe scenario according to the ISO 7637 pulse 2a standard is [7]:

- V_{PULSE} = 75 V
- R_{SOURCE} = 4 Ω
- V_{CLAMP} = 33 V

Where:

- V_{PULSE} is the voltage of the pulse that TVS diode is clamping
- R_{SOURCE} is the source impedance of the pulse
- V_{CLAMP} is the clamping voltage from TVS diode

The worst case assumption is that the load is drawing zero current and all the current flows through the TVS diode. Thus, the power rating of the diode is calculated as:

$$P_{TVS} = \frac{V_{PULSE} - V_{CLAMP}}{R_{SOURCE}} \times V_{CLAMP} = \frac{75 - 33}{4} \times 33 = 346.5\ W \quad (1)$$

Two SMB sized TVS diodes with a 600-W peak power rating are selected for positive and negative clamping respectively for the design.

2.2 Buck-Boost Converter

The procedure for calculating the surrounding components of the buck-boost converter are given in this section. The design specifications are shown in Table 2. A schematic of the buck-boost converter is shown in Figure 4.

Table 2. Buck-Boost Converter Specifications

PARAMETER	SPECIFICATION
Input voltage (V_{IN})	3 to 24 V
Output voltage (V_{OUT})	15 V
Output ripple	± 2%
Maximum output current (I_{OUT_MAX})	2.2 A
Switching frequency	320 kHz
Maximum output power (P_{OUT_MAX})	33 W

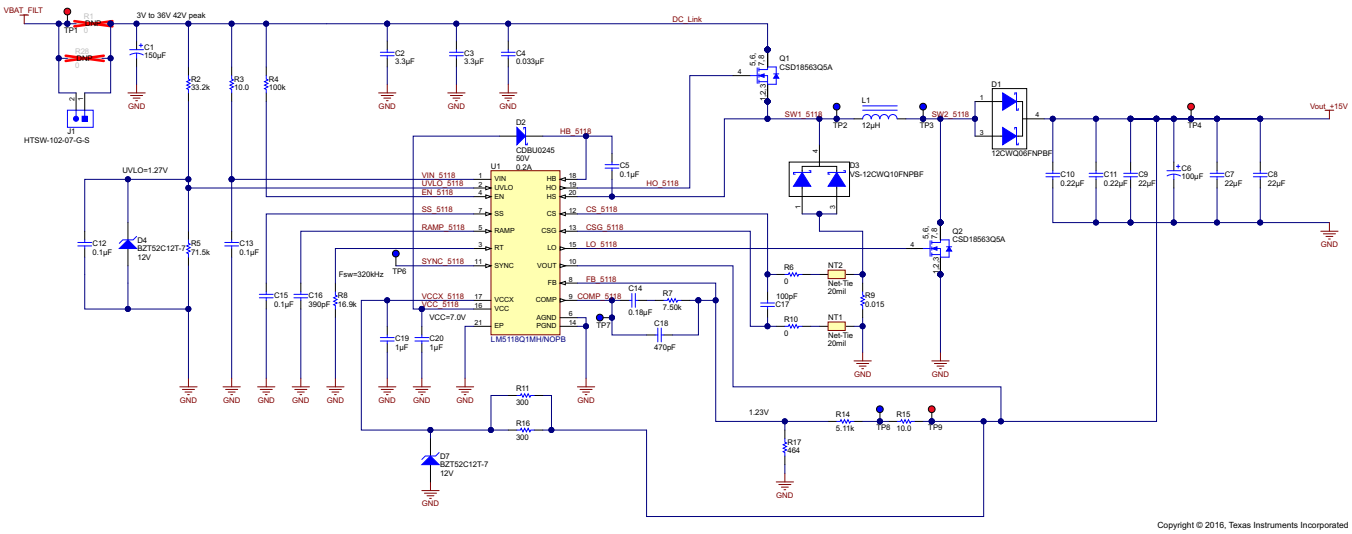


Figure 4. Schematic of Buck-Boost DC-DC Converter

2.2.1 Switching Frequency

The switching frequency of the LM5118 is set by the oscillation resistor, which is connected to the RT pin (R8 in Figure 4). A switching frequency of 320 kHz is selected as a compromise between component size and efficiency. The value of RT is calculated as:

$$R_T = \frac{6.4 \times 10^9}{F_{SW}} - 3.02 \times 10^3 = 16.98\ k\Omega \quad (2)$$

where:

- F_{SW} is the switching frequency

2.2.2 Inductor Selection

The maximum ripple into the inductor is selected as 40% of the maximum load current. Target inductor values are then calculated for both operating modes. Then a compromise inductance value between the two calculated values must be chosen. The inductance in buck mode is calculated from Equation 3 and Equation 4.

For buck mode:

$$L_1 = \frac{V_{OUT}\left(V_{IN\_MAX} - V_{OUT}\right)}{V_{IN\_MAX} \times F_{SW} \times I_{RIPPLE}} = \frac{15 \times (28 - 16)}{28 \times 320k \times 1.7 \times 40\%} = 32\ \mu H \tag{3}$$

For buck-boost mode:

$$L_2 = \frac{V_{OUT} \times V_{IN\_MAX}}{\left(V_{OUT} + V_{IN\_MAX}\right) \times F_{SW} \times I_{RIPPLE}} = \frac{15 \times 3}{(15 + 3) \times 320k \times 1.7 \times 40\%} = 11.49\ \mu H \tag{4}$$

where:

- V_{OUT} is the output voltage
- V_{IN_MAX} is the maximum input voltage
- V_{IN_MIN} is the minimum input voltage
- F_{SW} is the switching frequency
- I_{RIPPLE} is the selected inductor peak to peak ripple current

The inductor value is selected as 10 µH as a compromise between the two calculated values. The inductance must be selected as low as possible to remove the buck-boost right-half-plane zero to a higher frequency.

Assuming 80% of efficiency of the converter, the peak inductor current at maximum V_{IN} is calculated in buck mode (I_{1PEAK}) and buck-boost mode (I_{2PEAK}) respectively:

For buck mode:

$$I_{1PEAK} = \frac{I_{OUT}}{\eta} + \frac{I_{RIPPLE\_BUCK}}{2 \times \left(1 - L_{TOL}\right)} = \frac{2}{0.8} + \frac{1.81}{2 \times (1 - 20\%)} = 3.63\ A \tag{5}$$

where:

- I_{OUT} is the output current
- η is the efficiency
- L_{TOL} is the inductor tolerance
- I_{RIPPLE_BUCK} is the inductor ripple current in buck mode

For buck-boost mode:

$$I_{2PEAK} = \frac{I_{OUT\_MIN}\left(V_{OUT} + V_{IN\_MIN}\right)}{\eta \times V_{IN\_MIN}} + \frac{I_{RIPPLE\_BUCKBOOST}}{2 \times \left(1 - L_{TOL}\right)} \tag{6}$$

$$I_{2PEAK} = \frac{1 \times (15 + 3)}{0.8 \times 3} + \frac{0.65}{2 \times (1 - 20\%)} = 7.9\ A$$

where:

- $I_{RIPPLE\_BUCKBOOST}$ is the inductor ripple current in buck-boost mode
- I_{OUT_MIN} is the output current at the minimum input voltage (3 V)
- η is the efficiency of the converter
- L_{TOL} is the inductor tolerance

Therefore, the selected inductor must have a saturation current rating at least as high as 7.9 A. The AEC-Q200 grade inductor from Coil craft with a 10-µH, 12.5-A saturation current is chosen for this design.

2.2.3 Current Sense Resistor

K factors for each mode need to be calculated before selecting a current sense resistor. K represents the slope compensation of the LM5118-Q1 and is different for buck mode K_{BUCK} and buck-boost mode $K_{BUCK-BOOST}$.

$$K_{BUCK} \geq 1 + \frac{10}{V_{IN\_MAX} - V_{OUT}} = 1.77 \quad (7)$$

$$K_{BUCK\_BOOST} \geq 1 + \frac{10}{V_{IN\_MIN}} = 4.33 \quad (8)$$

where:

- V_{IN_MAX} is the maximum input voltage
- V_{OUT} is the output voltage
- V_{IN_MIN} is the minimum input voltage

The sense resistor (R_{SNS}) is calculated for each mode of operation. A design margin (M) is selected as 15% to allow for component tolerances. Therefore:

$$R_{BUCK} = \frac{1.25 \times (1 - M)}{10 \times \left(\frac{I_{OUT\_PEAK}}{\eta} + \frac{I_{RIPPLE\_BUCK}}{2} \times K_{BUCK} \right)} = \frac{1.25 \times (1 - 0.15)}{10 \times \left(\frac{2}{0.8} + \frac{1.81}{2} \times 1.77 \right)} = 0.026\ \Omega \quad (9)$$

$$R_{BUCK\_BOOST} = \frac{2.5 \times (1 - M)}{10 \times \left(\frac{V_{IN\_MIN} + V_{OUT}}{V_{IN\_MIN}} \times \frac{I_{OUT\_PEAK}}{\eta} + \frac{I_{RIPPLE\_BUCKBOOST}}{2} \times K_{BUCK\_BOOST} \right)} \quad (10)$$

$$R_{BUCK\_BOOST} = \frac{2.5 \times (1 - 0.15)}{10 \times \left(\frac{3 + 15}{3} \times \frac{2}{0.8} + \frac{0.65}{2} \times 4.33 \right)} = 0.013\ \Omega$$

where:

- R_{BUCK} is the required sense resistance in buck mode
- R_{BUCK_BOOST} is the required sense resistance in buck-boost mode
- I_{RIPPLE_BUCK} is the inductor ripple current in Buck mode
- $I_{RIPPLE\_BUCKBOOST}$ is the inductor ripple current in buck-boost mode
- I_{OUT_PEAK} is the output peak current
- M is the current limit margin

Choose an R_{SENSE} value of around 13 mΩ to ensure the required maximum output current in buck-boost mode. A standard value of 15 mΩ is selected for this design. Power rating is calculated as:

$$P_{SNS} = I_{2PEAK}^2 \times R_{SNS} \times \frac{V_{OUT}}{V_{IN\_MIN} + V_{OUT}} = 15.4^2 \times 0.015 \times \frac{15}{3 + 15} = 2.96\ W \quad (11)$$

2.2.4 Input Capacitors

The input capacitor must supply the input current during the input voltage dip in cold crank conditions. Input capacitors are essential in limiting the ripple voltage at the input pin of the LM5118-Q1 while supplying most of the switch current during the buck switch on-time. When the buck switch turns on, the current into the buck switch steps from zero to the lower peak of the inductor current waveform, then ramps up to the peak value, and then drops to the zero and turn-off. The RMS current rating of the input capacitors for the buck (I_{RMS_BUCK}) and buck-boost ($I_{RMS\_BUCKBOOST}$) modes can be calculated as:

$$I_{RMS\_BUCK} = I_{OUT} \times \sqrt{D_{MAX\_BUCK} \times \left(1 - D_{MAX\_BUCK}\right)} = 2 \times \sqrt{\frac{15}{24} \times \left(1 - \frac{15}{24}\right)} = 0.97\ A \quad (12)$$

where:

- I_{OUT} is the output current of the buck-boost converter
- D_{MAX_BUCK} is the maximum duty cycle when converter is in buck mode

$$I_{RMS\_BUCKBOOST} = \frac{I_{OUT}}{1 - D_{MAX\_BUCKBOOST}} \times \sqrt{D_{MAX\_BUCKBOOST} \times \left(1 - D_{MAX\_BUCKBOOST}\right)} \quad (13)$$

$$I_{RMS\_BUCKBOOST} = \frac{2}{1 - \frac{15\ V}{3\ V + 15\ V}} \times \sqrt{\frac{15\ V}{3\ V + 15\ V} \times \left(1 - \frac{15\ V}{3\ V + 15\ V}\right)} = 4.47\ A$$

where:

- $D_{MAX\_BUCKBOOST}$ is the maximum duty cycle when the converter is in buck-boost mode

The required input capacitance is calculated as:

$$C = \frac{I_{RMS\_BUCKBOOST} \times D_{MAX}}{F_{SW} \times V_{IN\_MIN} \times 2\%} = \frac{4.47 \times 0.833}{320k \times 3 \times 2\%} = 193\ \mu F \quad (14)$$

where:

- D_{MAX} is the maximum duty cycle in buck-boost mode
- V_{IN_MIN} is the minimum input voltage

A 150-µF electrolytic capacitor with two 3.3-µF ceramic capacitors and one 0.033-µF ceramic capacitor are applied at the input. One 10-Ω resistor is added at the LM5118 input pin to limit the current and damping the possible ringings.

2.2.5 Output Capacitors

The output capacitor must supply the entire output current during the switch on time in the buck-boost mode. Both capacitance and ESR must be considered to ensure a given output ripple voltage. The minimum output capacitance for buck-boost mode is calculated from:

$$C_{MIN} = \frac{I_{OUT}}{F_{SW} \times \Delta V_{OUT}} \times \frac{V_{OUT}}{V_{IN\_MIN} + V_{OUT}} = \frac{2\ A}{320\ kHz \times 15\ V \times 2\%} \times \frac{15\ V}{3\ V + 15\ V} = 17.4\ \mu F \quad (15)$$

where:

- ΔV_{OUT} is the desired output ripple
- F_{SW} is the switching frequency

The maximum ESR (ESR_{MAX}) can be calculated by:

$$ESR_{MAX} = \frac{\Delta V_{OUT}}{\frac{V_{OUT} + V_{IN\_MIN}}{V_{IN\_MIN}} \times I_{OUT} + \frac{I_{RIPPLE\_BUCKBOOST}}{2}} = \frac{15\ V \times 2\%}{\frac{15\ V + 3\ V}{3\ V} \times 2 + \frac{15.4\ A}{2}} = 15.2\ m\Omega \quad (16)$$

where:

- $I_{RIPPLE\_BUCKBOOST}$ is the inductor ripple current in buck-boost mode
- V_{IN_MIN} is the minimum input voltage
- ΔV_{OUT} is the derivation of the output voltage

One 150-µF electrolytic capacitor is added for buck capacitance and at the mean time increase the V_{OUT} hold-up time. Multiple 22-µF capacitors are applied to achieve the ESR required. Two 0.22-µF ceramic capacitor are placed at the output pins of the LM5118-Q1 to reduce the high frequency noise.

2.2.6 Bias Supply Path

The LM5118 has internal architecture, which allows the system to increase tolerance to the low input voltage. This feature is introduced through the VCCX pin. Whenever the voltage at the VCCX pin is greater than 3.9 V, the internal VCC regulator is disabled and the VCC pin is internally connected to VCCX pin supply. With an auxiliary bias supply the device can function properly with input voltage down to 3 V, which is the most severe battery cold cranking situation.

In this design, the output voltage of the LM5118 is connected to the VCCS pin (as shown in Figure 5) in order to:

1. Reduce the IC power dissipation.
2. Bias the internal regulator and decrease the device UVLO level allowing for the input voltage drop.

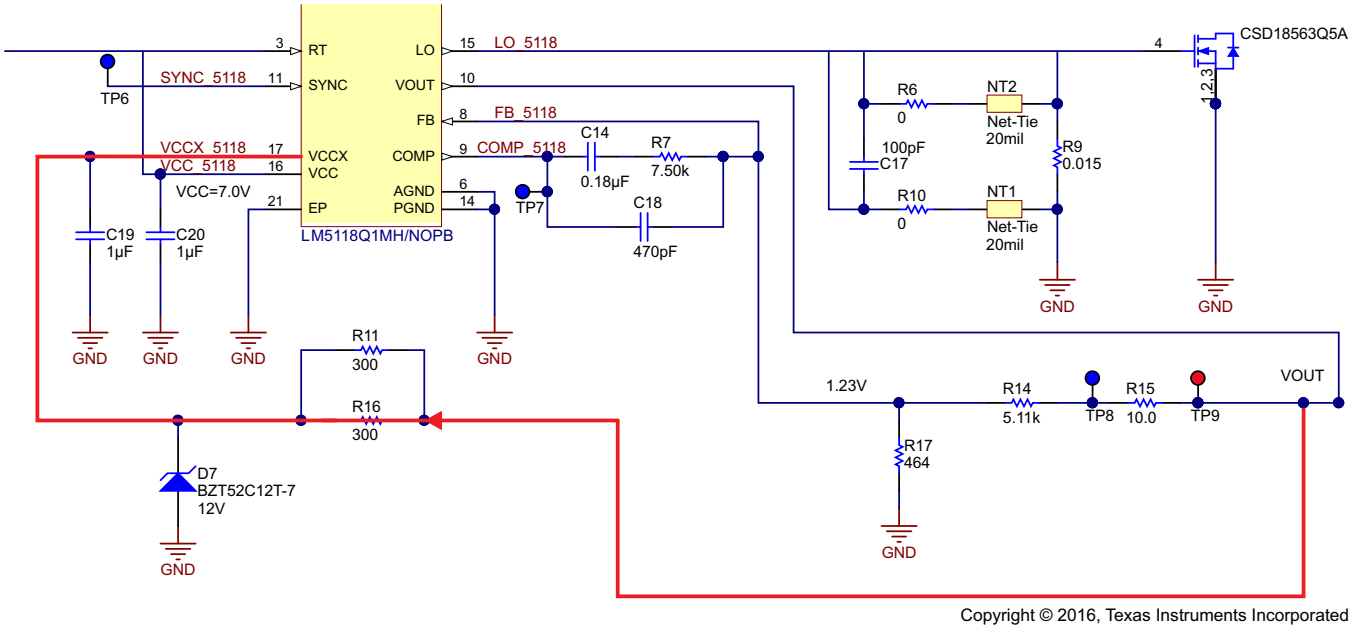


Figure 5. Bias Supply Path From LM5118 Output for Power Saving and Decreasing UVLO During Input Voltage Drop

However, the voltage applied to the VCCX pin must never exceed 15 V. Considering reliability of the design, one Zener diode (D7) with two current limiting resistors (R11 and R16) are placed at the pin for over voltage protection.

2.2.7 Calculated Control Loop Frequency Response

The LM5118 implements Type II error amplifier compensation which is provided by C14, R7 and C18 (shown in Figure 4). For most conditions, the regulator will need a phase margin between 60 and 90 degrees at the cross over frequency. The Right-Half-Plane (RHP) zero complicates the compensation. The empirical approach is to reduce the loop gain to cross zero at about 25% of the calculated RHP zero frequency. The second pole must be placed close to the RHP zero. Place the error amplifier zero near the dominate modulator pole. The LM5118 component calculation tool [4] is used for compensation network components calculation.

Figure 6 shows the calculated gain and phase margin plots in buck-boost mode and Figure 7 shows the calculated gain and phase margin plots in buck mode. The converter mainly works under buck-boost mode. Therefore, an overall phase margin of about 75° can be expected with implemented compensation component values.

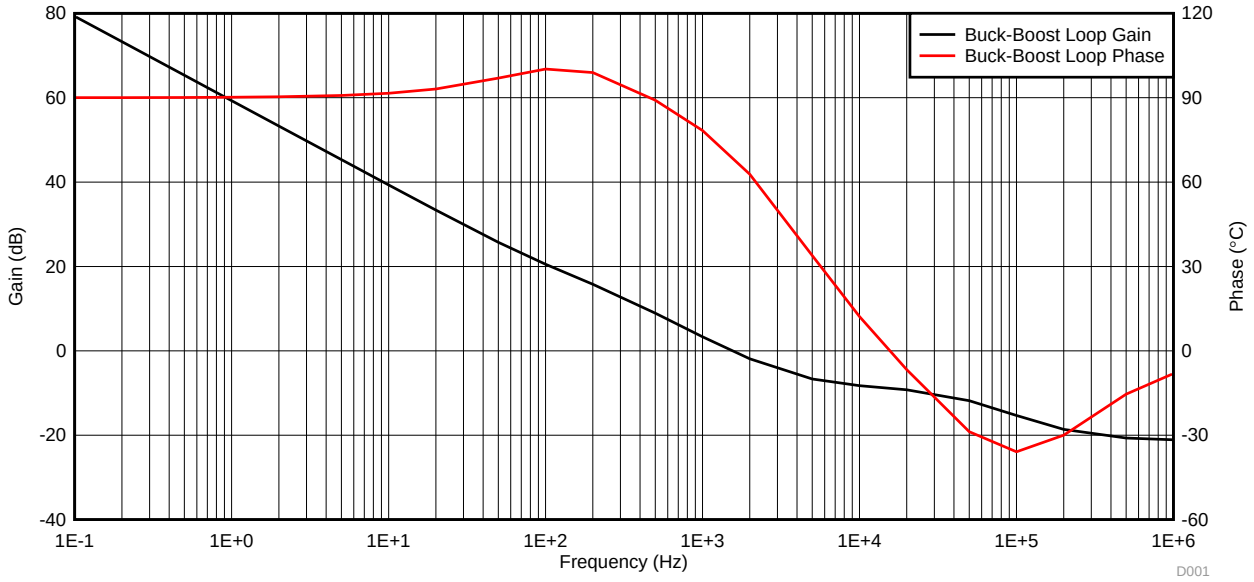


Figure 6. Calculated Loop Response of LM5118 Buck-Boost Modulator

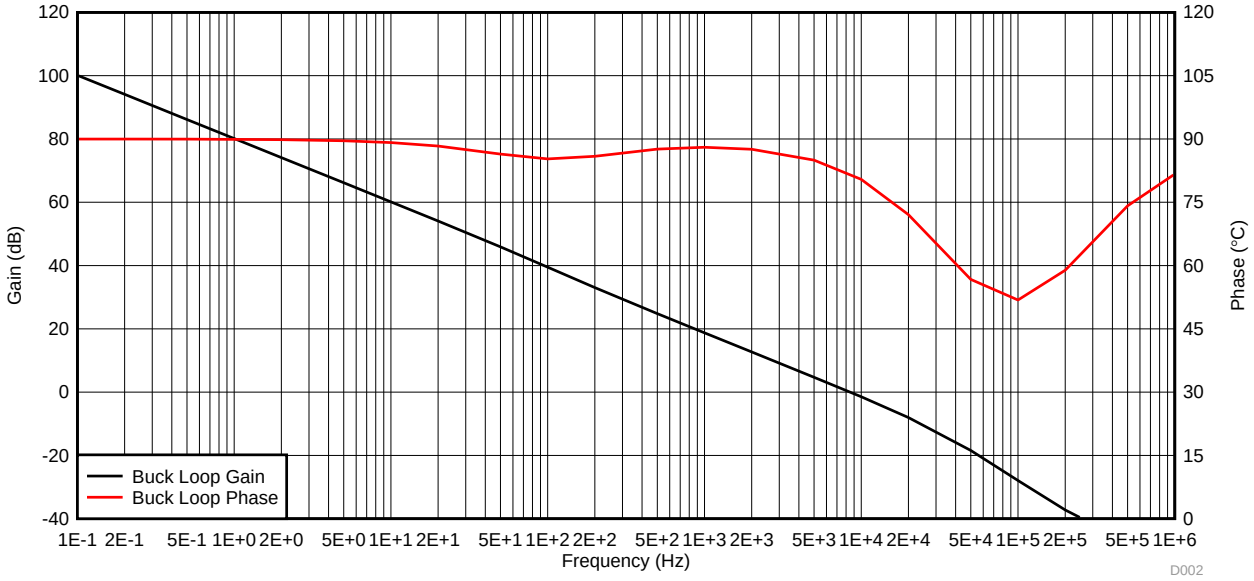


Figure 7. Calculated Loop Response of LM5118 Buck Modulator

2.3 Buck Converter

This section lists the procedure for calculating the surrounding components of the buck converter. The design specifications are shown in Table 3. A schematic of the buck converter is shown in Figure 8.

Table 3. Buck Converter Specifications

PARAMETER	SPECIFICATION
Input voltage (V_{IN})	9 to 20 V
Output voltage (V_{OUT})	5 V
Output ripple	± 2%
Maximum output current (I_{OUT_MAX})	4.5 A
Switching frequency	400 kHz
Maximum output power (P_{OUT_MAX})	22.5 W

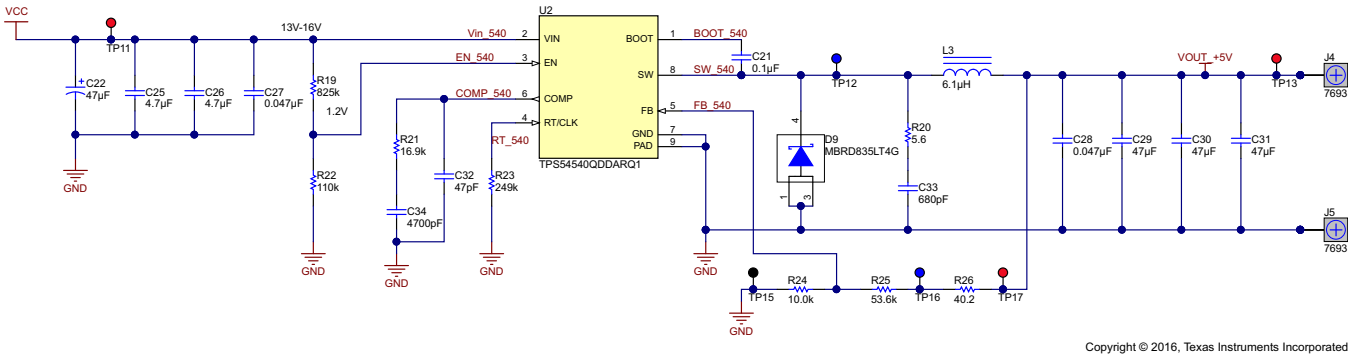


Figure 8. Schematic of 15- to 5-V DC/DC Buck Converter

2.3.1 Switching Frequency

The switching frequency of the TPS54540 is limited by the limited on-time of the internal power switch. The switching frequency is set by the oscillation resistor, which is connected to the RT pin (R23 in Figure 8). A switching frequency of 400 kHz is selected as a compromise between component size and efficiency. The value of RT is calculated as:

$$R_T = \frac{92417}{F_{SW}^{0.991}} = 243\ k\Omega \quad (17)$$

where:

- F_{SW} is the switching frequency

2.3.2 Inductor Selection

The minimum required inductance (L_{MIN}) is calculated as:

$$L_{MIN} = \frac{V_{IN\_MAX} - V_{OUT}}{I_{OUT} \times K_{IND}} \times \frac{V_{OUT}}{V_{IN\_MAX} \times F_{SW}} = \frac{16 - 5}{4.5 \times 0.3} \times \frac{5}{16 \times 400k} = 6.3\ \mu H \quad (18)$$

where:

- K_{IND} is a ratio of the inductor ripple current to the maximum output current
- V_{IN_MAX} is the maximum input voltage
- F_{SW} is the switching frequency of the converter

The RMS and peak current flowing through the inductor must not exceed the inductor RMS current and saturation ratings. The ripple current flowing into the inductor is calculated as:

$$I_{RIPPLE} = \frac{V_{OUT} \times \left(V_{IN\_MAX} - V_{OUT}\right)}{V_{IN\_MAX} \times L \times F_{SW}} = \frac{5 \times (16 - 5)}{16 \times 6.3\ \mu H \times 400k} = 1.36\ A \quad (19)$$

where:

- V_{OUT} is the output voltage
- F_{SW} is the switching frequency
- L is the output inductance
- V_{IN_MAX} is the maximum input voltage

The RMS and peak inductor currents are calculated as:

$$I_{L\_RMS} = \sqrt{\left(I_{OUT}\right)^2 + \frac{1}{12} \times \left(\frac{V_{OUT} \times \left(V_{IN\_MAX} - V_{OUT}\right)}{V_{IN\_MAX} \times L \times F_{SW}}\right)} = \sqrt{(4.5)^2 + \frac{1}{12} \times \left(\frac{5 \times (16 - 5)}{5 \times 6.3\ \mu H \times 400k}\right)} = 4.5\ A \quad (20)$$

where:

- I_{OUT} is the output current
- V_{OUT} is the output voltage
- F_{SW} is the switching frequency
- L is the output inductance

$$I_{L\_PEAK} = I_{OUT} + \frac{I_{RIPPLE}}{2} = 4.5\ A + \frac{1.36\ A}{2} = 5.18\ A \quad (21)$$

where:

- I_{OUT} is the output current
- I_{RIPPLE} is the ripple current flowing into the inductor

The AEC-Q200 grade inductor with a 6.1-µH inductance, 7.6-A rated current, and 8.6-A saturation current is selected for this design.

2.3.3 Input Capacitors

The TPS54540-Q1 requires a high quality ceramic type X5R or X7R input decoupling capacitor with at least 3 µF of effective capacitance. Capacitance loss due to DC bias effects must be taken into account. The ripple current rating of the capacitor must be higher than the maximum input ripple current of the converter.

The input ripple current (I_{IN_RMS}) is calculated as:

$$I_{IN\_RMS} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN\_MIN}} \times \frac{\left(V_{IN\_MIN} - V_{OUT}\right)}{V_{IN\_MIN}}} = 4 \times \sqrt{\frac{5}{14} \times \frac{(14 - 5)}{14}} = 1.92\ A \quad (22)$$

where:

- I_{OUT} is the output current
- V_{IN_MIN} is the minimum input voltage
- V_{OUT} is the output voltage

A 47-µF electrolytic capacitor with two 4.7-µF ceramic capacitors and one 0.047-µF ceramic capacitor are used at the input in this design.

The input capacitance determines the input ripple voltage of the regulator. The maximum input voltage ripple occurs at 50% duty cycle and can be calculated as:

$$\Delta V_{IN} = \frac{I_{OUT} \times 0.25}{C_{IN} \times F_{SW}} = \frac{4.5\ A \times 0.25}{56.4\ \mu F \times 400\ kHz} = 49.8\ mV \quad (23)$$

where:

- I_{OUT} is the output current
- C_{IN} is the selected input capacitance
- F_{SW} is the switching frequency

2.3.4 Output Capacitors

There are three primary considerations for selecting the value of the output capacitor. The output capacitor determines the converter compensation network, the output voltage ripple, and the load transient response of the converter.

To maintain the output voltage during load current abrupt change is the first criteria. The output capacitance must be large enough to supply the difference for two clock cycles within the specified range. To meet this requirement the output capacitance is calculated as:

$$C_{OUT} > \frac{2 \times \Delta I_{OUT}}{F_{SW} \times \Delta V_{OUT}} = \frac{2 \times 4.5\ A}{400\ kHz \times 5 \times 5\%} = 90\ \mu F \quad (24)$$

where:

- ΔI_{OUT} is the output current change
- F_{SW} is the switching frequency
- ΔV_{OUT} is the allowable change in the output voltage

The output capacitor must also be sized to absorb energy used in the inductor when transitioning from a high to a low load. Three 47-μF ceramic capacitors are implemented and connected in parallel.

2.3.5 Calculated Control Loop Frequency Response

The TPS54540-Q1 voltage regulation loop is controlled by a trans-conductance error amplifier. The error amplifier compares the FB pin voltage to the lower of the internal soft-start voltage or the internal 0.8-V voltage reference. The trans-conductance (gm) of the error amplifier is 350 μA/V during normal operation.

The TPS54540 component calculation tool [5] is used for compensation network components calculation. Figure 9 shows the calculated gain and phase margin plots of the TPS54540-Q1 buck converter.

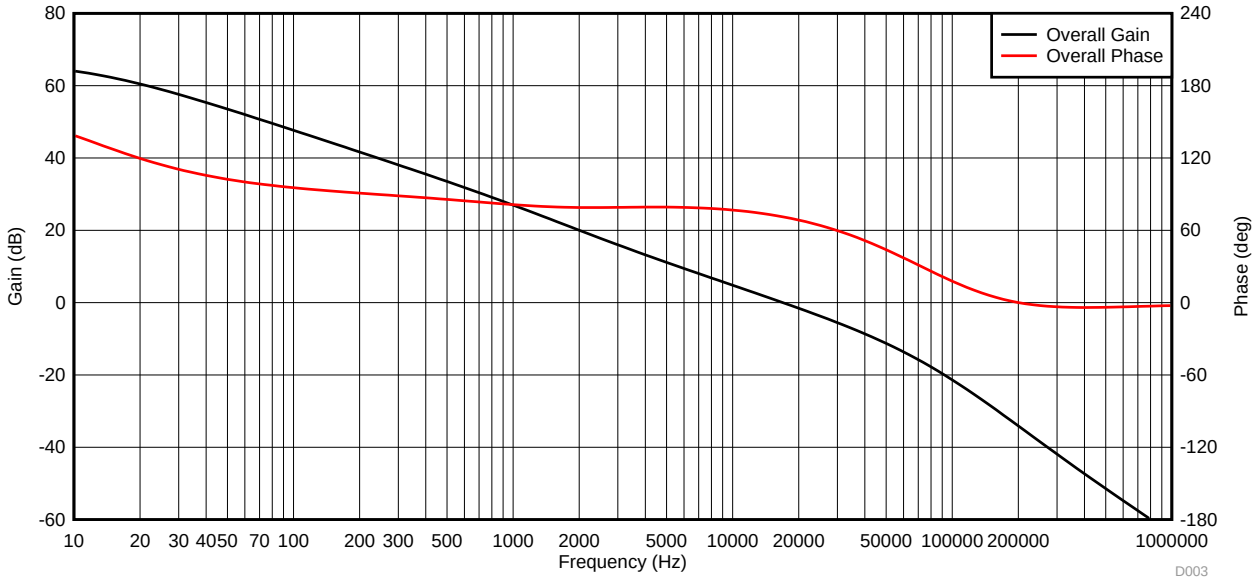


Figure 9. Calculated Loop Response of LM54540-Q1 Buck Converter

2.4 EMI Filter

EMI compliance is very stringent in current automotive environment in order to avoid interference with other subsystems. The important automotive standards that are most applicable to front-end power supplies are conducted in the test: SO7637-2, ISO16750-2, and CISPR25. The filter design discussed in this section targets for suppressing conducted emissions. Radiated emission mainly depends on the board layout and switching speed of the MOSFETs.

2.4.1 DM Filter Design

The differential-mode (DM) filter suppresses the noise in low frequency range. Two C-L-C Pi filters, which creates a two-stage filter for the whole system, are added at the input of the buck-boost converter and the input of the buck converter, respectively. This is because:

1. For the buck converter, most of the conducted noise is generated at the input. The on and off switching of the buck switch generates large switching currents.
2. For the buck-boost converter, the conducted noise is generated at both of the input and output. Therefore, the EMI filter implemented at the input of buck converter serves for the buck-boost output at the mean time.

The designed EMI filter is mainly for conducted emission suppression. Radiated emission mainly depends on the board layout and switching speed of the MOSFETs. Schematics of the filters are shown in Figure 10 and Figure 11, respectively. The component values are calculated according to the application report [1].

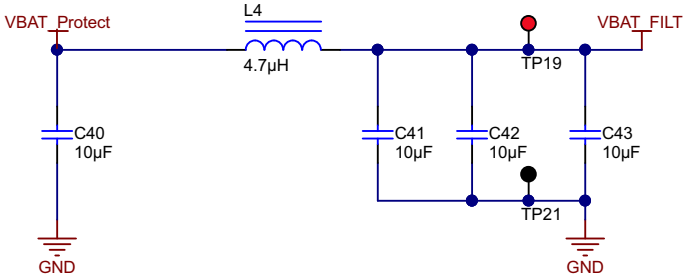


Figure 10. Schematic of DM EMI Filter for Buck-Boost Converter

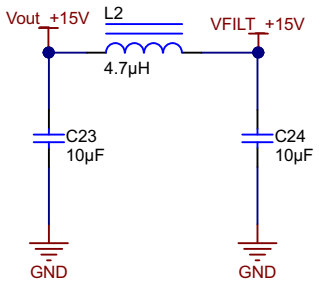


Figure 11. Schematic of DM EMI Filter for Buck Converter

The CISPR25 spec does not define a limit at 320 kHz for components or modules, while at a middle frequency range (from 530 kHz to 1.8 MHz) it is defined as a 54-dBµV peak for class 5 [6]. Therefore, for the buck-boost converter the required attenuation is calculated as:

$$Att_{dB} = 20 \times \log\left(\frac{\frac{I_L}{\pi^2 \times F_{SW} \times C_{IN}} \sin(\pi D)}{1\,\mu V}\right) - V_{ST(dB)}$$

$$Att_{dB} = 20 \times \log\left(\frac{\frac{7.9\ A}{\pi^2 \times 320k \times 6.6\ \mu F} \sin(\pi \times 0.833)}{1\,\mu V}\right) - 54\ dB = 30.76\ dB \quad (25)$$

where:

- Att_{dB} is the required attenuation for the designed input filter
- D is the maximum duty cycle of the buck-boost converter
- I_L is the DC inductor current
- F_{SW} is the switching frequency
- C_{IN} is the low ESR ceramic type input capacitor of the converter
- $V_{ST(dB)}$ is the noise level prescribed by the EMC standard in dB.

The first order capacitor (C_f) is calculated based on Equation 26 and Equation 27:

$$C_{1a} = \frac{C_{IN}}{C_{IN} \times L_f \times \left(\frac{2\pi \times F_{SW}}{10}\right)^2 - 1} = \frac{6.6\ \mu F}{6.6\ \mu F \times 4.7\ \mu H \times \left(\frac{2\pi \times 320k}{10}\right)^2 - 1} = 26.1\ \mu F \quad (26)$$

where:

- C_{IN} is the low ESR ceramic type input capacitor of the converter
- F_{SW} is the switching frequency
- L_f is the filter inductance

$$C_{1b} = \frac{1}{L_f} \times \left(\frac{10^{Att_{dB}/40}}{2\pi \times F_{SW}}\right)^2 = \frac{1}{4.7\ \mu H} \times \left(\frac{10^{30.76/40}}{2\pi \times 320k}\right)^2 = 1.8\ \mu F \quad (27)$$

A 10-µF capacitor is implemented as a compromise from values of C_{1a} and C_{1b}. Thus, the corner frequency of the filter is placed at:

$$f_c = \frac{1}{2\pi \times \sqrt{L_f \times C_f}} = \frac{1}{2\pi \times \sqrt{4.7\ \mu H \times 10\ \mu F}} = 23.2\ kHz \quad (28)$$

The corner frequency is 10 times lower than the switching frequency. Since a second-order filter is applied, 40 dB of attenuation at the switching frequency is expected. A damping capacitor C_d with high ESR is applied on the output of the filter. The purpose is to increase the input impedance of the boost converter thus decrease the oscillations between filter and the converter. The value is selected as:

$$C_d \geq 4 \times C_{IN} = 4 \times 6.6\ \mu F = 26.4\ \mu F \quad (29)$$

ESR of C_d is calculated as:

$$ESR_{Cd} \geq \sqrt{\frac{L_f}{C_1}} = \sqrt{\frac{4.7\ \mu H}{10\ \mu F}} = 0.68\ \Omega \quad (30)$$

A high value 150-µF electrolytic input capacitor is implemented at the input of the buck-boost converter, which also helps to hold-up the input power during battery cold cranking situation.

As the 23.3-kHz corner frequency is also effective for the buck converter which switches at 400 kHz, the same values of the filter inductance and capacitance are implemented for the buck converter in order to consolidate the BOM cost.

2.4.2 CM Filter

A common-mode (CM) filter is essential in filtering the noise in the high frequency range. CM chokes in combination with Y capacitors are commonly used and placed at the input of the system for CM noise suppression. The CM choke needs to present high impedance over a broad high frequency range. One CM choke example is shown in reference [3]. The CM filter is not included into this design considering that there is no connecting point to the Protective Earth (PE) for Y capacitors. However, EMI tests are performed in Section 5 and guidelines are given for CISPR 25 conducted EMC compliance.

3 Automotive Tests and EMC Standards

Compliance with automotive tests and EMC standards is one of the main focuses for this design. The focuses are those most applicable to front-end (off-battery) power supplies: ISO 7637-2, ISO 16750-2, and CISPR25. The focused tests are detailed in this section. See their original standard documents for more details [6][7][8]. Those standards are the guideline that the automotive OEMs will base on. Each OEM has internal standards that specify the levels and testing that components used in their vehicles must meet. The levels vary but are not significant:

1. ISO 7637-2 Pulse 1
2. ISO 7637-2 Pulse 2a
3. ISO 7637-2 Pulse 3a and 3b
4. ISO 7637-2 Pulse 5b
5. ISO 16750-2 Jump Start
6. ISO 16750-2 Reversed Voltage
7. ISO 17650-2 Cold Cranking
8. CISPR 25 Conducted Emissions

The electrical transient tests in this standard are designed to see how the subsystem behaves before, during, and after these events. The required behavior can be classified into multiple "Functional Classes":

- Functional Class A
  All functions of the device or system perform as designed during and after the test.
- Functional Class B
  All functions of the device or system perform as designed during the test. However, one or more may go beyond the specified tolerance. All functions return automatically to within normal limits after the test. Memory functions remain Class A.
- Functional Class C
  One or more functions of a device or system do not perform as designed during the test but return automatically to normal operation after the test.
- Functional Class D
  One or more functions of a device or system do not perform as designed during the test and do not return to normal operation after the test until the device or system is reset by a simple "operator/use" action.
- Functional Class E
  One or more functions of a device or system do not perform as designed during and after the test and cannot be returned to proper operation without repairing or replacing the device or system.

This TI Design targets at Class A where all functions of the device or system perform as designed during and after the test.

4 Getting Started Hardware

Figure 12 and Figure 13 show the PCB board image of TIDA-01179 from top side and bottomed side respectively. Placement of the devices are indicated.

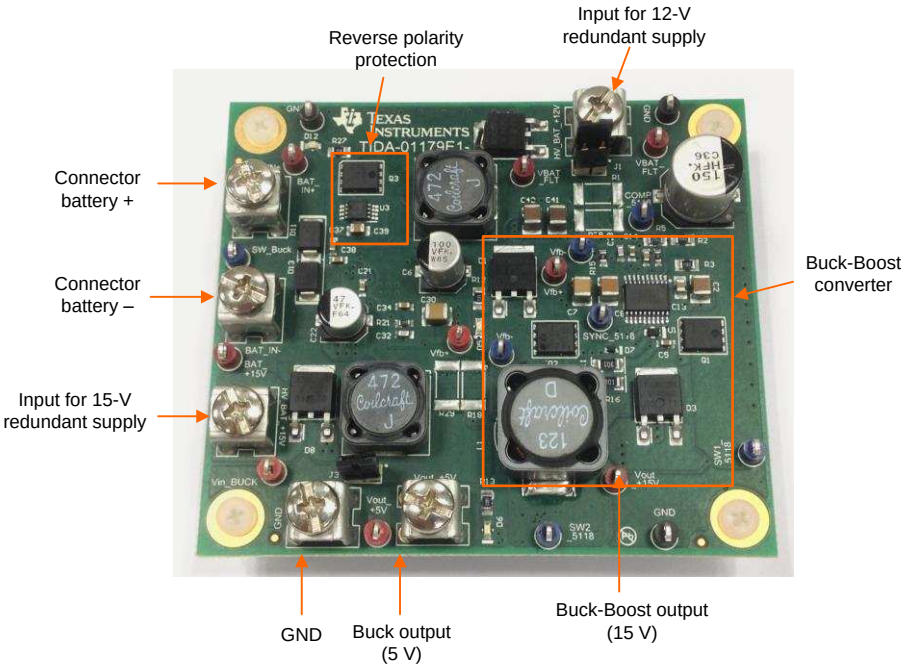


Figure 12. TIDA-01179 PCB Board Top Side

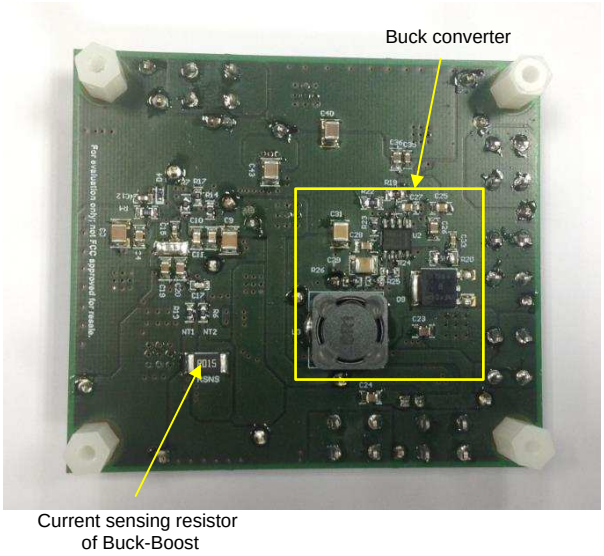


Figure 13. TIDA-01179 PCB Board Bottom Side

5 Testing and Results

5.1 Start-up

The startup waveforms of the buck-boost and buck converters are shown in Figure 14 and Figure 15, respectively. The soft start time is 12.4 ms for the buck-boost converter and 2.86 ms for the buck converter.

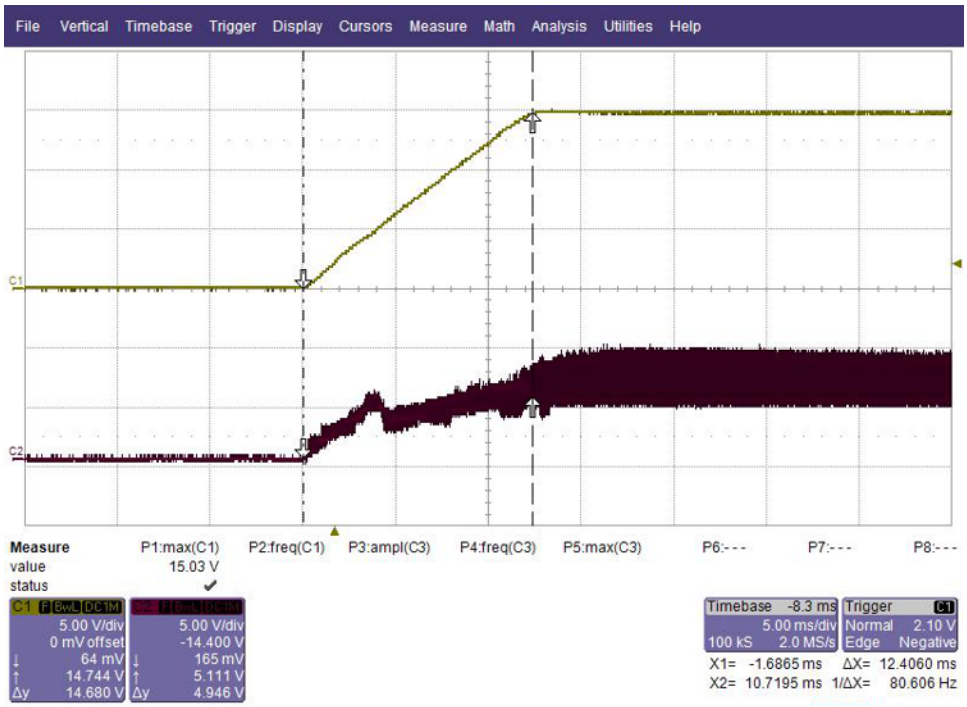


Figure 14. Start-up Waveform of Buck-Boost Converter

NOTE: CH1: Output voltage of the buck-boost converter, CH2: Boost switch node (SW2) of the buck-boost converter

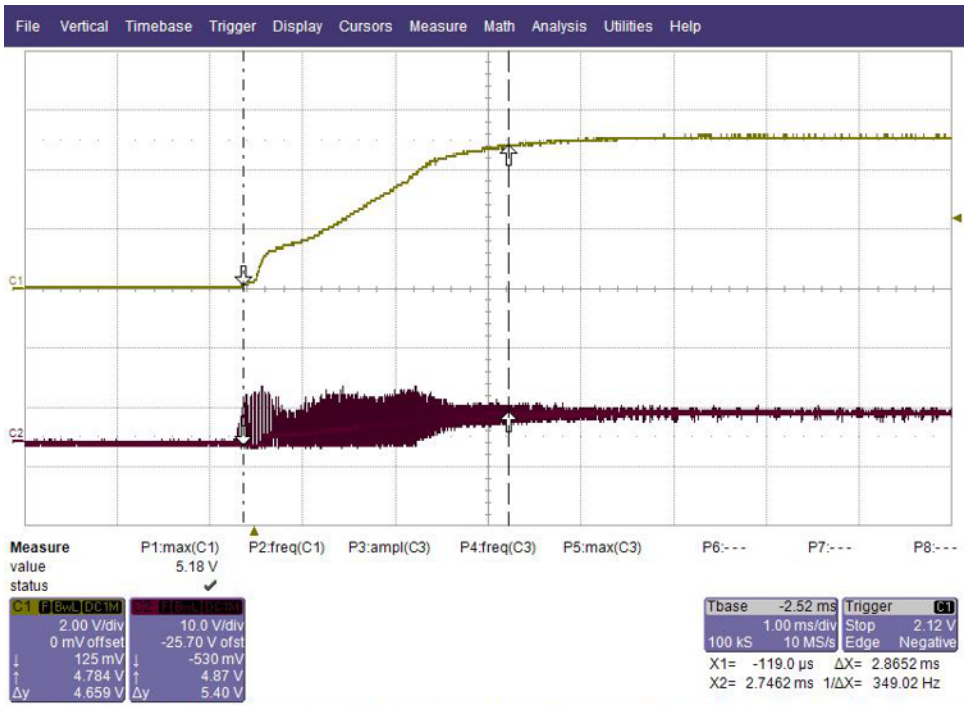


Figure 15. Start-up Waveform of Buck Converter

NOTE: CH1: Output voltage of the buck converter, CH2: Switch node of the buck converter

5.2 Efficiency

Efficiency of the buck-boost converter, the buck converter, and the total system (two converters connected in series) are measured respectively under conditions of different input voltages. The measurement setup is shown in Figure 16. Four digital multi-meters are used to measure the input voltage, input current, and output voltage, respectively. Output current is measured through the electronic load. When measuring the total system efficiency, two DC/DC converters are connected in series and load is connected to the buck converter only, as shown in Figure 17.

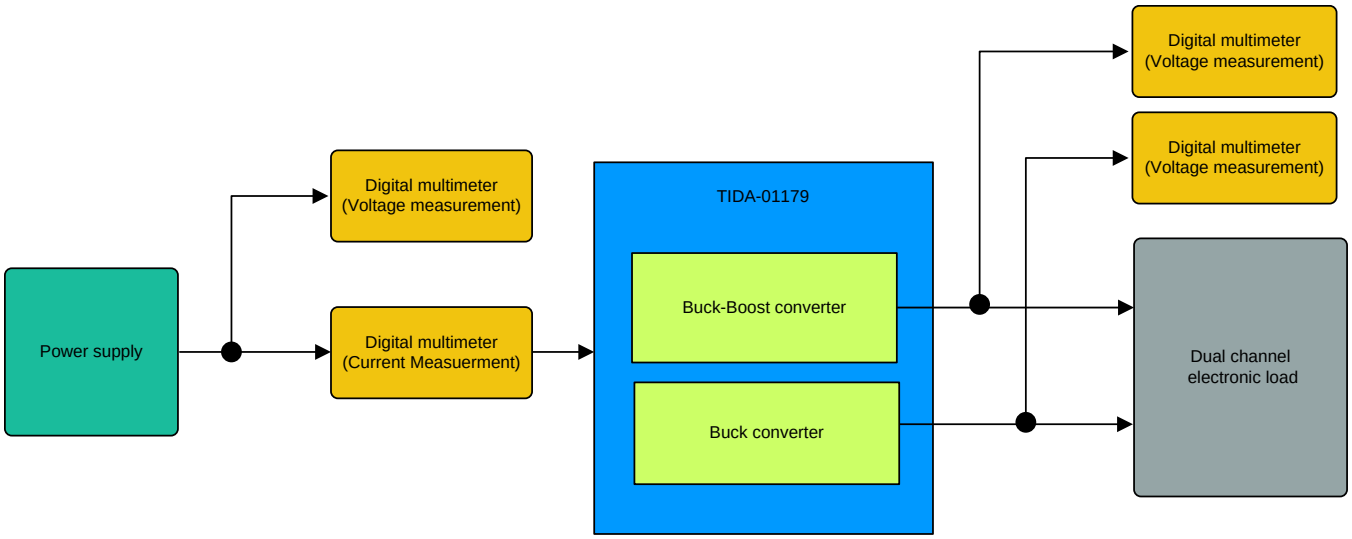


Figure 16. Experiment Setup for Measuring Efficiency of Two DC/DC Converters Separately

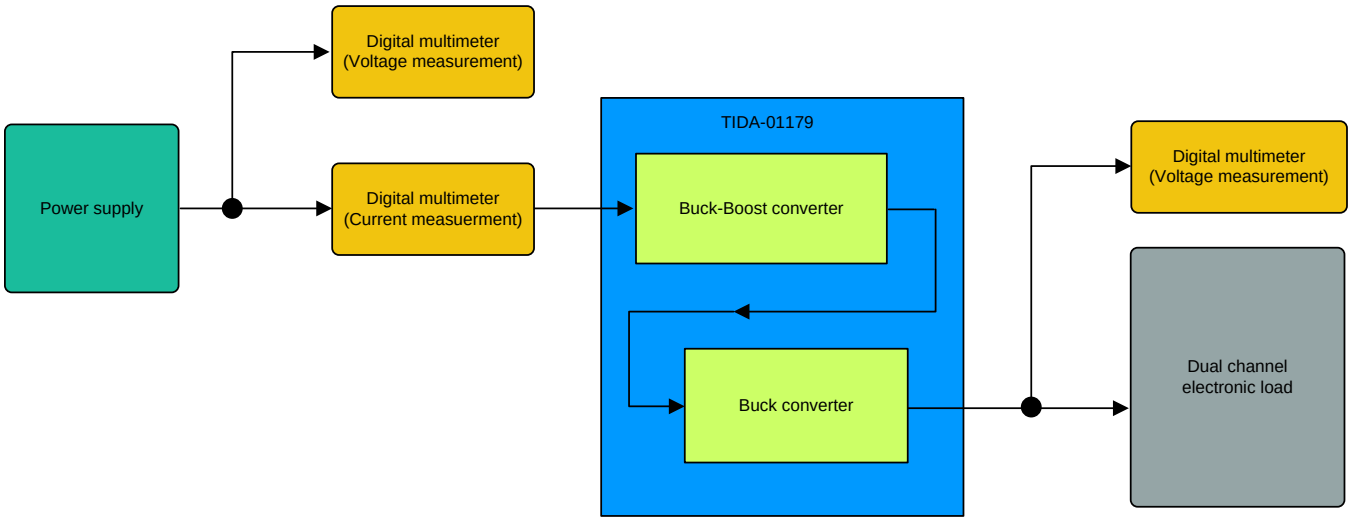


Figure 17. Experiment Setup for Measuring Efficiency of Total System

Figure 18 shows the measured efficiency of the LM5118 buck-boost converter solely. When 86% efficiency is achieved in the nominal operation mode, a higher efficiency is obtained when the LM5118 works under buck mode.

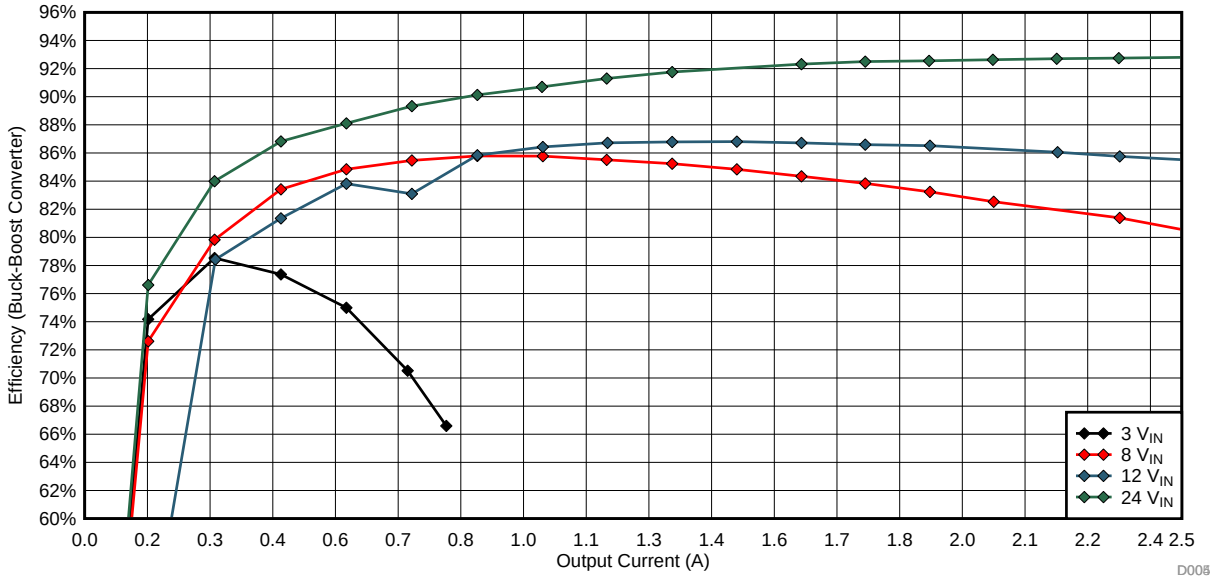


Figure 18. Measured Efficiency of Buck-Boost Converter

Figure 19 shows the measured efficiency of the buck converter solely. A peak efficiency of 92% is obtained at the 12-V input voltage. Most of the losses are dissipated on the external freewheeling diode.

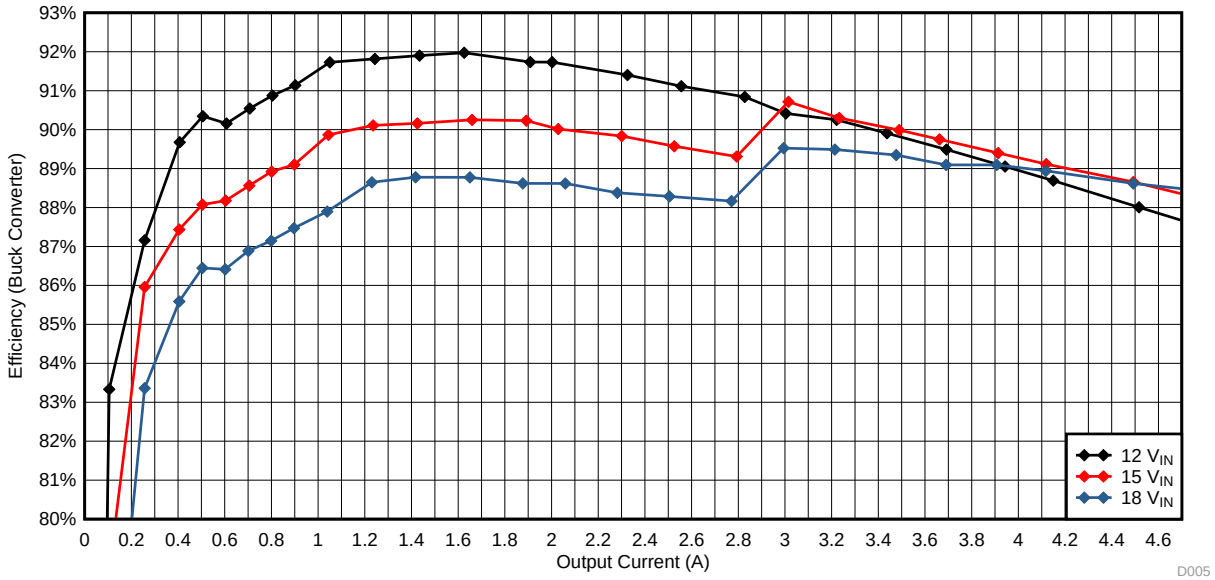


Figure 19. Measured Efficiency of Buck Converter

Figure 20 shows the measured efficiency of the total system. An overall efficiency of 75% can be expected when the input voltage is 12 V.

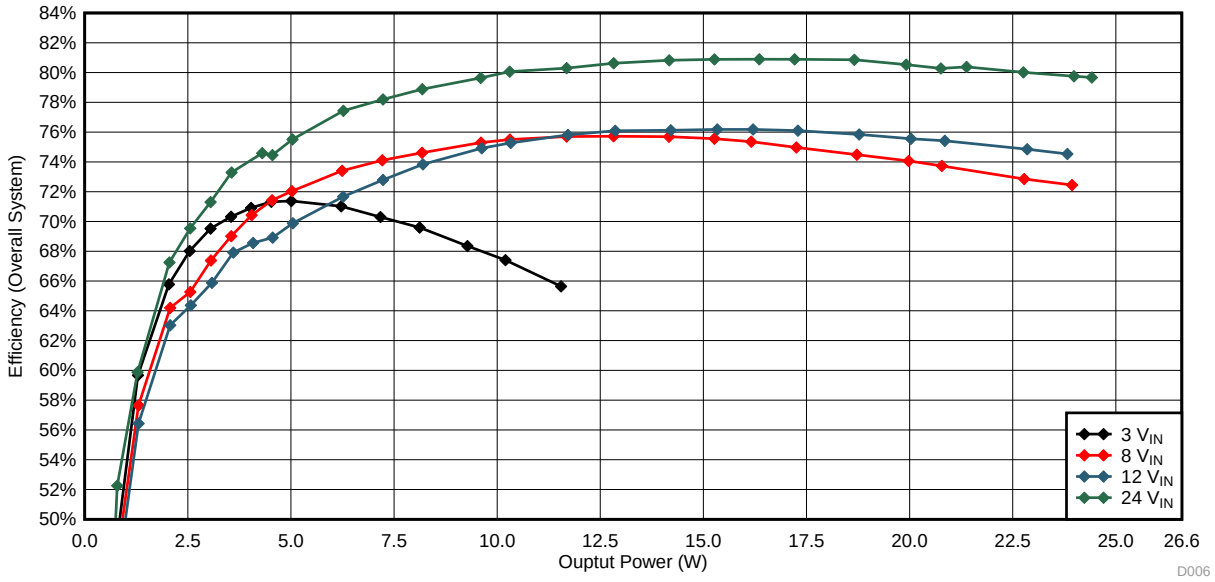


Figure 20. Measured Efficiency of Total System

5.3 Load Regulation

Load regulation measurements show the percent deviation from nominal output voltage as a function of output current at input voltages of: 3.0 V, 8 V, 12 V, and 24 V. The experiment setup is the same as that of the efficiency measurement, as shown in Figure 21.

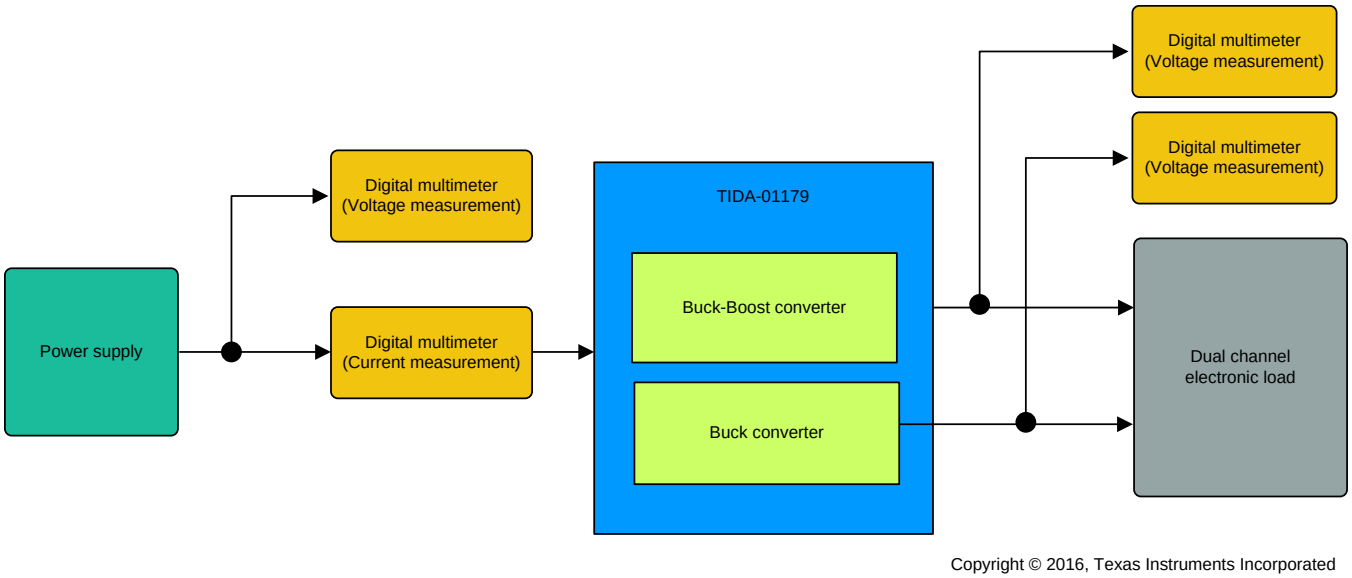


Figure 21. Experiment Setup for Measuring Load Regulation of Two DC/DC Converters

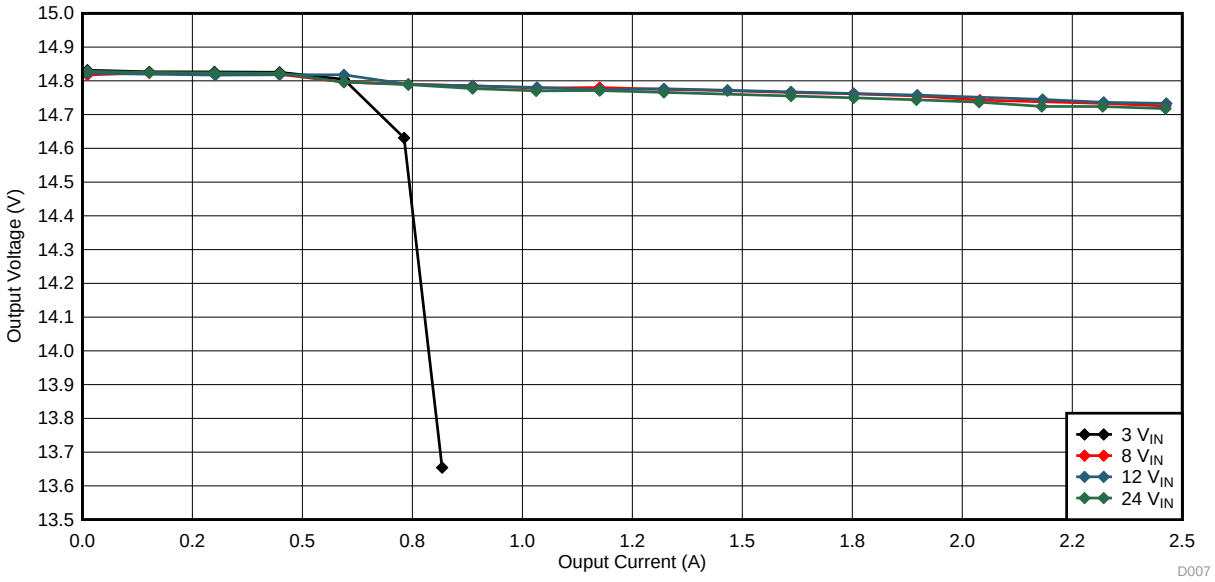


Figure 22. Load Regulation of Buck-Boost Converter

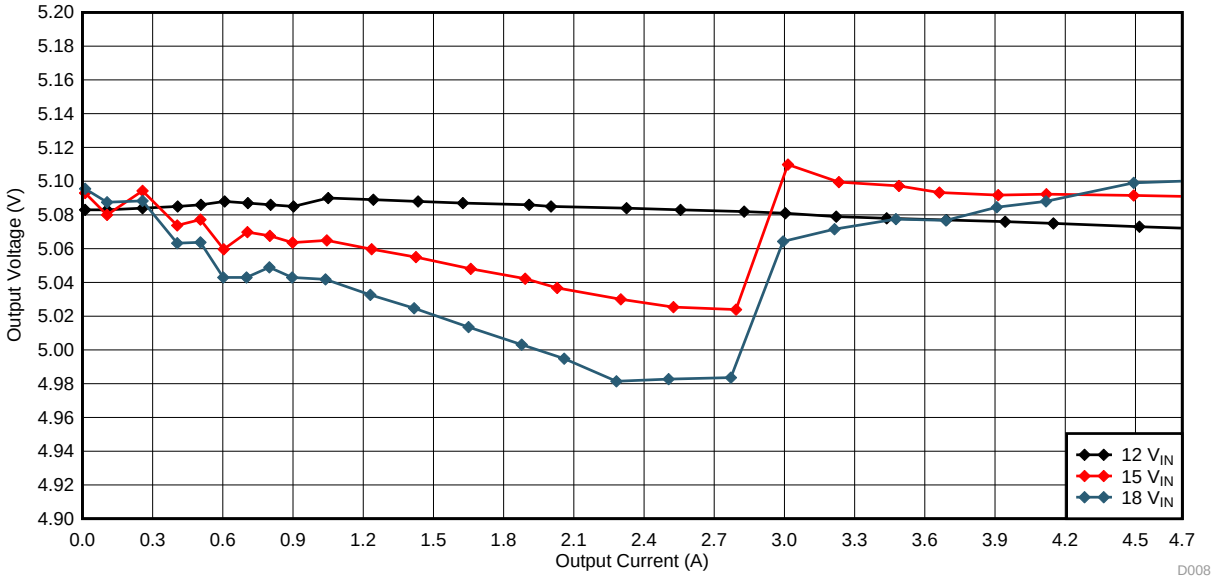


Figure 23. Load Regulation of Buck Converter

5.4 Output Voltage Ripple

The output voltage ripple of the buck-boost converter and buck converter are measured respectively under various input voltages and different load conditions.

5.4.1 Buck-Boost Converter

The output voltage ripples of the buck-boost converter under different input voltages (3 V, 8 V, and 13 V) and different loads (0.1 A, 0.6 A, and 2.2 A) are shown from Figure 24 to Figure 29.

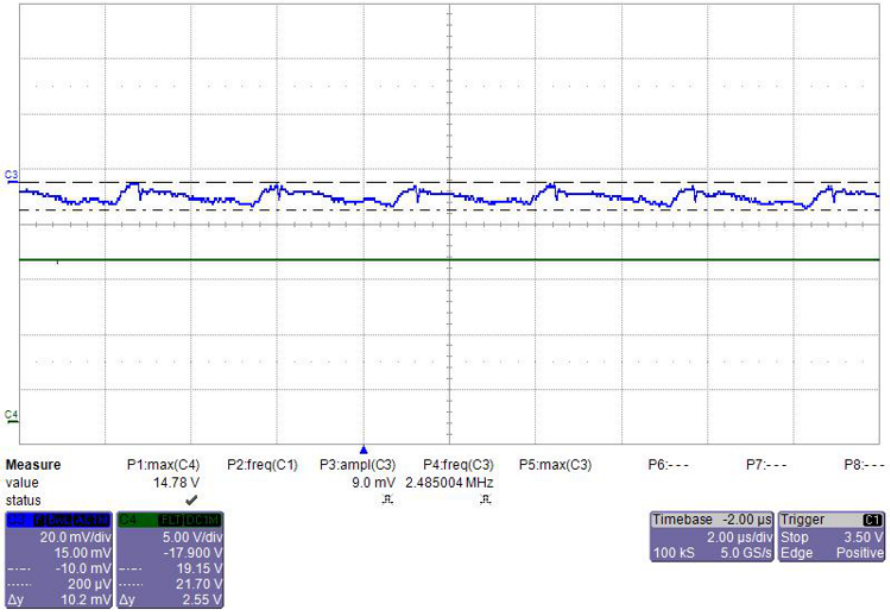


Figure 24. Output Voltage Ripple of Buck-Boost Converter Under V_{IN} = 3.0 V and I_{OUT} = 0.1 A

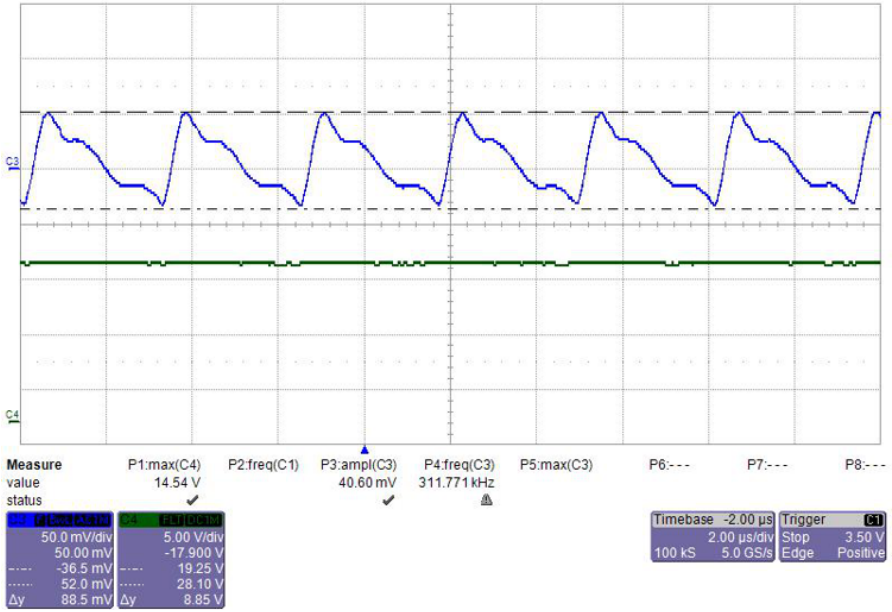


Figure 25. Output Voltage Ripple of Buck-Boost Converter Under V_{IN} = 3.0 V and I_{OUT} = 0.6 A

NOTE: CH3: Output voltage ripple of the buck-boost converter, CH4: Output voltage of the buck-boost converter

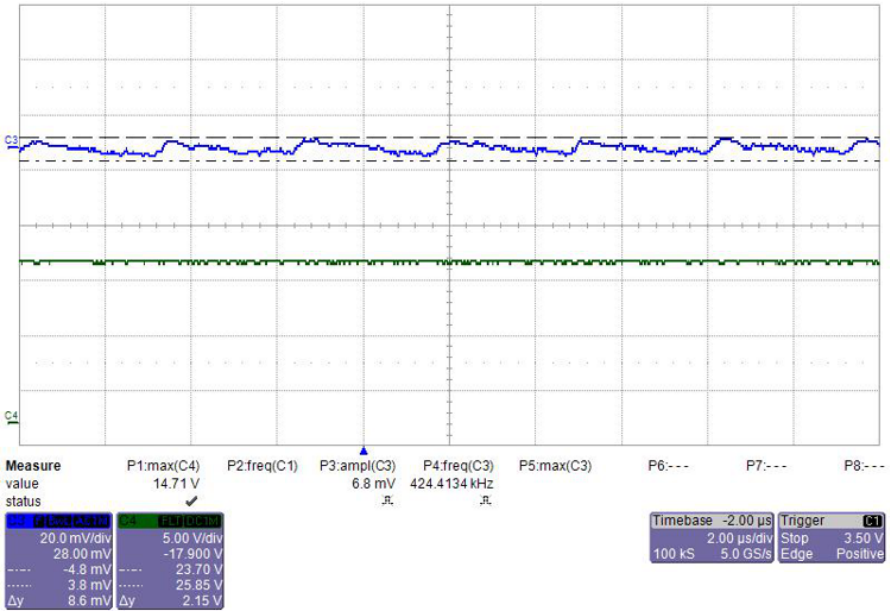


Figure 26. Output Voltage Ripple of Buck-Boost Converter Under V_{IN} = 8 V and I_{OUT} = 0.1 A

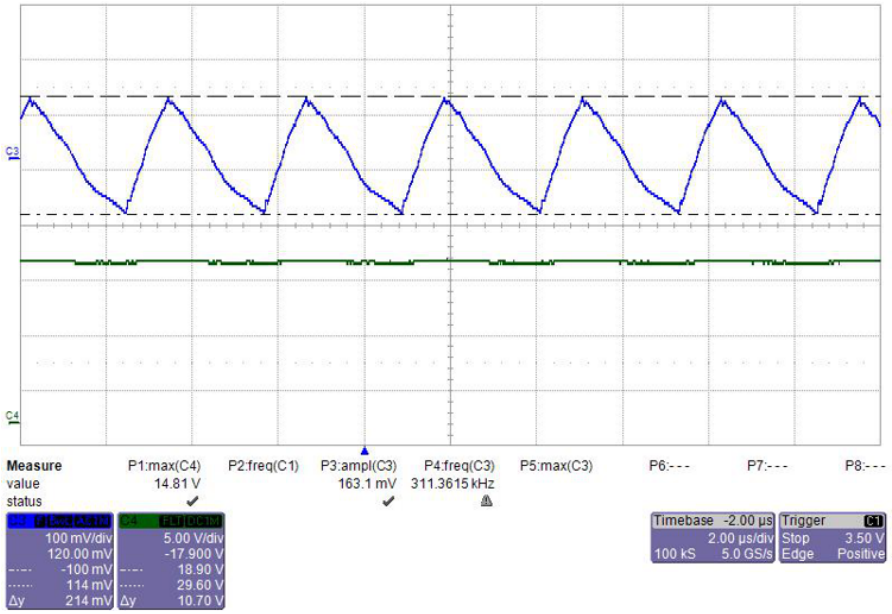


Figure 27. Output Voltage Ripple of Buck-Boost Converter Under V_{IN} = 8 V and I_{OUT} = 2.2 A

NOTE: CH3: Output voltage ripple of the buck-boost converter, CH4: Output voltage of the buck-boost converter

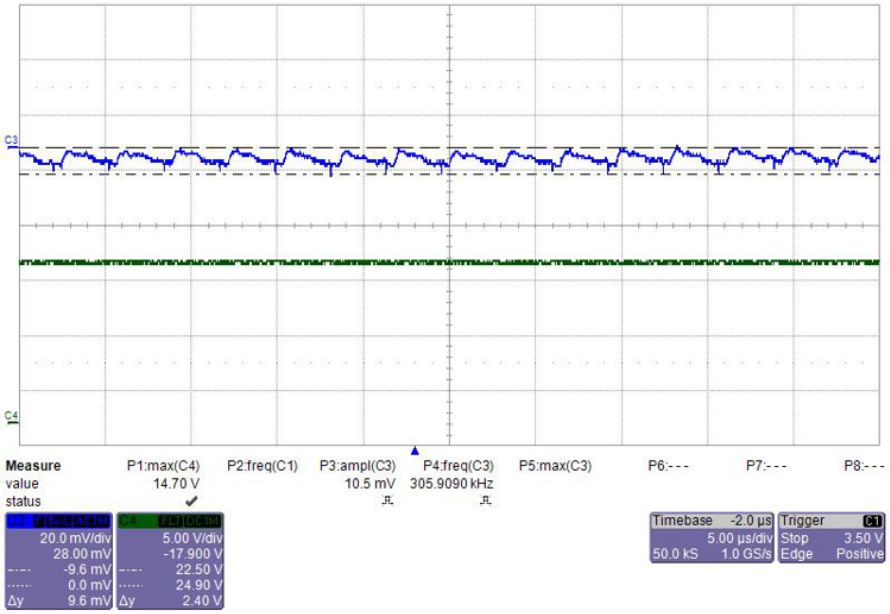


Figure 28. Output Voltage Ripple of Buck-Boost Converter Under V_{IN} = 13 V and I_{OUT} = 0.1 A

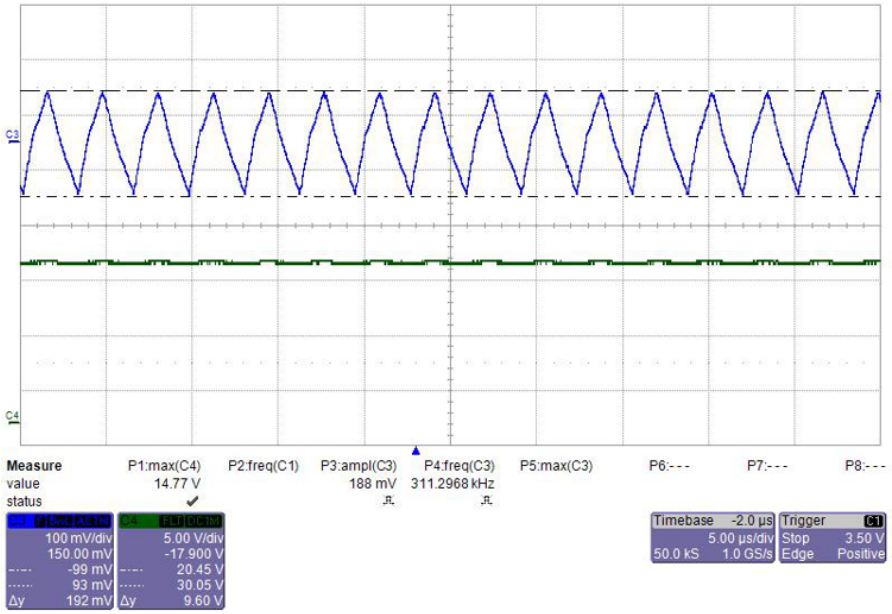


Figure 29. Output Voltage Ripple of Buck-Boost Converter Under V_{IN} = 13 V and I_{OUT} = 2.2 A

NOTE: CH3: Output voltage ripple of the buck-boost converter, CH4: Output voltage of the buck-boost converter

5.4.2 Buck Converter

Output voltage ripples of the buck converter under a 15-V input and different loads (0.1 A and 4.1 A) are shown in Figure 30 and Figure 31.

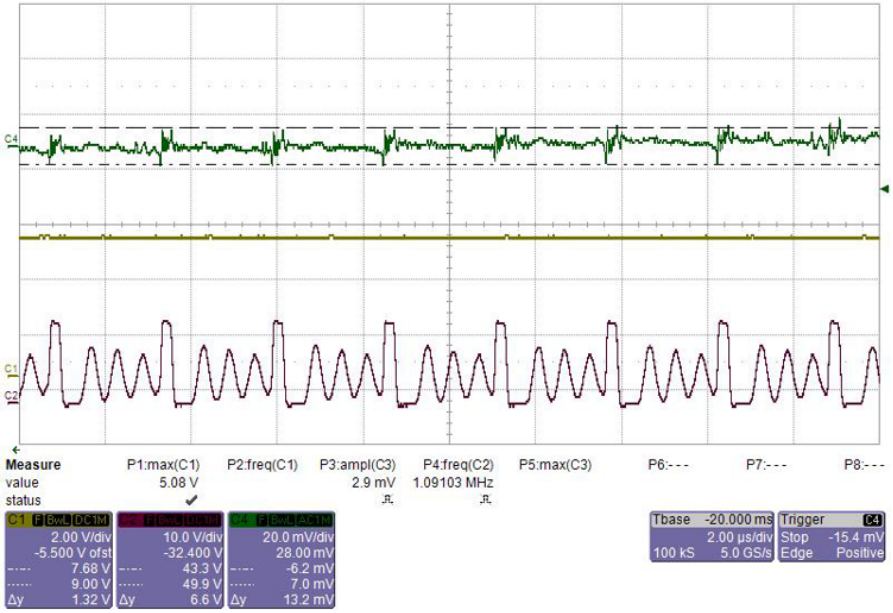


Figure 30. Output Voltage Ripple of Buck Converter Under V_{IN} = 15 V and I_{OUT} = 0.1 A

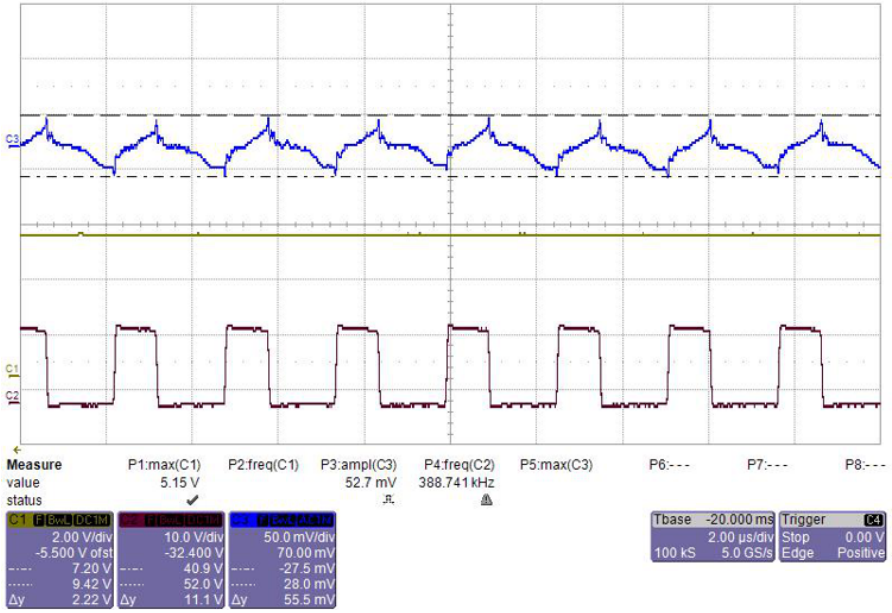


Figure 31. Output Voltage Ripple of Buck Converter Under V_{IN} = 15 V and I_{OUT} = 4.1 A

NOTE: CH4: Output voltage ripple of the buck converter, CH1: Output voltage of the buck converter, CH2: Switching node of the buck converter

5.5 Load Transients

5.5.1 Buck-Boost Converter

NOTE: For Figure 32 through Figure 35:
CH2: Output voltage ripple of the buck-boost converter, CH1: Load current of the buck-boost converter

Figure 32 shows the load transient response of the buck-boost converter. The load is switching from 1 to 2.2 A with a period of 36 ms. The input voltage is set to 13 V.

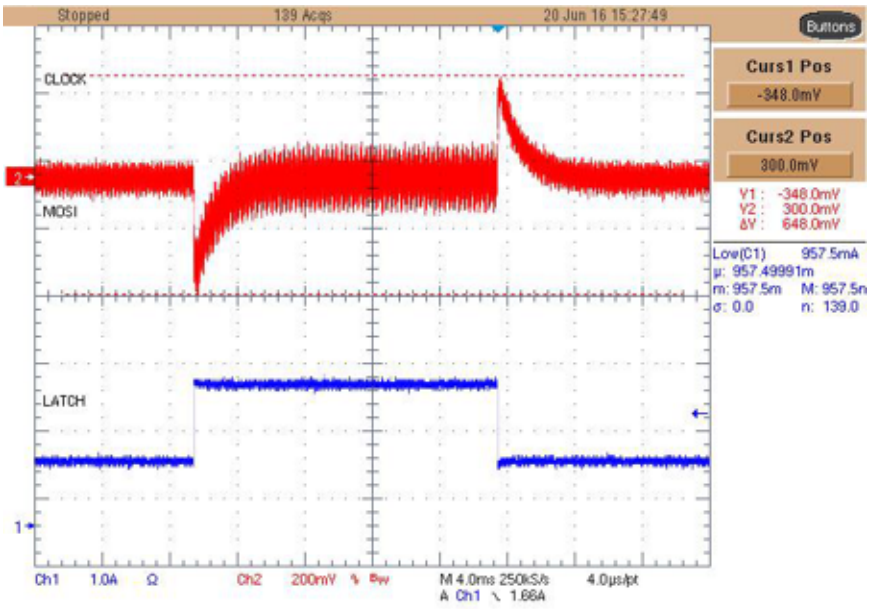


Figure 32. Load Transient Response of Buck-Boost Converter Under V_{IN} = 13 V and I_{OUT} Switching Between 2.2 A and 1 A

Figure 33 shows the load transient response of the buck-boost converter. The load is switching from 1 to 2.2 A with a period of 36 ms. The input voltage is set to 24 V.

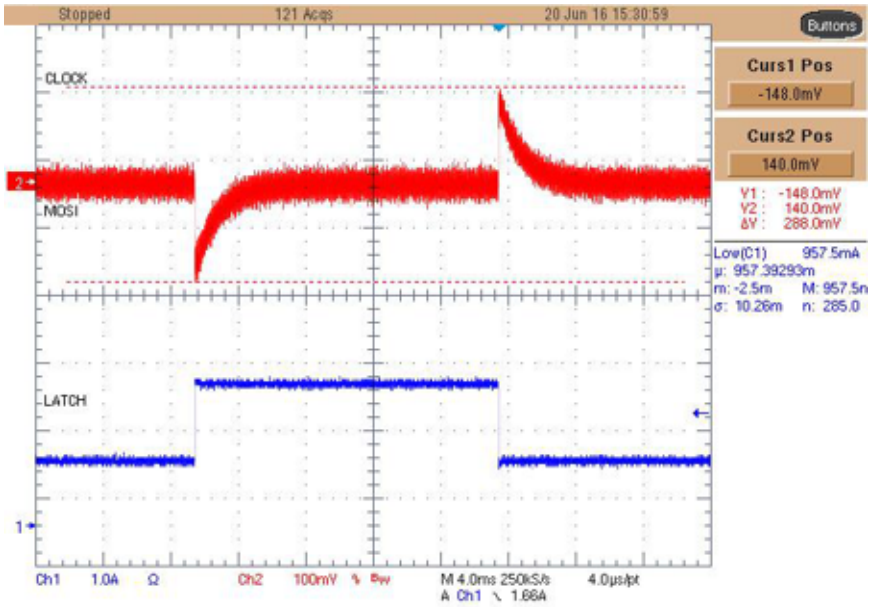


Figure 33. Load Transient Response of Buck-Boost Converter Under V_{IN} = 24 V and I_{OUT} Switching Between 2.2 A and 1 A

Figure 34 shows the load transient response of the buck-boost converter. The load is switching from 1 to 2.2 A with a period of 36 ms. The input voltage is set to 8 V.

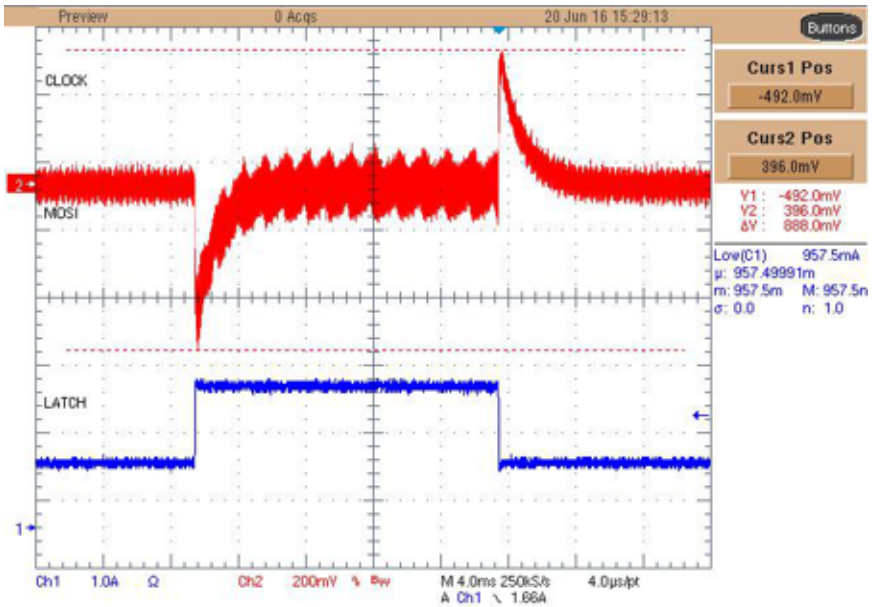


Figure 34. Load Transient Response of Buck-Boost Converter Under V_{IN} = 8 V and I_{OUT} Switching Between 2.2 A and 1 A

Figure 35 shows the load transient response of the buck-boost converter. The load is switching from 0.3 to 0.8 A with a period of 36 ms. The input voltage is set to 3 V.

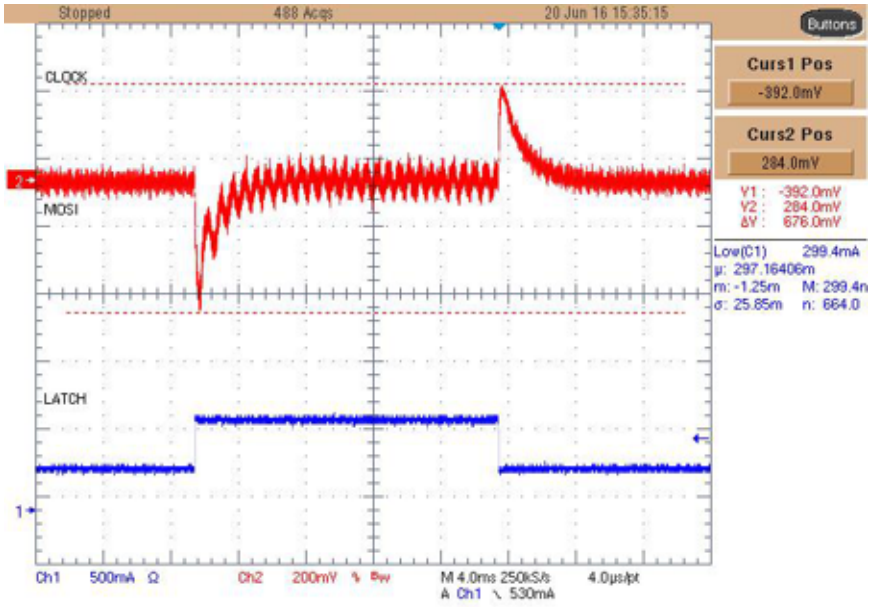


Figure 35. Load Transient Response of Buck-Boost Converter Under V_{IN} = 3.0 V and I_{OUT} Switching Between 0.8 A and 0.3 A

5.5.2 Buck Converter

NOTE: For Figure 36 through Figure 38:
CH2: Output voltage ripple of the buck converter, CH1: Load current of the buck converter

Figure 36 shows the load transient response of the buck converter. The load is switching from 2 to 4.7 A with a period of 5 ms. The input voltage is set to 3 V.

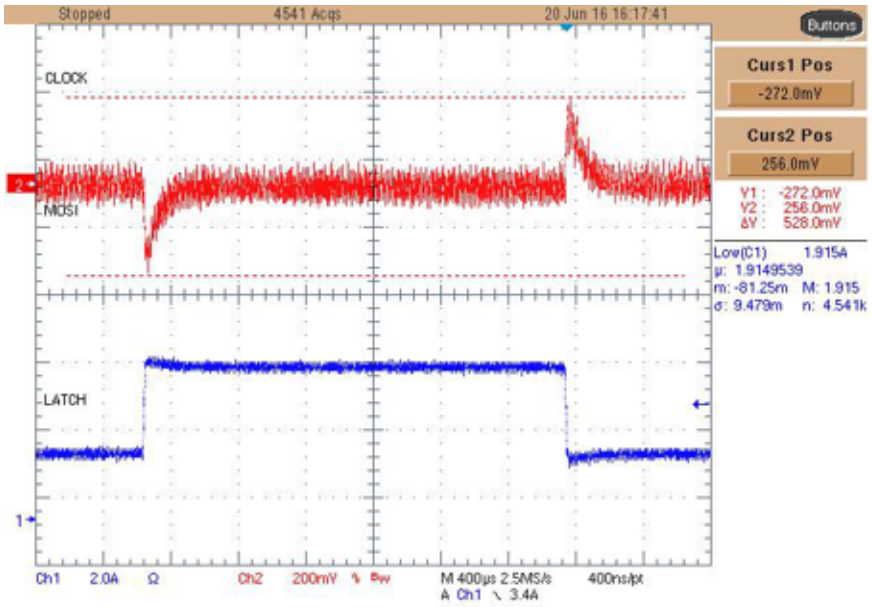


Figure 36. Load Transient Response of Buck Converter Under V_{IN} = 13 V and I_{OUT} Switching Between 4.7 A and 2 A

Figure 37 shows the load transient response of the buck converter. The load is switching from 2 to 4.7 A with a period of 5 ms. The input voltage is set to 8 V.

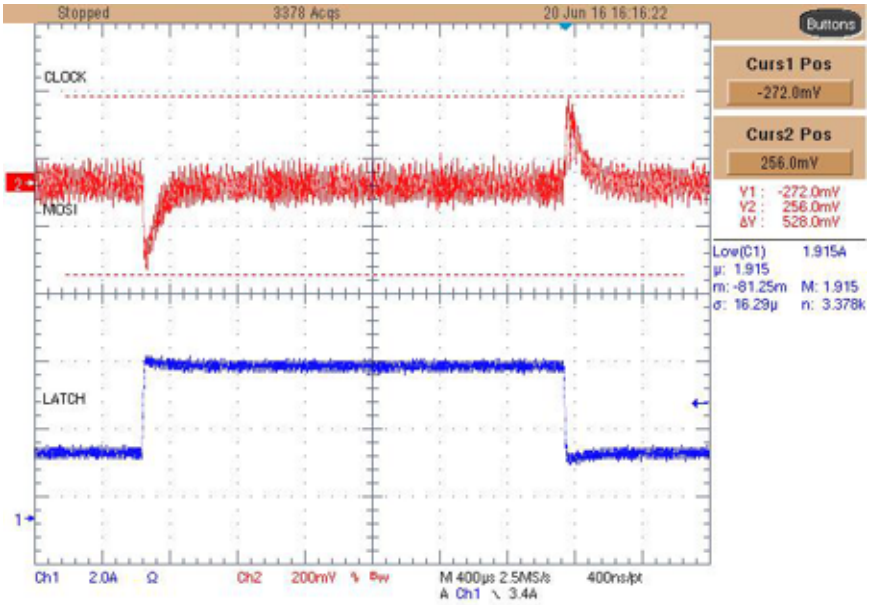


Figure 37. Load Transient Response of Buck Converter Under V_{IN} = 8 V and I_{OUT} Switching Between 4.7 A and 2 A

Figure 38 shows the load transient response of the buck converter. The load is switching from 2 to 4.7 A with a period of 5 ms. The input voltage is set to 24 V.

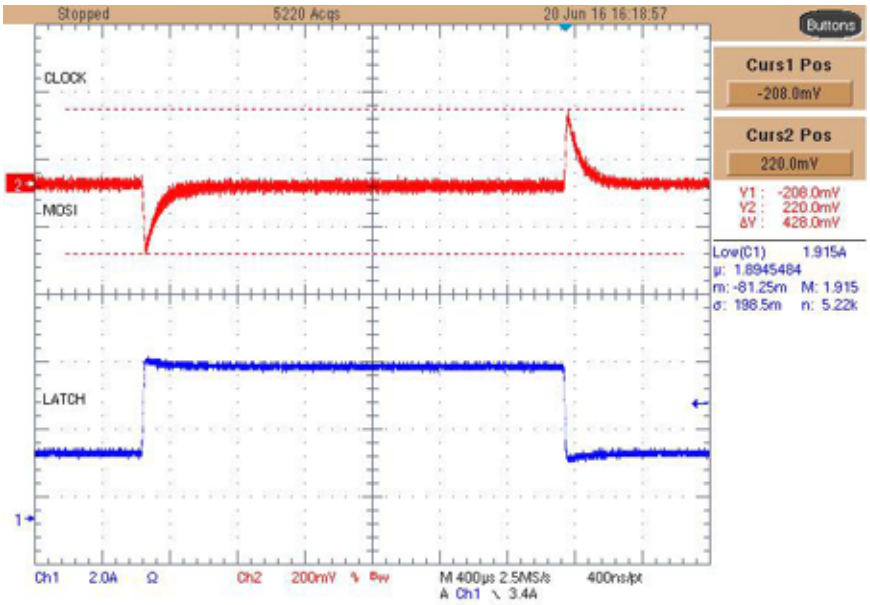


Figure 38. Load Transient Response of Buck Converter Under V_{IN} = 24 V and I_{OUT} Switching Between 4.7 A and 2 A

5.6 Thermal Images

Thermal performance of the design board is measured by taking the thermal images. The circuit is running at the room temperature (25°C) for 30 minutes. The allowed maximum, normal and minimum input voltages are applied. The measurement setup is shown in Figure 39. The test conditions for evaluating the thermal performance are listed in Table 4.

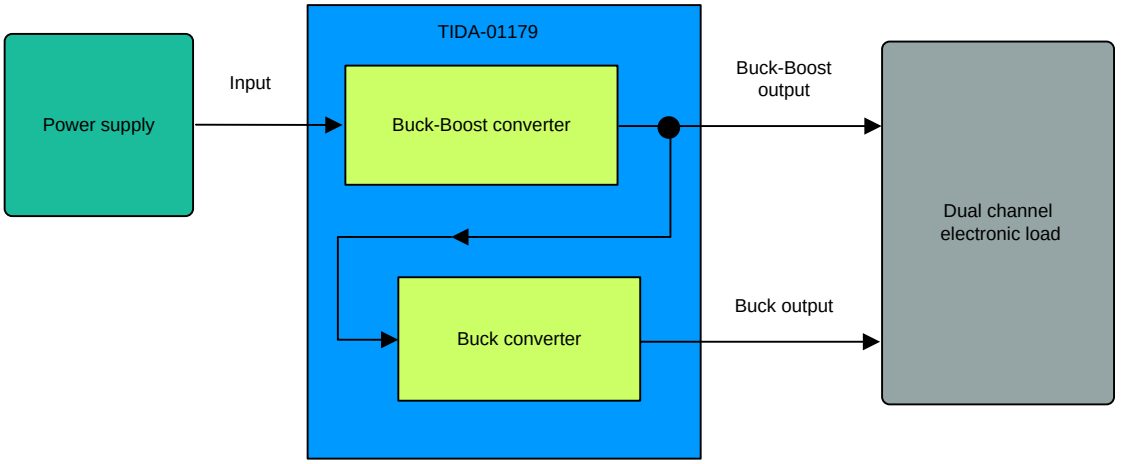


Figure 39. Experiment Setup for Measuring Thermal Performance of TIDA-01179

Table 4. Thermal Test Conditions

INPUT VOLTAGE	BUCK-BOOST V_{OUT}/I_{OUT} TO ELECTRONIC LOAD	BUCK V_{OUT}/I_{OUT} TO ELECTRONIC LOAD	TOTAL OUTPUT POWER	RUNNING TIME	AMBIENT TEMPERATURE
13 V	15 V/0.77 A	5 V/4.0 A	31.55 W	30 minutes	25°C
13 V	15 V/0.5 A	5 V/2.5 A	20 W	30 minutes	25°C
24 V	15 V/0.77 A	5 V/4.0 A	31.55 W	30 minutes	25°C
24 V	15 V/0.5 A	5 V/2.5 A	20 W	30 minutes	25°C
6 V	15 V/0.5 A	5 V/2.7 A	21 W	30 minutes	25°C
6 V	15 V/0.3 A	5 V/1.1 A	10 W	30 minutes	25°C

The thermal images of the board under various conditions are shown from Figure 40 to Figure 51.

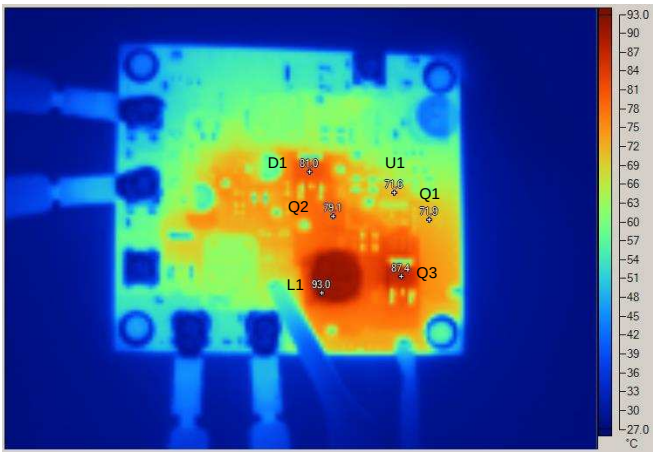


Figure 40. Thermal Image of Board Top Side With V_{IN} = 13 V and P_{OUT} = 31.55 W

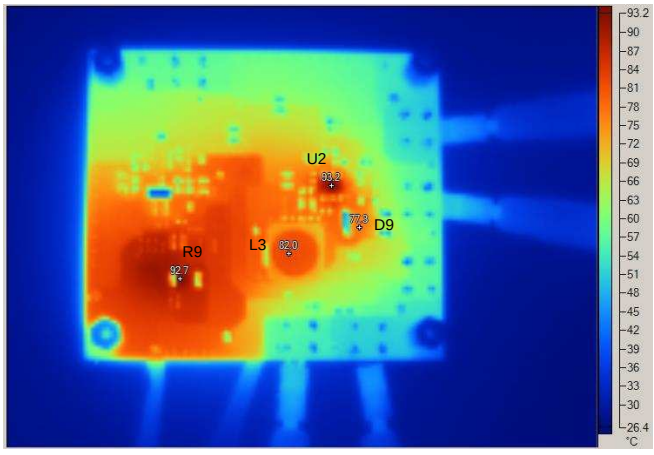


Figure 41. Thermal Image of Board Bottom Side With V_{IN} = 13 V and P_{OUT} = 31.55 W

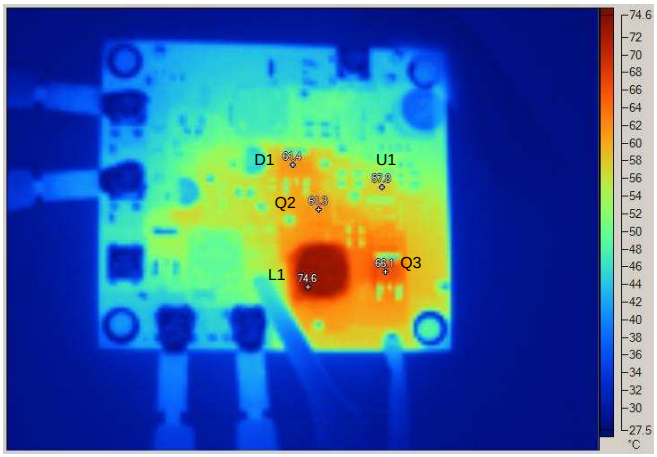


Figure 42. Thermal Image of Board Top Side With V_{IN} = 13 V and P_{OUT} = 20 W

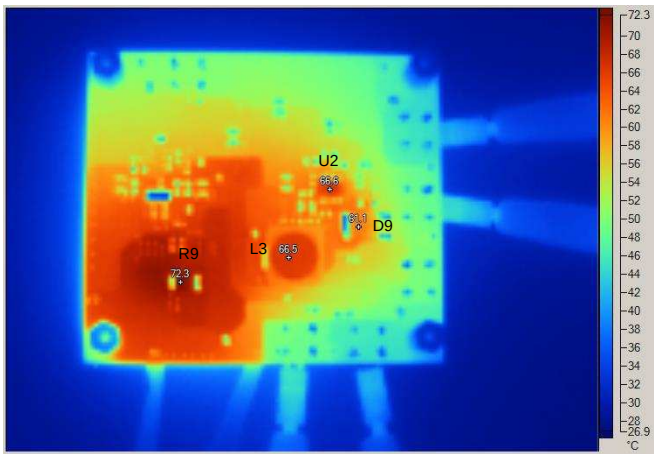


Figure 43. Thermal Image of Board Bottom Side With V_{IN} = 13 V and P_{OUT} = 20 W

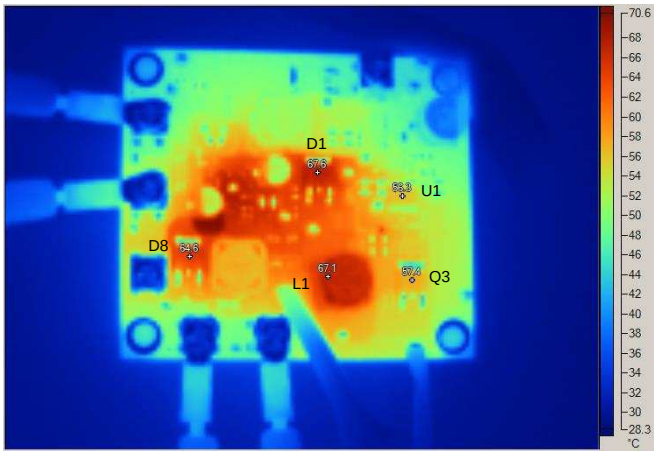


Figure 44. Thermal Image of Board Top Side With V_{IN} = 24 V and P_{OUT} = 31.5 W

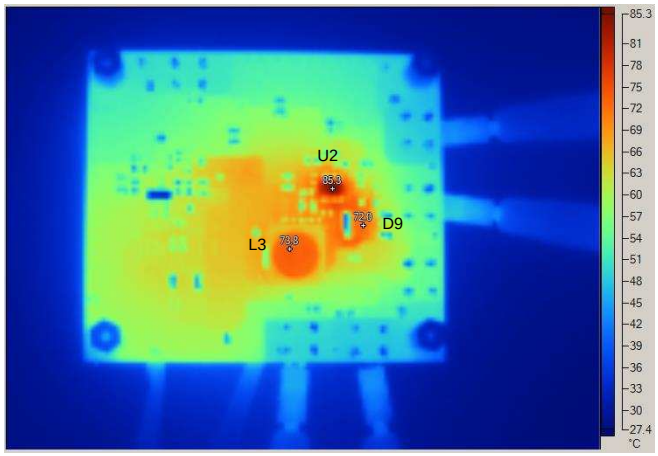


Figure 45. Thermal Image of Board Bottom Side With V_{IN} = 24 V and P_{OUT} = 31.5 W

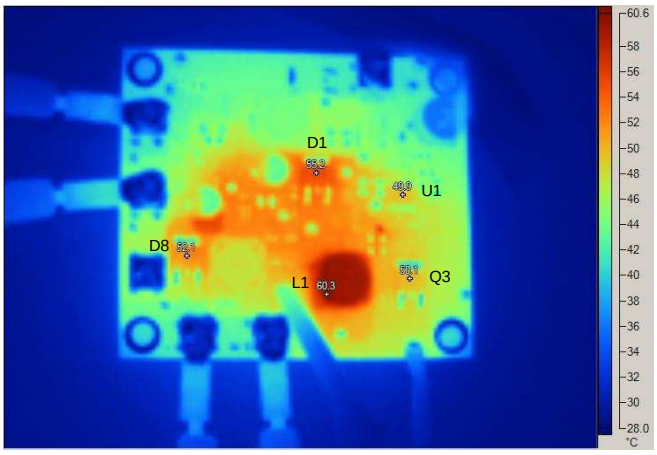


Figure 46. Thermal Image of Board Top Side With V_{IN} = 24 V and P_{OUT} = 20 W

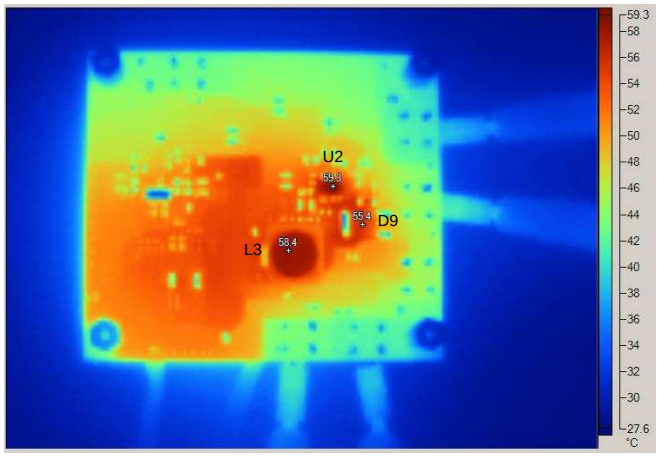


Figure 47. Thermal Image of Board Bottom Side With V_{IN} = 24 V and P_{OUT} = 20 W

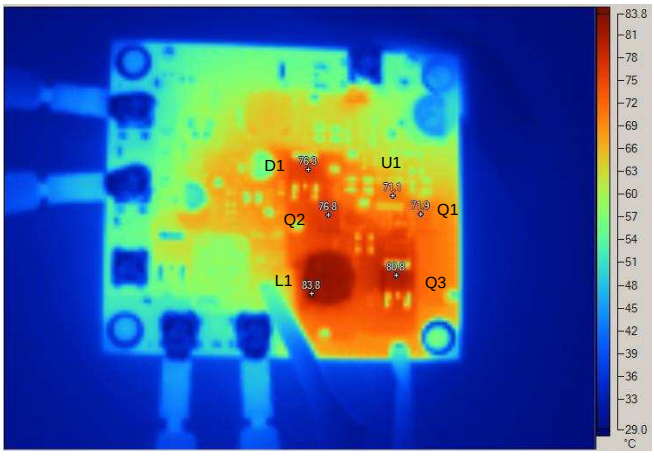


Figure 48. Thermal Image of Board Top Side With V_{IN} = 6 V and P_{OUT} = 21 W

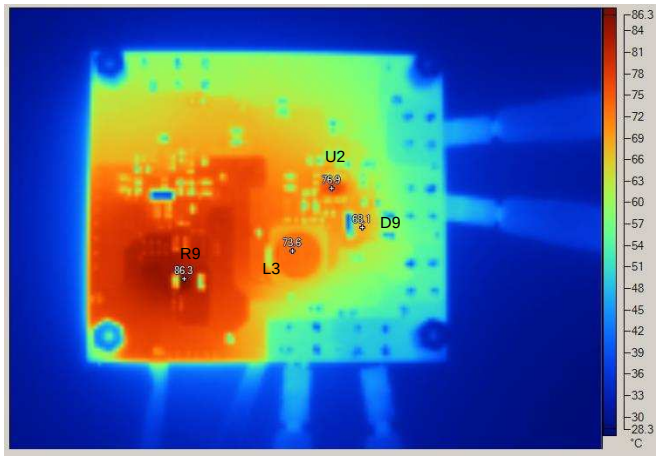


Figure 49. Thermal Image of Board Bottom Side With V_{IN} = 6 V and P_{OUT} = 21 W

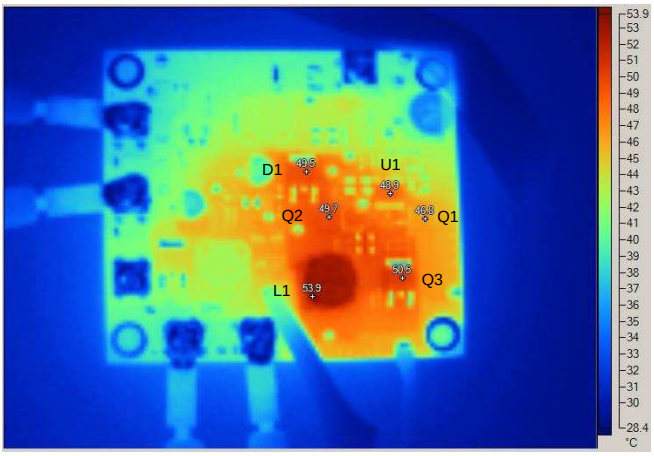


Figure 50. Thermal Image of Board Top Side With V_{IN} = 6 V and P_{OUT} = 10 W

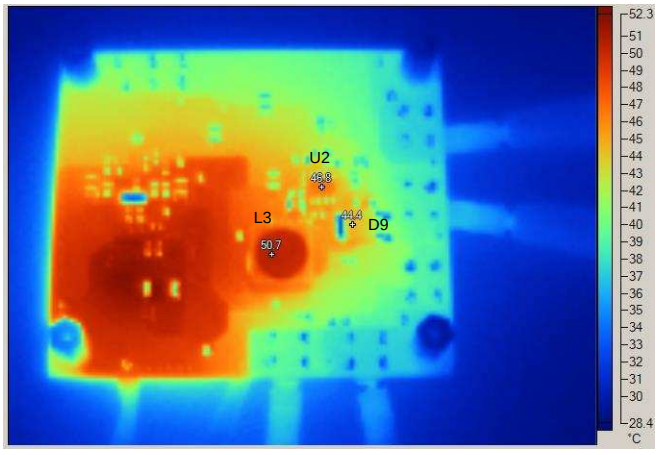


Figure 51. Thermal Image of Board Bottom Side With V_{IN} = 6 V and P_{OUT} = 10 W

5.7 Control Loop Frequency Response

The control loop responses are measured for the buck-boost and buck converters under various loads and input voltages, respectively. The measurement setup for the buck-boost converter is shown in Figure 52. Output of the network analyzer is connected to the test points TP8 and TP9, which is cross the injection resistor R15. TP8 and TP9 are also connected to the input channel A and channel B, respectively.

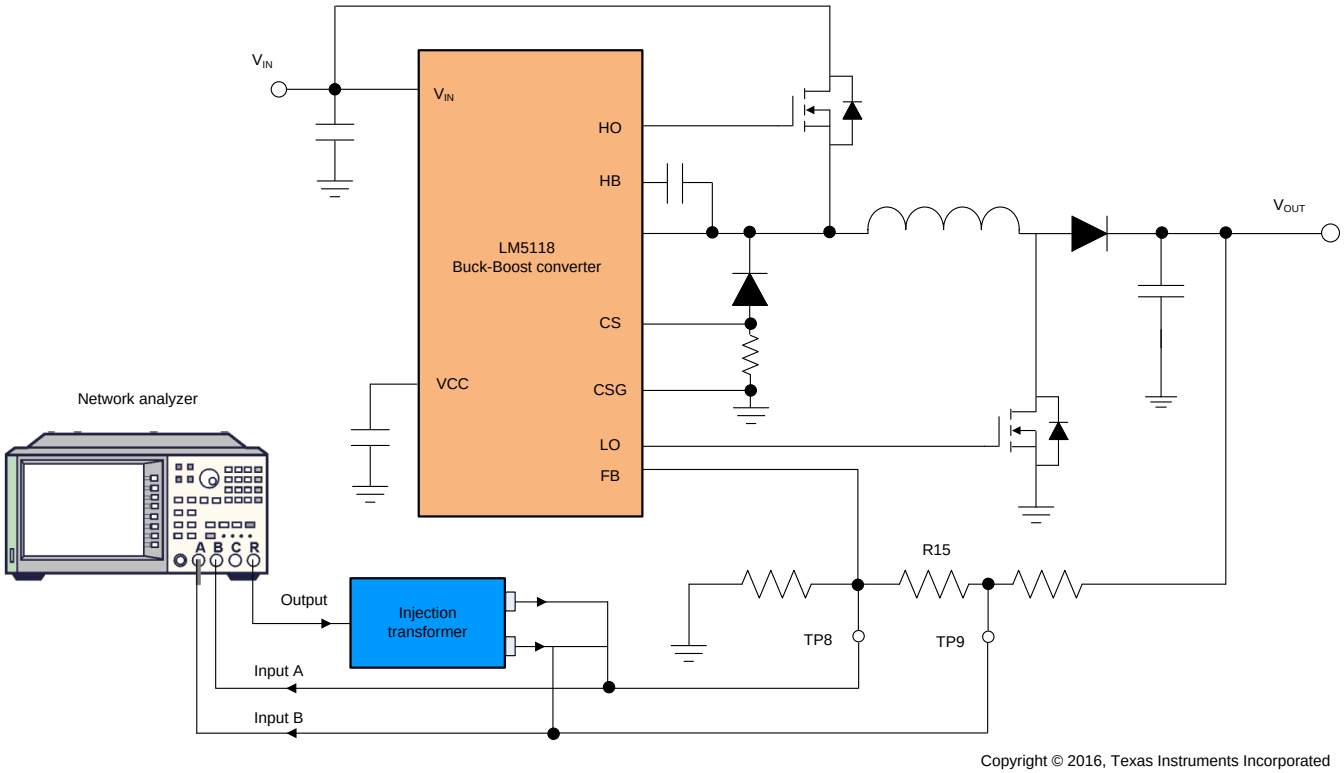


Figure 52. Control Loop Frequency Response Measurement Setup

5.7.1 Buck-Boost Converter

The loop frequency response of the buck-boost converter is tested under various conditions as shown in Table 5. The measured results are shown from Figure 53 through Figure 60.

Table 5. Test Conditions of Frequency Response of Buck-Boost Converter

INPUT VOLTAGE	OUTPUT CURRENT I_{OUT}	OUTPUT POWER
13 V	0.5 A	7.4 W
	2.2 A	32.56 W
24 V	0.5 A	7.4 W
	2.2 A	32.56 W
6 V	0.5 A	7.4 W
	0.9 A	13.32 W
3 V	0.2 A	2.96 W
	0.5 A	7.4 W

Loop frequency responses of the buck-boost converter with a 13-V input voltage are shown in Figure 53 and Figure 54.

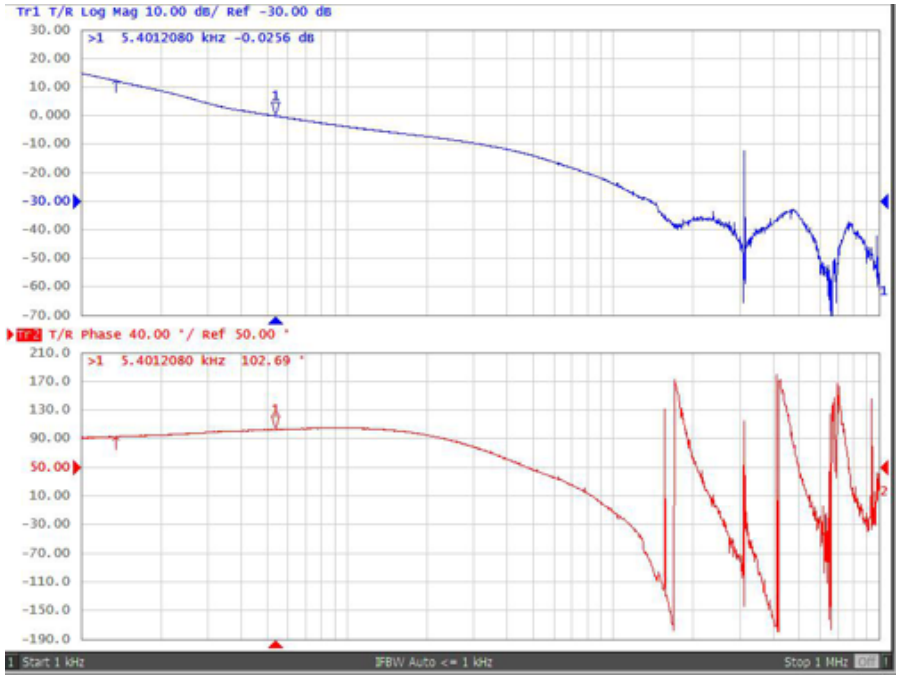


Figure 53. Loop Frequency Response of Buck-Boost Converter With V_{IN} = 13 V and I_{OUT} = 0.5 A

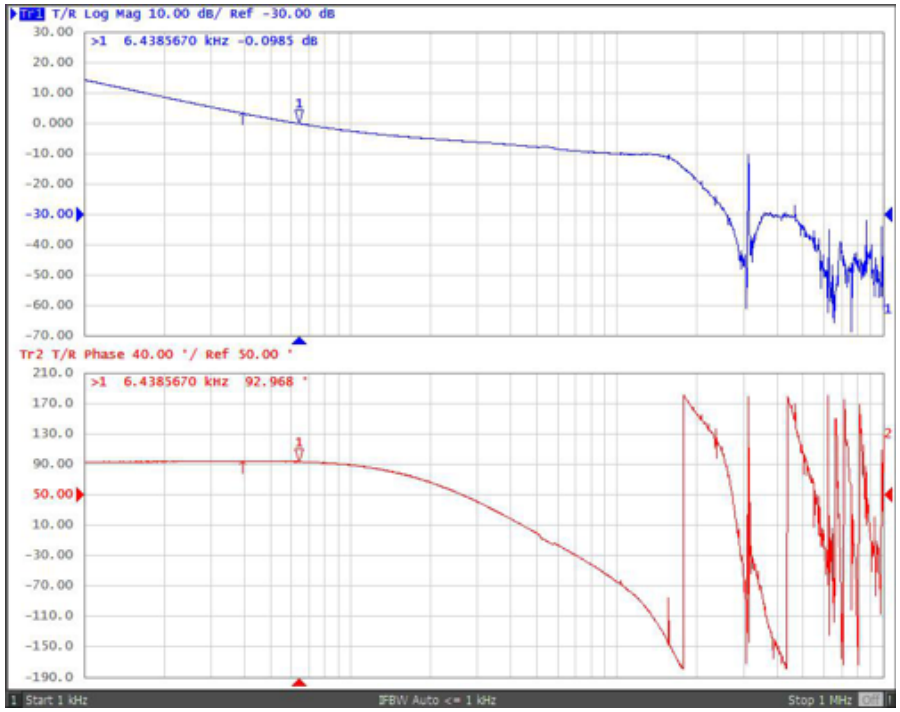


Figure 54. Loop Frequency Response of Buck-Boost Converter With V_{IN} = 13 V and I_{OUT} = 2.2 A

NOTE: Trace1: Buck-boost converter loop response gain, Trace2: Buck-boost converter loop response phase

Loop frequency responses of the buck-boost converter with a 24-V input voltage are shown in Figure 55 and Figure 56.

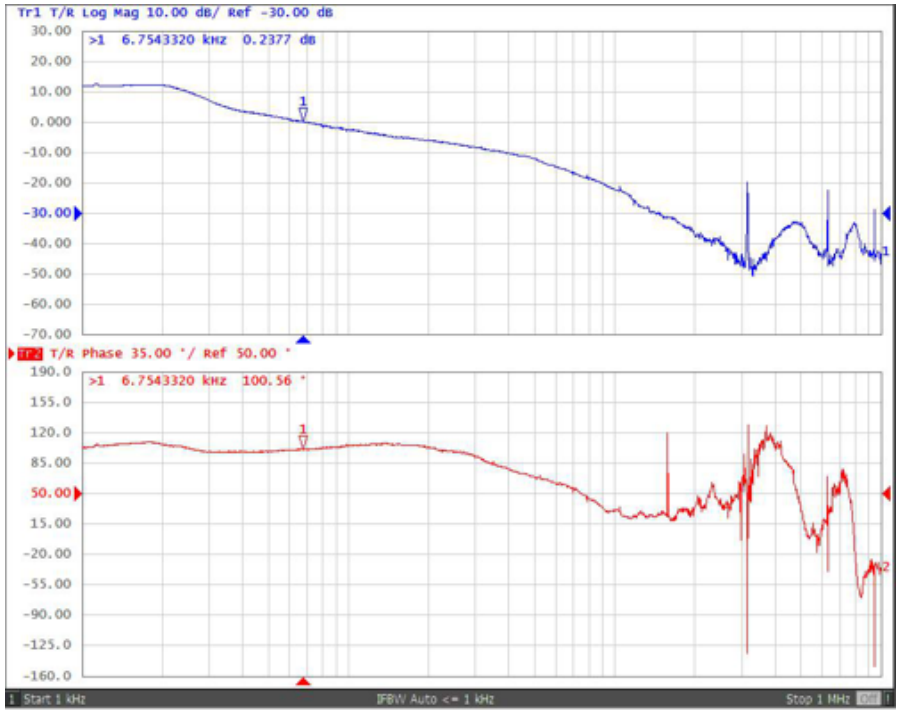


Figure 55. Loop Frequency Response of Buck-Boost Converter With V_{IN} = 24 V and I_{OUT} = 0.5 A

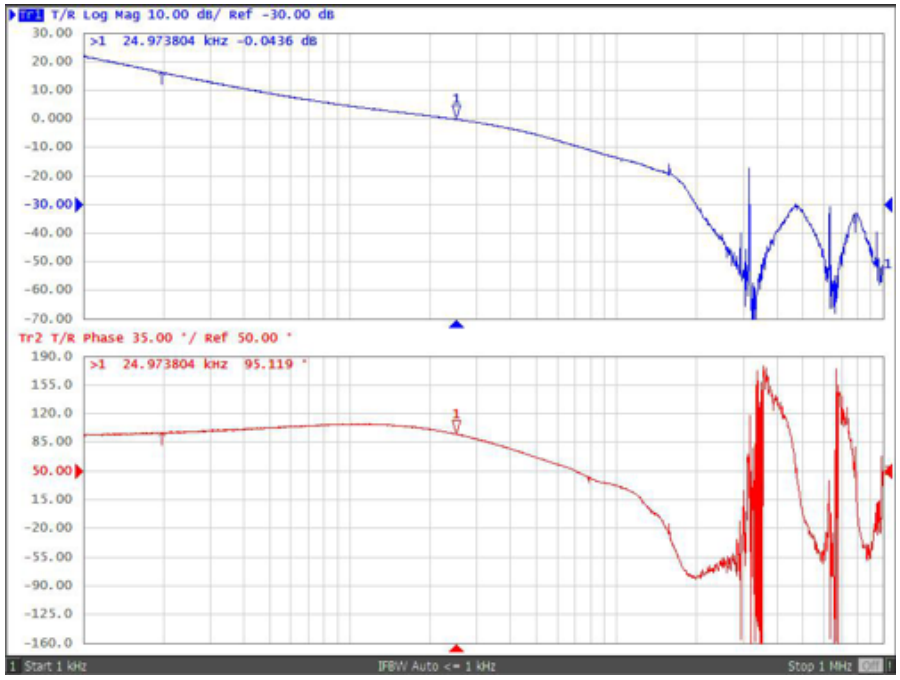


Figure 56. Loop Frequency Response of Buck-Boost Converter With V_{IN} = 24 V and I_{OUT} = 2.2 A

NOTE: Trace1: Buck-boost converter loop response gain, Trace2: Buck-boost converter loop response phase

Loop frequency responses of the buck-boost converter with a 6-V input voltage are shown in Figure 57 and Figure 58.

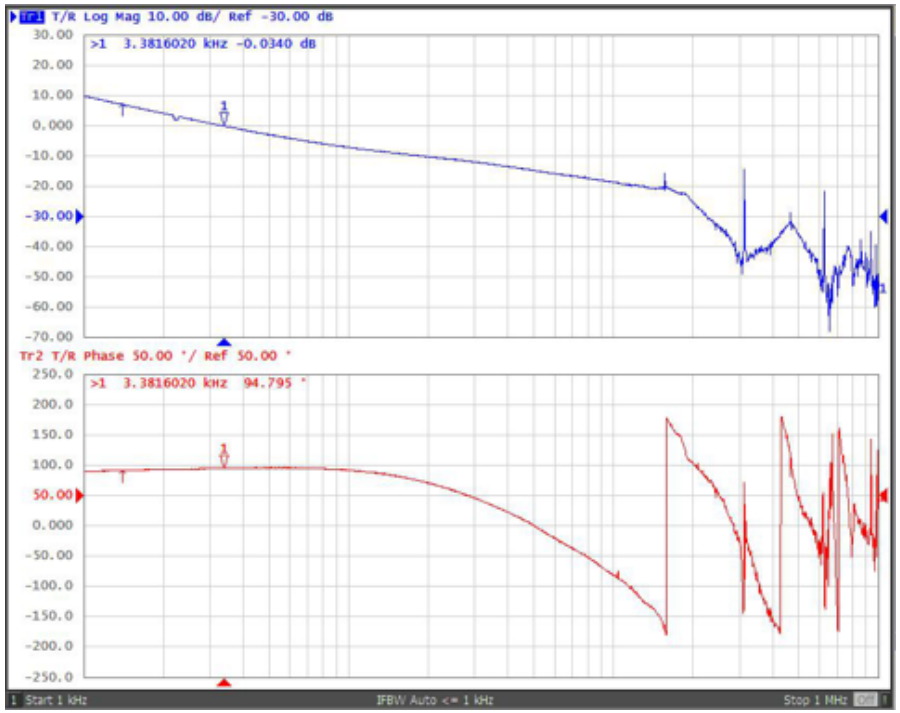


Figure 57. Loop Frequency Response of Buck-Boost Converter With V_{IN} = 6 V and I_{OUT} = 0.5 A

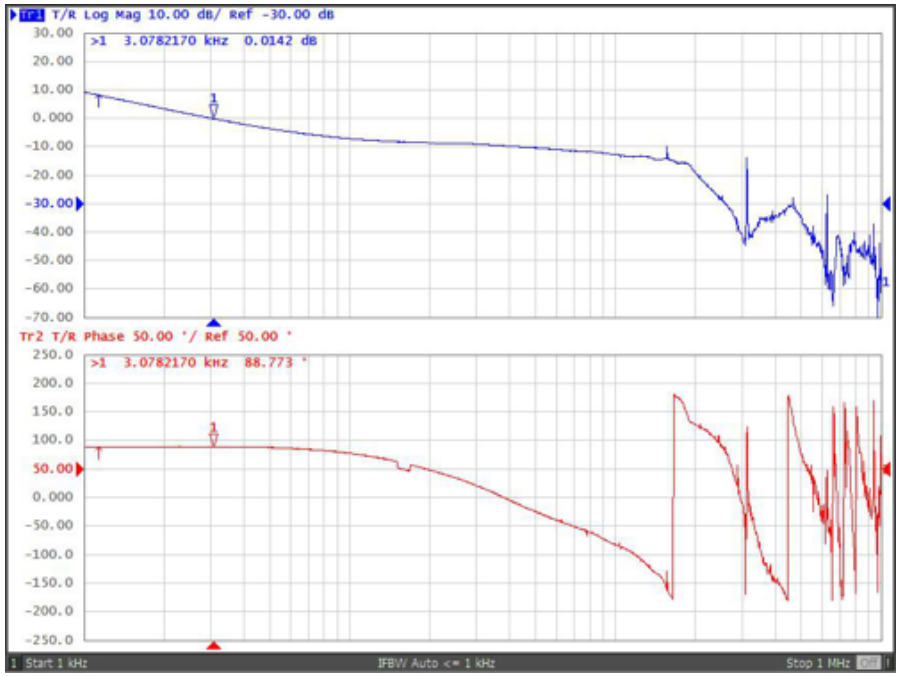


Figure 58. Loop Frequency Response of Buck-Boost Converter With V_{IN} = 6 V and I_{OUT} = 0.9 A

NOTE: Trace1: Buck-boost converter loop response gain, Trace2: Buck-boost converter loop response phase

Loop frequency responses of the buck-boost converter with a 3-V input voltage are shown in Figure 59 and Figure 60.

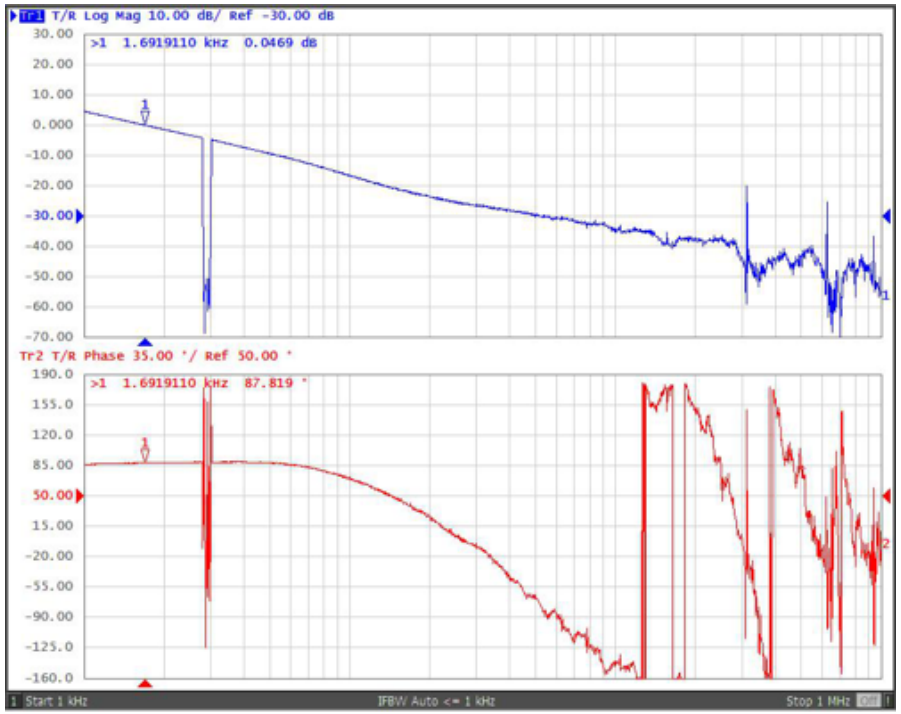


Figure 59. Loop Frequency Response of Buck-Boost Converter With V_{IN} = 3.0 V and I_{OUT} = 0.2 A

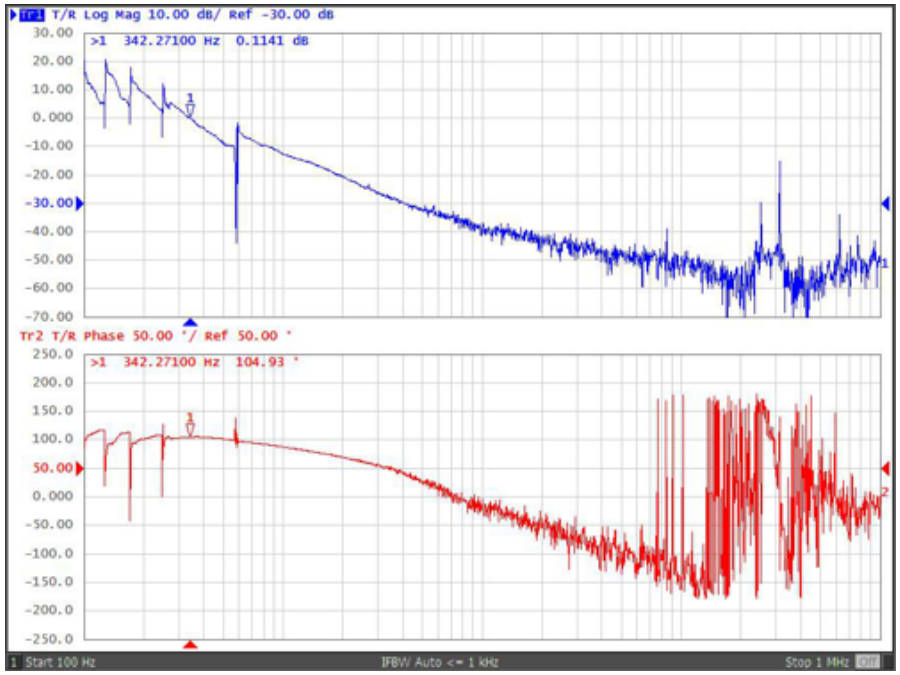


Figure 60. Loop Frequency Response of Buck-Boost Converter With V_{IN} = 3.0 V and I_{OUT} = 0.5 A

NOTE: Trace1: Buck-boost converter loop response gain, Trace2: Buck-boost converter loop response phase

5.7.2 Buck Converter

The loop frequency response of the buck converter is tested under various conditions as shown in Table 6. The measured results are shown from Figure 61 to Figure 64.

Table 6. Test Conditions of Frequency Response of Buck Converter

INPUT VOLTAGE	OUTPUT CURRENT I_{OUT}	OUTPUT POWER
15 V	1 A	5 W
	4 A	20 W
9 V	1 A	5 W
	4 A	20 W

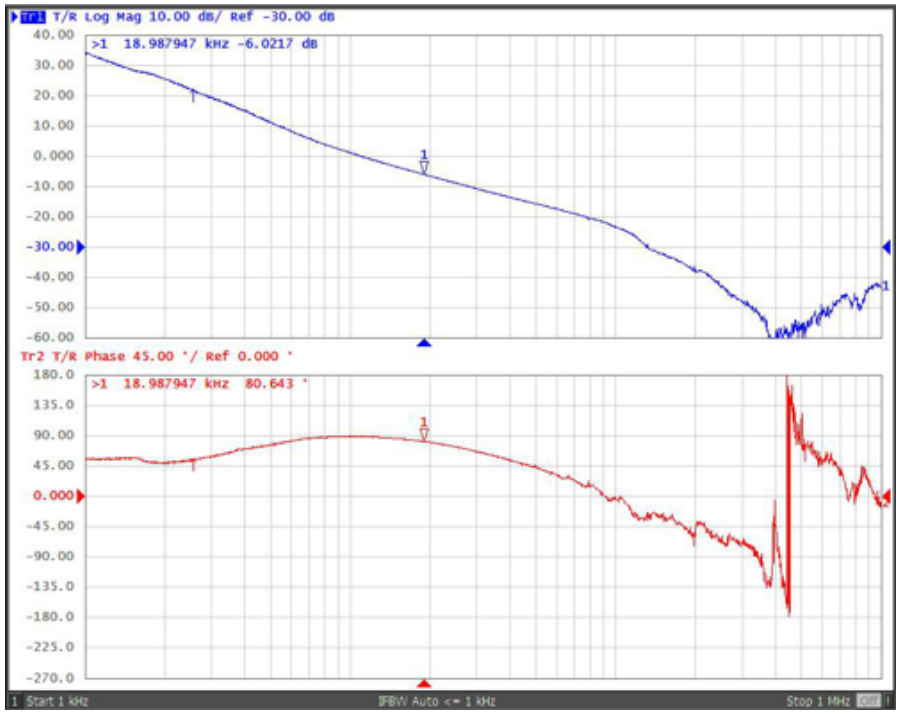


Figure 61. Loop Frequency Response of Buck Converter With V_{IN} = 15 V and I_{OUT} = 1 A

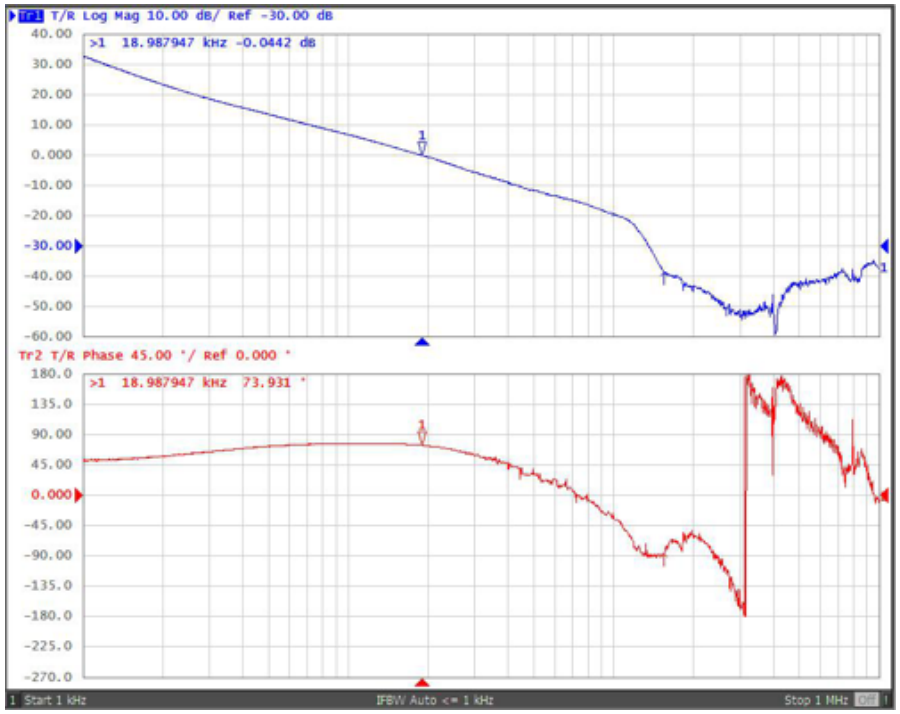


Figure 62. Loop Frequency Response of Buck Converter With V_{IN} = 15 V and I_{OUT} = 4 A

NOTE: Trace1: Buck converter loop response gain, Trace2: Buck converter loop response phase

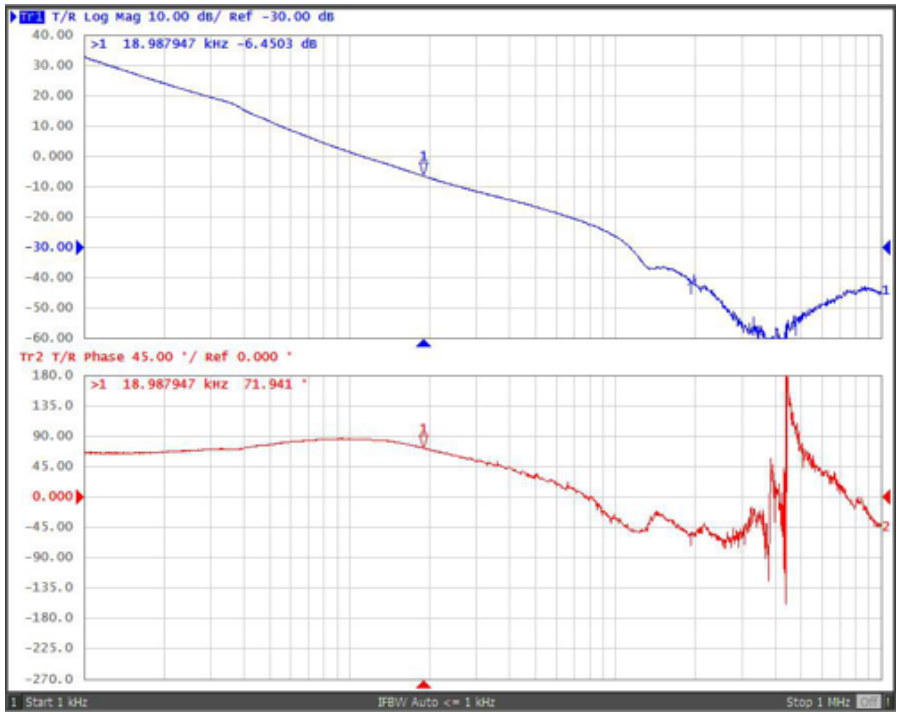


Figure 63. Loop Frequency Response of Buck Converter With V_{IN} = 9 V and I_{OUT} = 1 A

Figure 64. Loop Frequency Response of Buck Converter With V_{IN} = 9 V and I_{OUT} = 4 A

NOTE: Trace1: Buck converter loop response gain, Trace2: Buck converter loop response phase

5.8 Electrical Transient Testing

Three electrical transient test pulses, ISO 7637-2:2004 Pulse 1, 2a, 3a, and 3b are performed. For all the tests, the battery DC voltage of 13.5 V is applied to the input, and a 3.5-A load current is applied to the buck converter.

The measurement setup for electrical transients testing, the equipment model, and functions are shown in Figure 65.

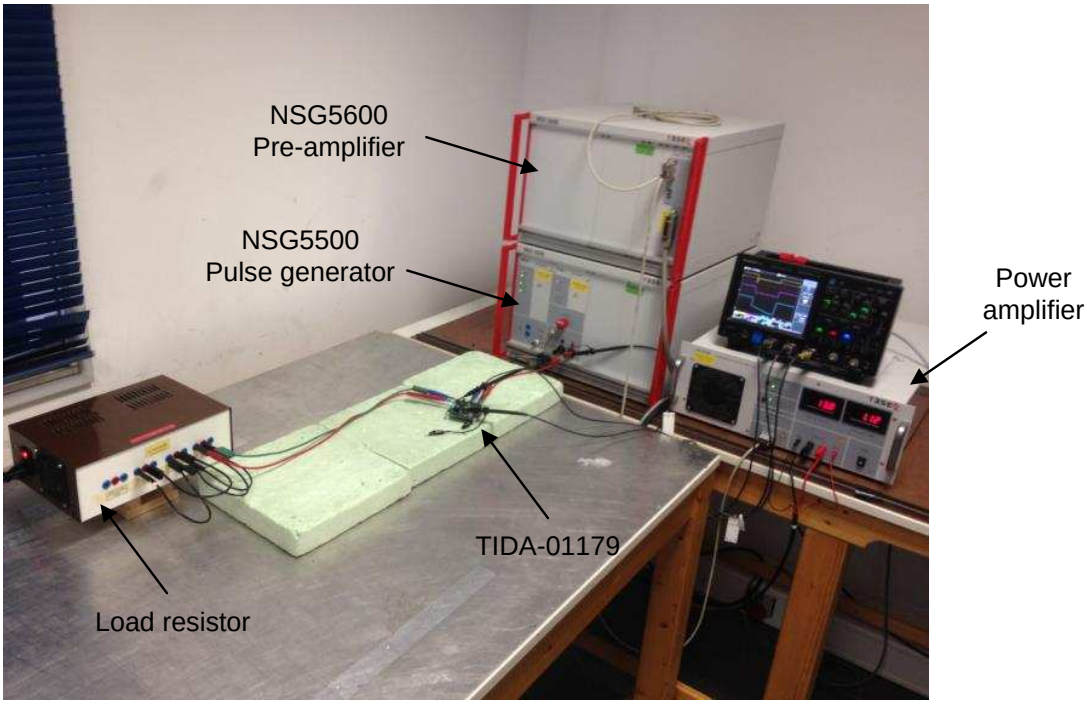


Figure 65. Measurement Setup for Electrical Transients Test

5.9 Electrical Transient Testing Parameters From OEMs

As stated previously, OEMs (and other standards organizations) maintain their own versions of these pulses in their own standards. Table 7 shows an example comparison of the ISO 7637-2 defined pulses with various OEM's definitions.

Table 7. Comparison of ISO 7637-2 Defined Pulses From Various OEMs

PARAMETER	V_{MAX} (V)	R_{SOURCE} (Ω)	T_r	$T_{DURATION}$
ISO 7637-2: PULSE 1				
OEM#1	–100	10	1 µs	2 ms
OEM#2	–100	10	1 µs	2 ms
OEM#3	–100	10	1 µs	2 ms
OEM#4	–100	4	1 µs	2 ms
ISO 7637-2: PULSE 2A				
OEM#1	75	4	1 µs	50 µs
OEM#2	100	10	1 µs	50 µs
OEM#3	50	2	1 µs	50 µs
OEM#4	75	4	1 µs	50 µs
ISO 7637-2: PULSE 3A				
OEM#1	–150	50	5 ns	0.1 µs
OEM#2	–150	50	5 ns	0.1 to 0.2 µs
OEM#3	–150	50	5 ns	0.1 µs
OEM#4	–150	50	5 ns	0.1 µs
ISO 7637-2: PULSE 3B				
OEM#1	100	50	5 ns	0.1 µs
OEM#2	100	50	5 ns	0.1 to 0.2 µs
OEM#3	100	50	5 ns	0.1 µs
OEM#4	100	50	5 ns	0.1 µs

5.9.1 ISO 7637-2 Pulse 1

ISO7637-2 Pulse 1 is defined as "a simulation of transients due to supply disconnection from inductive loads. It is applicable to DUTs which, as used in the vehicle, remain connected directly in parallel with an inductive load."

The waveform of the applied pulse for the Pulse 1 test is shown in Figure 66. A minimum voltage of –150 V is reached. Find detailed parameters for the test in Table 7.

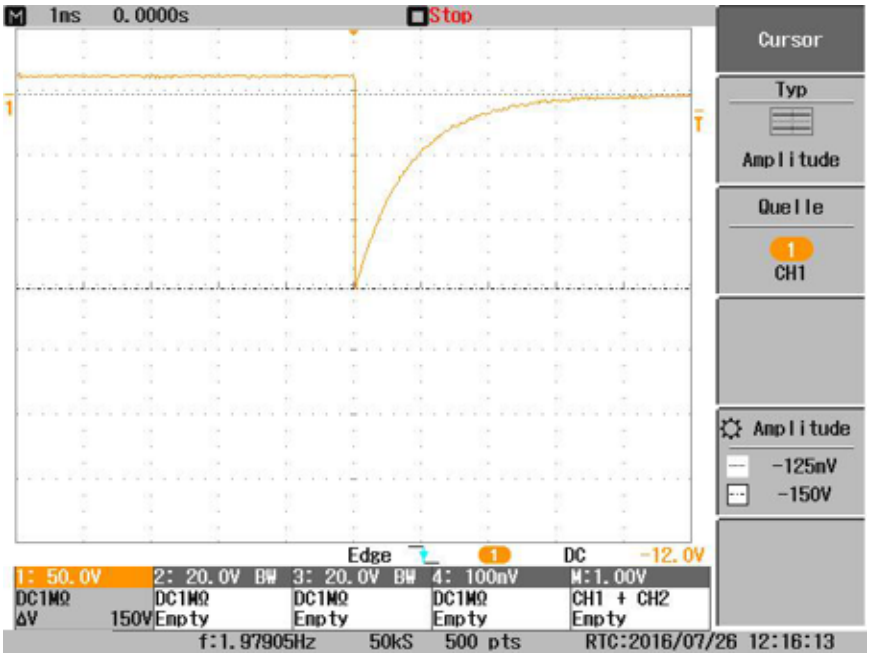


Figure 66. Pulse 1 Test Pulse

Figure 67 shows the performance of the system during the test. Figure 68 shows the pulse falling slope in expanded scale. The circuit functions recover as designed after the test. The TVS diode clamped the voltage at –19.7 V.

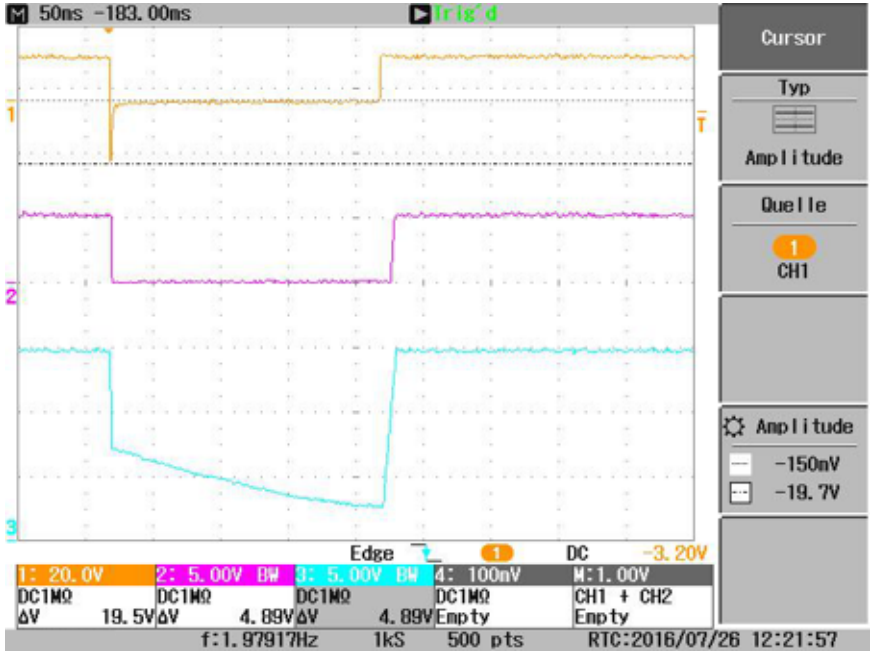


Figure 67. Outputs of Power Rails During Pulse 1 Test

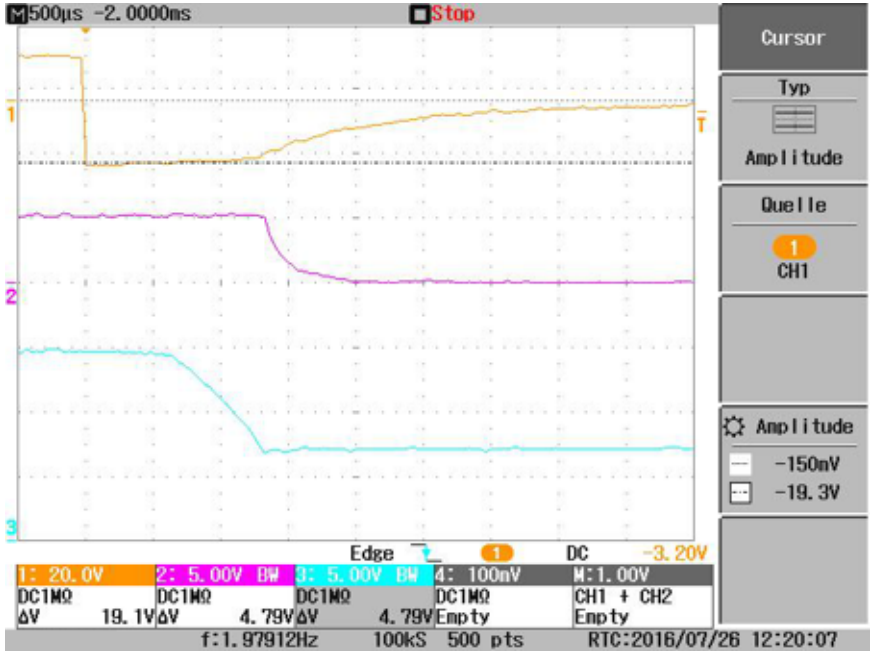


Figure 68. Falling Slopes During Pulse 1 Test

NOTE: CH1: Test pulse applied to the system input. CH2: Output voltage of the buck converter, CH3: Output voltage of the buck-boost converter

5.9.2 ISO 7637-2 Pulse 2a

ISO7637-2 Pulse 2a is defined as "simulates transients due to sudden interruption of currents in a device connected in parallel with DUT due to inductance of the wiring harness."

The waveform of the applied pulse for Pulse 2a test is shown in Figure 69. A peak voltage of 130 V is reached. Find detailed parameters for the test in Table 7.

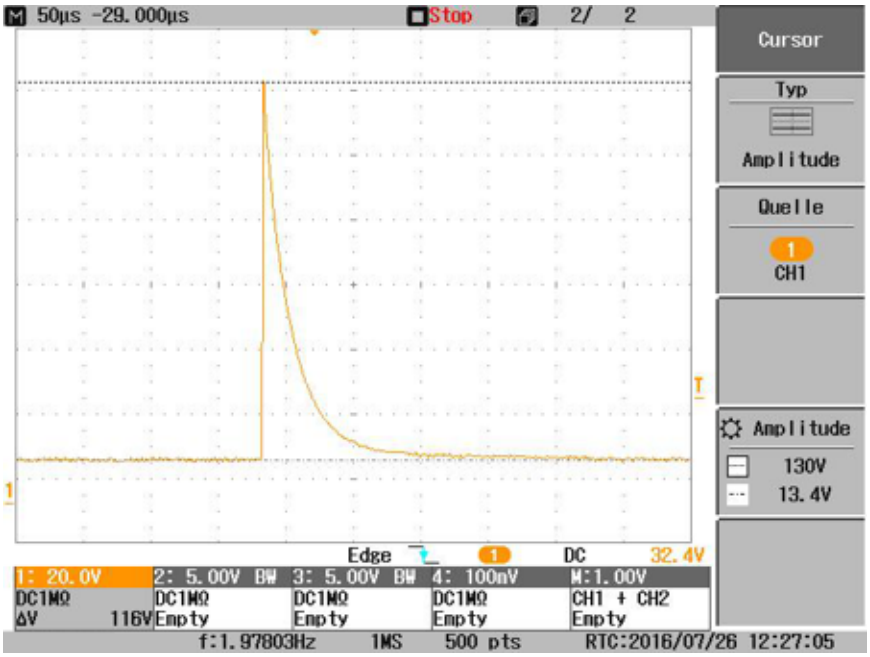


Figure 69. Pulse 2 Test Pulse

Figure 70 shows the performance of the system during the test. An overshoot of 23.4 V with a duration of 2 µs is observed at the output of the buck-boost converter. An overshoot of 14.3 V with a duration of 2 µs is observed at the output of the buck converter.

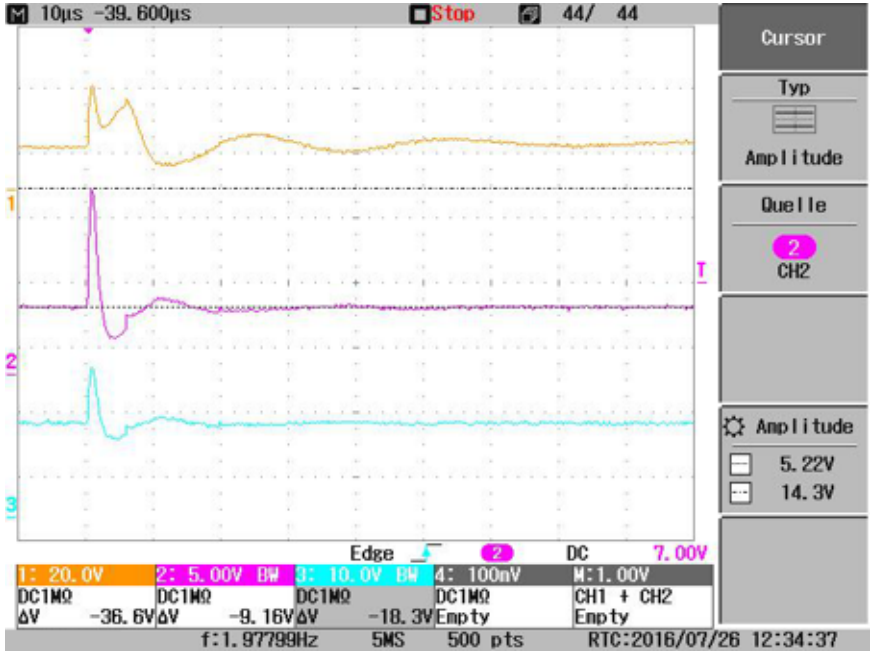


Figure 70. Outputs of Power Rails During Pulse 2a Test

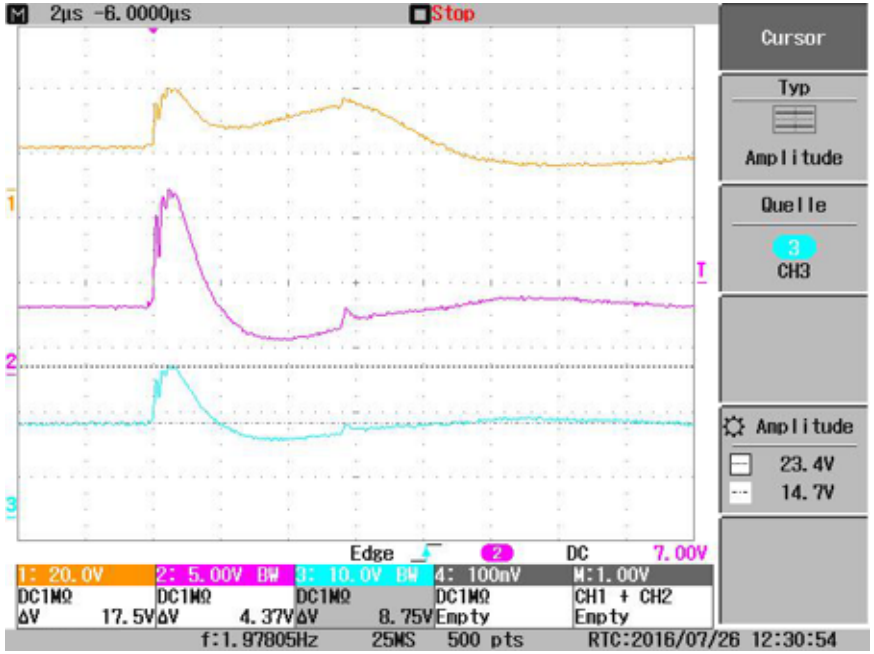


Figure 71. Output Overshoot During Pulse 2a Test

NOTE: CH1: Test pulse applied to the system input, CH2: Output voltage of the buck converter, CH3: Output voltage of the buck-boost converter

5.9.3 ISO 7637-2 Pulse 3a

ISO7637-2 Pulse 3a and 3b are defined as: "These test pulses are a simulation of transients which occur as a result of the switching processes. The characteristics of these transients are influenced by distributed capacitance and inductance of the wiring harness."

The waveform of the applied pulse for Pulse 3a test is shown in Figure 72. A minimum voltage of –235 V is reached. Find detailed parameters for the test in Table 9.

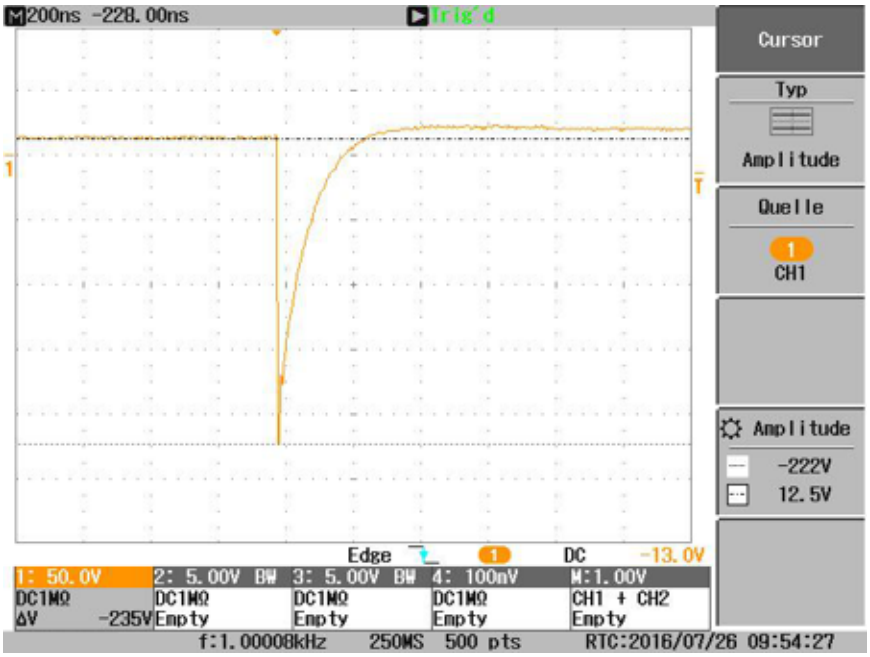


Figure 72. Pulse 3a Test Pulse

Figure 73 shows the performance of the system during the test. A undershoot of –43.4 V with a duration of 25 ns is observed at the output of the buck-boost converter. An overshoot of –34.2 V with a duration of 25 ns is observed at the output of the buck converter.

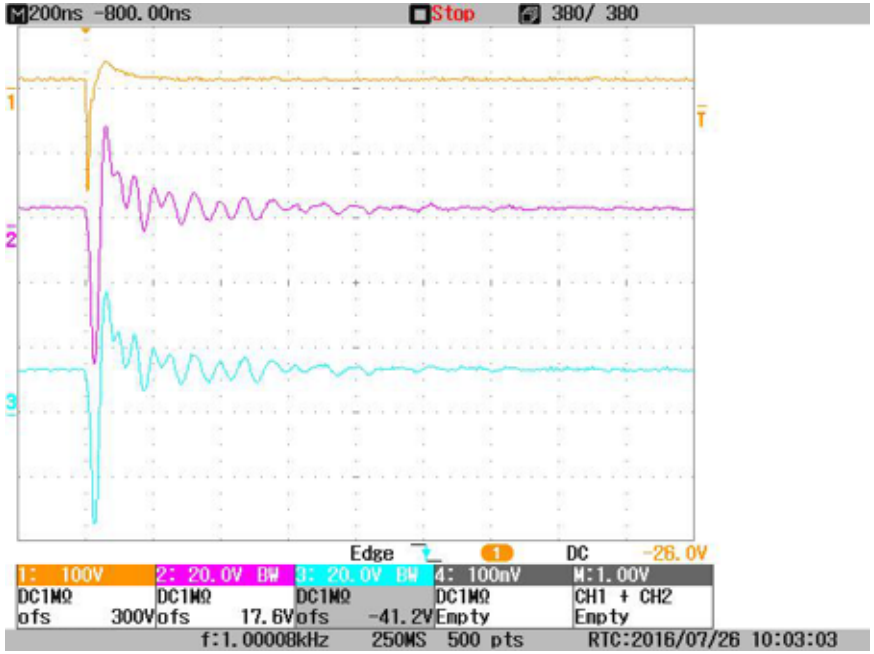


Figure 73. Outputs of Power Rails During Pulse 3a Test

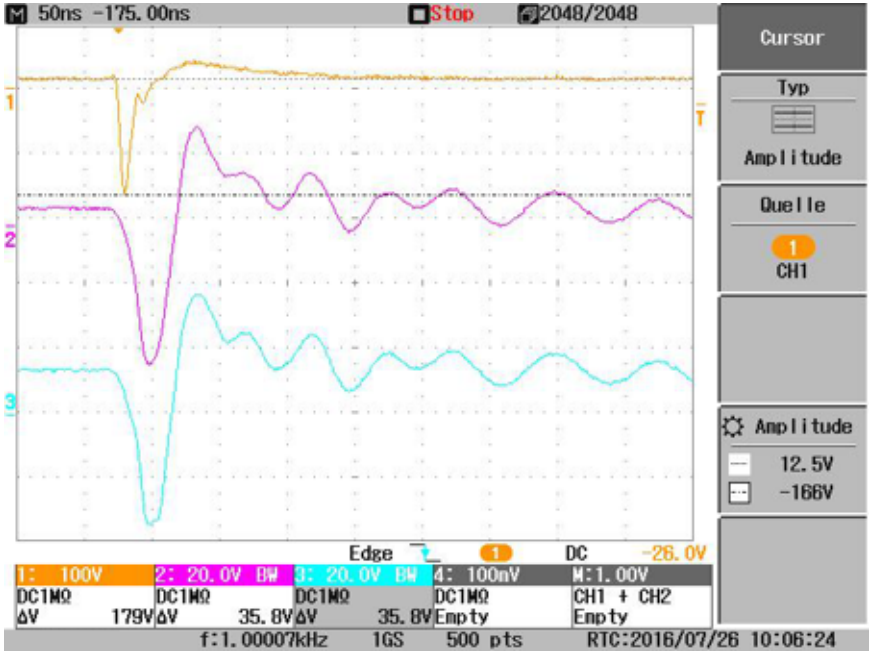


Figure 74. Output Voltage Undershoots During Pulse 3a Test

NOTE: CH1: Test pulse applied to the system input, CH2: Output voltage of the buck converter, CH3: Output voltage of the buck-boost converter

5.9.4 ISO 7637-2 Pulse 3b

The waveform of the applied pulse for Pulse 3b test is shown in Figure 75.

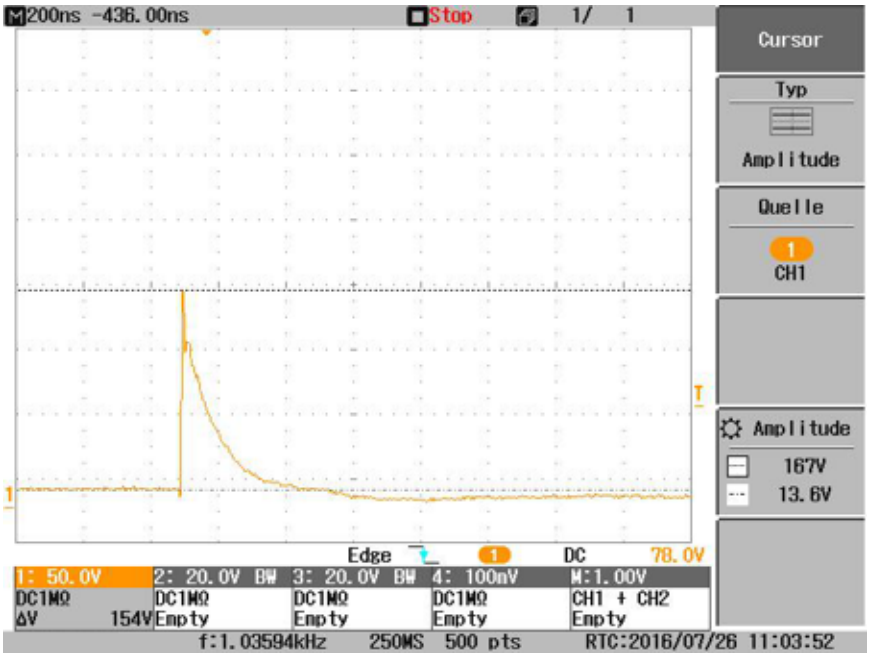


Figure 75. Pulse 3b Test Pulse

Figure 76 and Figure 77 show the performance of the system during the test. An overshoot of 43.4 V with a duration of 25 ns is observed at the output of the buck-boost converter. An overshoot of 54.1 V with a duration of 25 ns is observed at the output of the buck converter. The oscillations settle time is 594 ns.

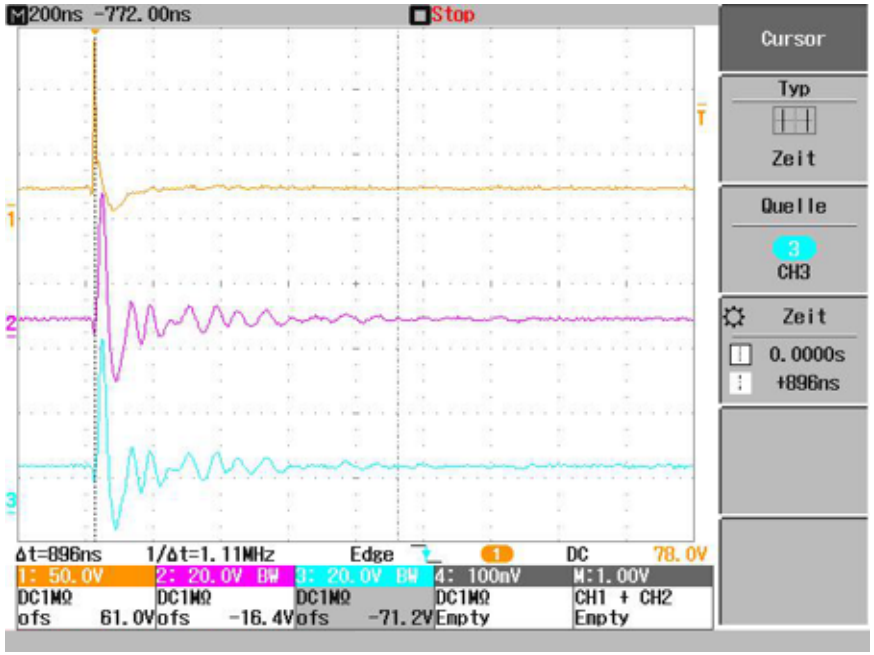


Figure 76. Outputs of Power Rails During Pulse 3b Test

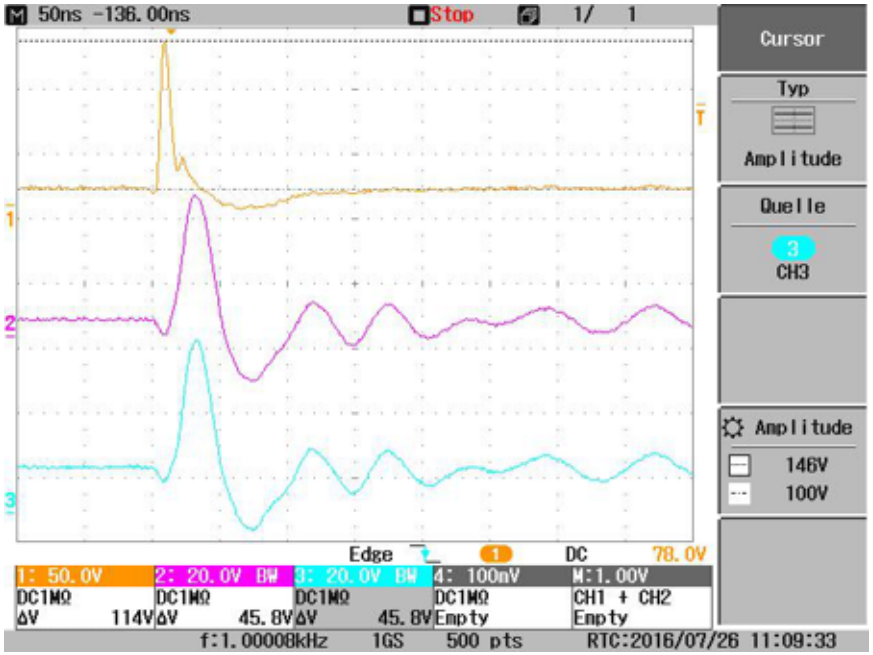


Figure 77. Output Voltage Overshoots During Pulse 3b Test

NOTE: CH1: Test pulse applied to the system input, CH2: Output voltage of the buck converter, CH3: Output voltage of the buck-boost converter

5.10 ISO 16750-2: Jump Start

ISO 16750-2 jump start simulates the condition where two 12-V batteries are connected to the supply lines in series. This is an overvoltage condition, which is sustained for a period of time. The jump start waveform applied to the system input is shown in Figure 78. A step-up voltage from 1.8 to 24.8 V is applied.

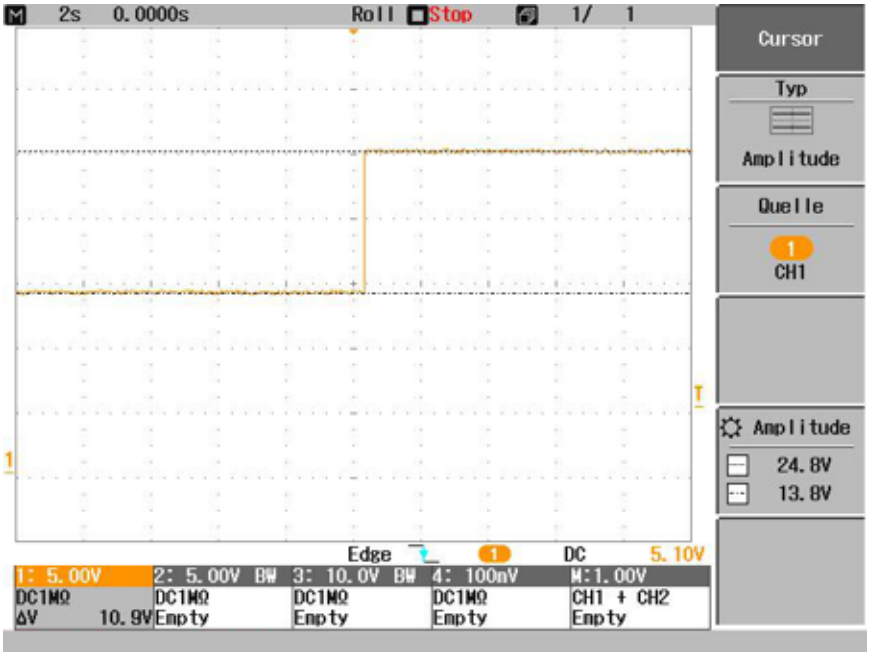


Figure 78. Applied Jump Start Waveform

Figure 79 shows output power rails of the system during the jump start test, which lasted for 60 seconds. Both the buck-boost converter and the buck converter remain stable and function normally as designed.

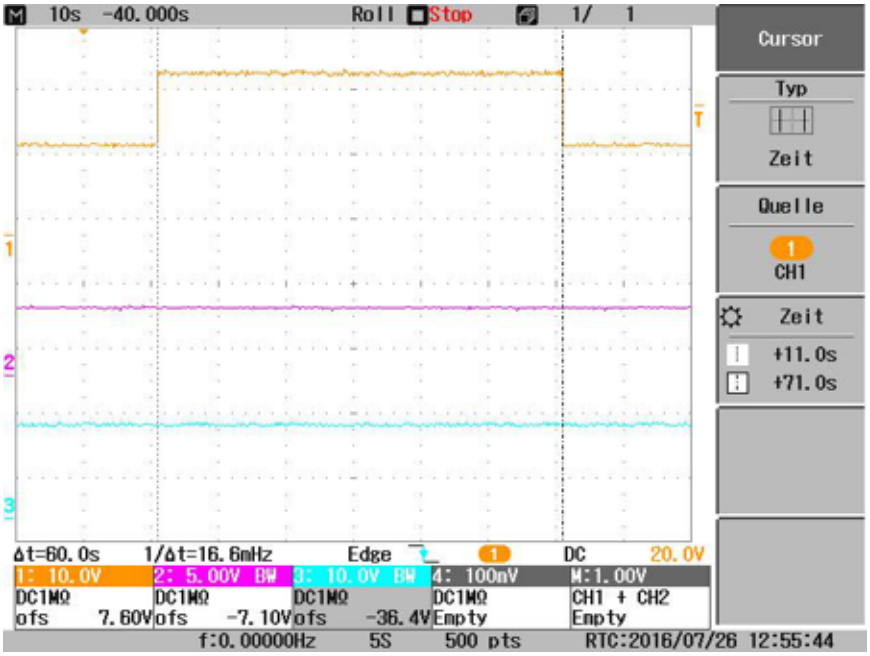


Figure 79. Outputs of Power Rails During Jump Start Test

NOTE: CH1: Jump start waveform applied to the system input, CH2: Output voltage of the buck converter, CH3: Output voltage of the buck-boost converter

5.11 ISO 16750-2: Reversed Voltage

ISO7637-2 reversed voltage test is defined as: "This test checks the ability of a DUT to withstand against the connection of a reversed battery in case of using an auxiliary starting device." The waveform of the reversed voltage, which is applied to the system input, is shown in Figure 80. A step-down voltage of –14 V is applied.

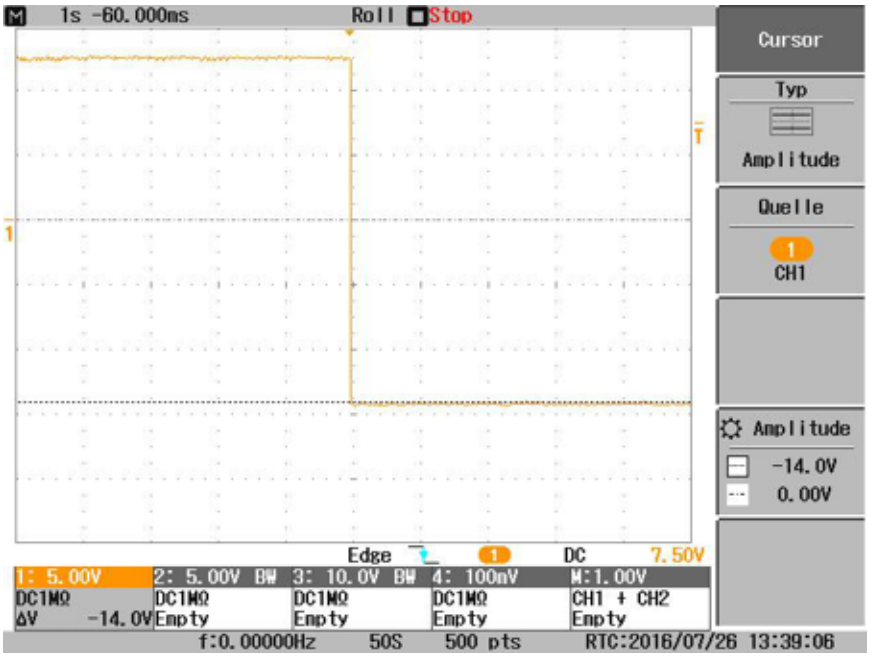


Figure 80. Applied Reversed Voltage Waveform

Figure 81 shows output power rails of the system during the reversed voltage test, which lasted for 60 seconds. Both the buck-boost converter and the buck converter recover and perform as designed after the test.

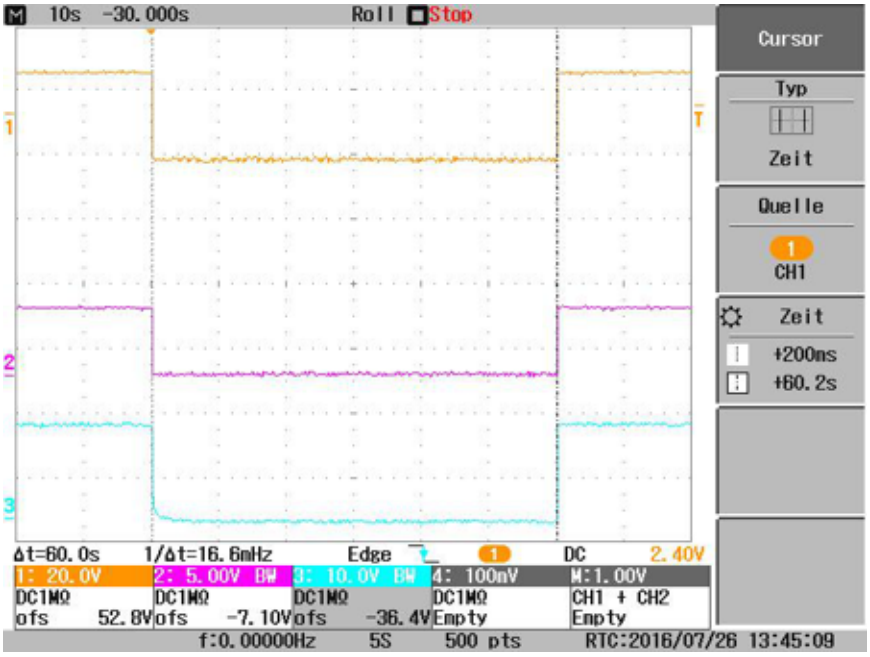


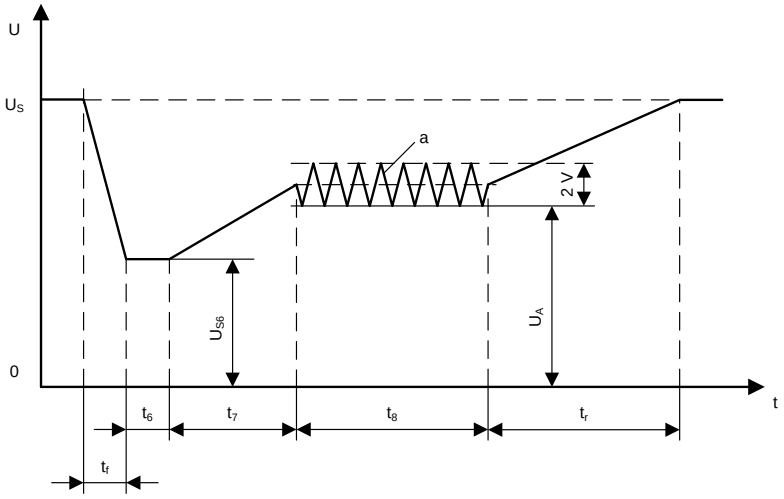
Figure 81. Outputs of Power Rails During Reversed voltage Test

NOTE: CH1: Reversed voltage waveform applied to the system input, CH2: Output voltage of the buck converter, CH3: Output voltage of the buck-boost converter

5.12 Cold Crank Test

Cranking tests simulate the droop in supply voltage when the engine is started due to the large current draw of the starter motor. The voltage levels are very dependent on the temperature of the car during start-up, with severe cold leading to the largest drop in voltage ("cold crank").

The starting profile values for systems with a 12-V nominal voltage are listed in Table 8. The TIDA-01179 is tested under severe cold cranking pulses (level 3) where the battery voltage droop down to 3.0 V for 15 ms. This is one of the key objectives of this design. The buck-boost converter needs to sustain the output voltage when the battery voltage falls very low, which also prevent the downstream circuits from malfunctioning.



Key

t	time
U	test voltage
t_f	falling slope
t_r	rising slope
t_6, t_7, t_8	duration parameters (in accordance with Table 8)
U_A	supply voltage for generator in operation (see ISO16750-1)
U_S	supply voltage
U_{S6}	supply voltage at t_6
a	f = 2 Hz

Figure 82. Battery Cranking Profile per ISO16750-2 Standard

Table 8. Starting Profile Values for Systems With 12-V Nominal Voltage

PARAMETER		LEVEL			
		I	II	III	IV
Voltage (V)	U_{S6}	8 (–0, 2)	4, 5 (–0, 2)	3 (–0, 2)	6 (–0, 2)
	U_S	9, 5 (–0, 2)	6, 5 (–0, 2)	5 (–0, 2)	6, 5 (–0, 2)
Duration (ms)	t_f	5 (±0, 5)	5 (±0, 5)	5 (±0, 5)	5 (±0, 5)
	t_6	15 (±1, 5)	15 (±1, 5)	15 (±1, 5)	15 (±1, 5)
	t_7	50 (±5)	50 (±5)	50 (±5)	50 (±5)
	t_8	1000 (±100)	10,000 (±1000)	1000 (±100)	10,000 (±1000)
	t_r	40 (±4)	100 (±10)	100 (±10)	100 (±10)
Minimum functional status		A[a]	B[a]	B[a]	A[a]
		A[b]	B[b]	C[b]	B[b]
		B[c]	C[c]	C[c]	C[c]
		B[d]	C[d]	C[d]	C[d]

5.12.1 Level 2 Test

The system outputs during the clod cranking test are shown in Figure 83. The system remains loaded with 3.5 A during the test.

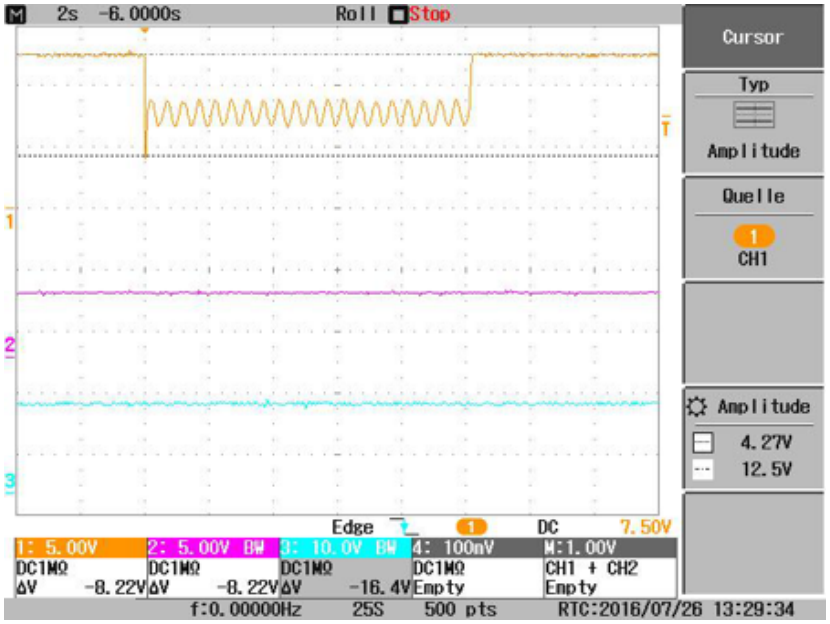


Figure 83. Cold Cranking Test Pulse (Level 2)

Figure 84 shows the expanded time scale at the beginning transient of the input pulse. The minimum voltage droop reached 4.06 V. Both the buck-boost and buck converter outputs remain constant.

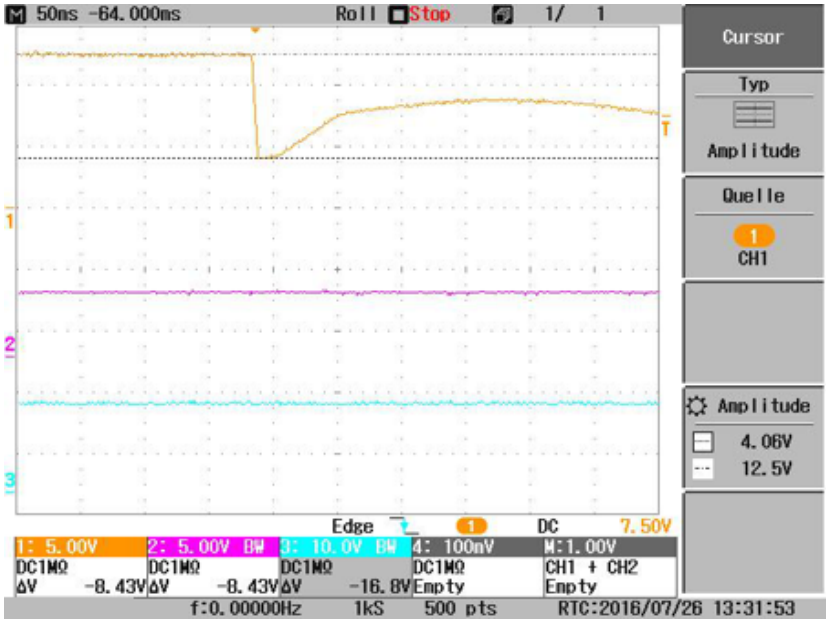


Figure 84. Expanded Time Scale at Beginning of Cold Cranking Pulse (Level 2)

NOTE: CH1: Test pulse applied to the system input, CH2: Output voltage of the buck converter, CH3: Output voltage of the buck-boost converter

5.12.2 Level 3 Test

Level 3 is the most stringent cold cranking pulse, where the minimum voltage droop can reach 3.0 V (as shown in Figure 85). The system outputs during the test are shown in Figure 86. During the test, the system remains loaded as 3.5 A.

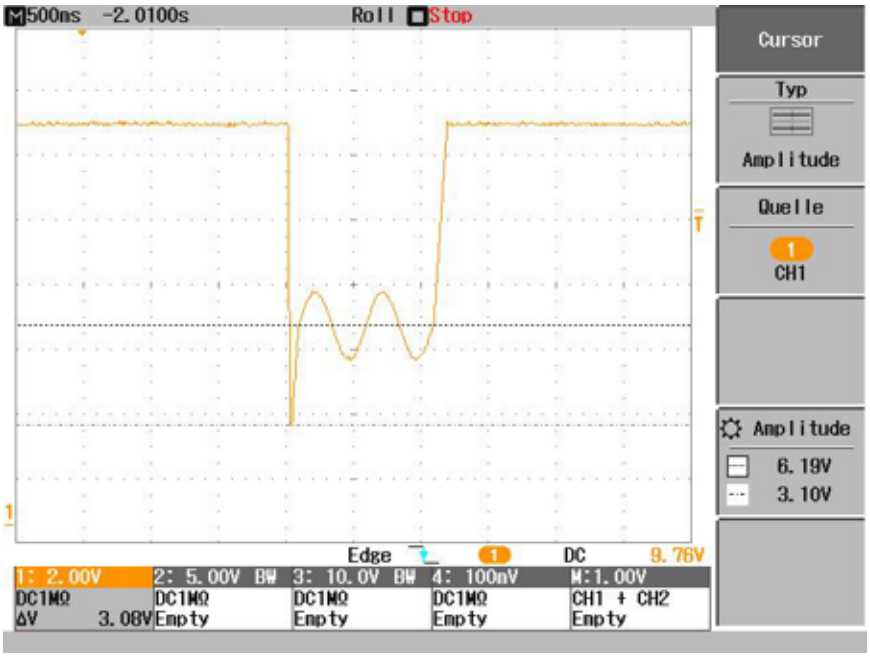


Figure 85. Severe Cold Cranking Test Pulse (Level 3)

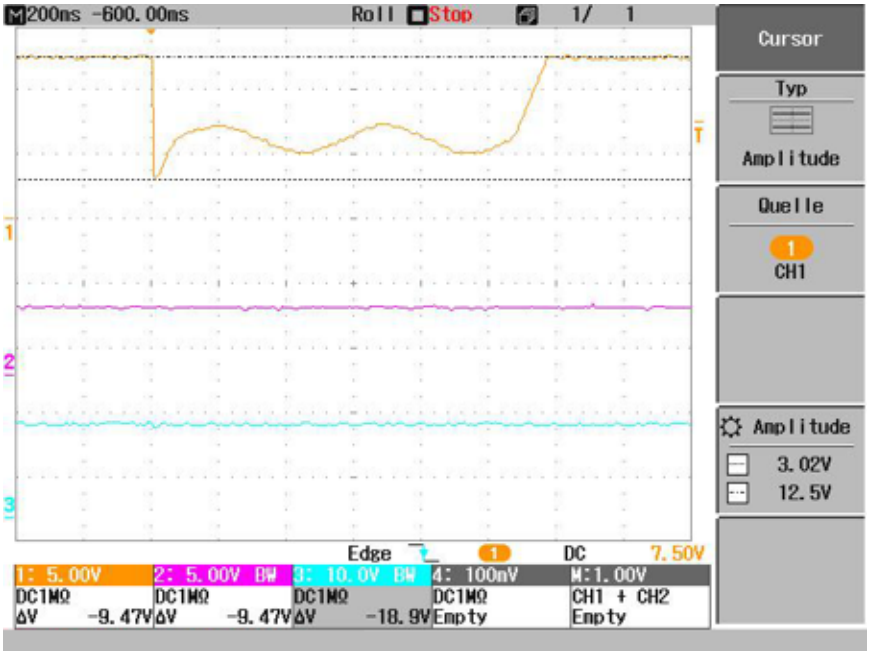


Figure 86. Outputs of Power Rails During Severe Cold Cranking Test (Level 3)

NOTE: CH1: Test pulse applied to the system input, CH2: Output voltage of the buck converter, CH3: Output voltage of the buck-boost converter

Figure 87 shows the expanded time scale at the beginning transient of a cold cranking pulse. The minimum voltage droop reached 3.02 V with a duration of 15 ms. Both the buck-boost and buck converter outputs remain constant.

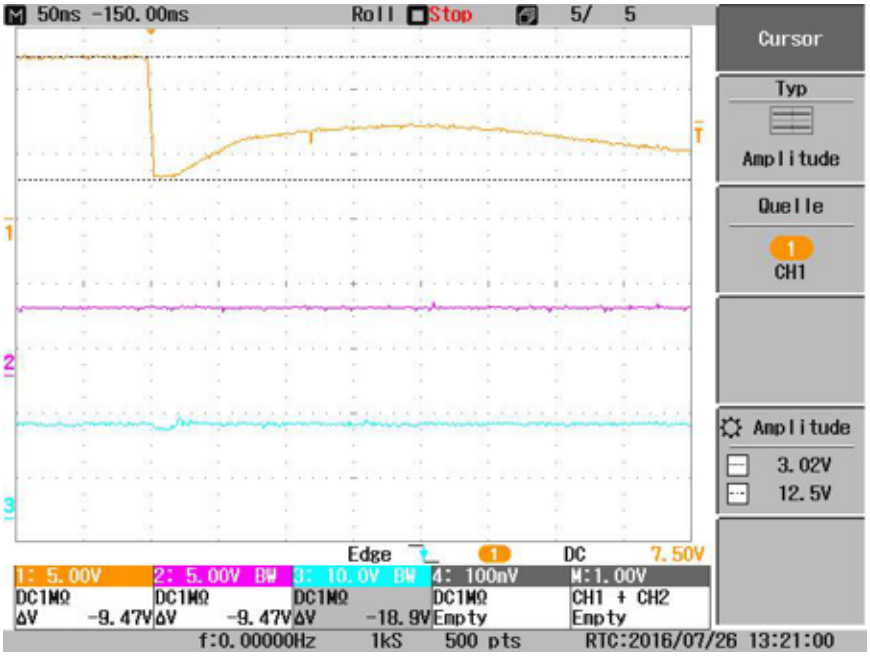


Figure 87. Expanded Time Scale at Beginning Transient of Cold Cranking Pulse (Level 3)

NOTE: CH1: Test pulse applied to the system input, CH2: Output voltage of the buck converter, CH3: Output voltage of the buck-boost converter

5.12.3 Summary of Electrical Transient Tests

Table 9 summarizes the performed transient pulse tests, the applied parameters, and the test results.

Table 9. Summary of Electrical Transient Pulse Tests

PARAMETER	$V_{MAX/MIN}$ (V)	R_{SOURCE} (Ω)	T_r	$T_{DURATION}$	T_{TOTAL}	I_{LOAD} (A)	V_{INDC} (V)	RESULT
ISO 7637-2: Pulse 1	–150	10	1 µs	2 ms	42 minutes	3.5	13.5	Pass
ISO 7637-2: Pulse 2a	112	2	1 µs	50 µs	42 minutes	3.5	13.5	Pass
ISO 7637-2: Pulse 3a	–220	50	5 ns	0.1 µs	60 minutes	3.5	13.5	Pass
ISO 7637-2: Pulse 3b	150	50	5 ns	0.1 µs	60 minutes	3.5	13.5	Pass
Jump Start	26	4	10 ms	60 s	60 seconds	3.5	26	Pass
Reversed Voltage	–14	4	10 ms	60 s	60 seconds	3.5	–14	Pass
Cold Crank level 2	4.5	4	100 ms	NA	10 seconds	3.5	NA	Pass
Cold Crank level 3	3	4	100 ms	NA	1.2 seconds	3.5	NA	Pass

where:

- V_{MAX} is the maximum peak voltage of the pulse
- R_{SOURCE} is the source impedance
- T_r is the rising slope time
- $T_{DURATION}$ is the duration of the pulse
- T_{TOTAL} is the total testing time
- I_{LOAD} is the load current
- V_{INDC} is the input DC voltage
- NA — not applicable

5.13 CISPR25 Conducted Emissions Testing

CISPR 25 contains limits and procedures for the measurement of radio disturbances in the frequency range of 150 kHz to 2.5 GHz. The standard applies to any electronic or electrical component intended for use in vehicles, trailers, and devices. The emission standard consists of conducted emission and radiated emission, respectively. The TIDA-01179 focuses on the conducted emission tests. Radiated emissions are not of interest because this subsystem as part of the HEV/EV traction inverter system is placed into an aluminum case where most the radiated emissions will be shielded.

5.13.1 Conducted Emissions Test Setup and Conditions

The test setup for conducted emission is shown in Figure 88 as per outlined in the CISPR 25 standard documentation. The EUT is powered through an artificial network or LISN and loaded. The EUT must be placed on a non-conductive, low relative permittivity material $\varepsilon r \leq 1.4$) at (50 ± 5) mm above the ground plane. The power supply lines between the connector of artificial network and the connector of the EUT must have a standard length of 200 mm. The load simulator is placed directly on the ground plane. A spectrum analyzer is connected to the artificial network through a BNC cable to measure the conducted emission of the EUT.

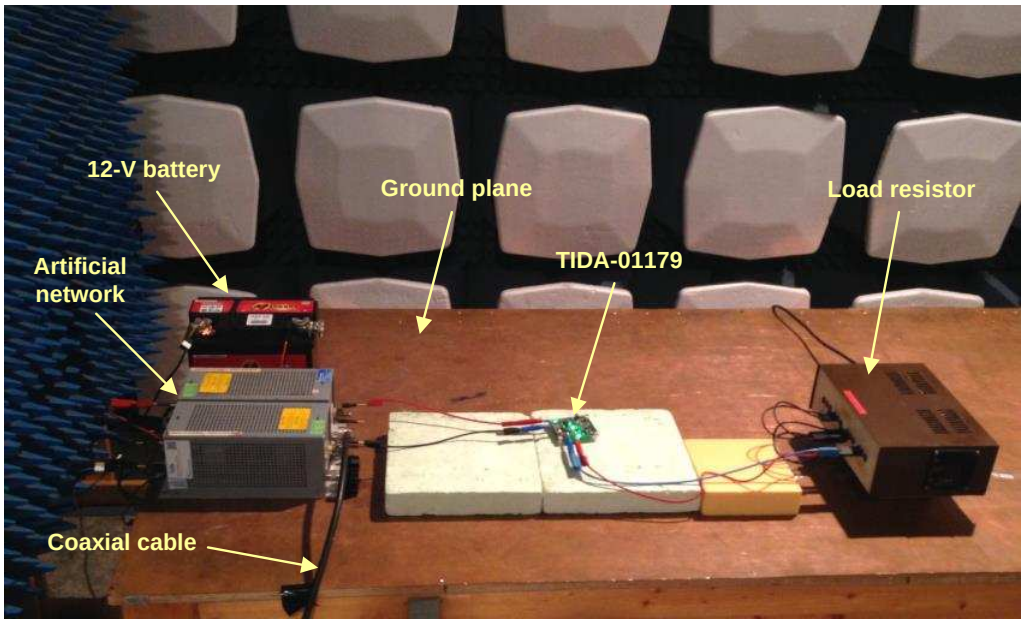


Figure 88. Conducted Emission Measurement Setup

Table 10 and Table 11 show the peak limits and average limits from CISPR 25 standard. OEMs define which class a specific subsystem must satisfy.

Table 10. Conducted Emission Peak Limits per CISPR 25

SERVICE OR BAND	FREQ (MHz)	LEVELS IN dB(µV)									
		CLASS 1		CLASS 2		CLASS 3		CLASS 4		CLASS 5	
		PEAK	QUASI-PEAK	PEAK	QUASI-PEAK	PEAK	QUASI-PEAK	PEAK	QUASI-PEAK	PEAK	QUASI-PEAK
BROADCAST											
LW	0.15 to 0.30	110	97	100	87	90	77	80	67	70	57
MW	0.53 to 1.8	86	73	78	65	70	57	62	49	54	41
SW	5.9 to 6.2	77	64	71	58	65	52	59	46	53	40
FM	76 to 108	62	49	56	43	50	37	44	31	38	25
TV Band I	41 to 88	58	—	52	—	46	—	40	—	34	—
TV Band III DAB III TV Band IV/V DTTV DAB L band SDARS	174 to 230 171 to 245 468 to 944 470 to 770 1447 to 1494 2320 to 2345	Conducted emission — Voltage method Not applicable									
MOBILE SERVICES											
CB	26 to 28	68	55	62	49	56	43	50	37	44	31
VHF	30 to 54	68	55	62	49	56	43	50	37	44	31
VHF	68 to 87	62	49	56	43	50	37	44	31	38	25

Table 11. Conducted Emission Average Limits

SERVICE OR BAND	FREQ (MHz)	LEVELS IN dB(µV)				
		CLASS 1	CLASS 2	CLASS 3	CLASS 4	CLASS 5
		AVG	AVG	AVG	AVG	AVG
BROADCAST						
LW	0.15 to 0.30	90	80	70	60	50
MW	0.53 to 1.8	66	58	50	42	34
SW	5.9 to 6.2	57	51	45	39	33
FM	76 to 108	42	36	30	24	18
TV Band I	41 to 88	48	42	36	30	24
TV Band III DAB III TV Band IV/V DTTV DAB L band SDARS	174 to 230 171 to 245 468 to 944 470 to 770 1447 to 1494 2320 to 2345	Conducted emission — Voltage method Not applicable				
MOBILE SERVICES						
CB	26 to 28	48	42	36	30	24
VHF	30 to 54	48	42	36	30	24
VHF	68 to 87	42	36	30	24	18

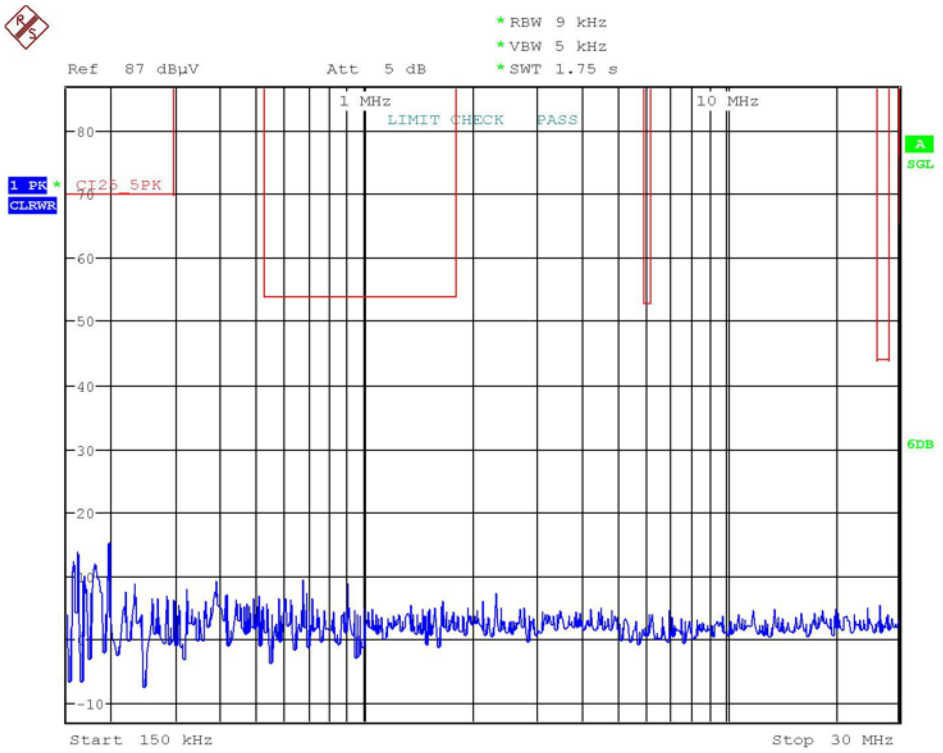


Figure 89. Ambient Noise (150 kHz to 30 MHz)

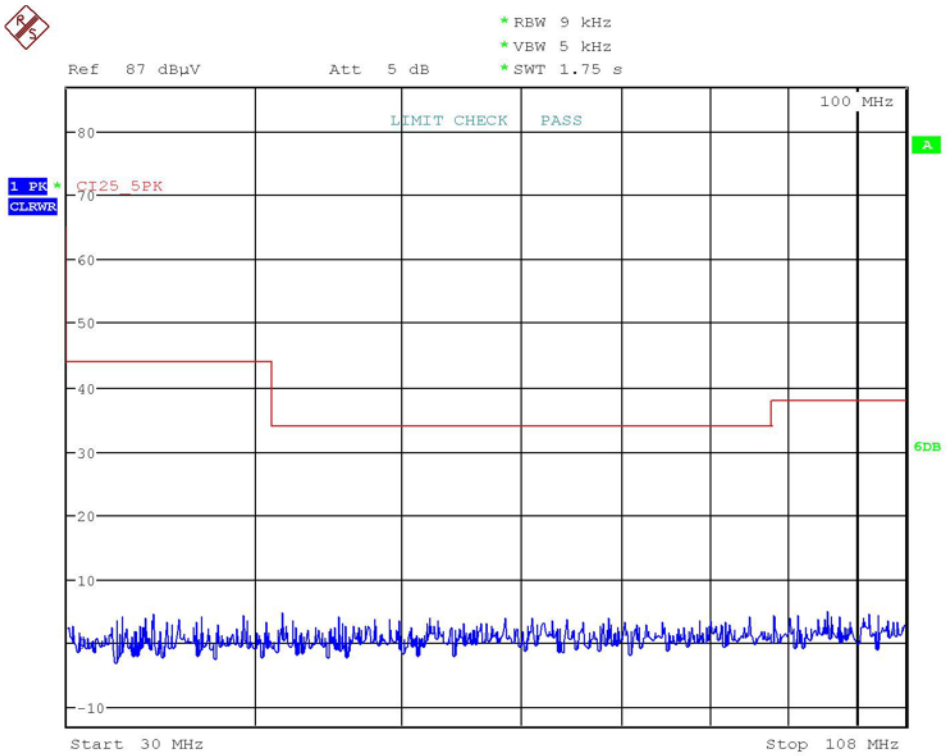


Figure 90. Ambient Noise (30 to 108 MHz)

5.13.2 Filter Implementation

Conducted EMI is tested with implementing DM and CM filters, respectively. The DM filter is implemented on board as introduced in Section 2.4.1.

The CM filter for TIDA-01179 is implemented externally on a separate board. It is connected to the TIDA-01179 design board for high frequency noise filtering. The schematic is shown in Figure 91. The CM choke appears high impedance over a broad high frequency range.

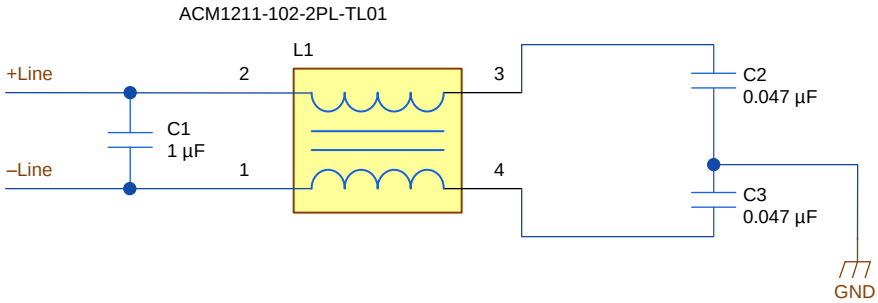


Figure 91. Schematic of Implemented CM Filter

Table 12. TIDA-01179 CM Filter BOM

DESIGNATOR	VALUE	PARTNUMBER	DESCRIPTION	FOOTPRINT	QTY
C1	1 µF	MKS4D041003F00KSSD	CAP, film, 1 µF, 100 V, ±10%	Bulk	1
L1	47 µF	ACM1211-102-2PL-TL01	1 kΩ at 100-MHz CM choke	Horizontal, 4 PC pad	1
C2, C3	0.047 µF	GCM21BR72A473KA37L	0.047-µF, 100-V ceramic capacitor X7R 0805	0805	2

5.13.3 With 13.5-V Input voltage

First, the conducted EMI is tested with 13.5-V nominal input voltage. The emissions are measured under various circuit configurations as listed here. The system is loaded at 3.5 A under all the test conditions. All tests are done on the +Line at the input of the board.

- Test condition 1 as shown in Figure 92
- Test condition 2 as shown in Figure 97
- Test condition 3 as shown in Figure 99
- Test condition 4 as shown in Figure 101

The experiments show that the system passed the Class 5 peak limit in the range from 150 kHz to 30 MHz with DM filter only, but fails in the average test. With the designed CM and DM filters, the system successfully passed CISPR 25 Class 5 tests (both average and peak limits).

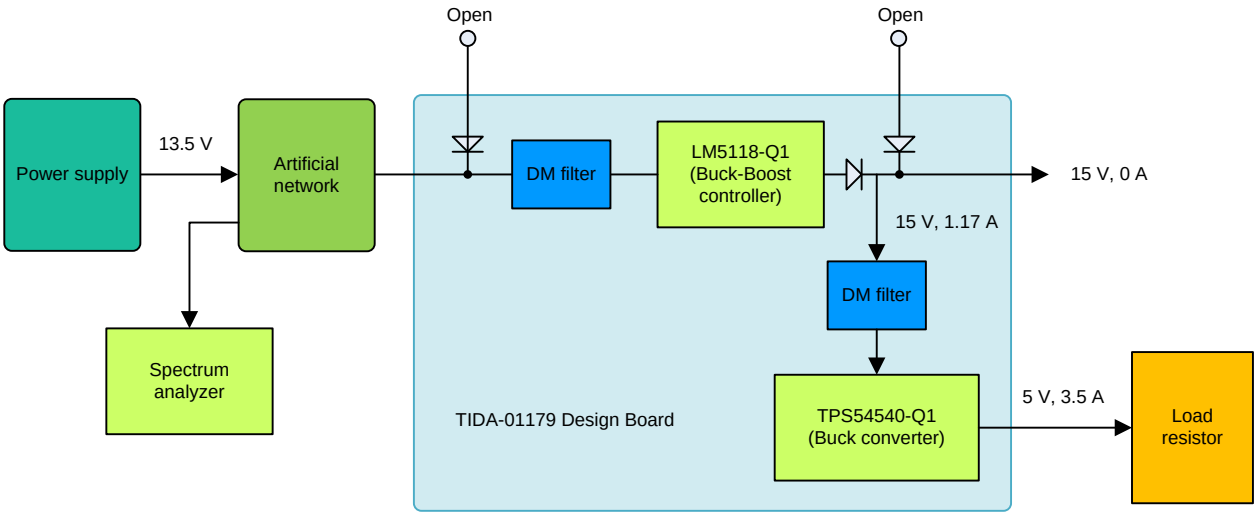


Figure 92. Test Circuit 1 With DM Filter

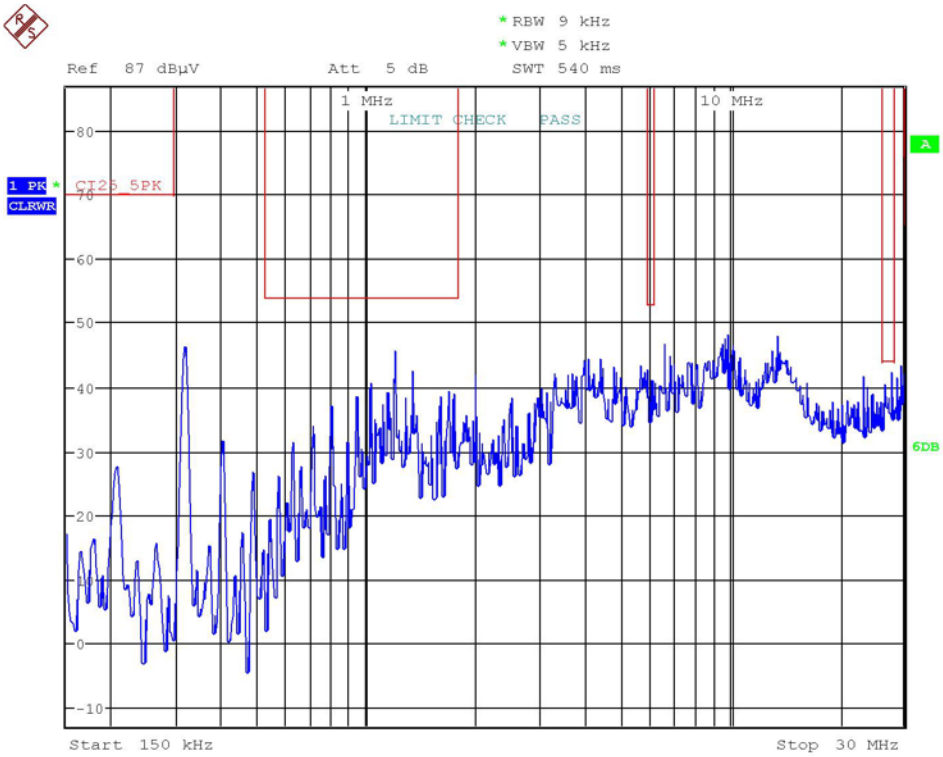


Figure 93. Measured Peak Noise of Test Circuit 1 (150 kHz to 30 MHz, Limit Line: CISPR 25 Class 5 Peak, Limit Check: Pass)

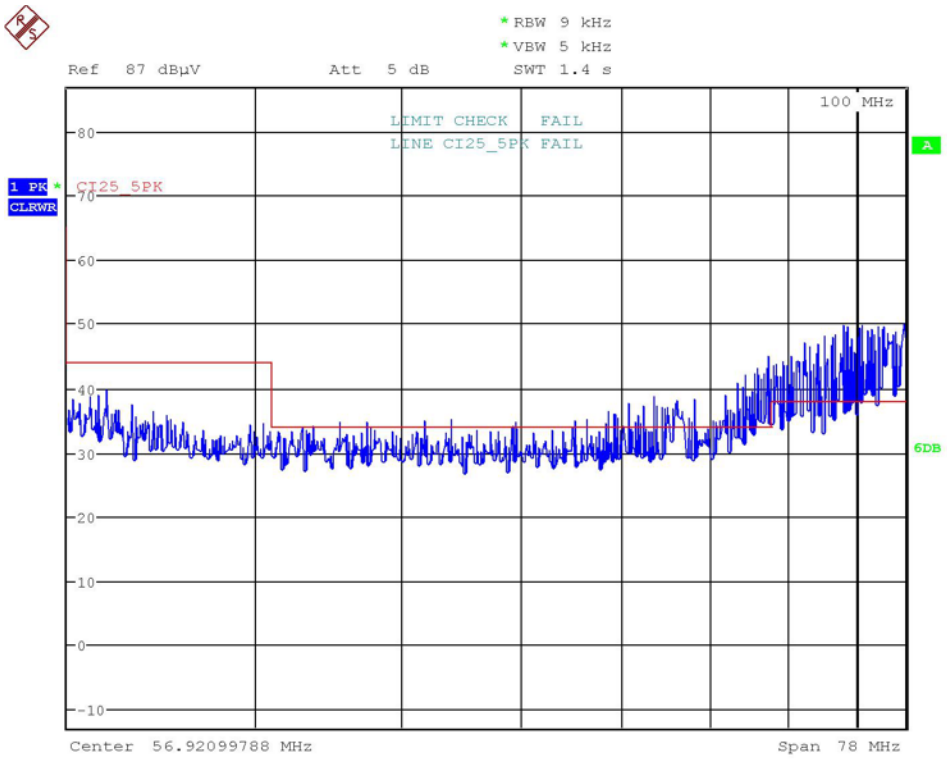


Figure 94. Measured Peak Noise of Test Circuit 1
(30 to 108 MHz, Limit Line: CISPR 25 Class 5 Peak, Limit Check: Fail)

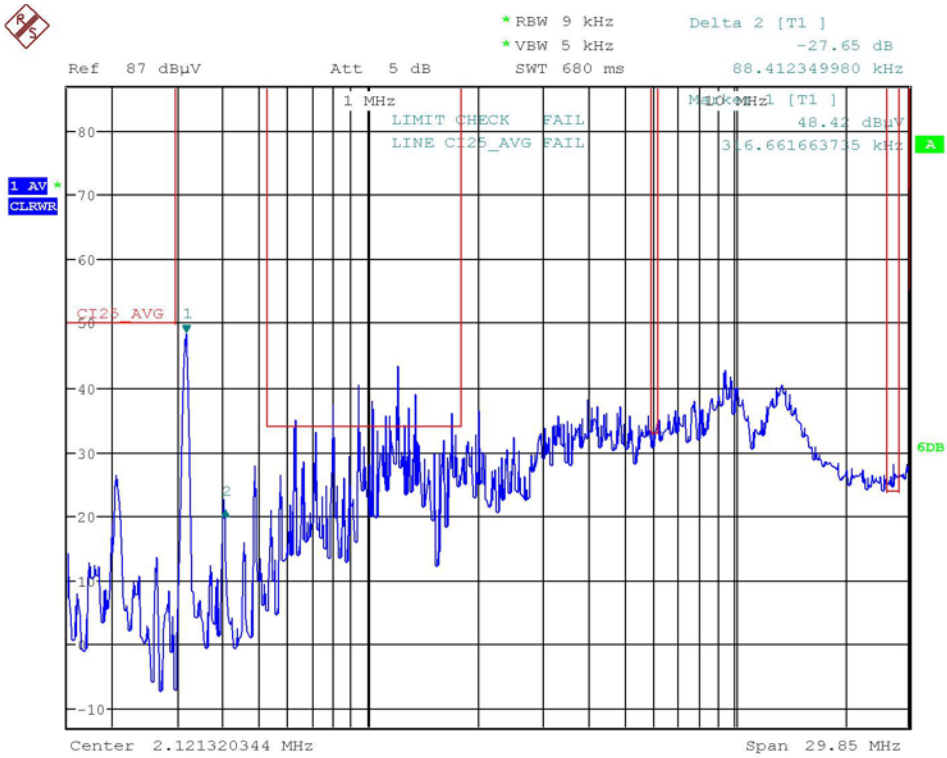


Figure 95. Measured Average Noise of Test Circuit 1
(150 kHz to 30 MHz, Limit Line: CISPR 25 Class 5 Average, Limit Check: Fail)

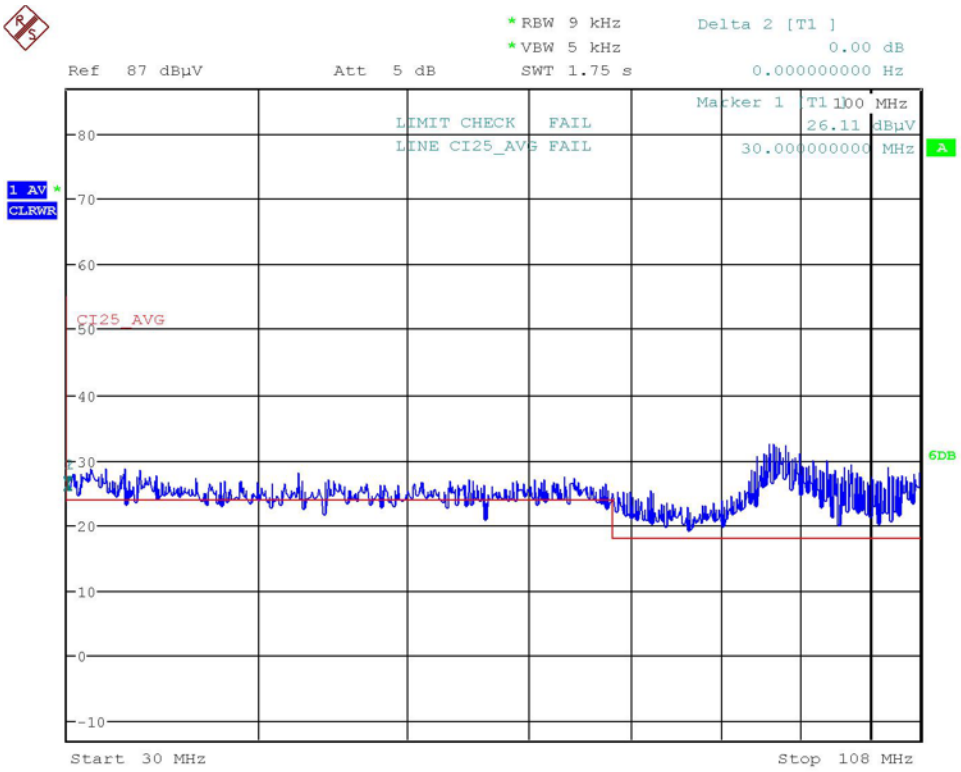


Figure 96. Measured Average Noise of Test Circuit 1
(30 to 108 MHz, Limit Line: CISPR 25 Class 5 Average, Limit Check: Fail)

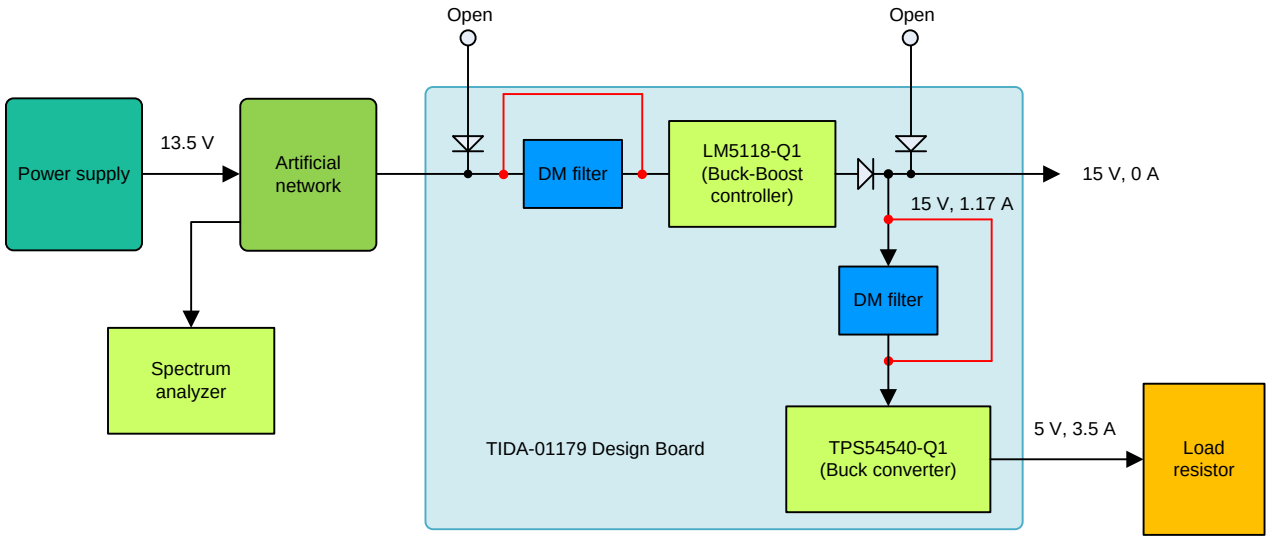


Figure 97. Test Circuit 2 With Both Buck-Boost and Buck DM Filter Inductors Bypassed

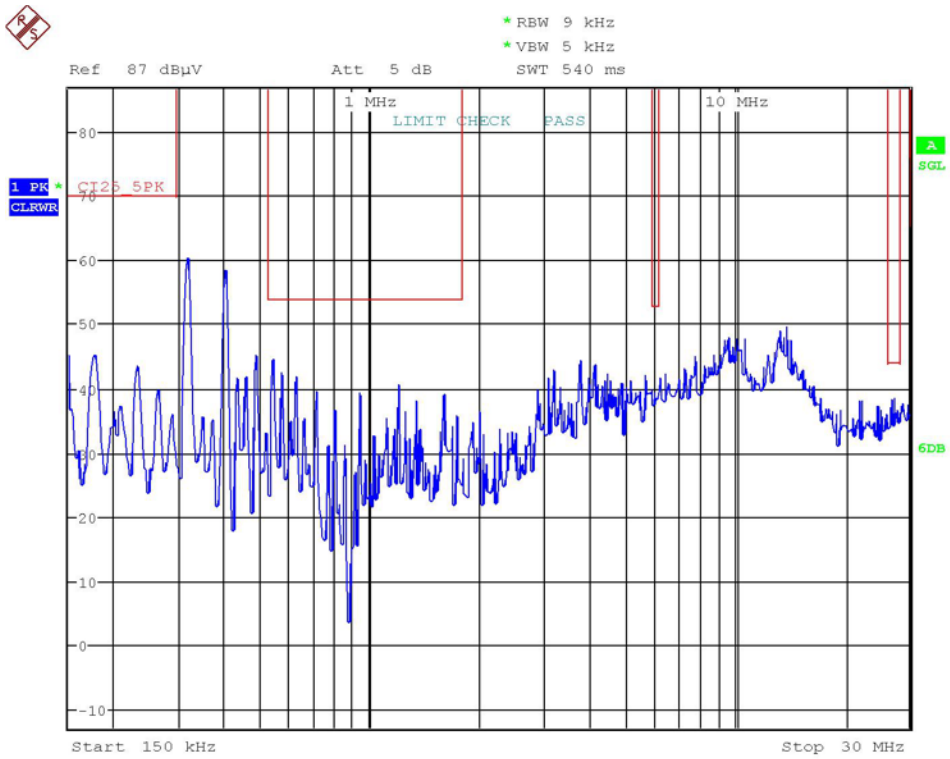


Figure 98. Measured Peak Noise of Test Circuit 2 (150 kHz to 30 MHz, Limit Line: CISPR 25 Class 5 Peak, Limit Check: Pass)

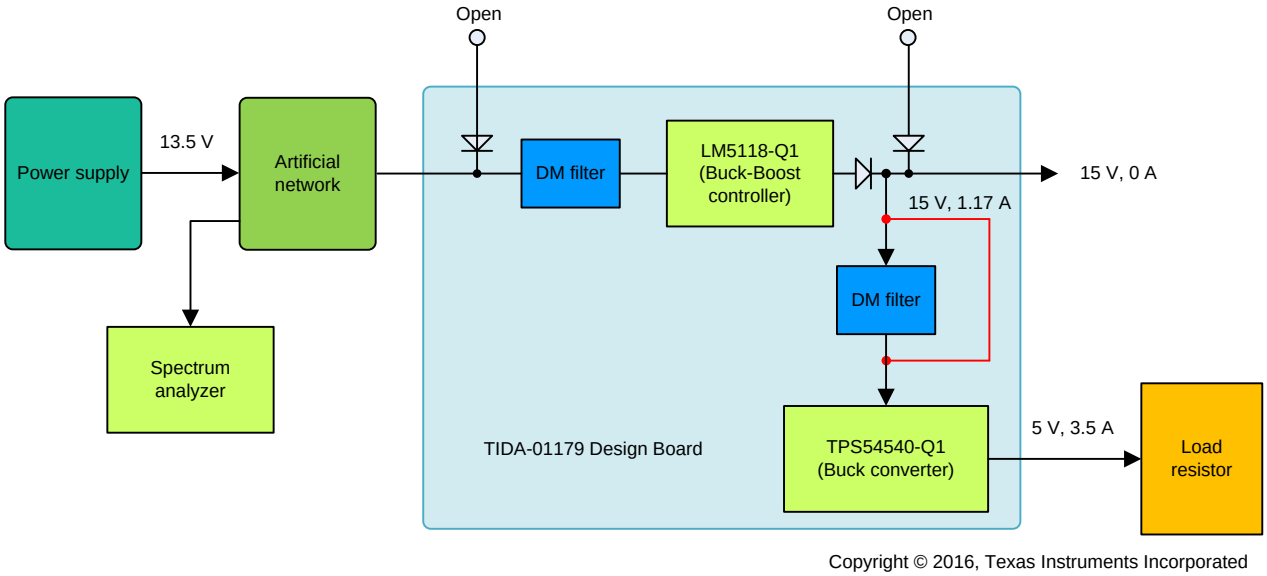


Figure 99. Test Circuit 3 With Buck DM Filter Inductor Bypassed

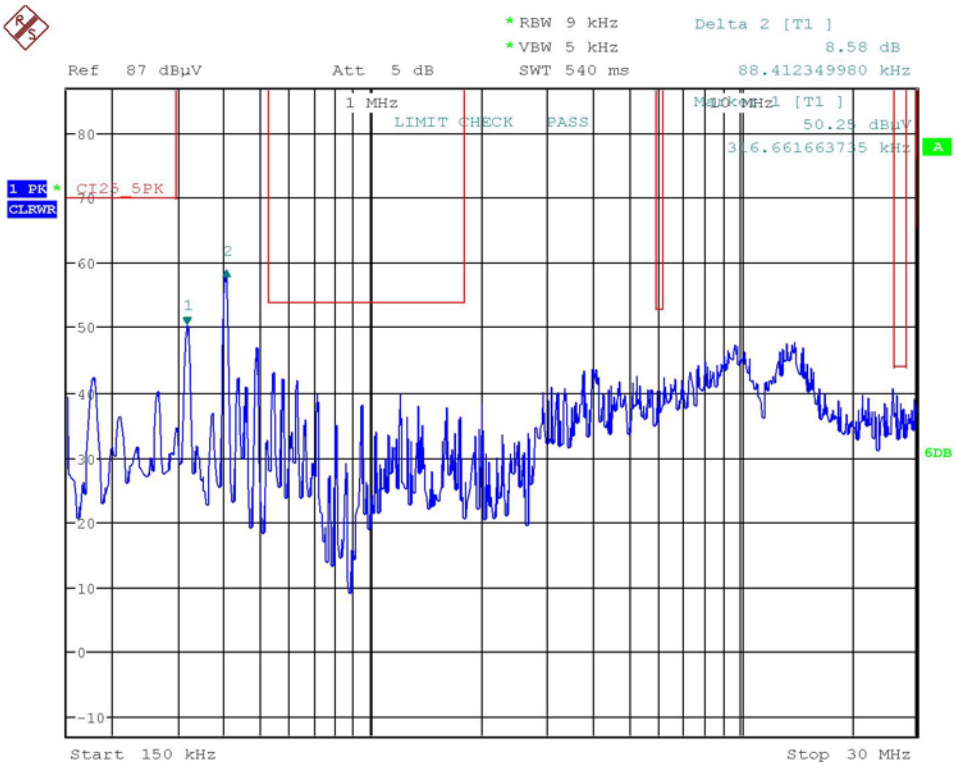


Figure 100. Measured Peak Noise of Test Circuit 3 (150 kHz to 30 MHz, Limit Line: CISPR 25 Class 5 Peak, Limit Check: Pass)

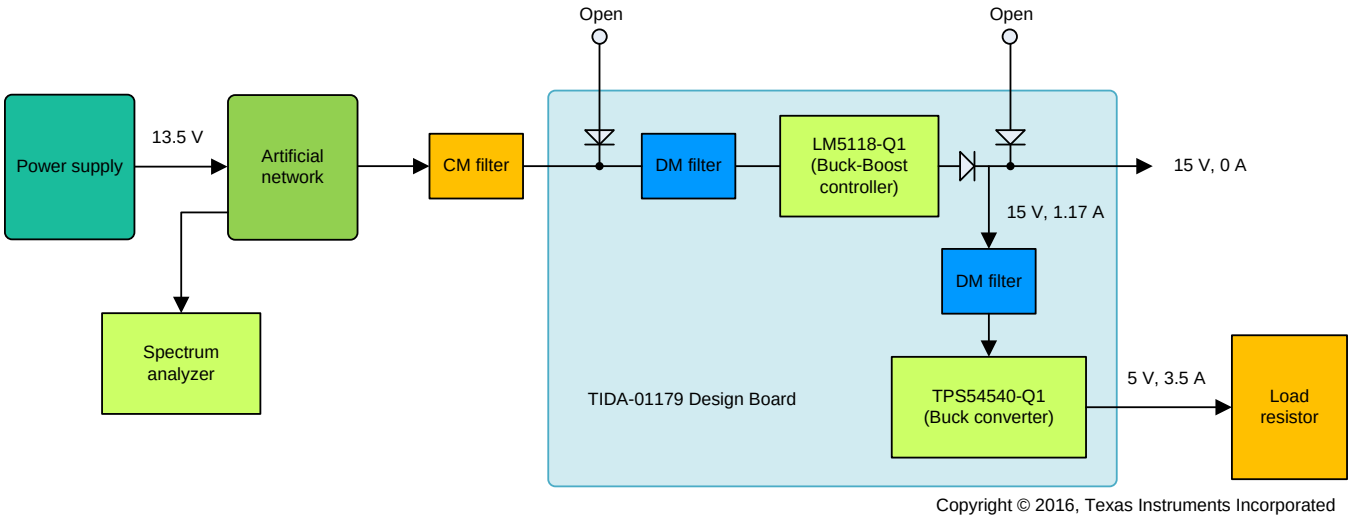


Figure 101. Test Circuit 4 With Both CM and DM Filters

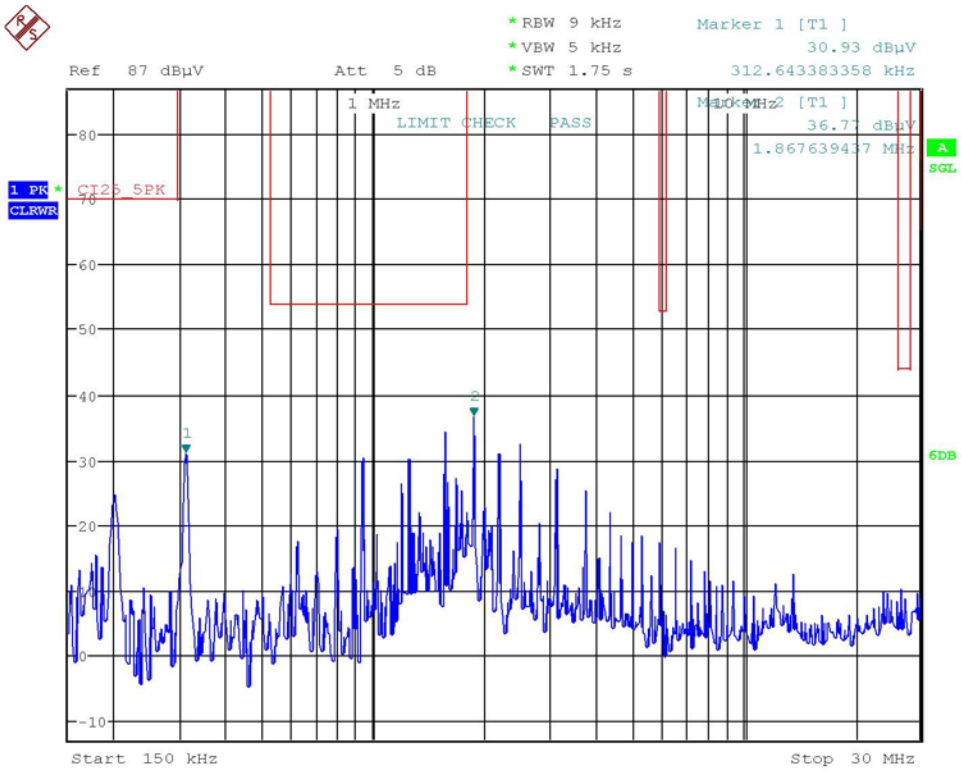


Figure 102. Measured Peak Noise of Test Circuit 4 (150 kHz to 30 MHz, Limit Line: CISPR 25 Class 5 Peak, Limit Check: Pass)

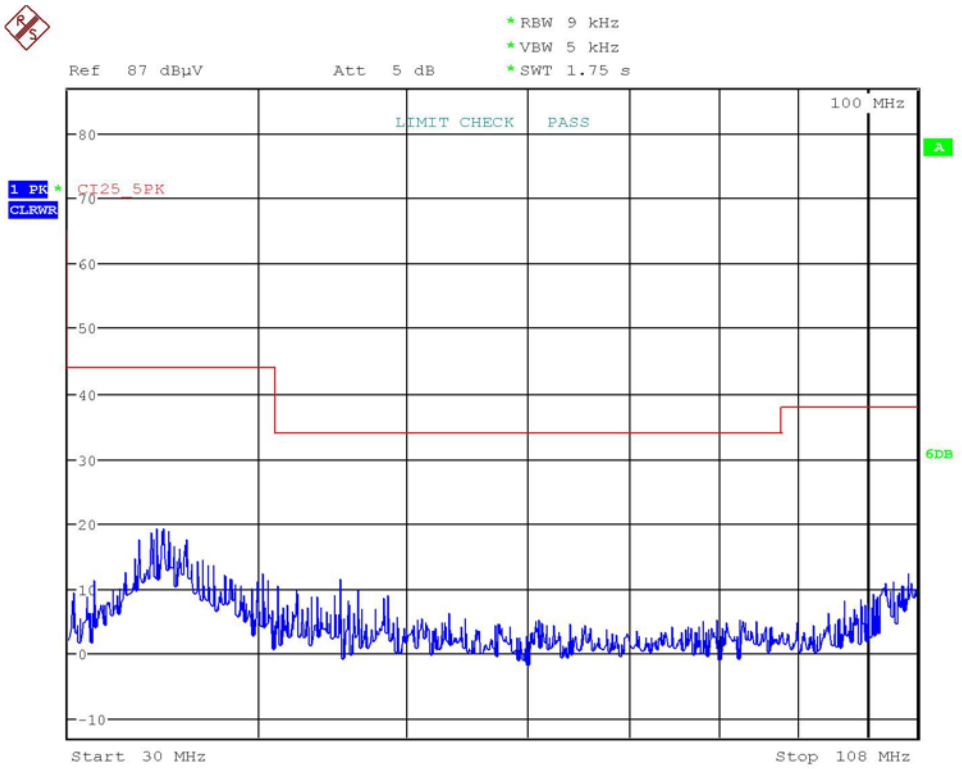


Figure 103. Measured Peak Noise of Test Circuit 4 (30 to 108 MHz, Limit Line: CISPR 25 Class 5 Peak, Limit Check: Pass)

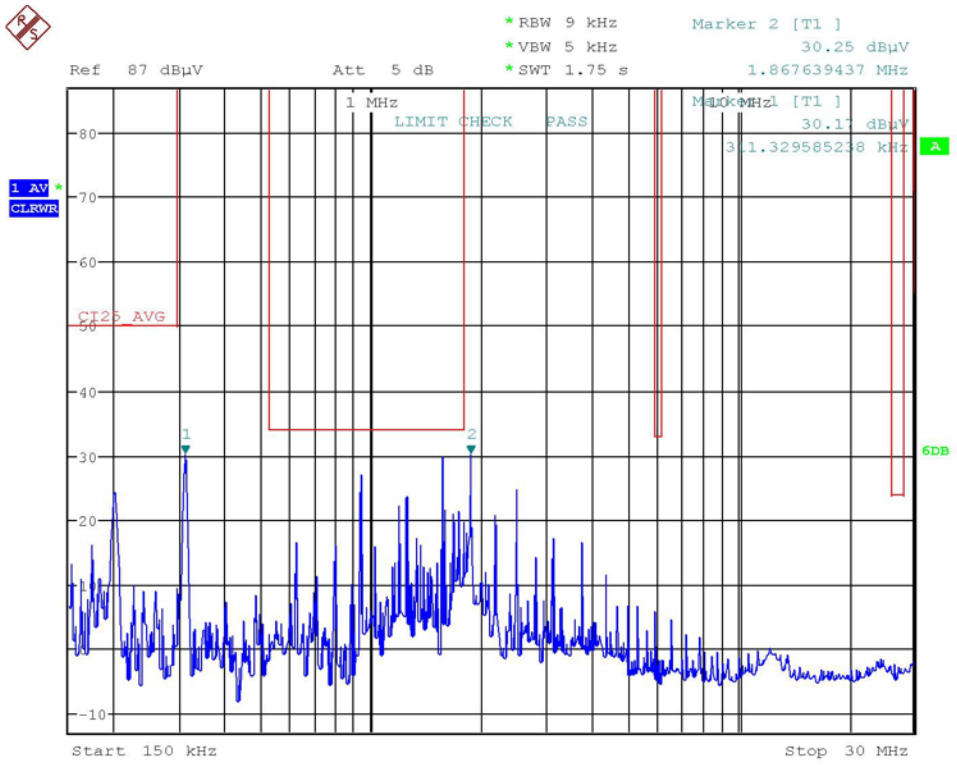


Figure 104. Measured Average Noise of Test Circuit 4
(150 kHz to 30 MHz, Limit Line: CISPR 25 Class 5 Average, Limit Check: Pass)

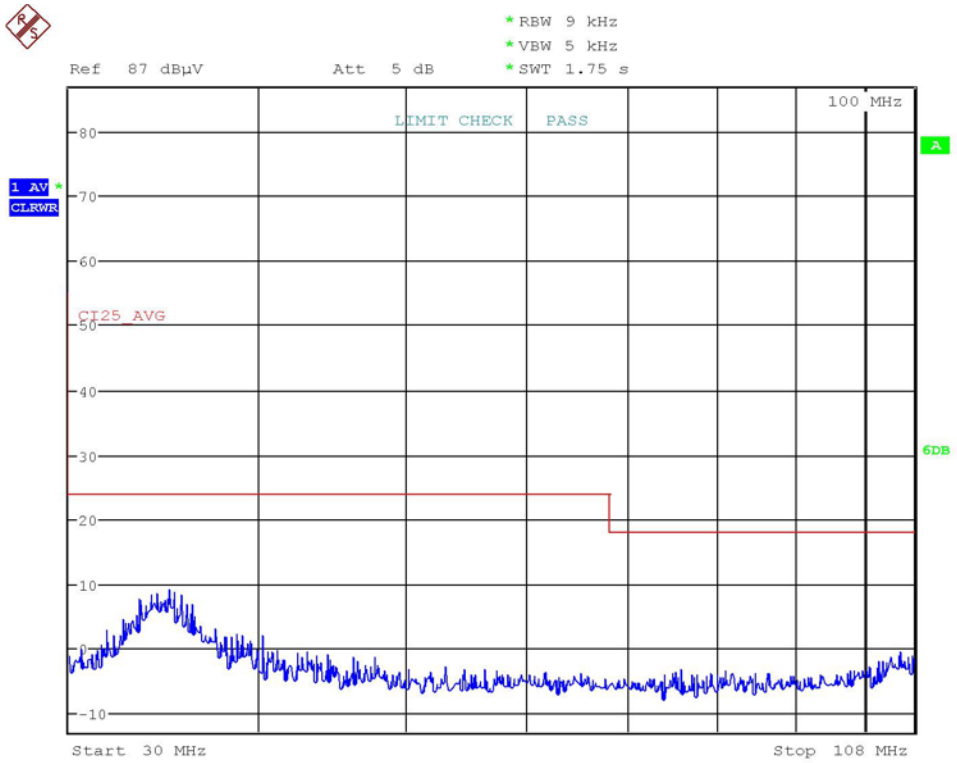


Figure 105. Measured Average Noise of Test Circuit 4
(30 to 108 MHz, Limit Line: CISPR 25 Class 5 Average, Limit Check: Pass)

5.13.4 With 6-V Input voltage

Secondly, the conducted EMI is tested with a 6-V input voltage. The emissions are measured under various circuit configurations as listed. The system is loaded at 3.5 A under all the test conditions. The experiments show that the system passes CISPR 25 Class 5 peak limit however fails in average limit. With the designed CM and DM filters the system successfully passed CISPR 25 Class 5 tests (both average and peak limits).

- Test condition 1 as shown in Figure 106
- Test condition 2 as shown in Figure 111

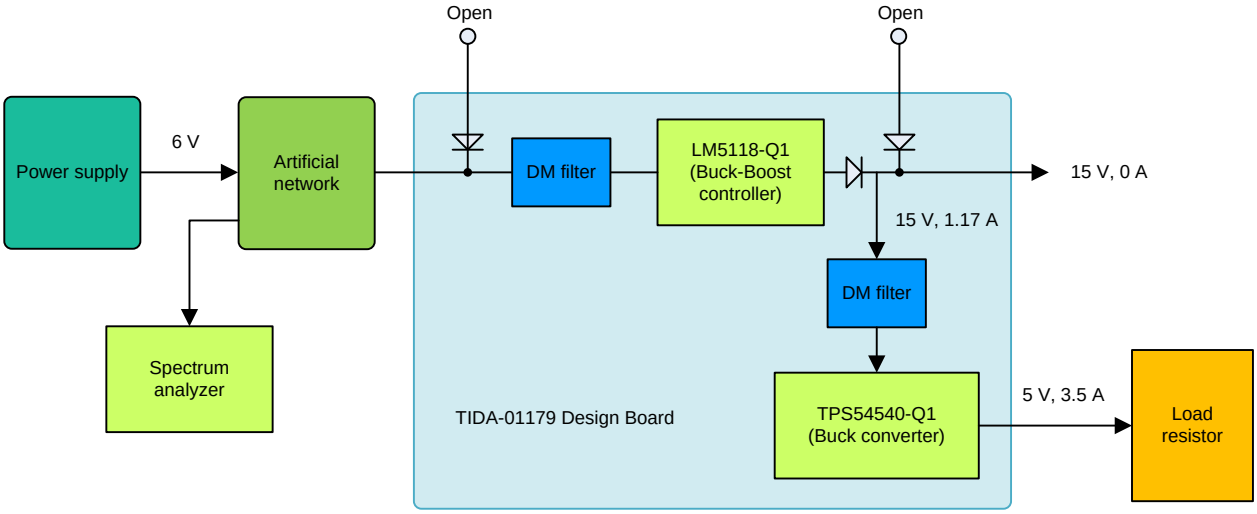


Figure 106. Test Circuit 1 With DM Filter, Without CM Filter

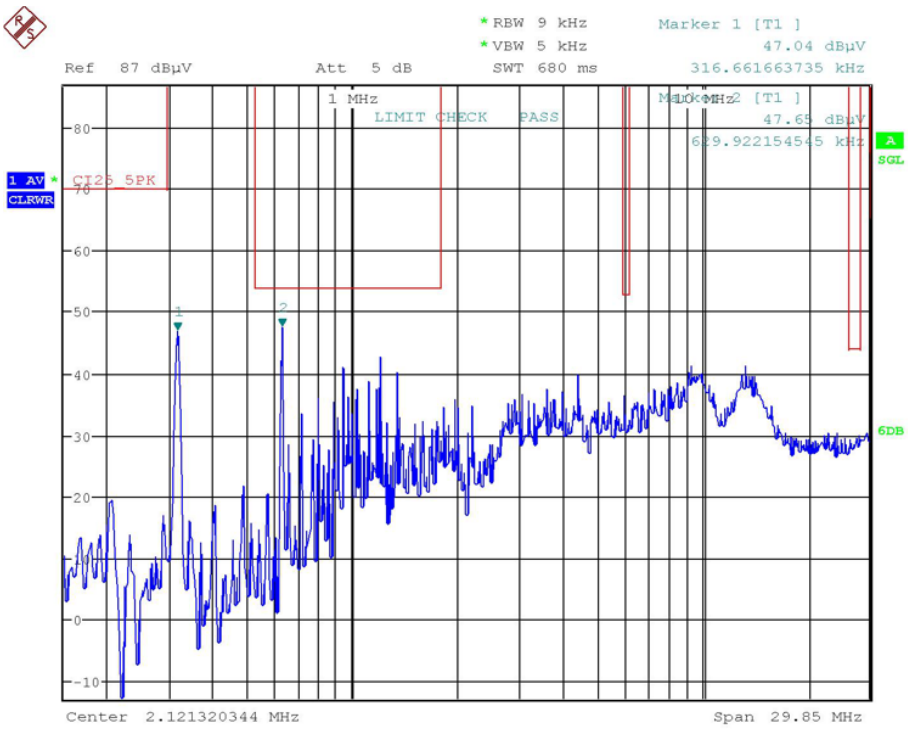


Figure 107. Measured Peak Noise of Test Circuit 1 (150 kHz to 30 MHz, Limit Line: CISPR 25 Class 5 Peak, Limit Check: Pass)

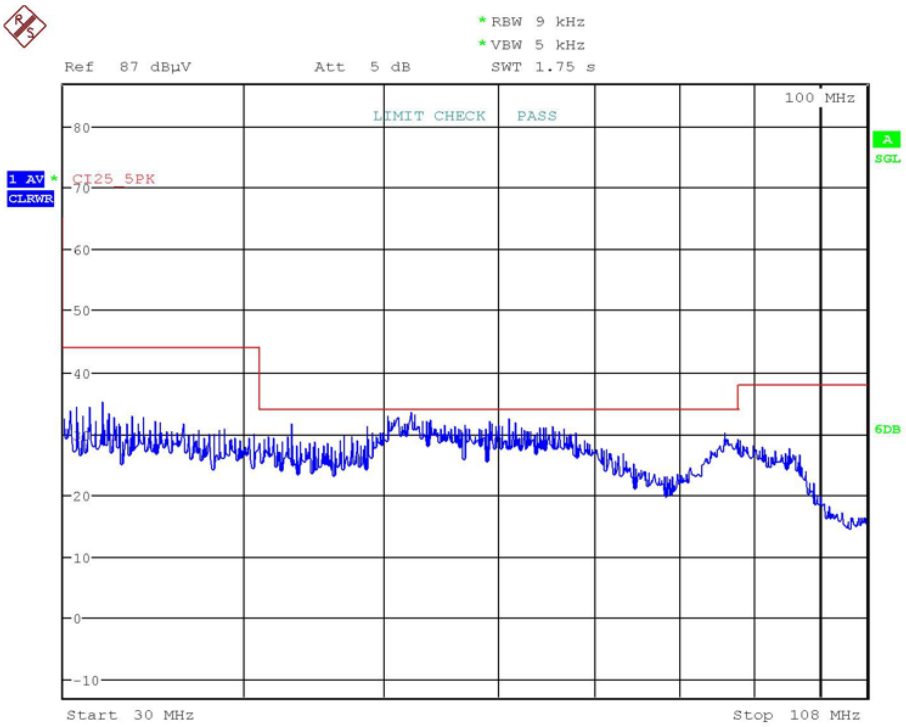


Figure 108. Measured Peak Noise of Test Circuit 1
(30 to 108 MHz, Limit Line: CISPR 25 Class 5 Peak, Limit Check: Pass)

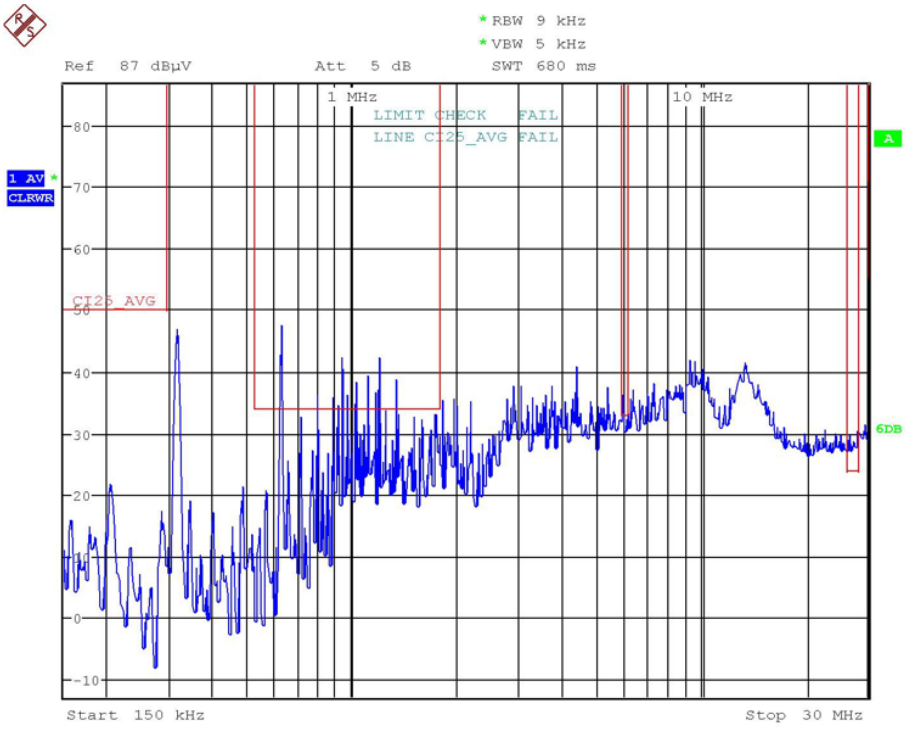


Figure 109. Measured Average Noise of Test Circuit 1
(150 kHz to 30 MHz, Limit Line: CISPR 25 Class 5 Average, Limit Check: Fail)

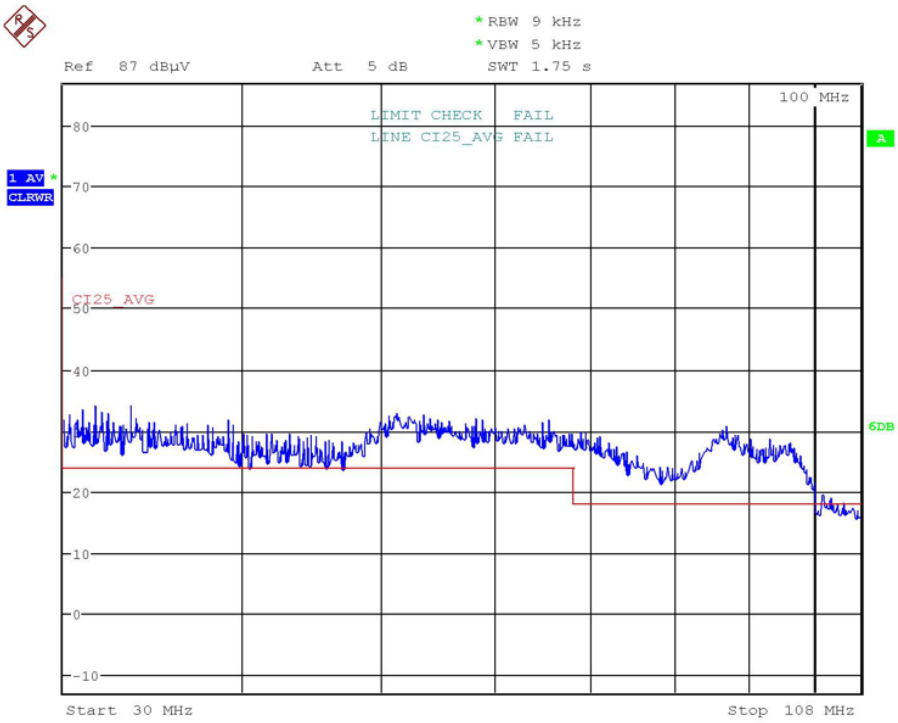


Figure 110. Measured Average Noise of Test Circuit 1
(30 to 108 MHz, Limit Line: CISPR 25 Class 5 Average, Limit Check: Fail)

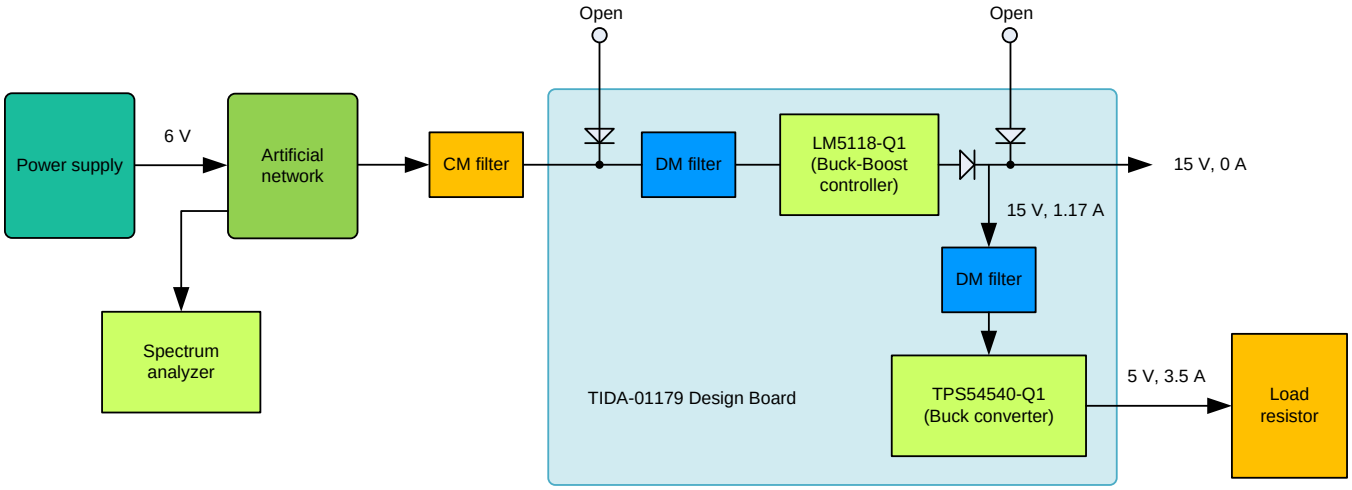


Figure 111. Test Circuit 2 With Both CM and DM Filters

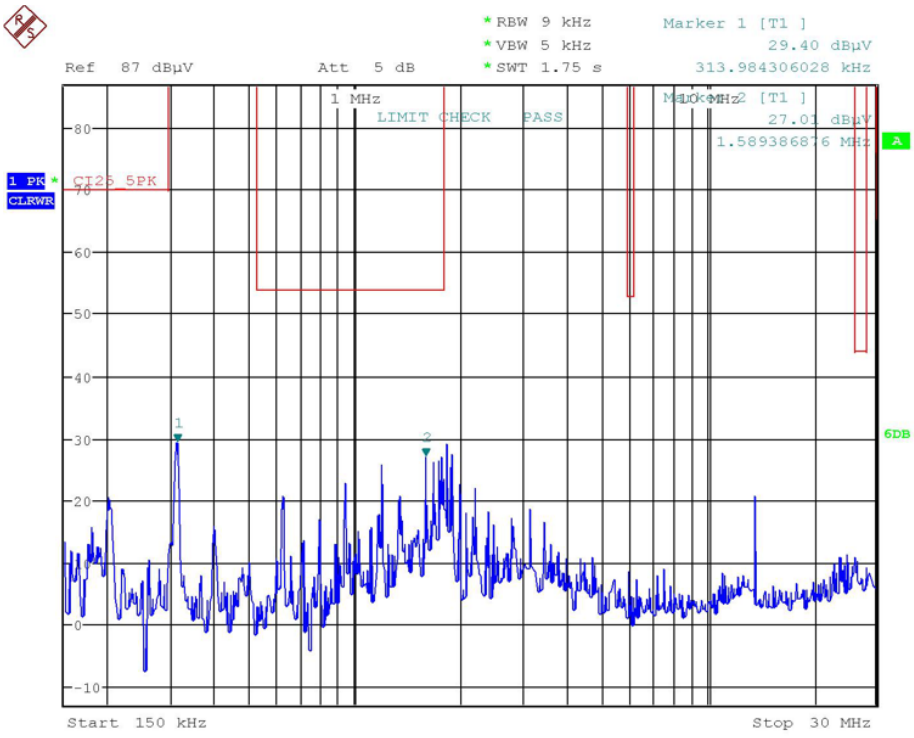


Figure 112. Measured Peak Noise of Test Circuit 2 (150 kHz to 30 MHz, Limit Line: CISPR 25 Class 5 Peak, Limit Check: Pass)

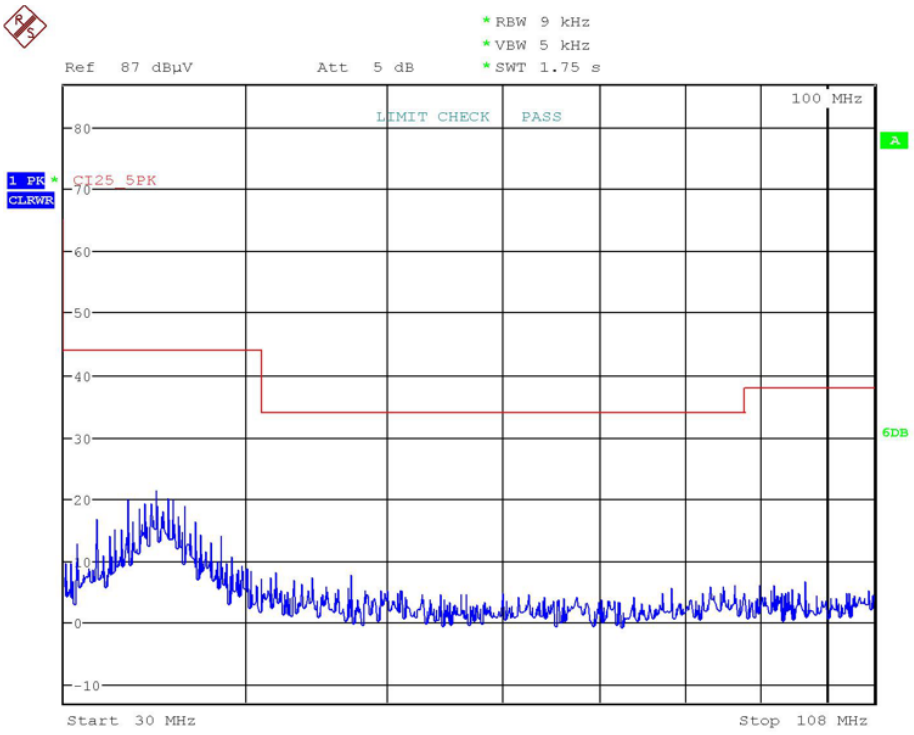


Figure 113. Measured Peak Noise of Test Circuit 2 (30 to 108 MHz, Limit Line: CISPR 25 Class 5 Peak, Limit Check: Pass)

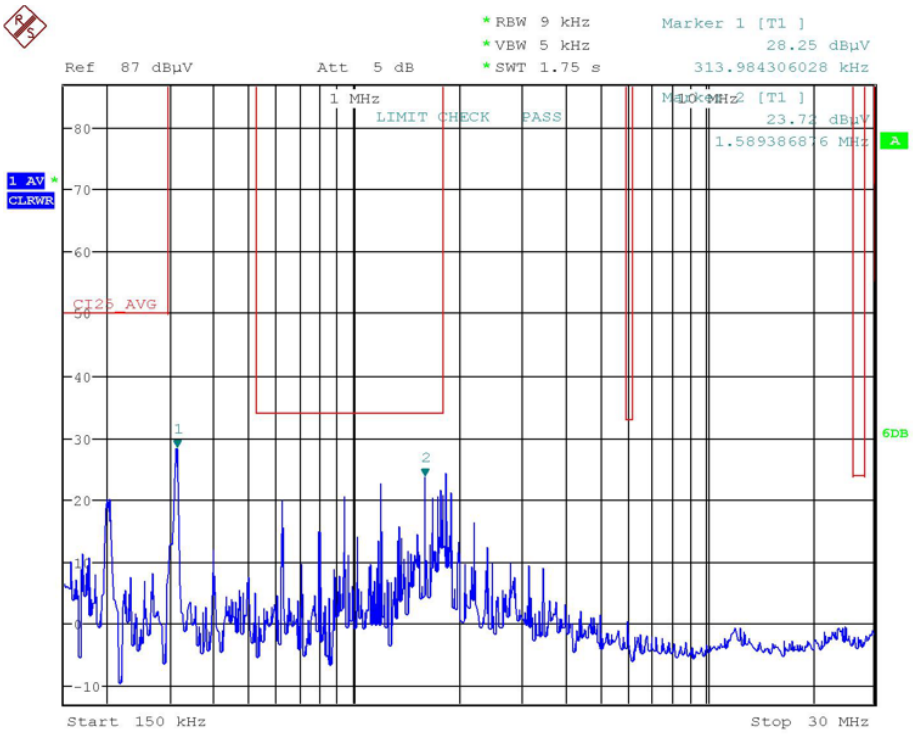


Figure 114. Measured Average Noise of Test Circuit 2 (150 kHz to 30 MHz, Limit Line: CISPR 25 Class 5 Average, Limit Check: Pass)

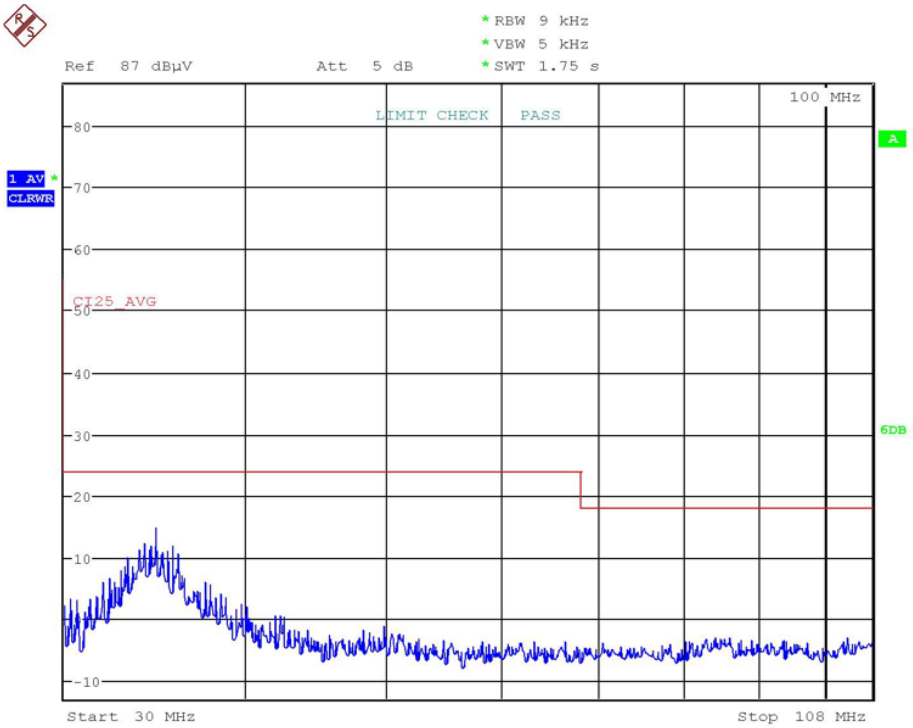


Figure 115. Measured Average Noise of Test Circuit 2 (30 to 108 MHz, Limit Line: CISPR 25 Class 5 Average, Limit Check: Pass)

6 Design Files

6.1 Schematics

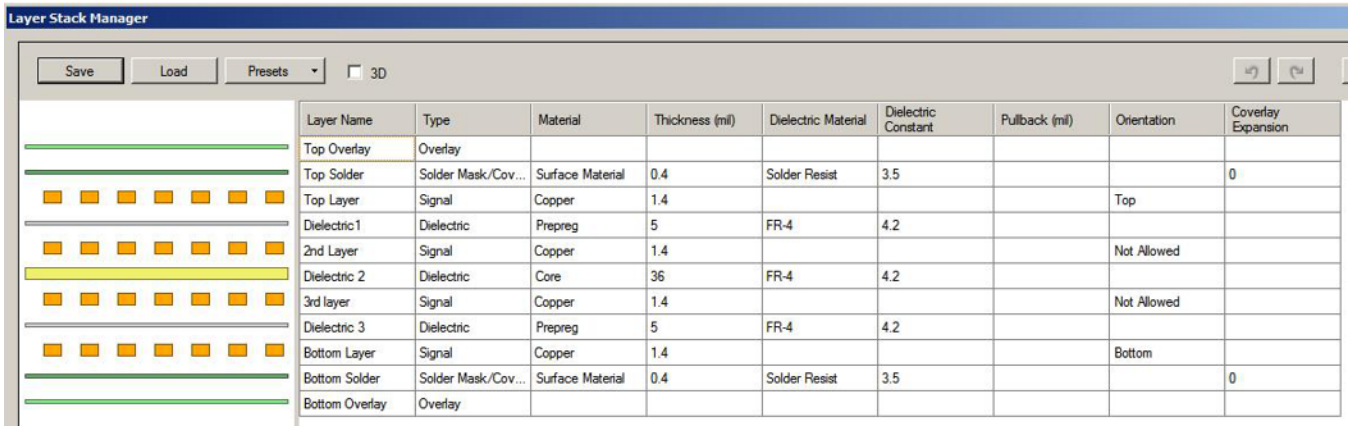
To download the schematics, see the design files at TIDA-01179.

6.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01179.

6.3 PCB Layout Recommendations

The TIDA-01179 implements a four-layer PCB. The board material, copper thickness, and the dielectric distance in between are shown in Figure 116. A 36-mil thickness dielectric is placed between the ground layer (second layer) and the third layer, where most of the switching nodes are placed. The aim is to minimize the noise couplings.



Layer Name	Type	Material	Thickness (mil)	Dielectric Material	Dielectric Constant	Pullback (mil)	Orientation	Coverlay Expansion
Top Overlay	Overlay							
Top Solder	Solder Mask/Cov...	Surface Material	0.4	Solder Resist	3.5			0
Top Layer	Signal	Copper	1.4				Top	
Dielectric1	Dielectric	Prepreg	5	FR-4	4.2			
2nd Layer	Signal	Copper	1.4				Not Allowed	
Dielectric 2	Dielectric	Core	36	FR-4	4.2			
3rd layer	Signal	Copper	1.4				Not Allowed	
Dielectric 3	Dielectric	Prepreg	5	FR-4	4.2			
Bottom Layer	Signal	Copper	1.4				Bottom	
Bottom Solder	Solder Mask/Cov...	Surface Material	0.4	Solder Resist	3.5			0
Bottom Overlay	Overlay							

Figure 116. Layer Stack of TIDA-01179

Figure 117 shows the placement of the input capacitors of the buck-boost converter. They are placed as close as possible to the chip.

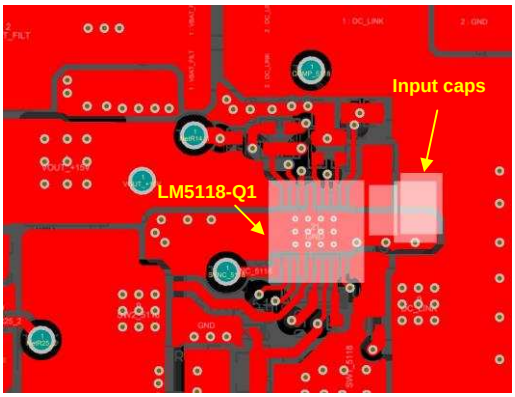


Figure 117. Place Input Capacitors Close to Buck-Boost Controller

Figure 118 shows the placement of the input MOSFETs of the buck-boost converter. They are placed as close as possible to the chip in order to ensure reliable turn-on and turn-off of the power transistors.

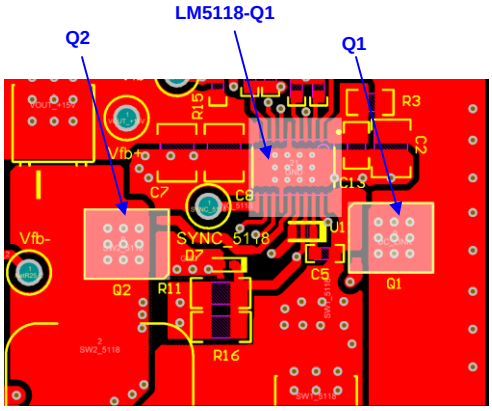


Figure 118. Place MOSFETs Close to Buck-Boost Controller

Figure 119 shows the switching loop when the LM5118-Q1 works in buck mode. The loop consists of the input capacitors, MOSFET Q1, freewheeling diode D3, and the current sensing resistor R9.

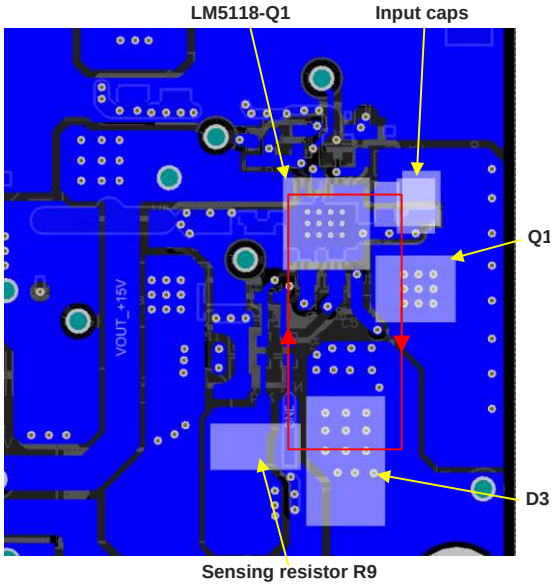


Figure 119. Buck Switching Loop of LM5118-Q1

Figure 120 shows the switching loop when the LM5118-Q1 works in boost mode. The loop consists of the output capacitors, MOSFET Q2, and the boost diode D1.

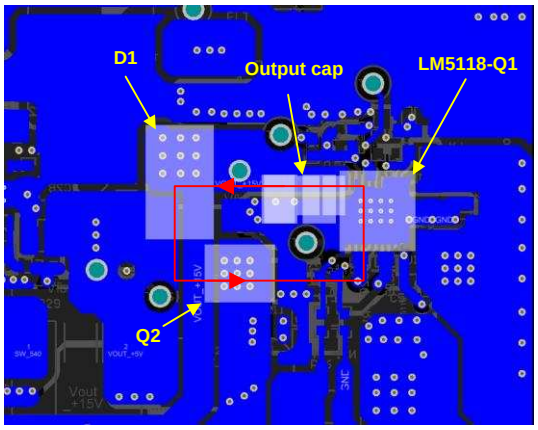


Figure 120. Boost Switching Loop of LM5118-Q1

Figure 121 shows the placement of the input capacitors of the buck converter. They are placed as close as possible to the chip.

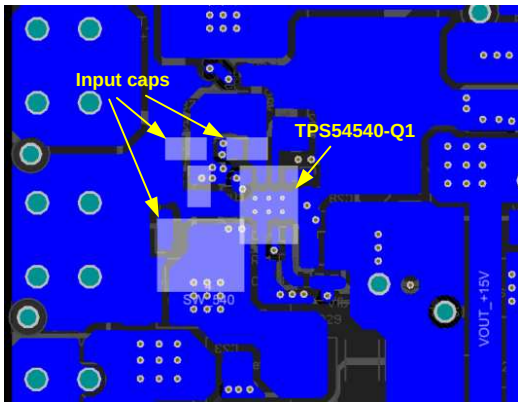


Figure 121. Place Input Capacitors Close to Buck Converter

Figure 122 shows the placement of the output capacitors of the buck converter. They are placed as close as possible to the chip.

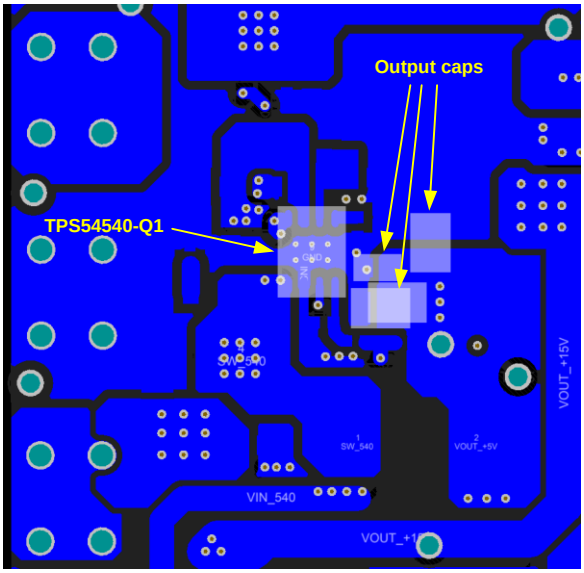


Figure 122. Place Output Capacitors Close to Buck Converter

Figure 123 shows the placement of the components in the LM5118-Q1 compensation network. They are placed away from the switching node. Their underneath is shielded by the ground plane. The aim is to minimize the noise couplings into the compensation so that the buck-boost converter is maintained stable.

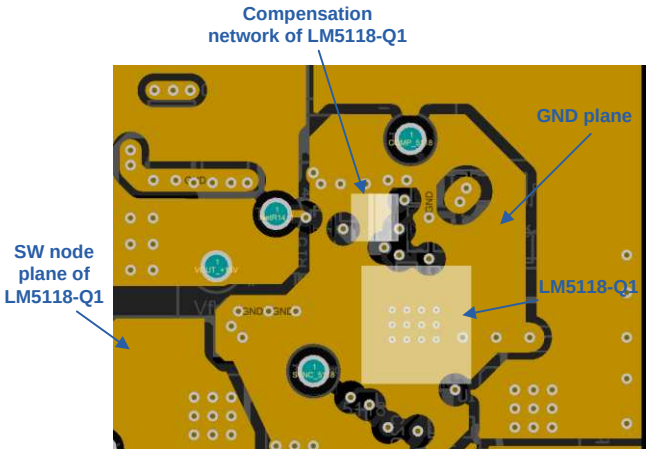


Figure 123. Place Compensation Network Close to Controller and Away From Any Switch Node

Figure 124 shows the placement of the components in the TPS54540-Q1 compensation network. They are placed away from the switching node. Their underneath is shielded by the ground plane. The aim is to minimize the noise couplings into the compensation so that the buck converter is maintained stable.

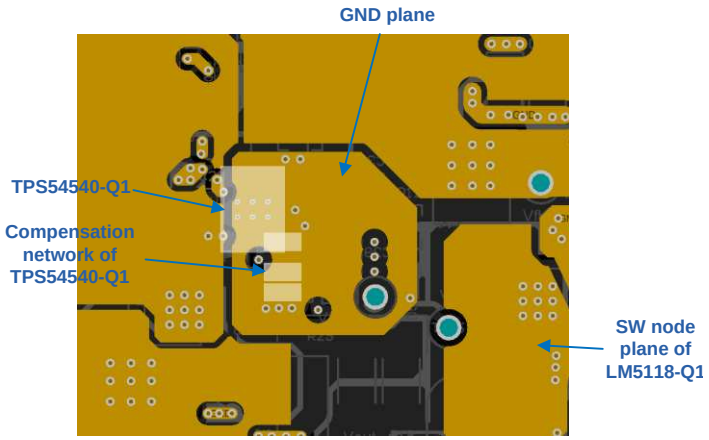


Figure 124. Place Compensation Network Close to Controller and Away From Any Switch Node

Figure 125 shows the placement of thermal vias surrounding the diode D3. Heat dissipation for this component is important for this design. The power losses onto D3 are significant due to the large peak current and relatively large forward voltage comparing to a MOSFET.

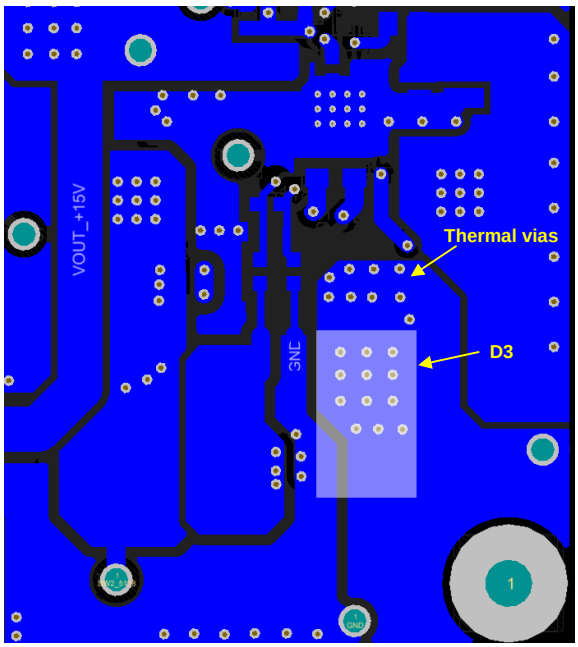


Figure 125. Thermal Vias Placement for Increased Cooling of Schottky Diode D3

6.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-01179.

6.4 Altium Project

To download the Altium project files, see the design files at TIDA-01179.

6.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01179.

6.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01179.

7 References

1. Texas Instruments, *AN-2162 Simple Success With Conducted EMI From DC-DC Converters*, Application Report (SNVA489)
2. Texas Instruments, *AN-2155 Layout Tips for EMI Reduction in DC / DC Converters*, Application Report (SNVA638)
3. TDK Corporation, *Common Mode Filters For automotive power line ACM-V Series*, ACM9070-701-2PL-TL01 Datasheet (PDF)
4. Texas Instruments, *LM5118/LM25118 Quick Start Component Calculator*, Software (SNVU065)
5. Texas Instruments, *TPS54360 and TPS54361 Family Design Excel Tool*, Software (SLVC452)
6. CISPR 25: *Limits and methods of measurement of radio disturbance characteristics for protection of receivers used on board vehicles*, Second edition 2002-08, IEC.
7. ISO7637-2: *Road vehicles — Electrical disturbances from conduction and coupling — Part 2: Electrical transient conduction along supply lines only*
8. ISO16750-2: *Road vehicles — Environmental conditions and testing for electrical and electronic equipment*

8 Terminology

AFE— Analog front-end

AEC— Automotive electronics council

ESR— Equivalent series resistance

EMI— Electromagnetic interference

EMC— Electromagnetic compatibility

DM— Differential mode

CM— Common mode

UVLO— Undervoltage lockout

MOSFET— Metal oxide semiconductor field effect transistor

CISPR— International special committee on radio interference

PE— Protective earth

ISO— International organization for standardization

BOM— Bill of material

OEM— Original equipment manufacturer

AN— Artificial network

LISN— Line impedance stabilization network

EUT— Equipment under test

PCB— Printed circuit board

HEV— Hybrid electric vehicle

EV— Electric vehicle

9 About the Author

XUN GONG is an automotive systems engineer at Texas Instruments, where he is responsible for developing reference design solutions for the automotive segment in Power Train applications. Xun brings to this role his extensive experience in IGBT gate drivers, Silicon Carbide (SiC) transistor gate drivers, IGBT temp sensing, EMC in motor drive applications, and DC-DC converters. Xun achieved his Ph.D. in electrical engineering from Delft University of Technology in Delft, Netherlands. Xun Gong won the First Prize Paper Award of the IEEE Transactions on Power Electronics in 2014.

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