TI Designs

20-Series Battery Management Module Reference Design

Description

High serial cell count battery (> 15 s) systems are becoming more and more common for industrial applications. These applications are cost sensitive and require a simple solution that includes monitoring, protection, and control or even SOC information rather than only basic independent hardware protection. A platform for such complete pack side solution is proposed in this design.

Resources

TIDA-01093	Design Folder
bq76930	Product Folder
MSP430G2955	Product Folder
LM25018	Product Folder
ISO1541	Product Folder
ISO1050	Product Folder

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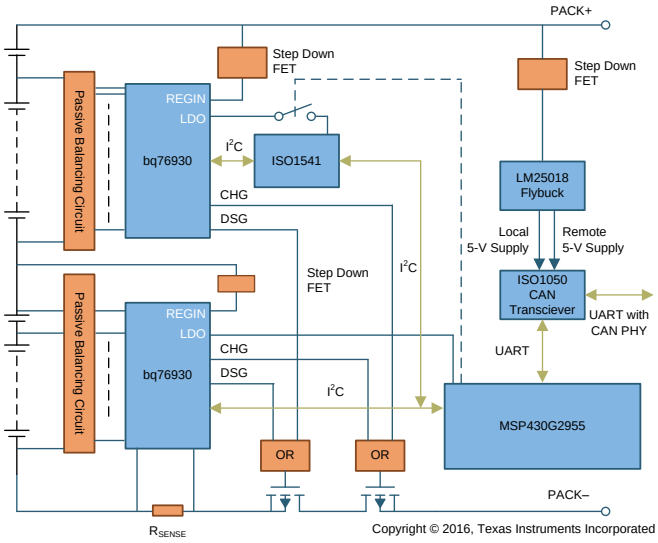
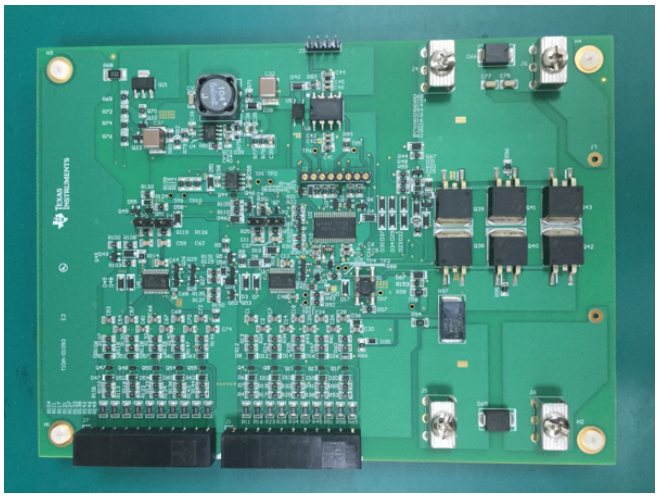
Features

- Supports 16-Series to 20-Series Cell Application
- All Independent Hardware Protecting Function Inherited From bq76930
- Charger Insertion Detectable
- Load Removal Detectable
- Isolated Differentiated CAN PHY for Communication With Host System
- Supports up to 128k Baud Rate UART Communication With External Host
- External Cell Balancing Available
- Programmable and Independent Hardware Protection for OV, UV, OCD, SCD Protection

Applications

- Power and Garden Tool
- LEVs: EBike, Scooters, Pedelec, and Pedal-Assist Bicycles
- ESS and UPS





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1 System Overview

1.1 System Description

This design incorporates two bq76930 devices and one MCU MSP430G2955 to monitor 16 to 20 cells connected in series, with the typical overall battery stack voltage ranges from 50 V (2.5 V for each cell) to 84 V (4.2 V for each cell). The MCU communicates with each bq76930 with multiplexed I^2C buses alternately. An I^2C isolator ISO1541 is used for the MCU to access the upper bq76930. The MCU can also act as a slave device to respond the access from external host with isolated differentiated CAN PHY, facilitated with ISO1050 and its internal UART module. A Fly-Buck™ DC-DC controller is used to provide two isolated power rails to the ISO1050. The FETs control signals from each bq76930 are synthesized with the OR circuits in Figure 1 to control charge and discharge FETs, respectively. All independent hardware controlled protect functions are inherited from the bq76930.

1.1.1 bq76930

The bq76930 supports 6- to 10-series cell battery pack, a variety of battery chemistries including lithium ion, lithium iron phosphate, and more may be managed by this device. Through I^2C, a host controller can use the bq769x0 to implement many battery pack management functions, such as monitoring (cell voltages, pack current, pack temperatures), protection (controlling charge or discharge FETs), and balancing. Integrated ADCs enable a purely digital readout of critical system parameters, with calibration handled in TI's manufacturing process.

1.1.2 MSP430G2955

The MSP430G2955 series is an ultra-low-power mixed signal microcontroller with built-in 16-bit timers, up to 32 I/O touch-sense-enabled pins, a versatile analog comparator, and built-in communication capability using the universal serial communication interface. For detail configurations, see Table 1.

Table 1. MSP430G2955 Configurations

DEVICE	BSL	EEM	FLASH (KB)	RAM (B)	TIMER_A TIMER_B	COMP_A+ CHANNELS	ADC10 CHANNELS	USCI_A0 USCI_B0	CLOCK	I/O	PACKAGE TYPE
MSP430G2955IDA38	1	1	56	4096	2xTA3 1xTB3	8	12	1	HF, LF, DCO, VLO	32	38-TSSOP

1.1.3 ISO1541

The ISO1451 is a lower power, bidirectional isolator that is compatible with I^2C interfaces, the device has its logic input and output buffers separated by TI's capacitive isolation technology using a silicon dioxide barrier. When used with isolated power supplies, this device blocks high voltages, isolates grounds, and prevents noise currents from entering the local ground and interfering with or damaging sensitive circuitry. The ISO1541 has a bidirectional data and a unidirectional clock channel, which is suitable for a single master system.

1.1.4 ISO1050

The ISO1050 is a galvanically isolated CAN transceiver that meets the specification of the ISO11898-2 standard. The device has the input and output logical buffers separated by silicon oxide insulation barrier that provides galvanic isolation of up to 2500 V_{RMS} for the ISO1050DUB. Used in conjunction with isolated power supplies, the device prevents noise current on a data bus or other circuits from entering the local ground and interfering with or damaging sensitive circuitry.

As a CAN transceiver, the device provides differential transmit capability to the bus and differential receiver capability to a CAN controller at signaling up to 1 Mb per second. The device is designed for operation especially in harsh environments, and it features cross-wire, overvoltage, and loss of ground protection from –27 to 40 V and over temperature shutdown, as well as –12 to 12 V common-mode range.

1.1.5 LM25018

The LM25018 is a 48-V, 325-mA synchronous step-down voltage regulator with integrated high-side and low-side MOSFETs. The constant on-time (COT) control scheme employed in the LM25018 requires no loop compensation, provides excellent transient response, and enables very high step-down ratios. The on-time varies inversely with the input voltage, resulting in nearly constant frequency over the input voltage range. A high-voltage startup regulator provides bias power for internal operation of the IC and for integrated gate drivers.

1.2 Key System Specifications

Table 2. Key System Specifications

PARAMETER	SPECIFICATION	
Cell series number	16 to 20 s	
Max stack voltage	144 V	
Consumption current	Shutdown	0.6 µA typical
	Normal (MCU in LPM3, bq76930 ADC on, bq76930 CC off)	60 µA typical
	Normal (MCU on, bq76930 ADC on, bq76930 CC on)	4.5 mA typical
	Communication with host	17.5 mA typical
Balancing current	40 mA typical	
Additional FETs shutdown delay caused by the OR circuits in block diagram	Discharge	48.6 µs typical
	Charge	372.4 µs typical
Support baud rate	38.4 to 128 kb/s	
Minimum gap between PACK– and BAT– for charger detection	2 V	
Load detect removal delay	≈ 408.1 s (Stack voltage = 80 V)	

1.3 Block Diagram

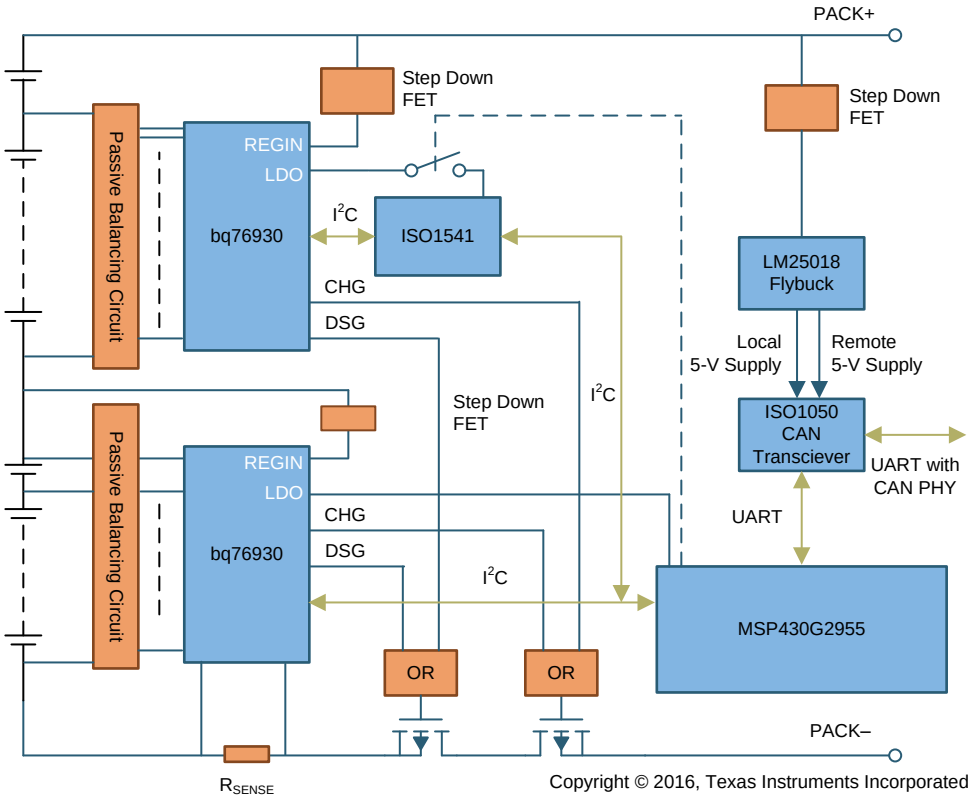

Figure 1. TIDA-01093 Block Diagram

1.4 Highlighted Products

1.4.1 bq76930

Figure 2 shows the function block diagram of the bq76930.

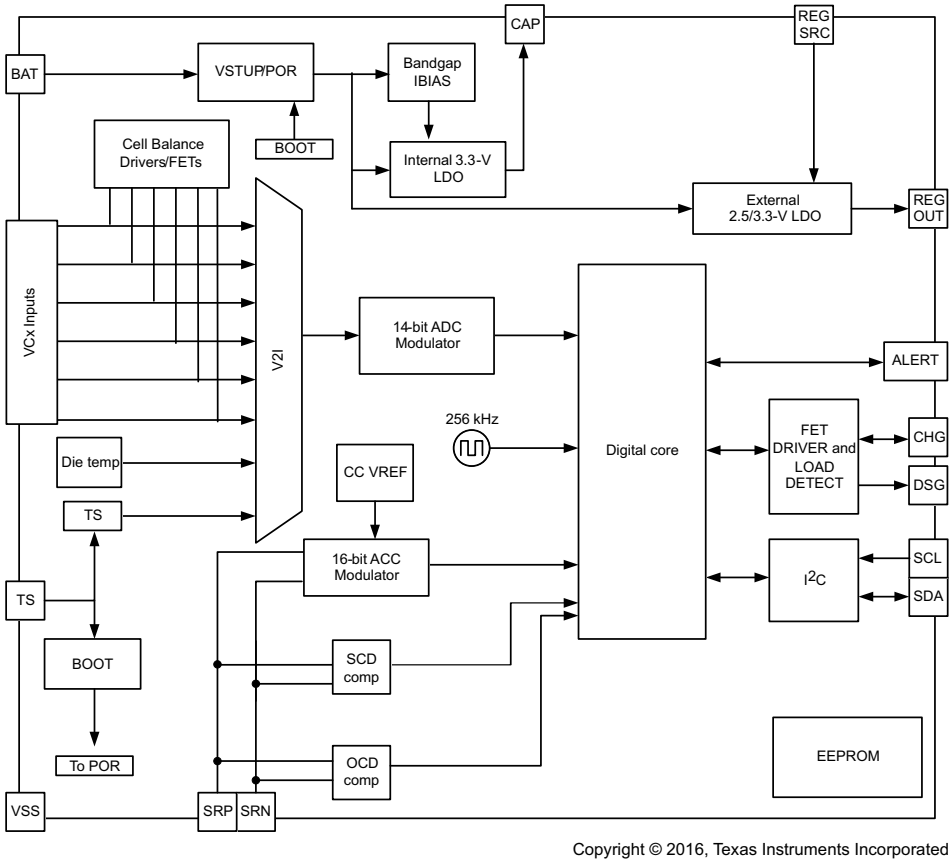

Figure 2. bq76930 Function Block Diagram

Features:

- AFE monitoring features
  - Pure digital interface
  - Internal ADC measures cell voltage, die temperature, and external thermistor
  - A separate, internal ADC measures pack current (coulomb counter)
  - Directly supports up to three thermistors (103AT)
- Hardware protection features
  - Overcurrent in discharge (OCD)
  - Short circuit in discharge (SCD)
  - Overvoltage (OV)
  - Undervoltage (UV)
  - Secondary protector fault detection
- Additional Features
  - Integrated cell balancing FETs
  - Charge, discharge low-side NCH FET drivers
  - Alert interrupt to host microcontroller
  - 2.5-V or 3.3-V output voltage regulator
  - No EEPROM programming necessary
  - High supply voltage abs max (up to 108 V)
  - Simple I^2C compatible interface (CRC option)
  - Random cell connection tolerant

2 System Design Theory

2.1 FETs Control Synthesizing Circuit

In this TI Design, two bq76930 devices are used for monitoring the 20 cells connected in series, one device for monitoring lower 10 cells in series, and another for the upper 10 cells in series, The bottom device references to BAT–, which is the negative end of the first cell (the lowest cell at the bottom of the cell stack) as its ground, and the upper device references the point of positive end of the 10th cell or negative end of the 11th cell as its ground, so these two devices work at different reference potentials. The output FET control signals of DSG and CHG of the upper device needs have the level shifted so that these two signals can be ORed as inverted logic to control the charge and discharge FETs. The FETs of Q26 to Q32 in Figure 3 implemented the shifted OR function for FETs control signals.

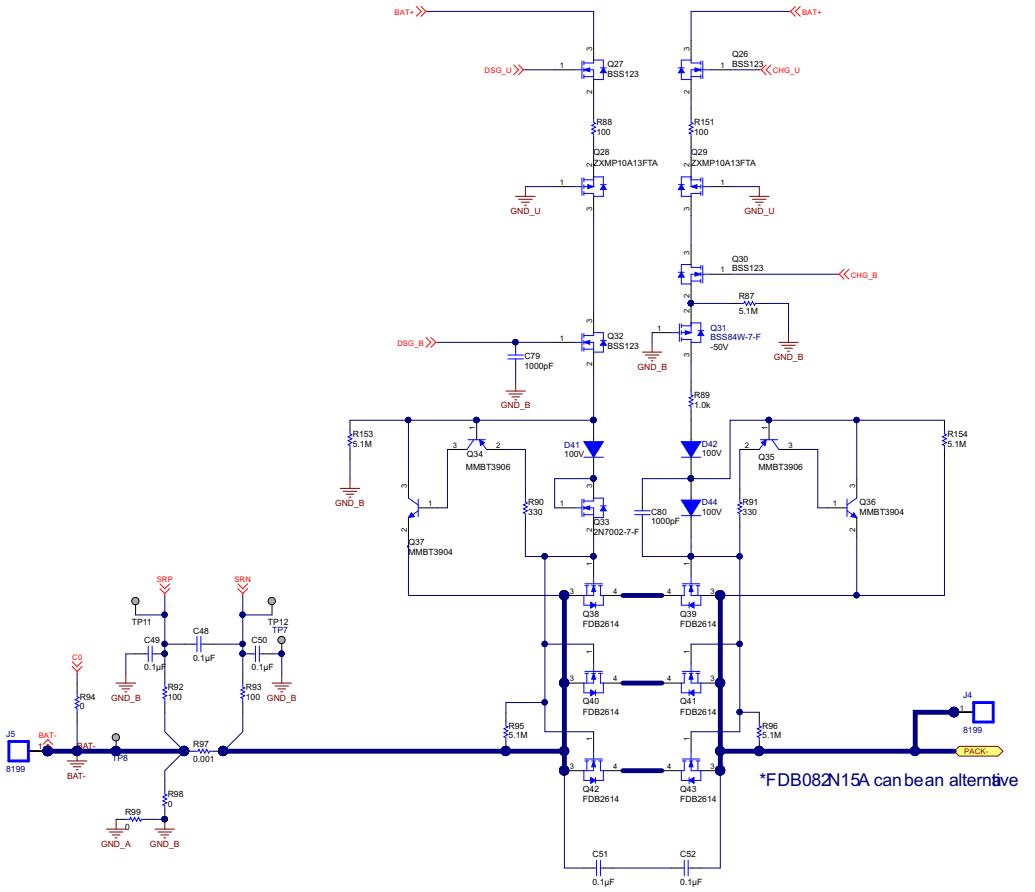

Figure 3. FETs Control Signal Schematic

There two paths of the control signals in above circuit, one for discharge FETs control and another for charge FETs control. They are designed with the same idea. The path for discharge FETs control signal would be used for interpretation in the following section.

Given that the voltage at BAT+ in Figure 3 is 80 V, and both DSG outputs of upper and bottom devices assert upon initializing with no fault detected. With the DSG output of upper device labeled as DSG_U asserts, the voltage of DSG_U to the ground reference GND_U for upper device would be ≈ 12 V; because the ground reference of the upper device is in the middle of battery stack, the voltage between GND_U and GND_B is ≈ 40 V, as the GND_B is the ground reference of the bottom device. Then the voltage of DSG_U to the GND_B is ≈ 52 V, with the typical $V_{GS(TH)}$ of Q27 being about 1.7 V; the voltage at

the source of Q27 is about 52 V – 1.7 V = 50.3 V. With this voltage at the source of FET Q28, this FET is on, and the voltage at Q32 drain is also 50.3 V. With DSG_B asserts at ≈ 12 V to GND_B, the voltage at source of Q32 is also clamped at ≈ 10.3 V, subtracting the forward voltage of D41 and V_{GS} of Q33 summed at 2.6 V, the voltage at the gates of Q38, Q40, and Q42 is about 7.7 V, thus the DSG FETs are all turned on.

If the DSG output of bottom device deasserts, then the DSG_B would be ≈ 0 V, and the source of Q32 would be 0 V. This turns off all discharge FETs.

If the DSG output of the upper device deasserts, then FETs Q27 and Q28 are turned off, and the voltage at the drain of Q28 drops to 0 V. This also turns off all discharge FETs.

When the voltage at the Q32 source starts to drop either caused by deassertion of the upper or bottom devices' DSG outputs, it drops slowly if there is no additional pulldown circuit. Q34, Q37, D41, and D43 constitute an expedite shutdown circuit so that the voltage at the gates of the discharges FETs drops quickly.

2.2 Charger Detection Circuit

Like most of the battery packs, the charger connection to the charge input end between PACK+ and PACK– in this design must be sensed by the system either when the charge FETs are open or closed. The purposes of this are for fault detection, fault recovery, system activation from shutdown mode, and coulomb counting if SOC information is required. When charge FETs are closed, the charge current can be sensed by the bq76930 and the MCU. If the charge current is too low to be sensed, charger detection is typically not required in most application scenarios. As for a 20s battery, charging is almost always terminated either by full charge detection or OV conditions; for both scenarios, the charge FETs cut off the charge current before the charge current tapers to 0 V.

When the charge FETs are open, there should be a voltage gap between charger output and battery stack side because the charge FETs are always cut off before the current tapers to 0 V. The charger detection circuit senses this voltage as the measure to detect the charger presence. Figure 4 is the schematic of this circuit.

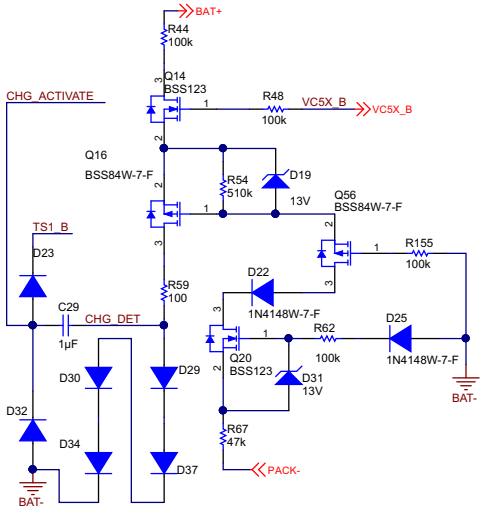

Figure 4. Charger Detection Circuit Schematic

For a 20-series lithium ion cell battery, the charger voltage is typically designed with a constant output voltage at 84 V; however, given that the relaxed battery stack voltage is 80 V, and the charge FETs are open due to full charge detection, OV fault, or bq76930 device being shutdown, when the charger presented to PACK+ and PACK–, the voltage between PACK– and BAT– is about –4 V. The typical $V_{GS(TH)}$ is about 1.7 V, the voltage across R67 would be 2.3 V, and the voltage across R54 would be clamped by D19. Then Q16 is turned on, and the voltage at Q14 source would be clamped at about 18.3 V if the

VC5X_B is 20 V. R59 limits the current flow through the diodes D29, D37, D30, and D34, which develop a voltage at about 2.7 to 2.8 V at the point with the net label of CHG_DET. This voltage would also generate a rising edge at TS1_B, which is directed to the TS1 pin of the bottom bq76930. With the rising edge occurring at the TS1 pin, the bottom device is waken up if it is previously in shutdown state. The MCU can also sense this event by monitoring the voltage CHG_DET.

D23 and C29 is used to isolate the temperature measurement circuitry at the TS1 pin. With these two devices in place, the pulse occurs at TS1 pin for temperature measurement will not be distorted most of the time except for the moment when a charger connects to the PACK+ and PACK– or the button S1 is pressed down.

The signal CHG_ACTIVATE is used to propagate itself to the upper device through the circuit in Figure 5.

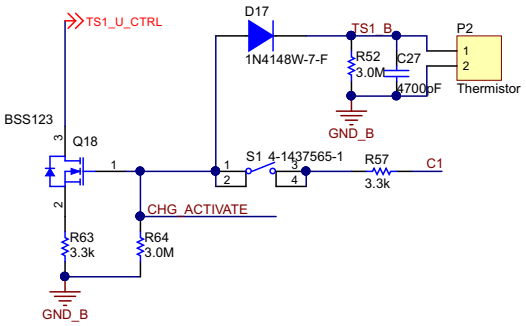

Figure 5. Activate Circuit for Bottom and Top Device Schematic

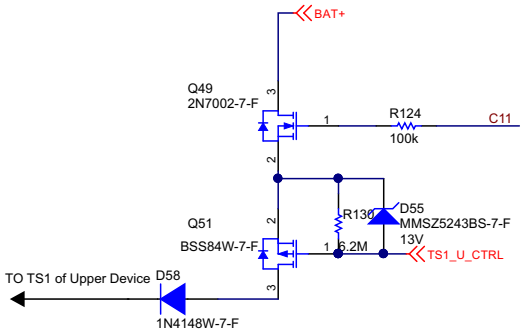

Figure 6. Activate Circuit of Upper Device Schematic

In Figure 5, the CHG_ACTIVATE signal turns on Q18 when charger presents, according the test result, the voltage at the gate of Q18 jumps up to 2.7 V then tapers down exponentially to 0 V with the time constant of C29 × R64, which is 3 s. Assuming the $V_{GS(TH)}$ of Q18 is 1.7 V, thus a pulling down current is created by R63, the peak of pulling down current is about (2.7 V – 1.7 V) / 3.3K ≅ 0.3 mA; this current is enough to clamp the voltage across R130 at about 13 V. Q51 is turned on, then the voltage at source of Q49 presents at TS1 of the upper bq76930, and gets this device waken up accordingly.

From Figure 5 and Figure 6, pressing the button can also activate both bq76930 devices. The signals C1 and C11 are from the positive end of 1st cell and 11th cell in the battery pack counting up from the bottom of the stack.

2.3 Load Removal Detection Circuit

Load removal detection is also a basic function for a battery pack. The major purpose of such function is for short-circuit discharge fault recovery. Without a load removal detection circuit, the battery system has to turn on the FET very briefly to see if the short persists, or simply never recover until a charger is detected. But the latter solution is not feasible in some application, like a light electric vehicle system. The circuit in Figure 7 works for this purpose.

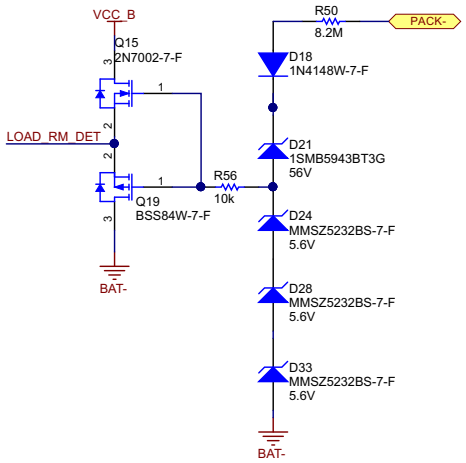

Figure 7. Load Removal Detection Circuit Schematic

The major challenge for such a circuit is that the battery has to present very high impedance at its output between PACK+ and PACK– when short protection for discharge (SCD) is detected and DSG FETs are open. The circuit in Figure 7 makes a path with very high impedance between BAT– and PACK–, thus the leakage current is very low when the shorted load persists at pack output.

In Figure 7, when the SCD is not detected, PACK– and BAT– are bypassed with a path with very low impedance, which is made up of Q38 to Q43 and R97 in Figure 3. The voltage at Q15 and Q19 gates is low, and the signal LOAD_RM_DETECT is low. This signal is sensed by the MCU. When SCD protection occurs, Q38 to Q43 are open. A voltage will be developed at the gates of Q15 and Q19; this voltage turns on the Q19 and turns off Q15, and the signal LOAD_RM_DETECT goes high. When the load is removed, the voltage at the gates of Q15 and Q19 tapers to 0, and the signal LOAD_RM_DET signal drops accordingly, thus the load removal event can then be detected by the MCU.

Table 6 logs the data for a load removal test under various battery stack voltages when the charge and discharge FETs are all open. The column of V_{BAT} logs the battery stack voltages, $I_{LEAKAGE}$ logs the leakage current between PACK+ and PACK– when the Q38 to Q43 are open, V_{PACK} logs the voltage between PACK+ and PACK– when the short is removed, and V_{LOAD} is the voltage measured at signal LOAD_RM_DET. T_{DELAY} is the time from the moment when the load is removed to the next moment when the voltage V_{LOAD} goes to the voltage below 0.5 V again.

2.4 I²C Communication Between MCU and AFEs

In this TI Design, the two bq76930 devices reference to different ground potentials. One device references to the same ground with the MCU, another references to the ground at the middle of the battery stack. The I²C bus has to be multiplexed so that the MCU can talk with two bq76930 devices with no bus conflicts.

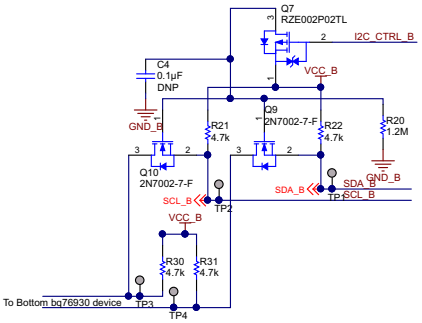

Figure 8. I²C Communication Between MCU and Bottom bq76930 Device

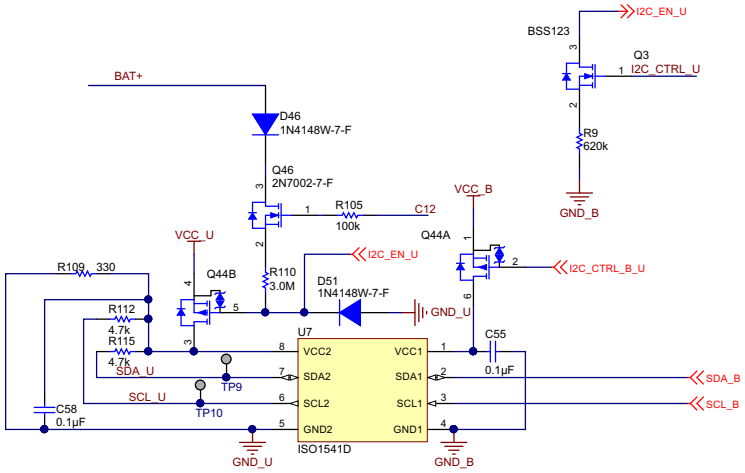

Figure 9. I²C Communication Between MCU and Upper bq76930 Device

The circuits in Figure 8 and Figure 9 are for duplex I²C communication between the MCU and two bq76930 devices at different ground references.

Figure 8 is for I²C communication between the MCU and the bottom bq76930, when MCU is to sponsor an I²C transaction with the bottom AFE, the I2C_CTRL_B signal is set low, I2C_CTRL_B_U is set high, and I2C_CTRL_U is set low so that the signal I2C_EN_U can be pulled high. Q44A and Q44B are turned off, which disables VCC1 and VCC2 supplies of U7. With I2C_CTRL_B being low, the Q7 is on, and Q9 and Q10 are both turned on. By such configuration of signals I2C_CTRL_B, I2C_CTRL_B_U, and I2C_CTRL_U from the MCU, the MCU sees high impedance on SDA_B and SCL_B to the upper bq76930 and all I²C transactions are directed to the bottom bq76930.

Figure 9 is for I²C communication between the MCU and the upper bq76930 device, when the MCU is to sponsor an I²C transaction with the upper AFE, the I2C_CTRL_B signal is set high, I2C_CTRL_B_U is set low, and I2C_CTRL_U is set high so that the signal I2C_EN_U can be pulled down. Q44A and Q44B are turned on, which enables VCC1 and VCC2 inputs of U7. With I2C_CTRL_B being high, the Q7 is off and Q9 and Q10 are both turned off. By such configuration of signals I2C_CTRL_B, I2C_CTRL_B_U, and I2C_CTRL_U from the MCU, the MCU sees high impedance on SDA_B and SCL_B to the bottom bq76930 and all I²C transactions are directed to the upper bq76930.

2.5 Isolated Differential Communication With External Host

A CAN PHY is used for the MCU to respond to the access from external host with required battery information such as voltage, current, temperature, or even SOC. A CAN transceiver ISO1050 is used to bridge the UART interface and the differential CAN PHY. The TTL signal from the MCU UART and CAN PHY signal are transferred to each other by this device.

In Figure 10, the Fly-Buck DC-DC controlled by the LM25018 provides two isolated power rails for the ISO1050: the 5V_REMOTE rail is for the VCC2 of the CAN PHY side to the external host, and the 5-V rail is for the VCC1 of the TTL signal side with the UART interface to the MCU. The TXD signal is directly connected to the MCU, as signals from the MCU ranging from 0 to 3.3 V are recognizable to the ISO1050. However, the RXD signal from the ISO1050 is shifted to 0 to 3.3 V from the range of 0 to 5 V of the ISO1050 by Q24 and Q25. U5 is used to sense the first incoming transaction initiated by the host and notify the MCU through the signal COMM_INT. This implies that if an external host wants to communicate with the MCU, a garbage transaction needs to be sent first for notification purposes so that the system can shut down the DC-DC in most of the time when no communication is needed.

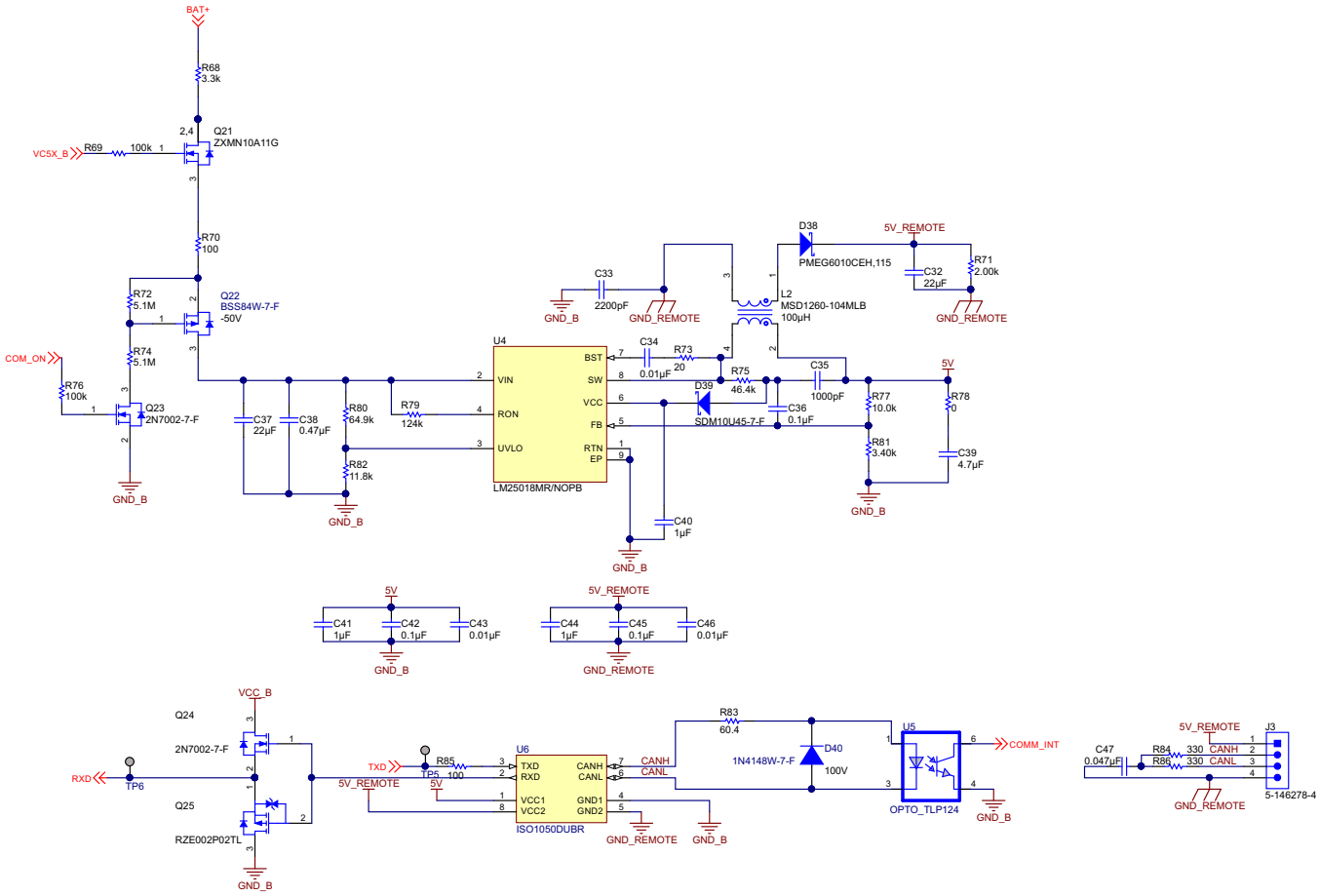

Figure 10. Isolated Differentiated Communication With External Host

3 Getting Started Hardware and Software

3.1 Hardware

To start debugging the system, a cell simulator and real cells are needed to provide power of the board, and an MSP430™ debug tool MSP-FET430UIF is needed to debug and develop firmware. Once the cells or cell simulators are connected to the module, by pressing the button S1, the LDO outputs of upper and bottom bq76930 devices are enabled and the MCU is powered up. The user can debug the system with debugging tool MSP-FET430UIF and Code Composer Studio™ (CCS) software.

3.1.1 Cell Simulator

To simulate the cell stack connected to the module, two power supplies with a maximum output above 30 V at least is needed. These two power supplies must be connected in series or at least isolated to GND terminals of the power supplies so that they can be used to simulate the 20-series cell battery stack. Two voltage dividing boards with 10 resistors connected in series to simulate each cell voltage are needed. The power supplies, 10-Series Resistor Boards, and the TIDA-01093 PCBA must be connected per the diagram in Figure 11.

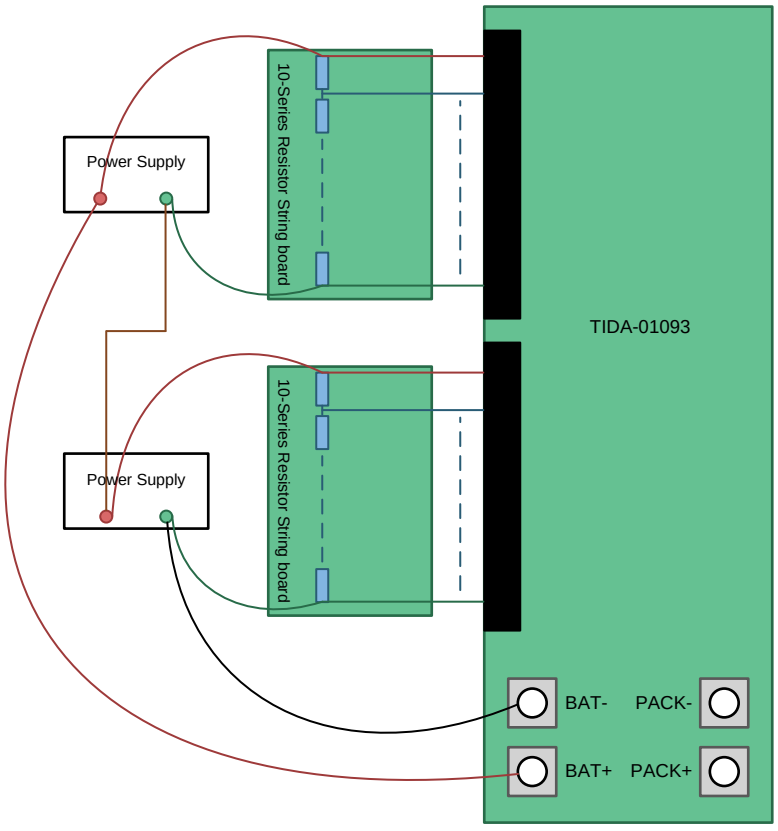

Figure 11. Debug Connecting Diagram

3.1.2 MSP430 Debug Tool

The MSP-FET430UIF is needed for hardware debugging purpose. For details, see the *MSP430 Hardware Tools User's Guide* (SLAU278).

3.2 Software

To debug and develop the firmware on the TIDA-01093 with the MSP430G2955, CCS is needed. The software can be downloaded from the website (http://processors.wiki.ti.com/index.php/Download_CCS). For how to use this software, see the *Code Composer Studio™ for MSP430™ User's Guide* (SLAU157).

4 Testing and Results

4.1 Test Setup

Six basic functions are tested for TIDA-01039 design verification. They are short circuit discharge test, charger detect test, load removal test, UART communication test, and OV and UV protections.

4.1.1 Short Circuit Discharge Test

The real 20s battery instead of a cell simulator is connected to the left side of the TIDA-01093 board with the positive end to BAT+ and the negative end to BAT–. Other wires for each monitoring cell voltage can be connected to its corresponding inputs on the TIDA-01093 board. The output of the TIDA-01093 between PACK+ and PACK– terminals is shorted when doing the test as shown in Figure 12. The basic parameters are as listed as the following:

- The voltage of the battery: 64.2 V
- The battery configuration: 20s 20AH LiFePO4 battery
- The resistance of the shorting wire applied to the PACK+ and PACK–: ≈ 2.5 mΩ

Short discharge protect configuration in U1: Register PROTECT1 (0x06) is configured at 0x30. This configures the SCD delay at 400 µs and the SCD threshold at 22 mV. A program for the MPS430 needs to be implemented for this configuration to enable the charge and discharge FETs upon the MCU's power up.

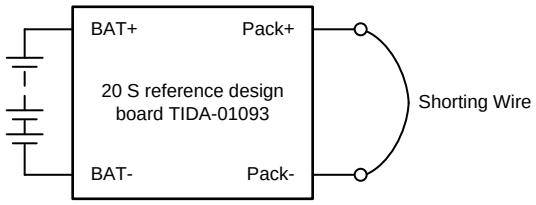

Figure 12. Short Circuit Discharge Test

4.1.2 Charger Detect Test

Two power supplies and two voltage divider resistor string boards are needed to simulate the battery stack. They are symbolized as Power Supply 1 in Figure 13. Another additional power supply is connected between PACK– and BAT–, which is symbolized as Power Supply 2 in Figure 13. Power Supply 1 is for cell simulating, and Power Supply 2 is used to simulate the gap between PACK– and BAT– when a charger is applied to PACK+ and PACK–. Power Supply 1 has to be able to provide a voltage greater than 60 V.

For each round test, Power Supply 1 turns on first. At this moment, both U1 and U8 in the TIDA-01039 schematic are not activated. The LDO outputs of both devices are off. Power Supply 2 turns on after Power Supply 1 is enabled to simulate the application of the charger between PACK+ and PACK–. If the test succeeds, the entire system will turn on and the CHG and DSG FETs will turn on accordingly. To make this happen, a simple program for the MSP430G2955 to enable the charge and discharge FETs upon the MCU's power up is needed.

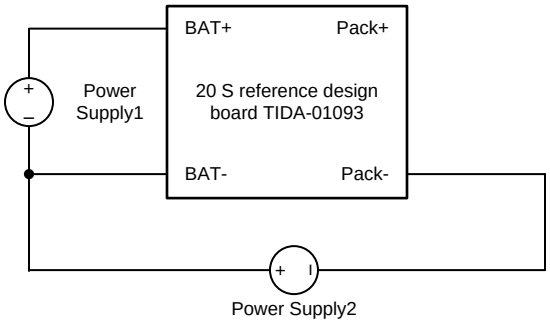

Figure 13. Charger Detect Test

4.1.3 Load Removal Test

Two power supplies and two voltage divider resistor string boards are needed to simulate the battery stack. Once the output of this power supply turns on, the system is in shutdown state, and the CHG and DSG FETs are all open. An ampere meter is connected between PACK+ and PACK– to measure the leakage current; it is also a short load connected between PACK+ and PACK–. Once this meter is removed, the load removal detect circuit should be able to detect this, and the MCU can be signaled accordingly. A simple program for the MSP430G2955 is needed to disable the charge and discharge FETs upon the MCU's power up.

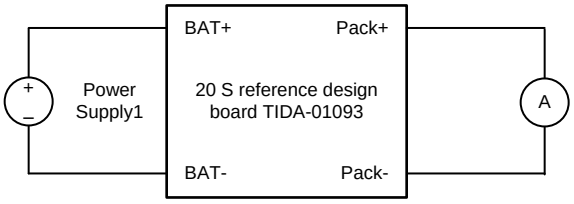

Figure 14. Load Removal Test

4.1.4 OV Protection Test

This test is done with two power supplies, two 10s serial resistor divider boards, a TIDA-01093 board, and a power supply with sourcing and sinking current capability to simulate the OV condition for the bottom and upper bq76930 devices. An oscilloscope is used to capture the relevant signals. Signals at the gates of CHG FETs, the original FET control output of the relevant device, and the voltage across the selected resistor in the resistor string simulating the OV condition with its voltage going above the OV threshold during the test are captured. The program running on the MSP430G2955 for configuring the devices with protection threshold needs to be implemented by the tester. In this test, the OV threshold is configured at 3.7 V, and the delay is configured at 1s. Figure 15 is the hardware setup diagram for this test.

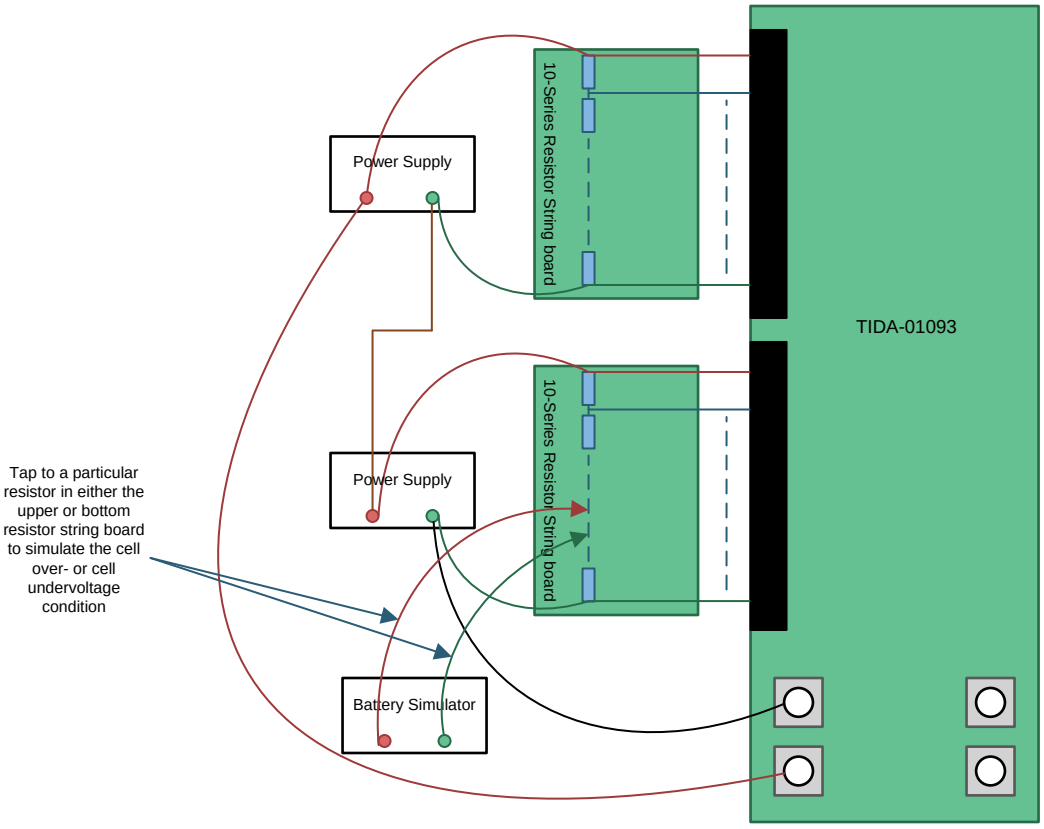

Figure 15. Cell OV or Cell UV Test Diagram

4.1.5 UV Protection Test

This test is done with two power supplies, two 10s serial resistor divider boards, a TIDA-01093 board, and a power supply with sourcing and sinking current capabilities to simulate the UV condition for the bottom and upper bq76930 devices. An oscilloscope is used to capture the relevant signals. Signals at the gates of DSG FETs, the original FET control output of the relevant device, and the voltage across the selected resistor in the resistor string simulating the UV condition with its voltage going below the UV threshold during the test are captured. The program running on the MSP430G2955 for configuring the devices with a protection threshold needs to be implemented by the tester. In this test, the UV threshold is configured at 2.5 V, and the delay is configured at 1s. Figure 15 is the hardware setup diagram for this test.

4.1.6 UART Communication Test

This test is done with a PC, two power supplies and two 10s serial resistor divider boards, an ISO1050EVM, an FTDI's USB to TTL Serial converter cable with the part number TTL-232R-5V and a TIDA-01093 board. Figure 16 is the basic connection diagram.

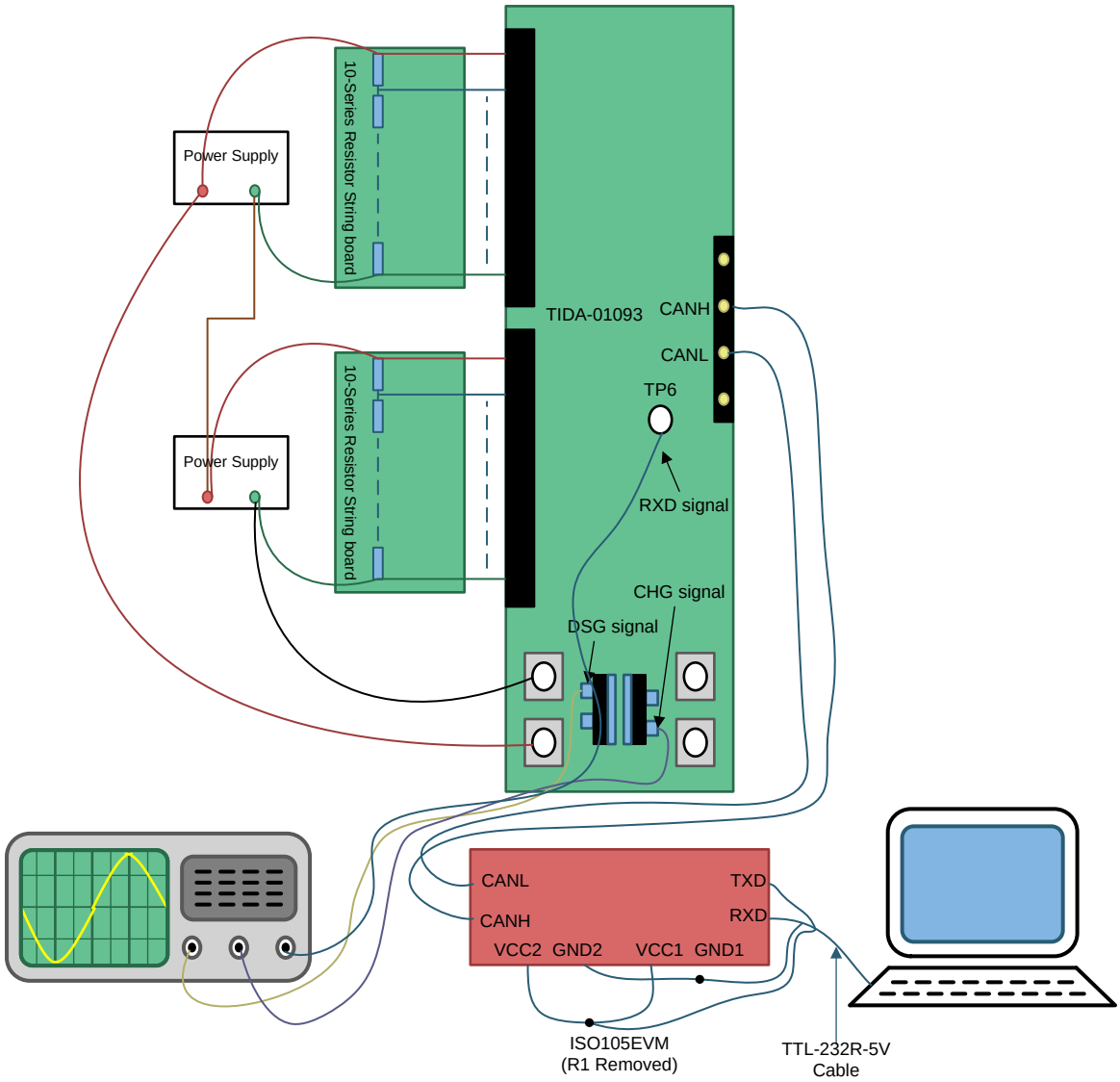

Figure 16. UART Test Diagram

The TTL-232R-5V cable provides a 5-V power supply to the ISO1050EVM, the VCC1, VCC2, GND1, and GND2 are shorted together respectively to 5 V and GND of the TTL-232R-5V cable, RXD, and TXD are also connected to the corresponding pins of the cable. For the pin assignment of the TTL-232R-5V cable, see Table 3.

Table 3. TTL-232R-5V Cable Pin Assignments

PIN NUMBER	PIN FUNCTION	MATING CABLE COLOR
1	Ground	Black
2	Not used	Brown
3	5-V input from PC	Red
4	RX from PC to ISO1050EVM	Orange
5	TX from ISO1050EVM to PC	Yellow
6	Not used	Green

The commands are sent from the PC to the TIDA-01093 through the CAN PHY from the ISO1050EVM. The UART communication is verified by sending commands to the target the TIDA-01093 to turn on and off the CHG and DSG FETs alternately to see if the FETs control signals would go high and low as expected. The UART command are received and interpreted by the MCU on the TIDA-01093 board. The MCU then sends the desired commands to each bq76930 in stack to manipulate the DSG and CHG output over the multiplexed I^2C bus. Table 4 lists the commands sent periodically in sequence.

Table 4. Commands for UART Communication

COMMAND IN SEQUENCE	COMMAND NAME	COMMAND FRAME (H STANDS FOR HEXADECIMAL)
1	UpperDsgFetOn	4AH, 02H, 03H, 01H, 06H
2	BottomDsgFetOn	4AH, 02H, 03H, 05H, 0AH
3	UpperChgFetOn	4AH, 02H, 03H, 03H, 08H
4	BottomChgFetOn	4AH, 02H, 03H, 07H, 0CH
5	UpperDsgFetOff	4AH, 02H, 03H, 02H, 07H
6	BottomDsgFetOff	4AH, 02H, 03H, 06H, 0BH
7	UpperChgFetOff	4AH, 02H, 03H, 04H, 09H
8	BottomChgFetOff	4AH, 02H, 03H, 08H, 0DH

In each command frame, the sixth byte is for command byte. Other bytes are for protocol implementation; for details of the frame structure, see the document *UART based communication protocol for intermodule communication of Light Vehicle systems*. In Section 4.2.4, the waveform of the FET gates and the command sequence are presented not only to demonstrate if the UART communication between the PC and targeted TIDA-01093 board works correctly, but also to imply if the multiplexed I^2C are working correctly. A program running on the MSP430G2955 to receive and interpret the command sent by the PC and perform corresponding operations to control the FETs needs to be implemented by the tester. The command frame structure used here is only for demonstration. Such commands can also be defined in different way.

4.2 Test Data

4.2.1 Short Circuit Discharge Test

4.2.1.1 Captured Plot

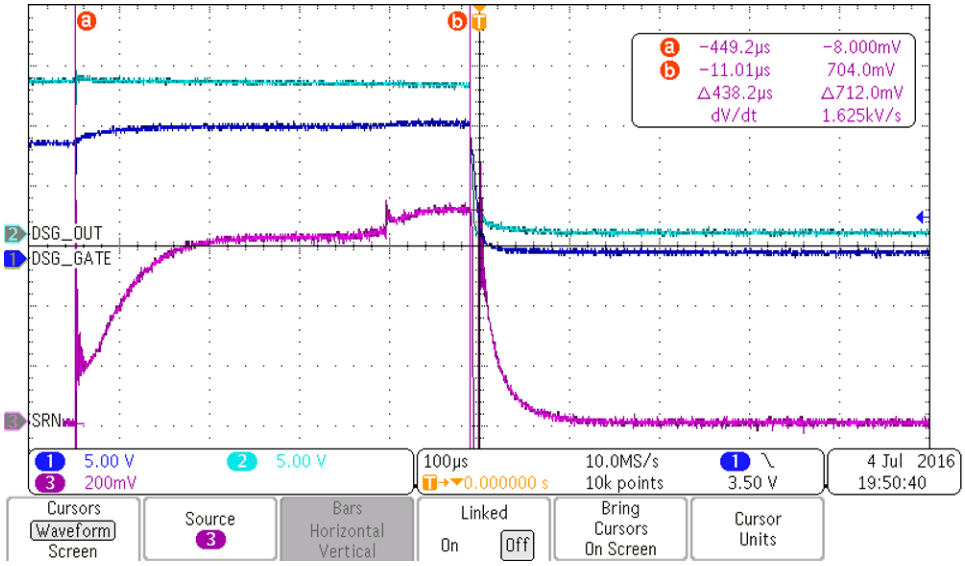

Figure 17. Short Circuit Discharge Test Captured Plot

Signal definition:

- Channel 1: The signal at the gates of DSG FETs Q38, Q40, and Q42
- Channel 2: The signal at DSG(Pin1) output of U1 (light blue) in the schematic of the TIDA-01093
- Channel 3: The signal at SRN(Pin 29), test point TP12 in the schematic of the TIDA-01093

4.2.1.2 Conclusion

These tests indicate the short-circuit protection test as successful. The current corresponding to the Channel 3 signal is cut off when the DSG output of U1 drops to 0. The current ramps up and is cut off at 700 A when protection is triggered. The 438.2-µs delay time also conforms to the delay configuration.

4.2.2 Charger Detect Test

4.2.2.1 Test Data

Data in Table 5 are monitored during the charger detect test:

- VBAT: Voltage between BAT+ and BAT–
- VGAP: Voltage between BAT– and PACK–
- VCHG_DET: Voltage at the point with the net label of CHG_DET in the TIDA-01093 schematic
- VTS1_B_r: Voltage at the point with the net label of TS1_B at the moment right after the rising edge of the pulse
- VTS1_B_f: Voltage at the point with the net label of TS1_B at the moment right before the falling edge of the pulse
- TDSG_r: The time from the rising edge of VCHG_DET to the rising edge of DSG signal
- TDET_f: The time between the rising edge and falling edge of VCHG_DET

Table 5. Charger Detect Test Data

VBAT (V)	VGAP (V)	VCHG_DET (V)	VTS1_B_r (V)	VTS1_B_f (V)	TDSG_r (ms)	TDET_f (ms)
60	24	2.238	2.081	1.885	91.09	126.2
	20	2.234	2.081	1.817	91.09	126.2
	10	2.235	2.087	1.801	91.09	126.2
	5	2.235	2.079	1.896	91.09	126.2
	2	2.235	2.088	1.816	91.09	126.2
50	2	2.236	2.036	1.879	93.23	131.2
	5	2.235	2.055	1.803	93.23	131.2
	10	2.243	2.052	1.803	93.23	131.2
	20	2.243	2.057	1.814	93.23	131.2
	30	2.253	2.053	1.821	93.23	131.2
	34	2.244	2.065	1.889	93.23	131.2
82	2	2.245	2.160	1.860	91.09	125.6
	5	2.240	2.160	1.860	91.09	125.6

Figure 18 is the typical captured plot for this test.

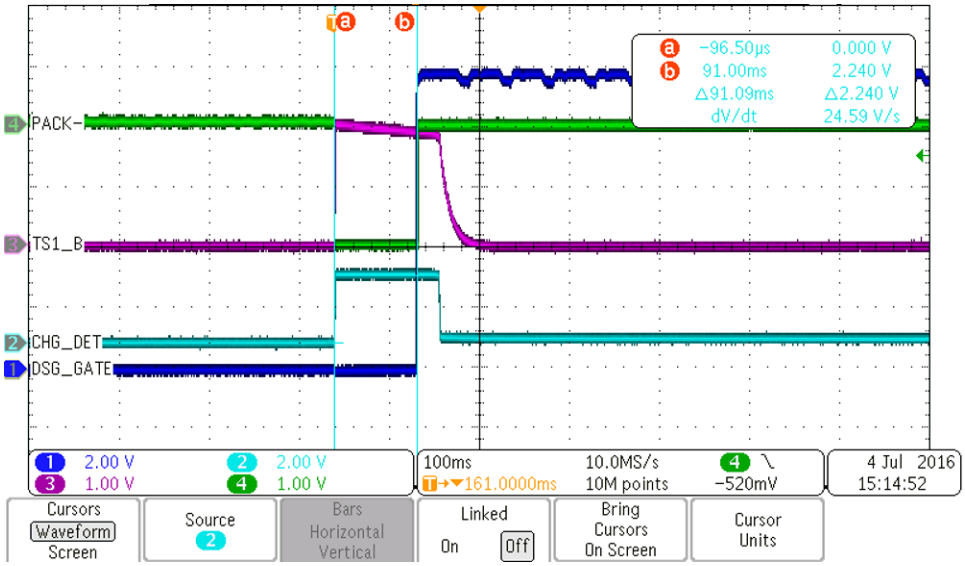

Figure 18. Typical Charger Detect Plot

In Figure 18, signals are defined as the following:

- Channel 1: The signal at the gates of DSG FETs Q38, Q40, and Q42
- Channel 2: The signal at the point with the net label of CHG_DET in the TIDA-01093 schematic
- Channel 3: The signal at the point with the net label of TS1_B in the TIDA-01093 schematic
- Channel 4: The signal at the point with the net label of PACK– in the TIDA-01093 schematic

In these tests, the Channel 1 signal is controlled by the MCU. A program can be written to assert this signal upon POR of the MCU. Once the TS1 pin of U1 driven by TS1_B goes high, U1 is activated, and the LDO output of U1 at REGOUT pin is enabled. The MCU then runs its initialize code accordingly, and the DSG output is asserted. This causes the Channel 1 signal going high, which indicates the entire system is activated and ready to respond to any inquiries from the communication interface initiated by an external host. After both CHG and DSG FETs are enabled, the voltage at CHG_DET and TS1_B would drop accordingly. Channel 4 is the voltage measured at PACK–. When a charger is applied, the voltage on the PACK– goes low. In this test, a charger with a charging voltage of 2 V greater than the battery voltage is used. The falling edge of this signal indicates the event of a charger insertion, and the rising edge of this signal indicates that the charging FETs are turned on and the voltage at PACK– gets equalized to BAT–.

Table 5 logs each element in the plot of Figure 18 under different VBAT and VGAP.

4.2.2.2 Conclusion

Per Table 5 and Figure 18, the charger detect circuit would be effective when the BAT voltage in the range from 50 to 82 V, a reasonable charger voltage with the minimum 2-V gap to the BAT voltage can always activate the system. It takes approximately 100 ms after the charger is applied to the PACK+ and PACK– for the system to be ready to response to any inquiries from the host in this implementation.

4.2.3 Load Removal Detect Test

4.2.3.1 Test Data

In Table 6, signals are defined as the following:

- V_{BAT}: Voltage applied between BAT+ and BAT–
- $I_{LEAKAGE}$: Current measured when Power Supply 1 is turned on and all CHG and DSG FETs are off
- V_{PACK}: Voltage between PACK+ and PACK– when the Power Supply 1 is turned on, all CHG and DSG FETs are off, and the ampere meter is removed
- V_{LOAD}: Voltage output at the point with the net label of LOAD_RM_DET in the TIDA-01093 schematic when Power Supply 1 is turned on, all CHG and DSG FETs are off, and the ampere meter is connected between PACK+ and PACK–
- T_{DELAY}: The time after the ampere meter is removed until the voltage at LOAD_RM_DET drops to 0

Table 6. Load Removal Detect Test

V_{BAT} (V)	$I_{LEAKAGE}$ (uA)	V_{PACK} (V)	V_{LOAD} (V)	T_{DELAY} (S) (V < 0.5 V)
50	0.1	< 0.5	2.44	207.2
60	0.1	< 0.5	3.28	297.6
80	1.8	8.368	3.24	408.1

Table 6 logs the voltage at the point with the label of LOAD_RM_DET before the ampere meter is removed as well as the delay time when the ampere meter is removed until V_{LOAD} drops to below 0.5 V. The capture plots for Table 6 are listed from Figure 19 to Figure 21. Their signals are defined as the following:

- Channel 1: The signal capture at the point with the net label of LOAD_RM_DET in the schematic
- Channel 2: The voltage at BAT+

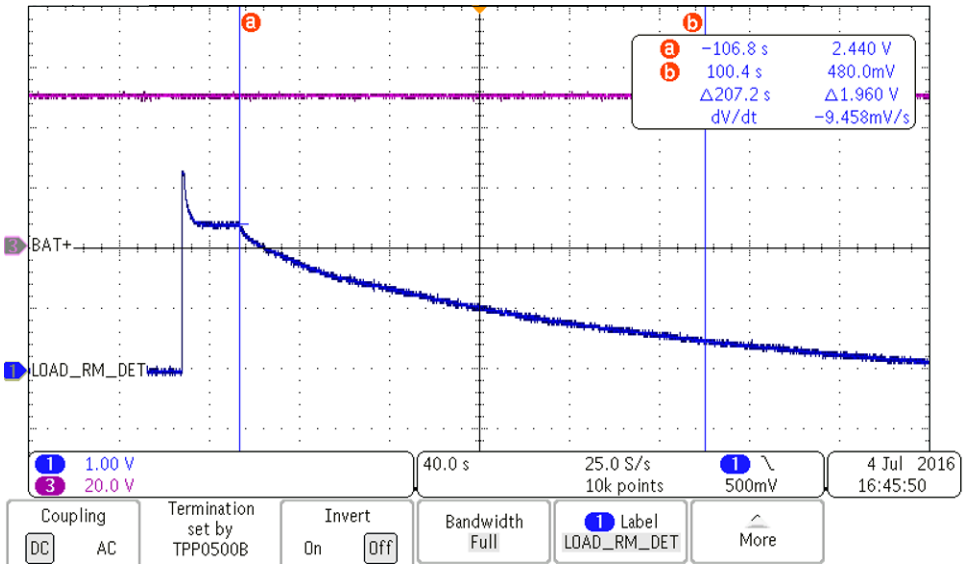

Figure 19. Load Removal Test With 50-V Battery Voltage

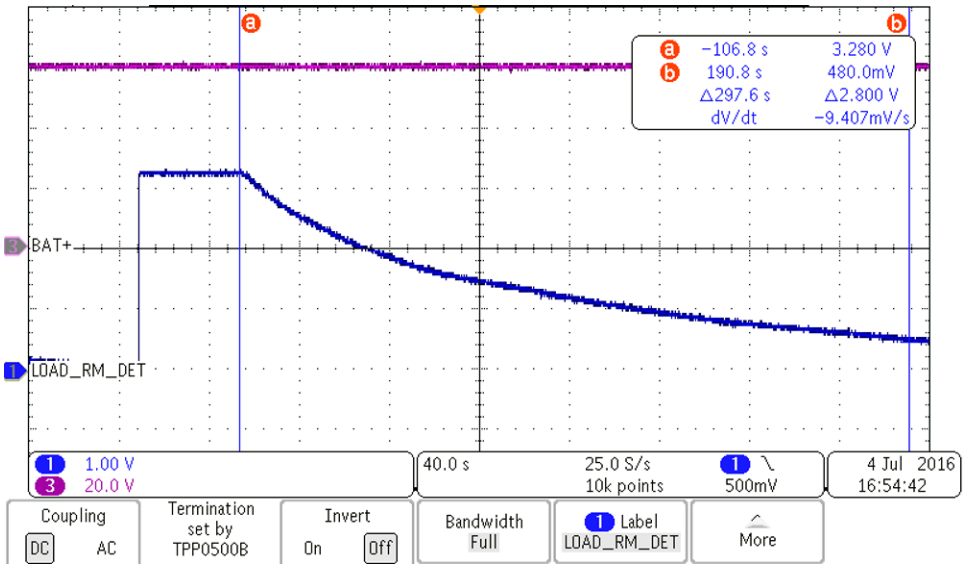

Figure 20. Load Removal Test With 60-V Battery Voltage

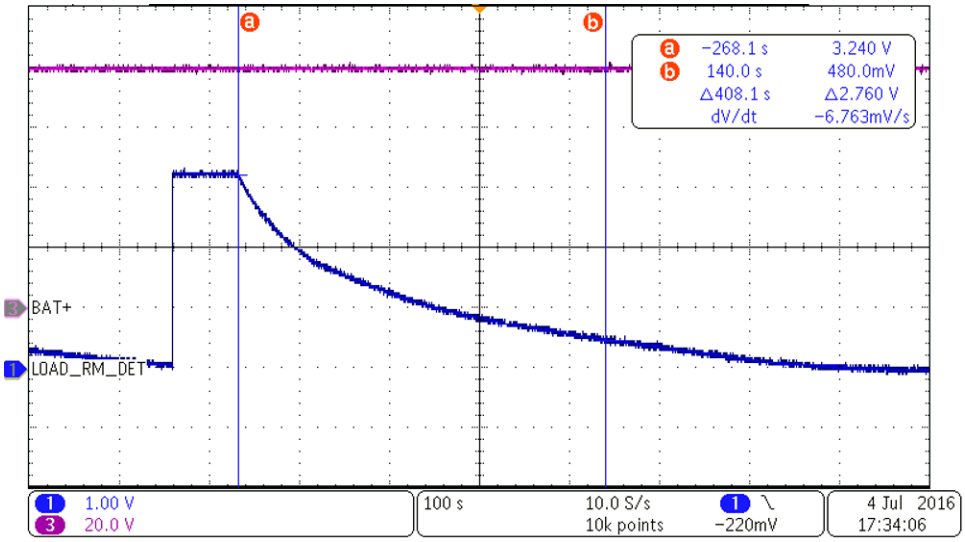

Figure 21. Load Removal Test 80-V Battery Voltage

4.2.3.2 Conclusion

With the voltage of V_{BAT} ranging from 50 to 80 V, the load removal event can be sensed by the MCU by monitoring the voltage V_{LOAD}, which represents the voltage at the point with the net label of LOAD_RM_DET in the TIDA-01093 schematic with the delay ranging from 200 to 400 s.

4.2.4 OV Protection Test

4.2.4.1 Test Data

Both the upper and bottom bq76930 devices are tested for OV protection. Figure 22 is the captured plot for the upper device OV test. Signals are defined as the following:

- Channel 1: Signal at the CHG pin of the upper bq76930 device
- Channel 2: Signal at the positive side of the battery simulator (connected to Cell16+) in Figure 15
- Channel 3: Signal at the gates of the CHG FETs
- Channel 4: Signal at the negative side of the battery simulator (connected to Cell16–) in Figure 15
- Channel M: Voltage across Cell16, equals to Channel 2 – Channel 4

Figure 23 is the zoomed in plot showing the delay between the original CHG output and the actual signal at the gates of CHG FETs.

Figure 24 is the captured plot for bottom device OV test. Signals are defined as the following:

- Channel 1: Signal at the CHG pin of the bottom bq76930 device
- Channel 2: Signal at the positive side of the Battery Simulator (Connected to Cell5+) in Figure 15
- Channel 3: Signal at the gates of the CHG FETs
- Channel 4: Signal at the negative side of the battery simulator (connected to Cell5–) in Figure 15
- Channel M: Voltage across Cell5, equals to Channel 2 – Channel 4

Figure 25 is the zoomed-in plot showing the delay between the original CHG output and the actual signal at the gates of CHG FETs.

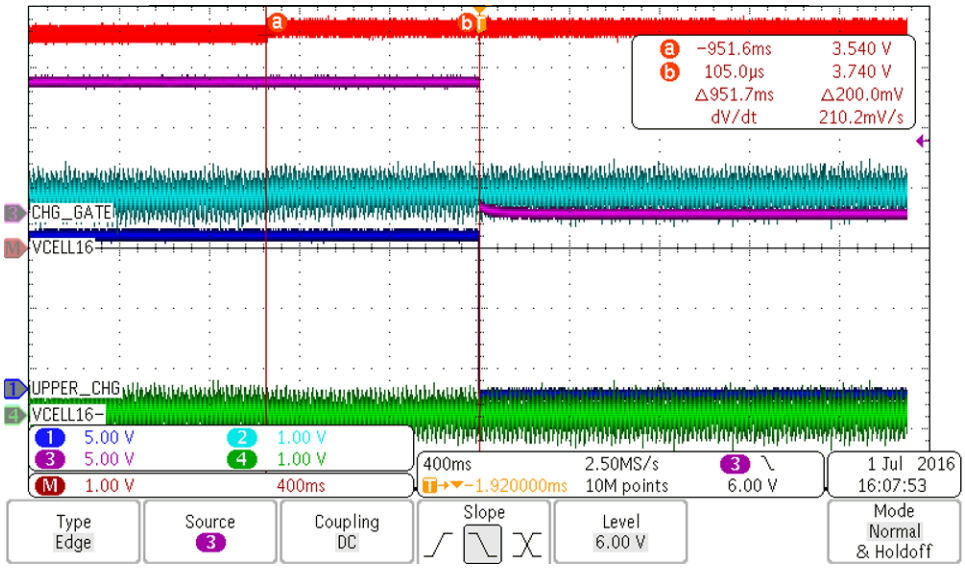

Figure 22. Upper bq76930 OV Protection Test

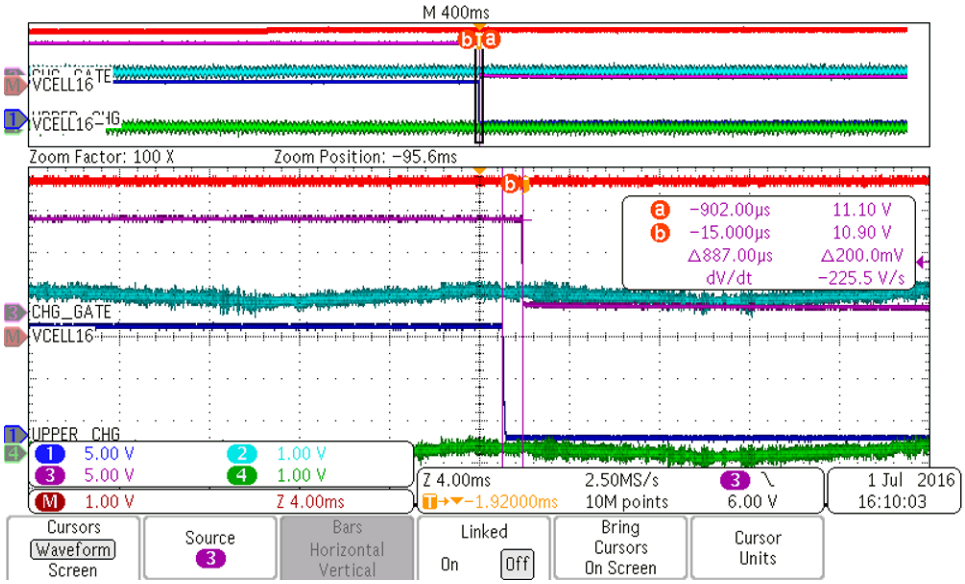

Figure 23. Zoomed-in Plots for Upper bq76930 OV Protection Test

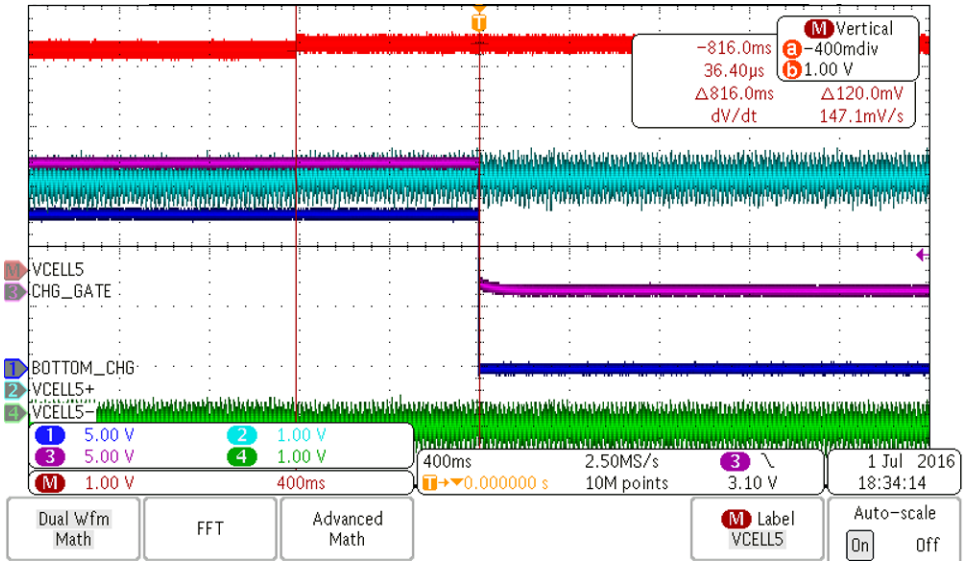

Figure 24. Bottom bq76930 OV Protection Test

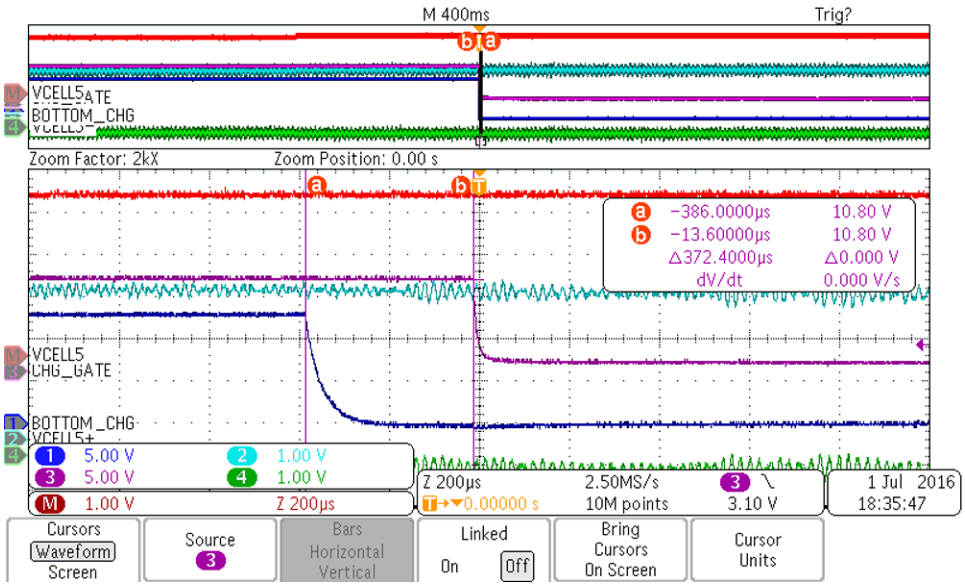

Figure 25. Zoomed-in Plots for Bottom bq76930 OV Protection Test

4.2.4.2 Conclusion

From these plots, it is verified that for both the upper and bottom bq76930 devices, when the cell voltage goes across the OV threshold, the OV protection is triggered. The delay of the protection is about 1 s, which is within the range specified in the datasheet. For the upper bq76930 device, the additional delay between the falling edge of CHG pin output and the falling edge of the voltage at the gates of the CHG FETs is 887 µs as measured in Figure 23. This additional delay is caused by the depletion of the charge on the capacitance between drains and gates, sources and gates of the FETs Q26, Q29, Q30, and Q31, and the depletion of the charge on C80. For the bottom bq76930 device, the additional delay between the falling edge of the CHG pin output of the device and the falling edge of the voltage at the gates of the CHGE FETs is 372.4 µs as measured in Figure 25. This additional delay is caused by the depletion of the charge on the capacitance of Q30 and Q31 and the depletion of the charge on C80. The additional delay for both the upper and bottom devices can be ignored comparing to the minimum configurable delay of 1 s for OV protection.

4.2.5 UV Protection Test

4.2.5.1 Test Data

Both upper and bottom bq76930 devices are tested for UV protection. Figure 26 is the captured plot for the upper device UV test. Signals are defined as the following:

- Channel 1: Signal at the DSG pin of the upper bq76930 device
- Channel 2: Signal at the positive side of the battery simulator (connected to Cell16+) in Figure 15
- Channel 3: Signal at the gates of the DSG FETs
- Channel 4: Signal at the negative side of the battery simulator (connected to Cell16–) in Figure 15
- Channel M: Voltage across the Cell16, equal to Channel 2 through Channel 4

Figure 27 is the zoomed in plot showing the delay between the original DSG output and the actual signal at the Gates of DSG FETs.

Figure 28 is the captured plot for bottom device UV test. Signals are defined as the following:

- Channel 1: Signal at the DSG pin of the bottom bq76930 device
- Channel 2: Signal at the positive side of the battery simulator (connected to Cell5+) in Figure 15
- Channel 3: Signal at the gates of the DSG FETs
- Channel 4: Signal at the negative side of the battery simulator (connected to Cell5–) in Figure 15
- Channel M: Voltage across the Cell5, equal to Channel 2 through Channel 4

Figure 29 is the zoomed in plot showing the delay between the original DSG output and the actual signal at the gate of DSG FETs.

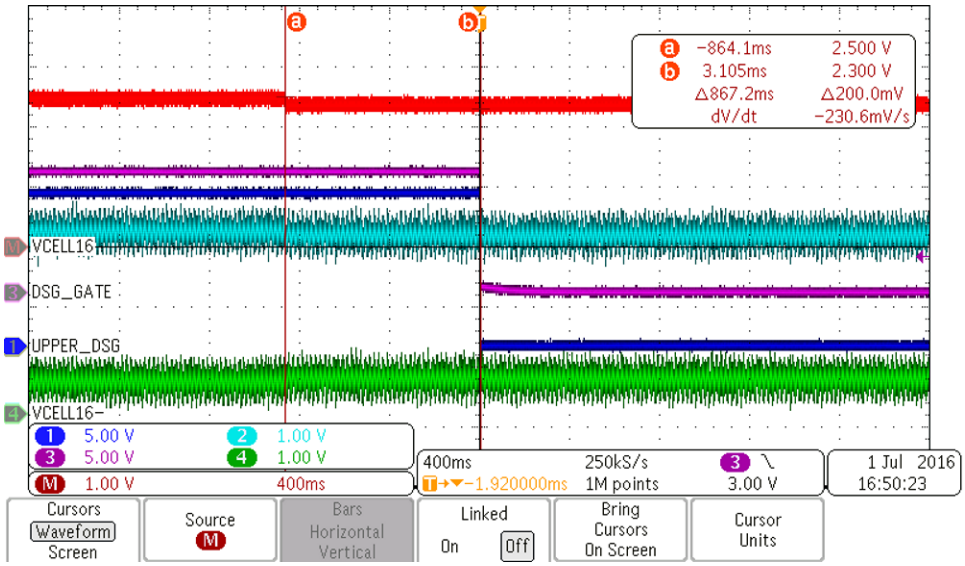

Figure 26. Upper bq76930 UV Protection Test

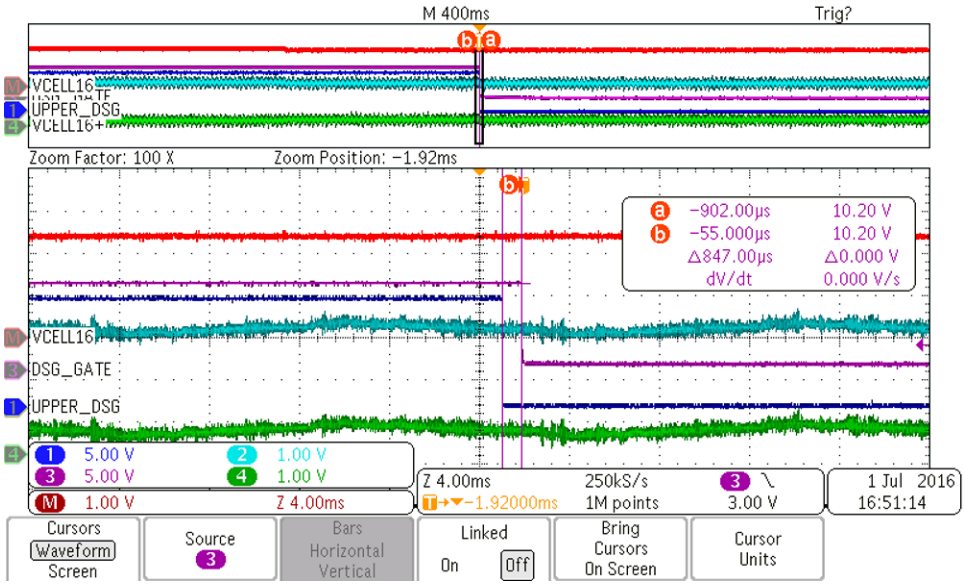

Figure 27. Zoomed in Plots for Upper bq76930 UV Protection Test

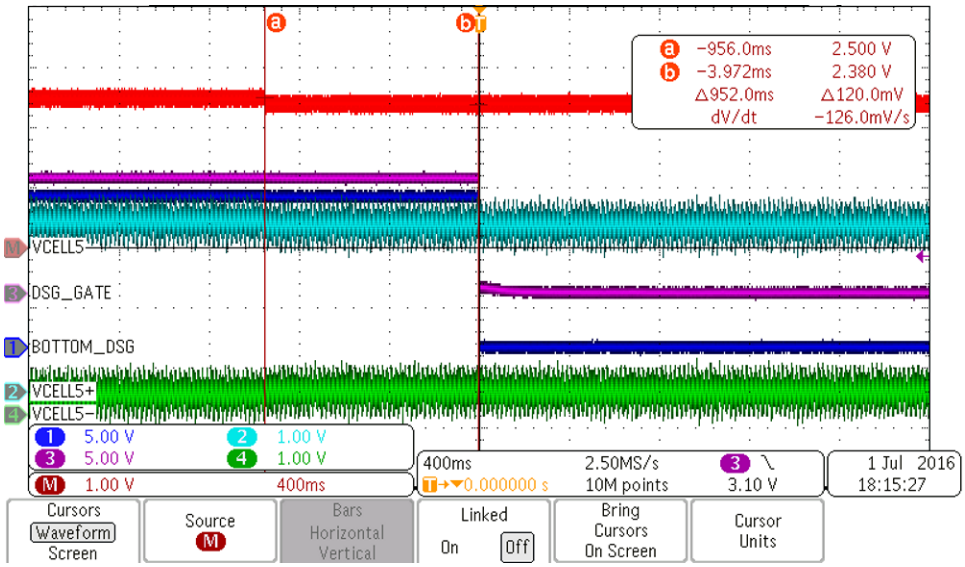

Figure 28. Bottom bq76930 UV Protection Test

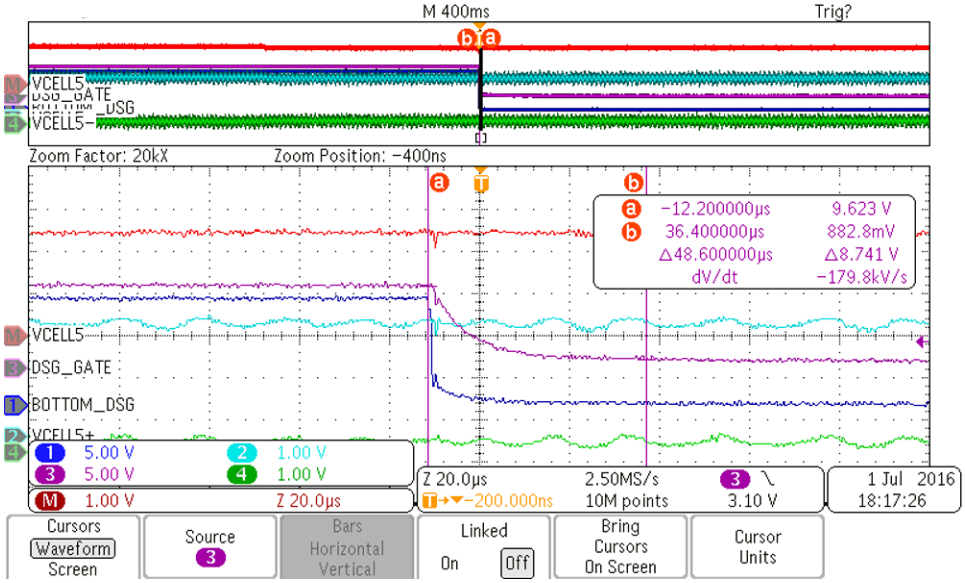

Figure 29. Zoomed in Plots for Bottom bq76930 UV Protection Test

4.2.5.2 Conclusion

From these plots, it is verified that for both upper and bottom bq76930 devices the UV protection is triggered when the cell voltage goes below the UV threshold. The delay of the protection is about 1 s, which is within the range specified in the datasheet. For the upper bq76930, the additional delay between the falling edge of DSG pin output and the falling edge of the voltage at the gates of the DSG FETs is 847 µs as measured in Figure 27. This additional delay is caused by the charge depletion on the capacitance between drains and gates, sources and gates of the FETs Q27, Q28, and Q32. For the bottom bq76930, the additional delay between the falling edge of the DSG pin output of the device and the falling edge of the voltage at the gates of the DSG FETs is almost 0 as measured in Figure 29, the falling time of the voltage at the gates of the DSG FETs is about 48.6 µs. The additional delay for both upper and bottom device can be ignored comparing to the minimum configurable delay of 1 s for UV protection.

4.2.6 UART Communication Test

4.2.6.1 Test Data

For the UART communication test, the channels in the captured plots are defined as the following:

- Channel 1: Voltage at the gates of the DSG FETs
- Channel 2: RXD signal at the test point TP6
- Channel 3: Voltage at the gates of the CHG FETs

The UpperDsgFetOn command is captured in Figure 30, followed by the two acknowledging bytes sent by the MCU. The two identical acknowledge bytes are captured in Figure 31 and Figure 32, which indicate the successful reception and interpretation of the command sent by external host as well as the successful execution of the desired operation defined by the command.

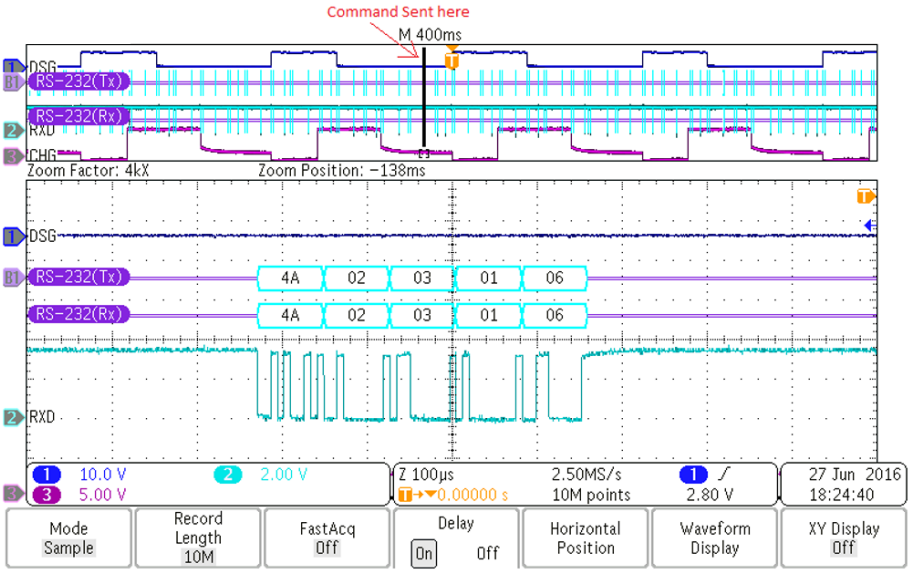

Figure 30. UpperDsgFetOn Command

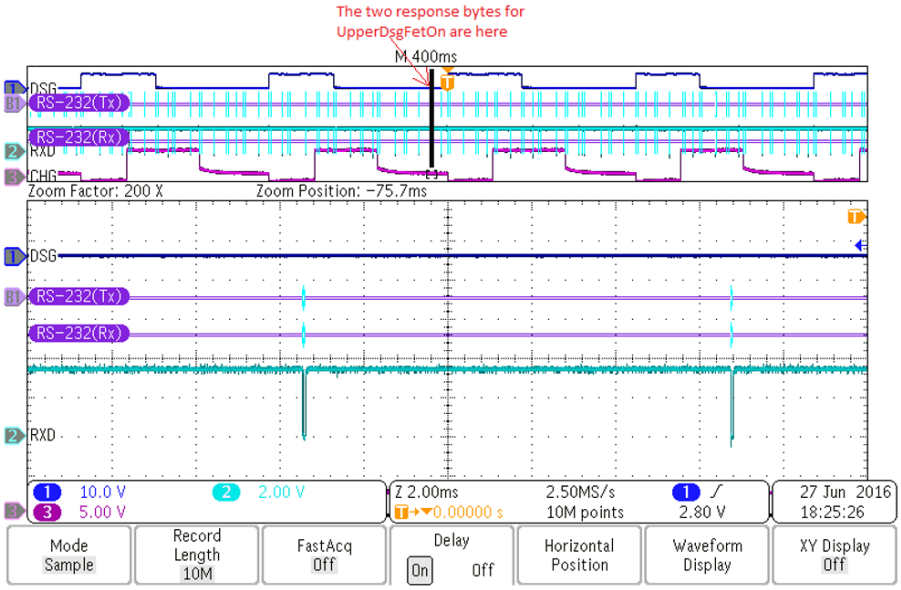

Figure 31. Two Identical Response Bytes for UpperDsgFetOn Command

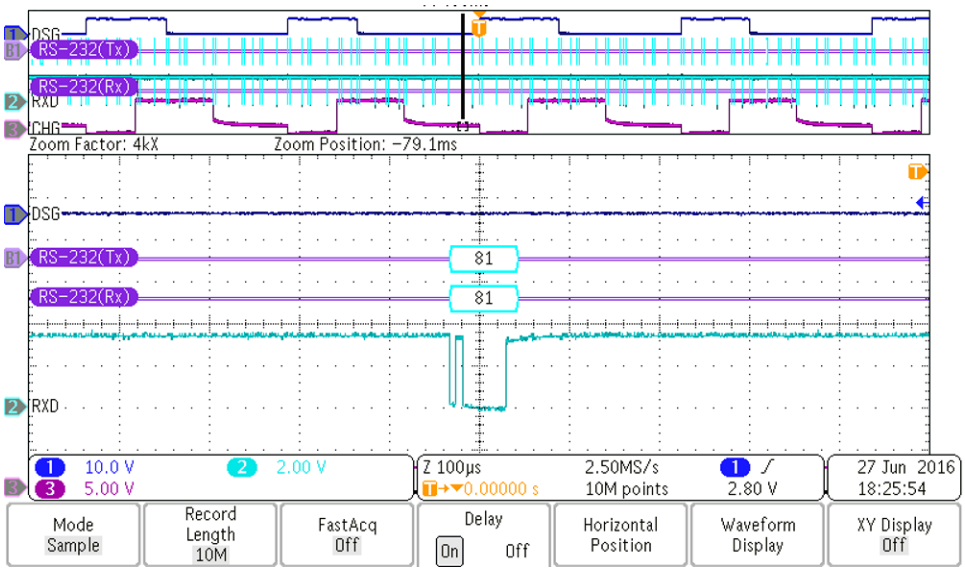

Figure 32. One Response Byte for UpperDsgFetOn

The BottomDsgFetOn command is captured in Figure 33, followed by the two acknowledging bytes sent by the MCU. The two identical acknowledge bytes are captured in Figure 34 and Figure 35, which indicate the successful reception and interpretation of the command sent by external host as well as the successful execution of the desired operation defined by the command.

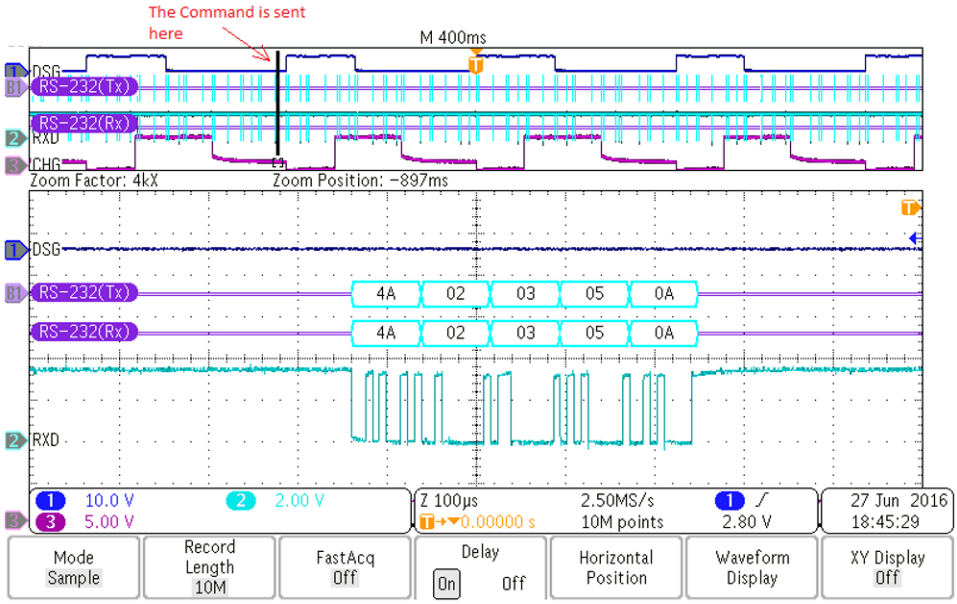

Figure 33. BottomDsgFetOn Command

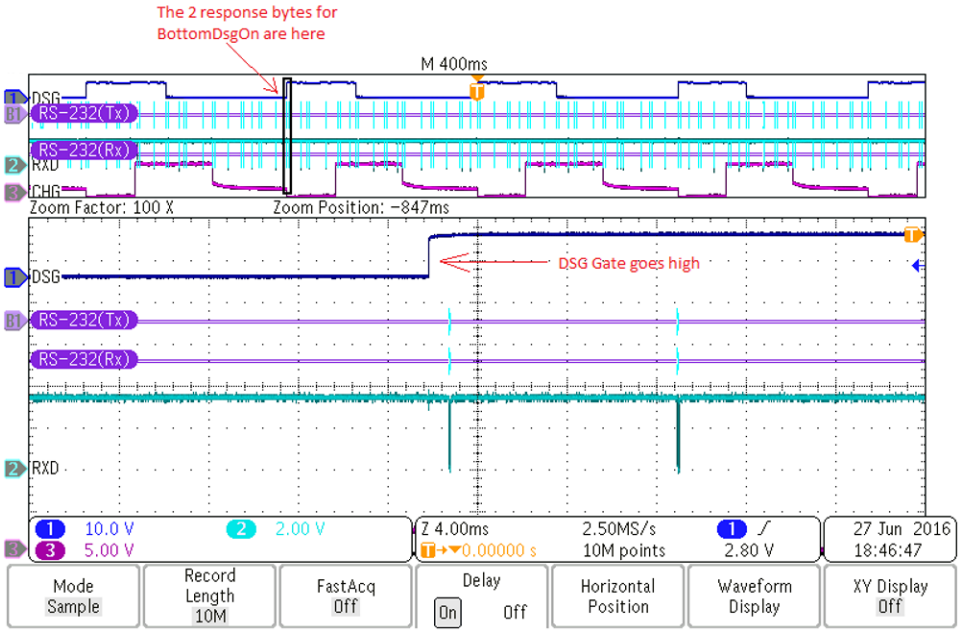

Figure 34. Two Identical Response Bytes for BottomDsgFetOn Command

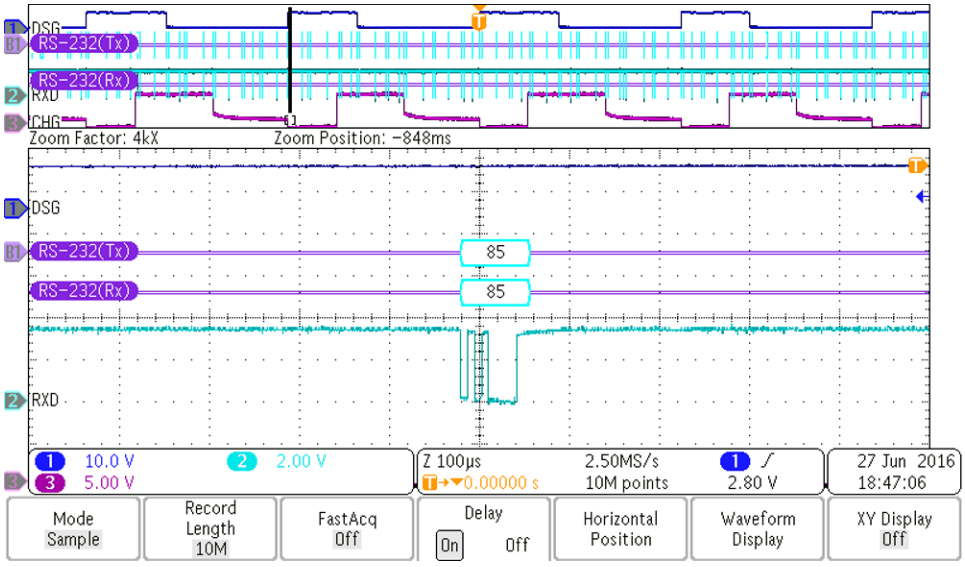

Figure 35. One Response Byte for BottomDsgFetOn

The UpperChgFetOn command is captured in Figure 36, followed by the two acknowledging bytes sent by the MCU. The two identical acknowledge bytes are captured in Figure 37 and Figure 38, which indicate the successful reception and interpretation of the command sent by external host as well as the successful execution of the desired operation defined by the command.

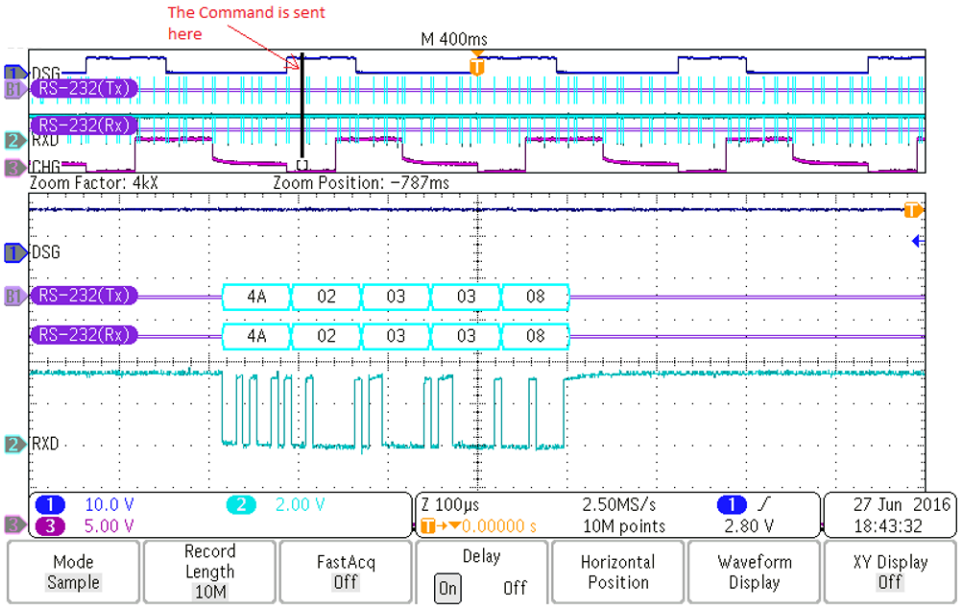

Figure 36. UpperChgFetOn Command

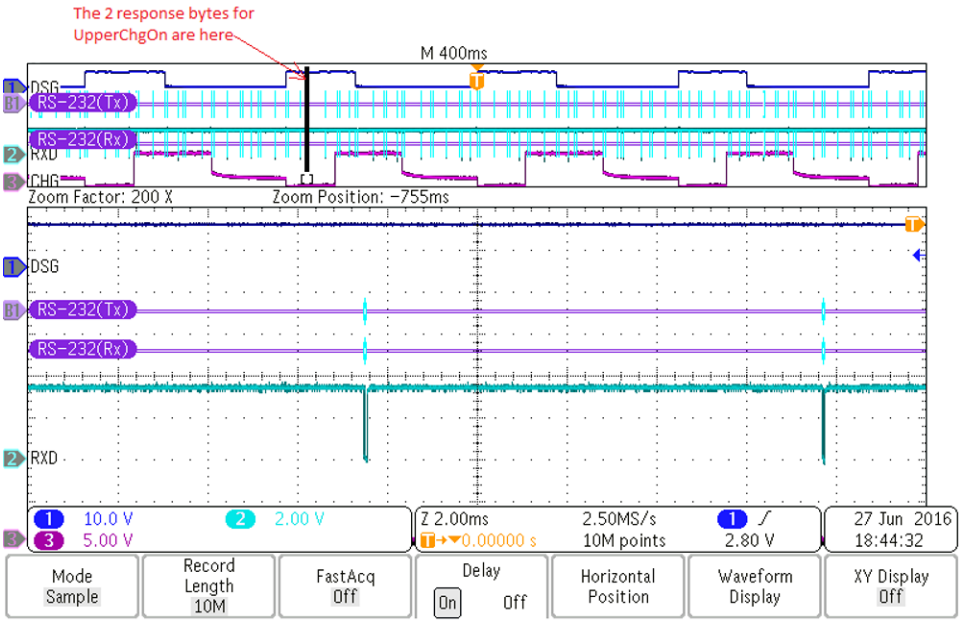

Figure 37. Two Identical Response Bytes for UpperChgFetOn Command

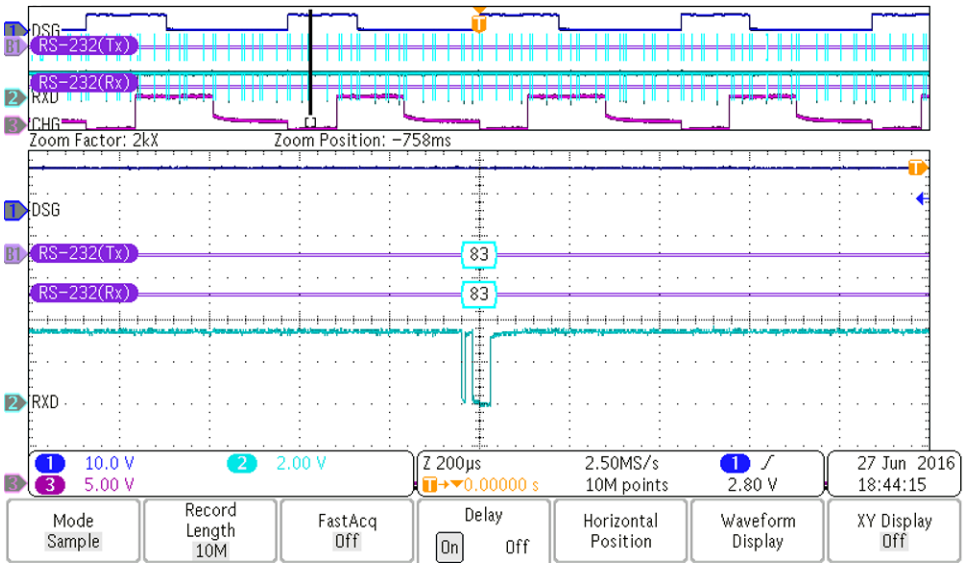

Figure 38. One Response Byte for UpperChgFetOn

The BottomChgFetOn command is captured in Figure 39, followed by the two acknowledging bytes sent by the MCU. The two identical acknowledge bytes are captured in Figure 40 and Figure 41, which indicate the successful reception and interpretation of the command sent by external host as well as the successful execution of the desired operation defined by the command.

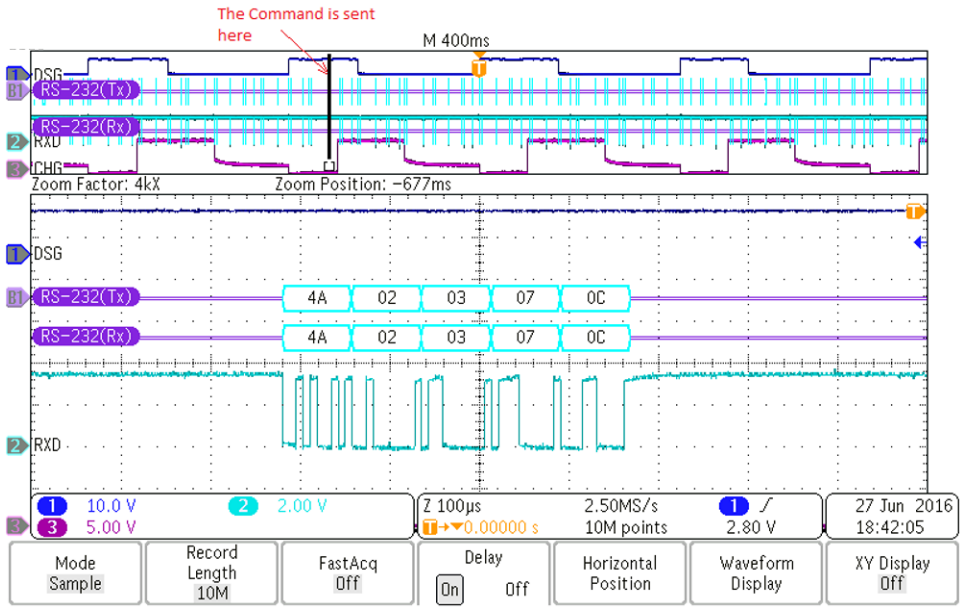

Figure 39. BottomChgFetOn Command

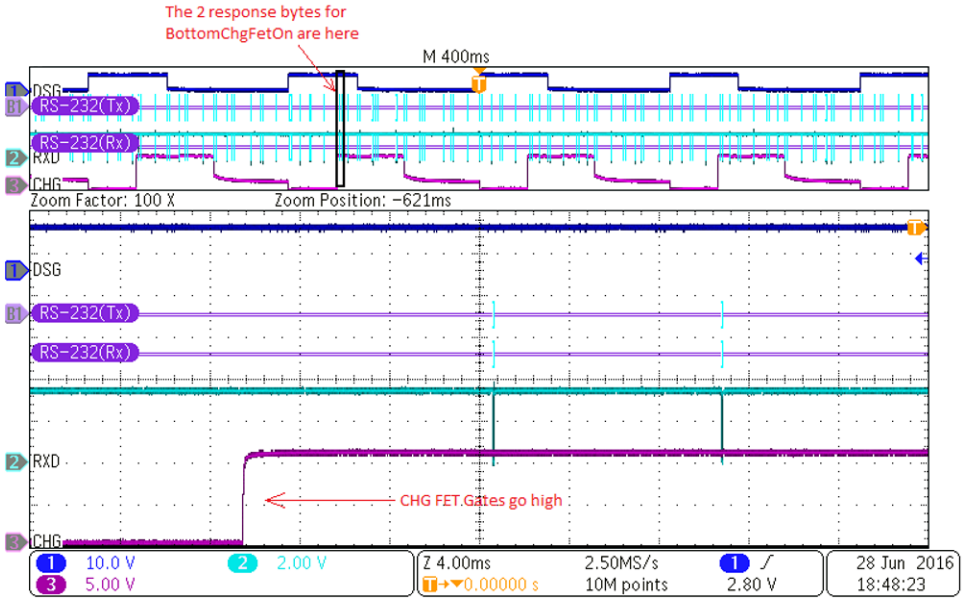

Figure 40. Two Identical Response Bytes for BottomChgFetOn Command

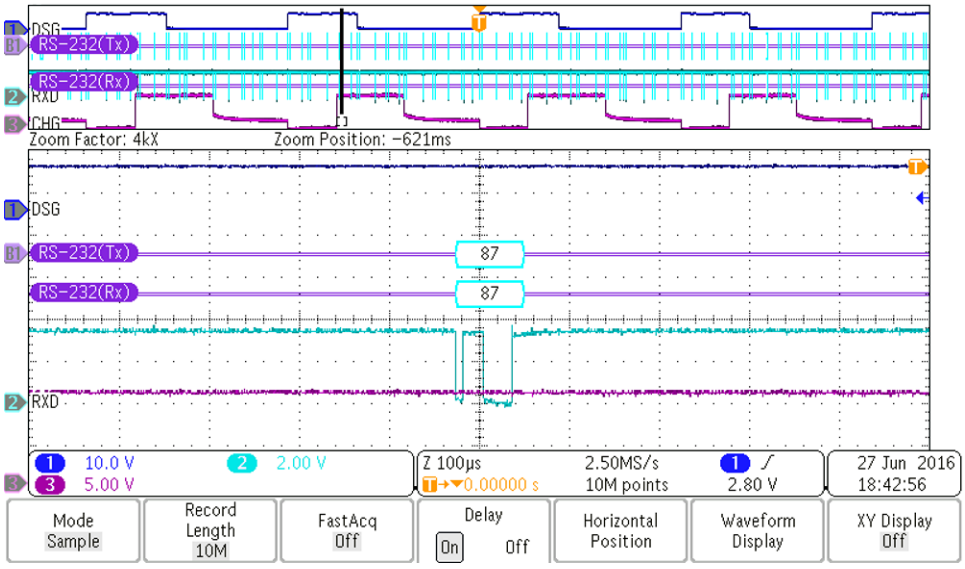

Figure 41. One Response Byte for BottomChgFetOn

The UpperDsgFetOff command is captured in Figure 42, followed by the two acknowledging bytes sent by the MCU. The two identical acknowledge bytes are captured in Figure 43 and Figure 44, which indicate the successful reception and interpretation of the command sent by external host as well as the successful execution of the desired operation defined by the command.

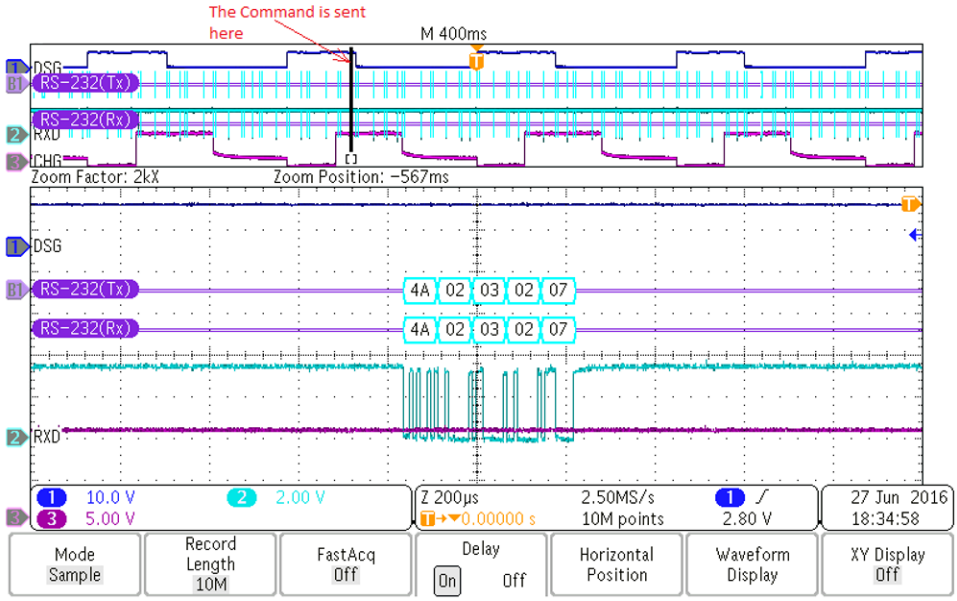

Figure 42. UpperDsgFetOff Command

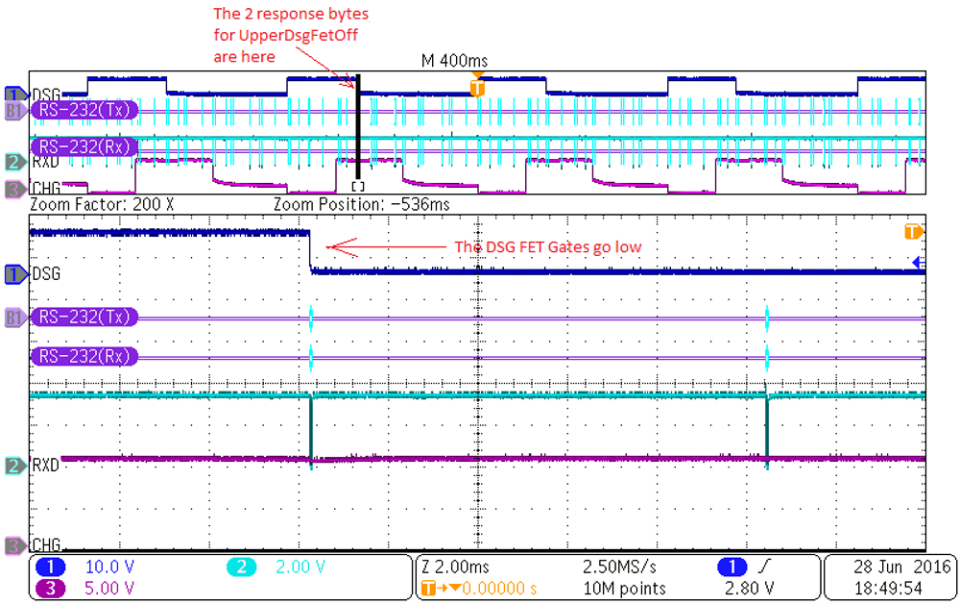

Figure 43. Two Identical Response Bytes for UpperDsgFetOff Command

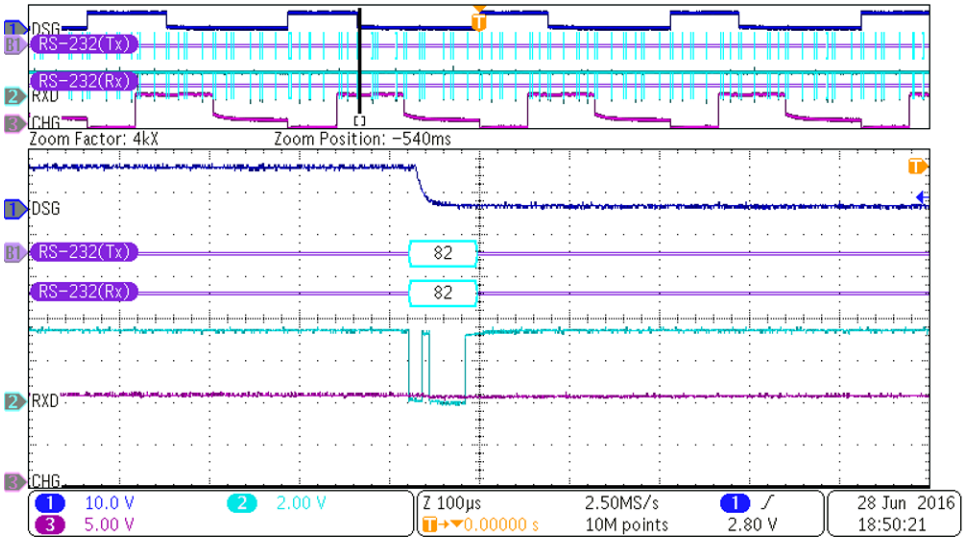

Figure 44. One Response Byte for UpperDsgFetOff

The UpperChgFetOff command is captured in Figure 45, followed by the two acknowledging bytes sent by the MCU. The two identical acknowledge bytes are captured in Figure 46 and Figure 47, which indicate the successful reception and interpretation of the command sent by external host as well as the successful execution of the desired operation defined by the command.

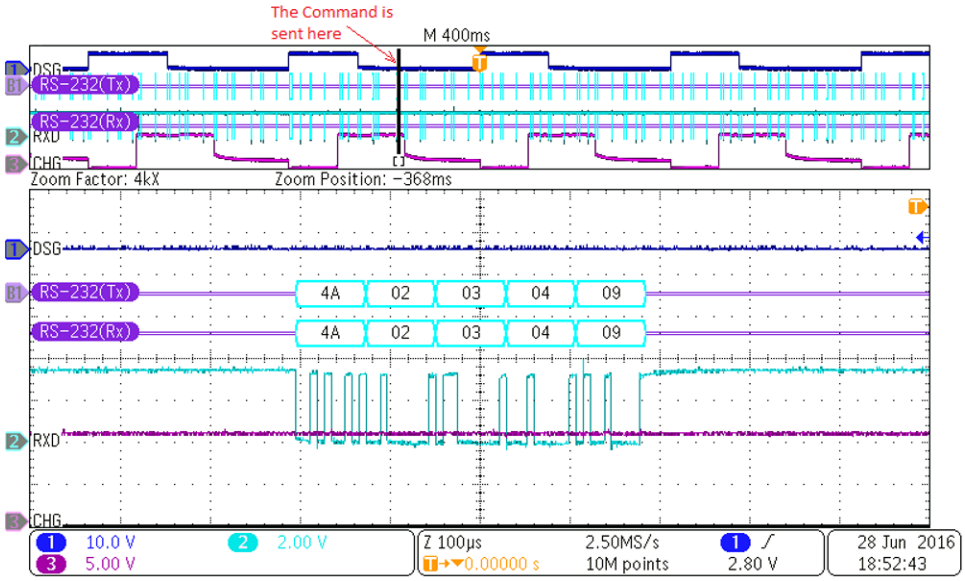

Figure 45. UpperChgFetOff Command

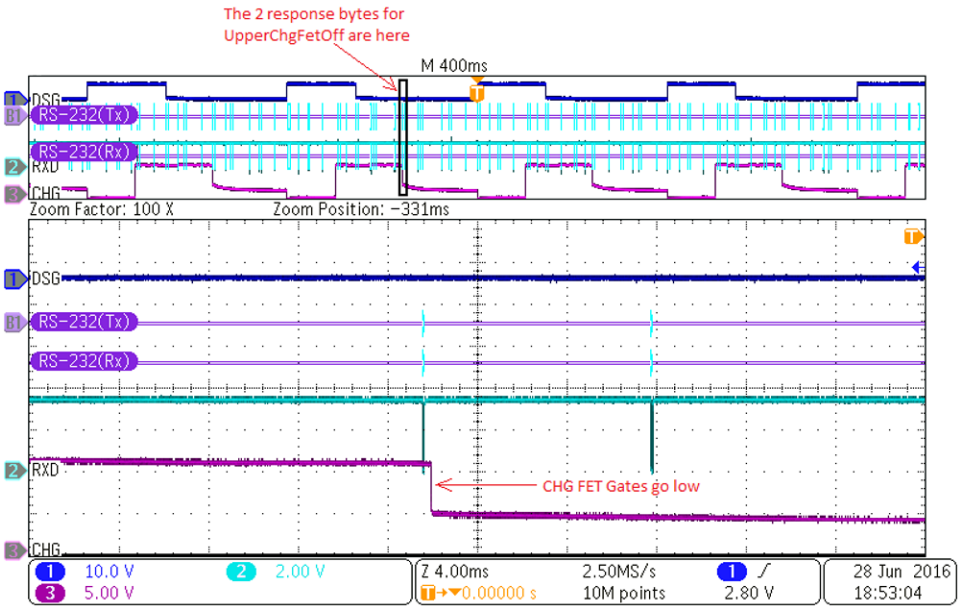

Figure 46. Two Identical Response Bytes for UpperChgFetOff Command

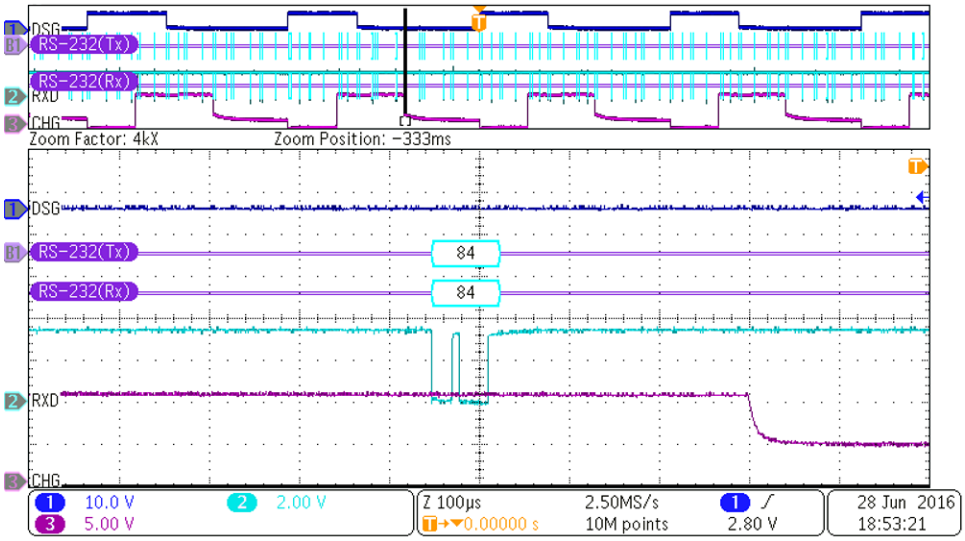

Figure 47. One Response Byte for UpperChgFetOff

5 Design Files

5.1 Schematics

To download the schematics, see the design files at TIDA-01093.

5.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01093.

5.3 PCB Layout Recommendations

- The high-current path section must be separated small signal section. The high-current patch section in this design refers to the section where charge and discharge current between battery and load or battery and charger. The small signal section refers to the section where the MCU communicates with the AFEs, sensing, and control signals to the AFEs or MCU.
- The ground of the small signal section must be connected to the high-current path between PACK– and BAT– at single point.
- Current sensing signal from the sense resistor resides at the high-current path (R97) must follow the Kevin connection pattern.
- The clearance between BAT+ and BAT– or GND_B must be no less than 0.8 mm.

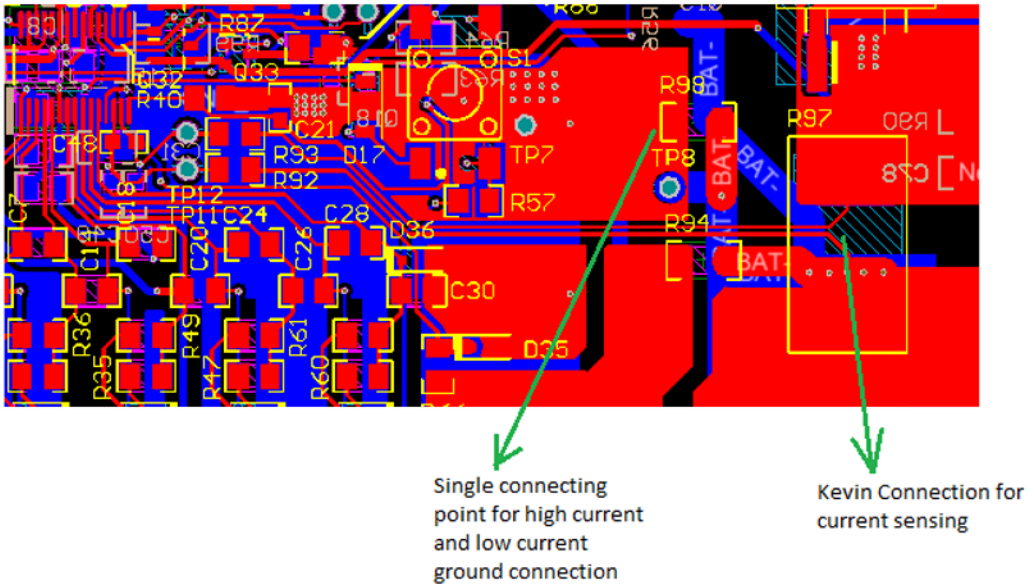

Figure 48. Ground Connection and Current Sensing

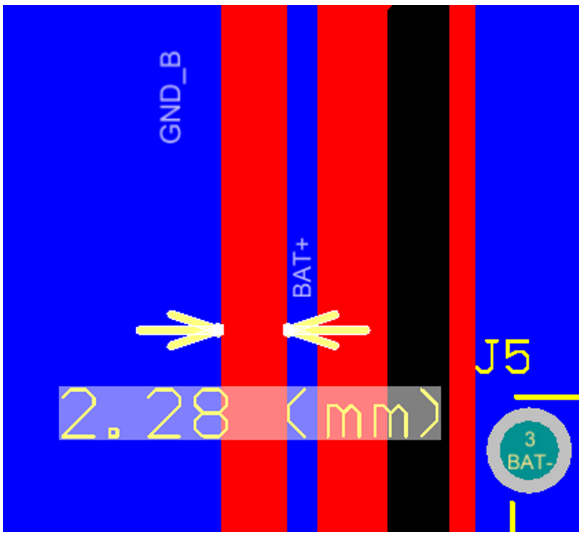

Figure 49. Keep Enough Clearance Between BAT+ and GND_B or BAT–

5.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-01093.

5.4 Altium Project

To download the Altium project files, see the design files at TIDA-01093.

5.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01093.

5.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01093.

6 References

1. Texas Instruments, *bq769x0 3-Series to 15 Series Cell Battery Monitor Family for Li-ion and Phosphate Applications*, bq76930 Datasheet (SLUSBK2)
2. Texas Instruments, *MSP430G2x55 Mixed Signal Microcontroller*, MSP430G2955 Datasheet (SLAS800)
3. Texas Instruments, *ISO154x Low-Power Bidirectional I^2C Isolators*, ISO1541 Datasheet (SLLSEB6)
4. Texas Instruments, *ISO1050 Isolated CAN Transceiver*, ISO1050 Datasheet (SLLS983)
5. Texas Instruments, *LM25018 48-V, 325-mA Constant On-Time Synchronous Buck Regulator*, LM25018 Datasheet (SNVS953)
6. Texas Instruments, WEBENCH® Design Center (http://www.ti.com/webench)

7 Terminology

ADC— Analog-to-digital converter

AFE— Analog front end

CAN— Controller area network

FET— Field-effect transistor

GPIO— General purpose input-output

MCU— Microcontroller unit

UART— Universal asynchronous receiver and transmitter

8 About the Author

STEVEN YAO is a system application engineer at Texas Instruments, where he is responsible for region customer support for BMS application in China. Steven joined TI as an FAE for BMS applications in 2004, and transitioned to SAE for BMS in 2015.

Revision A History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (August 2016) to A Revision	Page
• Changed from preview draft	1

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