TI Designs

High-Speed Digital Output PLC Module Reference Design

Description

This high-speed digital output module TI Design for programmable logic controllers (PLCs) illustrates the design of low-cost, simple high-speed single-ended digital output module using standard low-side driver and backplane powered using isolated power stage. High-speed digital output modules are required for motor control and positioning applications.

Resources

TIDA-00319	Design Folder
DRV8803	Product Folder
ISO7140CC	Product Folder
SN6501	Product Folder
LM2765	Product Folder
TIDEP0027	Tools Folder

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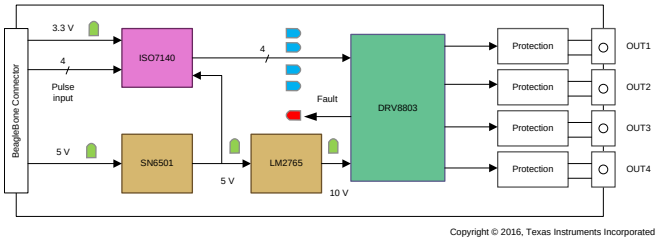
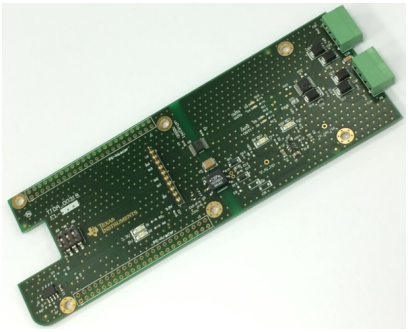


Features

- Four High-Speed Digital Outputs
- External Load Power
- Single-Ended Outputs Working up to
  - 500 kHz With 5-V Field Power
  - 100 kHz With 24-V Field Power
- 210-mW Power Consumption From Backplane Isolated Power Stage
- Less Than 100-ns Transition Time With 15-m Cable
- 300-mW Power Consumption Per Load for 5-V Supply and 44-Ω Load

Applications

- Factory Automation and Process Control
- Programmable Logic Controllers (PLCs)
- Position Controller
- Servo Motor and Stepper Motor driver



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1 System Overview

Programmable logic controller (PLC) digital outputs can be classified into low-speed outputs and high-speed outputs. High-speed outputs like pulse width modulated (PWM) signals or pulse train output (PTO) signals are typically used in position controllers.

Each motor (constituting an axis of motion) is controlled through two signals, typically representing speed and direction or equivalent quantities. PLC output module cards are available from one axis up to three axes required in 3D positioning.

Figure 1 and Figure 2 show a single axis position control PLC system in an open loop scheme used for stepper motors and a closed loop scheme used for servomotors. In both schemes, a high-speed PTO module is used to run the motor driver with a constant duty cycle variable frequency signal.

PTO signals might be speed and direction (forward, reverse) or speed in clockwise or counterclockwise directions. High-speed digital output modules are used to transmit the PTO signals to the motor driver over cables that can extend to several meters.

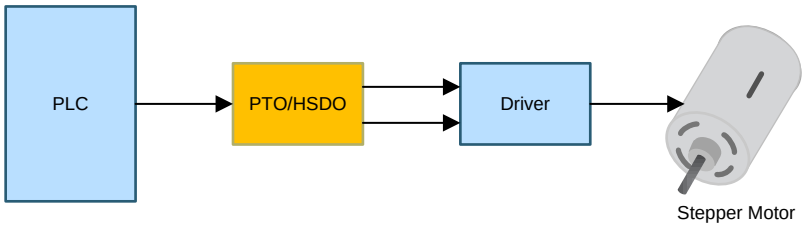

Figure 1. Open Loop Positioning Control

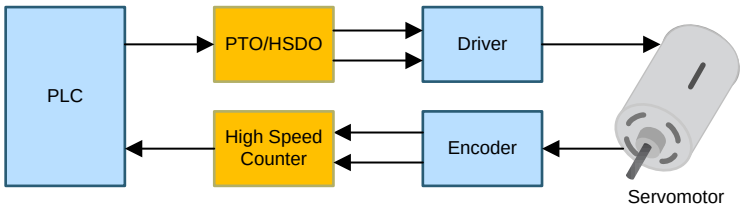

Figure 2. Closed Loop Positioning Control

1.1 System Description

High-speed digital output (HSDO) modules are based on a single-ended line driver. The isolated power stage provides 5 V to the isolated side. The digital isolator is required to connect the four digital pulse outputs from BeagleBone Black (BBB) programmable real-time unit (PRU) outputs or external inputs. For compatibility with BBB, a voltage of 3.3 V is used as primary-side isolator voltage, while 5 V is chosen for the secondary side to simplify the power stage. A voltage converter is needed if the line driver requires a supply voltage different than 5 V. Main power is driven from the BBB SYS_5V pins. Outputs are protected against surge and ESD. Backplane power is preferred here due to low power requirements.

Figure 3 reflects the conceptual block diagram.

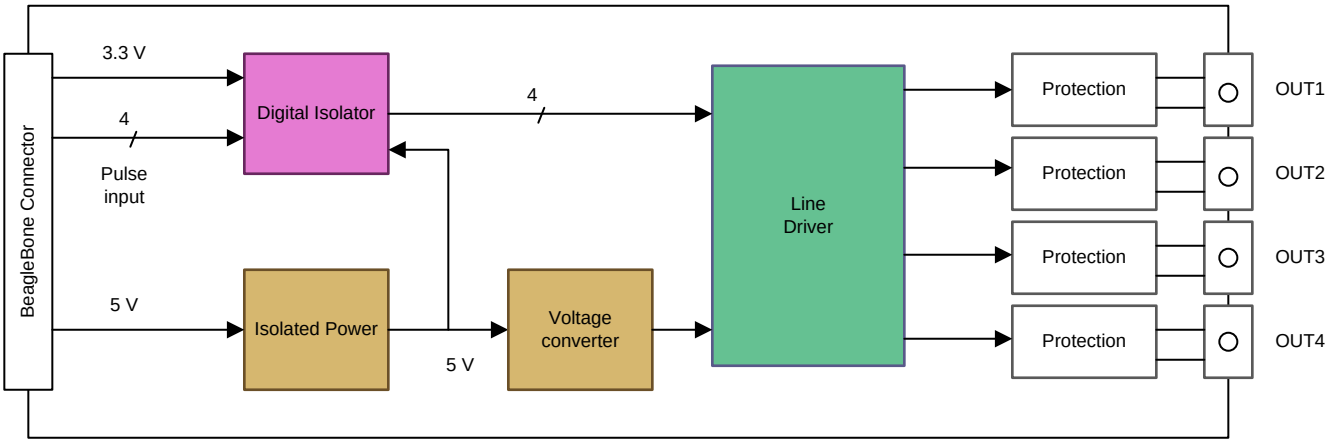

Figure 3. HSDO Module Block Diagram

1.2 Key System Specifications

Table 1 lists the target specifications for the HSDO module. This design targets a single-ended output. See TI Design TIDA-00766 for a counterpart in differential-ended output implementation. To enable the module to work with the TIDEP0027 reference design, the design is made in BBB cape format.

Table 1. Design Specifications

PARAMETER	DETAILS
Number of outputs	2 channels, 4 single-ended outputs
Load type	ohmic, opto-coupler inputs for step or servo amplifier
Load voltage	5 to 36 V external
Rated output current	125 mA rated, 500 mA max over temp range
Output signaling	5- to 36-V open drain
Load impedance	20 to 100 Ω: for 5-V supply; 120 to 300 Ω: for 24-V supply
Frequency	100 Hz to 500 kHz: for 5-V external load; 100 Hz to 200 kHz: for 24-V external load
Input duty cycle (mark/space ratio)	50% typical
Cable length	10 m minimum
Electrical Isolation	2 kV
Power source	5-V backplane power
Power consumption	0.5 W maximum
Temperature range	0°C to 85°C
EMC protection	ESD: 12 kV IEC Contact: 15 kV HBM EFT: 4 kV Surge: 1 kV

1.3 Block Diagram

Figure 4 reflects the component selected in Section 2 as well as the signage LED components added to monitor the availability of different power levels and input signals.

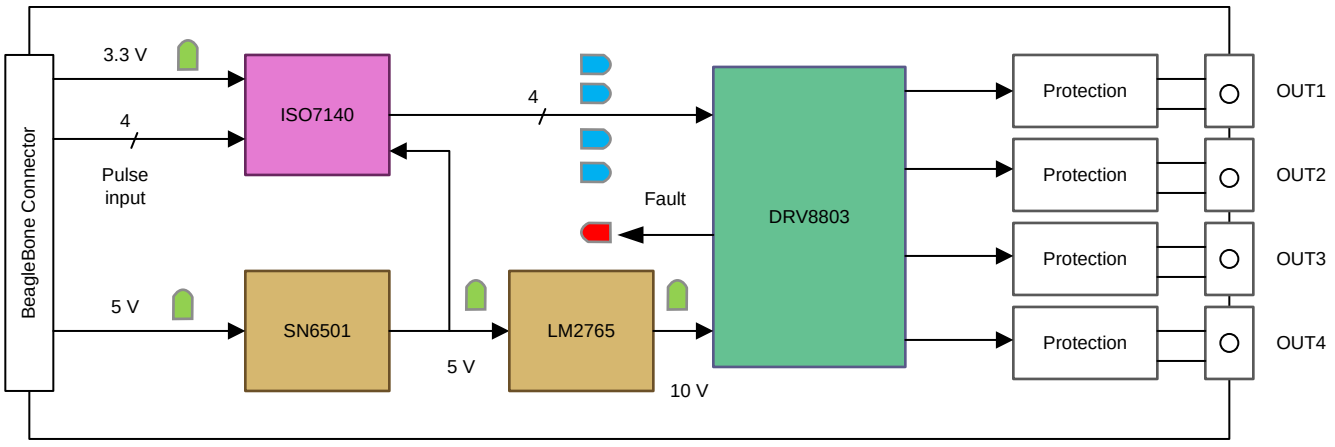

Figure 4. TIDA-00319 Block Diagram

2 Component Selection

2.1 Line Driver

For a targeted >10-m cable drive capability, single-ended high-speed driving is challenging. Higher speed driving calls for higher driving capability as well as low load impedance, which means high power consumption.

Assuming load capacitance is around 5 nF including cable and receiver capacitance. If 1-MHz speed is to be achieved and RC time constant of the load is to be kept below 0.1 in a period of 1 μs, a maximum load of 20 Ω must be used. When full-swing driving is used (like CMOS or TTL) and to maintain the VOL and VOH levels, driver output impedance must be in the range of 1 Ω for proper voltage levels.

Such low impedance with industrial voltage level of 24 V would result in high current (> 1 A) per output and significant load power consumption (> 20 W). The high current is restricting the driver choice. The high power requirement also limits the supply choice to the external field power supply. A low-side (LS) driver is suitable for these requirements. An LS switch allows for external power of the load and allows a higher drive for the same package compared to push-pull drivers. To allow higher speed with reasonable power, a restriction on the load supply voltage can be set (for example, 5 V) to limit both the power and maximum current in the driver. Select the receiver on the other side to be sensitive to the falling edge as the rising time is dominated by the load impedance.

Because this design will be used with the TIDEP0027, a direct output control is needed rather than encoded input or serial interface. LS motor drivers is a suitable solution for single ended line drivers, search in the Stepper Motor with integrated FETs page would show a wide range of selection. The DRV8803 is the best (and only valid) choice that provides four outputs direct interface. The DRV8803 is a small form-factor device with four integrated low-side drivers with 0.5 A each of simultaneous RMS current driving with only PCB passive cooling.

2.2 Isolated Power

Among the simplest topologies to realize the 5-V to 5-V isolated power is the push-pull DC-DC converter. There are almost no design equations. The push-pull driver SN6501 is a highly integrated driver. It is limited in output power, but for the application at hand where the line driver is relying on the external load power, the power requirement is way below the SN6501 maximum limit.

2.3 Voltage Converter

The DRV8803 works with a voltage supply in the range of 9 to 60 V. As this design will use external load power, the driver voltage is only used for gate driving. A voltage level as low as 8.3 V can still switch the gate with a little bit of higher driver impedance. Given that the DRV8803 requires a maximum < 2.1 mA to operate, one of the simplest power solutions is using a voltage doubler (charge pump) as a voltage converter. With a 5-V input, a stable 10-V output is generated using the charge pump given light load. The LM2765 is a switched capacitor voltage converter running with a supply voltage in the range of 1.8 to 5.5 V with 90% efficiency at a 20-mA load. Compared to the alternative boost converters, the switched capacitor solution is much more compact and cost effective.

2.4 Digital Isolator

The ISO7140 is selected as a four-channel digital isolator. The ISO714x family provides galvanic isolation at 2500 V_{RMS} for 1 minute per UL or 4242 V_{PK} per VDE. The selected isolators support up to 50 Mbps, which is well above the communication speed used in this TI Design.

3 Getting Started Hardware

3.1 DRV8803 Driver

The DRV8803 is a four-channel low-side driver with overcurrent protection. It has built-in diodes to clamp turnoff transients generated by inductive loads and can be used to drive unipolar stepper motors, DC motors, relays, solenoids, or other loads like cables and resistive loads as in our design. The DRV8803 can supply up to a 0.8-A continuous current per channel with all channels turned on at 25°C with passive PCB heat sinking. Being controlled through a simple parallel interface allows it to work with existing TIDEP0027 PTOs.

Internal shutdown functions are provided for overcurrent protection, short-circuit protection, undervoltage lockout, over-temperature protection, and faults are indicated by a fault output pin. A 16-pin HTSSOP package is used for its compact layout.

The DRV8803 can withstand power supply voltage up to 65 V, giving more flexibility in field power supply selection and a more robust application.

Figure 5 shows the internal structure of the DRV8803. The four-input parallel interface (IN1 to IN4) can be disabled by nENBL pin. nFAULT indicates fault conditions, which requires RESET assertion to restore operation. VCLAMP is used to clamp output voltage to a certain level or to the field supply level.

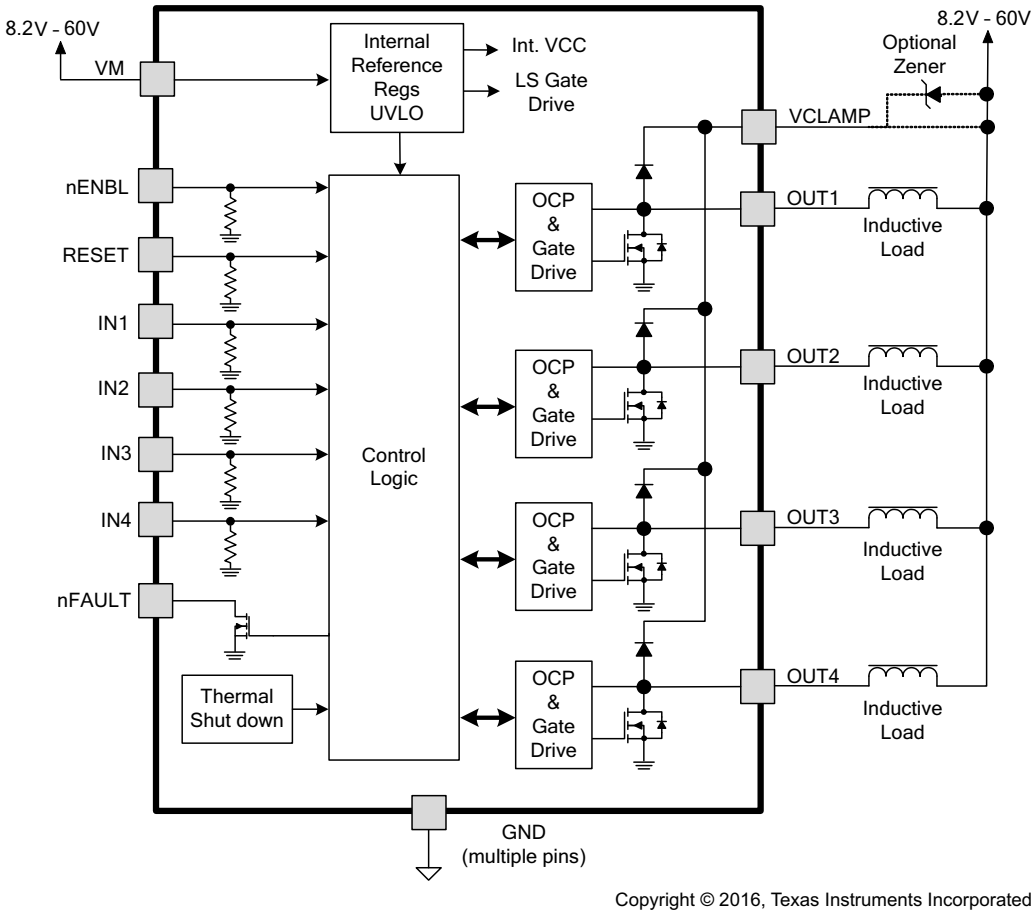

Figure 5. DRV8803 Functional Block Diagram

3.1.1 External Load

External load (resistive and capacitive) is calculated here within the limits of low side maximum current and reasonable power dissipation as well as maximum expected frequency.

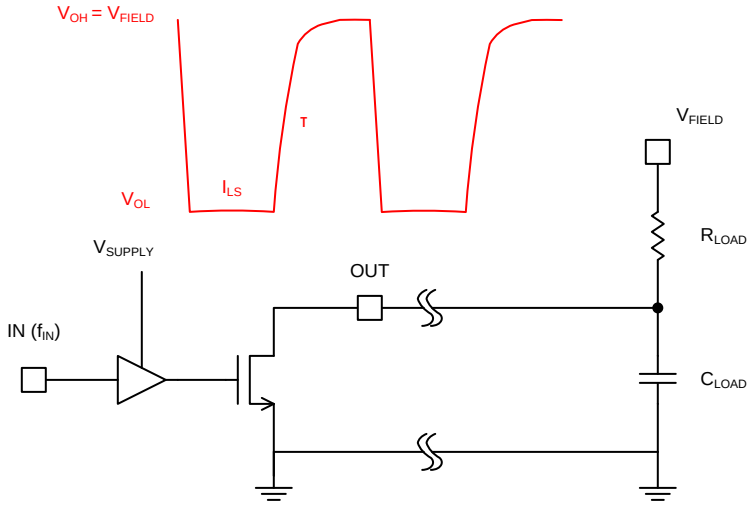

Figure 6. TIDA-00319 Driver Load Circuit

Figure 6 illustrates the load circuit connected to the LS driver. The output waveform is also plotted in Figure 6. Use these simple equations to calculate the different design parameters:

- Average load power

$$\bar{P}_R = D\frac{V_{FIELD}^2}{R_L} \quad (1)$$

where D is the duty cycle of the input signal (50% in case of PTO)

- Load current when V_{OUT} is low

$$I_R = \frac{V_{FIELD}}{R_L} \quad (2)$$

- Output low level

$$V_{OL} = I_R \times r_{DS} \quad (3)$$

where low-side switch resistance is 0.4 to 0.8 Ω for a low V_{SUPPLY}

- Output high level

$$V_{OH} = V_{FIELD} - I_{OFF} \times R_{LOAD} \quad (4)$$

as I_{OFF} is in the µA range, consider $V_{OH} = V_{FIELD}$

- Time constant of the rising edge

$$\tau = R_{LOAD} \times C_{LOAD} \quad (5)$$

- Period

$$T = \frac{1}{f_{IN}} \quad (6)$$

Assuming the maximum frequency of 500 kHz, and assuming t = T/10 and 4 nF of the total load including the cable, this results in a maximum load of 50 Ω.

If targeting a lower frequency such as 200 kHz, use a higher impedance of 120 Ω. Assuming a field supply of 5 V and a load of 40 Ω, a maximum current of 125 mA and an average power of 0.3125 W is calculated for one channel.

Assuming a field supply of 24 V and a load of 100 Ω, a maximum current of 240 mA and an average power of 2.9 W is calculated for one channel. This shows the high power requirement of a high field supply, which prevents high-speed operation on that field supply level.

With the given current calculations, and assuming worst case switch resistance of 0.8 Ω, a worst case output low level would be ~0.1 V for a 5-V supply, and ~0.2 V for the 24-V supply; this does not include reflection and other signal distortion aspects.

3.1.2 Clamp Diode

The DRV8803 has internal diodes to a common clamping pin. This pin allows setting a clamping voltage different from the operating voltage set by external Zener diode. Unlike the application circuit in the DRV8803 datasheet (SLVSAW5), the Zener diodes are connected between the clamping point and ground. This connection guarantees independence of the low voltage supply used (10 V) and the clamping voltage (rated field supply, for example, 36 V max).

The unidirectional SMB TVS diode with a 36-V reverse standoff voltage is used. This allows the usage of high field supply with low power supply for the driver, still protecting the driver from surges and other transient events.

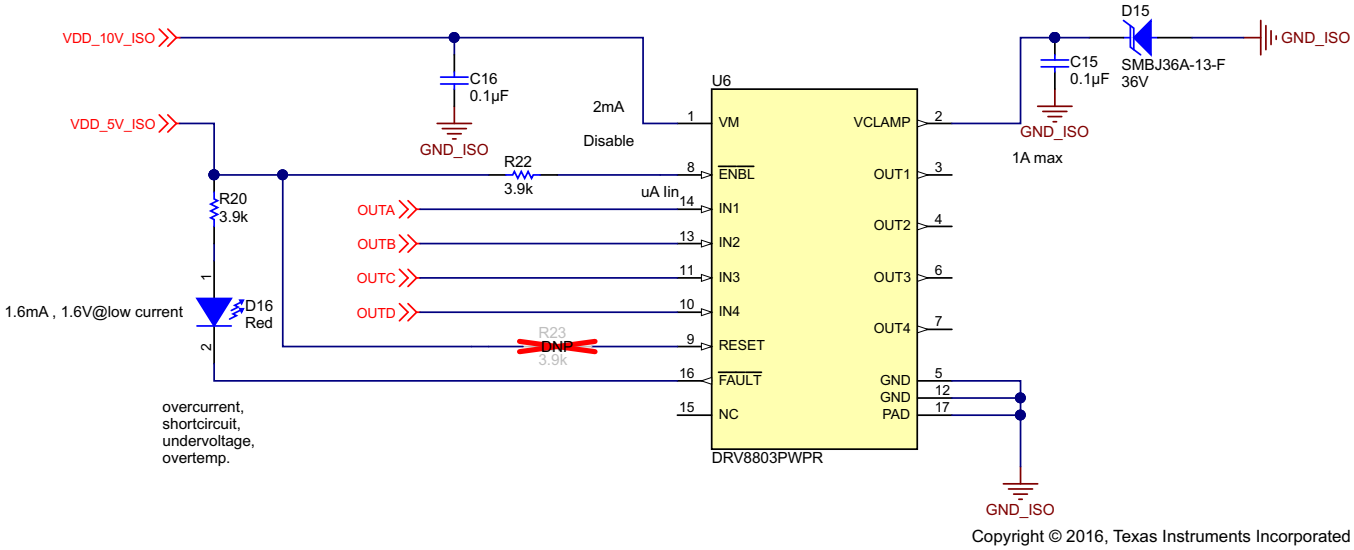

Figure 7. DRV8803 Output Driver Schematic

3.1.3 Thermal Considerations

At its peak power dissipation, an area of about 15 cm^2 per DRV8803 device would suffice to operate at ambient temperatures of 85°C with only PCB cooling. The layout design provides around 26-cm2 copper on the top layer, and 33 cm^2 on the bottom layer per device. The thermal management should not be an issue at all, and the layout area can be further reduced if smaller footprint is required.

3.1.4 Protection

In addition to the clamp diode, similar diodes are placed at each output for protection against electrical transient. Same unidirectional SMB TVS diode with a 36-V reverse standoff voltage is used for each output plus a 100-pF output capacitor to reduce the output transient time and enhance signal properties. Figure 8 shows the TVS diodes on a couple of outputs.

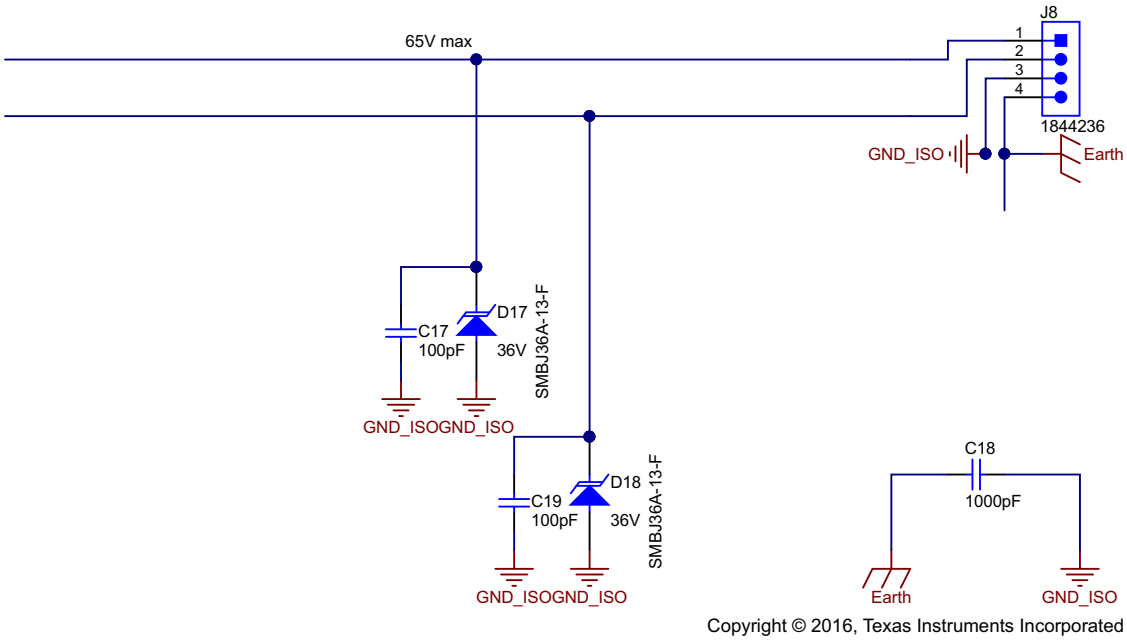

Figure 8. Protection TVS Diodes for Two Outputs

3.2 Isolated Power

The SN6501 is a monolithic oscillator and power-driver, specifically designed for small form factor, isolated power supplies in isolated interface applications. The device drives a low-profile, center-tapped transformer primary from a 3.3-V or 5-V DC power supply. The secondary can be wound to provide any isolated voltage based on transformer turns ratio.

The SN6501 is a transformer driver designed for low-cost, small form-factor, isolated DC-DC converters using the push-pull topology. The device includes an oscillator that feeds a gate-drive circuit. The gate drive, comprising a frequency divider and a break-before-make (BBM) logic, provides two complementary output signals, which alternately turn the two output transistors on and off.

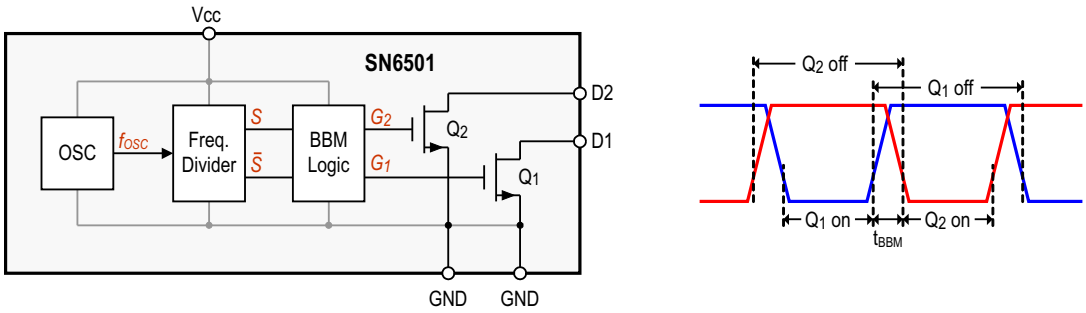

Figure 9. SN6501 Block Diagram

The output frequency of the oscillator is divided down by an asynchronous divider that provides two complementary output signals, S and S, with a 50% duty cycle. A subsequent BBM logic inserts a dead time between the high pulses of the two signals.

The switching frequency for the 5-V input is in the range of 300 to 600 kHz with 400 kHz nominal. The push-pull driver is an unregulated supply, which is acceptable if the input voltage range is limited, and the load range is also limited. In this TI Design, the load is almost constant regardless of the input activity and output driver load.

The push-pull stage design consists of:

- Diode selection
- Capacitor selection
- Transformer selection

3.2.1 Diode Selection

A diode is chosen to minimize the forward voltage to maximize secondary voltage and minimize power dissipation. In a high-frequency application like using with the SN6501, a short recovery time is also required. Diode breakdown voltage must exceed the output voltage, and maximum current handling must exceed maximum current in the switch. A good choice for low-volt applications and ambient temperatures of up to 85°C is the low-cost Schottky rectifier MBR0520L with a typical forward voltage of 275 mV at a 100-mA forward current.

3.2.2 Capacitor Selection

Two capacitor components are required at the output of the push-pull stage: a bypass capacitor with low impedance at high frequencies, typically in the range of 10 to 100 nF, and a bulk capacitor at the rectifier output to smooth output voltage, which is at least 10 µF. 22 µF plus 0.1-µF caps are used at the output. An input bulk capacitor at the center tap of the primary supports large currents into the primary during the fast switching transients. To minimize ripple, two capacitors (1 µF and 10 µF) are used.

3.2.3 Transformer Selection

Transformer design parameters include the V-t product to prevent transformer from saturation and turns ratio to deliver the output voltage in presence of the diode drop. Maximum power and isolation voltage are other two parameters to consider when selecting. For more details about transformers and other components selection, see SN6501 datasheet (SLLSEA0).

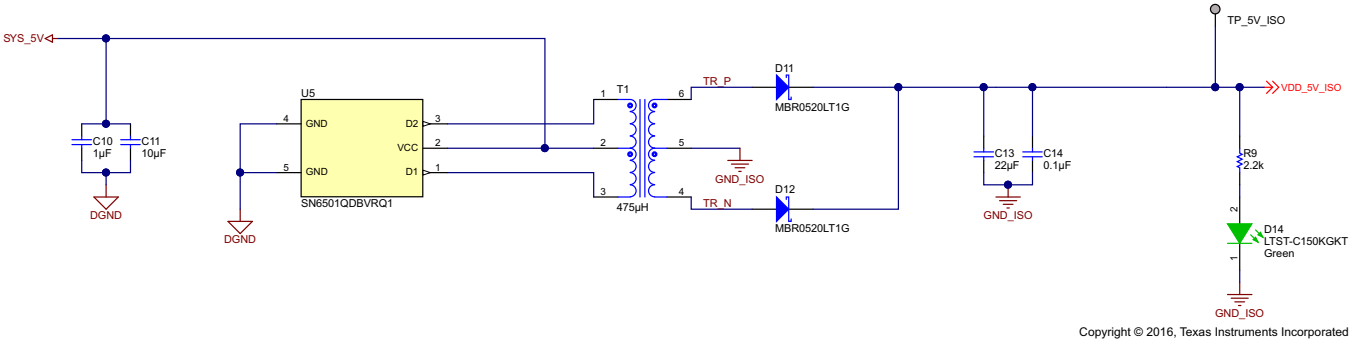

Figure 10. Push-Pull Circuit Schematic

3.3 Charge Pump Voltage Converter

The LM2765 CMOS charge-pump voltage converter operates as a voltage doubler for an input voltage in the range of 1.8 to 5.5 V. Two low-cost capacitors and a diode are used in this circuit to provide an output current of up to 20 mA.

The operating principle is shown in Figure 11. Input voltage is stored on capacitor C1 in one phase, and in the next phase this voltage is added to the input voltage to generate double the voltage at the output.

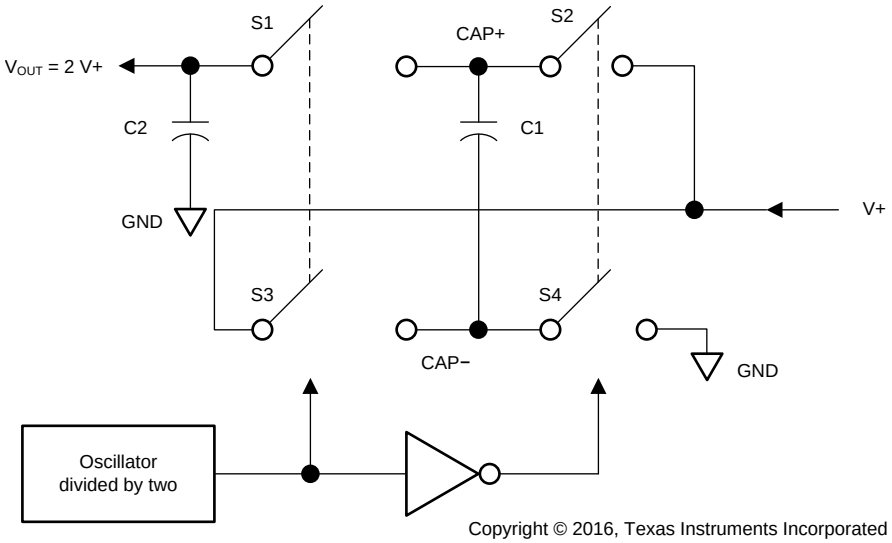

Figure 11. Voltage Doubling Principle

The LM2765 operates at a 50-kHz switching frequency to reduce output resistance and voltage ripple with an operating current of only 130 μA (operating efficiency greater than 90% with most loads) and 0.1-μA typical shutdown current.

One important design parameter in the charge pump circuit is the output resistance, which is a function of the switch resistance, oscillator frequency, pumping capacitor C1, and output capacitor C2.

$$R_{OUT} \cong 2R_{SW} + \frac{2}{f_{OSC} \times C_1} + 4ESR_{C1} + ESR_{C2} \quad (7)$$

R_{SW} is typically 8 Ω in the LM2765. Equation 7 shows the benefit of increasing the switching frequency and selecting low ESR capacitors to reduce the output resistance.

Output ripple voltage is a function of the load current, switching frequency, output capacitance, and its effective series resistance.

$$V_{RIPPLE} = \frac{I_O}{f_{OSC} \times C_2} + 2 \times I_O \times ESR_{C2} \quad (8)$$

A high capacitance, low ESR reduces both the output ripple and the output resistance.

The diode connecting input and output only needs to protect the device from turning on its own parasitic diode and potentially latching up. During start-up, D1 will also quickly charge up the output capacitor to VIN minus the diode drop, thereby decreasing the start-up time. Therefore, the diode D1 must have enough current carrying capability to charge the output capacitor at start-up, as well as a low forward voltage to prevent the internal parasitic diode from turning on. Instead of a using a typical Schottky diode, a Zener diode BZT52C5V6T-7 is used. The purpose of this Zener is to prevent the voltage from exceeding 2× the input voltage as a simple regulating method.

The same method is used at the input side, where the same Zener diode of the 5.6-V reverse breakdown is used to regulate the push-pull output and ensure the maximum input voltage of the charge pump LM2765 is not exceeded.

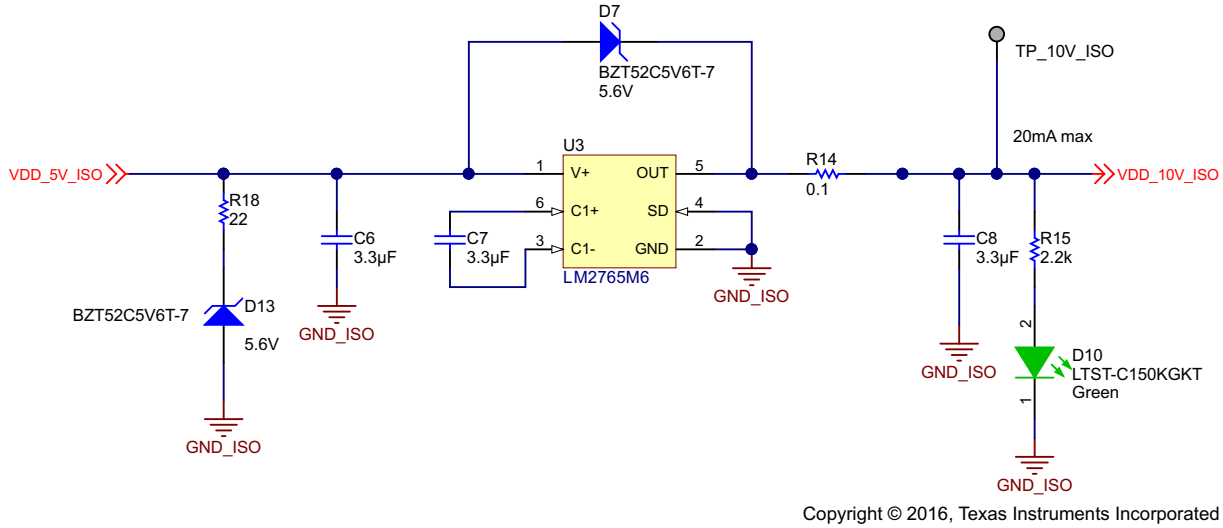

Figure 12. Charge Pump Doubler Schematic

4 Testing and Results

4.1 Test Setup

Figure 13 shows the test setup for one channel of the TIDA-00319 reference design. The Agilent E3631A dual power supply is used to power the board with the needed 3.3-V and 5-V supplies. The Agilent 33120A wave generator is used to feed the high-speed input square wave signal, using a T-junction, the same input signal is fed to the scope for triggering. Output is connected to a load using a typical twisted pair cable, with the second wire connected to the remote ground and connected to both ground and earth terminals of the TIDA-00319. Load is powered by another Agilent E3631A, which provides a voltage from 5 to 24 V. The load supply is stabilized using a local electrolytic 50-V, 330-µF capacitor. in addition to the cable capacitance of 30 pF/ft, a load capacitance is attached to the load to ground. The LeCroy Wavefurfer 454 scope is used to probe output node voltage. Load power and system power is directly monitored using the power supplies.

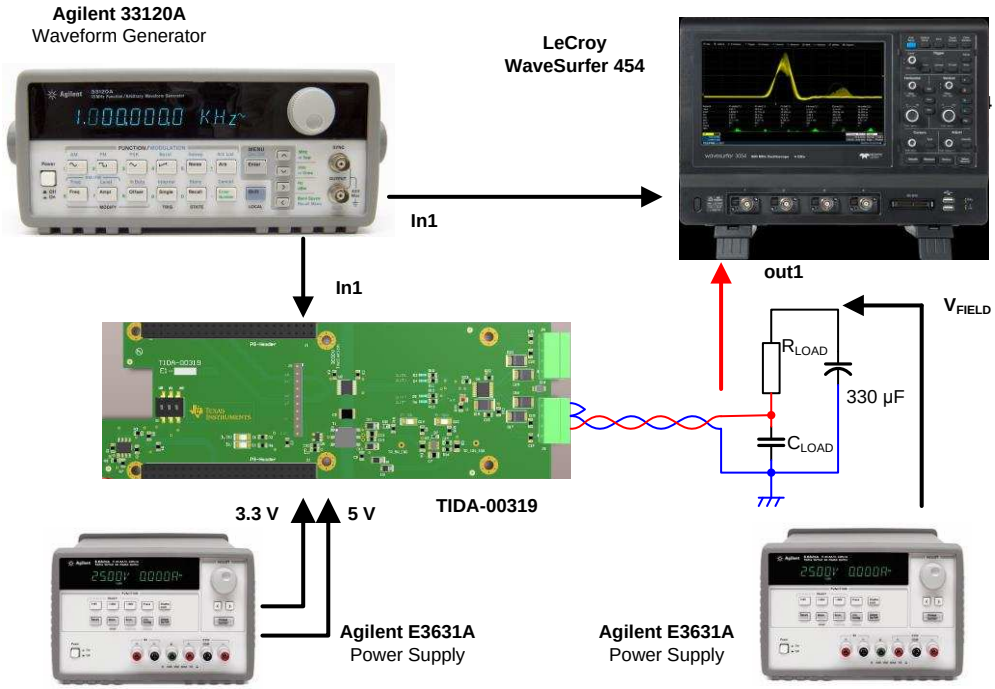

Figure 13. TIDA-00319 Test Setup

4.1.1 Test Procedure

An output waveform as well as rise and fall times, output delay, output delay variation, output high, output low levels, system, and load power are measured for different input frequencies as well as different field voltages. High field voltage is limited only to lower input frequency for limiting power of the load.

4.1.1.1 High-Speed 5-V Field Supply

For a 5-V high-speed test, the circuit in Figure 14 is used including about 15 m (50 ft) of twisted-pair cable with about 30 pF/ft of parasitic capacitance.

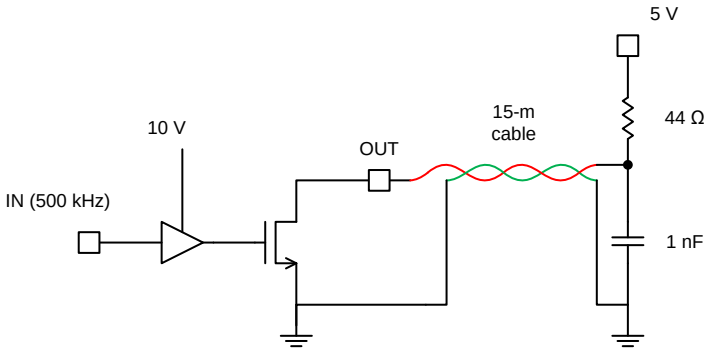

Figure 14. Test Circuit for 5-V Field Supply

Table 2 lists the test results of the 500-kHz signal input. The cable effect on the signal waveform is shown in Figure 15, which clearly shows large undershoot. Lower overshoot levels can be achieved by reducing the transition times using a higher load capacitor close to the driver. The higher low-voltage level is due to cable impedance. 400 mV is still acceptable even for the standard TTL and CMOS logic.

Table 2. Test Results at V_{FIELD} = 5 V With 15-m Cable

PARAMETER	VALUE
Backplane power consumption	5 V: 37 mA , 3.3 V: 8 mA
Field power consumption	Average current = 60 mA
Rise time 20% to 80%	93 ns
Fall time 80% to 20%	78 ns
Output low level	431 mV
Output high level	5 V
Overshoot +	1.8%
Overshoot –	3.5%

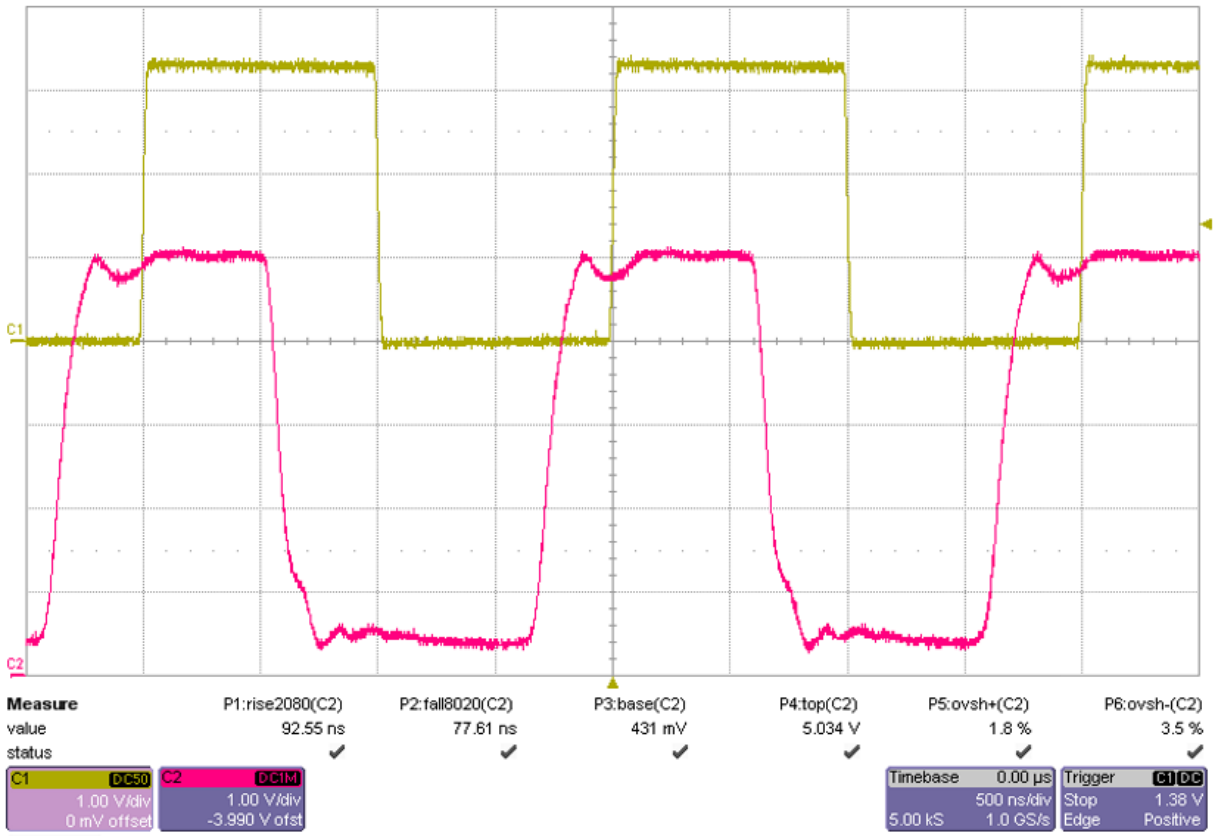

Figure 15. Output Waveform at 500 kHz With 15-m Cable

The test is repeated with the cable removed to have transition times measured. Capacitive load is also removed. Low level voltage is lower as expected and transition times are about the half of the previous test. Rise and fall times are symmetric, which shows the attached direct capacitive load is at an appropriate value.

Table 3. Test Results at V_{FIELD} = 5 V, No Cable

PARAMETER	VALUE
Rise time 20% to 80%	50 ns
Fall time 80% to 20%	47 ns
Output low level	131 mV
Output high level	5 V
Overshoot +	3.8%
Overshoot –	2.9%

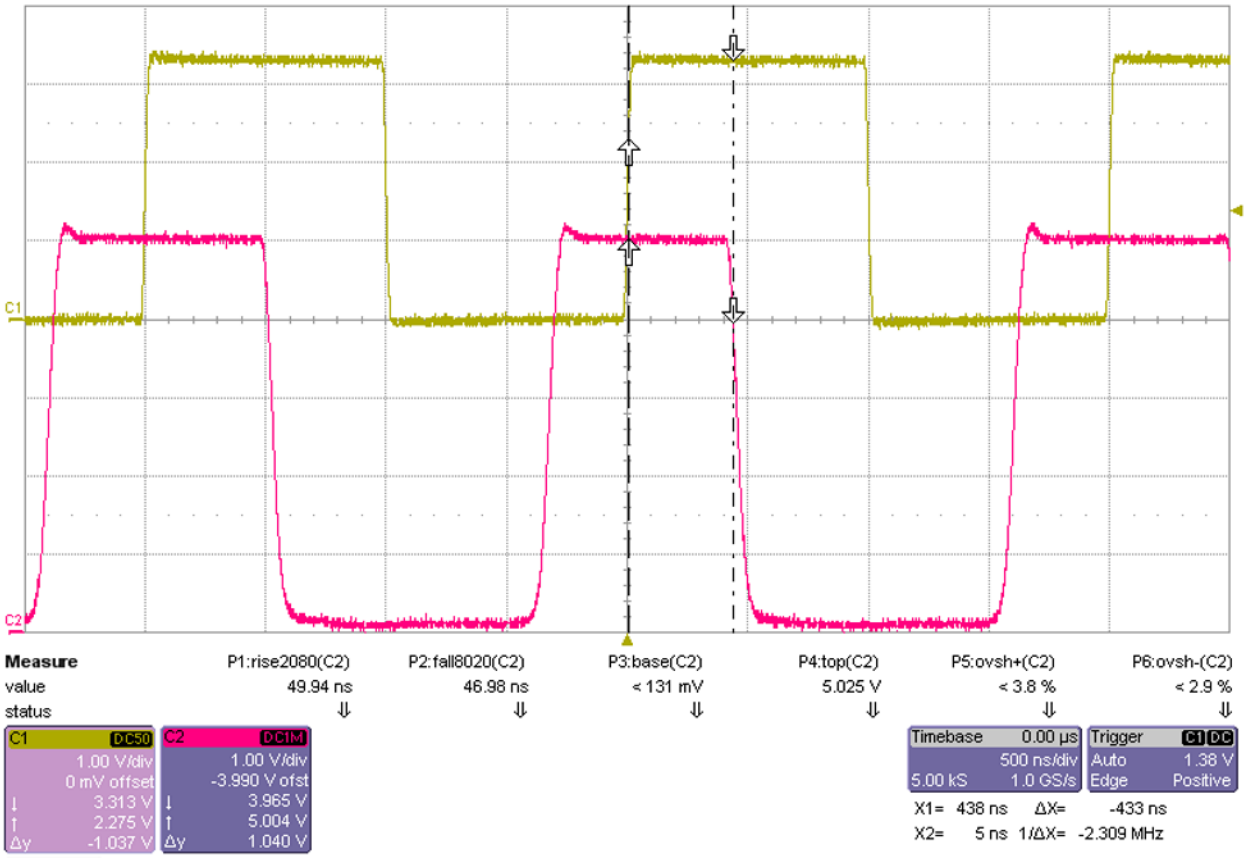

Figure 16. Output Waveform Without Cable at 500 kHz

The delay variation of the driver is shown in Figure 17. The delay itself is due to the isolator and the driver as well as external load. The delay variation, though, is solely a function of the DRV8803 driver. This is one of the limiting factors (among other factors mentioned earlier) that limits the maximum frequency of operation in the case of a single-ended driver.

Table 4. Delay Variation at V_{FIELD} = 5 V, No Cable

PARAMETER	VALUE
Rising delay	550 ns
Falling delay	430 ns
Rising delay variation	144 ns
Falling delay variation	144 ns
Minimum output duty cycle	40.5 %
Maximum output duty cycle	48.3 %

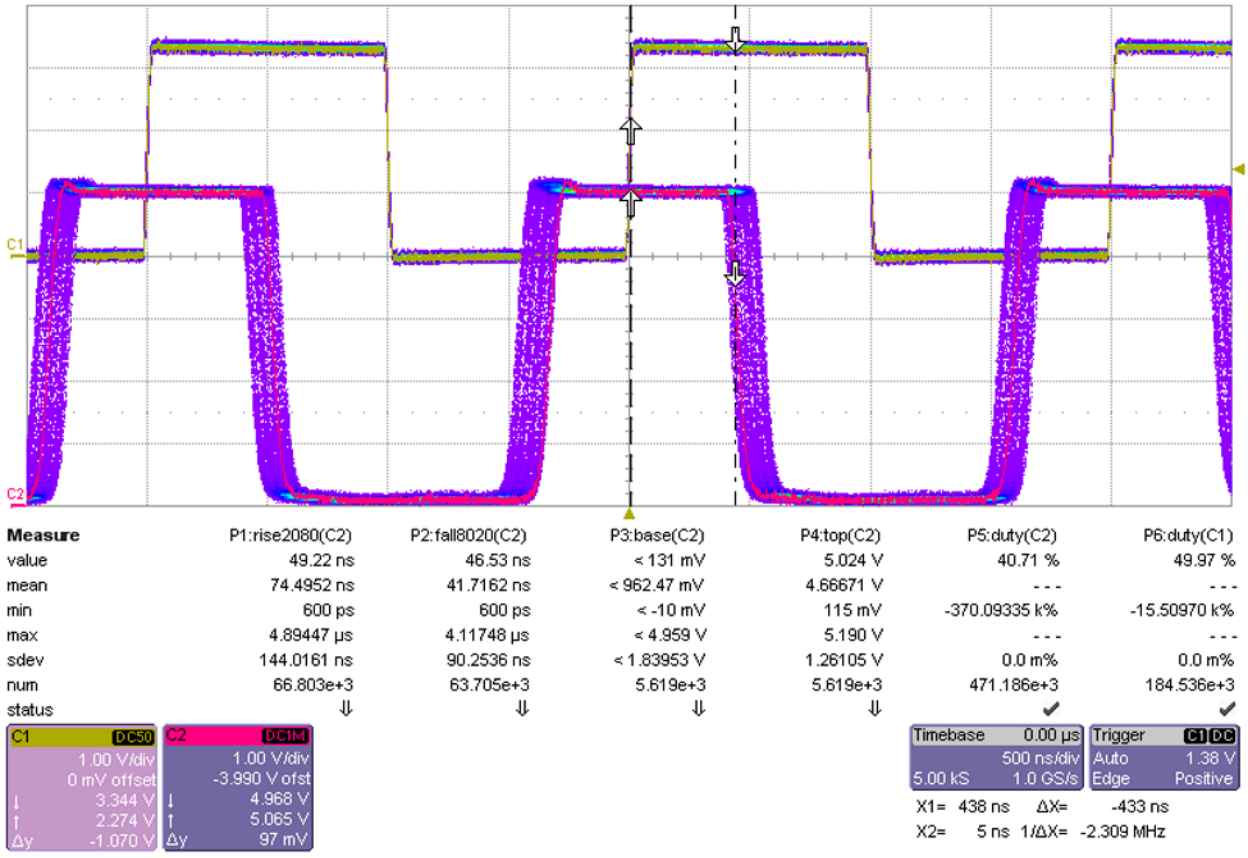

Figure 17. Delay Variation of Output Driver

4.1.1.2 24-V Field Supply Test

For the 24-V field supply voltage test, a similar circuit to the circuit in Figure 5 is used, first without a cable, and with a 220-Ω resistive load. The 200-kHz waveform proves the driver is able to work at 200 kHz with a high voltage supply.

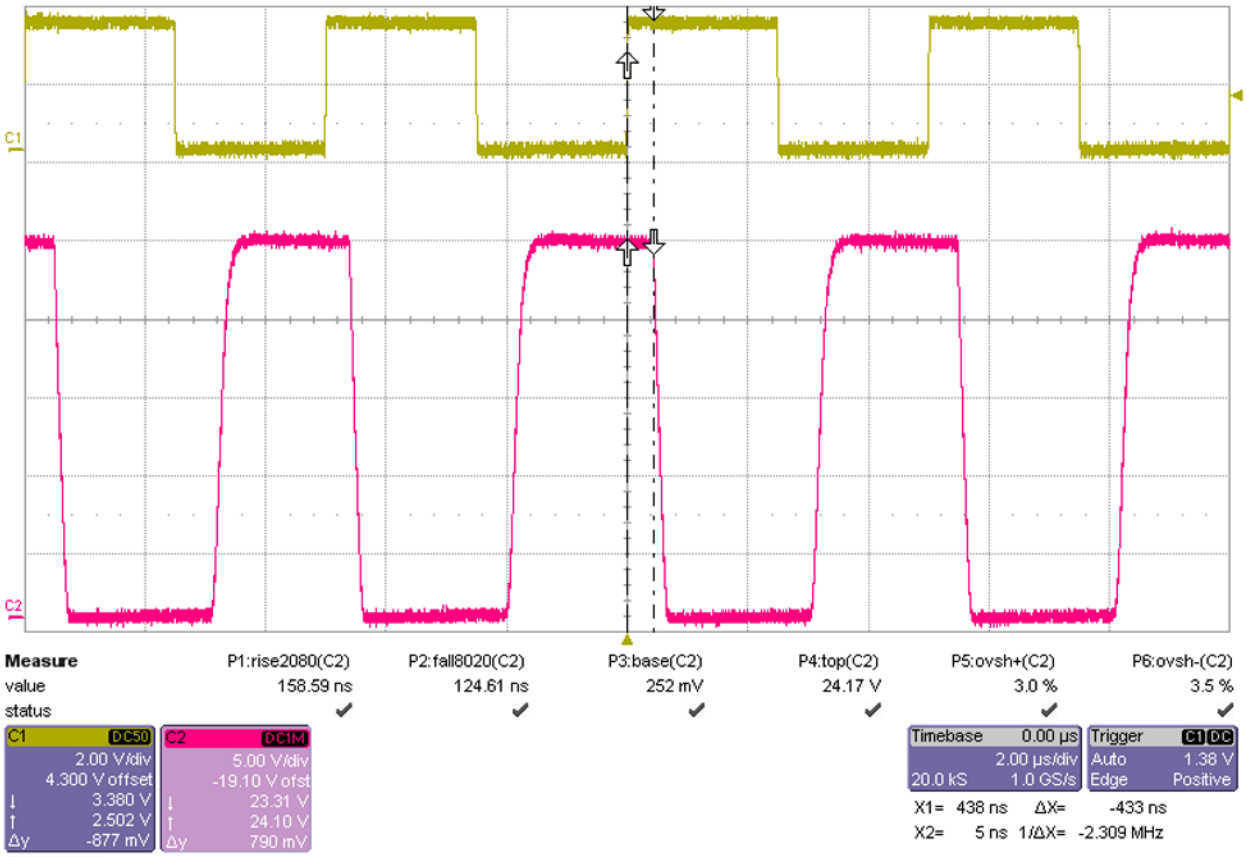

Figure 18. Output Waveform for 24-V Field Supply (No Cable)

Signal transmission artifacts start to appear when the 15-m twisted pair cable and a 1-nF capacitive load is used. The resistive load is reduced to 122 Ω in this test. The symmetry between rise and fall times diminishes, and it becomes clear that falling edge must be used for receiver detection. A large undershoot is also observed, which must be taken care of to properly operate. Finally, the low value minimum is about 600 mV, which is acceptable for a 24-V supply. Note that the waveform in Figure 19 represents a 100-kHz signal, which is quite good for 24 V. However, for the 500-kHz signal, use a 5-V supply. Consider the power rating of the external resistor for a higher voltage.

Table 5. Test Results at V_{FIELD} = 24 V, 100 kHz With 15-m Cable

PARAMETER	VALUE
Backplane power consumption	5 V: 37 mA , 3.3 V: 8 mA
Field power consumption	Average current = 100 mA
Rise time 20% to 80%	440 ns
Fall time 80% to 20%	116 ns
Output low level	623 mV
Output high level	24 V
Overshoot +	3%
Overshoot –	23%

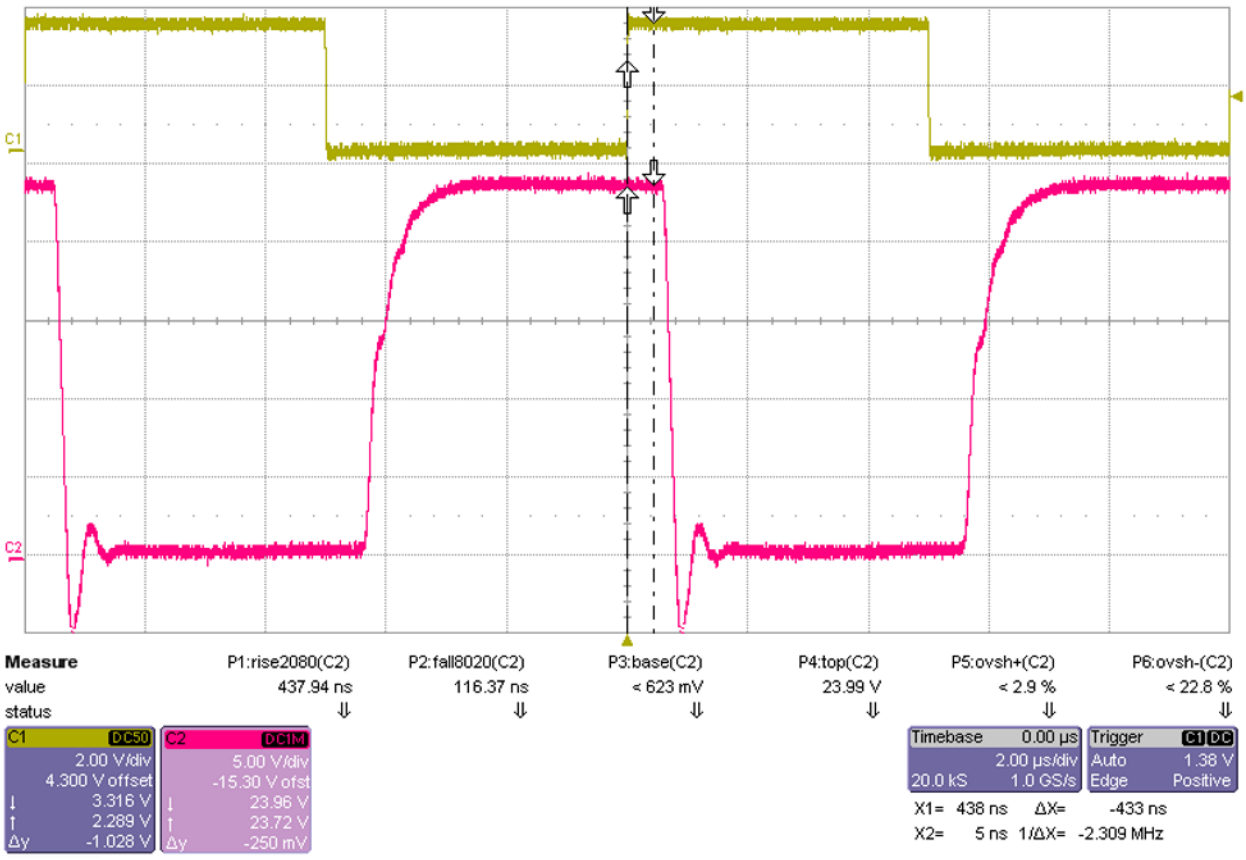

Figure 19. Output Waveform for 24 V Supply (With Cable)

5 Design Files

5.1 Schematics

To download the Schematics for each board, see the design files at TIDA-00319.

5.2 Bill of Materials

To download the Bill of Materials for each board, see the design files at TIDA-00319.

5.3 Layout Prints

To download the Layout Prints for each board, see the design files at TIDA-00319.

5.4 Altium Project

To download the Altium project files for each board, see the design files at TIDA-00319.

5.5 Gerber Files

To download the Gerber files for each board, see the design files at TIDA-00319.

5.6 Assembly Drawings

To download the Assembly Drawings for each board, see the design files at TIDA-00319.

6 About the Author

AHMED NOEMAN is a system engineer at Texas Instruments Germany developing reference design solutions for industrial applications. Ahmed has many years of experience in analog and RF design, AMS modeling, and verification as well as application and system engineering in a wide range of fields including RF transceivers, clocks and PLLs, memory systems, and others. Ahmed received his BSC and MSEE from Ain Shams University, Egypt.

Revision A History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (August 2016) to A Revision	Page
• Changed from preview draft	1

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