TI Designs

Operating a Low-Power, High-Performance PLL From a Single-Cell Battery Using a Buck-Boost Converter

Description

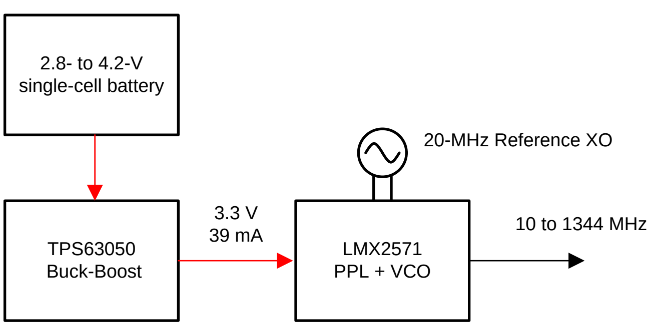
The TIDA-00886 consists of a low-power, high-performance, wideband PLLatinum™ RF synthesizer being powered from a buck-boost converter. The LMX2571, a low-power RF synthesizer, will be powered by a single-cell battery using the TPS63050, a DC-DC buck-boost converter. The TIDA-00886 shows that the DC-DC has a small to negligible effect on the phase noise performance of the LMX2571.

The LMX2571 is very popular in two-way radio applications and handheld test and measurement equipment. Although this is a low-current consumption device, 39 mA in synthesizer mode (internal VCO) and 9 mA in PLL mode (external VCO), efficiency is critical for battery operated applications.

Resources

TIDA-00886	Design Folder
LMX2571	Product Folder
TPS63050	Product Folder

TI E2E™ Community — ASK Our E2E Experts



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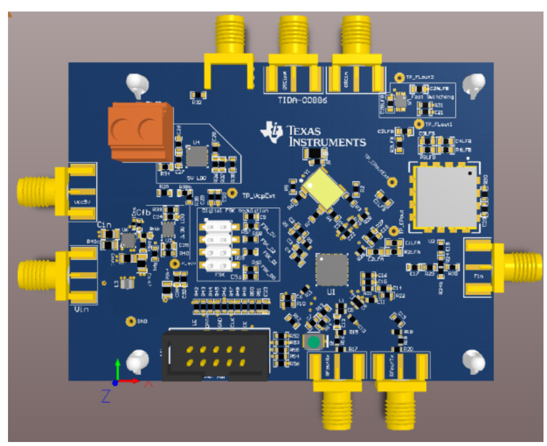
Features

- 3.3-V DC Buck-Boost to Power LMX2571 From Single-Cell Battery
- 2.5- to 5.5-V Input Voltage Range
- TPS63050 Can Source up to 0.5 A in Boost Mode, 1 A in Buck Mode
- Efficiency > 90% in Boost Mode and > 95% in Buck Mode
- Any Frequency From 10 to 1344 MHz
- Low Phase Noise and Spurs
  – –123 dBc/Hz at 12.5-kHz Offset at 480 MHz
  – –145 dBc/Hz at 1-MHz Offset at 480 MHz
  – –231 dBc/Hz Normalized PLL Noise Floor

Applications

- Duplex Mode Digital Professional Two-Way Radio
- Handheld Test and Measurement Equipment
- Wireless Microphone



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1 System Overview

1.1 System Description

The TIDA-00886 is a low-power, high-performance, wideband PLLatinum™ RF synthesizer. The LMX2571 will be powered by a single-cell battery using the TPS63050, a DC-DC buck-boost converter. The voltage of the battery will be in the range of 2.8 to 4.2 V. Therefore, a buck-boost converter that has capabilities to step up or down the voltage is needed. There are several other advantages of using DC-DC converters. High efficiency is critical in battery operated applications to maximize battery life. Another advantage of efficiency is that most of the power loss is dissipated in heat. It can be impractical to use a heat sink when trying to keep solution size at a minimum.

The TIDA-00886 demonstrates that using a DC-DC will have negligible effect on the performance of the low-power synthesizer. Typically, a low-noise LDO is considered for RF PLL applications. LDOs do not have good efficiency and cannot step up the voltage as needed for this application. Selecting the right output capacitance for the DC-DC regulator is critical to maintain a lower output voltage ripple, which might affect the performance of the synthesizer.

This TI Design can be controlled from any Windows® PC through a USB2ANY SPI controller. A low-cost microcontroller or DSP can also program the synthesizer.

1.2 Key System Specifications

Table 1. Key System Specifications

PARAMETER	SPECIFICATION
Output frequency range	10 to 1344MHz
Optional input reference clock frequency	10 to 150MHz
Input voltage range	2.5 to 5.5 V
DC-DC switching frequency	2.5 MHz
DC-DC I_{OUT} max	1 A in buck mode 0.5 A in boost mode
Onboard XO	20 MHz

1.3 Block Diagram

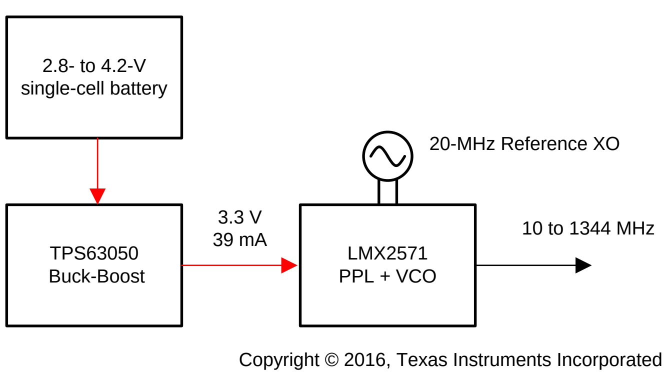

Figure 1. TIDA-00886 Block Diagram

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1.4 Highlighted Products

1.4.1 LMX2571

The LMX2571 is a low-power, high-performance, wideband PLLatinum™ RF synthesizer that integrates a delta-sigma fractional N PLL, multiple core voltage-controlled oscillator (VCO), programmable output dividers and two output buffers. The VCO cores work up to 5.376 GHz resulting in continuous output frequency range of 10 to 1344 MHz.

This synthesizer can also be used with an external VCO. To that end, a dedicated 5-V charge pump and an output divider are available for this configuration.

A unique programmable multiplier is also incorporated to help improve spurs, allowing the system to use every channel even if it falls on an integer boundary.

The output has an integrated SPDT switch that can be used as a transmit and receive switch in FDD radio application. Both outputs can also be turned on to provide two outputs at the same time.

The LMX2571 supports direct digital FSK modulation through programming or pins. Discrete level FSK, pulse shaping FSK, and analog FM modulation are supported.

A new FastLock technique can be used allowing the user to step from one frequency to the next in less than 1.5 ms even when an external VCO is used with a narrow band loop filter.

The LMX2571 has low current consumption: 39-mA typical synthesizer mode (with internal VCO) and 9-mA typical PLL mode (with external VCO). This makes it ideal for handheld test equipment and battery operated applications.

1.4.2 TPS63050

The TPS6305x family of devices is a high-efficiency, low-quiescent current buck-boost converter, suitable for applications where the input voltage is higher or lower than the output.

Continuous output current can go as high as 500 mA in boost mode and as high as 1 A in buck mode. The maximum average current in the switches is limited to a typical value of 1 A. The TPS6305x family of devices regulate the output voltage over the complete input voltage range by automatically switching between buck or boost mode depending on the input voltage, ensuring seamless transition between modes.

The buck-boost converter is based on a fixed-frequency, pulse-width-modulation (PWM) controller using synchronous rectification to obtain the highest efficiency. At low load currents, the converter enters power save mode to maintain high efficiency over the complete load current range.

The power saving mode (PFM)/PWM pin allows the user to select between automatic-PFM/PWM mode operation and forced-PWM operation. During PWM mode, a fixed-frequency of typically 2.5 MHz is used. The output voltage is programmable using an external resistor divider or is fixed internally on the chip. The converter can be disabled to minimize battery drain. During shutdown, the load is disconnected from the battery. The device is packaged in a 12-pin DSBGA and in a 12-pin HotRod package.

1.4.3 Programming Interface

SPI is used to program the LMX2571. See the LMX2571EVM user guide (SNAU176) to use the Code Loader GUI to program the LMX2571 using USB2ANY.

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2 System Design Theory

The system consists of the LMX2571, a low-power, high-performance, wideband PLLatinum™ RF synthesizer that integrates a delta-sigma fractional N PLL, multiple core VCO, programmable output dividers, and two output buffers. The VCO cores work up to 5.376 GHz resulting in continuous output frequency range of 10 to 1344 MHz.

The LMX2571 input voltage 3.3 V at 39 mA in synthesizer mode (internal VCO). The single-cell battery voltage will be from 2.8 to 4.2 V at the input of the DC-DC regulator. The output of the regulator will be 3.3 V to power the LMX2571. The TPS63050 can source up to 1 A in buck mode and 0.5 A in buck mode.

2.1 Frequency Synthesizer

The LMX2571 needs a reference frequency provided from an XO. The input frequency must be in the range of 10 to 150 MHZ. The onboard XO could be used as the input frequency. If the XO is powered from the DC-DC, a 47-µF decoupling capacitor between the XO V_{CC} pin and ground is recommended. The output frequency range is 10 to 1344 MHz.

The LMX2571 supports direct digital FSK modulation through programming or pins. Discrete level FSK, pulse shaping FSK, and analog FM modulation are supported.

The RF output buffer type is in push-pull configuration for the TIDA-00886. See Section 8.1.8: RF Output Buffer Type in the LMX2571 datasheet for more details (SNAS654).

2.2 Buck-Boost Regulator

The TPS63050 can take an input voltage of 2.5 to 5.5 V. The output voltage is in the range of 2.5 to 5.5 V. For the TIDA-00886, the output voltage of the regulator was designed to be 3.3 V to power the LMX2571 synthesizer. The switching frequency of the DC-DC regulator is 2.5 MHz.

The TPS63050 has two modes of operation, PFM and PWM. Pin 6 enables PFM mode. If pin 6 is tied to ground, it is automatically enabled. If pin 6 is tied to V_{IN} or 3.3 V, forced PWM is enabled. If PFM is enabled, the device enters PFM mode automatically if the load current is below a certain threshold, in this case, 350 mA. PFM mode causes the switching frequency to fallback and increase the output voltage ripple from 30 to 50 mV (with a 10-µF output capacitor); this mode of operation has a significant negative impact on the performance of the LMX2571 if the current is below 350 mA in PFM. There is no upper limit for the output capacitance value. Larger capacitors cause lower output voltage ripple as well as lower output voltage drop during load transients. At least a 20-µF capacitance at the output of the regulator is suggested.

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3 Getting Started Hardware and Firmware

3.1 Hardware

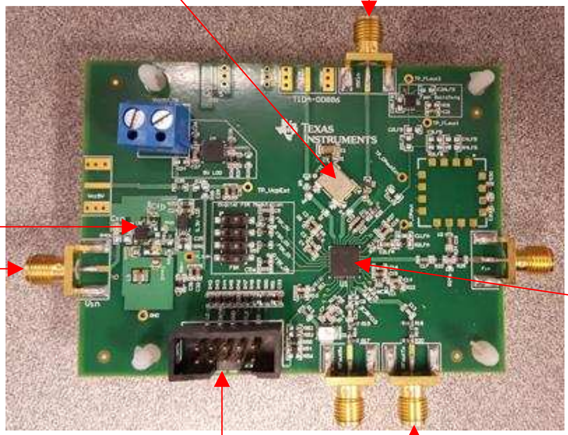

Figure 2. TIDA-00886 Top View of PCB

3.1.1 Power

1. Operate using the TPS63050 buck-boost (default).
   (a) Apply a voltage from 2.5 to 5.5 V at V_{IN}.
   (b) Do not populate R38, R39b R40, R40d, C31, and C32 with this configuration.
   (c) Populate R40c and R39.
2. Apply 3.3 V at V_{IN} SMA.
   (a) Do not populate R40c, R40d, R39b, and R38.
   (b) Populate C31, C32, and R39.
3. Apply a voltage higher than 5 V to VCC5VSMA or VCC5V_TB.
   (a) Use regulator U4 to get 5 V at VCC5V_TP.
   (b) Use regulator U3 to get 3.3 V for VCC3V_TP.
4. Apply 5V to Vcc5V SMA.
   (a) Connect resistors to get this same voltage at VCC5V_TP.
   (b) Use regulator U3 to get 3.3 V for VCC3V_TP.
   (c) Do not populate R34, R39b, R39, R40c, and R40d with Option 2.
   (d) Populate R35, R33, and R40.

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3.1.2 Input Signal

- Option 1 (default): The onboard crystal oscillator is powered on and outputs a 20-MHz signal to OSCin (pin34) of the device input.
- Option 2: Power supply resistor (R1) should be removed (Powers XO) and resistor R3 moved to position R2, which routes the input signal from the OSCin SMA connector instead of the onboard oscillator.

NOTE: If using a noisy signal source such as a signal generator, be aware that this can dominate close-in phase noise.

3.1.3 Output Signal

Connect RFoutRx or RFoutTx to a phase noise analyzer. Connect a 50-Ω termination on the unused output if using only single-end.

3.2 Firmware

3.2.1 Download Code Loader

1. Download the Code Loader 4 software from TI.com.
2. To start the software, open Codeloader4.exe from the installed directory.

3.2.2 Getting Started With Code Loader

1. After completing the installation, start the software.

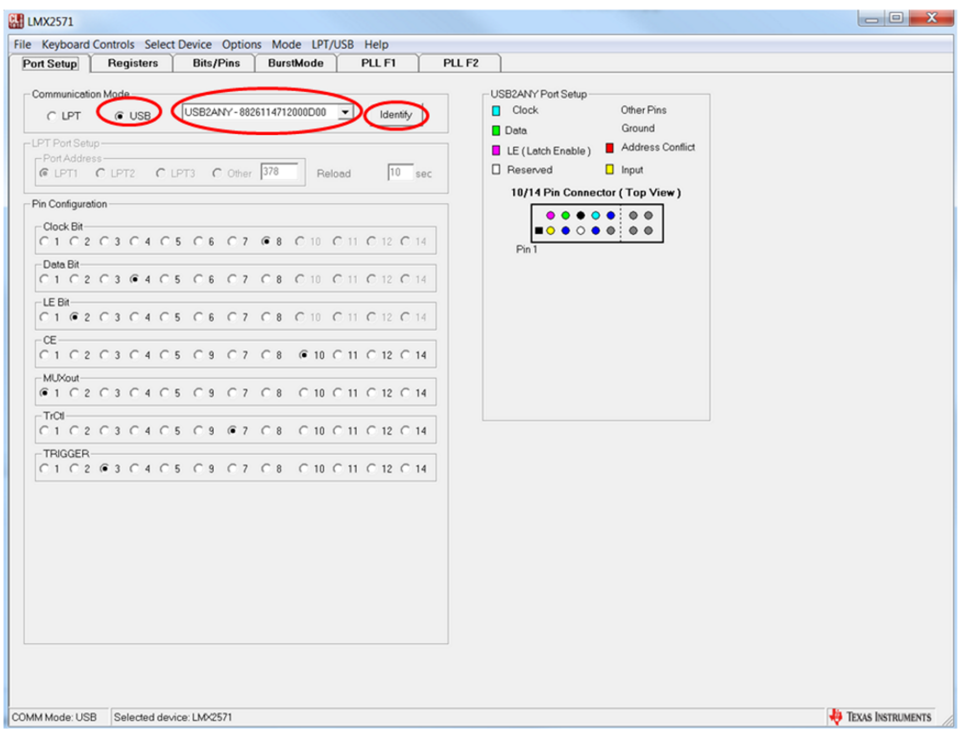

Figure 3. Getting Started With Code Loader

2. Click on USB if using USB2ANY. Click on identify, check if the adapter on USB2ANY is blinking and it is communicating with the PC.
3. Select the LMX2571 device from the *Select Device* menu on Code Loader.

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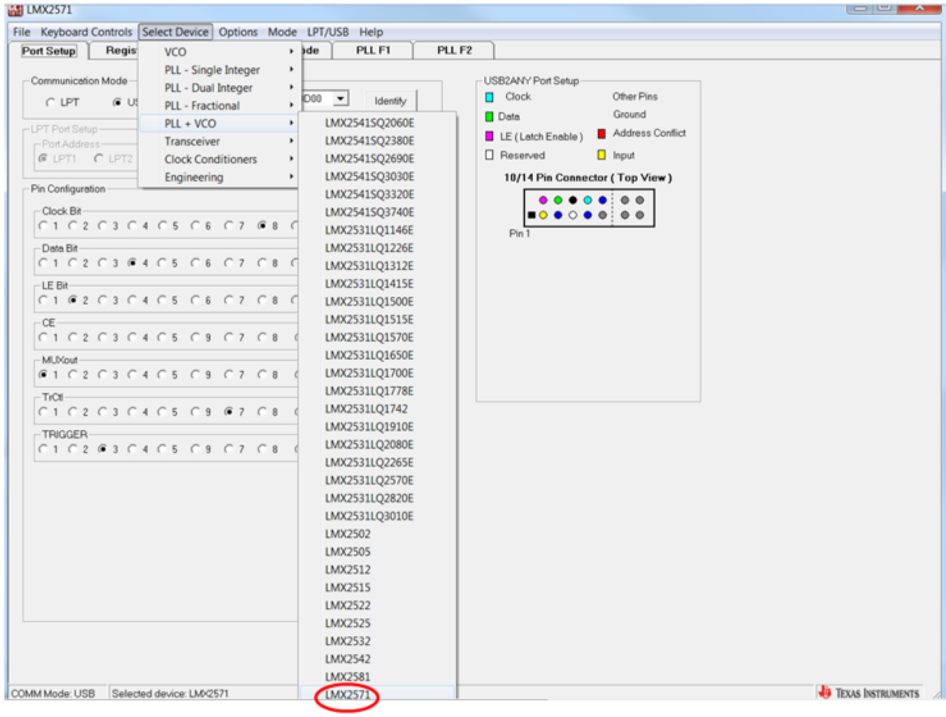

Figure 4. Selecting LMX2571 in Code Loader

4. Click on the *Mode* menu and select the default mode. For the test results, a 480-MHz output frequency was used.

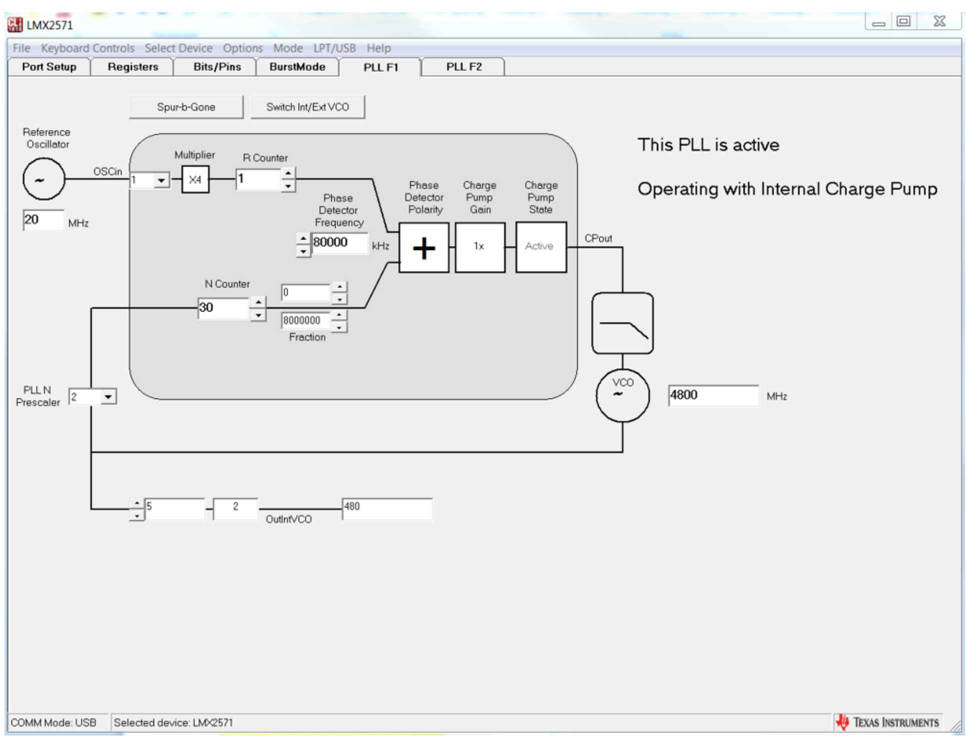

Figure 5. LMX2571 PLL F1 Tab Settings

A text file with register values will be provided. These values can be easily imported into Code Loader. To download the software files for this reference design, see the link at http://www.ti.com/tool/TIDA-00886.

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4 Testing and Results

4.1 Test Setup

Figure 6 shows the test setup used in the lab to test the reference design and make the measurements in Section 4.2.

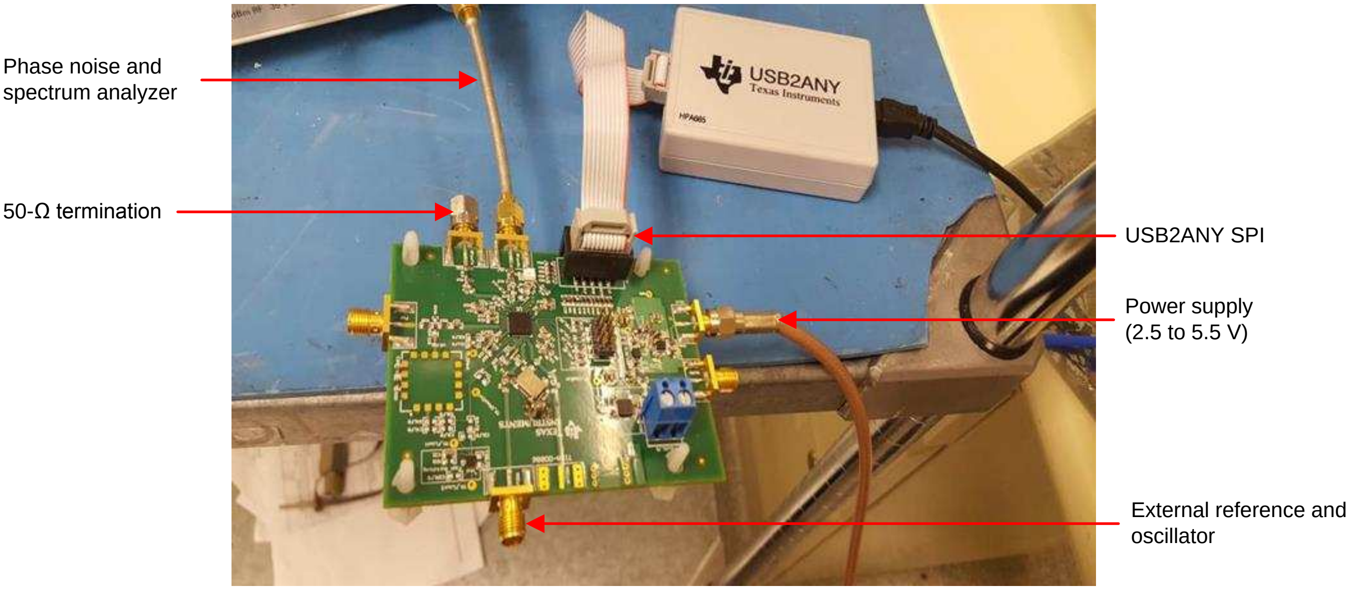

Figure 6. Test Setup Used in Lab For TIDA-00886

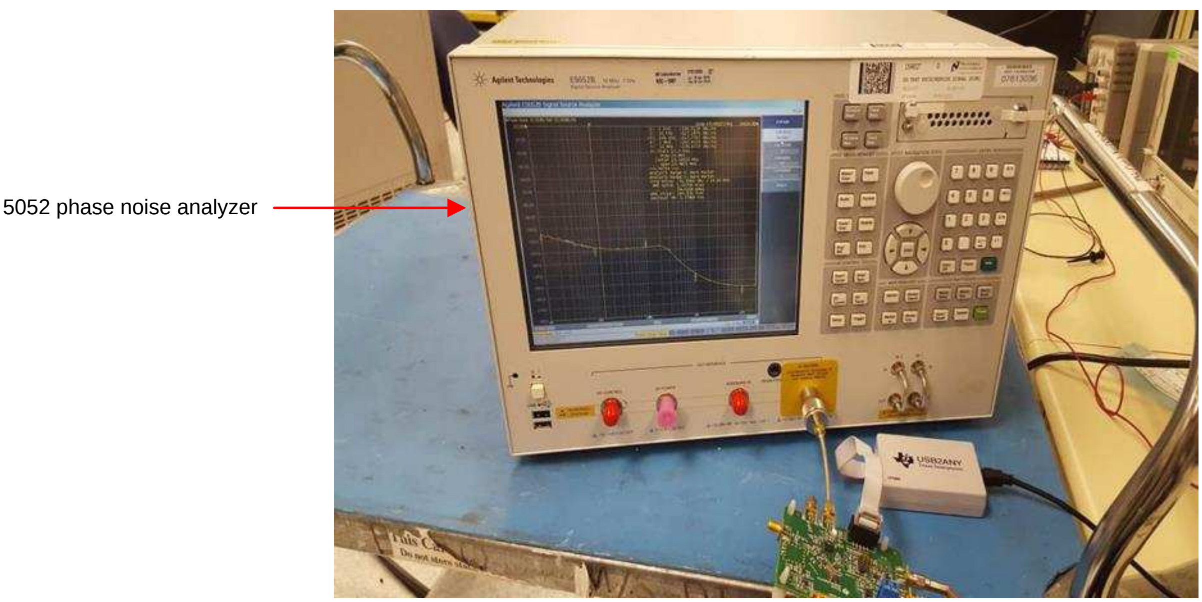

Figure 7. E5052 Phase Noise Analyzer

4.2 Test Data

The test results were taken using the E5052 Phase Noise analyzer.

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Table 2. Phase Noise Performance of LMX2571 in Different Regulator Modes

OFFSET FREQ	PHASE NOISE (dBc/Hz)		
	3.3 V	REGULATOR ON BUCK MODE	REGULATOR ON BOOST MODE
1 kHz	–103.66	–104.14	–102.91
10 kHz	–116.94	–117.23	–116.25
100 kHz	–117.68	–117.65	–117.67
1 MHz	–142.38	–142.38	–142.39
10 MHz	–155.84	–156.18	–155.64

4.2.1 Results in Boost Mode

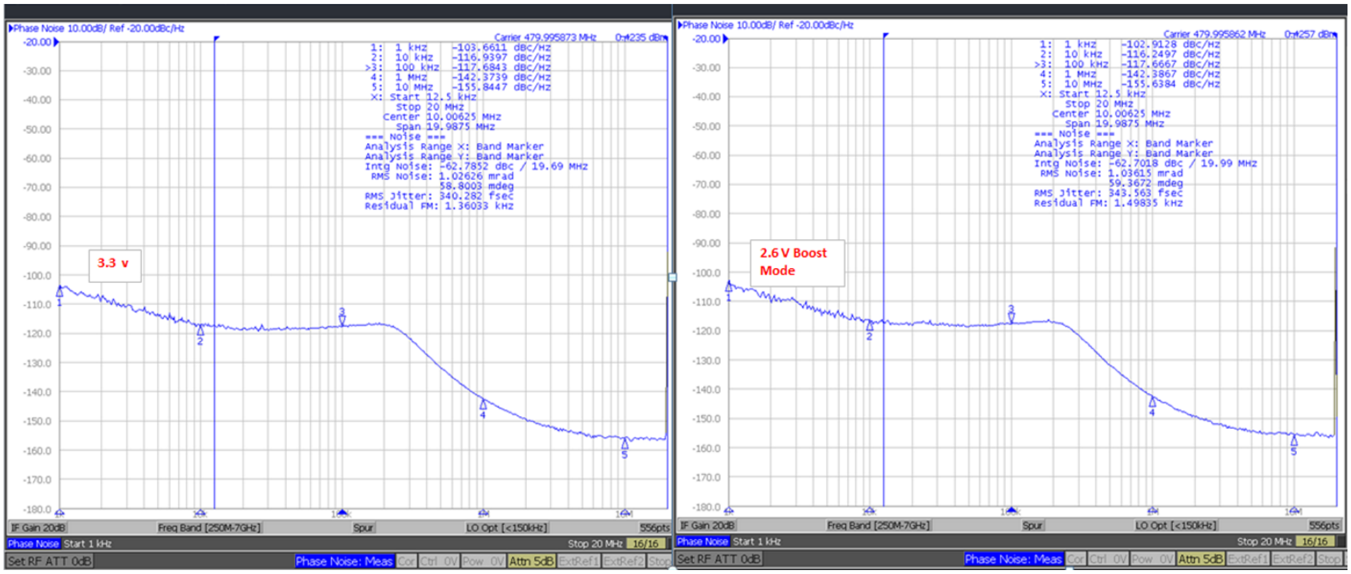

Figure 8. Phase Noise Performance in Boost Mode

4.2.2 Results in Buck Mode

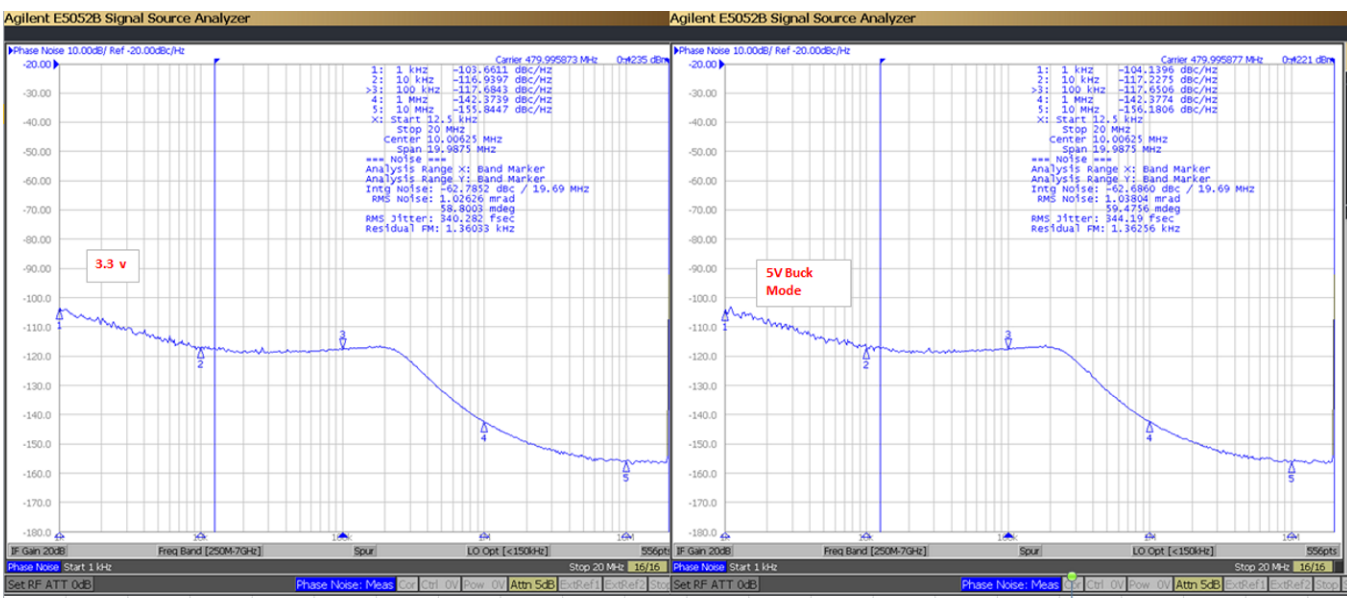

Figure 9. Phase Noise Performance in Buck Mode

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4.2.3 PWM Mode versus PFM Mode at Light Loads

If PFM is enabled, the device enters PFM mode automatically if the load current is below a certain threshold, in this case 350 mA. PFM mode causes the switching frequency to fallback and increase the output voltage ripple from 30 to 50 mV (with a 10-µF output capacitor), this mode of operation has a significant negative impact on the performance of the LMX2571 if the current is below 350 mA in PFM. PWM is recommended when using the LMX2571 unless the total load will be above 350 mA.

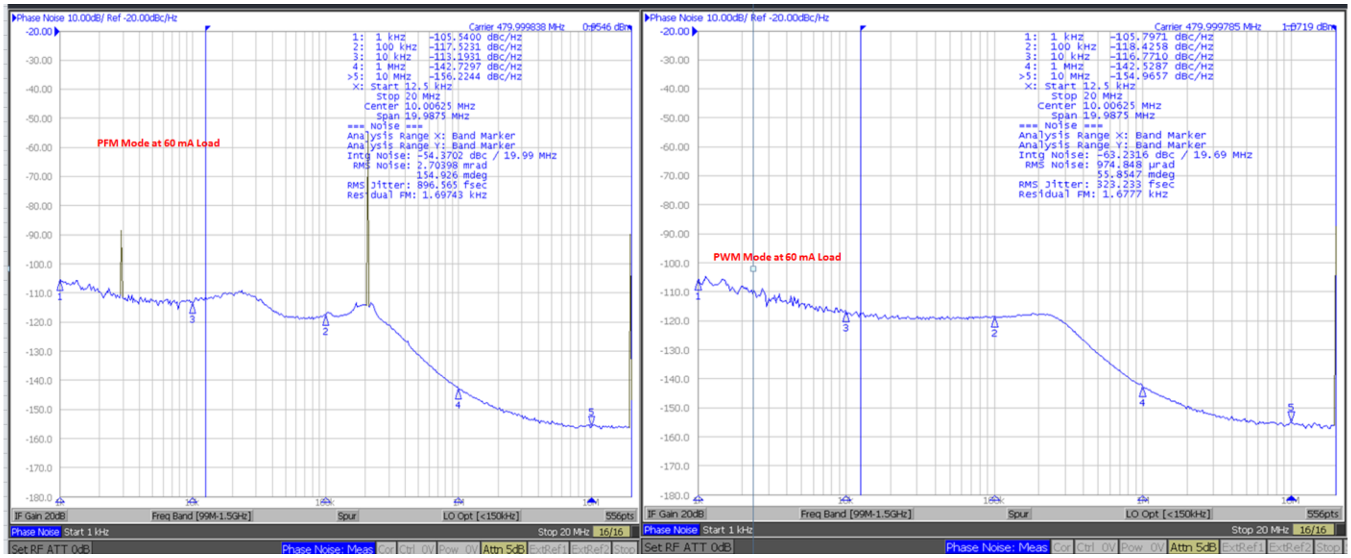

Figure 10. PWM versus PFM at Light Loads

4.2.4 Using a Ferrite Bead to Mitigate Switching Frequency Spur

DC-DC regulators may affect the spurious performance of the LMX2571. Using a ferrite bead at the output of the DC-DC will help mitigate spurs related to the switching frequency or other noise in the system.

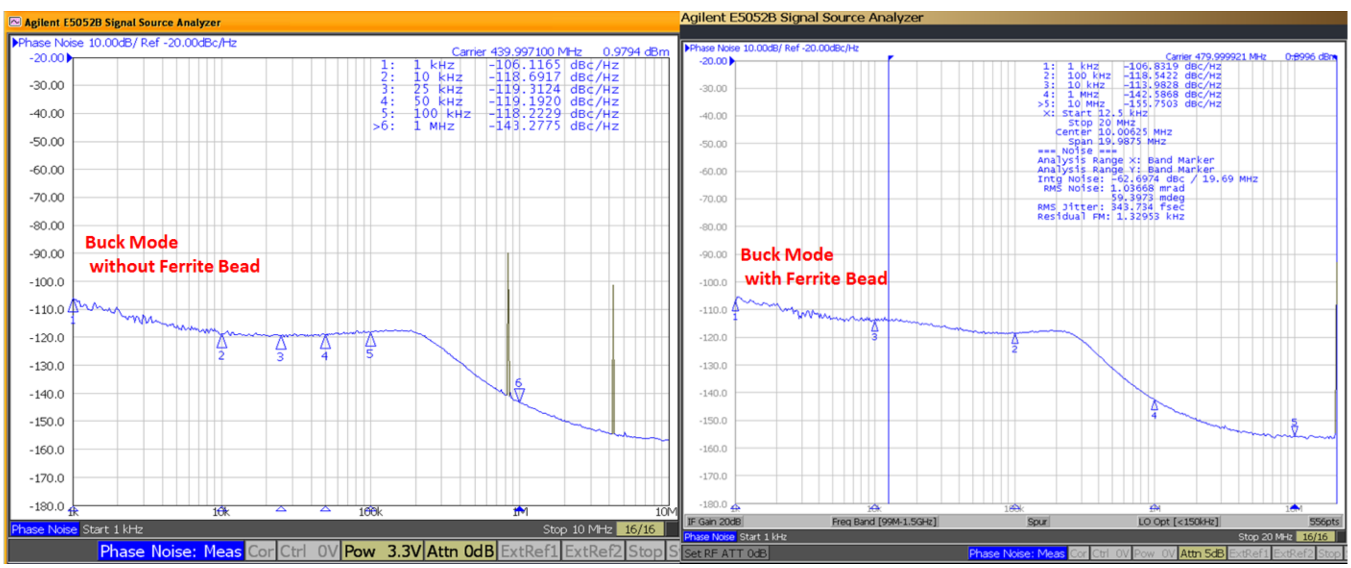

Figure 11. Spur Mitigation Using a Ferrite Bead

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5 Design Files

5.1 Schematics

To download the Schematics for each board, see the design files at: TIDA-00886.

5.2 Bill of Materials

To download the Bill of Materials for each board, see the design files at TIDA-00886

5.3 PCB Layout Recommendations

5.3.1 Board Stackup Information

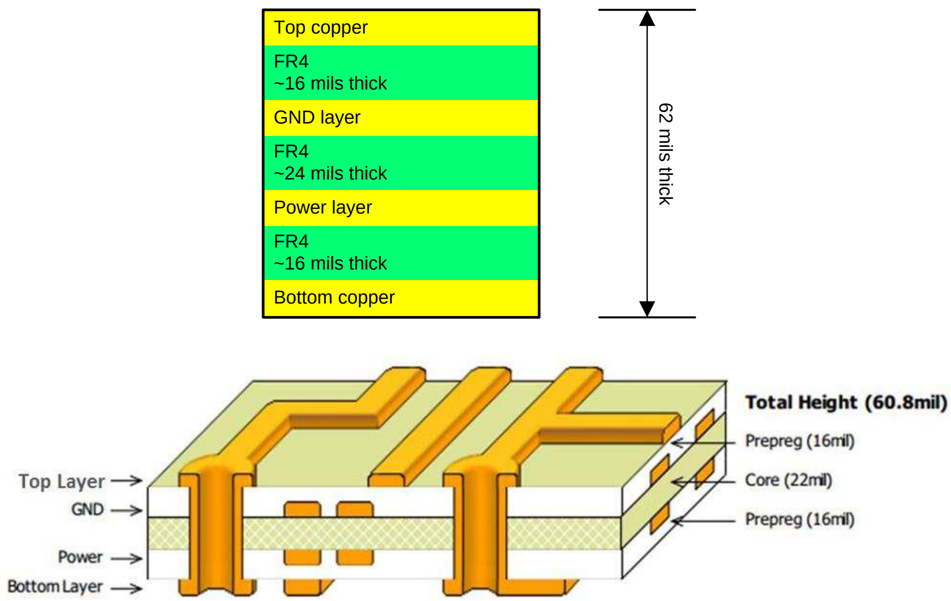

Figure 12. TIDA-00886 Layer Stackup Information

FR4 material was chosen because of convenience, availability, and cost.

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5.3.2 DC-DC Regulator Guidelines

The PCB layout is an important step to maintain the high performance of the TPS6305x devices.

- Place input and output capacitors as close as possible to the IC. Keep traces short. Routing wide and direct traces to the input and output capacitor results in low-trace resistance and low parasitic inductance.
- Use a common-power GND.
- The sense trace connected to FB is signal trace. Keep these traces away from L1 and L2 nodes.
- For the HotRod package option, add a capacitor between FB node and ground to filter ground noise and to match efficiency results documented in the TPS63050 datasheet (SLVSAM8) .

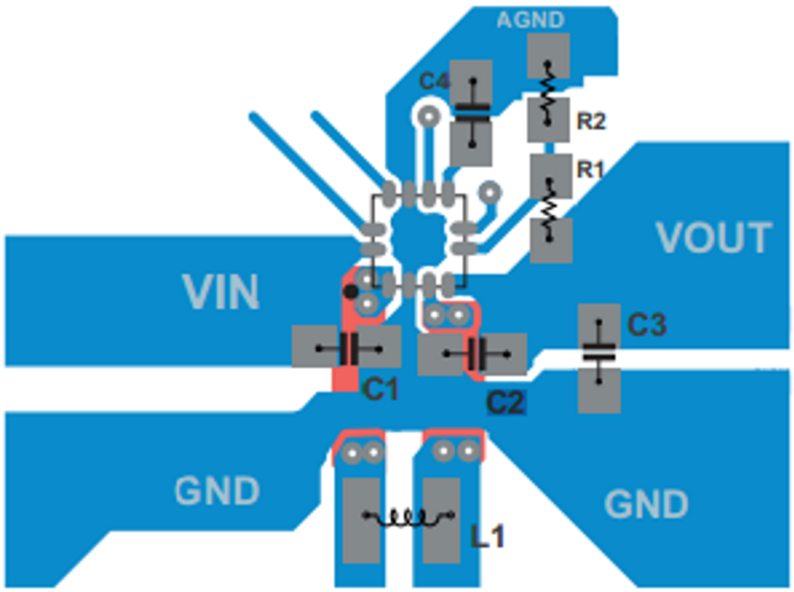

Figure 13. TPS63050 Layout Guidelines

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5.3.3 Frequency Synthesizer Guidelines

See EVM instructions EVM instructions for details. In general, the layout guidelines are similar to most other PLL devices. The followings are some guidelines specific to the device.

- It may be beneficial to separate main ground and OSCin ground, crosstalk spurs might be reduced.
- When using FSK I2S mode on this device, take care to avoid coupling between the I2S clock and any of the PLL circuiI2S clock and any of the PLL circuit.

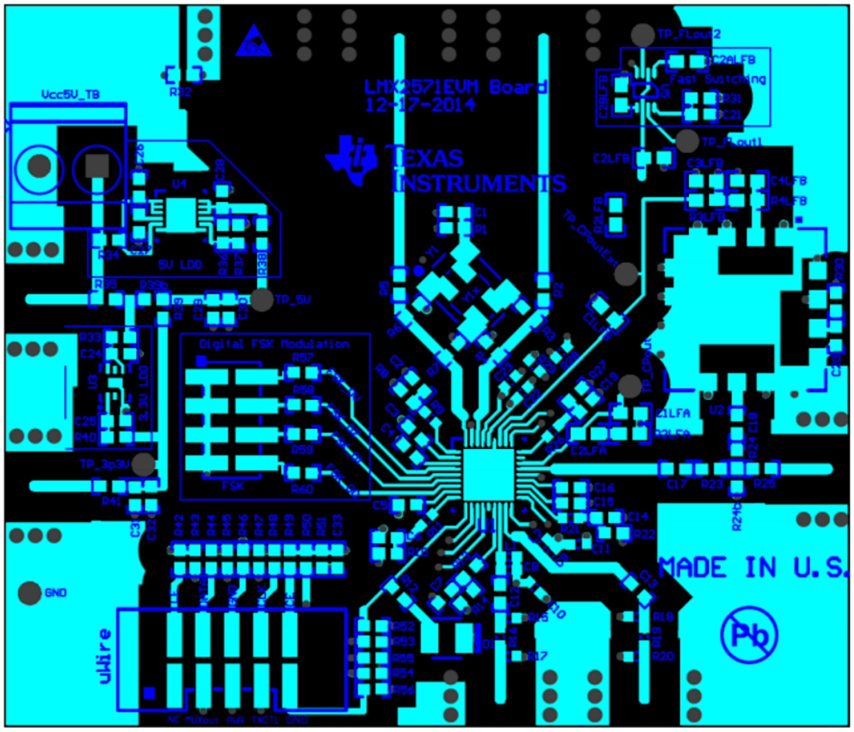

Figure 14. LMX2571 Layout Example

5.3.4 Layout Prints

To download the layer plots, see the design files at TIDA-00886.

5.4 Gerber Files

To download the Gerber files, see the design files at TIDA-00886.

5.5 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-00886.

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6 Software Files

To download the software files for this reference design, please see the link at TIDA-00886.

7 References

1. Texas Instruments, *LMX2571 Low-Power, High-Performance PLLatinum™ RF Synthesizer with FSK Modulation*, LMX2571 Datasheet (SNAS654)
2. Texas Instruments, *LMX2571 User's Guide* (SNAU176)
3. Texas Instruments, *TPS6305x Single Inductor Buck-Boost With 1-A Switches and Adjustable Soft Start*, TPS63050 Datasheet (SLVSAM8)
4. Texas Instruments, *TPS63050 User's Guide* (SLVU806)
5. Texas Instruments, WEBENCH® Design Center http://www.ti.com/webench

8 About the Author

JULIAN DI MATTEO is an applications engineer at Texas Instruments, who works for the Frequency Control Products product line.

Special thanks go to **NOEL FUNG** for his support for this reference design.

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Revision A History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (September 2016) to A Revision	Page
• Changed from preview draft	1

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