TI Designs
AC-Coupled RS-485

TEXAS INSTRUMENTS

Design Overview

This reference design details AC-coupling of RS-485 signals. Although these signals are typically DC-coupled, using AC-coupling has several advantages. AC-coupling allows transceivers to operate with large common-mode offsets, enabling long-distance communication without routing an additional ground wire. AC-coupling also protects the transceivers against high-voltage DC faults (for example, if the differential bus is shorted to a power supply). This protection is useful in industrial applications that require data transfers across long distances with a minimum number of wires.

Design Resources

ASK Our E2E Experts

Design Features

- Functional Isolation of RS-485 Allows Large Ground-Potential Differences Between Nodes
- Protection Against Short to Batteries or Power Supplies
- Supports Wide Range of Data Rates Without Protocol Overhead

Featured Applications

- RS-485 Repeaters
- E-Meters
- Industrial Automation
- Security and Surveillance Equipment
- Encoders and Decoders
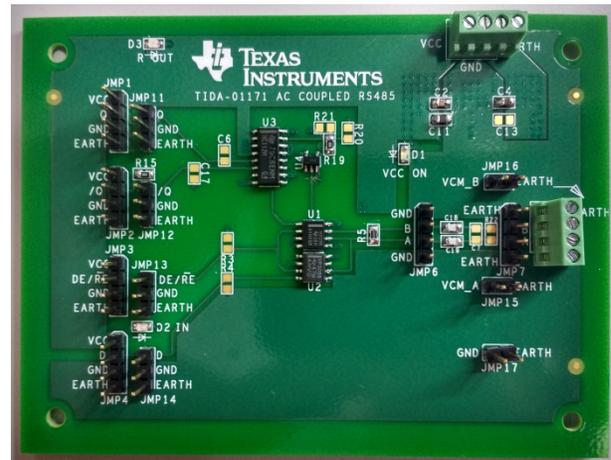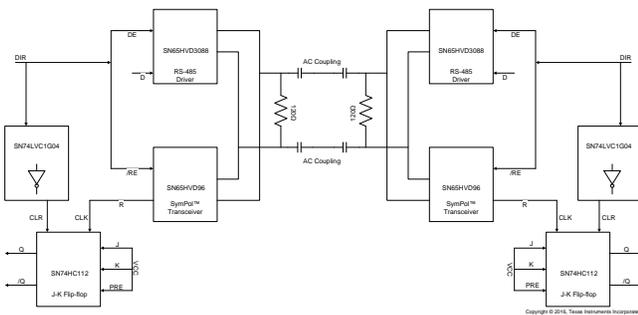
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1 Key System Specifications

The reference design can be applied to any application that uses RS-485 signaling, but it is particularly applicable to communication links that require the transfer of data over long distances or require protection against high voltages on the RS-485 bus. AC-coupling allows the different nodes on a network to operate on independent voltage domains (with independent ground references) and removes restrictions on DC common-mode voltage variations that are typically present in RS-485 systems.

A key component in this reference design is the AC-coupling capacitor. Although the capacitance does not need to be high, the voltage rating must be enough to protect against the maximum DC voltage that is expected on the bus. For example, if the system must withstand a short to a 48-V power supply, a capacitor rating of 60 V or higher is required.

This reference design operates at any standard RS-485 data rate and does not require additional protocol, encoding, or modulation. However, the benefits of this topology are primarily at lower rates (under 1 Mbps). For high data rates, it may be possible to AC-couple the link using only series capacitors without additional circuitry. In this design, though, the user must ensure that this approach functions during worst-case data patterns.

2 System Description

Each node has an AC-coupling capacitor, an RS-485 transceiver, a SymPol™ transceiver, and a J-K flip-flop. The AC-coupling capacitor blocks the circuitry installed on the node from DC voltages that may be present on the bus. The RS-485 transceiver functions only as a transmitter. The SymPol transceiver detects transitions on the RS-485 bus, and the J-K flip-flop latches the bus state when a transition is detected.

2.1 SN65HVD96 SymPol Transceiver

The SN65HVD96 transceiver allows for communication in differential-signaling systems regardless of the orientation of the bus lines (normal or reversed). The SymPol transceiver detects two states on the bus: passive and active. When the differential voltage on the bus is between +500 mV and –500 mV, the bus is said to be passive and the receiver outputs a logic low. When the differential voltage is greater than +900 mV or less than –900 mV, the bus is active and the receiver outputs a logic high.

In this design, the SymPol transceiver detects transition edges on the bus. Usually, the output of transceiver remains high during idle periods and produces a logic low output on every transition edge on the bus (low-to-high or high-to-low).

2.2 SN65HVD3088E

The SN65HVD3088E is a 5-V half-duplex transceiver designed for RS-485 data bus networks with signaling rates of up to 20 Mbps. The SN65HVD3088E is optimized for faster slew rates (faster transition edges). The device operates over a wide common-mode range, bus-fault protection, and fail-safe protection.

In an AC-coupled design, transmitting data to the bus at a lower data rate requires a device with faster transition edges, which have frequency content high enough to pass through the high-pass filter formed by the termination resistor and the capacitor. The SN65HVD3088E fits this requirement because of the high-speed-optimized design.

2.3 SN74HC112

The SN74HC112 is a J-K flip-flop that is triggered by a negative edge with preset and clear options to set or reset the outputs (Q and /Q). This design takes advantage of the toggle mode of the flip-flop to regenerate the data from the edge detected by the SymPol transceiver. In the toggle configuration, the RX output of the SymPol transceiver acts as the clock signal that toggles the output of the flip-flop on each negative edge, allowing for the original data signal to be recovered. To ensure the recovered signal maintains the correct polarity, the flip-flop is reset to an initial state (Q low and /Q high) each time the node transmits data.

2.4 SN74LVC1G04

A single inverter generates the complement of the driver and receiver enable signal to clear (reset) the output of the J-K flip-flop to a known initial state. The output of the inverter connects to the J-K flip-flop and holds the flip-flop clear while the node is driving data to the bus. When data transmission is completed, the node switches to receive mode by enabling the receiver. Next, the output of the inverter sets the J-K flip-flop to the toggle mode with the initial state of Q being low and /Q being high.

3 Block Diagram

Figure 1 shows the block diagram of the reference design.
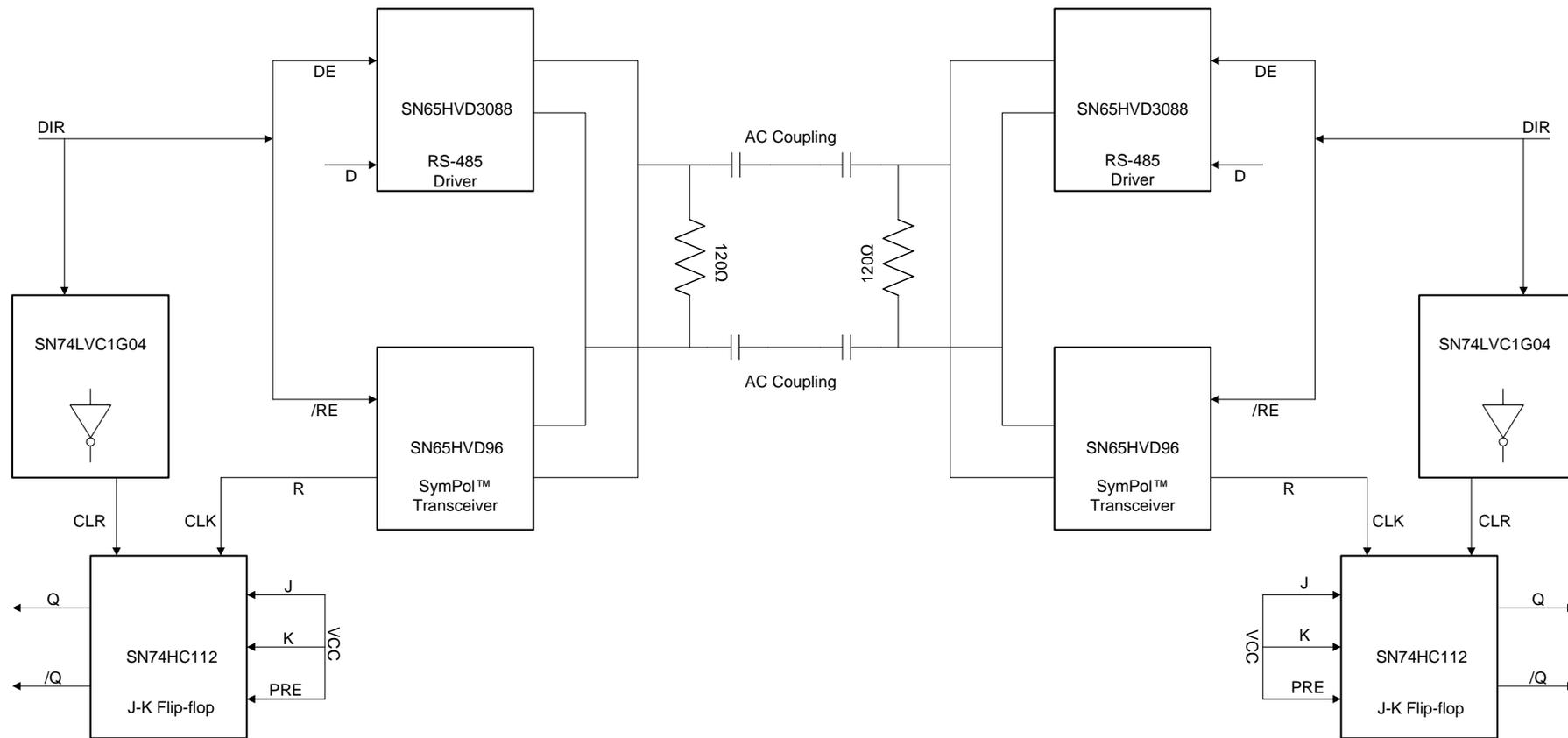
Figure 1. AC-Coupled RS-485 Reference Design

3.1 Highlighted Products

Section 3.1.1, Section 3.1.2, Section 3.1.3, and Section 3.1.4 detail the products used in this design.

For more information on each of these devices, see their respective product folders at www.ti.com.

3.1.1 SN65HVD3088E

The SNx5HVD308xE devices are half-duplex transceivers designed for RS-485 data bus networks. Powered by a 5-V supply, the devices are fully compliant with TIA/EIA-485A standards. With controlled transition times, these devices can transmit data through long twisted-pair cables. The SN65HVD3082E and SN75HVD3082E devices are optimized for signaling rates of up to 200 Kbps. The SN65HVD3085E device can transmit data of up to 1 Mbps, and the SN65HVD3088E device is suitable for applications that require signaling rates of up to 20 Mbps.

These devices operate using a very low supply current exclusive of the load (typically 0.3 mA). These devices are ideal for power-sensitive applications because the supply current drops to a few nanoamps when inactive-shutdown mode is on.

The wide common-mode range and high ESD-protection levels of these devices make them suitable for demanding applications such as energy meter networks, electrical inverters, status and command signals across telecom racks, cabled chassis interconnects, and industrial automation networks where noise tolerance is essential. These devices match the industry-standard footprint of the SN75176 device. Power-on-reset circuits keep the outputs in a high-impedance state until the supply voltage has stabilized. A thermal-shutdown function protects the device from damage due to system fault conditions. The SN75HVD3082E is characterized for operation from 0°C to 70°C, and SN65HVD308xE devices are characterized for operation from –40°C to +85°C air temperature.

3.1.2 SN65HVD96

The SN65HVD96 is designed to meet the requirements for a transceiver that operates with no errors if the twisted-pair signal wires are connected normally or reversed. The design of this device allows for error-free operation in applications where the signal wires may become inadvertently reversed during installation or maintenance. This feature is corrected internally so no intervention from the controller or operator is required. The SN65HVD96 complies with the requirements of *ANSI/TIA-4963, Electrical Characteristics of Reversible Balanced Voltage Digital Interface Circuits*.

3.1.3 CD74HC112

The CD74HC112 is a J-K flip-flop with set and reset controls and has a negative-edge trigger. The device features hysteresis on the clock inputs for improved noise immunity and the device can operate at frequencies of up to 60 MHz, making it suitable for buffering the data coming from the RS-485 bus. The device has buffered-complementary outputs that can drive up to 10 low-power Shottky transistor-transistor logic (LSTTL) loads and features balanced propagation delays and transition times.

3.1.4 SN74LVC1G04

The SN74LVC1G04 device has an inverter gate. This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs and prevents damaging current backflow through the device when it is powered down. The DPW package technology is a breakthrough in IC packaging. The 0.64-mm square footprint saves significant board space compared to other package options and retains the traditional manufacturing-friendly lead pitch of 0.5 mm.

4   System Design Theory

AC-coupling a data link introduces a high-pass-filter effect because of the interaction between the series capacitances and termination resistances. Typically, the frequency content of the data that is being transmitted must be high enough to not be degraded by this filtering effect. This can be challenging for links that use low data rates or for protocols that allow the link to remain at a constant level for long periods of time (because of the transmission of consecutive identical bits or the idle periods between data frames). Although the filter corner frequency can be lowered by increasing the AC-coupling capacitance or increasing the termination resistance, this is often impractical for the lower data rates that are commonly used in RS-485 links because the series capacitance becomes too large to be practical.

This reference design addresses this issue by no longer requiring the corner frequency of the filter to be below the full spectrum of the data signal. Instead, the filter is able to attenuate all signal components except for the transition edges (chosen to be very high in frequency by selecting a high-speed RS-485 transceiver). The receiver circuitry (comprised of the SymPol transceiver and flip-flop) is designed so it translates these edge transitions into a reconstructed data signal.

Using this approach removes any limitations on the data pattern, allowing for arbitrarily low data rates or patterns with long periods of static (constant) data. This approach works with a fairly low capacitance value as well, which often allows for a capacitor with a higher voltage rating to be chosen. This makes it possible for the transceiver to continue to operate even with large voltages present on the external bus.

5   Getting Started Hardware

Two boards are required to evaluate both sides of the RS-485 connection. The design comes prepopulated with all four of the TI ICs that enable the board to function.

VCC and GND are connected at the top right corner of the boards at terminal TB1. The RS-485 bus lines must be connected between nodes using a twisted pair cable. The boards include a terminal block with screw heads to securely attach the power and bus cables. Connect the transmitter output line (from an MCU or UART) at the D pin and the receiver input to Q or /Q (depending on the desired polarity of the signal). These connections can be made to other nodes on the RS-485 bus.

In this AC-coupled application, the receiver and driver of each node must be correctly enabled. This is to ensure the outputs of the J-K flip-flop (Q and /Q) are in a known state. For example, while the node is transmitting data it sets the Q output to low and the /Q output to high. If the driver of the transmitting node is enabled before the driver of the receiving node is disabled the correct data appears on /Q. If the driver of the transmitting node is enabled after the driver of the receiving node is disabled the correct data appears on Q, as shown in Figure 2 and Figure 3.
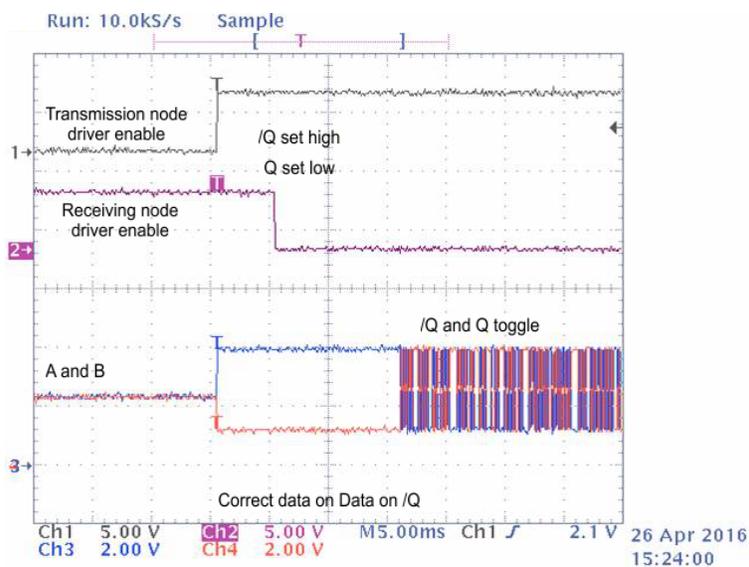
Figure 2. Transmission-Node Driver Enabled Before Receiving-Node Driver is Disabled
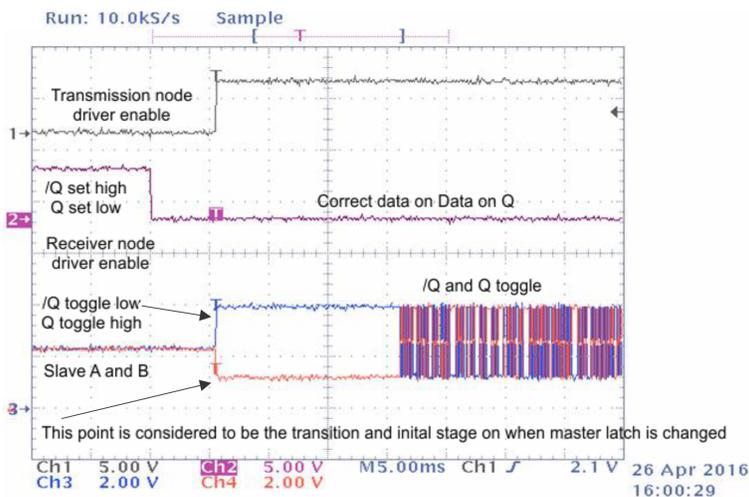
Figure 3. Transmission-Node Driver Enabled After Receiving-Node Driver is Disabled

6 Test Data

6.1 250-kHz Signal

Figure 4 shows the logic signal to be transmitted, the output from the SymPol transceiver of the receiving node, and the reconstructed logic signal of the receiving node at 250 kHz. Figure 5 shows the same transmitted and reconstructed logic signals, and also shows the differential input to the SymPol transceiver (A and B) at 250 kHz.
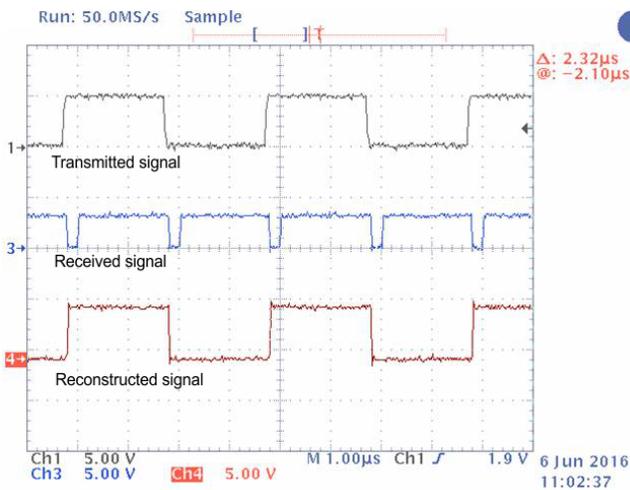
Figure 4. Signals at 250 kHz (500 Kbps)
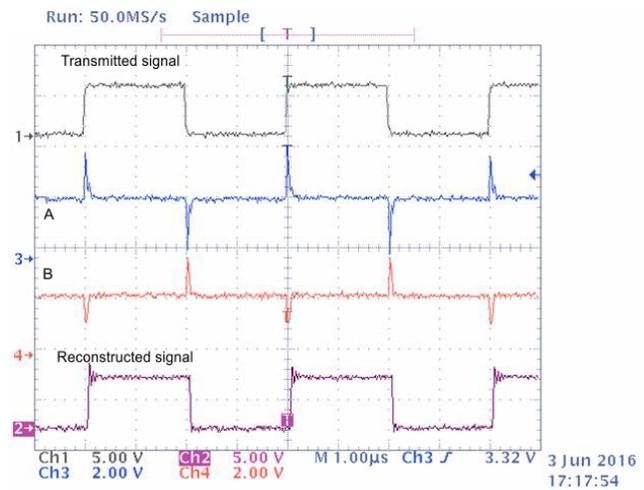
Figure 5. Signals and Differential Input at 250 kHz (500 Kbps)

6.2 1-MHz Signal

Figure 6 shows the logic signal to be transmitted, the output from the SymPol transceiver of the receiving node, and the reconstructed logic signal of the receiving node at 1 MHz. Figure 7 shows the same transmitted and reconstructed logic signals, and also shows the differential input to the SymPol transceiver (A and B) at 1 MHz.
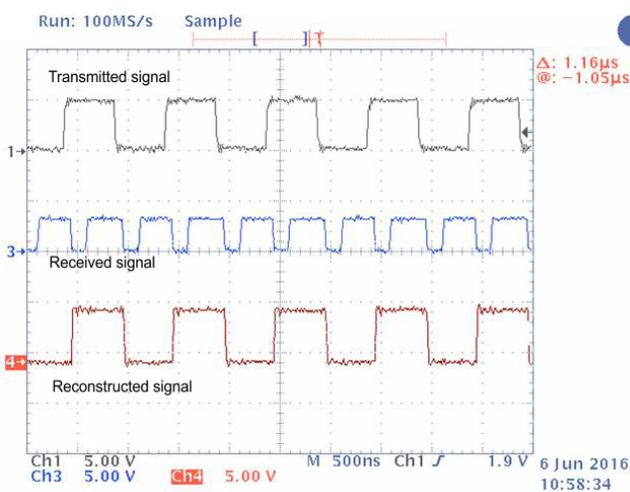
Figure 6. Signals at 1 MHz (2 Mbps)
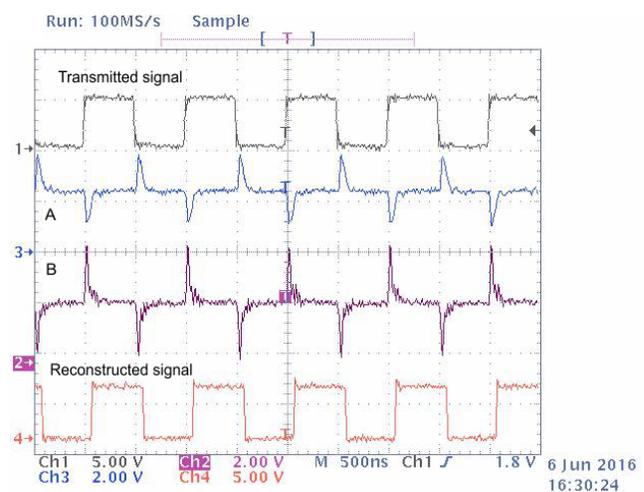
Figure 7. Signals and Differential Input at 1 MHz (2 Mbps)

7 Design Files

7.1 Schematics

To download the schematics, see the design files at TIDA-01171.

7.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01171.

7.3 PCB Layout Recommendations

TI recommends the following:
- Place protection circuitry close to the bus connector to prevent noise transients from entering the board.
- Use VCC and ground planes to provide low-inductance, low-power connections.
- Apply 100-nF to 220-nF bypass capacitors as close as possible to the VCC pins of the transceiver, UART, and controller ICs on the board.
- Use at least two vias for VCC and ground connections of bypass capacitors and protection devices to minimize effective via inductance.

7.4 Layout Prints

To download the layer plots, see the design files at TIDA-01171.

7.5 Allegro Project

To download the Allegro project files, see the design files at TIDA-01171.

7.6 Layout Guidelines

Figure 8 shows the layout guidelines for the TIDA-01171 board. Use local decoupling at each IC, provide bulk decoupling, and match the bus line length.
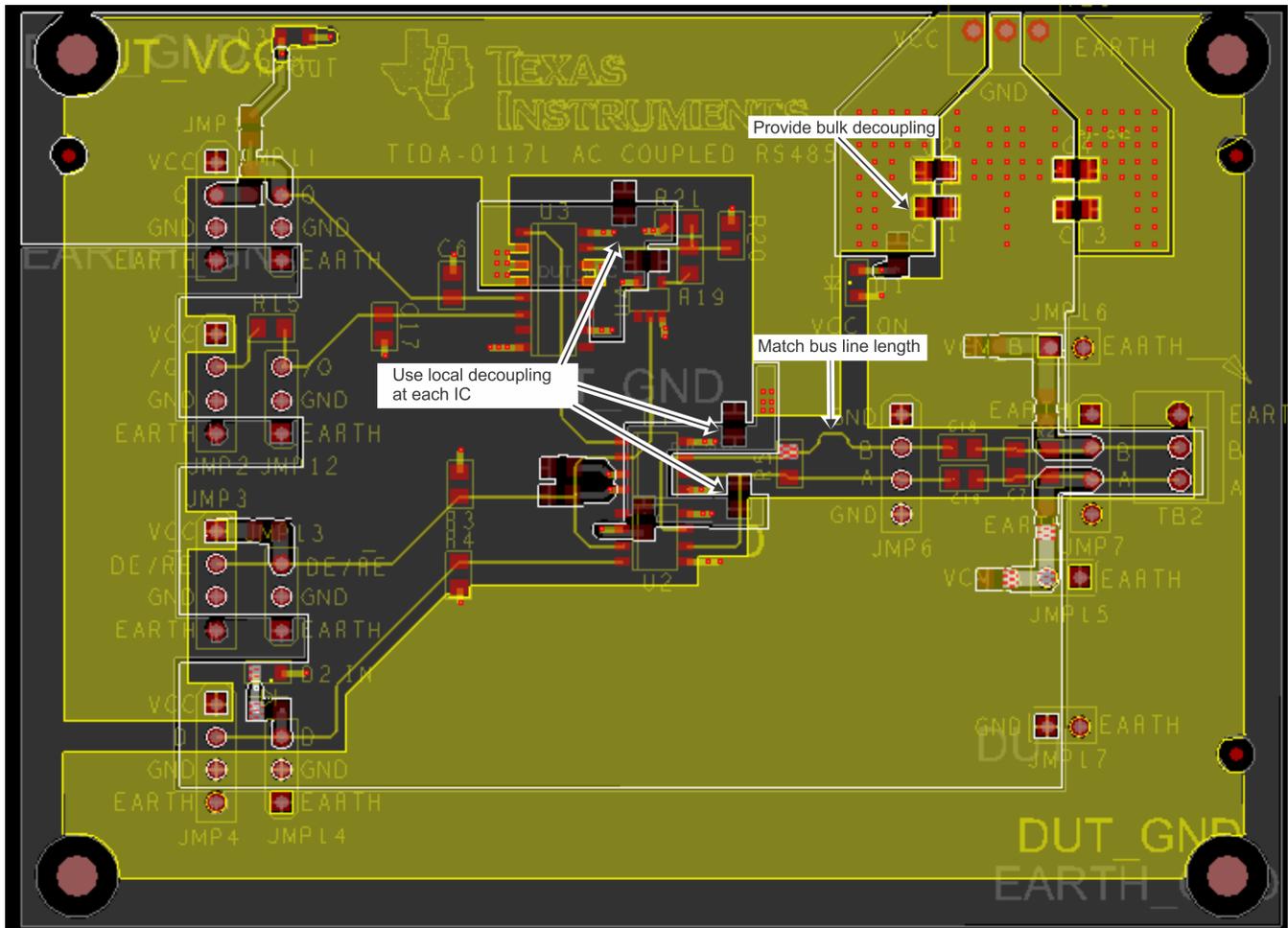
Figure 8. TIDA-01171 Guidelines

7.7 Gerber Files

To download the Gerber files, see the design files at TIDA-01171.

7.8 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01171.

8 Software Files

To download the software files, see the design files at TIDA-01171.

IMPORTANT NOTICE FOR TI REFERENCE DESIGNS