TI Designs

Reference Design to Measure AC Voltage and Current in Protection Relay With Delta-Sigma Chip Diagnostics

Description

This high-accuracy analog front-end (AFE) reference design measures analog input performance and includes chip diagnostics to help identify power system failures using AC voltage and current measurement AFE using a 4-channel, 24-bit simultaneously sampling differential input delta-sigma ADC for measurement over a wide dynamic range. The ADC is configured to measure 0- to 5-V unipolar. The inputs are scaled to ADC measurement range using a fixed-gain amplifier with 2.5-V DC output level shift. The AFE can be used to measure output of a current transformer, potential divider with analog isolation, and Rogowski coil-based active integrator. The AFE uses a 10-bit, low-resolution successive approximation register (SAR) ADC in parallel with ADS131A04 delta-sigma ADC for diagnostics.

Resources

TIDA-00810	Design Folder
ADS131A04	Product Folder
CDCLVC1102PW	Product Folder
OPA4180ID	Product Folder
LMV331	Product Folder
AMC1200	Product Folder
SN6501	Product Folder
TPS71733DCKR	Product Folder
TLV70450DBVR	Product Folder
LM4040	Product Folder
ADC104S021	Product Folder
MSP432P401R	Product Folder

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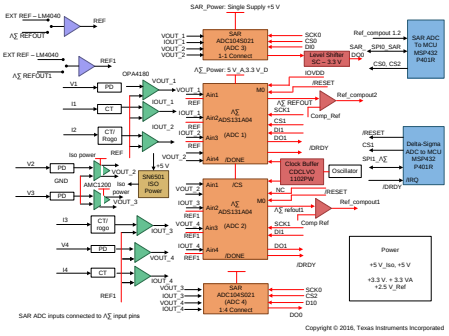
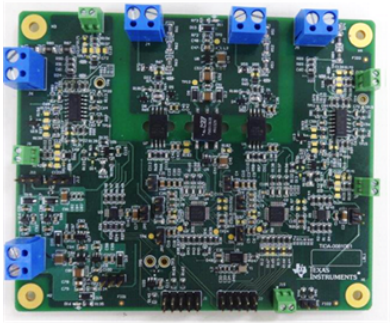
Features

- Data Acquisition
  - Four-Channel, Simultaneous-Sampling, 24-Bit Delta-Sigma ADS131A04 ADC-Based AFE Measures Wide Inputs Within ±0.5% Accuracy
  - Two ADCs Synchronized For Expanding Input Channels (Eight)
- Analog Inputs
  - Current Measurement With Onboard Burden (Low-Value Resistor and Current Transformer)
  - Interfaces to Output of TIDA-00777 Rogowski Sensor With Active Hardware Integrator
  - Voltage Measurement Using Potential Divider (Alternative to Potential Transformer [PT] or Instrument Transformer) and Isolation Amplifier (AMC1200, Basic Isolation)
- Diagnostics
  - Alternate Measurement Path Using 10-Bit SAR ADC for Delta-Sigma ADC Chip Diagnostics
  - Provision for 0- to 5-V AVDD Power Supply and 3.3-V DVDD Power Supply for Host Interface
  - Interfaces With ARM® Cortex®-M4F-Based Low-Power MCU MSP432P401R

Applications

- Merging Unit, Bay Control Unit
- Protection Relay
- Molded Case Circuit Breaker
- Power Quality Analyzer





1 System Overview

1.1 System Description

Protection relays are installed along the power systems to protect primary equipment like transformers, breakers, and customer loads (motors and busbar). Protection relays are used in generation, transmission, distribution, and at consumer locations. The features and complexities vary depending on the installation. Protection relays detect defective lines, apparatus, and other abnormal or dangerous power system conditions. Protection relays also initiate appropriate control over circuit action. Relays detect and locate faults by measuring electrical quantities in the power system which are different during normal and intolerable conditions. The most important role of protection relays is to first protect individuals and then protect equipment.

Protection relays also minimize the damage and expense caused by insulation breakdowns, which (above overloads) are called faults. These faults can occur as a result of deteriorated insulation or unforeseen events such as lightning strikes or power trips caused by contact with trees and foliage. Protection relays are not required to operate during normal operation, but must immediately activate to handle intolerable system conditions. This immediate availability criterion is necessary to avoid serious outages and damage to portions of or the entire power network. In theory, a relay system should be able to respond to an infinite number of abnormalities that may occur within the network.

Protection relays are intelligent electronic devices (IEDs) that receive measured signals from the secondary side of current transformers (CTs) and voltage transformers (VTs). The relays detect whether or not the protected unit is in a stressed condition (based on the type and configuration of the unit). The protective relays send a trip signal to the circuit breakers to disconnect the faulty components from the power system if necessary.

1.1.1 Introduction to Protection Relays and Subsystems for Grid Applications

Figure 1 shows a generic block diagram for a multifunction protection relay.

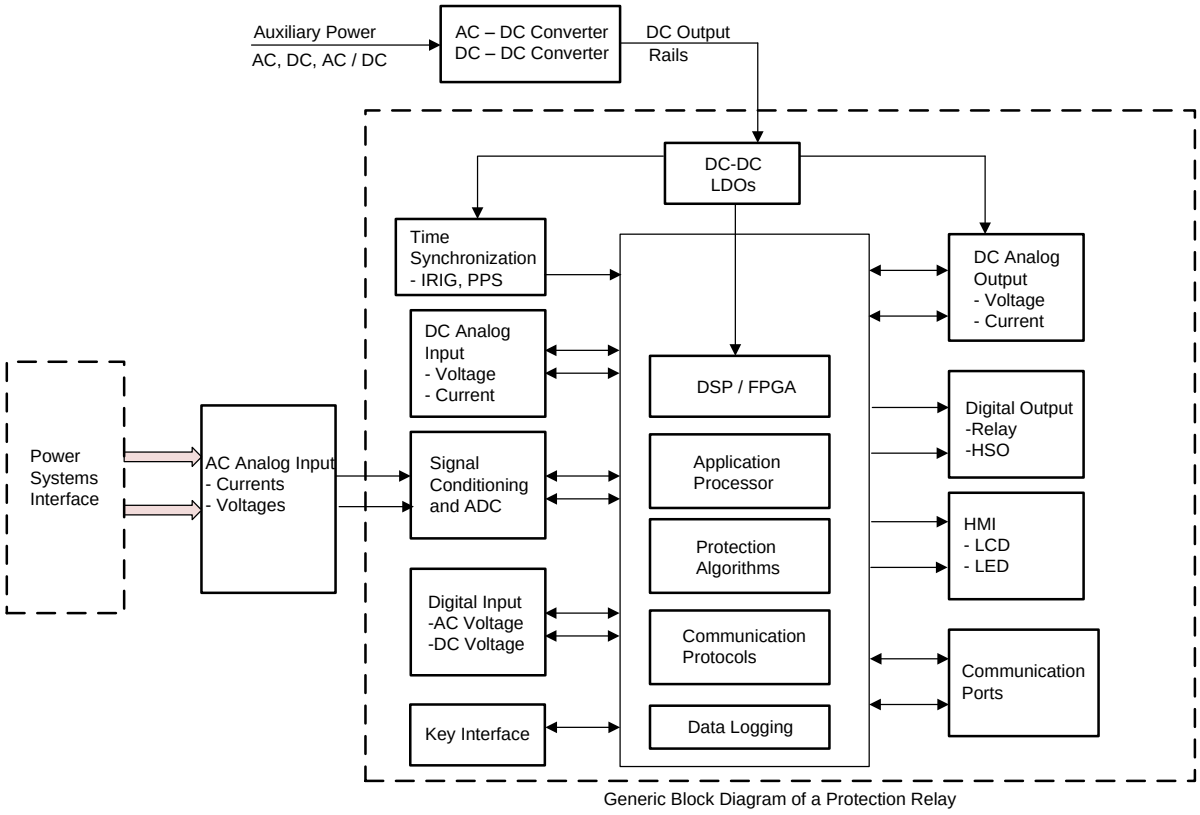


Figure 1. Generic Block Diagram of Protection Relay

Protective relays are categorized based on the equipment type protected such as generators, transmission lines, transformers, and loads.

The protection relays or IEDs used in grid applications have the following generic subsystems. The subsystems are based on the functionality.

- CPU or DSP module – This module handles all protection functions and logic. Additionally, this module also handles the HMI and communication functions.
- Power supply
  - Nominal auxiliary voltage: 24-V DC, 48- to 60-V DC, 110- to 125-V DC, 220-V DC, 230-V AC, 50 or 60 Hz, ±20%, and 40-W maximum admissible consumption
  - Stored energy for up to 50-ms power supply interruption
- AC measurement inputs
  - Nominal frequency (FNOM): 50 or 60 Hz
  - Operating range: 45 to 66 Hz
  - Accuracy: 0.2% FS at FNOM
- CT measurements inputs
  - Nominal current: 1 or 5 A (IN)
  - Nominal consumption per phase: < 0.15 A at IN
  - Load rating: 20 A in continuous; 30 A for 3 s; 100 A for 1 s
- VT measurements inputs
  - Nominal voltage: 57.7 to 500 V
  - Nominal consumption per phase: < 0.1 VA at 130 V
  - Maximum measurable voltage: 577 V_{RMS}
- DC analog input range (independently configurable):
  - ±1.25, ±2.5, ±5, and ±10 V
  - ±1, ±5, ±10, and ±20 mA
  - 0 to 1, 0 to 5, 0 to 10, 0 to 20, and 4 to 20 mA
- DC analog output range (independently configurable): ±5, ±10, ±20 mA, and 4 to 20 mA
- Digital inputs
  - Nominal voltage: 24-V DC, 48- to 60-V DC, 110- to 125-V DC or AC, 220-V DC or AC, ±20% or multi-voltage (24- to 250-V DC or AC)
  - Groups of 4, 8, 12, 16, or 32
- Digital output relays – Continuous current: 5 A
- Control output relays – Continuous current: 5 A
- Time synchronization
  - IRIG–B GPS clock (through the IRIG-B input)
  - Ethernet SNTP server
  - Time telegram message issued by remote SCADA (DNP3.0, IEC 60870-5-101 or IEC 60870-5-104)
- Communication capabilities – Ethernet communication
- 10BASE-TX or 100BASE-TX, auto-crossing, or 100BASE-FX
- Protocols include UCA2 or IEC 61850, IEC 60870-5-104 (multi-client), or DNP3.0 IP
- Embedded Ethernet switch module with up to six ports (permitting a compact connection of various devices or I/O extensions) – Serial communication
- Up to two SCADA or four IED links per device
- SCADA protocol can be switched between DNP3.0, IEC 60870-5-101, and MODBUS.
- IED protocol can be switched between DNP3.0, IEC 60870-5-103, MODBUS, and IEC 60870-5-101.

This TI reference design focuses on the accurate measurement of voltage and current inputs using a high-resolution delta-sigma ADC.

1.1.2 Voltage, Current, and Power Measurement AFE

The AFE for measurement of AC voltage and current inputs consists of the following:

- Voltage input circuit with potential divider, signal conditioning, and interface to ADC
- Current input circuit consisting of burden resistors, signal conditioning, and interface to ADC
- Signal condition circuit provides fixed or variable gain to the AC inputs and also provides a common mode DC level shift based on application to interface to the ADC.
- ADC for sampling the analog inputs includes multichannel inputs and a high-resolution ADC capable of sampling at ≥ 80 samples per cycle.
- Interface to the MCU to process the sampled values includes an MCU and interconnection to the AFE.
- Power supply subsystem includes generation of required positive and negative power supplies.

Additional features of the AFE include:

- Measurement of a wide range of input currents and voltages
- Accurate measurement of AC parameters over the entire input range
- Isolated measurement of voltages using isolation amplifiers
- Measurement of increased number of channels
- Option to diagnose the ADC performance

1.1.3 Accurate Measurement of AC Voltage, Current, and Power

Most of the multifunction protection relays from different manufacturers provide power-measurement features. Protection relays are specified to measure wide input voltage and currents within a specified range of accuracy. To achieve wide dynamic input measurement within specified accuracy, an ADC with PGA or a high-resolution ADC are used. This reference design uses a 24-bit delta sigma ADC.

1.1.4 Increasing Analog Input Channels

Depending on the protection relay configuration and application, the number of current and voltage channels varies from 4 to 16 channels. The 4 to 16 channels are realized by using multiple ADCs. If each ADC has separate interfaces, the complexity increases. Also, it may be necessary to synchronize multiple ADCs to ensure accuracy. The simplest way to interface multiple ADCs is by daisy-chaining and using a common clock. In this reference design, two ADCs are used. Each ADC has four channels. The ADCs are chained as a single interface and both the ADCs share a common clock.

1.1.5 Measurement of Voltages and Currents

Protection relay is used in HV, MV, or LV applications. Depending on the application the voltage levels are high, and during fault conditions the protection relay becomes damaged due to the high voltage levels. The solution to this issue is isolating the voltage and current inputs. The voltages are isolated to provide user safety. The inputs can be isolated using analog isolation amplifiers or digitally using modulators. In this reference design isolation amplifiers are used and the output of the isolation amplifiers is interfaced to the delta-sigma ADC.

1.1.5.1 Current Transformer or Rogowski Coil Inputs

Primary current is reduced to measurable secondary current by an external CT and applied to the protection relay. The protection relay has an internal CT to transform the secondary current to a measurable input current level. The advantage of using a CT is that it provides isolation, and no additional isolation is required on the protection relay when an internal CT is used.

1.1.5.2 Voltage Inputs

High-voltage inputs are connected to a PT and the secondary is connected to the input of the protection relay. Internally the protection relays have a PT that can transform the input AC voltage into a measurable value. PTs are large and have inherent nonlinearity. This issue is overcome by using a resistor divider; however, resistor dividers do not provide isolation like a PT. When using resistor dividers, isolation amplifiers provide the required isolation. Isolation amplifiers with basic or reinforced isolation can be used based on the application. The solution of using the resistor divider and isolation amplifier can be considered as an alternative to the conventional PT.

1.1.6 Alternative Methods for Interfacing Analog Inputs to ADC

ADS131A04 is a differential input. In applications where differential measurement is preferred, the following solutions can be considered:

- THS4551 – a low-noise, precision, 150-MHz, fully differential amplifier
- THS4531 – an ultra-low-power, RRO, fully differential amplifier

For cost-sensitive applications, sensor output can be directly interfaced to the differential input of the ADC. The performance must be evaluated with specific sensors for accuracy.

1.1.7 Diagnostics

With the demand to improve safety in the workplace and reliability of power systems, as well as reduce operating costs, industries including grid infrastructure have implemented functional safety complying with the functional safety requirements of standard IEC 61508. To conform with functional safety requirements, system manufacturers must perform safety analysis not just at the system level, but also down to the device level.

The high-resolution ADCs used for measurement can be diagnosed without stopping the conversion by using an additional lower-resolution ADC. The results of the lower resolution can be used to validate the higher-resolution ADC measurement in the application requiring functional safety.

1.2 Key System Specifications

Table 1. Key System Specifications

SERIAL NUMBER	PARAMETERS	DESCRIPTION	COMMENTS
1	ADC for measurement of analog inputs • Type • Resolution • Channels	Delta-sigma, 24-bit, 4 channel	Measurement accuracy ±0.5%
2	Number of analog inputs	Eight, two ADCs chained	Both ADCs are synchronized using a common clock.
3	Non-isolated voltage input range	5 V to 300 V with resistor divider and fixed-gain amplifier	Measurement accuracy ±0.5%
4	Isolated voltage input range	10- to 270-V AC AMC1200 isolation (basic) amplifier based	Measurement accuracy ±0.5%
5	Current input measurement range	0.25-A to 100-A AC with fixed-gain amplifier	Measurement accuracy ±0.5%
6	ADC clock	16.384-MHz oscillator with two buffered output clocks	—
7	Reference	Internal: • 2.442 VDC • 4 VDC	ADC on power up defaults to external reference.
		External (optional): • 2.5 VDC	
8	Power supply for AFE	Positive • Digital: +3.3 V • Analog: +5 V	Analog input voltage: VAVDD to VAVSS +5 V is used for unipolar input.
9	Isolated power	Positive • Analog: +5 V	—
10	Interface to MCU for delta-sigma and SAR	SPI™	See Section 3 for connection details.
11	Diagnostics ADC	10-bit SAR, with 0-V to 5-V input range	—
12	Diagnostics of reference output	Comparator with fixed threshold	—
13	SAR ADC to MCU interface	5-V to 3.3-V level shifter	SAR ADC SPI clock output level of 5 V must be level shifted to 3.3 V to interface to the MSP432P401R.

NOTE: All the voltage and current values are in V_{RMS}.

1.3 Block Diagram

The high-performance AC analog input data acquisition (see Figure 2) has two 24-bit delta-sigma ADCs chained to measure up to eight analog inputs. Potential dividers are provided to directly connect the AC voltage up to 300 V. The option to measure isolated voltage has been provided using isolation amplifiers. The current and isolated voltage inputs have a fixed-gain front-end amplifier for adjusting the current measurement range, and the output of the amplifier is connected to the ADCs. The voltage and current inputs are measured as pseudo-differential inputs and the voltage inputs from the isolation amplifier are measured as differential input.

The required positive power supply for the ADCs operation is generated from one DC input, and provision to configure the power supply based on the input configuration has been provided. Isolated power required to operate isolation amplifiers is also generated onboard. Additionally the reference design has provision to diagnose reference, delta-sigma ADC using comparators, and low-resolution SAR ADCs.

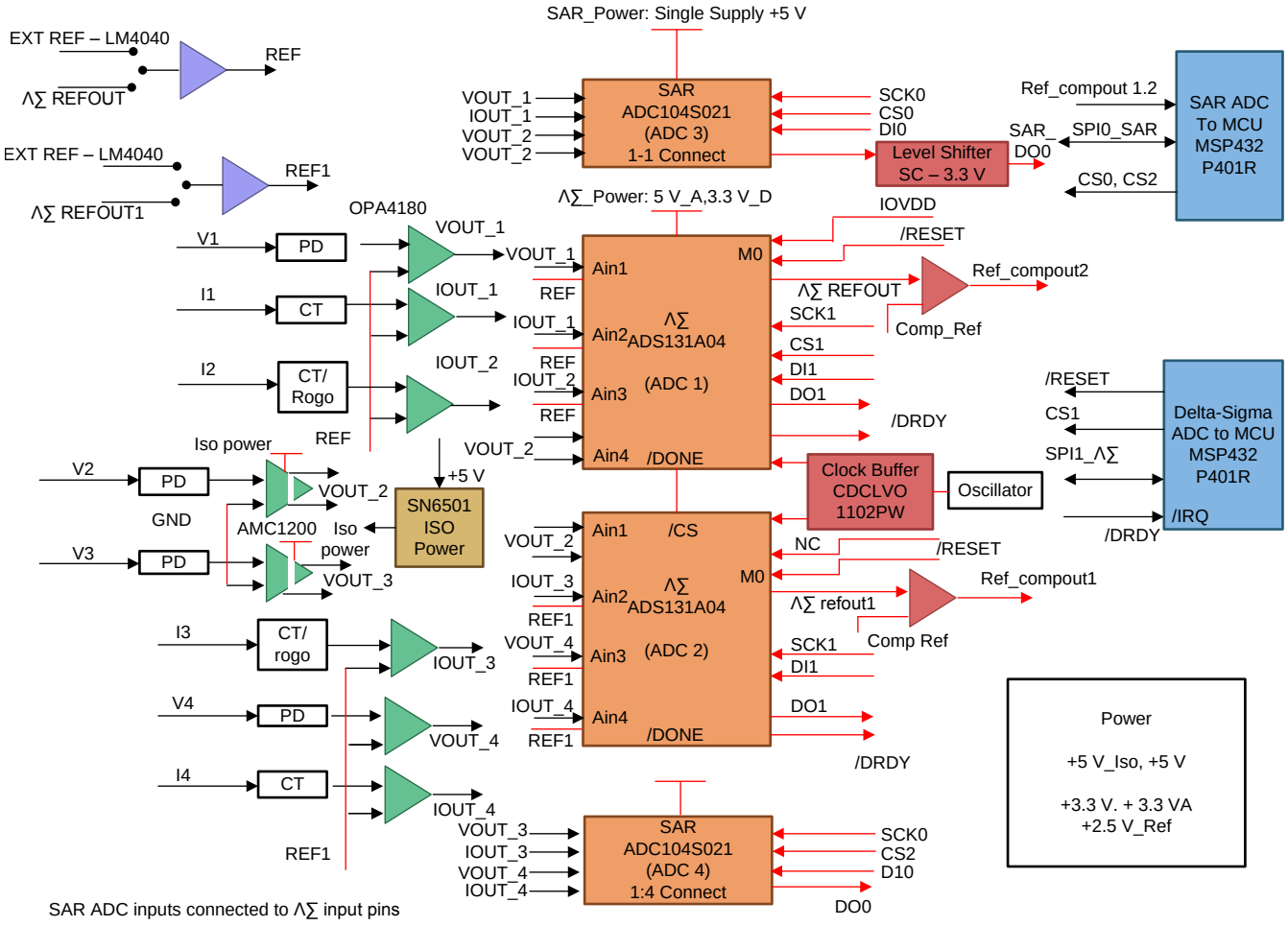


Figure 2. Block Diagram of AFE With Delta-Sigma Chip Diagnostics

1.3.1 Delta-Sigma ADC for Measurement

ADS131A04, a 24-bit, 4-channel, simultaneous-sampling differential ADC is used to measure the analog input accurately over a wide range. Two ADCs are chained to measure up to eight channels. For synchronizing the chained ADCs a common clock oscillator of 16.384 MHz frequency and clock buffer CDCLVC1102PW is used. The ADC analog power input is configurable from 0 to 5 V or ±2.5 V based on the application and the input configuration. The isolated voltage output is connected differentially to the ADC. The current and non-isolated voltage gain amplifier outputs are connected in a pseudo-differential input configuration to the ADCs.

1.3.1.1 ADC Interface to MCU—MSP432P401R

Provision to interface ADS131A04 to the MSP432P401R LaunchPad™ has been provided onboard. The SPI signals, ADC reset, and the ADC data ready signals are interfaced to the MSP432P401R LaunchPad. The ADC IOVDD is configured as asynchronous interrupt mode for communicating with the MCU.

1.3.2 Signal Conditioning

1.3.2.1 Current and Non-Isolated Voltage Inputs (With Potential Divider)

The current inputs are connected to external CT of accuracy class 0.1 and the secondary output is connected to the AFE. The transformer has a turns ration of 2000. The secondary of the current transformer is differentially connected to the signal conditioning circuit. The gain is provided using an accurate opamp OP4180. The output of the gain amplifier is a single-ended output connected to the delta-sigma ADC.

An AC voltage input up to 300 V can be directly connected to the AFE. The AFE has an onboard potential divider which divides the 300-V AC input to less than 1.5 V. An amplifier is used to provide a fixed gain and the output of the amplifier is connected to the ADC.

1.3.2.2 Isolated Voltage Input Using Isolation Amplifier AMC1200

In applications that require basic isolation for voltage inputs AMC1200 is used. The voltage input is applied across a potential divider and the potential divider output is connected to the AMC1200. The AMC1200 has an input range of ±250 mV. The output has a common-mode shift of 2.55 V with 5-V supply and ×8 gain. The output of AMC1200 is differentially connected to the ADC.

1.3.2.3 Reference

The reference is configured depending on the input. When operating in 0- to 5-V input mode the reference is 2.5 V. The ADC internal reference is 2.442 V or 4 V. The ADC provides a reference output, which can be used for the AFE signal conditioning. The ADC reference is by default configured for external reference. The device must be configured to internal reference for the reference output to be active. Alternatively, an external 2.5-V reference can be used to maximize dynamic range.

1.3.2.4 Analog Inputs Protection

The current inputs are protected against opening by using two parallel resistors and TVS. The voltage inputs are protected for overvoltage and multiple resistors are used as potential divider for improved reliability.

The potential divide input to the isolation amplifier is also protected for overvoltage. Additionally, the isolation amplifiers are protected for overvoltage.

1.3.3 Power Supply

1.3.3.1 Non-Isolated Power

ADS131A04 has flexible analog power supply input options for operation.

- Unipolar supply: 3.3 to 5.5 V
- Digital supply: 1.65 to 3.6 V

The required power supplies are generated from a single 5.5-V input. The positive voltages generated are 5 V and 3.3 V. These voltages provide flexibility to operate the ADC in any required input configuration.

1.3.3.2 Isolated Power

The isolation amplifier is operated with 5 V on the analog input side. The isolated power supply required is generated from 5 V on the digital side. The required isolated power is generated using the SN6501 transformer driver and LDO. The transformer for the isolated power has been chosen with dielectric voltage of > 5 kV_{RMS}.

1.3.4 Delta-Sigma ADC Diagnostics

For applications requiring functional safety, a low-resolution SAR ADC (ADC104S021CIMM) has been provided. By using the data from the SAR ADC, a delta-sigma ADC can be diagnosed. The references are diagnosed by using external comparators (LMV331) connected as GPIO inputs to the MCU. The ADC operates on 5 V and MCU operates on 3.3 V. The input levels from the MCU are compatible with the expected levels of the ADC. The ADC output is not compatible with the MCU input. A 5-V to 3.3-V level shifter (SN74LV1T34) is used to make the data output signal level from the SAR ADC compatible with MCU input levels.

2 System Design Theory

2.1 Delta-Sigma ADC for Analog Input Measurement

Figure 3 and Figure 4 show two ADS131A04 devices in chain configuration interfaced to the MCU.

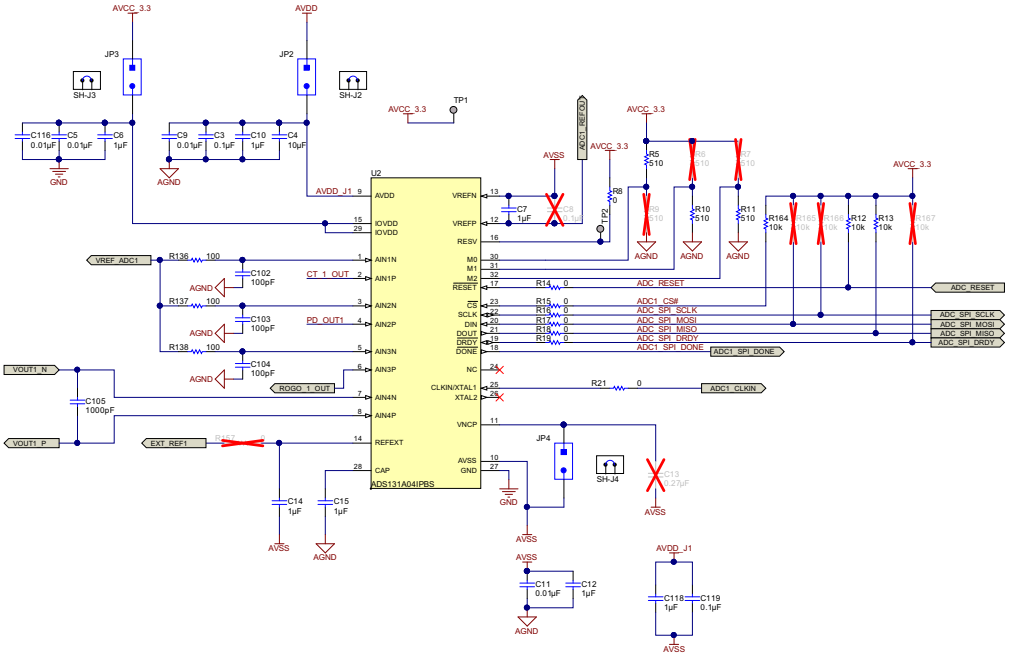


Figure 3. Delta-Sigma ADC1 Configuration

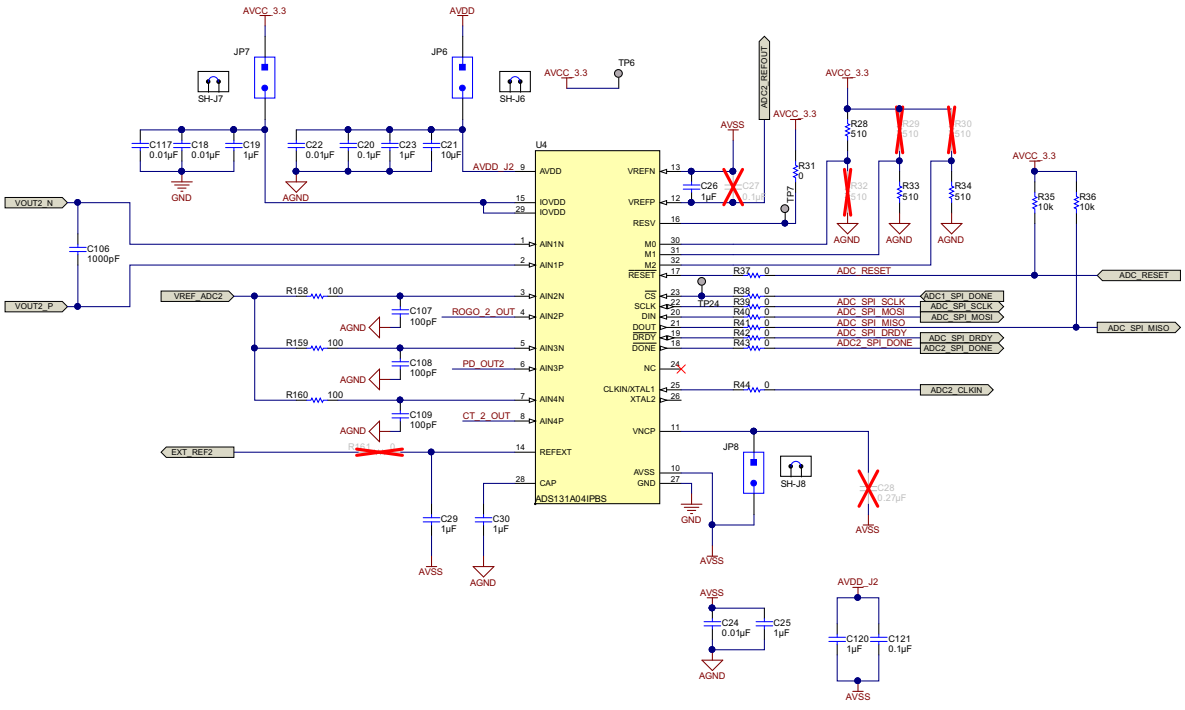


Figure 4. Delta-Sigma ADC2 Configuration

Two ADS131A04 ADCs are chained in this reference design. The following inputs have been connected:

- Current input
- Non-isolated voltage inputs
- Isolated amplifier output (isolated voltage)

The current inputs and the non-isolated voltage inputs are applied in a pseudo-differential configuration. The isolated voltage inputs are applied as differential inputs to the ADC. The ADC has an internal reference. The ADC is configured to use the internal reference, and an external clock input is applied for operation.

Jumpers are provided for the following:

- AVDD – JP2 and JP6
- AVCC – JP7 and JP3
- Charge pump disable – JP4 and JP8

In the current design configuration the charge pump is disabled by mounting the jumpers. The power supply jumpers must also be mounted for proper operation.

For the unipolar mode of operation, an input of 0 to 5 V can be applied, and for bipolar mode input of ±2.5 V can be applied. The M0, M1, and M2 pins are used to configure the ADC. The ADC is configured in asynchronous interrupt mode in this design. Two devices have been chained to achieve eight inputs.

2.1.1 Delta-Sigma ADC—ADS131A04

The ADS131A04 are 4-channel, simultaneously sampling, 24-bit, delta sigma ADCs. Wide dynamic range, scalable data rates, and internal fault monitors make the ADS131A04 ideally suited for energy monitoring, protection, and control applications. Flexible power-supply options are available to maximize the effective number of bits (ENOB) for high dynamic range applications. Asynchronous and synchronous master and slave interface options are available, providing ADC configuration flexibility when chaining multiple devices in a single system.

Features:

- Four simultaneously sampling differential inputs
- Data rates up to 128 kSPS
- Noise performance
  - Single-channel accuracy better than 0.1% at 10000:1 dynamic range
  - ENOB: 19.1 bits at 8 kSPS
  - THD: –100 dB at 50 Hz and 60 Hz
- Integrated negative charge pump
- Flexible analog power-supply operation:
  - Negative charge pump: 3.0 to 3.45 V
  - Unipolar supply: 3.3 to 5.5 V
  - Bipolar supply: ±2.5 V
- Digital supply: 1.65 to 3.6 V
- Low-drift internal voltage reference: 4 ppm/°C
- ADC self checks
- Cyclic redundancy check (CRC) and hamming code error correction on communications
- Multiple SPI data modes:
  - Asynchronous interrupt
  - Synchronous master and slave
- Package: 32-pin TQFP
- Operating temperature range: –40°C to 125°C

Find more information at the device's product page: http://www.ti.com/product/ADS131A04

NOTE: The ADS131A02 2-Channel AFE can be considered in single-phase applications.

2.1.2 Clock Buffer CDCLVC1102PW

Two ADCs are used in this reference design. To synchronize the sampling of the two ADCs, the same clock is applied to both ADCs. A 16.348-MHz oscillator is used to generate the clock. The clock output is buffered using a clock buffer (see Figure 5).

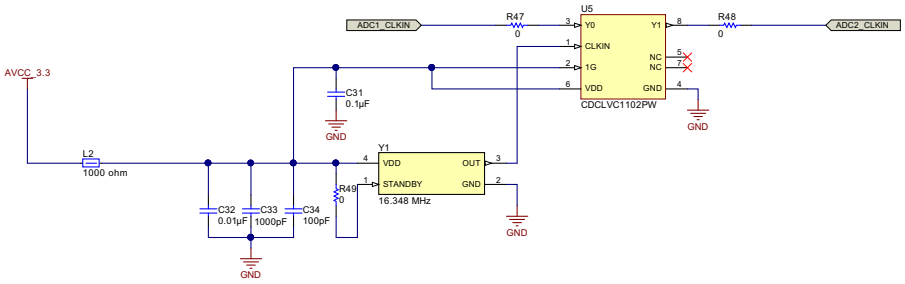


Figure 5. Clock Buffer for Delta-Sigma ADCs

The CDCLVC11xx is a modular, high-performance, low-skew, general-purpose clock buffer family from TI. Seven different fan-out variations, 1:2 to 1:12, are available. All of the devices are pin compatible to each other for easy handling. All family members share the same high-performing characteristics such as low-additive jitter, low skew, and wide operating temperature range.

Features:

- High-performance LVCMOS clock buffer family
- Very low pin-to-pin skew < 50 ps
- Very low additive jitter < 100 fs
- Supply voltage: 3.3 V or 2.5 V
- f_{max} = 250 MHz for 3.3 V
- f_{max} = 180 MHz for 2.5 V
- Operating temperature range: –40°C to 85°C

Table 2 lists the features of the CDCLVC1102PWR.

Table 2. CDCLVC1102PWR Features

PARAMETER	DETAILS
Part number	CDCLVC1102PWR
Description	IC CLK BUFFER 1:2 250-MHZ 8TSSOP
Type	Fan-out buffer (distribution)
Number of circuits	1
Ratio—input:output	1:02
Differential—input:output	No / no
Input	LVCMOS
Output	LVCMOS
Voltage supply	2.3 to 3.6 V
Mounting type	Surface mount
Supplier device package	8-TSSOP

Find more information at the device's product page: http://www.ti.com/product/CDCLVC1102

2.1.3 Delta-Sigma ADC Interface to MCU—MSP432P401R

Delta-sigma ADCs are interfaced to the MCU MSP432F401R through the SPI (see Figure 6). The required interface signals from the ADC are terminated to connector J2. Resetting the ADC is critical. Follow the instructions in Section 9.4.5 (RESET) of the data sheet (SBAS590) to reset the ADC during initialization.

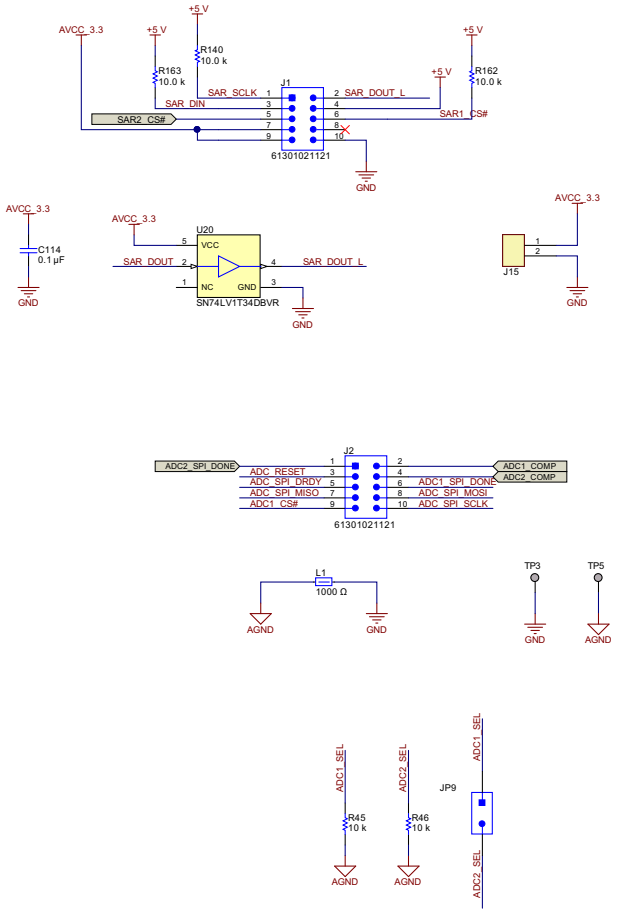


Figure 6. Delta-Sigma ADC to MCU Interface Connector

The MSP432P401x device family is TI's latest addition to its portfolio of efficient ultra-low-power mixed-signal MCUs. The MSP432P401x family features the ARM Cortex-M4 processor in a wide configuration of device options including a rich set of analog, timing, and communication peripherals, thereby catering to a large number of application scenarios where both efficient data processing and enhanced low-power operation are paramount.

Features:

- Core
  - ARM 32-bit Cortex-M4F CPU with floating-point unit and memory protection unit
  - Frequency up to 48 MHz
  - Performance benchmark
    - 1.196 DMIPS/MHz (Dhrystone 2.1)
    - 3.41 CoreMark/MHz
  - Energy benchmark:
    - 167.4 ULPBench score

- Memories
  - Up to 256KB of flash main memory (simultaneous read and execute during program or erase)
  - 16KB of flash information memory
  - Up to 64KB of SRAM (including 8KB of backup memory)
  - 32KB of ROM with MSPWare driver libraries
- Operating characteristics
  - Wide supply voltage range: 1.62 to 3.7 V
  - Temperature range (Ambient): –40°C to 85°C
- Serial communication
  - Up to four eUSCI_A modules
    - UART with automatic baud-rate detection
    - IrDA encode and decode
    - SPI (up to 16 Mbps)
  - Up to four eUSCI_B modules
    - I^2C (with multiple-slave addressing)
    - SPI (up to 16 Mbps)
- Flexible I/O features
  - Ultra-low-leakage I/Os (±20-nA maximum)
  - Up to four high-drive I/Os (20-mA capability)
  - All I/Os with capacitive touch capability
  - Up to 48 I/Os with interrupt and wake-up capability
  - Up to 24 I/Os with port mapping capability
  - Eight I/Os with glitch filtering capability
- Advanced low-power analog features
  - 14-bit, 1-MSPS SAR ADC
  - Internal voltage reference with 10-ppm/°C typical stability
  - Two analog comparators

Find more information at the device's product page: http://www.ti.com/product/MSP432P401R

2.1.3.1 MSP432P401R LaunchPad

The MSP432P401R LaunchPad lets users develop high-performance applications that benefit from low-power operation. The LaunchPad features the MSP432P401R, which includes the following:

- 48-MHz ARM Cortex-M4F
- 95-µA/MHz active power
- 850-nA RTC operation
- 14-bit 1-MSPS differential SAR ADC
- AES256 accelerator

This LaunchPad includes an onboard emulator with EnergyTrace™+ Technology, which means users can program and debug their projects without the need for additional tools, while also measuring total system energy consumption. All pins of the MSP-EXP432P401R device are fanned out for easy access.

2.1.4 Chaining of Multiple Delta-Sigma ADCs

In this reference design two ADS131A04 devices are chained to increase the number of analog channels. The ADS131A04 lets the designer add channels by adding an additional device to the bus. The first device in the chain can be configured using any of the interface modes. All subsequent devices must be configured in synchronous slave mode. In all cases, however, the chain of ADS131A04 devices appears as a single device with extra channels, with the exception that each device sends individual status and data integrity words. In this manner, no additional pins on the host are required for an additional device on the chain. The only special provision that must be made in the interface is to extend the frame to the appropriate length.

2.1.4.1 First Device Configured in Asynchronous Interrupt Mode

Figure 7 shows a multiple-device configuration where the first device is configured in asynchronous interrupt mode as noted by the state of the M0 pin. The second ADS131A04 device and any additional devices are configured in synchronous slave mode.

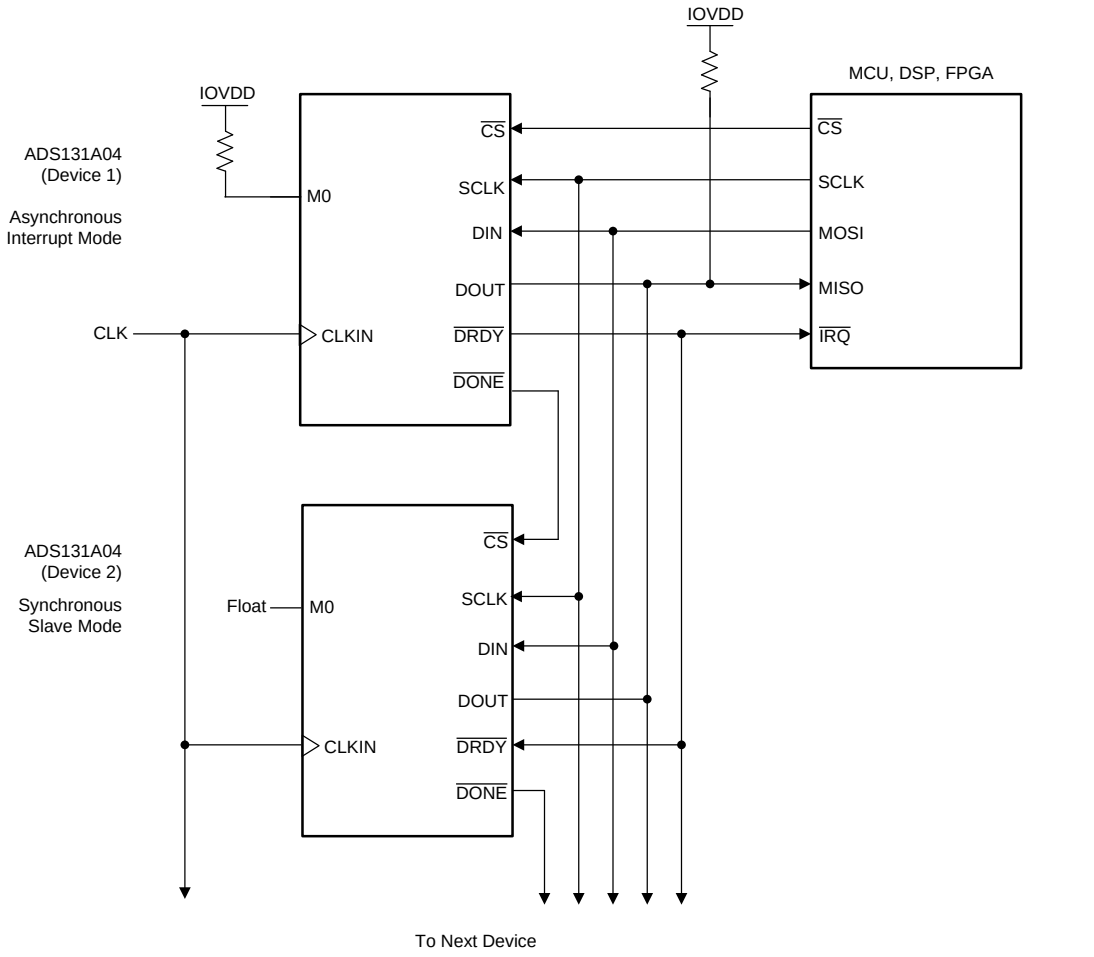


Figure 7. Multiple Device Configuration Using Asynchronous Interrupt Mode

See Section 10.1.3 of the data sheet *Chaining for Multiple Device Configuration* (SBAS590) for more information on chaining multiple devices.

2.2 Signal Conditioning With OPA4180 Amplifier

The OPA4180 operational amplifiers use zero-drift techniques to simultaneously provide low-offset voltage (75 μV), and near zero-drift over time and temperature. These miniature, high-precision, low-quiescent current amplifiers offer high-input impedance and rail-to-rail output swing within 18 mV of the rails. The input common-mode range includes the negative rail. Either single or dual supplies can be used in the range of 4.0 V to 36 V (±2 to ±18 V). The quad is offered in SOIC-14 and TSSOP-14 packages. All versions are specified for operation from –40°C to 105°C.

Features:

- Low offset voltage: 75 μV (maximum)
- Zero-drift: 0.1 μV/°C
- Low noise: 10 nV/√Hz
- Very low 1 / f noise
- Excellent DC precision:
  - PSRR: 126 dB
  - CMRR: 114 dB
  - Open-loop gain (AOL): 120 dB
- Quiescent current: 525 μA (maximum)
- Wide supply range: ±2 to ±18 V
- Rail-to-rail output: input includes negative rail
- Low bias current: 250 pA (typical)
- RFI filtered inputs

Find more information at the device's product page: http://www.ti.com/product/OPA4180

2.2.1 Current Inputs

Figure 8 shows the current input scaling amplifiers for four input currents.

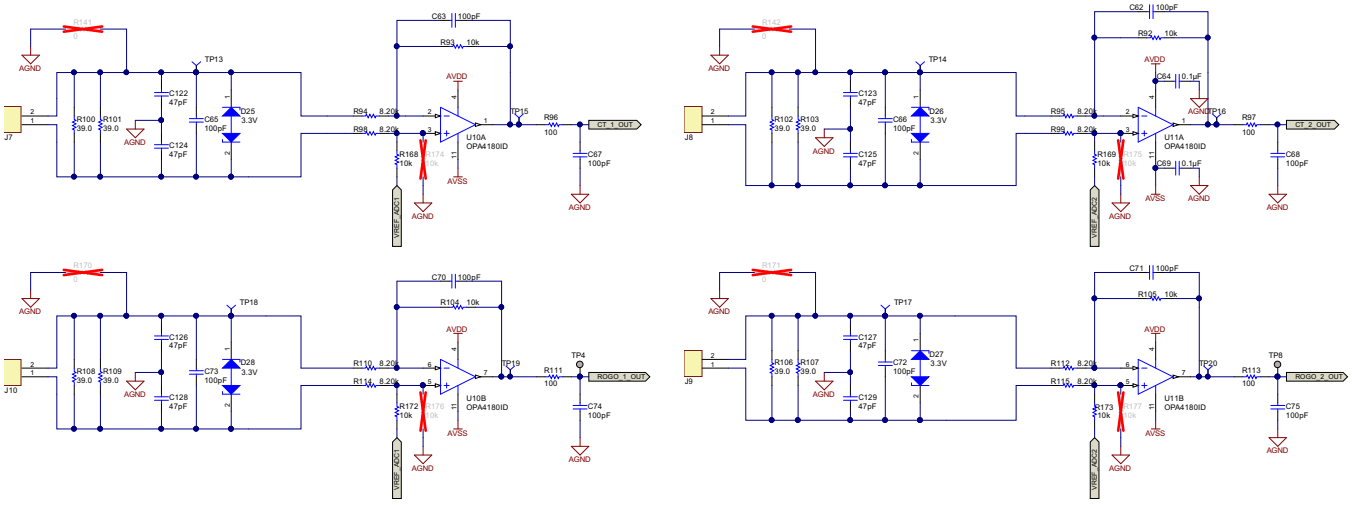


Figure 8. Current Input Signal Conditioning

This reference design provides provision to measure up to four current inputs. Two current channels are provided for each ADC. An external CT is used to step down the primary current. The CT ratio used in this TI Design is 1:2000. The secondary current is connected as input to a fixed-gain amplifier. The amplifier is configured in differential mode and depending on the application and the input voltage range the gain can be configured. The output of the amplifier is connected to the delta-sigma ADC for measurement.

The burden required for converting the current input to voltage is provided onboard.

Table 3 provides the calculation and the values for the current input scaling amplifiers.

Table 3. Calculation of Current Input Range

CURRENT MEASUREMENT	VALUE	UNIT
Burden	19.5000	Ω
Gain	1.2195	—
RF	10.0000	Ω
RI	8.2000	Ω
Op amp rail	2300.0000	mV
Op amp input	1886.0000	mV (PK)
Op amp input	1333.8048	mV (RMS)
CT sec current	68.4002	mA
CT ratio	2000.0000	—
Primary current	136.8005	A

The output of TIDA-00777 can be connected to the current inputs designated Rogo_1_out and Rogo2_Out. TIDA-00777 output is compatible to ADS131A04 output when configured for 2.442 V reference. To connect the Rogowski inputs make the following changes:

- Remove R111, R113, C74, and C75.
- Connect current inputs to TP4 and TP6.

NOTE: Ensure the ground of the two boards are connected together.

2.2.2 Non-Isolated Voltage Measurement (With Potential Divider)

Figure 9 shows voltage input scaling amplifiers for two non-isolated voltage inputs.

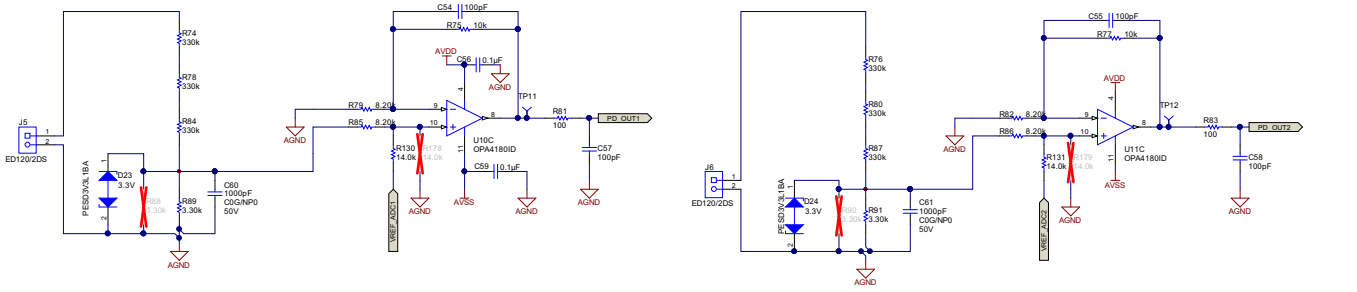


Figure 9. Voltage Input Signal Conditioning

This reference design provides the option to measure two non-isolated voltage inputs. One input is provided on each ADC. The AC input can be directly applied across the potential divider provided onboard. The output of the potential divider is connected to a fixed-gain amplifier. The amplifier is configured in differential mode and depending on the application and the input voltage range, the gain can be configured.

The output of the gain amplifier is connected to the ADC input.

Table 4 lists the input range calculation for voltage scaling of non isolated voltage input amplifiers.

Table 4. Input Range for Non-Isolated Voltage Input

VOLTAGE MEASUREMENT_PD	VALUE	UNIT
PD	993.3000	Ω
Gain	1.2195	—
RF	10.0000	Ω
RI	8.2000	Ω
Op amp rail	2300.0000	mV
Op amp input	1886.0000	mV (PK)
Op amp input	1333.8048	mV (RMS)
Volt division ratio	301.0000	—
Primary voltage	401.4752	V

2.2.3 Isolated Voltage Measurement Using AMC1200

Figure 10 shows the isolation amplifiers for voltage input.

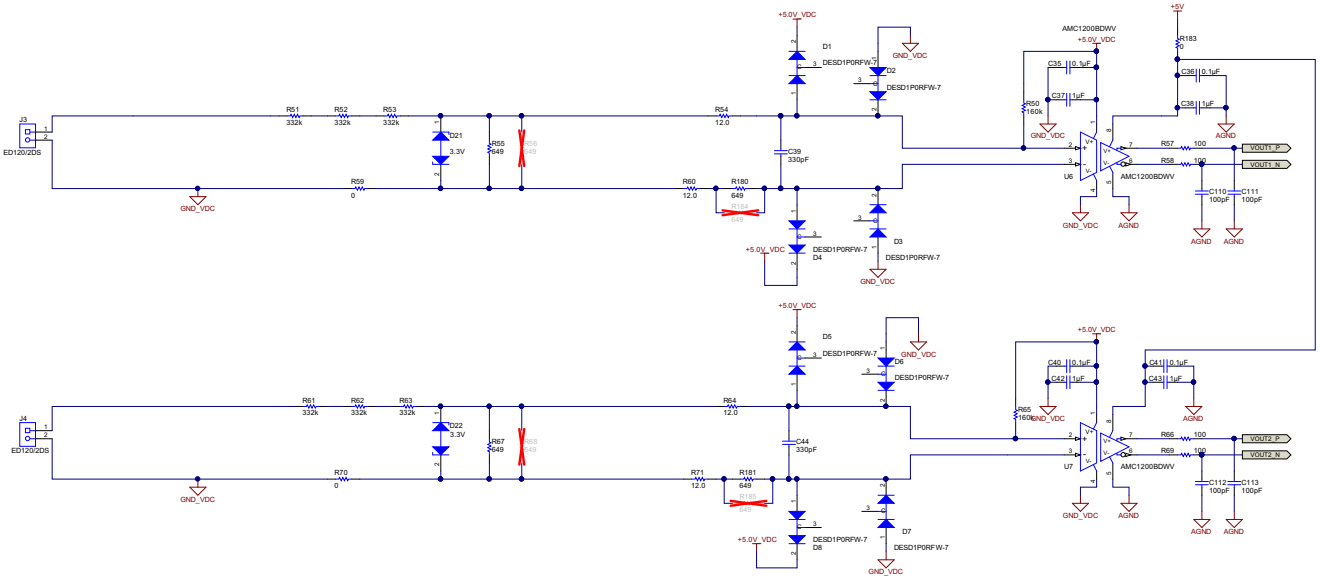


Figure 10. Isolation Amplifier With Input Protection and Potential Divider

The AMC1200 and AMC1200B are precision isolation amplifiers with an output separated from the input circuitry by a silicon dioxide (SiO2) barrier that is highly resistant to magnetic interference. This barrier has been certified to provide galvanic isolation of up to 4250 V_{PEAK} (AMC1200B) or 4000 V_{PEAK} (AMC1200) according to UL1577 and VDE V 0884-10. Used with isolated power supplies, these devices prevent noise currents on a high common-mode voltage line from entering the local ground and interfering with or damaging sensitive circuitry. The common-mode voltage of the output signal is automatically adjusted to either the 3- or 5-V low-side supply. The AMC1200 and AMC1200B are fully specified over the extended industrial temperature range of –40°C to 105°C and are available in a wide-body SOIC-8 package (DWV).

Features:

- ±250-mV input voltage range optimized for shunt resistors
- Very low nonlinearity: 0.075% maximum at 5 V
- Low offset error: 1.5-mV maximum
- Low noise: 3.1 mV_{RMS} typical
- Low high-side supply current: 8 mA maximum at 5 V
- Input bandwidth: 60-kHz minimum
- Fixed gain: 8 (0.5% accuracy)
- High common-mode rejection ratio: 108 dB
- 3.3-V operation on low side
- Certified galvanic isolation:
  - UL1577 and VDE V 0884-10 approved
  - Isolation voltage: 4250 V_{PEAK} (AMC1200B)
  - Working voltage: 1200 V_{PEAK}
  - Transient immunity: 10 kV/μs minimum
- Typical 10-year lifespan at rated working voltage
- Fully specified over the extended industrial temperature range

Find more information at the device's product page: http://www.ti.com/product/AMC1200

This reference design provides the option to measure two isolated voltage inputs. Isolation amplifiers are used to provide the required analog isolation. The isolator used provides basic isolation with a fixed gain of ×8. The common-mode output is set to 2.55 V in this design by applying 5-V supply. The AC input is specified to be linear up to ±250 mV input with saturation at ±312 mV. The output of the isolation amplifier is differentially connected to the ADC. The required protection for input overvoltage has been provided.

Table 5 provides calculations for scaling the voltage inputs to the isolation amplifier.

Table 5. Input Voltage Range Calculation for AMC1200

VOLTAGE MEASUREMENT _ISO AMP _AMC1200	VALUE	UNIT
PD	996.6500	Ω
Gain	8.0000	—
Output	2.0000	PK
RMS	1.4144	V
Input	0.1768	V
Volt division ratio	1533.0000	—
Primary voltage	271.0396	V

NOTE: The AMC1100 can be considered in the design based on the application.

NOTE: The OPA4188 can be consider for applications requiring improved accuracy performance.

2.2.4 Reference—LM4040 and Buffer (For DC Common-Mode Level Shift)

The reference and buffers are used to provide the required DC common-mode level shifting for using the ADC range (see Figure 11). Currently, internal ADC is used, and based on the application requirement, external reference can be configured.

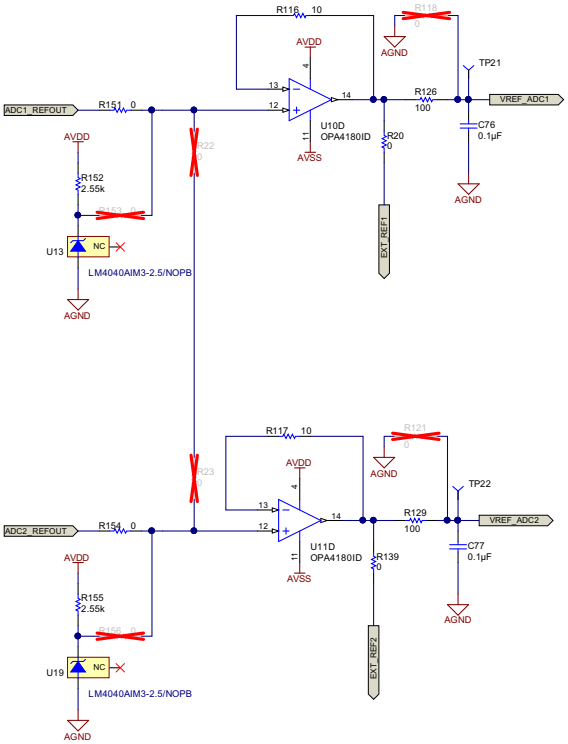


Figure 11. Reference With Buffer for Gain Amplifiers

The LM4040-N precision voltage reference is available in an SOT-23 surface-mount package. The advanced design of the LM4040-N eliminates the need for an external stabilizing capacitor while ensuring stability with any capacitive load, therefore making the LM4040-N easy to use. The minimum operating current increases from 60 µA for the 2.5-V LM4040-N to 100 µA for the 10-V LM4040-N. All versions have a maximum operating current of 15 mA.

The LM4040-N uses a fuse and Zener-zap reverse breakdown voltage trim during wafer sort to ensure that the prime parts have an accuracy of better than ±0.1% (A grade) at 25°C. Bandgap reference temperature drift curvature correction and low dynamic impedance ensure stable reverse breakdown voltage accuracy over a wide range of operating temperatures and currents.

Features:

- No output capacitor required
- Tolerates capacitive loads
- Key specifications (2.5-V LM4040-N)
  - Output voltage tolerance (A grade, 25°C): ±0.1% (maximum)
  - Low output noise (10 Hz to 10 kHz): 35 μV_{RMS} (typical)
  - Wide operating current range: 60 µA to 15 mA
  - Low temperature coefficient: 100 ppm/°C (maximum)

Table 6 lists the LM4040 features.

Table 6. LM4040 Features

PARAMETER	DETAILS
Part number	LM4040AIM3-2.5 / NOPB
Reference type	Shunt
Output type	Fixed
Voltage output (minimum or fixed)	2.5 V
Current output	15 mA
Tolerance	±0.1%
Temperature coefficient	100 ppm/°C
Noise: 10 Hz to 10 kHz	35 μV_{RMS}
Current cathode	65 µA
Supplier device package	SOT-23-3

The delta-sigma ADC operates with unipolar input or bipolar inputs. For bipolar inputs the reference is zero and for unipolar input the reference must be shifted – typically, the input range divided by 2. The amplifier outputs are level shifted depending on the input configuration. The references can be configured as follows:

1. Use ADC REFP out for DC level shifting the analog input.
   R151 and R154 mounted
   R153 and R156 not mounted
2. Use external Reference for DC level shifting the analog input.
   R153 and R156 mounted
   R151 and R154 not mounted

Based on the power supply configuration the reference output to the op amp gain amplifier can be selected as follows:

1. 0-V reference
   R118 and R121 mounted
   R126 and R129 not mounted
2. 2.5-V reference
   R126 and R129 mounted
   R118 and R121 not mounted

2.3 Power Supply

The delta-sigma ADC has flexible analog power-supply options for operation as follows:

- Unipolar supply: 3.3 to 5.5 V
- Bipolar supply: ±2.5 V
- Digital supply: 1.65 to 3.6 V

The power supplies required to operate the ADC are provided onboard. The power supply operates from a single positive input voltage (see Figure 12). The required overvoltage protection is provided using Zener diodes. Jumpers J11, J12, and J14 are used to configure the ADC analog supply input range.

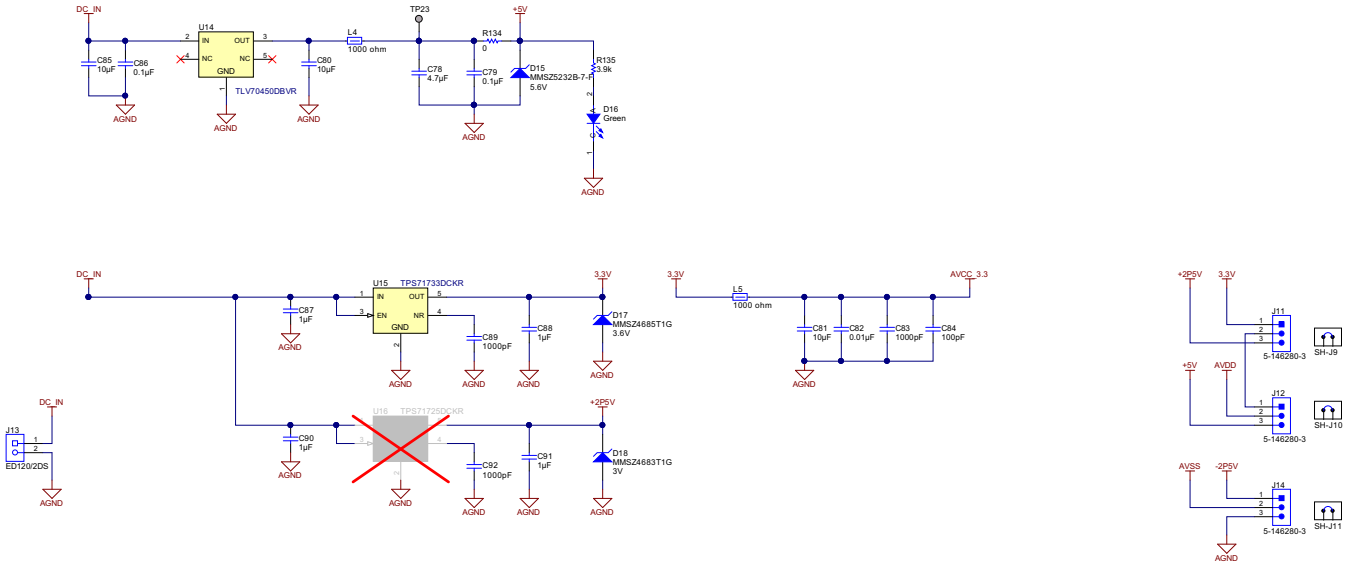


Figure 12. Onboard Positive Power Supply With Protection

2.3.1 Non-Isolated Power

2.3.1.1 +5 V (U14)

The TLV704 series of LDO regulators are ultra-low-quiescent current devices designed for extremely power-sensitive applications. Quiescent current is virtually constant over the complete load current and ambient temperature range. These devices are an ideal power-management attachment to low-power MCUs, such as the MSP430. The TLV704 operates over a wide operating input voltage of 2.5 to 24 V. Therefore, the device is an excellent choice for battery-powered systems and industrial applications that undergo large line transients.

Features:

- Wide input voltage range: 2.5 to 24 V
- Low 3.2-µA quiescent current
- Ground pin current: 3.4 µA at 100-mA I_{OUT}
- Stable with a low-ESR, 1-µF typical output capacitor

Table 7 lists the TLV70450 LDO features.

Table 7. TLV70450 LDO Features

PARAMETER	DETAILS
Part number	TLV70450DBVR
Regulator topology	Positive fixed
Voltage output	5 V
Current output	150 mA
Voltage dropout (typical)	0.85 V at 100 mA
Number of regulators	1
Voltage input	Up to 24 V
Current limit (minimum)	160 mA
Operating temperature	–40°C to 125°C
Supplier device package	SOT-23-5

2.3.1.2 +3.3 V (U15)

The TPS717xx family of LDO, low-power, linear regulators offers very high power-supply rejection (PSRR) while maintaining very low 45-μA ground current in an ultra-small, 5-pin SOT package. The family uses an advanced BiCMOS process and a PMOS pass device to achieve fast start-up, very low noise, excellent transient response, and excellent PSRR performance. The TPS717xx is stable with a 1-μF ceramic output capacitor and uses a precision voltage reference and feedback loop to achieve a worst-case accuracy of 3% overall load, line, process, and temperature variations.

Features:

- Input voltage: 2.5 to 6.5 V
- Available in multiple output versions:
  - Fixed output with voltages from 0.9 to 5 V
  - Adjustable output voltage from 0.9 to 6.2 V
- Ultra-high PSRR:
  - 70 dB at 1 kHz, 67 dB at 100 kHz, and 45 dB at 1 MHz
- Excellent load and line transient response
- Very low dropout: 170 mV typical at 150 mA
- Low noise: 30 μV_{RMS} typical (100 Hz to 100 kHz)

Table 8 lists the TPS71733 LDO features.

Table 8. TPS71733 LDO Features

PARAMETER	DETAILS
Part number	TPS71733DCKR
Regulator topology	Positive fixed
Voltage output	3.3 V
Current output	150 mA
Voltage dropout (typical)	0.17 V at 150 mA
Number of regulators	1
Voltage input	Up to 6.5 V
Current limit (minimum)	200 mA
Operating temperature	–40°C to 125°C
Supplier device package	SC-70-5

2.3.2 Power Supply Jumper Options

Table 9 shows the connectors configuration for a delta-sigma analog power supply.

Table 9. Power Supply for Delta-Sigma Analog supply

CONNECTOR	1-2	3-2
J11	NA	NA
J12	AVDD = 2.5 V	AVDD = 5 V
J14	AVSS = –2.5 V	AVSS = 0 V

2.3.3 Isolated Power

Figure 13 shows the transformer driver and LDO which generate an isolated power supply for the isolation amplifier.

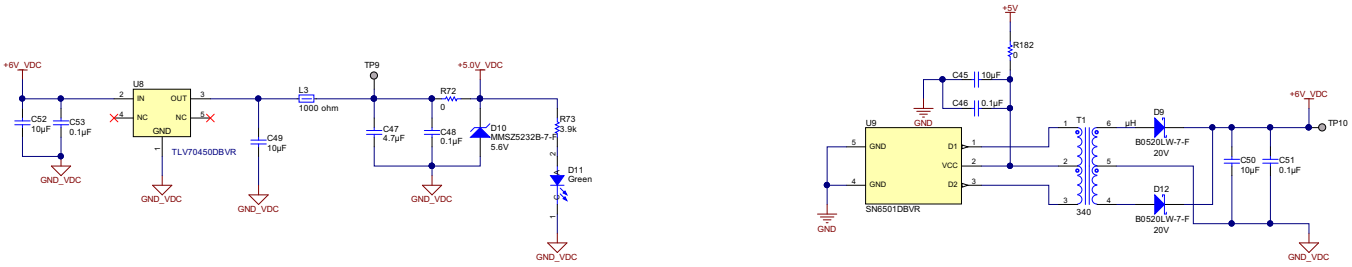


Figure 13. Isolated Power Supply for Isolation Amplifiers

The SN6501 is a monolithic oscillator and power-driver, specifically designed for small form factor, isolated power supplies in isolated interface applications. The device drives a low-profile, center-tapped transformer primary from a 3.3- or 5-V DC power supply. The secondary can be wound to provide any isolated voltage based on transformer turns ratio. The SN6501 consists of an oscillator followed by a gate drive circuit that provides the complementary output signals to drive the ground referenced N-channel power switches. The internal logic ensures break-before-make action between the two switches.

Features:

- Push-pull driver for small transformers
- Single 3.3- or 5-V supply
- High primary-side current drive:
  - 5-V supply: 350 mA (maximum)
  - 3.3-V supply: 150 mA (maximum)
- Low ripple on rectified output permits small output capacitors
- Small 5-pin SOT-23 package

Find more information at the device's product page: http://www.ti.com/product/SN6501

2.4 Delta-Sigma ADC Diagnostics

Table 10 lists the ADC selection table with pin compatibility.

Table 10. ADC Selection Table With Pin Compatibility

PARAMETER	ADC104S021	ADC084S021	ADC104S051	ADC104S101	ADC124S021
Resolution (bits)	10	8	10	10	12
Sample rate (maximum) (SPS)	200 kSPS	200 kSPS	500 kSPS	1 MSPS	200 kSPS
Number of input channels	4	4	4	4	4
Power consumption (typical) (mW)	94	1.6	2.7	3.9	2.2
Input range (minimum) (V)	0	0	0	0	0
Analog voltage AVDD (maximum) (V)	5.25	5.25	5.25	5.25	5.25
SNR (dB)	61.8	49.6	62.7	61.7	72

This reference design provides a method to diagnose the delta-sigma ADC. A low-resolution SAR ADC can be used. ADC104S021 10-bit or ADC124S021 12-bit ADC, which are pin compatible can be used in the design. This is a unipolar ADC. The 2.442-V or 2.5-V level shifted input is applied depending on the reference used. The ADC sample output is compared with the delta-sigma ADC output for diagnostics. The reference is diagnosed using comparators. The ADC is interface to the MCU using the SPI. Two chip selects are provided for selecting one of the two ADCs at a given time. The ADC input levels are compatible to the MCU output. To interface to the MCU, 5-V ADC output level must be shifted to 3.3 V. A single-channel level shifter does the level shifting. The ADC operates on 5 V and has internal reference. The SPI input is the clock for the ADC conversion.

2.4.1 SAR ADC—ADC104S021

Figure 14 shows the low resolution SAR ADC used for diagnostics interfaced to the MCU.

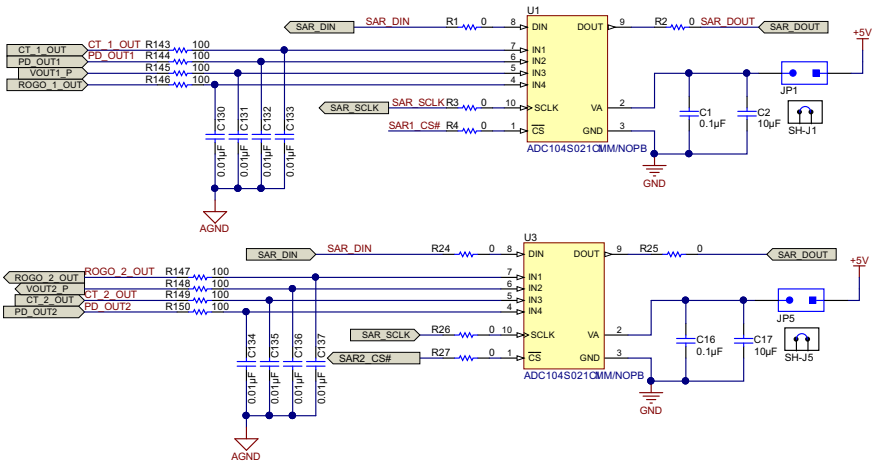


Figure 14. SAR ADC2 Configuration for Diagnostics

The ADC104S021 is a low-power, 4-channel CMOS, 10-bit ADC with a high-speed serial interface. The ADC104S021 and ADC104S021Q are fully specified over a sample rate range of 50 ksps to 200 ksps. The converter is based on a successive-approximation register architecture with an internal track-and-hold circuit. The ADC can be configured to accept up to four input signals at inputs IN1 through IN4.

The output serial data is straight binary, and is compatible with several standards, such as SPI™, QSPI™, MICROWIRE, and many common DSP serial interfaces. The ADC104S021 and ADC104S021Q operate with a single supply that can range from 2.7 to 5.25 V.

Features:

- Specified over a range of sample rates
- Four input channels
- Variable power management
- Single power supply with a 2.7- to 5.25-V range

Key specifications:

- DNL: ±0.13 LSB (typical)
- INL: ±0.13 LSB (typical)
- SNR: 61.8 dB (typical)
- Power consumption
  - 3-V supply: 1.94 mW (typical)
  - 5-V supply: 6.9 mW (typical)

Find more information at the device's product page: http://www.ti.com/product/ADC104S021

2.4.2 Comparator LMV331

Figure 15 shows the reference diagnostic comparators.

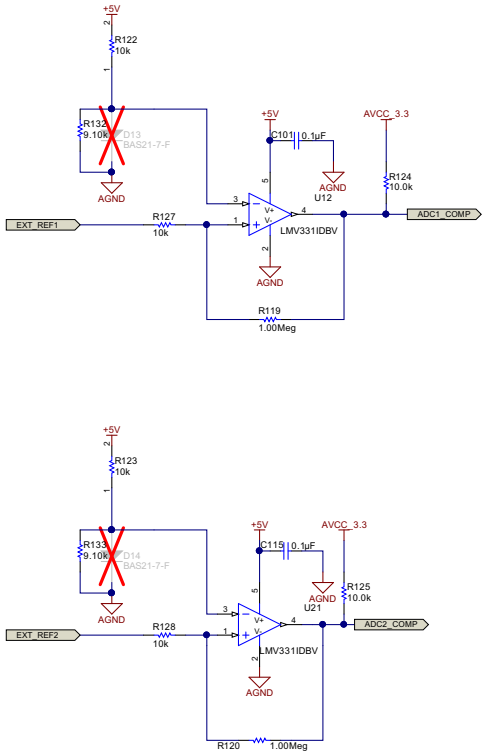


Figure 15. 2.5-V Reference Diagnostics Comparators

The LMV331 device is the single-comparator version. LMV331 devices are the most cost-effective solutions for applications where low-voltage operation, low power, and space saving are the primary specifications in circuit design for portable consumer products.

Features:

- 2.7-V and 5-V performance
- Low supply current
  - LMV331 130 µA (typical)
- Input common-mode voltage range includes ground
- Low output saturation voltage 200 mV (typical)
- Open-collector output for maximum flexibility

Find more information at the device's product page: http://www.ti.com/product/LMV331

2.4.3 Level Shifter—SN74LV1T34

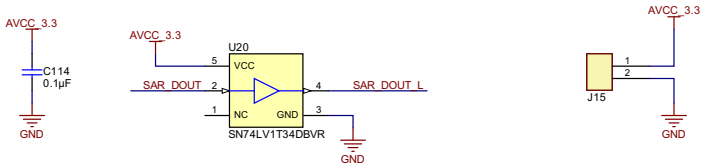


Figure 16. 5-V to 3.3-V Level Shifter for SAR ADC Interface to MCU

The SN74LV1T34 is a low-voltage CMOS gate logic that operates at a wider voltage range for industrial, portable, telecom, and automotive applications. The output level is referenced to the supply voltage and is able to support 1.8-, 2.5-, 3.3-, and 5-V CMOS levels.

The input is designed with a lower threshold circuit to match 1.8-V input logic at V_{CC} = 3.3 V and can be used in 1.8- to 3.3-V level up translation. In addition, the 5-V tolerant input pins enable down translation (for example, 3.3-V to 2.5-V output at V_{CC} = 2.5 V). The wide V_{CC} range of 1.8 to 5.5 V allows for generation of desired output levels to connect to controllers or processors. The SN74LV1T34 is designed with a current-drive capability of 8 mA to reduce line reflections, overshoot, and undershoot caused by high-drive outputs.

Features:

- Single-supply voltage translator at 5.0 V, 3.3 V, 2.5 V, and 1.8 V V_{CC}
- Operating range of 1.8 to 5.5 V
- Up translation
  - 1.2 to 1.8 V at 1.8 V V_{CC}
  - 1.5 to 2.5 V at 2.5 V V_{CC}
  - 1.8 to 3.3 V at 3.3 V V_{CC}
  - 3.3 to 5.0 V at 5.0 V V_{CC}
- Down translation
  - 3.3 to 1.8 V at 1.8 V V_{CC}
  - 3.3 to 2.5 V at 2.5 V V_{CC}
  - 5.0 to 3.3 V at 3.3 V V_{CC}
- Logic output is referenced to V_{CC}
- Output drive
  - 8.0-mA output drive at 5.0 V
  - 7.0-mA output drive at 3.3 V
  - 3.0-mA output drive at 1.8 V
- 5.0-V tolerance on input pins
- –40°C to 125°C operating temperature range

Find more information at the device's product page: http://www.ti.com/product/SN74LV1T34

2.4.4 SAR ADC to MCU Interface

Figure 17 shows the interface connections between SAR ADC and MSP432P401R MCU

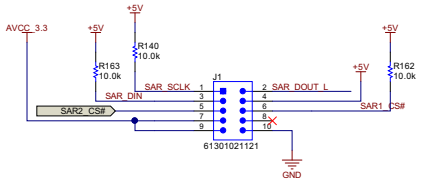


Figure 17. SAR ADC to MCU SPI Connector With Chip Select

2.5 Design Enhancements

2.5.1 Sampling Rate

This TI Design has been tested with the ADC configured to sample the analog input at 80 samples per cycle. The ADC can provide data rates up to 128 kSPS. There are 16 selectable oversampling ratio (OSR) options to optimize the converter for a specific data rate. Higher data rates are typically used in grid infrastructure applications that implement software resampling techniques to help with channel-to-channel phase adjustment for voltage and current. For more information, see Section 9.3.1, *Clock*, of the data sheet.

2.5.2 Using External Reference With ADS131A04

The delta-sigma ADC has an internal reference of 2.442 V. The dynamic range can be increased by using an external reference of 2.5 V. Provision to provide an external reference input to the delta-sigma ADC is provided.

In the ADS131A04 by default, the external reference is selected (INT_REFEN = 0). If reference output is required for testing before interfacing to the MCU, a low-cost reference can be used.

2.5.3 Using 4-V Reference for Analog Input Measurement

The differential input voltage range for ADS131A04 is –VREF / Gain to VREF / Gain. The internal reference can be programmed to either 2.442 V or 4 V. The dynamic range of the ADC can be improved by configuring VREF = 4 V. The VREF_4V bit can be set to 1, when VAVDD – VAVSS > 4.5 V. In the design the reference has been programmed to 2.442 V and tested. To use the 4-V reference, the ADC must be configured to measure bipolar input. By configuring VREF = 4 V, the input range can be increased from ±2.442 V to ±4 V, which increases the AC input range by ×1.65 compared to VREF = 2.442 V.

This configuration can be used when wider current ranges must be measured. The op amps used in the design can work for ±5 V. In this TI Design, ±5-V rails are available onboard. By making these simple changes in the design the input measurement range can be extended. Table 11 provides information to configure the power supply for different reference voltage configuration.

Table 11. Changes for Reference Configuration

REFERENCE	POPULATE	DEPOPULATE
2.442 V	R186 and R187	—
4 V	Use TP25 and TP26 to connect external voltage up to ±5 V	R186 and R187

2.5.4 Using ADS8688A for Diagnostics

The diagnostics feature is implemented with a unipolar 0- to 5-V input ADC. In applications with bidirectional input, ADS8688 or ADS8688A can be considered for diagnostics. ADS8688 and ADS8688A measure bidirectional input and operate on a single 5-V analog power supply input.

2.6 Board Design Guidelines

2.6.1 Delta-Sigma ADC

Recommendations:

- Partition the analog, digital, and power-supply circuitry into separate sections on the PCB.
- Use a single ground plane for analog and digital grounds.
- Place the analog components close to the ADC pins using short, direct connections.
- Keep the SCLK pin free of glitches and noise.
- Verify that the analog input voltages are within the specified voltage range under all input conditions.
- Tie unused analog input pins to GND.
- Provide current limiting to the analog inputs in case overvoltage faults occur.
- Use an LDO regulator to reduce ripple voltage generated by switch-mode power supplies. This reduction is especially true for AVDD, where the supply noise can affect performance.
- Keep the input series resistance low to maximize THD performance.
- Do not cross analog and digital signals.
- Do not allow the analog power supply voltages (AVDD – AVSS) to exceed 3.6 V under any conditions, including during power up and power down when the negative charge pump is enabled.
- Do not allow the analog power supply voltages (AVDD – AVSS) to exceed 6 V under any conditions, including during power up and power down when the negative charge pump is disabled.
- Do not allow the digital supply voltage to exceed 3.9 V under any conditions, including during power-up

2.6.2 ADC101C021 SAR ADC

For best accuracy and minimum noise, the PCB containing the ADC101C021 must have separate analog and digital areas. The areas are defined by the locations of the analog and digital power planes. Both of these planes should be on the same board layer. A single, solid ground plane is preferred if digital return current does not flow through the analog ground area. Frequently, a single ground plane design uses a fencing technique to prevent the mixing of analog and digital ground currents. Separate ground planes must be used only when the fencing technique is inadequate. The separate ground planes must be connected in one place, preferably near the ADC121C021. Take special care to ensure that signals do not pass over power plane boundaries. Return currents must always have a continuous return path below their traces.

The ADC101C021 power supply must be bypassed with 4.7-μF and 0.1-μF capacitors as close as possible to the device with the 0.1-μF capacitor located right at the device supply pin. The 4.7-μF capacitor must be a tantalum type and the 0.1-μF capacitor must be a low ESL type. The power supply for the ADC101C021 must be used only for analog circuits. Avoid the crossover of analog and digital signals and keep the clock and data lines on the component side of the board. The clock and data lines must have controlled impedances.

2.6.3 AMC1200

See Section 10 *Layout* in the data sheet for the PCB design and layout guidelines.

2.6.4 CDCLVC1102PW

See Section 11 *Power Supply Recommendations* and Section 12 *Layout* in the data sheet for the PCB design and layout guidelines.

2.7 Software Implementation

This section discusses the software implementation. The first subsection discusses the software used to setup the MSP432P401R peripherals, ADS131A04 ADC, and ADC104S021 ADC. Subsequently, the metrology software is described as two major processes: the foreground process and background process.

2.7.1 Setup Software

2.7.1.1 MCU Setup

The MCU is used to set up the ADS131A04 and ADC104S021, calculate metrology parameters, and communicate these parameters through RS-232 to a terminal program.

2.7.1.1.1 GPIO, SPI, and UART Setup

For communication of the metrology parameters, a UART port is used on the MCU. The UART communication is set to a baud rate of 57600 with 8 data bits, no parity, and a 1 stop bit. By connecting the UART port pins to an isolated UART and then to the RS-232 board (such as TIDA-00163), the metrology parameters calculated by the MCU can be displayed by a PC using a terminal program.

For communication to the ADS131A04 and ADC104S021, two different SPI ports are used. The SPI clock for both of these ports is set to 3 MHz with the MSB shifted out first. These different SPI ports are independent of each other, but are used to communicate to the two devices of a particular ADC. For example, the ADS131A04 uses the same UCB0 port for the two ADS131A04 devices on this board. Similarly, the ADC104S021 uses the same UCB2 port for the two ADC104S021 devices.

In addition to the normal SPI lines used to communicate to the A04, the A04 devices also use additional GPIO lines for communication. One of these additional GPIO pins is used to provide a reset signal to the ADS131A04 to get it to a known state before sending commands. The second GPIO pin is connected to the DRDY pin of the ADS131A04. This pin is used to alert the MCU of a new set of ADS131A04 ADC samples now ready, so that the MCU can query the ADS131A04 devices for these new ADC samples. To immediately alert the MCU of the new ADC samples, the MCU GPIO pin connected to DRDY is configured as an interruptible input.

As a method to determine when there is an issue with the ADC reference of the A04 devices, the board also has comparators which compare the ADS131A04 references to a set voltage threshold. By connecting the output of these comparators to the corresponding interruptible GPIO pins on the MCU, the state of the two ADC references can be logged.

In the application, the GPIO associations listed in Table 12 are used.

Table 12. GPIO Associations

PORT PIN	FUNCTION
RS-232 GPIO CONFIGURATION	
P3.2 (UCA2 UART port)	UART receive for RS-232 communication
P3.3 (UCA2 UART port)	UART transmit for sending metrology parameters using RS-232
ADS131A04 GPIO CONFIGURATION	
P5.2	ADS131A04 chip select
P1.5 (UCB0 SPI port)	ADS131A04 SPI clock
P1.6 (UCB0 SPI port)	ADS131A04 SPI input (SIMO)
P1.7 (UCB0 SPI port)	ADS131A04 SPI output (MISO)
P3.0	ADS131A04 DRDY
P4.5	ADS131A04 RESET
ADS131A04 REFERENCE CHECK GPIO CONFIGURATION	
P2.7	ADCREF1 OK (for status of U2 reference)
P2.6	ADCREF2 OK (for status of U4 reference)
ADC104S021 GPIO CONFIGURATION	
P5.0	Chip select 1 for U1 device on the board
P5.1	Chip select 2 for U3 device on the board
P3.5 (UCB2 SPI port)	ADC104S021SPI clock
P3.6 (UCB2 SPI port)	ADC104S021SPI input (SIMO)
P3.7 (UCB2 SPI port)	ADC104S021SPI output (MISO)

2.7.1.1.2 Clocks

The MSP432P401R uses multiple clocks in this application. Table 13 lists the different clock settings used in this application.

Table 13. Application Clock Settings

PORT PIN	FUNCTION
MASTER CLOCK (MCLK, CPU CLOCK)	
Clock frequency	48 MHz (clock divider = 1)
Number of flash wait states	2
Clock source	MCU internal DCO
SUBSYSTEM MASTER CLOCK (SMCLK)	
Clock frequency	24 MHz (clock divider = 2)
Clock source	MCU internal DCO
AUXILIARY CLOCK (ACLK)	
Clock frequency	32768 Hz
Clock source	32768 kHz crystal
RS-232	
Speed	57600 baud
Clock source	SMCLK
TIMER FOR UPDATE OF METROLOGY PARAMETERS	
Timer used	Timer A0
Clock source	ACLK
Generated interval	1 second (32768 counts)
Timer mode	Up mode
ADC104S021 SPI CLOCK	
Clock frequency	3 MHz (clock divider = 8)
Clock source	SMCLK
Clock polarity	Inactive state is high (UCCKPL = 1)
Clock phase	Data is valid on clock leading edge (UCCKPH = 0)
ADS131A04 SPI CLOCK	
Clock frequency	3 MHz (clock divider = 8)
Clock source	SMCLK
Clock polarity	Inactive state is low (UCCKPL = 0)
Clock phase	Data is valid on clock leading edge (UCCKPH = 0)

2.7.1.1.3 Direct Memory Access (DMA)

The DMA module is used to transfer all ADS131A04 and ADC104S021 ADC samples from these devices to the memory of the MCU with minimal bandwidth requirements from the CPU. To get the ADC sample data from the ADC devices, the MCU requires writing data to the SPI transmit buffers to activate the SPI clocks. The DMA module is used to not only transfer the received SPI data to memory, but also to write the dummy data to the SPI transmit buffers of the MCU so that the receive operations can be triggered. As a result, two DMA channels are used for each of SPI port used to communicate to an ADC; one channel is used to send the dummy data from MCU memory to the SPI transmit buffers and the other channel is used to move the received SPI data to the memory of the MCU. Once the transfer is complete, an interrupt is generated to complete any necessary post-transfer processing.

Table 14 lists the DMA channel associations.

Table 14. DMA Channel Associations

DMA CHANNEL NUMBER	FUNCTION
0	ADS131A04 SPI transmit (for triggering receive)
1	ADS131A04 SPI receive
2	Not used
3	Not used
4	ADC104S021 SPI transmit (for triggering receive)
5	ADC104S021 SPI receive
6	Not used
7	Not used

2.7.1.1.4 Interrupt Priorities

The software has five interrupts that are prioritized. Table 15 lists these interrupt priorities.

Table 15. Interrupt Priorities

INTERRUPT	SIGNIFICANCE	PRIORITY CODE
DMA1	Transfer of ADS131A04 ADC samples to MCU memory is completed.	0x20
PORT3	New ADS131A04 ADC samples are generated so the MCU can now query the ADS131A04 device for new ADC samples.	0x40
DMA2	Transfer of ADC104S021 ADC samples to MCU memory is completed.	0x60
TA0_0	It is time to send a new metrology parameter for RS-232 communication.	0x80
EUSCIA2	Transmit buffer for RS-232 communication is empty so a new byte of the RS-232 communication packet can be sent.	0x80

In Table 15, the interrupts with the lower priority code value have higher interrupt priority. In the software, communication to the terminal is a relatively low priority so the TA0_0 and EUSCIA2 priorities have the highest priority code. The DMA2 interrupt has the next lowest priority because no time-critical processing is required in this interrupt. For the PORT3 interrupt, a high-priority interrupt is selected because this interrupt is where the majority of the sample processing is done. The DMA1 interrupt has the highest priority because a CRC is performed on the sample data received from the ADS131A04 in this interrupt; and if there are any CRC errors are present it must be detected as soon as possible so that the MCU can request and receive the sample data again before the next ADC sample is ready.

2.7.1.2 ADS131A04 Setup

For communication to the ADS131A04 devices, the device chaining feature of these devices is enabled so that communication to the two ADS131A04 devices is achieved transparently by concatenating the packets to be sent to the two A04 devices into one merged packet. The merged packed is sent out through the shared SPI lines. This method of chaining does not use two different chip select lines from the MCU like the method used for the ADC104S021 devices.

After reset, the MCU device first sends a reset signal to the ADS131A04 device to get it to a known state. After resetting the ADS131A04 devices, commands are sent to these devices to initialize them. These setup commands are sent out manually to the software so a DMA is not used to transfer this command data to the ADS131A04. The order of commands sent follows:

1. Send an UNLOCK command to the ADS131A04 until an UNLOCK ACK is received from both ADS131A04 devices.
2. Send a WAKEUP command to the ADS131A04 until a WAKEUP ACK is received from both ADS131A04 devices.
3. Send a command to set the ICLK divider of the A04 devices to 2. Keep sending this command until the appropriate ACK is received.
4. Send a command to set the OSR to 256 and the Modclk divider to either 8 (for 50-Hz nominal line frequency) or 6 (for 60 Hz nominal line frequency). This setting results in a sample rate of 4000 samples per second whenever the software is configured for a line frequency of 50 Hz and a sample rate of 5333.3 whenever the software is configured for a line frequency of 60 Hz. Keep sending this command until the appropriate ACK is received.
5. Send a command to the A04 devices to use the following configuration:
   - High-resolution mode
   - Negative charge pump disabled
   - Internal reference enabled

   Keep sending this command until the appropriate ACK is received.
6. Send a command to the A04 devices to use a fixed frame size of six words. In the hardware configuration of the board, each word is set to be 24 bits long so this results in a communication frame size of 18 bytes per ADS131A04 device. Keep sending this command until the appropriate ACK is received.
7. Send a command to enable all of the ADS131A04 ADCs. Keep sending this command until the appropriate ACK is received.
8. Send a command to the A04 devices to use the following configuration:
   - CRC is enabled on all bits received and transmitted.
   - Time before the device asserts the done signal after the LSB is shifted out is set to 12 ns.
   - Time before the device asserts Hi-Z on Dout after the LSB of the data frame is shifted out is 12 ns.

After the ADS131A04 devices are set up, the ADC alerts the MCU of new sample data that is available. This alert is done by providing GPIO interrupts from the DRDY pin of the ADS131A04. After receiving one of these interrupts, the MCU needs only to write dummy data into the SPI transmit buffers so that it can receive the ADC sample data from the ADS131A04 devices. The ADS131A04 automatically sends this sample data out through the SPI port so no command data must be sent to the ADS131A04 once set up.

Due to the chaining of the two ADS131A04 devices, the received data frame consists of the data frames of each A04 device. This means that a total of twelve 24-bit words (36 bytes) are sent from the ADS131A04 devices. The first six words sent correspond to the first ADS131A04 device (designated as U2 on the PCB) and the last six words correspond to the second ADS131A04 device (designated as U4 on the PCB). Figure 18 shows the order of words in a data frame that is received from each individual ADS131A04 device by the MCU.

Figure 18. Words Received From Each ADS131A04 Device

In the data received from an A04 device, the first word provides a status update of the ADC internal system monitor. The next four words represent the ADC samples. The last word is the CRC word that is calculated by the ADS131A04. When this packet is received by the MCU, it extracts the CRC word, calculates its own CRC based on the values of the other words in the packet, and compares the two CRCs to ensure that no data transmissions have occurred. To accelerate the CRC calculation, the CRC module of the MCU performs the CRC calculations of the first 14 bytes of the 15-byte data used in the calculation. If the two CRCs match, the received sample words are parsed into the corresponding ADC sample data for use for metrology calculations. If the two CRCs do not match, the MCU initializes the resending of the sample data.

The ADC samples of the two ADS131A04 devices are concatenated to form a single array of eight ADC samples. Table 16 lists the channel associations used for these eight channels. These channel mappings differ when compared to the channel mappings of the ADC104S021.

Table 16. ADS131A04 ADC Channel Associations

SOFTWARE CHANNEL NUMBER	ADC NAME (PCB DESIGNATION)	ADC CHANNEL NUMBER	CORRESPONDING HEADER (PCB DESIGNATION)
0	U2	0	J7 (current transformer 1)
1	U2	1	J5 (potential divider 1)
2	U2	2	J10 (Rogowski 1)
3	U2	3	J3 (AMC 1)
4	U4	0	J4 (AMC 2)
5	U4	1	J9 (Rogowski 2)
6	U4	2	J8 (current transformer 2)
7	U4	3	J6 (potential divider 2)

2.7.1.3 ADC104S021 Setup

For communication to the ADC104S021, the only command that must be sent to the ADC is the next ADC channel to sample. In the software, a total of five 16-bit words (10 bytes) are sent as a packet to the ADC. Simultaneously, a total of five 16-bit words are read and then parsed to extract the values of the ADC sample data. The SPI transmission and reception from the ADC104S021 is done by the DMA module of the MCU. The extracted ADC sample data received from the ADC104S021 is translated into a signed 16-bit number for further processing. This translation allows the ADC results from the ADC104S021 to be treated as a 16-bit signed number when performing mathematical operations.

Words 1 through 4 sent to the ADC are used to select the next ADC to sample. In the software, all four channels of the ADC104S021 devices are sampled every time the SAR ADC is triggered. The corresponding ADC sample data is contained in words 2 to 5 of the response sent by the ADC. Word 1 of the ADC response is not used by the software. Also, to ensure that the fifth response word is read by the MCU, a dummy value is written to the SPI transmit buffer for the fifth transmission word. Writing this dummy value enables the SPI clock so that the fifth response word can be obtained. Figure 19 shows the order of the words written and received by the MCU in a data frame.

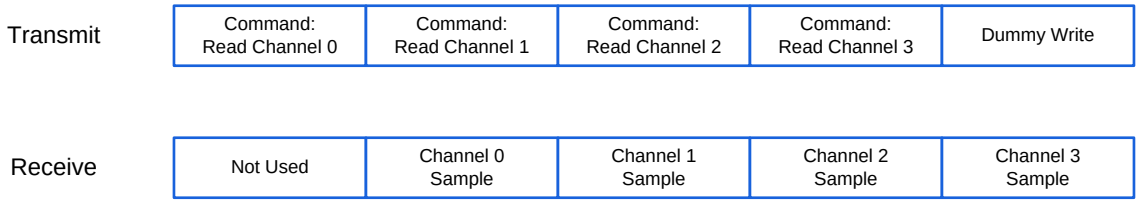


Figure 19. Words Sent and Received in ADC104S021 Data Frame

In this TI Design, all four channels of an ADC104S021 device are sampled every time a new set of ADS131A04 sample readings are generated. To enable sensing both ADC104S01 devices in this TI Design, the actual ADC104S021 device that is enabled is alternated every sample by toggling the individual ADC104S021 chip-select lines. As a result, the sampling rate of the ADC104S021 samples is half of the sample rate of the ADS131A04 samples.

The ADC samples of the two ADC104S021 devices are concatenated to form a single array of eight ADC samples. Table 17 lists the channel associations used for these eight channels. These channel mappings differ when compared to the channel mappings of the ADS131A04.

Table 17. ADC104S021 ADC Channel Associations

SOFTWARE CHANNEL NUMBER	ADC NAME (PCB DESIGNATION)	ADC CHANNEL NUMBER	CORRESPONDING HEADER (PCB DESIGNATION)
0	U1	0	J7 (current transformer 1)
1	U1	1	J5 (potential divider 1)
2	U1	2	J3 (AMC 1)
3	U1	3	J10 (Rogowski 1)
4	U3	0	J9 (Rogowski 2)
5	U3	1	J4 (AMC 2)
6	U3	2	J8 (current transformer 2)
7	U3	3	J6 (potential divider 2)

2.7.2 Foreground Process

The foreground process includes the initial setup of the hardware and MCU software immediately after a device RESET. Figure 20 shows the flowchart for this process.

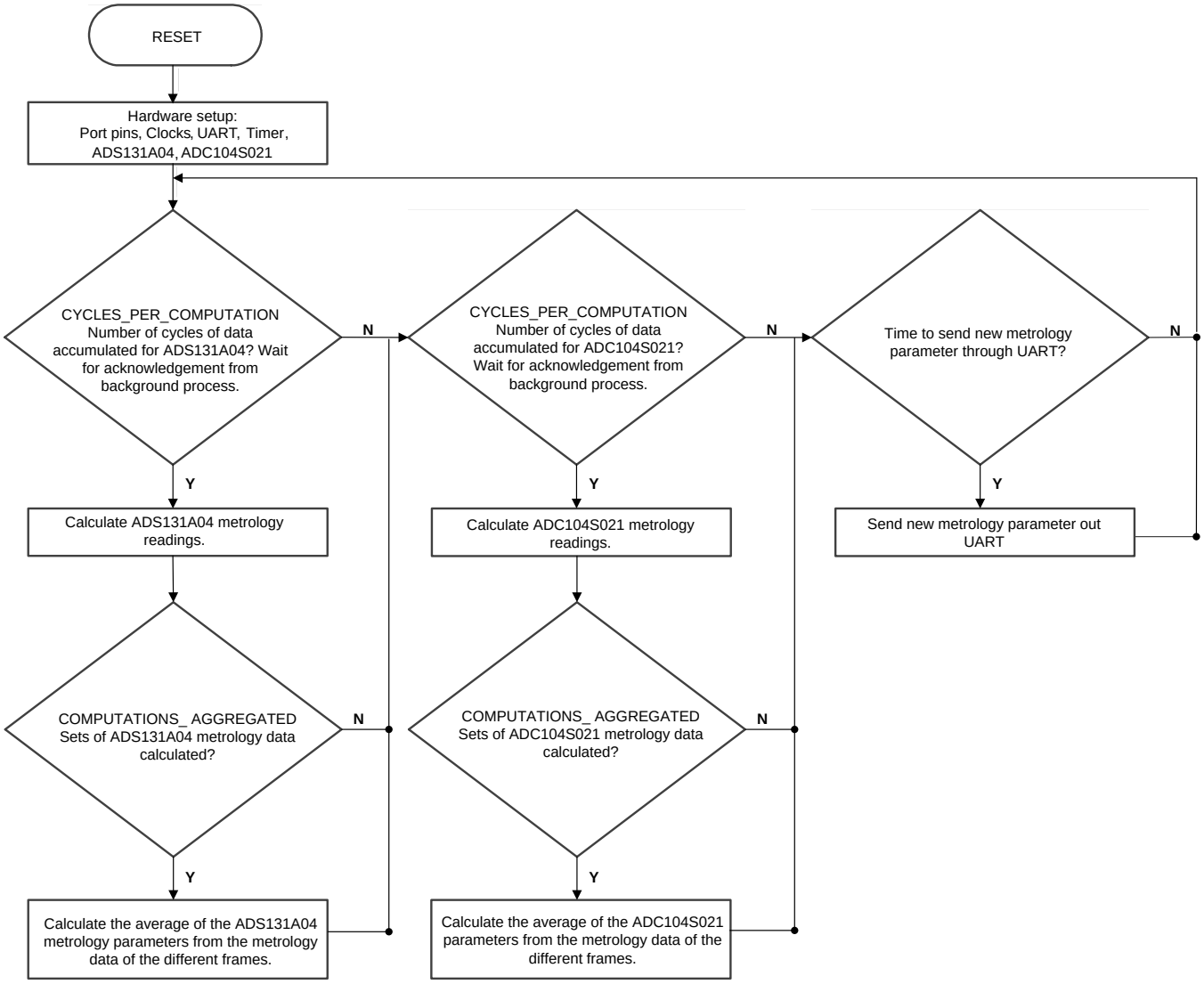


Figure 20. Foreground Process

The initialization routines involve the following:

- Setup of the GPIO port pins, clock system, and UART for metrology
- Parameter communication and its associated timer for triggering sending new parameters through the UART
- Software for enabling communication to the ADS131A04 and ADC104S021

A description of this setup software is provided in Section 2.7.1.

After the hardware is set up, the foreground process checks whether the background process has notified the foreground process to calculate new metering parameters based on the samples from the ADS131A04 devices. This notification is sent by asserting the PHASE_STATUS_NEW_LOG status flag whenever a frame of data is available for processing. The data frame consists of the processed dot products that were accumulated for the number of cycles that are set by the CYCLES_PER_COMPUTATION setting. By default, this macro is set to one tenth of the nominal frequency (that is, five cycles for a 50-Hz nominal frequency and six cycles for a 60-Hz nominal frequency).

The processed dot products for the ADS131A04-based metrology parameters include RMS voltage, RMS current, active power, and reactive power. The foreground process uses these dot products to calculate the corresponding metrology readings in real-world units. Using the calculated values of active and reactive power of the foreground, the apparent power is calculated. The frequency (Hz) and power factor are also calculated using parameters calculated by the background process using the formulas in Section 2.7.2.1. After the ADS131A04-based metrology parameters for one frame are calculated, the parameters are stored until a certain number of frames of ADS131A04-based frames of data have been computed. Once this number of frames of parameters (set by the COMPUTATIONS_AGGREGATED macro) has been calculated, they are averaged together to generate the aggregated metrology parameters. A similar process is also used to calculate the ADC104S021-based metrology parameters except only RMS voltage, RMS current, and frequency are calculated.

After checking whether it is time to calculate new ADS131A04- or ADC104S021-based metrology parameters, whether it is time to send out a new parameter through the UART port is also checked. A timer is used to generate the intervals between sending consecutive metrology parameters. In this software, this interval is set by default to 1 second.

2.7.2.1 Formulas

This section briefly describes the formulas used for the voltage, current, and power.

As previous sections describe, voltage and current samples are obtained at a sampling rate of either 4000 Hz (for a nominal frequency of 50 Hz) or 5333.3 Hz (for a nominal frequency of 60 Hz). All of the samples are taken over the number of cycles set by the CYCLES_PER_COMPURATION macro. The RMS values are obtained by the following formulas:

$$V_{RMS,\,ADS131A04} = K_{v,ADS13104} \times \sqrt{\frac{\sum_{n=1}^{\text{Sample count } v_{ADS131A04}} v_{ADS131A04}(n) \times v_{ADS131A04}(n)}{\text{Sample count}_{ADS131A04}}} - V_{offset,\,ADS131A04} \quad (1)$$

$$I_{RMS,\,ADS131A04} = K_{i,ADS13104} \times \sqrt{\frac{\sum_{n=1}^{\text{Sample count } v_{ADS131A04}(n)} i_{ADS131A04}(n) \times i_{ADS131A04}(n)}{\text{Sample count}_{ADS131A04}}} - i_{offset,\,ADS131A04} \quad (2)$$

$$V_{RMS,\,ADC104S021} = K_{v,ADC104S021} \times \sqrt{\frac{\sum_{n=1}^{\text{Sample count } v_{ADC104S021}(n)} v_{ADC104S021}(n) \times v_{ADC104S021}(n)}{\text{Sample count}_{ADC104S021}}} - v_{offset,\,ADC104S021} \quad (3)$$

$$I_{RMS,\,ADC104S021} = K_{i,ADC104S021} \times \sqrt{\frac{\sum_{n=1}^{\text{Sample count}_{ADC104S021}} i_{ADC104S021}(n) \times i_{ADC104S021}(n)}{\text{Sample count}_{ADS104S021}}} - i_{offset,\,ADC104S021} \quad (4)$$

Where:

- $v_{ADS131A04}(n)$ = ADC sample from the voltage channel of ADS131A04, taken at sample instant n
- $v_{offset,\ ADS131A04}$ = Offset used to subtract effects of the additive white Gaussian noise from the ADS131A04 ADC used to measure voltage
- $i_{ADS131A04}(n)$ = ADC sample from the current channel of the ADS131A04, taken at sample instant n
- $i_{offset,\ ADS131A404}$ = Offset used to subtract effects of the additive white Gaussian noise from the ADS131A04 current converter
- Sample $count_{ADS131A04}$ = Number of samples accumulated in the ADS131A04 window defined by the CYCLES_PER_COMPUTATION number of mains cycles
- $K_{v,ADS131A04}$ = Scaling factor for the voltage measured by the ADS131A04
- $K_{i,ADS131A04}$ = Scaling factor for current measured by the ADS131A04
- $v_{ADC104S021}(n)$ = ADC sample from the voltage channel of the ADC104S021, taken at sample instant n
- $v_{offset,\ ADC104s021}$= Offset used to subtract effects of the additive white Gaussian noise from the ADS104S021 ADC used to measure voltage
- $i_{ADC104S021}(n)$ = ADC sample from the current channel of the ADC104S021, taken at sample instant n
- $i_{offset,\ ADC104S021}$ = Offset used to subtract effects of the additive white Gaussian noise from the ADC104S021 current converter
- Sample $count_{ADC104S021}$ = Number of samples accumulated in the ADC104S021 window defined by the CYCLES_PER_COMPUTATION number of mains cycles
- $K_{v,\ ADC104S021}$ = Scaling factor for the voltage measured by the ADC104S021
- $K_{i,\ ADC104S021}$ = Scaling factor for current measured by the ADC104S021

Using the ADS131A04 current and voltage samples, power is calculated for a frame's worth of active and reactive energy samples. These samples are phase corrected and passed on to the foreground process, which uses the number of samples (sample count ADS131A04) to calculate phase active and reactive powers through the following formulas:

$$P_{ACT} = K_{ACT} \frac{\sum_{n=1}^{\text{Sample count}_{ADS131a04}} v_{ADS131A04}(n) \times i_{ADS131A04}(n)}{\text{Sample count}_{ADS131A04}} \quad (5)$$

$$P_{REACT} = K_{REACT} \frac{\sum_{n=1}^{\text{Sample count}_{ADS131A04}} v_{90,ADS131A04}(n) \times i_{ADS131A04}(n)}{\text{Sample count}_{ADS131A04}} \quad (6)$$

$$P_{App} = \sqrt{P_{ACT}^2 + P_{REACT}^2} \quad (7)$$

Where:

- $v_{90,\ ADS131A04}(n)$ = Voltage sample of the waveform that results from shifting $v_{ADS131A04}(n)$ by 90°, taken at a sample instant n
- K_{ACT} = Scaling factor for active power
- K_{REACT} = Scaling factor for reactive power

For reactive energy, the 90° phase-shift approach is used for two reasons:

- This approach allows accurate measurement of the reactive power for very small currents.
- This approach conforms to the measurement method specified by IEC and ANSI standards.

The calculated mains frequency from the ADS131A04 voltage channel is used to calculate the 90° shifted voltage sample. Because the frequency of the mains varies, it is important to first accurately measure the mains frequency to phase shift the voltage samples accordingly.

To get an exact 90° phase-shift, interpolation is used between two samples. For these two samples, a voltage sample slightly more than 90° before the current sample is used and a voltage sample slightly less than 90° before the current sample is used. The phase-shift implementation of the application consists of an integer part and a fractional part. The integer part is realized by providing an N samples delay. The fractional part is realized by a 1-tap FIR filter. In the software, a lookup table provides the filter coefficients used to create the fractional delays.

The background process also calculates the frequency in terms of samples per mains cycle. The foreground process then converts this samples per mains cycle to Hz by the following formulas:

$$\text{Frequency}_{\text{ADS131A04}}\,(\text{Hz}) = \frac{\text{Sampling Rate}_{\text{ADS131A04}}\,(\text{samples / second})}{\text{Frequency}_{\text{ADS131A04}}\,(\text{samples / cycle})} \tag{8}$$

$$\text{Frequency}_{\text{ADC104S021}}\,(\text{Hz}) = \frac{\text{Sampling Rate}_{\text{ADC104S021}}\,(\text{samples / second})}{\text{Frequency}_{\text{ADC104S021}}\,(\text{samples / cycle})} \tag{9}$$

2.7.3 Background Process

Figure 21 shows the background process, which mainly handles timing critical events in software. The background process uses the assertion of the DRDY signal to provide a GPIO interrupt to the MCU whenever new ADS131A04 samples are ready. The port interrupt is used to retrieve the sample data from the ADS131A04 and also trigger the ADC104S021 to start conversions and retrieve the new ADC104S021 values. While retrieving the ADC samples from the ADS131A04 and ADC104S021 devices using DMA, per-sample processing is done on the previous set of ADS131A04 and ADC104S021 samples. These ADC samples are stored in arrays for any desired ADC sample analysis. The sample processing is not done on every ADC channel, but it is done on the channels that are designated as the voltage ADC channel and the current ADC channel. The sampling processing done on the ADS131A04 sample data is done by the DS_processing function while the sample processing done on the ADC104S021 is done by the SAR_processing function.

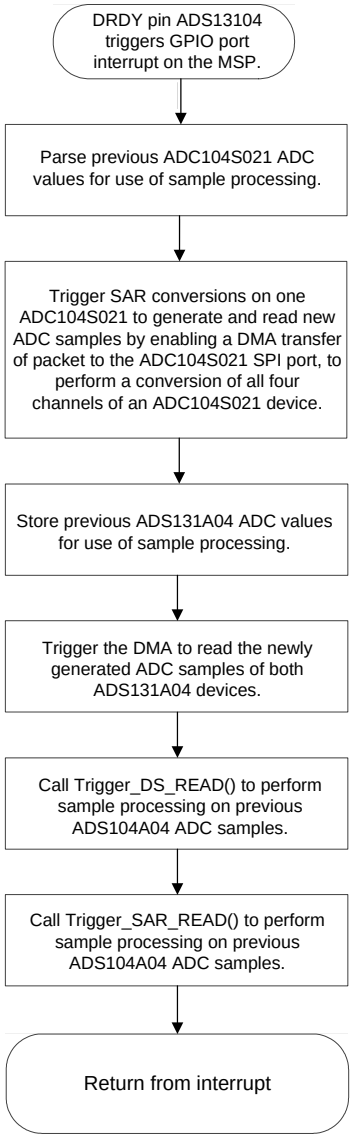


Figure 21. Background Process

Once the ADS131A04 response packet is completely transmitted from the ADS131A04 to the MCU, a DMA1 interrupt is generated. Figure 22 shows what occurs in the DMA1 ISR. In the DMA1 ISR, the packet received from the ADS131A04 has its sent CRC compared to the CRC calculated by the MCU, to ensure that the data is accurately transmitted to the MCU. This CRC check is done on each ADS131A04 device. If the CRC check passes for an ADS131A04 device, the corresponding packet for that ADS131A04 device is parsed to extract the sample values of the four ADC channels for that device. Sample processing is performed for these new ADC values during the next port interrupt that is generated by the DRDY pin of the ADS131A04. If any of the ADS131A04 devices do not pass the CRC check, then the DMA triggers rereading of the received data from all ADS131A04 devices. However, if only one of the ADS131A04 devices previously failed the CRC check, once the retransmitted data is received for both ADS131A04 devices only the packet of the ADS131A04 device that failed the CRC check is parsed if it passes the CRC check this time. There is no need to parse the data for the ADS131A04 that previously passed the CRC check because the correct data was already parsed when it previously passed the CRC check.

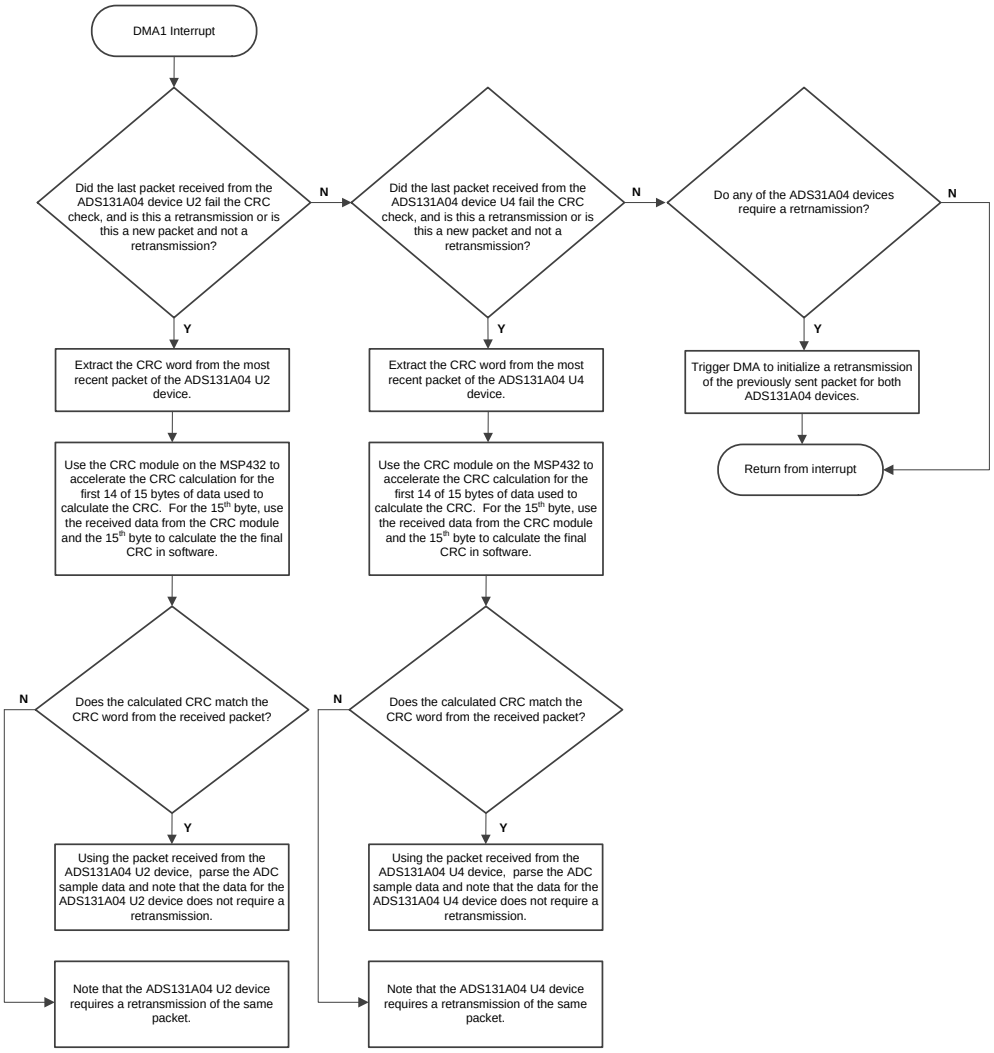


Figure 22. DMA1 ISR

After the MCU receives the response packet from the ADC104S021 device, a DMA2 interrupt is generated. In the DMA2 ISR, the state of the chip-select lines for both ADC104S021 devices are toggled so that the currently enabled ADC104S021 device is disabled and the currently disabled ADC104S021 device is enabled. The next time the SAR ADC is triggered, the most recently enabled ADC104S021 device performs conversions on all of its channels while the other ADC104S021 device is disabled. This causes the different ADC104S021 devices to have a sample rate that is half of the ADS131A04.

2.7.3.1 Sample Processing

Figure 23 shows the flow chart for the DS_processing function. The DS_processing function uses the ADS131A04 24-bit ADC samples to calculate intermediate dot product results that are fed into the foreground process for the calculation of the ADS131A04-based metrology readings. The current and voltage samples are processed and accumulated in dedicated 64-bit variables. In addition, active power and reactive power are also accumulated in dedicated 64-bit variables.

Figure 24 shows the flow chart for the SAR_processing function. The SAR_processing function uses the ADC104S021 ADC samples to calculate intermediate dot product results that are fed into the foreground process for the calculation of the ADC104S021-based metrology readings. The ADC104S021 ADC samples are translated from an unsigned 10-bit representation to a 16-bit signed integer representation for mathematical operations. The current and voltage samples are processed and accumulated in dedicated 64-bit variables. Because power is calculated only from the ADS131A04 ADCs, active power and reactive power are not accumulated in the SAR_processing function.

For both DS_processing and SAR_processing functions, arrays of the five largest ADC voltage and current samples within a mains cycle as well as arrays of the five smallest ADC readings within the same mains cycle are stored. Each of the five largest ADC samples for the ADS131A04 and the five largest ADC samples for the ADC104S021 are compared for diagnostic purposes. Similarly, each of the five smallest ADC samples for the ADS131A04 and the five smallest ADC samples for the ADC104S021 are also compared, as is described in Section 2.7.3.1.2.

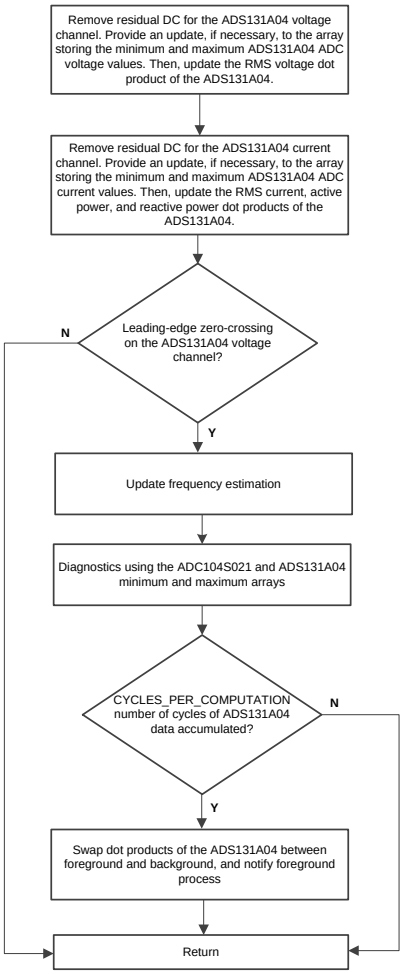


Figure 23. DS_processing Function

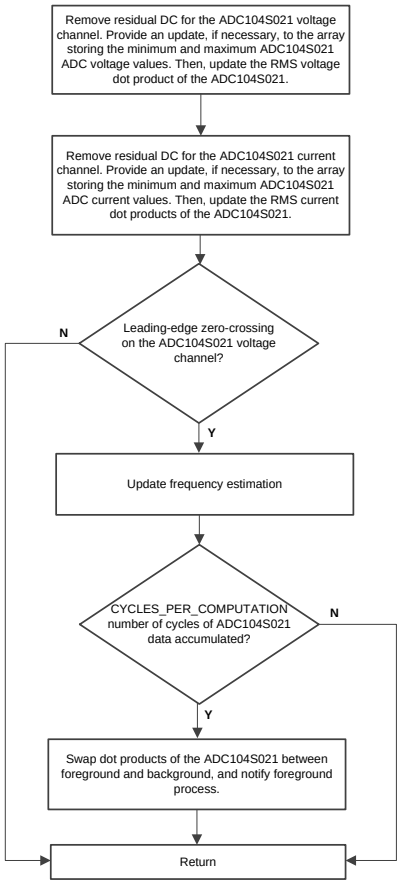


Figure 24. SAR_processing Function

Whenever there is a leading-edge zero-crossing (− to + voltage transition) on a voltage channel of an ADC, the corresponding frequency estimation of the ADC (in units of samples per cycle) is updated. Also, after data corresponding to the CYCLES_PER_COMPUTATION number of mains cycles has been accumulated for an ADC, the background process triggers the foreground function to calculate the metrology parameters for that ADC. For the ADS131A04, the calculated values include RMS voltage, RMS current, active power, reactive power, apparent power, and frequency. For the ADC104S021, the calculated values include RMS voltage, RMS current, and frequency.

In the software, there are two sets of dot products for each ADC (the ADS131A04 has two sets of dot products and the ADC104S021 has a separate two sets of dot products). At any given time, one set of dot products is used by the foreground for calculation and the other set is used as the working set by the background. After the background process has sufficient samples, it swaps the two dot products so that the foreground uses the newly acquired dot products that the background process just calculated, and the background process uses a new empty set to calculate the next set of dot products.

2.7.3.1.1 Voltage and Current Signals

The ADC samples are represented as signed integers and any stray DC or offset value on these converters are removed using a DC tracking filter. Separate DC estimates for all voltages and currents are obtained using the filter, voltage, and current samples, respectively. These estimates are then subtracted from each voltage and current sample. The resulting instantaneous voltage and current samples are used to generate the following intermediate dot product results:

- Accumulated squared values of ADS131A04 voltage and current samples, which are used for calculation of V_{RMS} and I_{RMS} of the ADS131A04, respectively
- Accumulated squared values of ADC104S021 voltage and current samples, which are used for calculation of V_{RMS} and I_{RMS} of the ADC104S021, respectively
- Accumulated ADS131A04 power samples to calculate active energy
- Accumulated ADS131A04 power samples using the ADS131A04 current samples and 90° phase-shifted ADS131A04 voltage samples to calculate reactive energies

These accumulated values are processed by the foreground process.

2.7.3.1.2 Diagnostics Using ADC104S021 and ADS131A04

Within each mains cycle, the five largest and smallest ADC samples are stored for both the ADS131A04 and ADC104S021 devices. This is represented in the software as eight different arrays:

- The ADS131A04 voltage minimum array
- The ADC104S021 voltage minimum array
- The ADS13A04 voltage maximum array
- The ADC104S021 voltage maximum array
- the ADS131A04 current minimum array
- The ADC104S021 current minimum array
- The ADS13A04 current maximum array
- The ADC104S021 current maximum array

When a new mains cycle is detected (specifically at the – to + zero crossing) on the ADS131A04 voltage channel the eight arrays are compared, where the following pairs of arrays are compared to each other:

- The voltage minimum array of the ADS131A04 and ADC104S021
- The voltage maximum array of the ADS131A04 and ADC104S021
- The current minimum array of the ADS131A04 and ADC104S021
- The current maximum array of the ADS131A04 and ADC104S021

In each of these array comparisons, each element of the corresponding array of the ADC104S021 is translated into high and low threshold values that can be directly compared to the corresponding element of the ADS131A04 array. As a result, during each mains cycle five sets of comparisons are done for each pair of arrays (element x of an ADC104S021 array is compared to element x of the corresponding ADS131A04 array).

For each array element comparison, a minimum and maximum threshold value is generated using the ADC104S021 array element, the THRESHOLD macro, and the SAR_OFFSET macro. These threshold values are then translated so that they can be directly compared to the ADS131A04 ADC value stored in the corresponding element of the ADS131A04 array. This translation ensures that the ADC sample comparisons done correspond to actually comparing the voltage and current readings of the ADS131A04 and ADC104S021 in real-world units.

If any of the five ADC samples in the ADS131A04 array are beyond the corresponding minimum and maximum thresholds that were calculated using the ADC104S021 samples, then a mismatch and its associated type is noted for this mains cycle. Four mismatch types based on the different arrays are compared:

- A voltage minimum mismatch
- A voltage maximum mismatch
- A current minimum mismatch
- A current maximum mismatch

The state of whether a mismatch has occurred for the voltage minimum, voltage maximum, current minimum, and current maximum is stored for each mains cycle. When the foreground process is called, the total number of cycle mismatches over the 5 (for 50 Hz) or 6 (for 60 Hz) cycle frames is summed for each type of mismatch (this means that the maximum value of the sum for a type of mismatch is either 5 or 6 because this value equals the number of cycles in the frame of data). This summed value is displayed as one digit in the mismatch diagnostic parameters that are sent out through the UART (for details, see Section 3.2.3.1).

2.7.3.1.3 Frequency Measurement and Cycle Tracking

A cycle-tracking counter and sample counter track the number of samples accumulated for an ADC. When approximately the CYCLES_PER_COMPUTATION number of mains cycles have been accumulated, the background process switches the foreground and background dot products and then notifies the foreground process to calculate the final values of metrology parameters for that frame of data.

For frequency measurements, a straight-line interpolation is used between the zero-crossing voltage samples. Figure 25 shows the samples near a zero cross and the process of linear interpolation.

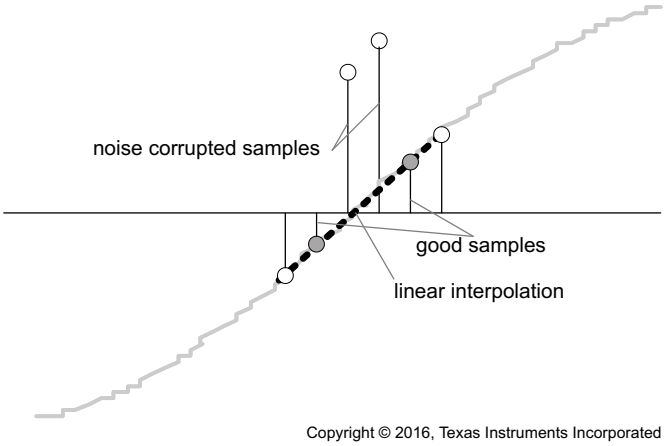


Figure 25. Frequency Measurement

Because noise spikes can also cause errors, the application uses a rate of change check to filter out the possible erroneous signals and ensure that the two points that are interpolated are from genuine zero crossing points. For example, with two negative samples, a noise spike can turn one of the samples positive, thereby making the negative and positive pair look as if there is a zero crossing. The resultant cycle-to-cycle timing goes through a weak low-pass filter to further smooth out cycle-to-cycle variations. This filtering results in a stable and accurate frequency measurement that is tolerant of noise.

2.7.3.2 Phase Compensation

To ensure accurate power measurements from the ADS131A04 samples, the relative phase-shift between voltage and current samples must be compensated. This phase-shift may be caused by the passive components of the voltage and current input circuit or even the current sensor used.

The implementation of the phase-shift compensation consists of an integer part and a fractional part. The integer part is realized by providing an N samples delay. The fractional part is realized by a 1-tap finite impulse response (FIR) filter that interpolates between two samples, similar to the FIR filter used for providing 90° shifted voltage samples for reactive energy measurements. In the software, a lookup table provides the filter coefficients that are used to create the fractional delays. The lookup table provides fractional phase shifts as small as $1/256^{th}$ of a sample. The 4000 sample rate at 50 Hz used in this application corresponds to a 0.0176° resolution, while the 5333.3 sample rate at 60 Hz corresponds to a 0.0158° resolution. In addition to the filter coefficients, the lookup table also has an associated gain variable for each set of filter coefficients. This gain variable is used to cancel the resulting gain from using a certain set of filter coefficients.

3 Getting Started Hardware and Firmware

3.1 Hardware

The following connections must be made for testing the AFE:

- DC power supply
- Interface to MSP432P401R for delta-sigma and SAR ADC
- Isolated voltage input
- Non-isolated voltage input
- Current input

Connectors have been provided to interface the input. Take care to use the proper connectors, as shown in Figure 26.

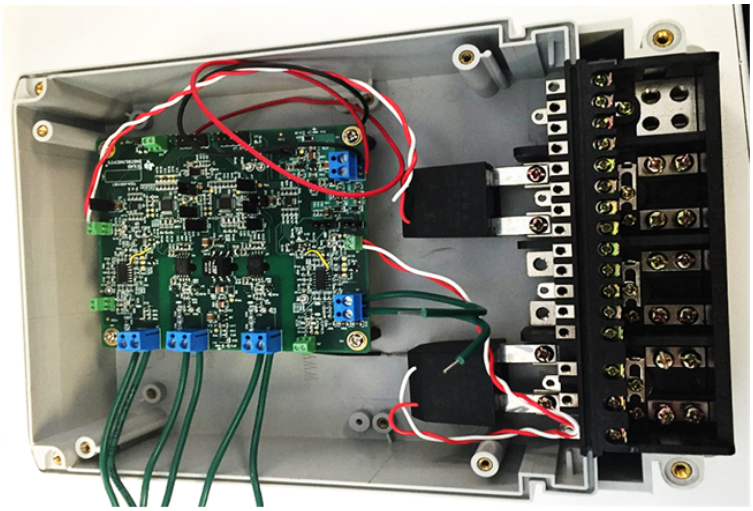


Figure 26. Data Acquisition AFE With External CTs

Figure 27 shows the interface between the ADS131A04 board and the MSP432 LaunchPad.

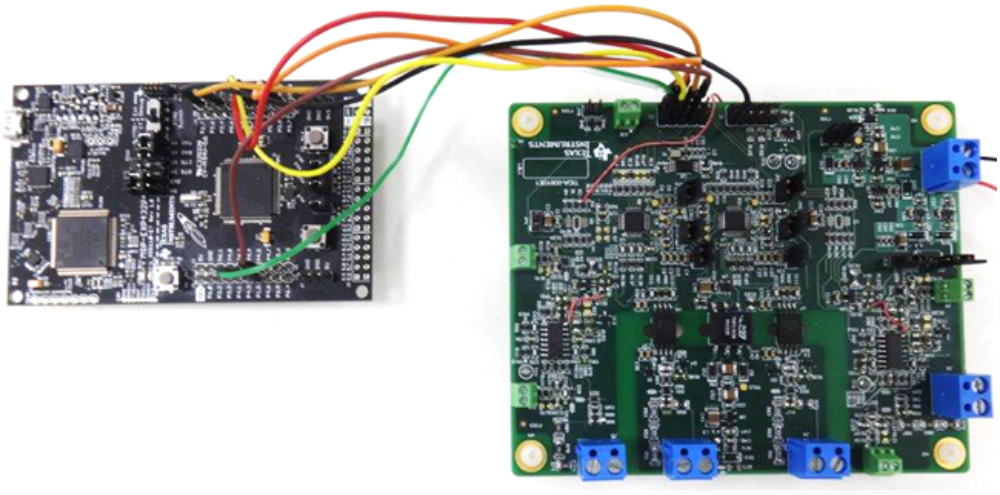


Figure 27. Data Acquisition AFE Interfaced to MCU

3.1.1 Power Supply Jumper

3.1.1.1 External DC Input

Table 18 describes the jumper that connects DC input of 5.5 V.

Table 18. External DC Input

JUMPER	PINS	DESCRIPTION
J13	1	DC_IN
	2	AGND

3.1.1.2 Jumpers for 0- to 5-V ADC Operation

Table 19 provides information on jumpers for 0- to 5-V delta-sigma ADC operation.

Table 19. Jumpers for Delta-Sigma ADC 0- to 5-V Operation

POWER	JUMPER	PINS	STATUS
AVDD	J11	1-2 (3.3)	N/A
		3-2 (2.5)	N/A
	J12	1-2 (3.3 / 2.5)	Open
		3-2 (+5 V)	Mounted
AVSS	J14	1-2 (–2.5)	Open
		3-2 (0 V)	Mounted

3.1.1.3 Jumpers for ±2.5-V Operation

Table 20 provides information on jumpers for ±2.5-V delta-sigma ADC operation.

Table 20. Jumpers for Delta-Sigma ADC ±2.5-V Operation

POWER	JUMPER	PINS	STATUS
AVDD	J11	1-2 (3.3)	N/A
		3-2 (2.5)	Mounted
	J12	1-2 (3.3 / 2.5)	Mounted
		3-2 (+5 V)	Open
AVSS	J14	1-2 (–2.5)	Mounted
		3-2 (0 V)	Open

3.1.2 TIDA-00810 AFE to MSP432P401R MCU Interface

3.1.2.1 ADS131A04 to MSP432P401R Interface

Table 21 provides information on jumpers for ±2.5-V delta-sigma ADC operation.

Table 21. MSP432P401R to Delta-Sigma ADC ADS131A04 Interface

SIGNAL	LAUNCHPAD PIN	TIDA-00810 INTERFACE
ADC_RESET	P4.5 (GPIO) Reset for ADS131A04	J2 – Pin 3
ADC_SPI_DRDY	Delta-sigma DRDY → P3.0 (interruptible GPIO pin)	J2 – Pin 5
ADC1_SPI_DONE	Done of device 1 → P5.1 (not used)	J2 – Pin 6
ADC_SPI_MISO	Delta-sigma data out → P1.7 (UCB0SOMI)	J2 – Pin 7
ADC_SPI_MOSI	Delta-sigma data in → P1.6 (UCB0SIMO)	J2 – Pin 8
ADC1_CS#	Delta-sigma chip select → P5.2 (GPIO pin)	J2 – Pin 9
ADC_SPI_SCLK	Delta-sigma SPI clock → P1.5 (UCBOCLK)	J2 – Pin 10
GND	J2 - GND	J1 – Pin 10
ADC1_Comp	P2.7 (GPIO)	J2 – Pin 2
ADC2_Comp	P2.6 (GPIO)	J2 – Pin 4

3.1.2.2 SAR ADC to MSP432P401R MCU Interface

Table 22 provides information on the interconnection between the SAR ADC board and MSP432 LaunchPad.

Table 22. MSP432P401R to SAR ADC—ADC104S021 Interface

SIGNAL	LAUNCHPAD PIN	TIDA-00810 INTERFACE
Chip select 1 for U1 device on the board	P5.0 (GPIO)	J1 – Pin 16
Chip select 2 for U3 device on the board	P5.1 (GPIO)	J1 – Pin 5
ADC104S021SPI clock	P3.5 (UCB2 SPI port)	J1 – Pin 1
ADC104S021SPI input (SIMO)	P3.6 (UCB2 SPI port)	J1 – Pin 3
ADC104S021SPI output (MISO)	P3.7 (UCB2 SPI port)	J1 – Pin 2
GND	J2 - GND	J1 – Pin 10

3.1.2.3 RS-232 Interface

Table 23 provides information on connecting the MSP432P401R LaunchPad to the PC through the RS-232.

Table 23. MSP432P401R LaunchPad Serial Interface

PORT PIN	FUNCTION
RS-232 GPIO configuration: P3.2 (UCA2 UART port) P3.3 (UCA2 UART port)	RS-232 GPIO configuration: UART receive for RS-232 communication UART transmit for sending metrology parameters using RS-232
J3 – Pin 22	Ground

3.1.3 AFE Interface

3.1.3.1 Current Inputs

3.1.3.1.1 CT Input

Table 24 provides information on the connector, which connects the current inputs to the ADCs.

Table 24. CT_Rogowski Input to Delta-Sigma ADC Configuration

ADC	CONNECTOR	ADC CHANNEL
U2	J7	CT_1_Out
	J10	ROGO_1_Out
U4	J8	CT_2_Out
	J9	ROGO_2_Out

NOTE: External current inputs are applied across the previous jumpers. To configure the previous inputs to measure Rogowski input from an external active integrator board, the following changes must be made.

3.1.3.1.2 Rogowski Coil Integrator Output

Table 25 provides information on the connector which connects the TIDA-00777 integrator output to the ADCs.

Table 25. Rogowski Coil Integrator Output Connection

ADC	CONNECTOR	ADC CHANNEL	CONFIGURATION
U2	J10	ROGO_1_Out	Depopulate R111 and C74
			Connector integrator output to TP4
U4	J9	ROGO_2_Out	Depopulate R113 and C75
			Connector integrator output to TP6

3.1.3.2 Non-Isolated Voltage Input

Table 26 lists the connectors used to connect the non-isolated AV voltage input for measurement.

Table 26. Non-Isolated Voltage Input to Potential Divider

ADC	CONNECTOR	ADC CHANNEL
U2	J5	PD_Out1
U4	J6	PD_Out2

3.1.3.3 Isolated Voltage Input

Table 27 lists the connectors used to connect the isolated AV voltage input for measurement.

Table 27. Isolated Voltage Input to Potential Divider

ADC	CONNECTOR	ADC CHANNEL
U2	J3	VOUT1_P
		VOUT1_N
U4	J4	VOUT2_P
		VOUT2_N

3.1.4 ADC Jumpers

3.1.4.1 Delta-Sigma

Table 28 provides jumper information for power supply configuration to delta-sigma ADCs.

Table 28. Delta-Sigma ADC Jumper Configuration

ADC	JUMPER	ENABLE	DISABLE
U2	Charge pump	Depopulate JP4	Populate JP4
	AVCC_3.3	Populate JP3	Depopulate JP3
	AVDD	Populate JP2	Depopulate JP2
U4	Charge pump	Depopulate JP8	Populate JP8
	AVCC_3.3	Populate JP7	Depopulate JP7
	AVDD	Populate JP6	Depopulate JP6

3.1.4.2 SAR

Table 29 provides jumper information for power supply configuration to SAR ADCs.

Table 29. SAR ADC Power Supply

ADC	JUMPER	ENABLE	DISABLE
U1	+5 V	Populate JP1	Depopulate JP1
U3	+5 V	Populate JP5	Depopulate JP5

3.1.5 Reference

3.1.5.1 External or Internal

3.1.5.1.1 AFE Signal Conditioning

Table 30 provides jumper information for configuring the AFE reference.

Table 30. AFE Reference Configuration

ADC	INTERNAL	EXTERNAL
U2	Populate R151	Populate R153
	Depopulate R153	Depopulate R151
U4	Populate R154	Populate R156
	Depopulate R156	Depopulate R154

3.1.5.1.2 Delta-Sigma ADC

Table 31 describes the configuration of reference to the delta-sigma ADC.

Table 31. Delta-Sigma Reference Configuration

ADC	INTERNAL	EXTERNAL
U2	Depopulate R157	Populate R157
U4	Depopulate R161	Populate R161

3.1.5.2 Analog Input Range

Table 32 provides jumper information for configuring the delta-sigma reference.

Table 32. Delta-Sigma Analog Input Configuration

ADC	0 to 5 V	±2.5 V
U2	Populate 126	Populate 118
	Depopulate 118	Depopulate 126
U4	Populate 129	Populate 121
	Depopulate 121	Depopulate 129

3.2 Firmware

3.2.1 Loading Code to MSP432P401R

This firmware was developed with Code Composer Studio™ (CCS) Version: 6.1.1.00022. To load this firmware onto the MCU, follow theses instructions:

1. From the downloaded software .zip file, run the *TIDA00810lib-1.0-windows-installer.exe* file to download and extract the firmware of the design. This download produces the TIDA-00810 lib folder, which contains the CCS project and software of the software.
2. Open CCS. From the *Workspace Launcher* window that appears after starting CCS (shown in Figure 28), select the desired workspace path and click *OK*. The *CCS Edit* window appears, as shown in Figure 29.

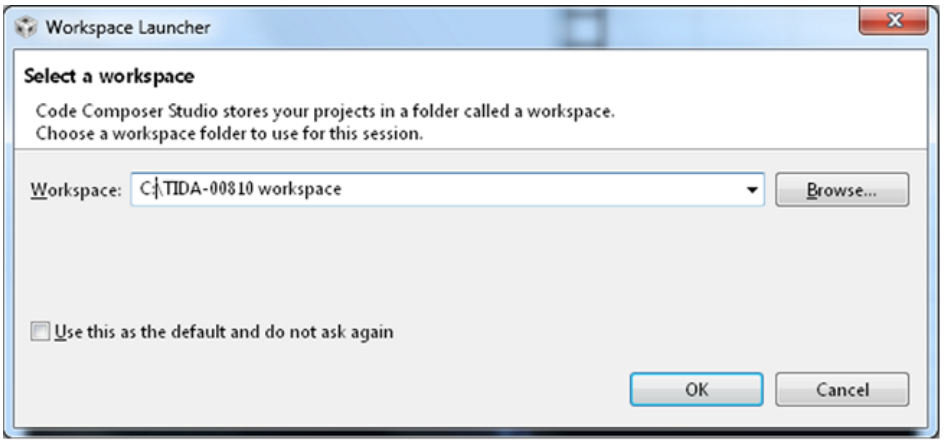


Figure 28. Workspace Launcher Window

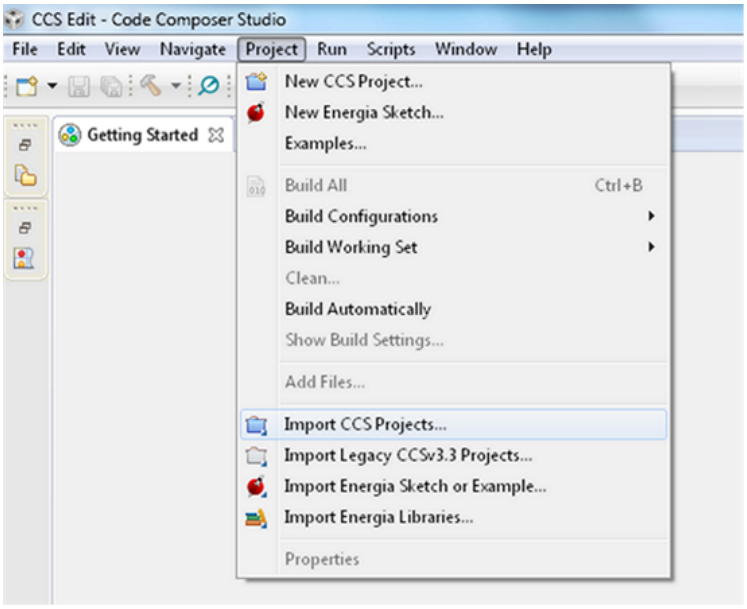


Figure 29. CCS Edit Window

3. From the *CCS Edit* window, click the *Project* button and select *Import CCS Projects...* as shown in Figure 29. The *Import CCS Eclipse Projects* window appears, as shown in Figure 30.

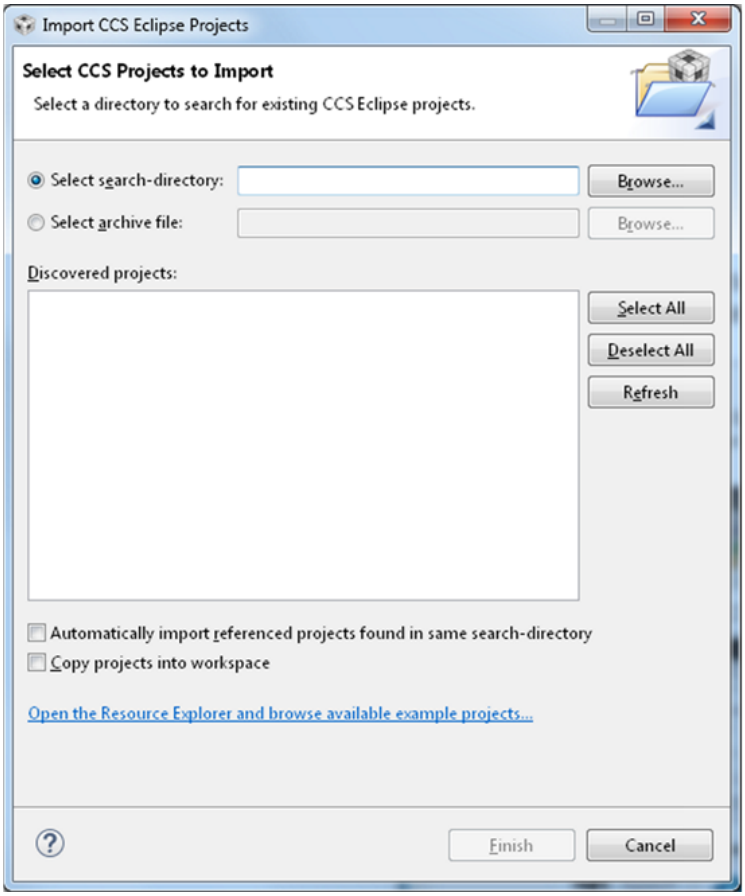


Figure 30. Import CCS Eclipse Projects Window

4. From the *Import CCS Eclipse Projects* window that appears, select the *Select search-directory* button and click the *Browse* button, then select the TIDA-00810 lib folder where the design software is located. After selecting the proper directory, the CCS project of the design must be discovered, as shown in Figure 31. Once this project has been discovered, click the *Finish* button.

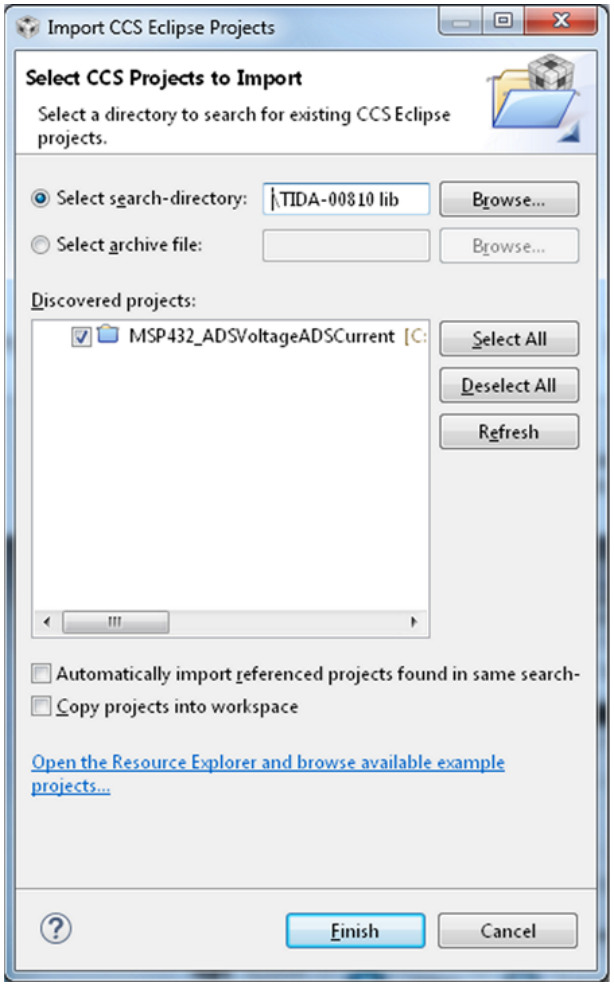


Figure 31. Import CCS Eclipse Projects Window With TIDA-00810 Software Discovered

5. In the *Project Explorer*, right-click the project name and select *Clean Project*, as shown in Figure 32.

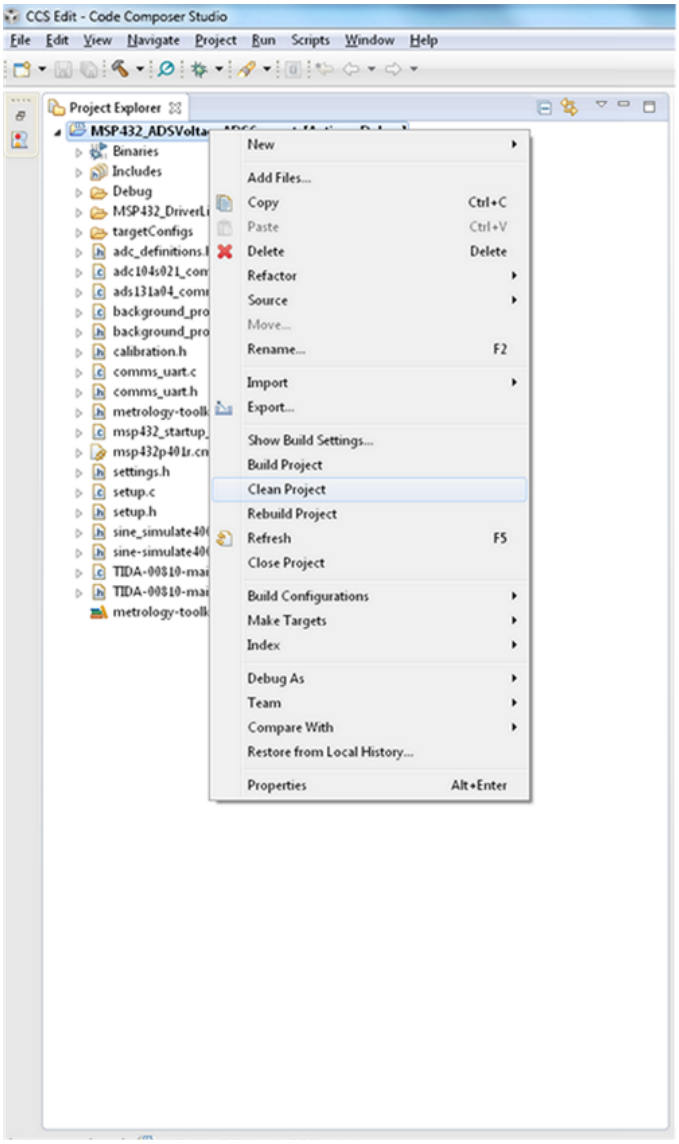


Figure 32. Steps for Cleaning a Project

6. After the project has been cleaned, load the code onto the MCU by clicking on the *Run* menu and selecting *Debug*, as shown in Figure 33.

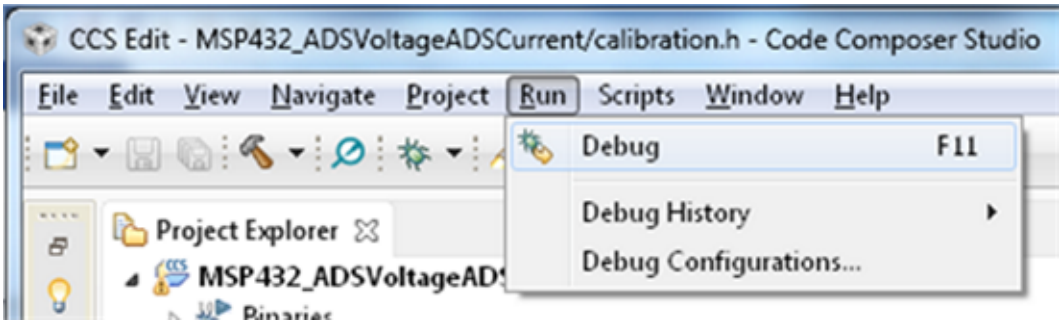


Figure 33. Loading Code on MSP432P401R

3.2.2 Configuration Options

In the firmware package, the settings.h file contains macros that can be adjusted to configure the system as necessary. In this file, the following macros are available:

- VOLTAGE_CHANNEL_NUMBER: The value of this macro defines which ADS131A04 channel corresponds to the voltage channel so that the voltage samples used for ADS131A04-based metrology calculations are taken from this ADS131A04 channel. To select a particular ADS131A04 channel for the voltage channel of the ADS131A04, define this macro to be equal to the corresponding software channel number mentioned in Table 16.
- CURRENT_CHANNEL_NUMBER: The value of this macro defines which ADS131A04 channel corresponds to the current channel so that the current samples used for ADS131A04-based metrology calculations are taken from this ADS131A04 channel. To select a particular ADS131A04 channel for the current channel of the ADS131A04, define this macro to be equal to the corresponding software channel number mentioned in Table 16.
- SAR_VOLTAGE_CHANNEL_NUMBER: The value of this macro defines which ADC104S021 channel corresponds to the voltage channel so that the voltage samples used for ADC104S021-based metrology calculations are taken from this ADC104S021 channel. To select a particular ADC104S021 channel for the voltage channel of the ADC104S021, define this macro to be equal to the corresponding software channel number mentioned in Table 17.
- SAR_CURRENT_CHANNEL_NUMBER: The value of this macro defines which ADC104S021 channel corresponds to the current channel so that the current samples used for metrology calculations are taken from this ADC104S021 channel. To select a particular ADC104S021 channel for the current channel of the ADC104S021, define this macro to be equal to the corresponding software channel number mentioned in Table 17.
- COMPUTATIONS_AGGREGATED: This value defines how many 100-ms frames of data must be averaged together for the metrology parameters that are actually sent through the UART. By default, this value is set to 10, which leads to the metrology parameters sent out through the UART being averaged over an approximately 1 second time interval.
- MAINS_NOMINAL_FREQUENCY: This macro defines the nominal mains frequency and can only take the values of 50 or 60. When this macro is configured for 50, the sample rate of the ADS131A04 is set to 4000 samples per second with metrology parameters calculated once every five mains cycles (approximately 100 ms). If this macro is configured for 60, the sample rate is set to 5333.3 samples per second with metrology parameters calculated once every six mains cycles (approximately 100 ms).
- SAR_OFFSET: When performing comparisons of the 24-bit ADS131A04 ADC results and the translated 16-bit ADC104S021 ADC results, this provides an acceptable offset threshold (in ADC units) so that the diagnostic logic does not indicate a possible mismatch in the minimum or maximum for low voltages or low currents. This macro is defined in terms of the 16-bit translated value of the ADC104S021. As a result, a value of 64 corresponds to 1 LSB of the ADC104S021.

- THRESHOLD: Along with the SAR_OFFSET macro, this macro defines what error percentage the software indicates the occurrence of a mismatch between the minimum and maximum values of the two ADCs, the ADS131A04 ADC values, and the translated, corresponding ADC104S021 ADC values. If the SAR_OFFSET is set to 0, the corresponding error threshold for determining a mismatch is found by using Equation 10.

$$\pm 100\% / 2^{THRESHOLD} \quad (10)$$

For example, a value of 2 for this threshold corresponds to an error threshold of ±25%, which means that an error is be triggered whenever the ADS131A04 value is either less than 75% of the translated ADC104S021 value or greater than 125% of the translated ADC104S021 value.

3.2.3 Viewing Metrology and ADC Sample Results

3.2.3.1 Viewing Metrology Results Using RS-232

By following the RS-232 and UART settings mentioned in Section 2.7.1.1.1, the metrology parameters can be viewed from a terminal program, as shown in Figure 34.

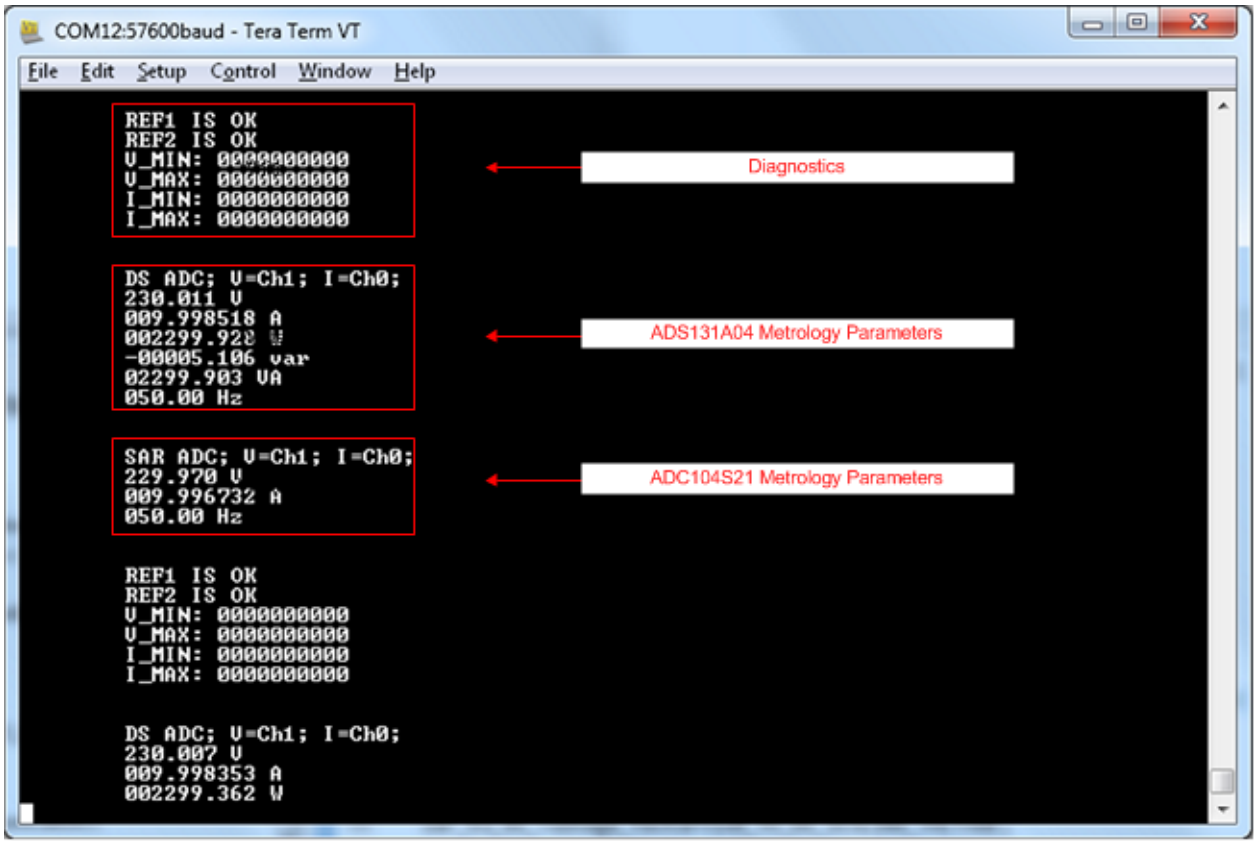


Figure 34. Viewing Metrology Results Using Terminal Program

By default, a new metrology parameter is sent from the UART of the MCU at a rate of approximately once per second. Three sets of parameters are sent out the UART of the MCU. The first item that is sent is the diagnostics information. Table 33 lists the different parameters that are sent in this set, the relative order these parameters are sent out through the UART, and a description of these parameters. The second set of parameters sent are the metrology parameters, which are calculated using the ADS131A04 ADC. Table 34 provides a description of these ADS131A04-based parameters. The final set of parameters sent are the metrology parameters, which are calculated using the ADC104S021. Similarly, Table 35 provides a description of these ADC104S021-based parameters.

Table 33. Diagnostic Parameters Sent Out UART

SENDING ORDER	PARAMETER	DESCRIPTION
Sent first	Reference voltage 1 status: start of diagnostic parameters	This parameter reflects the state of the comparator used to determine the health of reference voltage 1 (for the ADS131A04 U2 device). If the comparator indicates that the sensed reference is below the set threshold, this parameter is displayed as CHECK REF1. Otherwise, this parameter is displayed as REF1 IS OK.
Sent second	Reference voltage 2 status	This parameter reflects the state of the comparator used to determine the health of reference voltage 2 (for the ADS131A04 U4 device). If the comparator indicates that the sensed reference is below the set threshold, this parameter is displayed as CHECK REF2. Otherwise, this parameter is displayed as REF2 IS OK.
Sent third	Mismatches between ADS131A04 and ADC104S021 voltage minimum ADC values (V_MIN)	The value of this parameter contains 10 digits where each digit represents a different 5 cycle (for 50-Hz nominal frequency) or 6 cycle (for 60 Hz nominal frequency) frame of data. Within each mains cycle, five of the most minimum voltages are logged for both the ADS131A04 and the ADC104S021. If any of the logged minimum voltages for the ADS131A04 are beyond the corresponding minimum voltages logged by the ADC104S021 by a certain threshold, this cycle is noted as having a mismatch between the minimum voltages registered by the two ADCs. Each digit of the V_MIN parameter represents the number of cycles that have a voltage minimum mismatch out of the 5 or 6 cycle frame of data.
Sent fourth	Mismatches between ADS131A04 and ADC104S021 voltage maximum ADC values (V_MAX)	The value of this parameter contains 10 digits where each digit represents a different 5 cycle (for 50-Hz nominal frequency) or 6 cycle (for 60 Hz nominal frequency) frame of data. Within each mains cycle, five of the most maximum voltages are logged for both the ADS131A04 and the ADC104S021. If any of the logged maximum voltages for the ADS131A04 are beyond the corresponding maximum voltages logged by the ADC104S021 by a certain threshold, this cycle is noted as having a mismatch between the maximum voltages registered by the two ADCs. Each digit of the V_MAX parameter represents the number of cycles that have a voltage maximum mismatch out of the 5 or 6 cycle frame of data.
Sent fifth	Mismatches between ADS131A04 and ADC104S021 current minimum ADC values (I_MIN)	The value of this parameter contains 10 digits where each digit represents a different 5 cycle (for 50-Hz nominal frequency) or 6 cycle (for 60 Hz nominal frequency) frame of data. Within each mains cycle, five of the most minimum current are logged for both the ADS131A04 and the ADC104S021. If any of the logged minimum current for the ADS131A04 are beyond the corresponding minimum current logged by the ADC104S021 by a certain threshold, this cycle is noted as having a mismatch between the minimum current registered by the two ADCs. Each digit of the I_MIN parameter represents the number of cycles that have a current minimum mismatch out of the 5 or 6 cycle frame of data.
Sent sixth	Mismatches between ADS131A04 and ADC104S021 voltage maximum ADC values (I_MAX)	The value of this parameter contains 10 digits where each digit represents a different 5 cycle (for 50-Hz nominal frequency) or 6 cycle (for 60 Hz nominal frequency) frame of data. Within each mains cycle, five of the most maximum current are logged for both the ADS131A04 and the ADC104S021. If any of the logged maximum current for the ADS131A04 are beyond the corresponding maximum current logged by the ADC104S021 by a certain threshold, this cycle is noted as having a mismatch between the maximum current registered by the two ADCs. Each digit of the I_MAX parameter represents the number of cycles that have a current maximum mismatch out of the 5 or 6 cycle frame of data.

Table 34. ADS131A04-Based Metrology Parameters Sent Out Through UART

SENDING ORDER	PARAMETER	DESCRIPTION
Sent first	ADS131A04 metrology parameter designator	This parameter is used to denote the start of the ADS131A04-based metrology parameters and also provides information on which the ADS131A04 channels are used for the voltage and current samples. The value of this parameter is equal to DS ADC; V=Chx; I=Chy; where x is set to the VOLTAGE_CHANNEL_NUMBER macro and y is set to the CURRENT_CHANNEL_NUMBER.
Sent second	Voltage (V)	The ADS131A04-based metrology calculation of the RMS voltage.
Sent third	Current (A)	The ADS131A04-based metrology calculation of the RMS current.
Sent fourth	Active power (W)	The ADS131A04-based metrology calculation of the active power.
Sent fifth	Reactive power (var)	The ADS131A04-based metrology calculation of the reactive power.
Sent sixth	Apparent power (VA)	The ADS131A04-based metrology calculation of the apparent power.
Sent seventh	Frequency (Hz)	The ADS131A04-based metrology calculation of voltage frequency.

Table 35. AD04S021-Based Metrology Parameters Sent Out Through UART

SENDING ORDER	PARAMETER	DESCRIPTION
Sent first	ADC104S021 metrology parameter designator	This parameter is used to denote the start of the ADC104S021-based metrology parameters and also provides information on which ADC104S021 channels are used for the voltage and current samples. The value of this parameter is equal to SAR ADC; V=Chx; I=Chy; where x is set to the SAR_VOLTAGE_CHANNEL_NUMBER macro and y is set to the SAR_CURRENT_CHANNEL_NUMBER.
Sent second	Voltage (V)	The ADC104S021-based metrology calculation of the RMS voltage.
Sent third	Current (A)	The ADC104S021-based metrology calculation of the RMS current.
Sent fourth	Frequency (Hz)	The ADC104S021-based metrology calculation of voltage frequency.

3.2.3.2 Viewing Metrology Results and ADC Values Using Software Variables

In addition to viewing the metrology values using RS-232, the values of the metrology values as well as the ADC values can be obtained directly from the proper variables in the code. Specifically, there are four sets of variables of interest:

- Metrology parameters (parameters calculated every five or six cycles)
- Aggregated metrology parameters (parameters calculated once per second that are sent out through the UART)
- Sample data for all ADC channels (one sample per channel)
- Sample data for the voltage and current channels (4000 samples for both the voltage and current channels of each ADC)

Table 36, Table 37, Table 38, and Table 39 provide information on the specific variables to probe in the software for information on the values of the metrology parameters or the ADC results.

Table 36. Variable Names for 5- and 6-Cycle Metrology Parameters

VARIABLE NAME	VARIABLE TYPE	VARIABLE DESCRIPTION
active_power	int32_t [COMPUTATIONS_AGGREGATED]	The ADS131A04-based calculation of active power for a 5-cycle (50 Hz) or 6-cycle (60 Hz) frame of data. This array stores the last COMPUTATIONS_AGGREGATED number of these frames.
reactive_power	int32_t [COMPUTATIONS_AGGREGATED]	The ADS131A04-based calculation of reactive power for a 5-cycle (50 Hz) or 6-cycle (60 Hz) frame of data. This array stores the last COMPUTATIONS_AGGREGATED number of these frames.
apparent_power	int32_t [COMPUTATIONS_AGGREGATED]	The ADS131A04-based calculation of apparent power for a 5-cycle (50 Hz) or 6-cycle (60 Hz) frame of data. This array stores the last COMPUTATIONS_AGGREGATED number of these frames.
rms_voltage	int32_t [COMPUTATIONS_AGGREGATED]	The ADS131A04-based calculation of RMS voltage for a 5-cycle (50 Hz) or 6-cycle (60 Hz) frame of data. This array stores the last COMPUTATIONS_AGGREGATED number of these frames.
rms_current	int32_t [COMPUTATIONS_AGGREGATED]	The ADS131A04-based calculation of RMS current for a 5-cycle (50 Hz) or 6-cycle (60 Hz) frame of data. This array stores the last COMPUTATIONS_AGGREGATED number of these frames.
sar_rms_voltage	int32_t [COMPUTATIONS_AGGREGATED]	The ADC104S021-based calculation of RMS voltage for a 5-cycle (50 Hz) or 6-cycle (60 Hz) frame of data. This array stores the last COMPUTATIONS_AGGREGATED number of these frames.
sar_rms_current	int32_t [COMPUTATIONS_AGGREGATED]	The ADC104S021-based calculation of RMS current for a 5-cycle (50 Hz) or 6-cycle (60 Hz) frame of data. This array stores the last COMPUTATIONS_AGGREGATED number of these frames.
V_min_out_of_range	Int16_t [COMPUTATIONS_AGGREGATED]	This variable stores the number of V_min mismatches. Each element stores the number of V_min mismatches for one 5-cycle (50 Hz) or 6-cycle (60 Hz) frame of data.
V_max_out_of_range	Int16_t [COMPUTATIONS_AGGREGATED]	This variable stores the number of V_max mismatches. Each element stores the number of V_max mismatches for one 5-cycle (50 Hz) or 6-cycle (60 Hz) frame of data.
I_min_out_of_range	Int16_t [COMPUTATIONS_AGGREGATED]	This variable stores the number of I_min mismatches. Each element stores the number of I_min mismatches for one 5-cycle (50 Hz) or 6-cycle (60 Hz) frame of data.
I_max_out_of_range	Int16_t [COMPUTATIONS_AGGREGATED]	This variable stores the number of I_max mismatches. Each element stores the number of I_max mismatches for one 5-cycle (50 Hz) or 6-cycle (60 Hz) frame of data.
frequency	int16_t	The mains voltage frequency calculated from the ADS131A04 voltage channel
sar_frequency	int16_t	The mains voltage frequency calculated from the ADC104S021 voltage channel

Table 37. Variable Names for Aggregated Metrology Parameters

VARIABLE NAME	VARIABLE TYPE	VARIABLE DESCRIPTION
active_power_aggregated	int32_t	The aggregated active power calculation taken by averaging a COMPUTATIONS_AGGREGATED number of frames of the 5-cycle and 6-cycle active power readings calculated from the ADS131A04 ADC channels.
reactive_power_aggregated	int32_t	The aggregated reactive power calculation taken by averaging a COMPUTATIONS_AGGREGATED number of frames of the 5-cycle and 6-cycle reactive power readings calculated from the ADS131A04 ADC channels.
apparent_power_aggregated	int32_t	The apparent active power calculation taken by averaging a COMPUTATIONS_AGGREGATED number of frames of the 5-cycle and 6-cycle apparent power readings calculated from the ADS131A04 ADC channels.
rms_voltage_aggregated	int32_t	The aggregated rms voltage calculation taken by averaging a COMPUTATIONS_AGGREGATED number of frames of the 5-cycle and 6-cycle rms voltage readings calculated from the ADS131A04 ADC channels.
rms_current_aggregated	int32_t	The aggregated rms current calculation taken by averaging a COMPUTATIONS_AGGREGATED number of frames of the 5-cycle and 6-cycle rms current readings calculated from the ADS131A04 ADC channels.
sar_rms_voltage_aggregated	int32_t	The aggregated rms voltage calculation taken by averaging a COMPUTATIONS_AGGREGATED number of frames of the 5-cycle and 6-cycle rms voltage readings calculated from the ADC104S021 ADC channels.
sar_rms_current_aggregated	int32_t	The aggregated rms current calculation taken by averaging a COMPUTATIONS_AGGREGATED number of frames of the 5-cycle and 6-cycle rms current readings calculated from the ADC104S021 ADC channels.

Table 38. Variable Names of Arrays Used to Store all ADC Samples

VARIABLE NAME	VARIABLE TYPE	VARIABLE DESCRIPTION
channel_data	int32_t[8]	This array stores the raw ADC samples of the two ADS131A04 devices. The mapping of each element of the array is according to Table 16.
sar_channel_data	int16_t[8]	This array stores the raw ADC samples of the two ADC104S021 devices. The mapping of each element of the array is according to Table 17. This array is updated at half the rate of the channel_data array.

Table 39. Variable Names of Voltage and Current Samples of ADC104S021 and ADS131A04

VARIABLE NAME	VARIABLE TYPE	VARIABLE DESCRIPTION
results_current	int32_t[4000]	This array contains the last 4000 DC-filtered ADC samples of the current channel of the ADS131A04.
results_voltage	int32_t[4000]	This array contains the last 4000 DC-filtered ADC samples of the voltage channel of the ADS131A04.
sar_results_current	int16_t[4000]	This array contains the last 4000 DC-filtered ADC samples of the current channel of the ADC104S021.
sar_results_voltage	int16_t[4000]	This array contains the last 4000 DC-filtered ADC samples of the voltage channel of the ADC104S021.

3.2.4 Calibration

Calibration is critical to system performance. Different boards of this TI Design (and even different channels within the same board) exhibit different accuracies due to silicon-to-silicon differences, sensor accuracies, and other passive tolerances. To nullify these effects, the system must be calibrated. To perform calibration correctly an accurate AC test source and a reference meter must be available. The source must be able to generate any desired voltage, current, and phase-shifts (between V and I). To calculate errors in measurement, the reference meter acts as an interface between the source and the meter being calibrated. This section describes a simple and effective method of calibrating this design.

The received metrology values on the serial terminal can be used to calculate new calibration factors from the old calibration factors to give the least error in measurement. In this design, the six main calibration factors for the ADS131A04 are:

- VOLTAGE_CALIBRATION_DS (voltage scaling factor)
- VOLTAGE_AC_OFFSET_DS (voltage AC offset factor)
- CURRENT_CALIBRATION_DS (current scaling factor)
- CURRENT_AC_OFFSET_DS (current AC offset factor)
- ACTIVE_POWER_CALIBRATION (active power scaling factor)
- PHASE_SHIFT_CALIBRATION (phase shift compensation factor)

For the ADC104S021, the four main calibration factors are:

- VOLTAGE_CALIBRATION_SAR (voltage scaling factor)
- VOLTAGE_AC_OFFSET_SAR (voltage AC offset factor)
- CURRENT_CALIBRATION_SAR (current scaling factor)
- CURRENT_AC_OFFSET_SAR (current AC offset factor)

The voltage, current, and power scaling factors translate measured quantities in metrology software to real-world values represented in volts, amps, and watts, respectively. The voltage AC offset and current AC offset are used to eliminate the effect of additive white Gaussian noise (AWGN) associated with each channel. This noise is orthogonal to everything except itself; as a result this noise is present only when calculating RMS voltages and currents. The last calibration factor is the phase compensation factor, which is used to compensate any phase-shifts introduced by the current sensors and other passives. The voltage, current, and power calibration factors are independent of each other. Therefore, calibrating voltage does not affect the readings for RMS current or power.

When the firmware is first loaded onto the MCU, the default calibration factors are used. These default calibration values must be modified in the source code during calibration. After modifying these calibration factors, the code must be recompiled and reloaded onto the MCU to use the new calibration factors.

3.2.4.1 Gain Calibration

To calibrate the voltage and current readings, follow these steps:

1. Connect an isolated UART-to-RS-232 board to the UART port that is used to send metrology parameters and the RS-232 port of a computer. An example of a UART-to-RS-232 board is the TIDA-00163.
2. Open a terminal program to view the readings for voltage, current, and active power.
3. Configure the test source to supply desired voltage and current. Ensure that these are the voltage and current calibration points with a 0° phase-shift between the voltage and current. For example: 230 V, 10 A, 0º (PF = 1).
4. Based on the RMS voltage reading from the ADS131A04 devices, the actual RMS voltage supplied to the system, and the VOLTAGE_CALIBRATION_DS macro (from calibration.h), calculate a new value of the VOLTAGE_CALIBRATION_DS macro by using the following formula:

$$\left(\text{VOLTAGE\_CALIBRATION\_DS}_{\text{new}} \right) = \left(\text{VOLTAGE\_CALIBRATION\_DS}_{\text{old}} \right) \left(\frac{V_{\text{RMS, Supplied}}}{V_{\text{RMS, ADS131A04\_Reading}}} \right) \quad (11)$$

5. Replace the old value of VOLTAGE_CALIBRATION_DS in calibration.h with the $VOLTAGE\_CALIBRATION\_DS_{NEW}$ value calculated. For this macro, be sure to round to the nearest whole number.
6. Based on the RMS voltage reading from the ADC104S021 devices, the actual RMS voltage supplied to the system, and the VOLTAGE_CALIBRATION_SAR macro (from calibration.h), calculate a new value of the VOLTAGE_CALIBRATION_SAR macro by using the following formula:

$$\left(VOLTAGE\_CALIBRATION\_SAR_{new} \right) = \left(VOLTAGE\_CALIBRATION\_SAR_{old} \right) \left(\frac{V_{RMS,Supplied}}{V_{RMS,ADC104S021\_Reading}} \right) \quad (12)$$

7. Replace the old value of VOLTAGE_CALIBRATION_SAR in calibration.h with the $VOLTAGE\_CALIBRATION\_SAR_{NEW}$ value calculated. For this macro, be sure to round to the nearest whole number.
8. Based on the RMS current reading from the ADS131A04 devices, the actual RMS current supplied to the system, and the CURRENT_CALIBRATION_DS macro (from calibration.h), calculate a new value of the CURRENT_CALIBRATION_DS macro by using the following formula:

$$\left(CURRENT\_CALIBRATION\_DS_{new} \right) = \left(CURRENT\_CALIBRATION\_DS_{old} \right) \left(\frac{I_{RMS,Supplied}}{I_{RMS,ADS131A04\_Reading}} \right) \quad (13)$$

9. Replace the old value of CURRENT_CALIBRATION_DS in calibration.h with the $CURRENT\_CALIBRATION\_DS_{NEW}$ value calculated. For this macro, be sure to round to the nearest whole number.
10. Based on the RMS current reading from the ADC104S021 devices, the actual RMS current supplied to the system, and the CURRENT_CALIBRATION_SAR macro (from calibration.h), calculate a new value of the CURRENT_CALIBRATION_SAR macro by using the following formula:

$$\left(CURRENT\_CALIBRATION\_SAR_{new} \right) = \left(CURRENT\_CALIBRATION\_SAR_{old} \right) \left(\frac{I_{RMS,Supplied}}{I_{RMS,ADC104S021\_Reading}} \right) \quad (14)$$

11. Replace the old value of CURRENT_CALIBRATION_SAR in calibration.h with the $CURRENT\_CALIBRATION\_SAR_{NEW}$ value calculated. For this macro, be sure to round to the nearest whole number.
12. Based on the active power readings from the ADS131A04 devices, the actual active power readings, and the ACTIVE_POWER_CALIBRATION macro (from calibration.h), calculate a new value of the ACTIVE_POWER_CALIBRATION macro by using the following formula:

$$\left(ACTIVE\_POWER\_CALIBRATION_{new} \right) = \left(ACTIVE\_POWER\_CALIBRATION_{old} \right) \left(\frac{P_{ACT,actual}}{P_{ACT,ADS131A04\_Reading}} \right) \quad (15)$$

13. Replace the old value of ACTIVE_POWER_CALIBRATION in calibration.h with the $ACTIVE\_POWER\_CALIBRATION_{NEW}$ value calculated. For this macro, be sure to round to the nearest whole number.
14. Save calibration.h and load the code onto the MCU by clicking on the *Run* menu and selecting *Debug*, as shown in Figure 35.

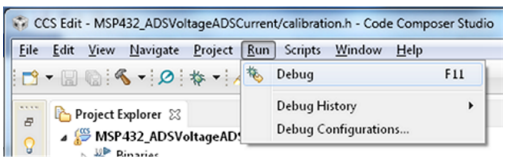


Figure 35. Loading Code on MSP432P401R

3.2.4.2 Phase Correction

After performing power gain calibration, phase calibration must be performed. To perform phase correction calibration, perform the following steps:

1. If the AC test source has been turned OFF or reconfigured, perform Steps 1 to 3 from the gain calibration section using the identical voltage and current used in that section.
2. Modify only the phase-shift to a nonzero value; typically, 60º is chosen.
3. Observe the active power readings and compare it to the actual active power value. Use these values to calculate the % error by the following formula:

$$\%_{error} = \left(\frac{P_{ACT,ADS131A04\_Reading}}{P_{ACT,actual}} - 1 \right) \times 100 \quad (16)$$

4. If the active power % error is not close to zero, or is unacceptable, perform phase correction by following these steps:
   (a) Modify the PHASE_SHIFT_CALIBRATION macro to minimize the active power % error. Usually, a small ± integer must be entered to bring the error closer to zero. If increasing the PHASE_SHIFT_CALIBRATION scaling factor causes the absolute value of the active percent error to increase then calibration must be performed by reducing the value of the PHASE_SHIFT_CALIBRATION scaling factor until the absolute value of active power % error is minimized. Alternatively, if increasing the PHASE_SHIFT_CALIBRATION scaling factor causes the absolute value of the active power percent error to decrease, then the PHASE_SHIFT_CALIBRATION scaling factor must be increased until the absolute value of the active power % error is minimized.
   (b) Save calibration.h and load the code onto the MSP432P401R by clicking on the *Run* menu and selecting *Debug*, as shown in Figure 33.
   (c) If this measurement error (%) is not accurate enough, fine-tune it by incrementing or decrementing by a value of 1, based on Steps 4a and 4b.

   NOTE: After a point, the fine-tuning only results in the error oscillating on either side of zero. The value that has the smallest absolute error must be selected.

   (d) Change the phase now to –60° and check if this error is still acceptable. Ideally, errors are symmetric for same phase-shift on lag and lead conditions.

After performing phase correction, calibration is complete.

4 Testing and Results

4.1 Test Setup

Figure 36 shows the setup for performance testing of the ADS131A04 based AFE.

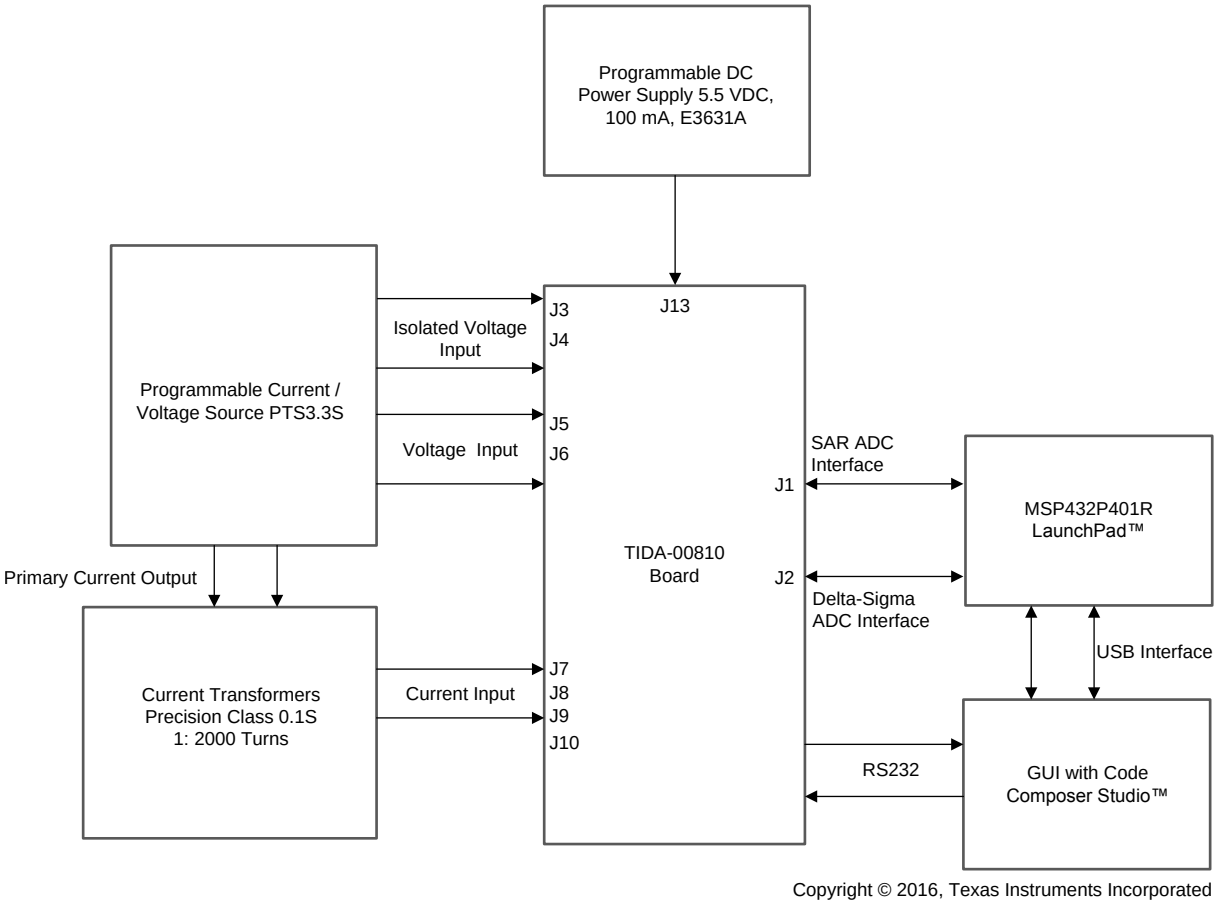


Figure 36. Test Setup for Testing AFE

The setup for testing the data acquisition AFE consists of:

- Current controlled DC power supply
- Accurate programmable voltage and current source with power factor
- External current transformer
- Voltage input from the AC source
- MSP432P401R LaunchPad interfaced to the AFE
- Computer to load the firmware and capture data from the AFE

4.2 Test Data

All measurements in this section are RMS values. The source uncertainty is ±0.05%. Do not open the current outputs during testing. The inputs must be connected with the AC voltage and current source output programmed to zero, and the output switched OFF.

4.2.1 Functional Testing

The functional testing was done by applying DC input and measuring the power supply output. The required AC RMS voltage and AC RMS currents were applied for testing the functionality of delta-sigma and SAR ADC. The AFE was interfaced to the MSP432P401R LaunchPad for testing.

Table 40 lists the test results.

Table 40. AFE Functional Test Results

PARAMETERS	SPECIFICATIONS	OBSERVATIONS
Non-isolated power	+5 V	4.9780
	+3.3 V	3.2987
Isolated power	+5 V	5.0510
AFE	Current input 1—output DC offset	OK
	Current input 2—output DC offset	OK
	Current input 3—output DC offset	OK
	Current input 4—output DC offset	OK
	Non-isolated voltage 1—output DC offset	OK
	Non-isolated voltage 2—output DC offset	OK
	Current input 1—amplifier gain	OK
	Current input 2—amplifier gain	OK
	Current input 3—amplifier gain	OK
	Current input 4—amplifier gain	OK
	Non-isolated voltage 1—amplifier gain	OK
	Non-isolated voltage 2—amplifier gain	OK
AFE – isolated voltage measurement	Isolated amplifier 1 common-mode DC output	OK
	Isolated amplifier 2 common-mode DC output Isolated amplifier 1 gain	OK
	Isolated amplifier 2 gain	OK
Reference	ADC1 REFP out	2.441
	External Ref 1 out	2.498
	Buffer 1 out	2.498
	Reference comparator1 output	OK
	ADC2 REFP out	2.441
	External Ref 2 out	2.5
	Buffer 2 out	2.5
	Reference comparator2 output	OK
Delta-Sigma ADC input channels functionality	ADC1—CH0	OK
	ADC1—CH1	OK
	ADC1—CH2	OK
	ADC1—CH3	OK
	ADC2—CH0	OK
	ADC2—CH1	OK
	ADC2—CH2	OK
	ADC2 – CH3	OK
SAR ADC input channels functionality	ADC1—CH0	OK
	ADC1—CH1	OK
	ADC1—CH2	OK
	ADC1—CH3	OK
	ADC2—CH0	OK
	ADC2—CH1	OK
	ADC2—CH2	OK
	ADC2—CH3	OK
Delta-sigma clock	16.385 oscillator	OK
	Clock buffer output 1	16.385 MHz
	Clock buffer output 2	16.385 MHz

4.2.2 Summary of Tests Performed

The focus of this TI Design is to test the performance of the following devices:

- ADS131EA04
  The ADC performance was tested by applying voltage and current over a wide range and capturing waveforms for 100 ms and 1000 ms. The ADC sampling rate was fixed at 4000 samples. The accuracy testing was performed with a 2.442-V reference. Two delta-sigma ADCs were chained and the synchronization between ADCs was tested by measuring active power at UPF and 0.5 Lag.
- ADC104S021
  The SAR ADC is for diagnostics and checking if the input is measured within a range of the delta-sigma to confirm the delta-sigma performance is within a range.

Table 41. Summary of Performance Tests Conducted

SERIAL NUMBER	TESTS	DETAILS
1	Unipolar_Input_with _ADC_REFPout_SignalConditioning	Power measurement—multiple devices synchronization
		Isolated and non-isolated voltage measurement—1-sec averaging
		Current measurement—1-sec averaging
		Isolated and non-isolated voltage measurement—100-ms averaging
		Current measurement—100-ms averaging
2	Performance testing—Unipolar_Input_Ext reference for signal conditioning	Voltage, current, and power measurement
		Measurement with isolated voltage input
		Measurement with Rogowski integrator output
3	Performance testing—Bipolar_Input_Ext reference for signal conditioning	Voltage, current, and power measurement
4	Performance testing SAR ADC	DC offset with AMC1200
		RMS measurement
		Peak sample comparison

NOTE: All errors in the following sections are a percentage of the reading.

4.2.3 Performance Testing—Unipolar_Input_with_ADC_Refout_SignalConditioning

Delta-sigma ADCs positive reference voltage output was used for providing the DC common-mode level shift to the AC inputs. This level shifting is required to make the op amp gain output compatible with the ADC input range when the ADC is configured for a 0- to 5-V input.

Power measurements were averaged for 3 seconds (average multiple 1 second values) voltage and current measurements were taken for 1 second and 100 ms

4.2.3.1 Power Measurement—Multiple Devices Synchronization

The synchronization of multiple devices was verified by measuring the accuracy in the combinations in Table 42.

Table 42. ADC Synchronization Combinations

COMBINATION	VOLTAGE	CURRENT
Combination1	ADC2	ADC2
Combination2	ADC2	ADC1

The voltage, current, power, and phase coefficients were kept the same for all combinations, and power accuracy for different current inputs was tested. The measurement accuracy was verified to be within ±0.5% in all conditions. There was no change in the phase error compensation factor in both conditions.

4.2.3.1.1 Non-Isolated Voltage × CT Input

Table 43 and Table 44 provide power measurement accuracy readings for non-isolated voltage and current transformer input.

Table 43. V (DS_ADC2) × I (DS_ADC2)

V-CH6	I-CH7	P-U	P-L	P-U-M	P-L-M	CH6_7 P-U-E	CH6_7 P-L-E	CH6_7 U-L-E
240	0.10	24	12	24.028	12.023	0.117	0.195	–0.079
240	0.25	60	30	60.029	30.038	0.048	0.125	–0.077
240	0.50	120	60	119.923	59.989	–0.064	–0.019	–0.045
240	1.00	240	120	239.804	120.035	–0.082	0.029	–0.111
240	2.50	600	300	599.326	299.813	–0.112	–0.062	–0.050
240	5.00	1200	600	1199.155	600.253	–0.070	0.042	–0.113
240	10.00	2400	1200	2401.153	1201.364	0.048	0.114	–0.066
240	15.00	3600	1800	3600.286	1800.730	0.008	0.041	–0.033
240	20.00	4800	2400	4798.003	2398.922	–0.042	–0.045	0.003
240	30.00	7200	3600	7194.587	3598.082	–0.075	–0.053	–0.022
240	50.00	12000	6000	11988.610	6000.167	–0.095	0.003	–0.098
240	75.00	18000	9000	17997.149	8996.299	–0.016	–0.041	0.025
240	100.00	24000	12000	23981.929	12003.501	–0.075	0.029	–0.104

Table 44. V (DS_ADC2) × I (DS_ADC1)

V-CH6	I-CH0	P-U	P-L	P-U-M	P-L-M	CH6_0 P-U-E	CH6_0 P-L-E	CH6_0 U-L-E
240	0.10	24	12	24.026	12.011	0.107	0.094	0.013
240	0.25	60	30	60.017	30.015	0.029	0.052	–0.023
240	0.50	120	60	119.914	59.965	–0.072	–0.058	–0.014
240	1.00	240	120	240.213	120.112	0.089	0.093	–0.004
240	2.50	600	300	600.171	299.880	0.029	–0.040	0.069
240	5.00	1200	600	1198.956	600.389	–0.087	0.065	–0.152
240	10.00	2400	1200	2399.035	1200.578	–0.040	0.048	–0.088
240	15.00	3600	1800	3598.754	1802.319	–0.035	0.129	–0.163
240	20.00	4800	2400	4802.330	2399.025	0.049	–0.041	0.089
240	30.00	7200	3600	7202.061	3602.318	0.029	0.064	–0.036
240	50.00	12000	6000	12007.262	5999.039	0.061	–0.016	0.077
240	75.00	18000	9000	18021.525	8999.077	0.120	–0.010	0.130
240	100.00	24000	12000	24028.951	12006.789	0.121	0.057	0.064

Figure 37 shows the graph for the previous two accuracy tables.

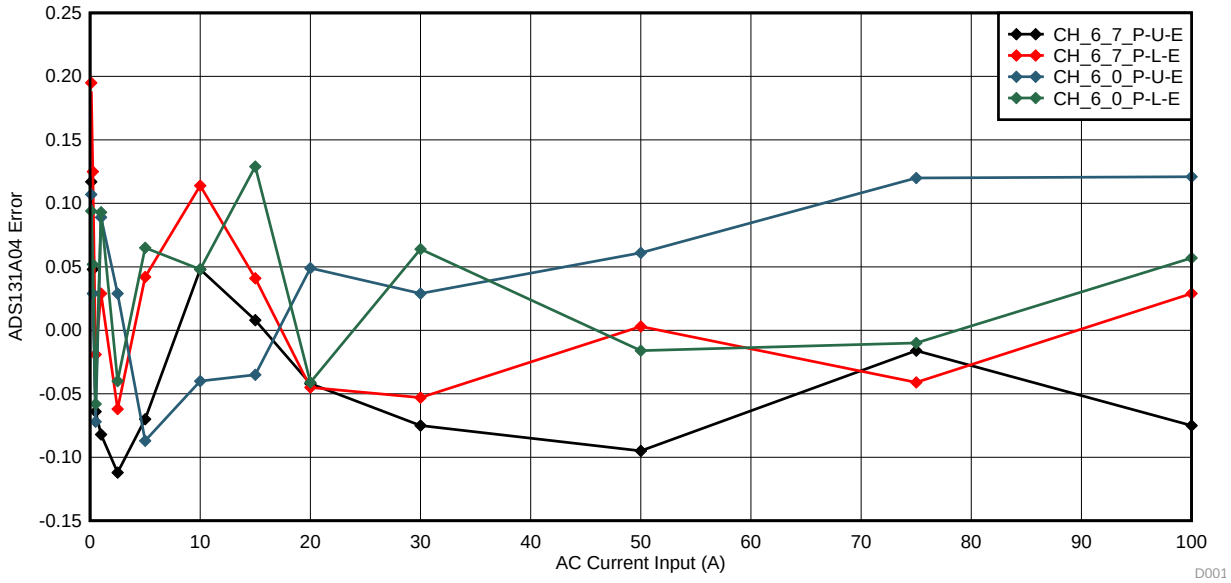


Figure 37. Non_ISO_V_CT_Power Measurement—ADC1 and ADC2

4.2.3.1.2 Isolated Voltage × CT Input

Table 45 and Table 46 provide power measurement accuracy readings for isolated voltage and current transformer input.

Table 45. V (DS_ADC2) × I (DS_ADC2)

V-CH4_Iso	I-CH5	P-U (W)	P-L (W)	P-U-M	P-L-M	CH4_5 P-U-E	CH4_5 P-L-E	CH4_5 U-L-E
240	0.25	60	30	60.035	30.050	0.058	0.167	–0.108
240	0.50	120	60	120.110	60.099	0.092	0.165	–0.073
240	1.00	240	120	240.434	120.276	0.181	0.230	–0.049
240	2.50	600	300	601.200	300.391	0.200	0.130	0.070
240	5.00	1200	600	1201.351	600.935	0.113	0.156	–0.043
240	10.00	2400	1200	2405.050	1201.960	0.210	0.163	0.047
240	15.00	3600	1800	3603.840	1800.921	0.107	0.051	0.055
240	20.00	4800	2400	4811.142	2401.129	0.232	0.047	0.185
240	30.00	7200	3600	7209.648	3605.880	0.134	0.163	–0.029
240	50.00	12000	6000	12022.727	6002.303	0.189	0.038	0.151
240	75.00	18000	9000	18015.882	9004.693	0.088	0.052	0.036
240	100.00	24000	12000	24022.446	12010.484	0.094	0.087	0.006

Table 46. V (DS_ADC2) × I (DS_ADC1)

V-CH4_Iso	I-CH2	P-U	P-L	P-U-M	P-L-M	CH4_2 P-U-E	CH4_2 P-L-E	CH4_2 U-L-E
240	0.25	60	30	60.081	30.033	0.135	0.110	0.024
240	0.50	120	60	120.140	60.051	0.116	0.085	0.031
240	1.00	240	120	240.162	120.047	0.067	0.039	0.028
240	2.50	600	300	600.559	299.774	0.093	–0.075	0.169
240	5.00	1200	600	1200.798	601.080	0.067	0.180	–0.113
240	10.00	2400	1200	2403.026	1201.646	0.126	0.137	–0.011
240	15.00	3600	1800	3601.895	1801.945	0.053	0.108	–0.055
240	20.00	4800	2400	4805.713	2399.741	0.119	–0.011	0.130
240	30.00	7200	3600	7207.286	3605.980	0.101	0.166	–0.065
240	50.00	12000	6000	12019.580	6013.253	0.163	0.221	–0.058
240	75.00	18000	9000	18030.600	9020.381	0.170	0.226	–0.056
240	100.00	24000	12000	24042.923	12025.172	0.179	0.210	–0.031

Figure 38 shows the graph for the previous two accuracy tables.

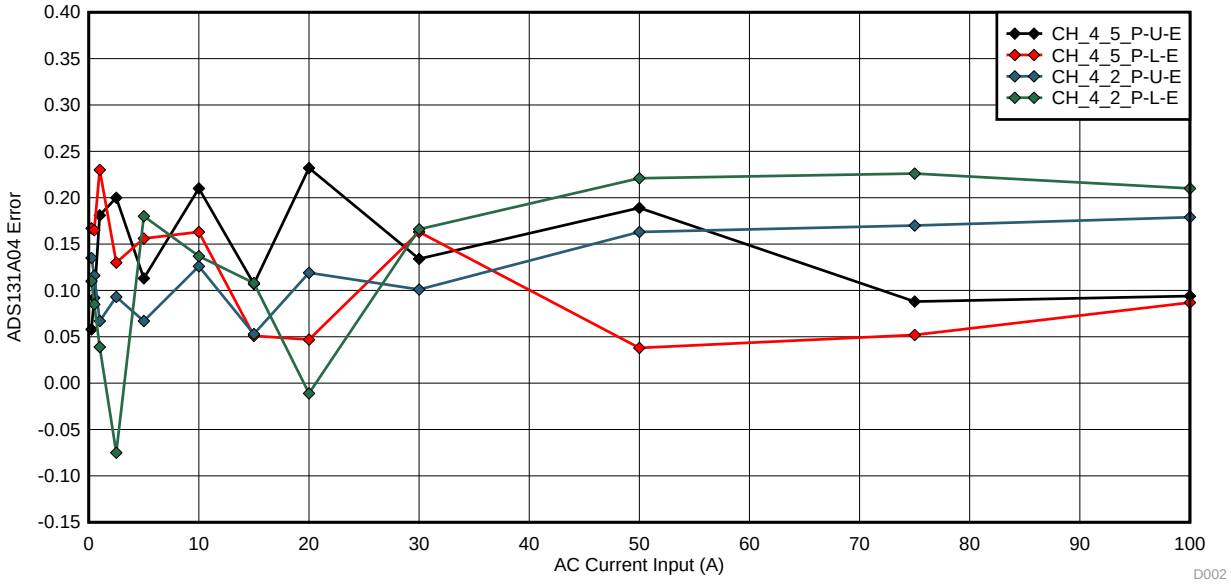


Figure 38. ISO_V_CT_Power Measurement—ADC1 and ADC2

4.2.3.2 Isolated and Non-Isolated Voltage and Current Measurement

Table 47 and Table 48 provide voltage and current measurement accuracies.

Table 47. Voltage and Current Measurement Results 1 Second for ADC1—Isolated and Non-Isolated

APPLIED				MEASURED				% ERROR			
V-CH1	I-CH0	V-CH3-Iso	I-CH2	V-CH1	I-CH0	V-CH3-Iso	I-CH2	V-CH1	I-CH0	V-CH3-Iso	I-CH2
—	0.25	—	0.25	—	0.251	—	0.251	—	0.200	—	0.240
—	0.50	—	0.50	—	0.500	—	0.501	—	0.070	—	0.140
—	1.00	—	1.00	—	1.002	—	1.001	—	0.160	—	0.070
5	2.50	5	2.50	4.997	2.502	5.000	2.501	–0.060	0.076	–0.002	0.044
10	5.00	10	5.00	9.985	5.004	9.990	5.003	–0.150	0.088	–0.100	0.066
25	10.00	25	10.00	24.968	10.007	24.998	10.011	–0.128	0.067	–0.008	0.110
50	15.00	50	15.00	49.898	15.019	50.001	15.019	–0.204	0.127	0.002	0.127
100	20.00	100	20.00	99.832	20.039	100.056	20.030	–0.168	0.196	0.056	0.152
150	30.00	125	30.00	149.856	30.038	125.215	30.019	–0.096	0.127	0.172	0.063
200	50.00	150	50.00	199.965	50.076	150.119	50.074	–0.017	0.151	0.079	0.148
250	75.00	200	75.00	249.980	75.056	200.169	75.043	–0.008	0.075	0.085	0.057
300	100.00	250	100.00	299.818	100.142	250.215	100.043	–0.061	0.142	0.086	0.043

Table 48. Voltage and Current Measurement Results 1 Second for ADC2—Isolated and Non-Isolated

APPLIED				MEASURED				% ERROR			
V-CH4-Iso	I-CH5	V-CH6	I-CH7	V-CH4-Iso	I-CH5	V-CH6	I-CH7	V-CH4-Iso	I-CH5	V-CH6	I-CH7
—	0.25	—	0.25	—	0.251	—	0.251	—	0.340	—	0.300
—	0.50	—	0.50	—	0.501	—	0.501	—	0.220	—	0.280
—	1.00	—	1.00	—	1.001	—	1.002	—	0.140	—	0.230
5	2.50	5	2.50	4.999	2.502	4.999	2.502	–0.020	0.079	–0.022	0.096
10	5.00	10	5.00	9.988	5.002	9.989	5.004	–0.120	0.035	–0.111	0.088
25	10.00	25	10.00	24.972	10.010	24.983	10.004	–0.112	0.099	–0.069	0.040
50	15.00	50	15.00	50.025	15.032	49.909	15.003	0.050	0.213	–0.181	0.023
100	20.00	100	20.00	100.027	20.013	99.956	20.016	0.027	0.067	–0.044	0.082
125	30.00	150	30.00	125.114	30.031	149.872	30.003	0.091	0.103	–0.085	0.009
150	50.00	200	50.00	149.945	50.054	199.910	50.074	–0.037	0.108	–0.045	0.147
200	75.00	250	75.00	200.175	75.102	249.951	75.012	0.088	0.136	–0.020	0.016
250	100.00	300	100.00	250.390	100.154	300.108	100.058	0.156	0.154	0.036	0.058

Figure 39 shows the graph for current measurement of ADC1 and ADC2.

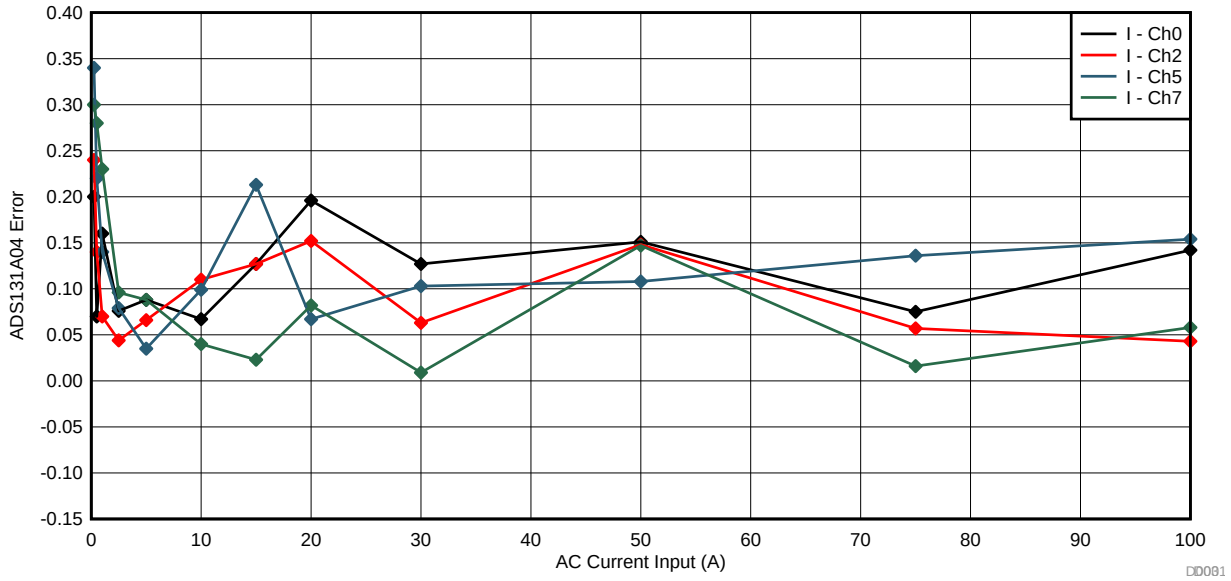


Figure 39. Current Measurement—ADC1 and ADC2

4.2.3.3 Isolated and Non-Isolated Voltage and Current Measurement (100 ms)

Table 49, Table 50, Table 51, and Table 52 show measurement accuracies for voltages and currents.

Table 49. 100-ms Current Measurement for ADC2—CH5

I-CH5 A	MEASURED		% ERROR	
	100 ms	1 sec	100 ms	1 sec
0.5	0.5000	0.5008	0.0010	0.1665
1.0	1.0006	1.0021	0.0583	0.2081
5.0	5.0192	5.0098	0.3839	0.1957
10.0	10.0256	10.0191	0.2564	0.1914
20.0	20.0229	20.0318	0.1144	0.1591
50.0	49.9967	50.0768	–0.0066	0.1535
100.0	100.2778	100.1970	0.2778	0.1970
110.0	110.1756	110.2830	0.1597	0.2572

Table 50. 100-ms Current for ADC1—CH0

I-CH0 A	MEASURED		% ERROR	
	100 ms	1 sec	100 ms	1 sec
0.5	0.5007	0.4990	0.1470	–0.1920
1.0	1.0011	0.9997	0.1149	–0.0300
2.5	2.5026	2.4958	0.1055	–0.1684
10.0	10.0077	10.0006	0.0768	0.0060
20.0	20.0284	20.0244	0.1420	0.1222
50.0	50.0643	50.0340	0.1286	0.0680
75.0	75.0832	75.0914	0.1109	0.1219
100.0	100.2538	100.2134	0.2538	0.2134
110.0	110.2736	110.0939	0.2487	0.0854

Table 51. Isolated Voltage Measurement for AMC1200

VCH4-V	MEASURED		% ERROR	
	100 ms	1 sec	100 ms	1 sec
10	9.981	9.972	–0.190	–0.280
25	24.977	24.955	–0.092	–0.180
110	109.883	109.864	–0.106	–0.124
240	240.087	240.003	0.036	0.001
260	260.186	259.982	0.072	–0.007

Table 52. Voltage With PD for ADC1

VCH1-V	MEASURED		% ERROR	
	100 ms	1 sec	100 ms	1 sec
10	9.986	9.987	–0.140	–0.130
25	24.967	24.913	–0.132	–0.348
110	109.907	109.768	–0.085	–0.211
240	240.024	239.836	0.010	–0.068
300	300.101	299.463	0.034	–0.179

4.2.4 Performance Testing—SAR ADC

4.2.4.1 DC Offset With AMC1200

Table 53 provides the DC level-shifted voltages measured by the SAR ADC.

Table 53. DC Offset Measurement

ADC	CHANNELS	EXPECTED	MEASURED
SAR1	CH1_Cur_CT	2.442	2.42
	CH2_PD_Volt	2.442	2.42
	CH3_Iso_Volt	2.550	2.59
	CH4_Cur_CT_Rogo	2.442	2.42
SAR2	CH1_Cur_CT_Rogo	2.442	2.42
	CH2_Iso_Volt	2.550	2.59
	CH3_Cur_CT	2.442	2.42
	CH4_PD_Volt	2.442	2.42

4.2.4.2 RMS Measurement

Table 54 provides the voltage and current values measured by the SAR ADC.

Table 54. RMS Voltage Measurement

ADC	CHANNELS	APPLIED	MEASURED
SAR1 (U1)	CH1_Cur_CT	1 A	1.252788 A
		5 A	5.159855 A
		20 A	19.746038 A
		100 A	97.736777 A
	CH2_PD_Volt	10 V	10.117 V
		50 V	49.94 V
		110 V	109.84 V
		230 V	229.892 V
	CH3_Iso_Volt	10 V	10.065 V
		50 V	49.902 V
		110 V	109.864 V
		230 V	229.968 V
	—	1 A	0.931638 A
		5 A	4.953084 A
		20 A	20.090649 A
		100 A	100.876436 A

Table 54. RMS Voltage Measurement (continued)

ADC	CHANNELS	APPLIED	MEASURED
SAR2 (U3)	—	1 A	1.224 A
		5 A	4.996778 A
		20 A	19.989207 A
		100 A	99.981346 A
	CH2_Iso_Volt	10 V	10.091 V
		50 V	49.904 V
		110 V	109.895 V
		230 V	230.028 V
	CH3_Cur_CT	1 A	1.275847 A
		5 A	5.129438 A
		20 A	19.722637 A
		100 A	97.792827 A
	CH4_PD_Volt	10 V	10.089 V
		50 V	49.851 V
		110 V	109.857 V
		230 V	229. 949 V

4.2.4.3 Sample Comparison

SAR ADC samples and delta-sigma AFE samples were compared by scaling the SAR ADC samples to match with the delta-sigma ADCs. This comparison must be done due to the resolution difference between SAR and delta-sigma ADC.

Figure 40 shows the SAR ADC output codes plotted to represent the input voltage.

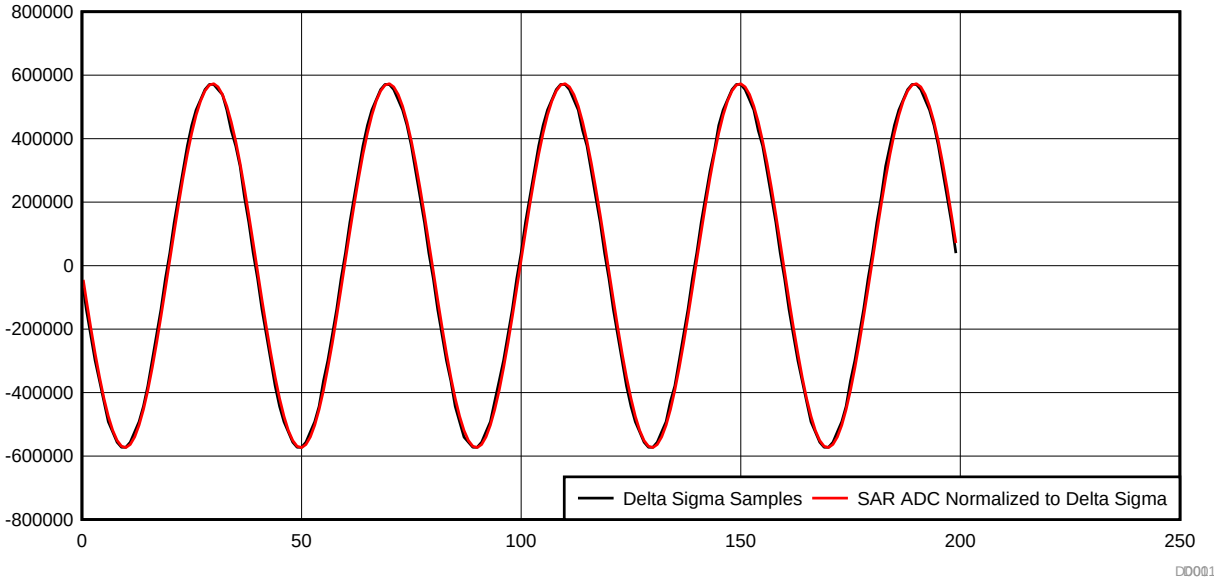


Figure 40. SAR and Delta-Sigma Samples Scaled and Compared for 10-A Input

4.2.5 Summary

Table 55 summarizes the tests done on the ADC board interfaced to the MSP432P401R LaunchPad.

Table 55. Test Results Summary for ADS131A04 AFE With Diagnostics

SERIAL NUMBER	PARAMETERS	OBSERVATIONS
1	Non-isolated power supply	OK
2	Isolated power supply	OK
3	Gain amplifier output – current and voltage	OK
4	Reference output – internal and external	OK
5	ADC interface to MCU	OK
6	Clock buffer output	OK
7	Measurement of voltage and current with different analog input voltage	OK
8	Multiple delta-sigma ADC synchronization test for accuracy	Accuracy within ±0.5% in all combinations
9	Voltage measurement accuracy – isolated or non-isolated	Within ±0.5%
10	Current measurement accuracy	Within ±0.5%
11	Active power-measurement accuracy	Within ±0.5%
12	Diagnostics – SAR and comparator performance	OK

5 Design Files

5.1 Schematics

To download the schematics, see the design files at TIDA-00810.

5.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00810.

5.3 PCB Layout Recommendations

5.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-00810.

5.4 Altium Project

To download the Altium project files, see the design files at TIDA-00810.

5.5 Gerber Files

To download the Gerber files, see the design files at TIDA-00810.

5.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-00810.

6 Software Files

To download the software files, see the design files at TIDA-00810.

7 Related Documentation

1. Texas Instruments, *ADC124S101EVM BoosterPack User's Guide* (SNAU166)
2. Texas Instruments, *ADS131A04 24-bit, Delta-Sigma Analog-to-Digital Converter Evaluation Module* (SBAU259)
3. Texas Instruments, *High Accuracy ±0.5% Current and Isolated Voltage Measurement Reference Design Using 24-Bit Delta-Sigma ADC*, TIDA-00835 Design Guide (TIDUBY8)
4. Texas Instruments, *High-Resolution, Fast Start-Up, Delta-Sigma ADC-Based AFE for Air Circuit Breaker (ACB) Reference Design*, TIDA-00661 Design Guide (TIDUB80)
5. Texas Instruments, *Active Integrator for Rogowski Coil Reference Design With Improved Accuracy for Relays and Breakers*, TIDA-00777 Design Guide (TIDUBY4)
6. Texas Instruments, *Tripping Point: Isolation amplifier-based alternating current voltage measurement in protection relays*, TI E2E Community (https://e2e.ti.com/blogs_/b/smartgrid/archive/2016/10/07/tripping-point-isolation-amplifier-based-alternating-current-voltage-measurement-in-protection-relays)

7.1 Trademarks

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8 Terminology

CT— Current transformer

RTU— Remote terminal unit

DTU— Distribution terminal unit

FTU— Feeder terminal unit

PD— Potential divider

9 About the Authors

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Revision A History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (August 2016) to A Revision	Page
• Changed from preview page	1

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