TI Designs

480-W, 97% η, Ultra-Compact (480 W/in³), Bidirectional DC-DC Reference Design

Description

The TIDA-00705 is an ultra-compact (27 mm × 27 mm × 25 mm), bidirectional DC-DC power converter for use in point of load DC-DC and battery backup power applications. The design's 97% high efficiency optimizes thermal management and extends battery backup time.

The reference design is a two-phase interleaved half-bridge power stage that is controlled using the UCD3138 digital controller and designed for 12-V bus applications. The design is capable of delivering 480 W as a backup power supply (buck converter) and 100 W as a battery charger (boost converter). The design has built-in protection for DC-bus over-current and over-voltage and battery over-current. The design also has phase current balancing to distribute the heat. The thermal performance derating curve with and without forced cooling for varying time periods is presented for effective usage in various end applications.

Resources

TIDA-00705	Design Folder
UCD3138A	Product Folder
CSD16325Q5C	Product Folder
UCD27211A	Product Folder
OPA2192	Product Folder
LM4041	Product Folder
TPS62125	Product Folder

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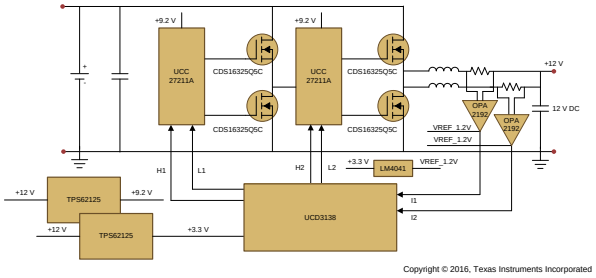
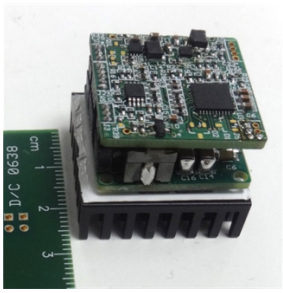
Features

- 97% High Efficiency as Backup Power Supply, Which Optimizes Thermal Management and Extends Battery Backup Time
- Delivers Continuous Power Output of >300W at Minimal Airflow of 200 LFM and 190 W Without Any Airflow
- Ultra-Compact Unit With Heat Sink Built-in (27 mm × 27 mm × 25 mm) and Effective Thermal Management Makes It a Retrofit Into Existing Server Power Supply Units (PSUs)
- UCD3138A Digital Power Supply Controller Solution Enables Programmability and Configurability for Different Voltages and Currents
- Ultra-Fast Changeover in 100 us From Charging to Backup Supply Mode Enables Seamless Power Transfer During Power Failure
- Built-In Battery Charging CC-CV Algorithm Compatible for Li-Ion and Li-Poly Batteries
- Delivers High-Power Output 41 A or 12 V as Backup Supply and Charges Battery at 6 A During Normal Operation

Applications

- Server Power Supply Units (PSU)
- Local Energy Storage (LES) Systems
- Battery Backup Units (BBU)
- Standalone DC-DC for Point of Load (POL) Applications
- DC-DC Non-Isolated Brick Modules





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1 System Overview

1.1 System Description

Battery backup and power storage systems find a role in a lot of industrial applications like uninterruptible power systems (UPSs), servers, and telecom rectifiers to power line communication (PLC) systems. These applications use a wide variety of energy storage elements like super capacitors, lead acid batteries, and li-Ion and li-poly batteries.

A typical battery backup or energy storage bank has the following subsystems:

1. A battery charger subsystem to charge the battery from a power source.
2. A battery discharge subsystem to power a load from the battery.
3. A battery management solution (BMS) system to monitor and protect the battery.

The block diagram of a typical battery backup system is shown in Figure 1.

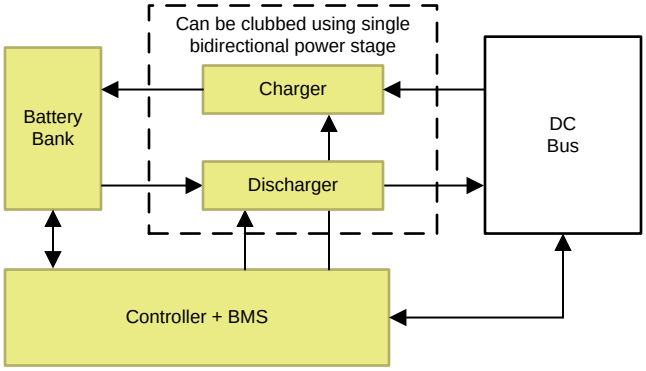

Figure 1. Block Diagram of Typical Battery Backup System

The battery charger subsystem draws power from the DC bus and charges the battery bank. The battery discharge subsystem takes power from the battery bank and feeds it back into the DC bus.

Under normal operating conditions, the battery backup system draws power from the DC bus to charge the battery bank and the battery discharge system remains inactive. Upon power failure at the DC bus input, the battery discharge system begins to immediately feed power into the DC bus. During this time the battery charger system remains inactive.

One way of decreasing the cost and size of the battery backup subsystem is to use a single, bidirectional power converter for doing both battery charging and backup power supply operation. When compared with the traditional arrangement of implementing battery backup systems using two individual power stages, a single bidirectional power stage implementation significantly reduces the number of components.

An additional benefit to using a single, bidirectional power stage is that the mode transition from charging to discharging can be achieved very quickly, which can reduce the bulk capacitor (holdup time) requirement at the DC bus.

The TIDA-00705 design is an ultra-compact, bidirectional DC-DC power converter specifically designed for space-constrained low-voltage battery backup units where high-power density would be required.

The design can charge a four cell li-ion battery pack from a 12-V bus. When the main power goes down, the device seamlessly transfers power to 12-V bus from the li-ion battery pack. The design is based on the UCD3138 digital controller powered interleaved half-bridge power stage, which works as synchronous buck backup supply and synchronous boost battery charger.

The half-bridge power stage is implemented with high-drive current, fast-switching gate driver UCC27211A, and DualCool™ CSD16325Q5C NexFET™ Power MOSFET. The design operates at 700kHz per phase achieving smallest form-factor and optimized high efficiency.

1.2 Key System Specifications

Table 1. Key System Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MINIMUM	NUMBER	MAXIMUM	UNIT
BACKUP SUPPLY MODE (BUCK)						
INPUT CONDITIONS						
Input voltage (battery voltage)	V_{BAT}		13	14.8	16.4	V
Brownout voltage	V_{BAT_UVLO}			13.5		V
OUTPUT CONDITIONS						
Output voltage (bus voltage)	V_{BUS}		11.3	12	12.3	V
Output current (bus current)	I_{BUS}				40	A
Line regulation (14 V – 16.4V_INDC)		At full load			±1	%
Load regulation (14 V – 16.4V_INDC)		10 to 100% load			±1	%
Output voltage ripple		At full load			100	mV
Input voltage ripple		At full load			200	mV
Efficiency		At 100% load	95.86		97.21	%
		At 50% load	97.05		97.62	
		At 20% load	97.19		97.97	
Output power peak					500	W
Output power for two minutes		At 200 LFM fan speed		425		W
Output power for two minutes		At 500 LFM fan speed		480		W
Output power for continuous operation		At 200 LFM fan speed		310		W
Output power for continuous operation		At 500 LFM fan speed		420		W
BATTERY CHARGER MODE (BOOST)						
INPUT CONDITIONS						
Input voltage (bus voltage)	V_{BUS}		13	14.8	16.4	V
Brownout voltage	V_{BUS_UVLO}			11.6		V
OUTPUT CONDITIONS						
Output voltage (bus voltage)	V_{BAT}		13.5	14.8	16.4	V
Output current (bus current)	I_{BUS}				6	A
Output voltage ripple		At full load			200	mV
Input voltage ripple		At full load			100	mV
Efficiency		At 25%, 50%, 75%, and 100% full load	87.87		96.49	%
Output power					100	W

Table 1. Key System Specifications (continued)

PARAMETER	SYMBOL	TEST CONDITIONS	MINIMUM	NUMBER	MAXIMUM	UNIT
Protections		Battery and bus overvoltage, undervoltage, and overcurrent				
Operating ambient			-40	25	55	°C
Dimension		Length × breadth × height	27 × 27 × 25			mm

1.3 Block Diagram

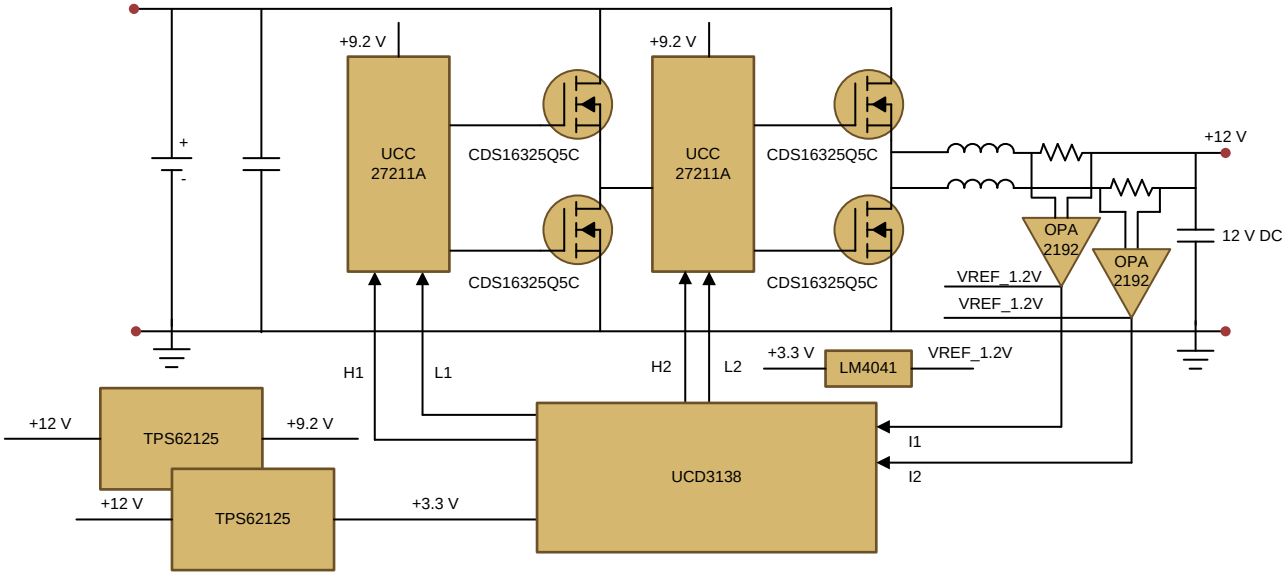

Figure 2. Block Diagram of TIDA-00705

1.4 Highlighted Products

The following are the highlighted products used in this reference design. Key features for selecting the devices for this reference design are described. Complete details of the highlighted devices can be found in respective product data sheets.

1.4.1 UCD3138

To implement high-performance and a small form-factor bidirectional converter design, the UCD3138A is the preferred controller as it offers a series of benefits to address the next generation needs of low-THD norms and provides a digital interface for health monitoring and controls.

The UCD3138A is a fully-programmable, power-optimized digital controller solution that offers the benefits of a simple design to speed up time to market while maintaining ample ability to develop high-performing and well-differentiated power supply solutions. Along with the general purposes of a microcontroller, the device is built to include a configurable digital state machine optimized to meet the performance requirements of telecom and server isolated power applications. The controller features optimized digital hardware for implementing many cutting edge power management functions such as burst mode, ideal diode emulation, mode switching, synchronous rectification, and reduced constant current consumption. In summary, the UCD3138A addresses all key concerns such as high efficiency across the entire operating range, high degree of flexibility for various control schemes and topologies, high integration for increased power density, high reliability, and lowest overall system cost.

Other key features include:

- Digital control of up to three independent feedback loops
- Up to 16-MHz error analog-to-digital converter (EADC)
- Up to eight high-resolution digital pulse width modulated (DPWM) outputs
- Fully-programmable, high-performance, 31.25 MHz, 32-bit ARM7TDMI-S™ processor
- 14-channel, 12-bit, 267-ksps general purpose ADC with integrated filters
- Communication peripherals (I²C/PMBus, UART)
- Configurable pulse width modulation (PWM) edge movement
- Configurable feedback control
- Configurable modulation methods
- Fast, automatic, and smooth mode switching
- High efficiency and light load management
- Soft start and stop with and without pre-bias
- Fast input voltage feed forward hardware
- Rich fault protection options
- Internal temperature sensor
- Timer capture with selectable input pins
- Up to five additional general purpose timers
- Built-in watchdog: brown out detection (BOD) and power on reset (POR)
- Operating temperature: –40°C to 125°C

1.4.2 CSD16325Q5C

For effective thermal management in small form-factor, high-power density designs, it is vital to have high-efficient devices and the capability to extract heat effectively.

The CSD16325Q5C is a DualCool NexFET power MOSFET optimized for synchronous buck applications. It is a 25-V MOSFET with ultra-low Qg of 18 nC, Qgd of 3.5 nc, and low Rdson of 1.4 mΩ at 25°C.

The design is optimized for two-sided cooling with low thermal resistance from junction to case.

The ability to extract heat from both sides of the MOSFET is a key parameter in enabling high power density in this application as it allows the designer to mount heat sink to the top of the MOSFET, which increases the power handling capability of the FET in most applications.

The Qg, Qgd, and Rdson parameters make this MOSFET an ideal choice for this application in which both the switching and conduction losses must be minimized.

More details on this FET can be obtained from the *DualCool N-Channel NexFET Power MOSFETs* data sheet.

1.4.3 UCC27211A

For high-power density designs, it is important to have high-frequency operation. This design requires a fast-switching driver capable of sourcing and sinking high currents.

The UCC27211A is a half-bridge gate driver capable of sourcing and sinking up to 4-A gate driver current. With very low pullup and pull down resistances, this device reduces the transition time of the power MOSFET through the miller region, which minimizes the switching loss on the MOSFET. The device is a robust half-bridge gate drive with input pins capable of tolerating up to -10-V input voltage.

This design takes advantage of this device's ability to minimize the switching loss on the power MOSFET and to operate at a high-switching frequency of >700 KHz per phase while performing hard switching off the main MOSFET.

More details on this driver can be obtained from the *CC27211A 120-V Boot, 4-A Peak, High-Frequency High-Side and Low-Side Driver* data sheet.

1.4.4 LM4041-N

The LM4041-N is a precision voltage reference, which gives a fixed 1.2-V reference voltage. The LM4041-N device's advanced design eliminates the need for an external stabilizing capacitor while ensuring stability with any capacitive load, which makes the LM4041-N easy to use. Bandgap reference temperature drift curvature correction and low-dynamic impedance ensure stable reverse breakdown voltage accuracy over a wide range of operating temperatures and currents.

The LM4041-N 1.2 is used to provide a precise reference offset voltage to the OPA2192-based, current-sense amplification circuit to enable bidirectional current sensing.

More details on the LM4041-N 1.2 can be obtained from the *LM4041-N-xx Precision Micropower Shunt Voltage Reference* data sheet.

1.4.5 OPA2192

The OPAX192 family is a new generation of 36-V, e-trim™ operational amplifiers. These devices offer very low input offset voltage, voltage drift, and an ability to operate with differential inputs close to the supply rail.

With close to 140-dB CMRR, this device is ideally suited for use in the TIDA-00705.

In this design, the OPA2192 is used for measuring high frequency (>700 KHz) switching currents flowing through the inductor. In order to sense the current across the sense resistor placed in series with the inductor, an opamp with high CMRR and BW is required. The OPA2192 opamps meets the required of the design.

More details on the OPA2192 can be obtained from the data sheet *OPAx192 36-V, Precision, Rail-to-Rail Input/Output, Low Offset Voltage, Low Input Bias Current Op Amp with e-trim* data sheet.

1.4.6 TPS62125

The TPS62125 is a high efficiency, synchronous buck converter with integrated MOSFET for providing up to 300-mA output current. The device can work from 3- to 17-V input voltage with a quiescent operating current of 13 uA and around 350 nA when shutdown.

Needing only a minimum number of external components and with an ability to operate at up to 1-MHz switching frequency, this device is ideal for the TIDA-00705 as it minimizes the sizing of the external inductor and capacitors.

In the TIDA-00705 the two TPS62125 devices are used to generate the 3.3 V required for the UCD3138 and the 8.2 V for the UCC27211A gate driver.

More details on the TPS62125 can be obtained from the *TPS62125 3-V to 17-V, 300-mA Step-Down Converter With Adjustable Enable Threshold and Hysteresis* data sheet.

2 System Design Theory

This reference design is a 480-W, DC-DC bidirectional power converter. The key aim of this design is to develop a high efficiency ultra-compact, non-isolated bidirectional power converter which can transfer 500-W power from a four-cell lithium ion and poly battery pack to a 12-V bus and vice-versa. This is realized using a two-phase, interleaved half bridge power stage, operating at high switching frequency of 700 kHz, optimizing filter inductor, input and output filter capacitors, and distribution of losses across the phases for effective thermal management.

It is important to optimize the right switching frequency as a low frequency operation can increase the flux swing on the inductor, the turnoff, and the conductions losses of the FET while reducing the turnon loss. Also, output capacitors need to suppress the ripple are larger. Similarly, a high-switching frequency increases the FET-switching loss and inductor-core loss. Considering these trade-offs, a per phase switching frequency of 700 KHz is selected. The effective output and input switching frequency for suppressing the voltage ripple on the capacitors becomes equal to 1.4 MHz.

Operating as a backup supply, the half bridge power stage works as a synchronous buck converter and transfers power from the battery pack to the 12-V bus. In this mode the TIDA-00705 delivers a peak output power of 480 W. While working as a battery charger, the half bridge power stage works as a synchronous boost converter and transfers power from the 12-V bus to the battery pack. The peak charging power required depends on the battery pack configuration and currently designed and tested for 100 W.

2.1 Operating Principle

When operating as the *synchronous buck converter* the high side MOSFET Q1 works as the main MOSFET and the low-side MOSFET Q2 works as the freewheeling MOSFET. The power flow path during the main MOSFET turn and the freewheeling phase is shown in the Figure 3.

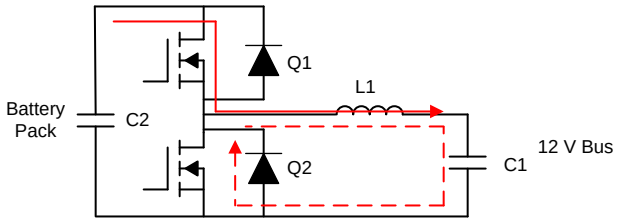

Figure 3. Power Flow While Working as Synchronous Buck Power Stage

When operating as a synchronous boost converter, the low-side MOSFET Q2 works as the main MOSFET and the high side MOSFET Q1 works as the freewheeling and synchronous MOSFET. The power flow path during the main MOSFET turnon and the freewheeling phase is shown in the figure below.

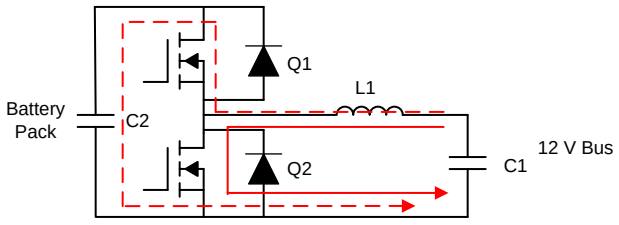

Figure 4. Power Flow While Working as Synchronous Boost Power Stage

2.2 Hardware Design and Component Selection Criteria

In the following sections calculations for the power stage are shown along with approximate loss estimation on the major components.

2.2.1 Current Calculations

The maximum average output current can be calculated using the following equation:

$$I_{out(max)} = \frac{P_{out(max)}}{V_{out(max)}} \quad (1)$$

$$I_{out(max)} = \frac{500\ W}{12\ V} = 41.7\ Amp \quad (2)$$

This output current is the sum of the average current of the two phases. The average current on each phase can then be calculated as:

$$I_{ph1(max)} = I_{ph2(max)} = \frac{I_{out(max)}}{2} = 20.85\ Amp \quad (3)$$

The input current will be the maximum when the battery voltage is equal to the bus voltage and will be equal to the output current.

$$I_{in(max)} = I_{out(max)} = 41.7\ Amp \quad (4)$$

2.2.2 Inductor L1 and L2

The maximum inductance required can be calculated from the maximum input voltage and the inductor ripple current that can be allowed. In typical synchronous buck and boost application the induct ripple current is between 20 and 40% of the average output current. In this application in order to meet the dimension requirements, the inductor ripple current is taken as 100% average output current.

The minimum duty cycle operation at full output load is obtained when the input battery voltage is at its maximum. This is given by:

$$VBat(max) = 16.8\ V \quad (5)$$

$$D(min) = \frac{Vout}{VBat(max)} = \frac{12}{16.8} = 0.71 \quad (6)$$

The minimum inductor can then be calculated from the following equation:

$$L\,min = \frac{\left(\left(VBat\left(max\right) - Vout\right) \times D\left(min\right)\right)}{\left(Iripple \times Fsw\right)} \quad (7)$$

$$L\,min = \frac{\left(16.8 - 12\right) \times 0.71}{20.85 \times 700 \times 10^{3}} = 233\ nH \quad (8)$$

An inductor with 230-nH inductance was chosen.

The maximum loss on the inductor occurs at the maximum input voltage. The loss on the inductor can be divided into the core losses and the root mean square (RMS) current induced losses. The core loss depends on the switching frequency, flux swing, and the RMS current induced losses are dictated by the DC resistance (DCR) of the inductor.

$$P_{Indloss} = P_{Indcoreloss} + P_{IndDCRloss} \quad (9)$$

The core loss can be calculated by using the formulae and graph given in the inductor data sheet. In this design the FP1208R1-R23-R inductor has been selected.

Calculate the flux swing B_{pp} in Gauss from the parameters mentioned in the *HIgh Frequency, HI Current Power Inductors Flat-Pac™ FP1208 Series*.

$$B_{pp} = 283 \times L\left(nH\right) \times Iripple \times 10^{-3} = 1366.89\ G \quad (10)$$

By using the obtained B_{pp} and F_{sw} in the Core Loss versus Gauss chart given in the *HIgh Frequency, HI Current Power Inductors Flat-Pac™ FP1208 Series* data sheet. It can be seen that the estimated core loss PIndcoreloss is approximately equal to 0.15 W.

The RMS current induced losses due to the DCR of the inductor can be calculated by using the following equation:

$$P_{IndDCRloss} = \left(I_{indRMS}\right)^2 \times DCR = \left(21.81\right)^2 \times 0.29 \times 10^{-3} = 0.138 \text{ W} \quad (11)$$

Therefore the total inductor losses (per phase) are approximately equal to $P_{Indloss} = 0.288$ W.

2.2.3 Switching MOSFET

In hard-switched synchronous buck topology, the switching MOSFET undergoes losses at turnon, conduction, and turnoff. However, the freewheeling MOSFET does not suffer turnon or turnoff losses but only suffers MOSFET and internal body diode conduction loss. There is also an additional body diode reverse recover loss of the bottom freewheeling FET.

The compact nature of the design poses another significant challenge in terms of thermal management. Because the major losses in this design are going to be on the switching FET, the chosen FET should allow for a easy way to remove heat from it.

One of the major challenges in this design is choosing a FET which can help in minimizing the switching and conduction losses, which also allows for efficient heat removal.

The CSD16xxx FET was chosen as it has a very low Rdson and an ultra-low Qg and Qgd, which can help decrease the conduction and switching losses. Additionally this device is a DualCool FET, which can be cooled on both the top and bottom sides. This feature is very important for this design as the heat sink can be connected to the top of the FET to effectively extract heat.

2.2.3.1 Losses in the High-Side Switching MOSFET

In the following section the loss estimation on each of the FET per phase is analyzed under the maximum input voltage conditions.

As described in Section 2.2.3, the losses in the high-side MOSFET can be divided into conduction loss and switching loss. The switching loss can be further divided into turnon loss and turnoff loss.

The conduction loss depends on the Rdson and the RMS current through the MOSFET. The RMS current through the MOSFET Q1 can be given as:

$$Ihs\left(RMS\right) = sqrt\left(D\left(min\right) \times \left(Iphi\left(avg\right)^2 + \frac{Iripple^2}{12}\right)\right) = 18.4 \text{ Amp} \quad (12)$$

Assuming the maximum temperature of the MOSFET in the period is 90° C, the Rdson(90°) of the MOSFET at this temperature can be obtained from the data *DualCool N-Channel NexFET Power MOSFETs* data sheet, which is equal to 1.875 mΩ.

The conduction loss is then as follows:

$$Phs_{cond} = Ihs\left(RMS\right)^2 \times Rdson\left(90^\circ\right) = 18.4^2 \times 0.001875 = 0.636 \text{ W} \quad (13)$$

The turnon process of a MOSFET when switching an inductive load can be broken down into many intervals (Figure 5)

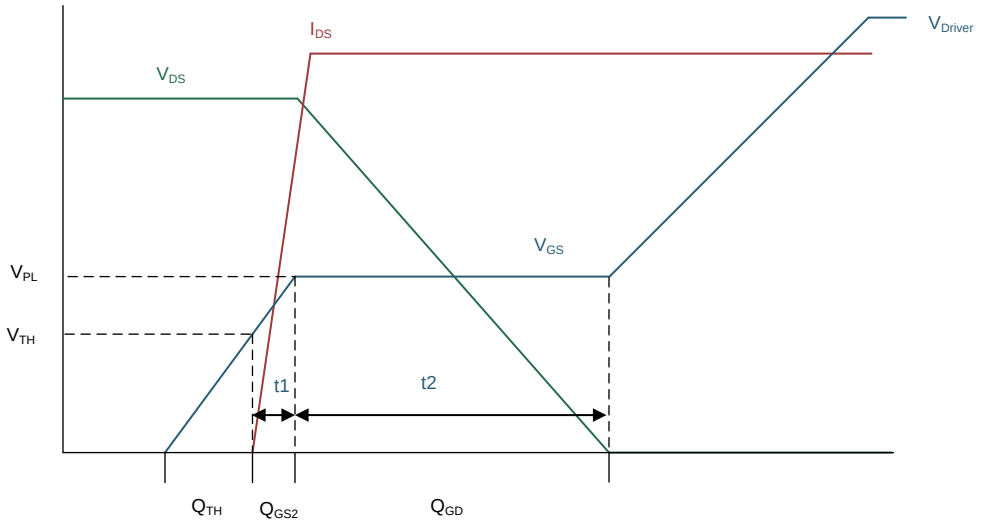

Figure 5. MOSFET Turnon

In the t1 interval, the V_{GS} raises from zero to V_{TH}. In this duration the V_{DS} stays high and the I_{DS} is zero because the MOSFET does not conduct yet. In this interval the power loss on the MOSFET is zero.

In the t2 interval, as the V_{GS} raises above the V_{TH} to reach the miller plateau voltage (V_{PL}), the drain current (I_{DS}) increases from zero to the inductor current, and the V_{DS} stays high. This duration is the period in which the MOSFET input capacitance (C_{iss}) is charged. The overlap between V_{GS} and I_{DS} results in a switching loss.

During the t3 interval, the V_{GS} stays at V_{PL} as the voltage (V_{GS}) across the MOSFET falls close to zero. The overlap between V_{GS} and I_{DS} in the duration of t3 also results in a switching loss.

It can be seen that the switching loss during turnon occurs mainly during t2 and t3. This loss can be estimated as:

$$Phs_{on} = \frac{Fsw \times Vds(max) \times Ids(turnon) \times (t1 + t2)}{2} \tag{14}$$

Considering 100% ripple current the:

$$Ids(trunon) = 0.5 \times Iph1(max) = 10.425 \text{ Amp} \tag{15}$$

$$t1 + t2 = \frac{Qsw}{IGate_{on}} \tag{16}$$

Where $Qsw = Qgs - Qth + Qgd = 7$ nC

The value of the Qgs, Qth, and Qgd can be obtained from the DualCool N-Channel NexFET Power MOSFETs data sheet.

Now $$IGate_{on} = \frac{(V_{Driver} - V_{PL})}{(R_{DriverHS} + R_G)} = \frac{(8.2 - 2.5)}{(0.9 + 1.6)} = 2.28 \text{ Amp}$$.

Using the above results the value of t1 + t2 can be estimated as:

$$t1 + t2 = \left(\frac{7}{2.28}\right) nS = 3.07 \text{ nS} \tag{17}$$

Substituting this in the equation, the Phs_{on} can be calculated as:

$$Phs_{on} = 0.19 \text{ W} \tag{18}$$

However, the actual turnon loss will be slightly higher than this due to the presence of the common source inductance.

Similarly the MOSFET high-side MOSFET turnoff loss also can be determined.

The MOSFET turnoff loss is given by following:

$$Phs_{off} = \frac{Fsw \times Vds(max) \times Ids(turnoff) \times (t1 + t2)}{2} \quad (19)$$

Here $Ids(turnoff) = 1.5 \times Iph1(max) = 31.275\ Amp$

$$t1 + t2 = \frac{Qsw}{IGate_{off}} \quad (20)$$

Where $IGate_{off}$ is given by $IGate_{off} = \frac{Vpl}{R_{DriverHS} + R_G} = \frac{2.5}{2.5} = 1\,A$.

Therefore $t1 + t2 = \left(\frac{7}{1}\right) nS = 7\ ns$.

Substituting these values in the equations , the turnoff loss can be calculated as:

$$Phs_{off} = 1.29\ W \quad (21)$$

The reverse recovers losses from the body diode of the low-side MOSFET, which can be estimated using the following equation:

$$Plss = Qrr \times Vin(max) \times Fsw \quad (22)$$

Here the Q_{rr} is the reverse recovery charge and can be obtained from the *DualCool N-Channel NexFET Power MOSFETs* data sheet. For the CSD16xxx used in this design, the $Plss = 63\ nC \times 16.8\ V \times 700\ KHz = 0.74\ W$.

The losses in the output capacitance of both the high side MOSFET can be given by the following equation:

$$Phs_{Coss} = \frac{Coss \times Fsw \times Vin(max)^2}{2} \quad (23)$$

From the *DualCool N-Channel NexFET Power MOSFETs* data sheet, the MOSFET Coss can be obtained as $Coss = 2.2\ nF$.

Substituting this value in the equation gives the $Phs_{coss} = 0.2173\ W$.

2.2.3.2 Losses in the Low-Side Switching MOSFET

In hard-switched continuous conduction mode (CCM) synchronous buck and boost the turnon of the low-side MOSFET happens under the zero voltage switching (ZVS) condition as the voltage across the MOSFET is clamped by the current flowing through its internal body diode. The turnoff also occurs under ZVS condition if the current through the MOSFET is greater than zero at turnoff.

In the current design, at full load the turnon and turnoff losses can be neglected. To calculate the conduction loss:

$$Pls_{cond} = Ils(RMS)^2 \times Rdson(90°) \quad (24)$$

Where $Ils(RMS) = sqrt\left(1 - D(min) \times \left(Iph1(avg)^2 + \frac{Iripple^2}{12}\right)\right) = 11.77\ Amp$

This gives Pls_{cond} = 0.259 W.

The body diode losses during the dead time can be given by the following:

$$Pls_{diode} = V_{diode} \times \left((Iph1(avg) - Iripple) \times TD1 + (Iph1(avg) + Iripple) \times TD2\right) \times Fsw \quad (25)$$

In the TIDA-00705 the value of the TD1 = TD2 = 25ns. Substituting this value in the above equation gives the diode conduction loss as $Pls_{diode} = 0.508\ W$.

2.2.4 Current Sense

To measure the current through each phase, a current sense resistor is placed in series with each inductor. A 0.5-Ω current sense resistor is used to minimize the losses on the sense resistor.

Because the current sense signal across the sense resistor will have a high-switching frequency combined with high common mode voltage, this design uses the OPA2192 opamp due its high common mode rejection ratio (CMRR) and gain bandwidth (GBW) product. A two-stage amplification amplifies the measure current sense signal by 30 times.

The output of the second stage of the amplification will have an offset of 1.25 V to enable the bidirectional current sensing required by this design.

2.2.5 Input Capacitors

The dimensions of the input capacitors are created based on the buck mode operation. Assuming a maximum of 100-mV ripple on the input voltage, the required value of the input capacitors can be calculated on the basis of the following equation. It can be seen that the below equation does not take into account the effect of equivalent series resistance (ESR) on the ripple. Therefore to get an approximate estimate of the required capacitance, the term $Vinripple_{ppmax}$ is taken as 75 mV.

$$Cin_{minimum} = \frac{\left(Iout(max) \times D(min) \times \left(1 - D(min)\right)\right)}{\left(Fsw_{comb} \times Vinripple_{ppmax}\right)} \tag{26}$$

The following equation substitutes the values of the known quantities in the above equation:

$$Cin_{minimum} = \frac{41.7 \times 0.2042}{1.4 \times 10^{6} \times 75 \times 10^{-3}} = 81\ uF \tag{27}$$

The above calculation neglects the effects of ESR on the ripple voltage. Including the ESR which is less than 0.5 Ω, the observed ripple will slightly higher than 75 mV.

Because ceramic capacitors show a decrease in effective capacitance as the DC bias voltage applied across it increases, care should be taken to account for the effective capacitance instead of the using the nominal value.

In this design four 22-µF and four 10-µF capacitors are used in parallel to provide the input capacitance.

2.2.6 Output Capacitors

The worst case output ripple current occurs in the two-phase interleaved buck converter when the duty cycle reaches 25% and 75% . This ripple current given as $Ioutripple_{pp}$ will be about 0.25 × Iout(max).

Therefore $Ioutripple_{pp} = 10.425\ Amp$

The minimum required output capacitance can be calculated using the following equation by assuming $Voutripple_{pp}$ as 75 mV.

$$Cout_{minimum} = \frac{Ioutripple_{pp}}{8 \times Fs_{comb} \times Voutripple_{pp}} = 12uF \tag{28}$$

Considering the effect of ESR and the effect of DC bias on the capacitance, eight 10uF capacitors are connected in parallel to provide the output capacitors.

3 Getting Started Software and Hardware

This section details the necessary equipment, test setup, and procedural instructions to program the TIDA-00707 board with the provided software.

3.1 Software

3.1.1 Programming the UCD3138A

The design needs the following equipment and necessary files to program the device:

- **PMBus-to-USB interface adapter kit: the USB interface adapter (HPA172)**
  Accessories include:
  - USB interface adapter
  - USB cable (five-pin B mini male to type A male)
  - Ribbon cable (socket-to-socket, ten pin, two headers, polarized)
  - Four male-to-female interface wires to connect USB interface adapter to connecter J5 on TIDA-00705 board

Figure 6. USB Interface Adapter for Programming UCD3138

- **GUI installations file:** *TI-Fusion-Digital-Power-Designer-2.0.16.exe* or later version
- **Firmware File:** *Boost_Buck.x0* file, which is located in the software package folder path \TIDA0705\Firmware\Firmware\Firmware\Boost_Buck\Boost_Buck\UCD3138
- **PC operating system:** Microsoft Windows XP, Vista, or Windows 7

3.1.1.1 GUI Setup

- File for installation:
  1. The GUI installation file is *TI-Fusion-Digital-Power-Designer-Version-2.0.16.exe* (or a later version).
- Installation:
  1. Double click and launch the *.exe* file to start the installation.
  2. Click *Next* all the way through the prompts.
  3. Click *I accept the agreement* after reading it.
  4. Click *Install*.
- Launch UCD3138 GUI:
  1. Click the Windows *Start* button.
  2. Click *All Programs*.
  3. Click *Texas Instruments Fusion Digital Power Designer*.
  4. Click *Device GUIs*.
  5. Click *UCD3xxx & UCD9xxx Device GUI*.

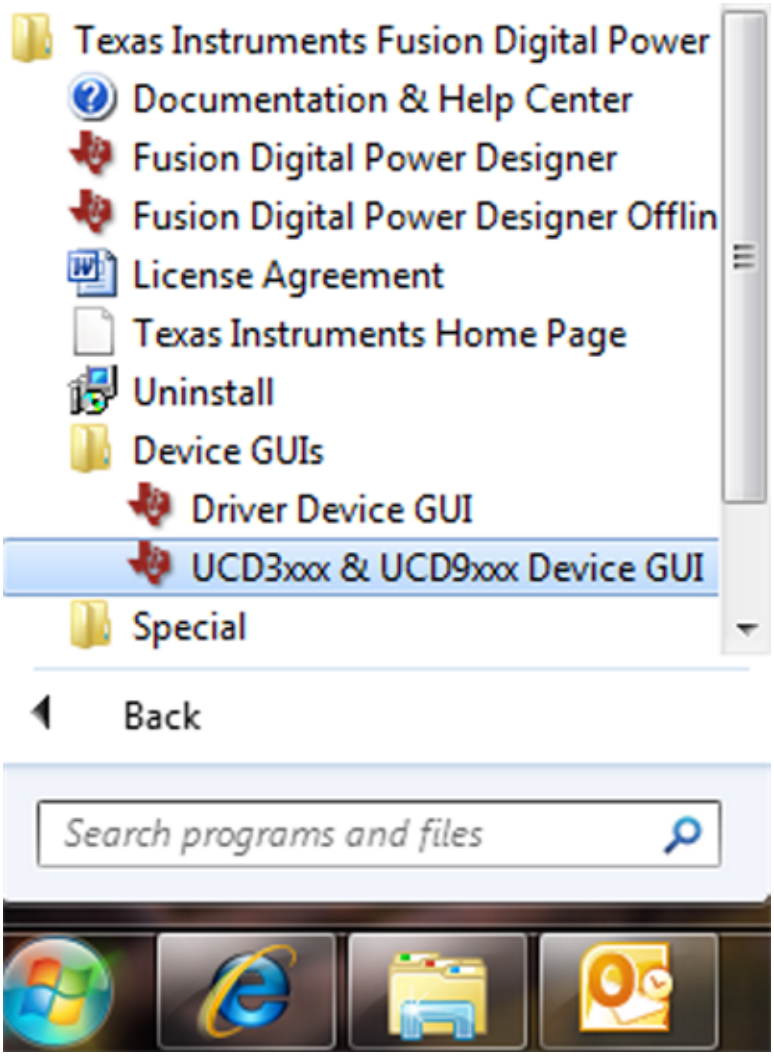

Figure 7. GUI Launch Path

3.2 Hardware

3.2.1 Setup Overview

Figure 8 shows the connection between the TIDA-00705 and the PC through a USB interface adapter (HPA172).

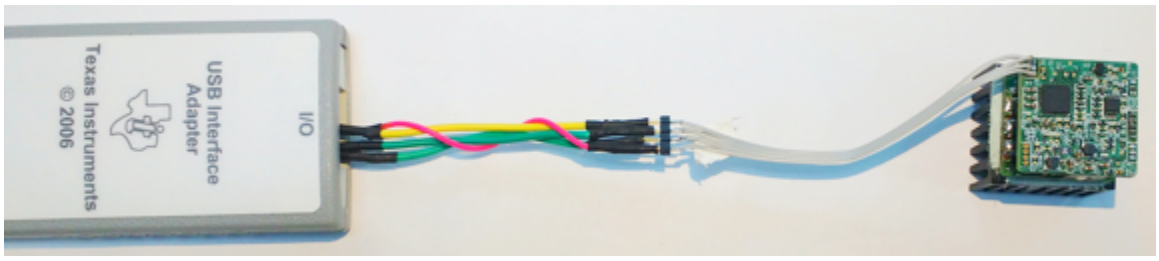

Figure 8. TIDA-00705 Setup for Programming UCD3138

3.2.2 USB Adaptor Connection

1. Use four jumper cables (male on one end and female on the other end) to connect the connector J7 of the TIDA-00705 board and the connector of USB interface adapter (HPA172). The connection details are shown in Table 2.

Table 2. Connection Details

PIN NUMBER ON THE CONNECTOR OF USB INTERFACE ADAPTER (HPA172) (FROM)	PIN NUMBER ON CONNECTOR J5 OF TIDA-00705 CONTROL CARD (TO)
5	1
6	10
9	3
10	5

2. Connect the mini connector of the USB cable to the USB interface adapter and connect the other end to the USB port of the PC.
3. The LED on HPA172 should light. If the LED does not light, unplug the USB cable and reconnect. If the LED is still does not light, change with a new HPA172 USB adapter. Once the LED lights, proceed to the next step.

3.2.3 Procedure

1. Launch the GUI following the steps described in Section 3.1.1.1. Wait until the window shown in Figure 9 appears.
2. Click Scan Device in ROM Mode then wait and check Figure 9 on its Log and confirm Found ROM v2 IC v3 – UCD31xx. If Found ROM is not shown, click Device ID. Click Command Program to jump to ROM (sendByte0xD9) and then click Scan Device in ROM Mode again. If the device is found, proceed to the next step.

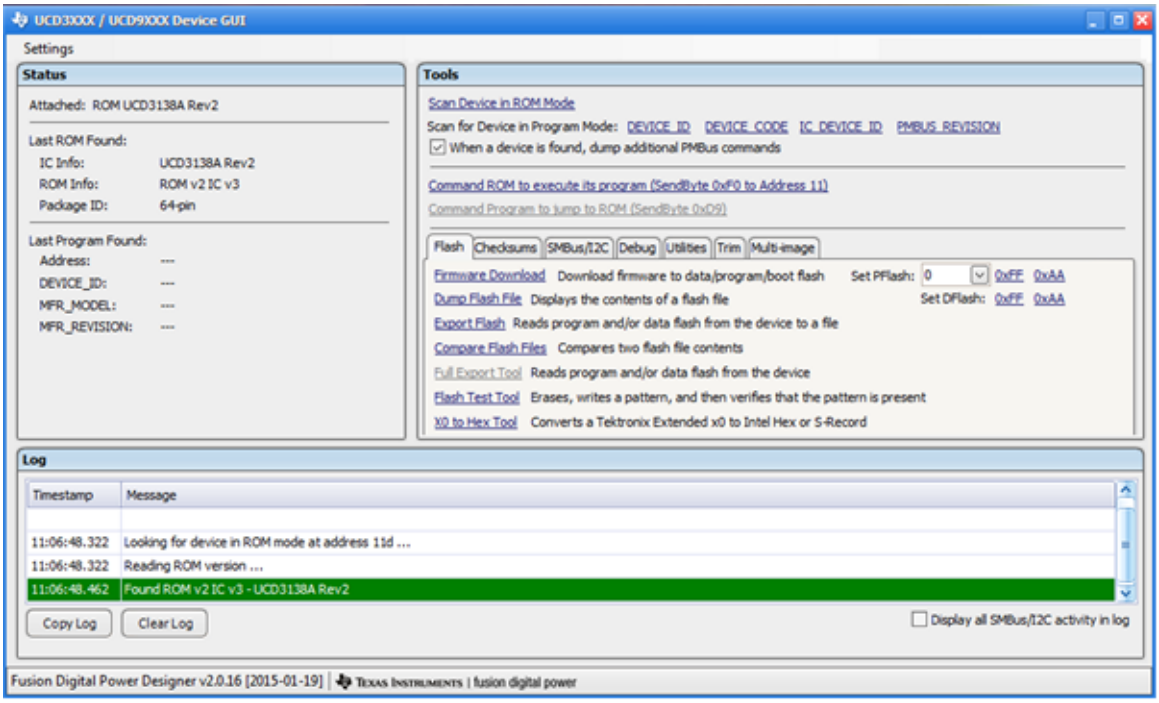

Figure 9. GUI Screenshot Indicating UCD3138 is Detected Successfully in ROM Mode

3. Once the GUI is shown as in Figure 9, click *Firmware Download*. A new window will appear, as in Figure 10. In this new window:
   (a) Check *Download data flash*.
   If the *DO NOT write program checksum* is selected (as shown in Figure 10), the firmware will not be executed once the board is powered up. Click *Command ROM to execute its program* to execute the program.
   If the *Write program checksum* is selected, the firmware will be executed automatically once the board is powered up.
   (b) Click *Select file* and find *Boost_Buck.x0* file. Click *Download*.
   (c) After downloading the program, click *Close* to close the window shown in Figure 10.

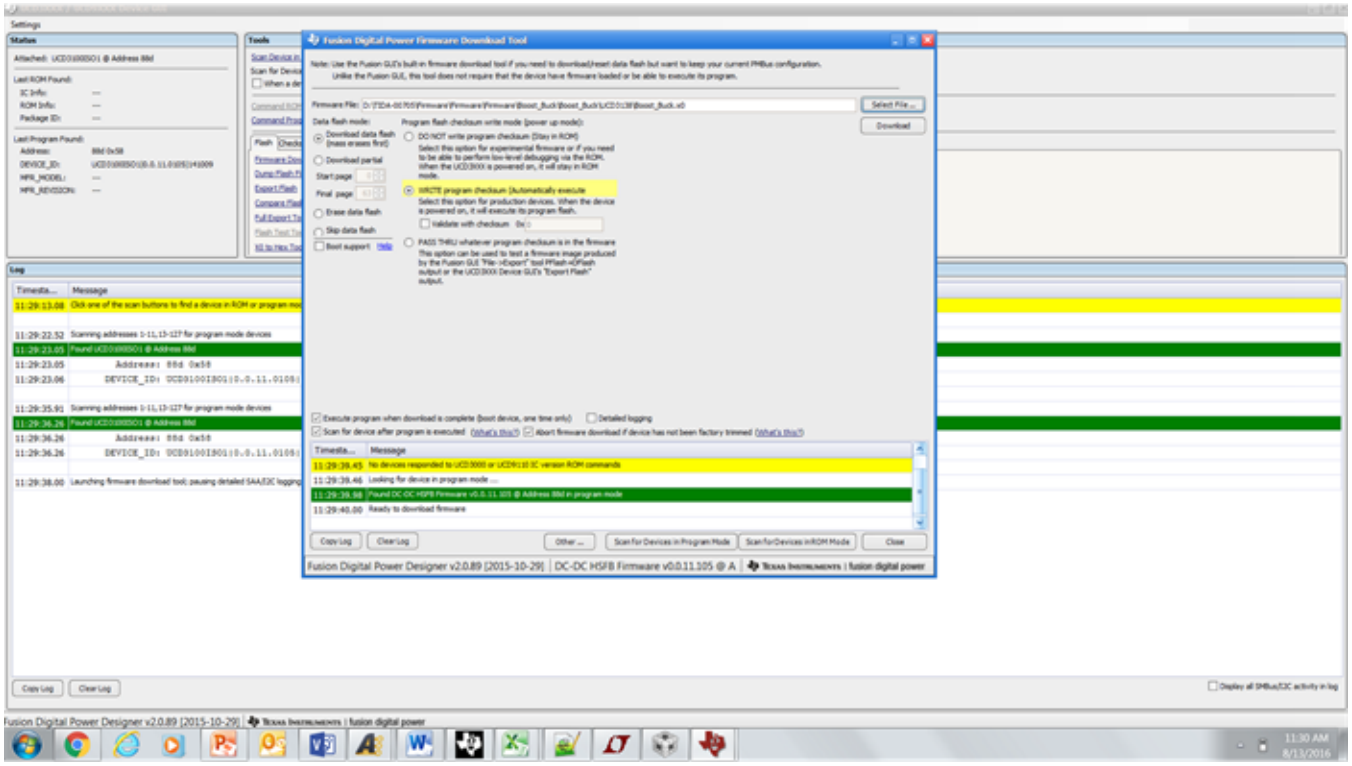

Figure 10. GUI Screenshot Showing the Settings and the File to be Downloaded to UCD3138

4 Testing and Results

4.1 Testing

4.1.1 Conditions

To test the TIDA-00705 two power supplies are used: one emulating the battery and the other emulating the 12-V bus. Electronic loads are used for applying load.

4.1.2 Equipment

1. Two DC power supplies capable of supplying up to 40-A current
2. Digital oscilloscope
3. At least two multimeters with greater than four-and-a-half digit accuracy for measuring efficiency
4. Precision current shunt resistors for measuring current
5. Electronic loads or resistor loads

4.1.3 Procedure

Figure 11 shows the setup recommendations for testing the TIDA-00705. The setup does not show the connections to the multimeters for measuring various voltages and currents. These can be connected by the user accordingly for testing efficiency.

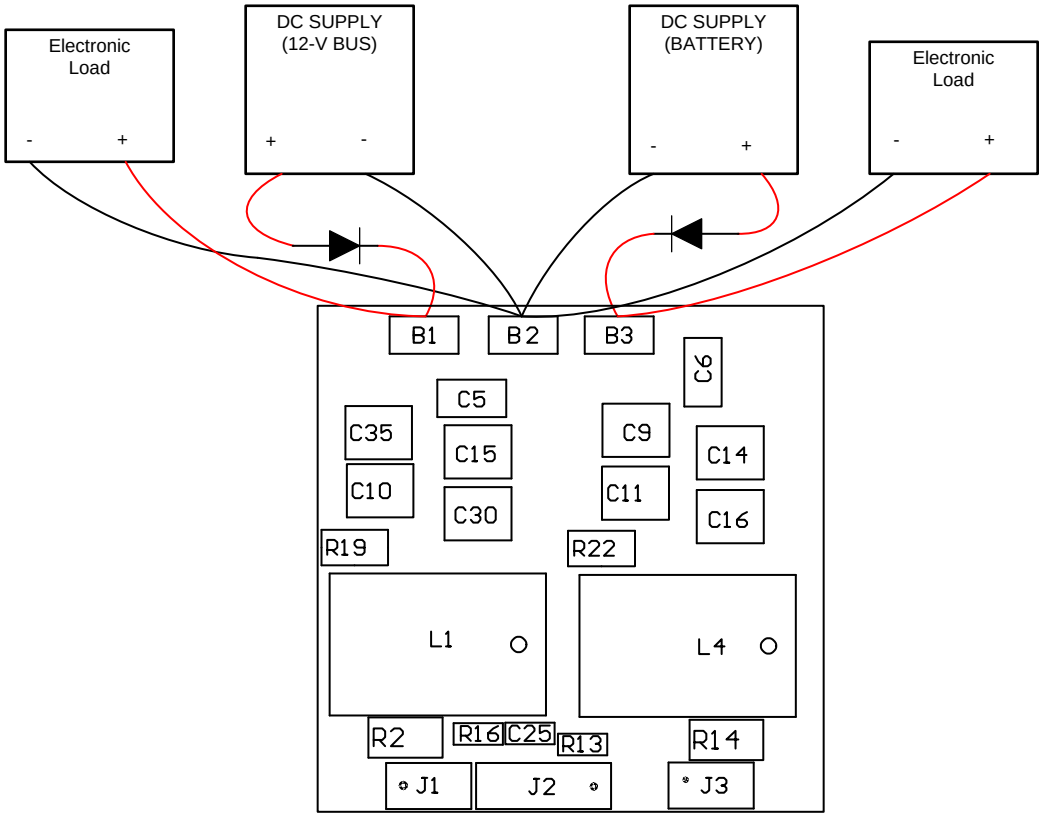

Figure 11. Recommended Test Setup for Testing TIDA-00705

1. Connect one set of wires to the battery input and the GND terminal pads on the TIDA-00705 board. Similarly connect another set between the bus input and the GND terminal pads of the TIDA-00705 board.
2. Connect a diode in series (anode to the DC supply +ve and cathode to the battery input terminal) with the DC supply and reconnect it to the TIDA-00705 board battery input terminal. Set it between 13.8 and16.4 V. Keep the supply turned off.
3. Connect another DC supply with a diode in series (anode to the DC supply +ve and cathode to the bus input terminal) to the bus input terminal and set it to 12.7 V (0.7 V extra to compensate for diode drop). Keep the supply turned off.
4. Connect an electronic load in constant resistance mode to the battery input terminal. The electronic load will act as the battery load.
5. Set the electronic load to take 100 mA at 16.4 V.
6. Connect an electronic load in constant resistance to the bus input terminal. The electronic load will act as the 12-V bus load.
7. Set the electronic load to take 10 A at 12 V.
8. Connect a DC fan and position it so the heatsink on the TIDA-00705 board receives between 200 and 500 LFM. 200 LFM is sufficient when operating up to 420 W. It is recommended to use 500 LFM if battery voltage is high and the applied load is closer to 500 W.
9. Turn on the DC supply connected to the battery input side.
10. Turn on the DC supply connected to the bus input side.
11. The TIDA-00705 will operate in the battery charging mode and maintain the battery terminal connector voltage at 16.4 V.
12. Slowly increase the load current in the electronic load connected to the battery terminal connector.
13. Once the point the load current (battery charging current) reaches around 6 A, the system will operate in constant voltage (CV) region and the battery terminal connector voltage will be maintained at 16.4 V.
14. As the battery charging current crosses 6 A, the system will begin to operate in constant current (CC) region and the batter terminal connector voltage will start reducing.
15. Reduce the battery charging current to less than 1 A.
16. Turn off the DC supply connected to the 12-V bus terminal.
17. The TIDA-00705 will switch over to working as a backup power supply. This transition will occur as soon as the voltage at the 12-V bus terminal drops below 11.65 V. This transition can be captured with a current probe capturing the bus current.
18. The TIDA-00705 will supply power to the electronic load while regulating the bus voltage to 12 V.
19. Now increase the load gradually up to 500 W to test the backup supply mode.
20. The necessary functional performance characteristics can be measured now.
21. Turn off the DC supply and disconnect the DC supply from the board.

4.2 Results

The test results are divided into multiple sections that cover the stead state performance, efficiency data, functional waveforms, and thermal performance.

4.2.1 Performance Data

4.2.1.1 Efficiency, Load and Line Regulation in Buck Mode

This test is conducted when the system is operating as a backup power supply. The system transfers power from the battery pack to the 12-V bus. The steady state performance and efficiency results are captured for different battery voltage and load conditions.

Table 3. Test Results in Buck Mode at 16.4-V Battery Voltage

VBAT (V)	IBAT (A)	VBUS (V)	IBUS (A)	PIN (W)	POUT (W)	EFF	% REG
16.4	0.785	12.10	0.864	12.874	10.46155	81.26	0.83
16.4	3.183	12.04	4.118	52.2012	49.58252	94.98	0.33
16.4	6.390	12.04	8.459	104.796	101.849	97.19	0.33
16.4	9.518	12.02	12.679	156.0952	152.4129	97.64	0.17
16.4	12.541	12.01	16.672	205.6724	200.2377	97.36	0.08
16.4	16.2	12.01	21.470	265.680	257.8547	97.05	0.08
16.4	18.662	11.98	24.729	306.0568	296.2575	96.80	-0.17
16.4	22.512	77.97	29.806	369.1968	356.7894	96.64	-0.25
16.4	25.986	11.95	34.405	426.1704	411.145	96.47	-0.42
16.4	28.8	11.94	38.130	472.320	455.277	96.39	-0.50
16.4	32.44	11.93	42.740	532.016	509.980	95.86	-0.58

Table 4. Test Results in Buck Mode at 15-V Battery Voltage

VBAT (V)	IBAT (A)	VBUS (V)	IBUS (A)	PIN (W)	POUT (W)	EFF	% REG
15	0.778	12.08	0.86	11.67	10.39028	89.03	0.67
15	3.365	12.05	4.059	50.475	48.9212	96.92	0.42
15	6.828	12.04	8.333	102.42	100.3412	97.97	0.33
15	10.351	12.02	12.608	155.265	151.3023	97.45	0.17
15	13.992	12	16.963	209.88	203.8974	97.15	0
15	17.631	12	21.395	264.465	256.74	97.08	0
15	20.223	11.98	24.576	303.345	294.4205	97.06	-0.17
15	24.447	11.96	29.72	366.705	355.4528	96.93	-0.33
15	28.225	11.95	34.329	423.375	410.2369	96.9	-0.42
15	31.553	11.93	38.362	473.295	457.6684	96.7	-0.58
15	35.117	11.92	42.768	526.755	509.796	96.78	-0.67

Table 5. Test Results in Buck Mode at 14-V Battery Voltage

VBAT (V)	IBAT (A)	VBUS (V)	IBUS (A)	PIN (W)	POUT (W)	EFF	% REG
14	0.806	12.08	0.839	11.284	10.14561	89.91	0.67
14	3.701	12.06	4.184	51.814	50.45906	97.38	0.5
14	7.392	12.05	8.384	103.488	101.0353	97.63	0.42
14	11.213	12.04	12.742	156.982	153.4206	97.73	0.33
14	15.06	12.03	17.112	210.84	205.8634	97.64	0.25
14	18.942	12.01	21.556	265.188	258.8881	97.62	0.08
14	21.409	12	24.359	299.726	292.3194	97.53	0
14	25.45	11.98	28.933	356.3	347.4891	97.53	-0.17
14	30.63	11.98	34.85	428.82	417.5091	97.36	-0.17
14	34.85	11.97	39.609	487.9	474.1255	97.18	-0.25
14	37.48	11.96	42.6493	524.72	510.0858	97.21	-0.33

4.2.1.2 Load Carrying Capability Buck Mode

The result presented in this section presents the *short time* and *continuous* load carrying ability of the TIDA-00705 at various FAN speeds.

The short time load carrying capability is measured as the output power at which the maximum temperature on the board reaches 90°C at two minutes under room temperature conditions.

Table 6. Short Time Load Carrying Capability at Different Battery Voltages and Fan Speeds

FAN SPEED (LFM)	OUTPUT LOAD (W) AT 16.4 V	OUTPUT LOAD (W) AT 14 V
0	300	340
200	425	475
500	500	500

The continuous load carrying capability is measured as the maximum output power at which the board temperature stabilizes with the maximum temperature being less than 90°C after running for more than 30 minutes at room temperature.

Table 7. Continuous Load Carrying Capability at Different Battery Voltages and Fan Speeds

FAN SPEED (LFM)	OUTPUT LOAD (W) AT 16.4 V	OUTPUT LOAD (W) AT 14 V
0	190	230
200	310	410
500	420	500

4.2.1.3 Efficiency in Boost Mode

The steady state performance in the boost mode is shown in the table below. In the boost mode, the TIDA-00705 charges the battery from the 12-V bus. The efficiency results obtained are presented in the table below.

Table 8. Power and Efficiency Data Obtained While Operating in Boost Mode

VBAT (V)	IBAT (A)	VBUS (V)	IBUS (A)	PIN	POUT	EFF
16.4	0.619493	12	1.1438	13.7256	10.15968	74.02
16.4	1.532827	12	2.383967	28.6076	25.13836	87.87
16.4	3.013814	12	4.397317	52.7678	49.42655	93.67
16.4	4.579468	12	6.555908	78.6709	75.10328	95.47
16.4	6.050854	12	8.57026	102.8431	99.234	96.49

4.2.2 Performance Curves

4.2.2.1 Buck Mode Efficiency Curves With Load and Line Variation

The buck mode efficiency performance variation curves as a function of load and battery voltage variation for a fixed fan speed of 200 LFM is shown in Figure 12.

This data is plotted for three different battery voltage conditions with the worst case performance obtained at maximum battery voltage of 16.4 V.

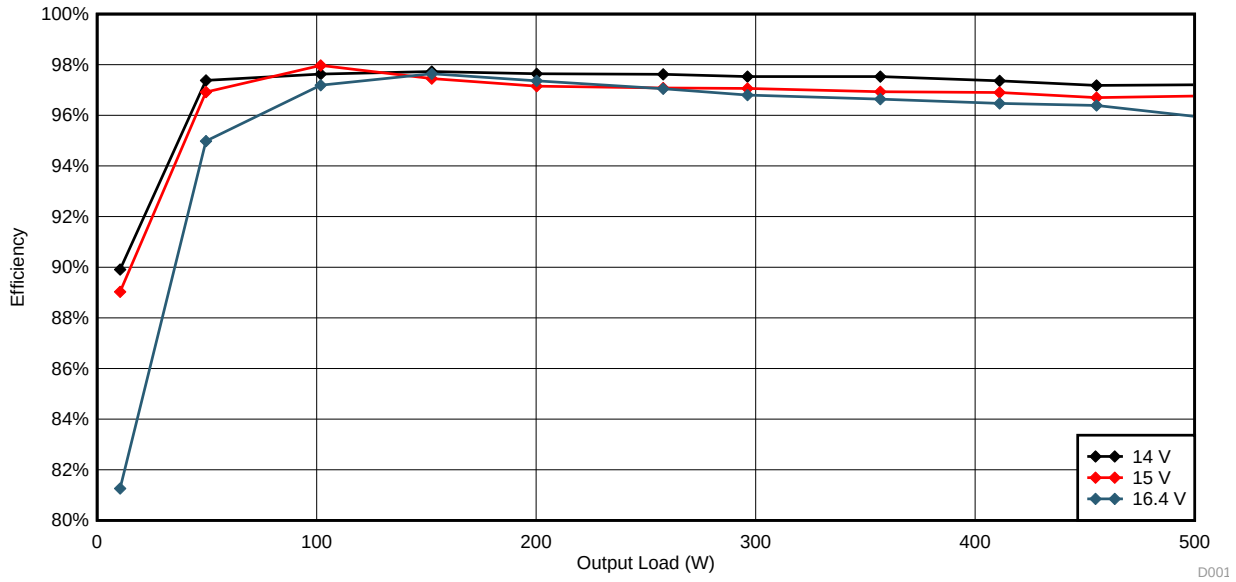

Figure 12. Efficiency Versus Output Load Curves in Backup Supply Mode at Various Input Voltage

4.2.2.2 Buck Mode Voltage Regulation Curve Versus Battery Voltage and Load Variations

The buck mode output voltage regulation curves is shown in Figure 13.

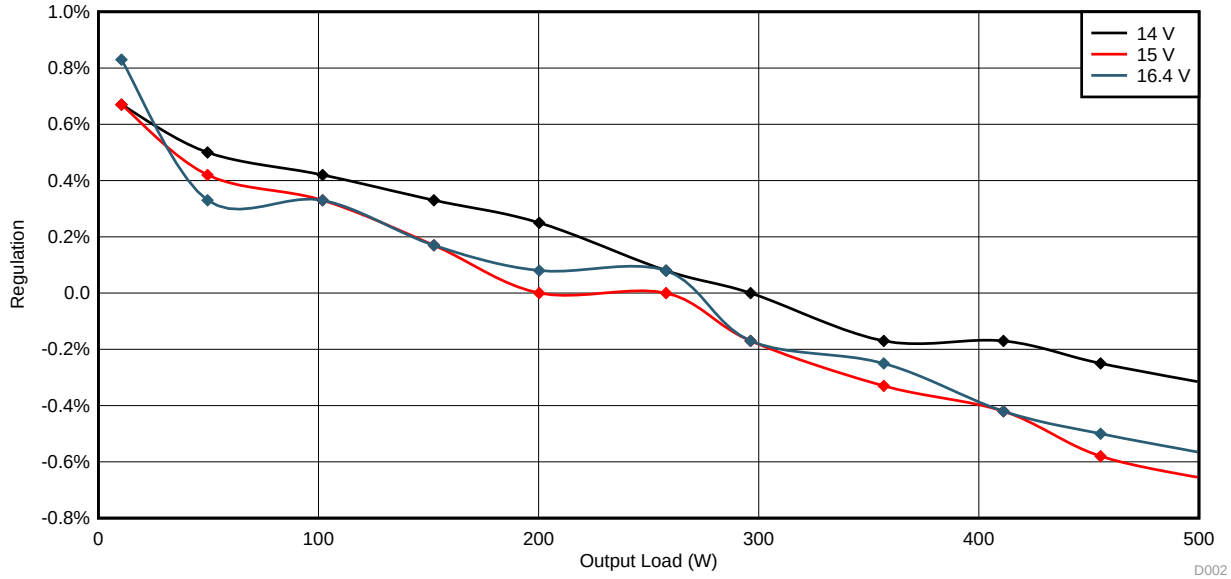

Figure 13. Output Voltage Regulation Versus Output Load Curves in Backup Supply Mode at Various Input Voltage

4.2.2.3 Buck Mode Short Time Load Carrying Capability Versus Fan speed and Battery Voltage

The maximum load that can be delivered for two minutes in buck mode for various battery voltages and fan speeds is plotted in Figure 14.

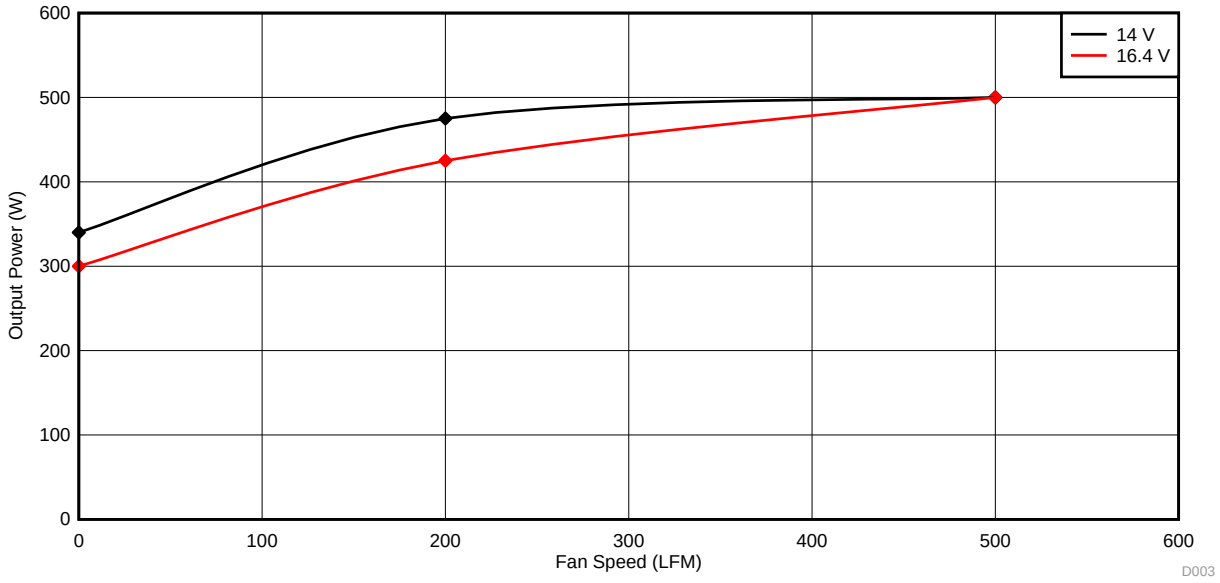

Figure 14. Short Time Output Power Capability Versus Air Flow at Various Input Voltage

4.2.2.4 Buck Mode Continuous Load Carrying Capability Versus Fan speed and Battery Voltage

The maximum load that the TIDA-00705 can deliver continuously in buck mode for various battery voltages and fan speeds is plotted in Figure 15.

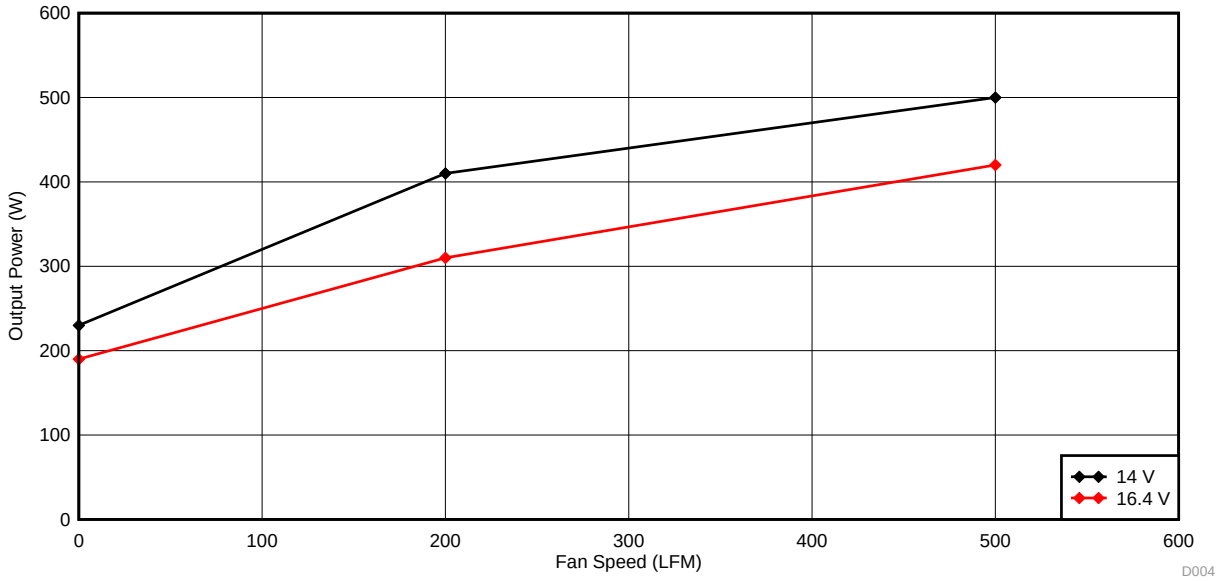

Figure 15. Continuous Output Power Capability Versus Air Flow at Various Input Voltage

4.2.2.5 Boost Mode Efficiency Curve

The efficiency results obtained in the boost mode is shown in Figure 16.

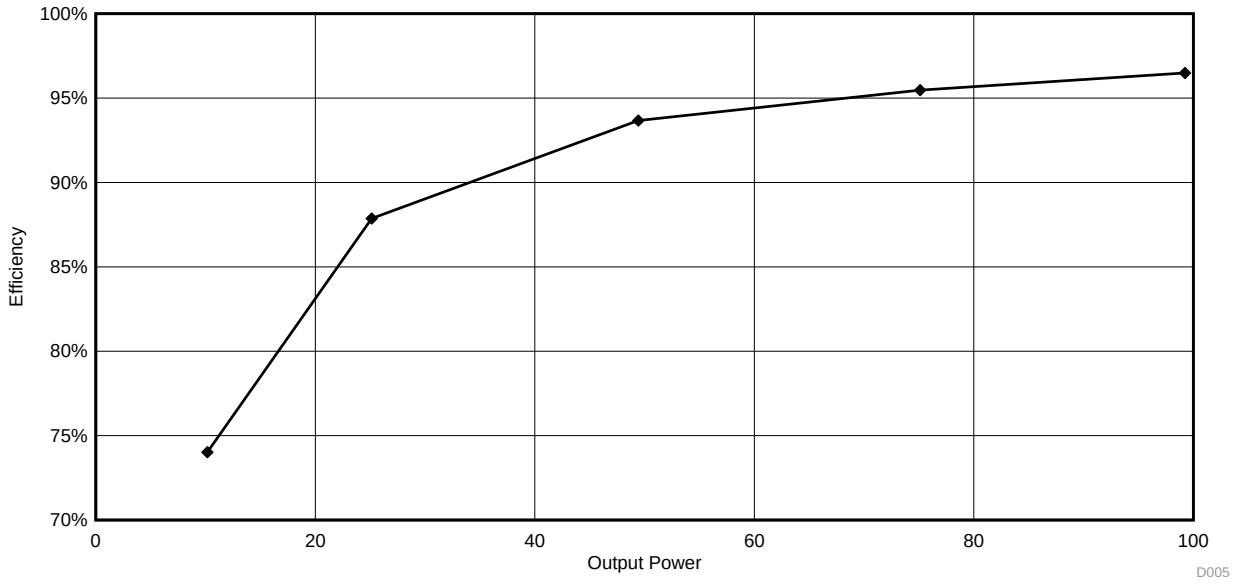

Figure 16. Efficiency Versus Output Power in Battery Charging Mode at 12-V Bus and 16.4-V Battery

4.2.3 Functional Waveforms

4.2.3.1 Two Phase Complementary PWM Signal

The two phase interleaved complementary PWM signal generated by the UCD3138 is shown in Figure 17

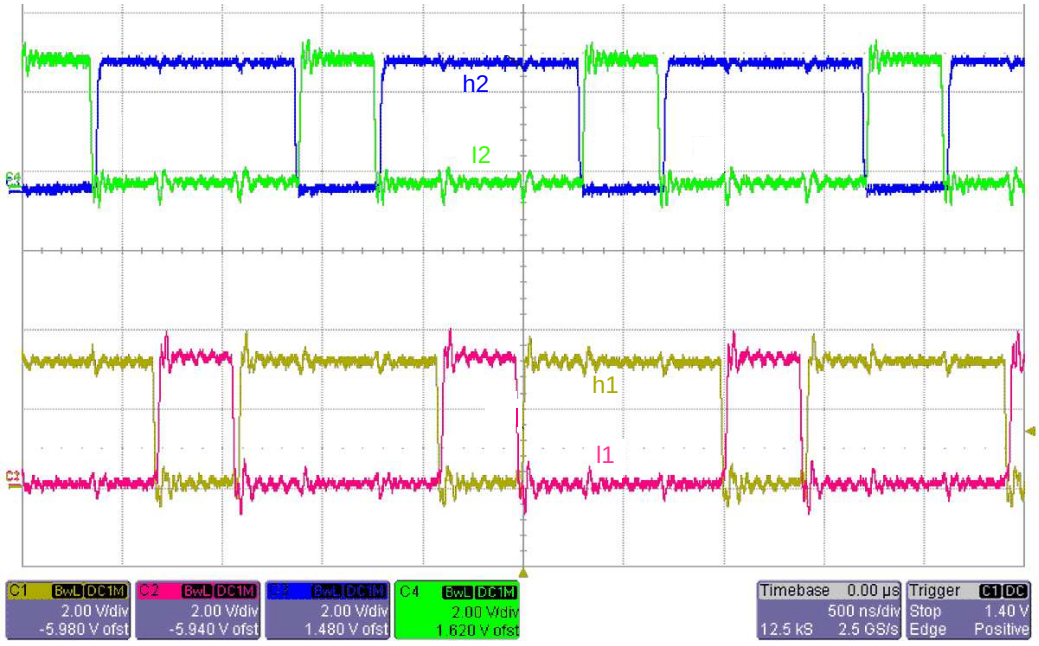

Figure 17. Complimentary PWM Outputs From UCD3138

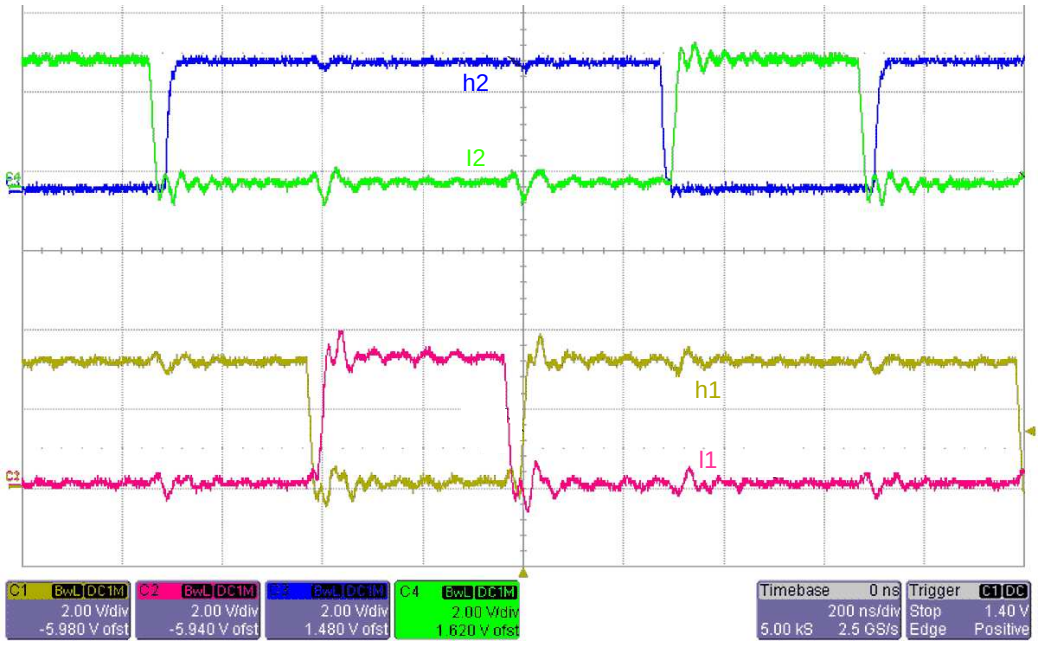

Figure 18. Complimentary PWM Outputs From UCD3138 (Zoomed in to Show the Dead Time)

4.2.3.2 Switching Node Waveforms

The switching node waveforms observed under full load at 16.4-V battery voltage input is shown in Figure 19. Figure 19 also shows the inductor current, switching node waveform, and the low-side gate voltage for phase one.

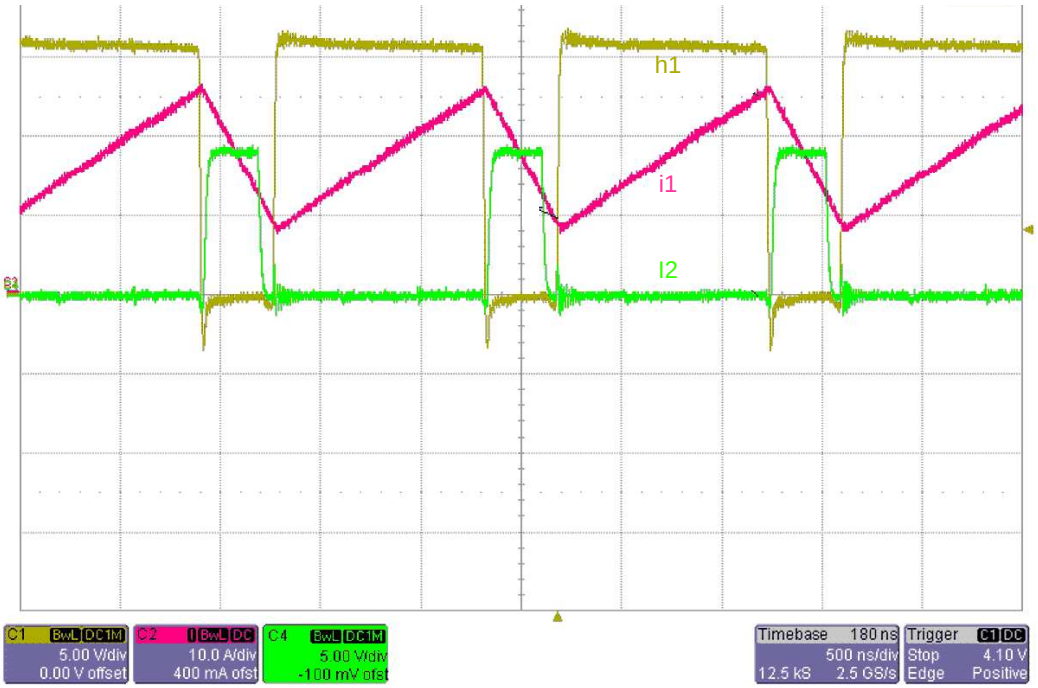

Figure 19. Switching Node Waveform Showing the Switching Node Voltage, Inductor Current, and the Low-Side MOSFET Gate Voltage

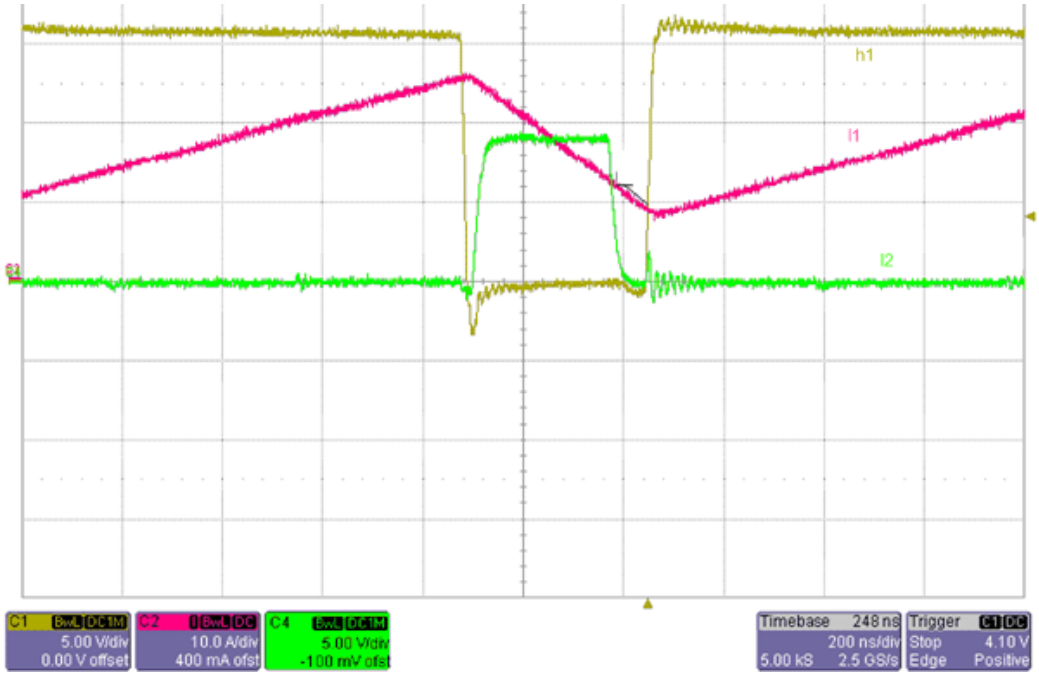

Figure 20. Switching Node Waveform Showing the Switching Node Voltage, Inductor Current, and the Low-Side MOSFET Gate Voltage (Zoomed in)

Figure 21 shows the actual positive and negative spike on the switching node. This image is captured without a snubber attached to the switching node.

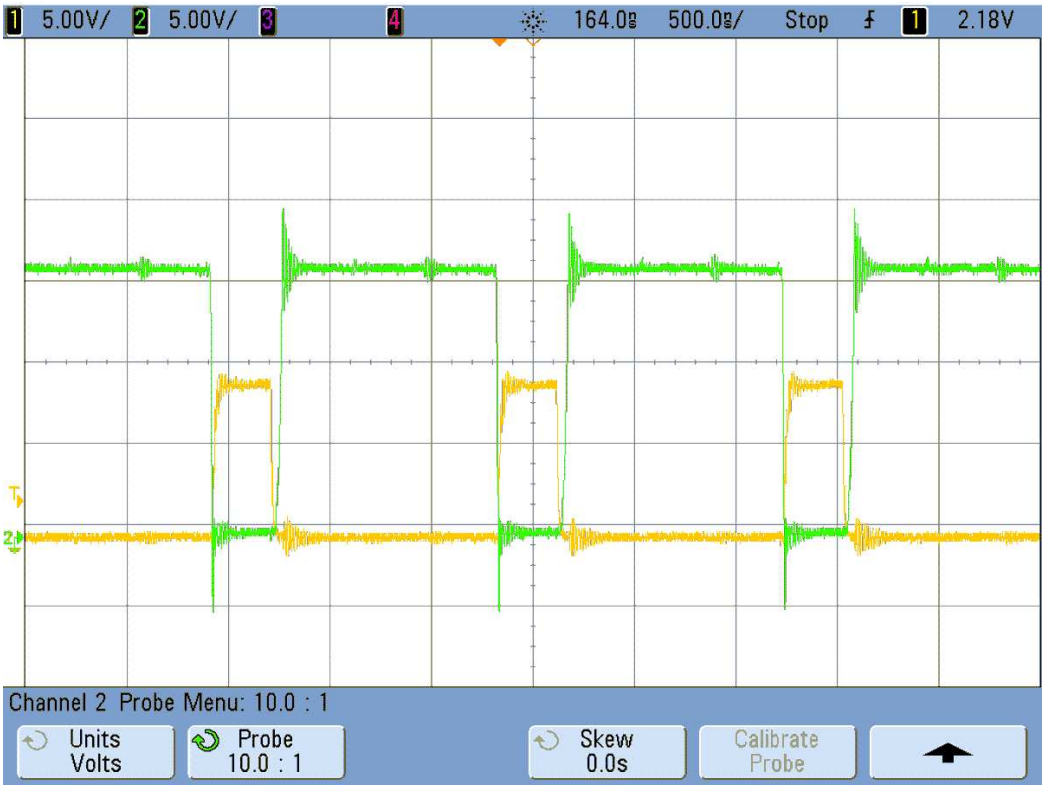

Figure 21. Switching Node Waveform Showing the Voltage Spikes at High-Side MOSFET Turn and Turn Off

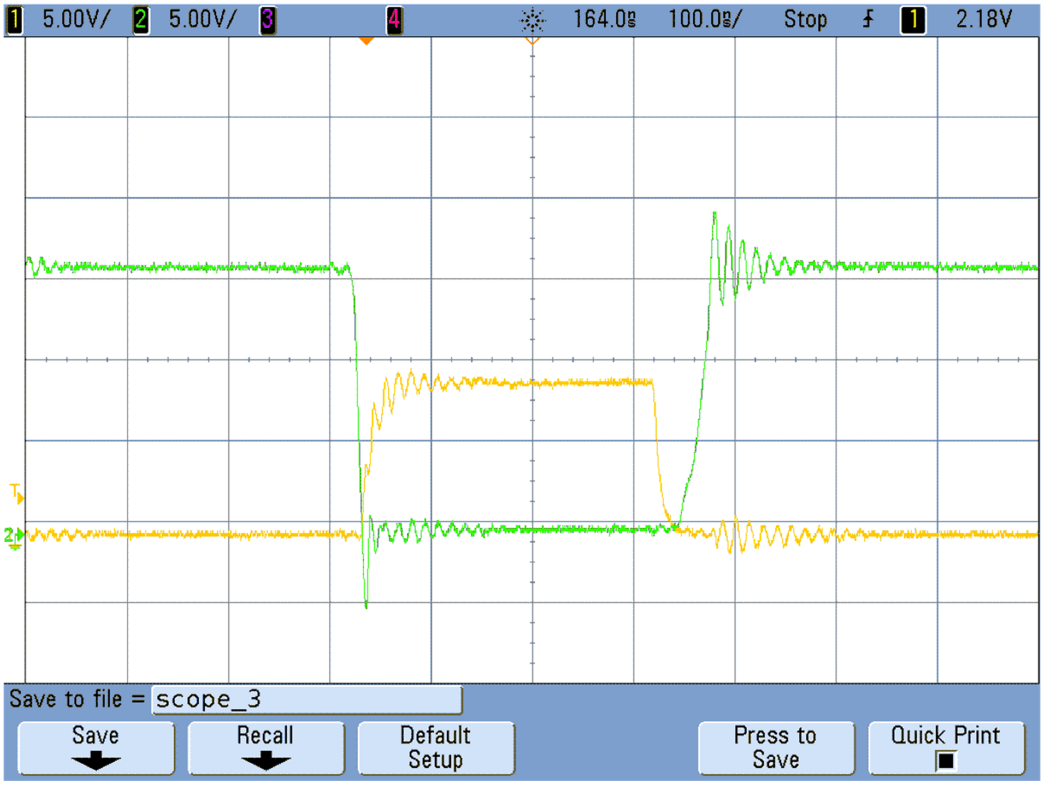

Figure 22. Switching Node Waveform Showing the Voltage Spikes at High-Side MOSFET Turn and Turn Off (Zoomed in)

4.2.3.3 Inductor Ripple Current

The two phase interleaved ripple current is shown in Figure 23.

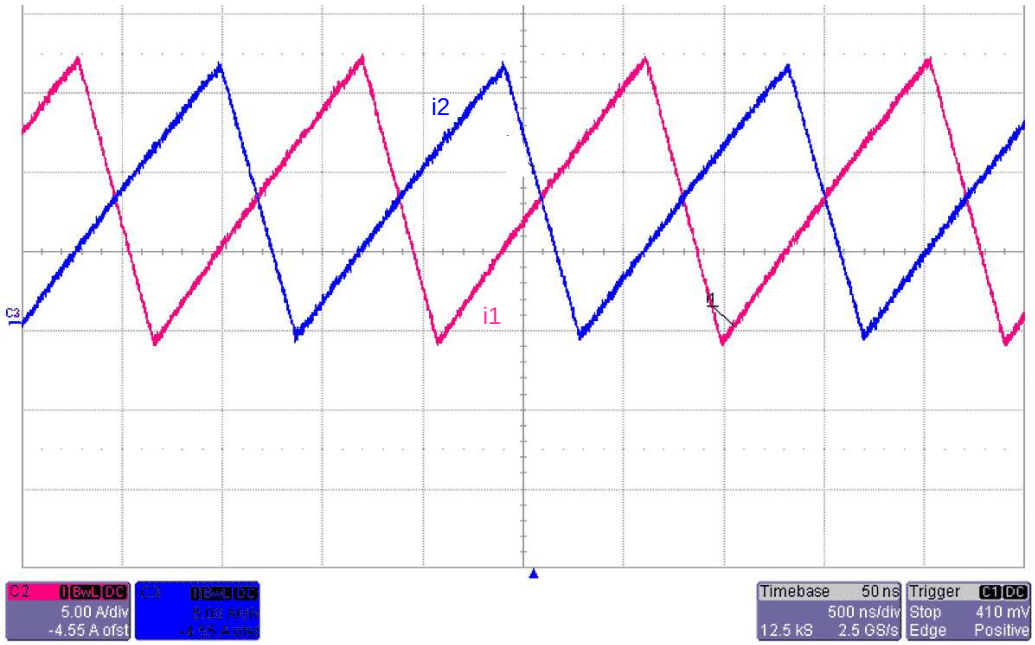

Figure 23. Two Phase Inductor Ripple Current

4.2.3.4 Input and Output Ripple in Buck Mode

The AC ripple voltage observed on the battery input terminals (input) and bus terminal (output) is shown in Figure 24.

The ripple is about 200-mV pk-pk on the battery input terminal and about 70-mV peak-to-peak on the bus terminal. The observed ripple at the battery input terminal is due to the limited amount of capacitance available on the TIDA-00705 board. In the actual system where bulk capacitors will be connected to this board, this ripple will be lower.

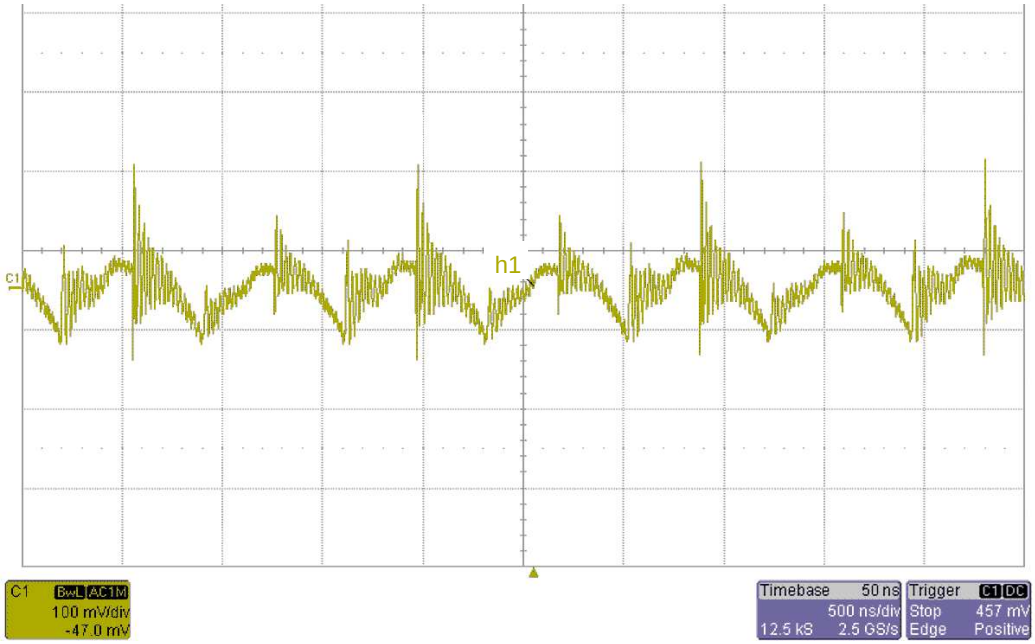

Figure 24. Input Voltage Ripple at the Battery Terminal

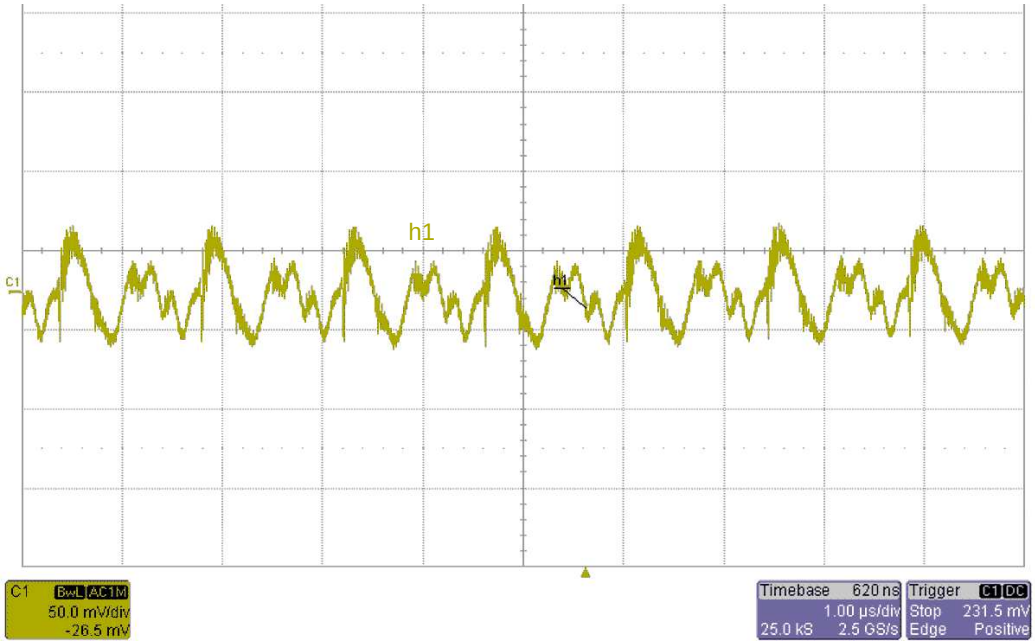

Figure 25. Output Voltage Ripple Measured at the Bus Terminal

4.2.3.5 Boost to Buck Mode Change Waveform

The boost (battery charging) to buck (backup mode) transition is triggered as the bus input voltage drops below 11.65 V. The TIDA-00705 will transition from working as a synchronous boost converter to a synchronous buck converter. This transition can be observed in Figure 26.

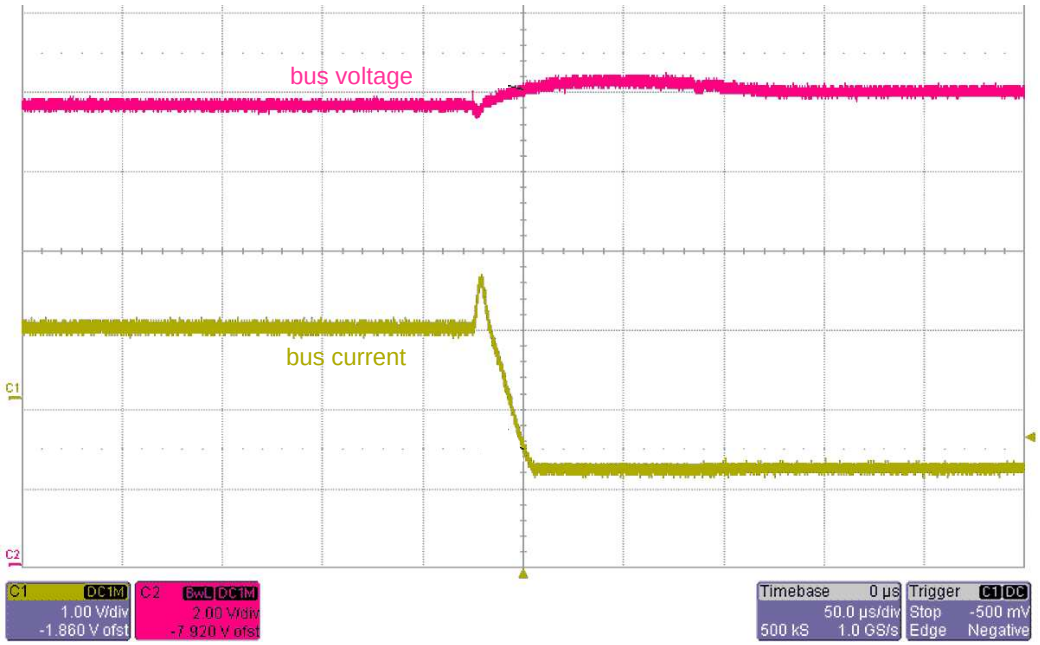

Figure 26. Mode Change From Battery Charging to Backup Supply

4.2.4 Thermal Images

In this section, two sets of thermal images are provided. Figure 27 is captured after loading the board with 425 W at 16.4-V battery input for a period of two minutes (short time test) under room temperature with 200 LFM air flow measured at the board.

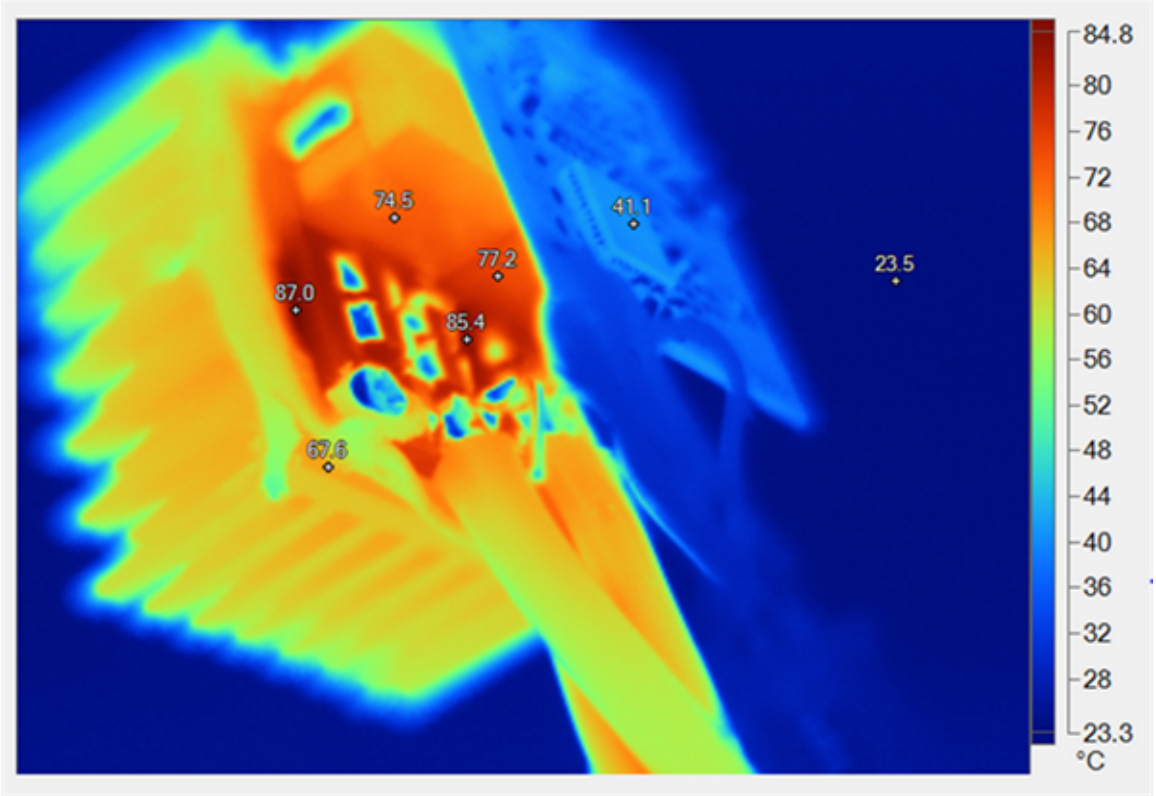

Figure 27. Thermal Image Captured After Two Minutes When Delivering 425 W at 16.4-V Battery

Table 9. Temperature of Major Components After 30 Minutes at 310 W

MAJOR COMPONENT	TEMPERATURE (°C)
Main MOSFET (phase one)	87.0
Main MOSFET (phase two)	85.4
Inductor (phase one)	74.5
Inductor (phase two)	77.2
Heat sink	67.6
UCD3138 controller	41.1

The second set of thermal images are captured with the board after loading the board with 310 W at 16.4-V battery input for a period greater than 30 minutes (continuous load test) under room temperature with 200 LFM air flow measured at the board.

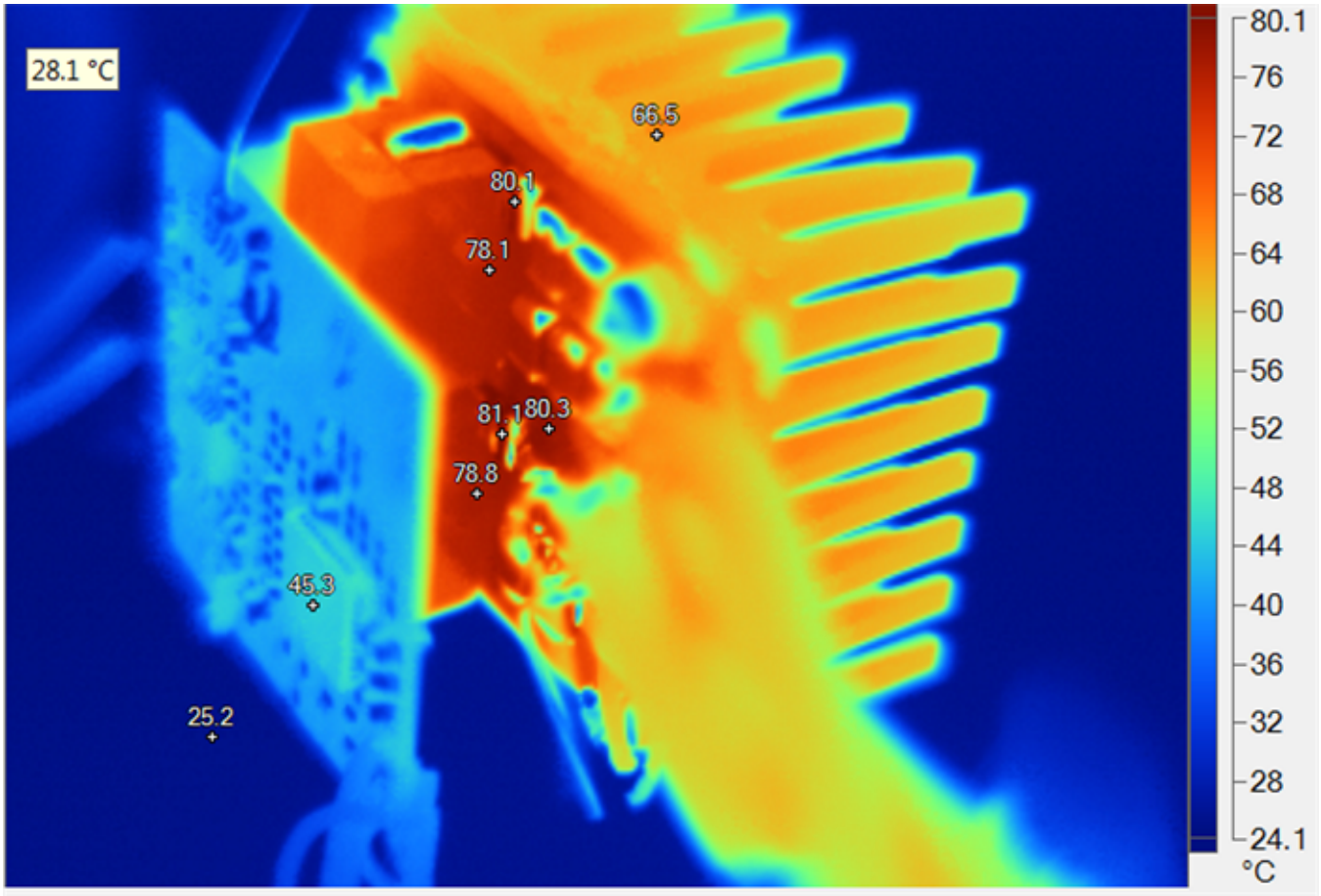

Figure 28. Thermal Image Captured After 30 Minutes When Delivering 310 W at 16.4-V Battery

Table 10. Temperature of Major Components After 30 Minutes at 310 W

MAJOR COMPONENT	TEMPERATURE (°C)
Main MOSFET (phase two)	80.3
Inductor (phase one)	78.1
Inductor (phase two)	78.8
Current sense resistor (phase one)	81.1
Current sense resistor (phase two)	80.1
Heat sink	66.5
UCD3138 controller	45.3

5 Design Files

5.1 Schematics

To download the schematics, see the design files at TIDA-00705.

5.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00705.

5.3 PCB Layout Recommendations

The TIDA-00705 contains two PCBs. The power stage PCB and the controller PCB. Due to the ultra-compact nature of this design, the layouts of the PCBs are very important.

As with all switching power supplies, attention to detail in the layout save time in troubleshooting.

- The main switching loop comprising of MOSFET Q1, Q2 and L1 along with the input and output ceramic caps must be minimized to the best possible extent. One approach is to reduce the traces to an absolute minimum. This reduction can be done by making the layout in such a way that the inductor is directly mounted on the top side over the MOSFET Q1 source and MOSFET Q2 drain (shown in the Figure 29).

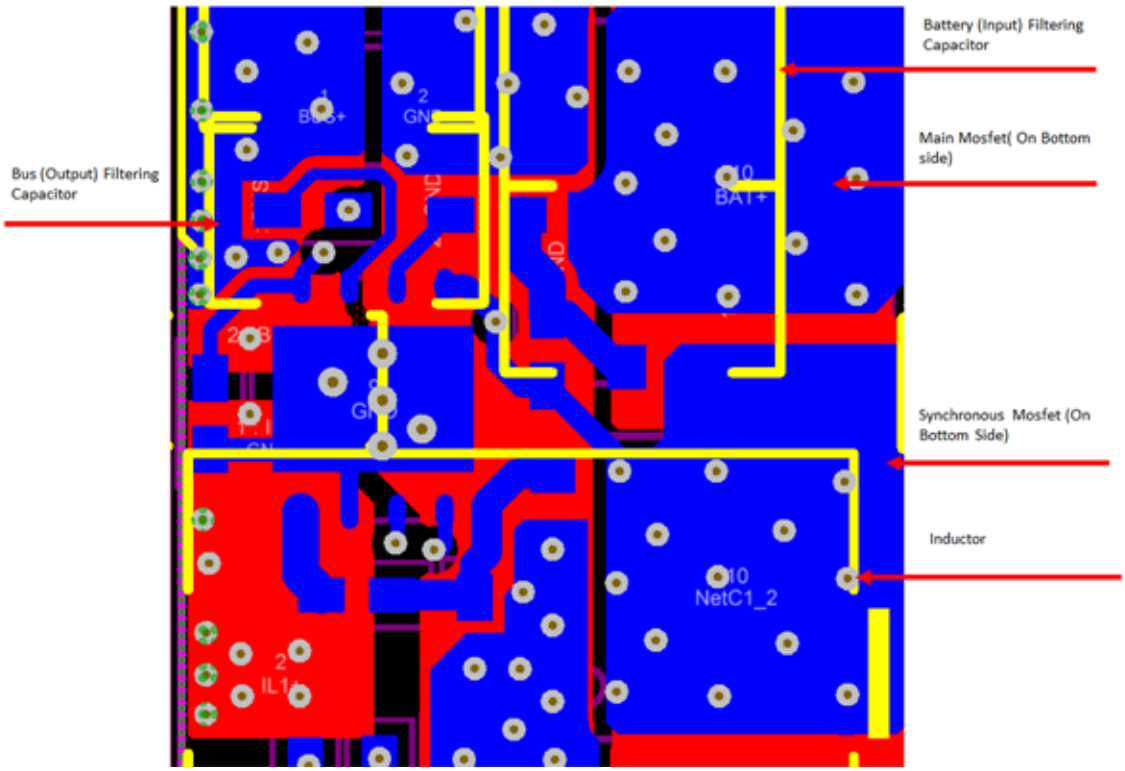

Figure 29. Half-Bridge Switching Loop Layout Highlighting Major Components

Figure 30 shows the placement of the major components on the TIDA-00705 power board in the 3D view.

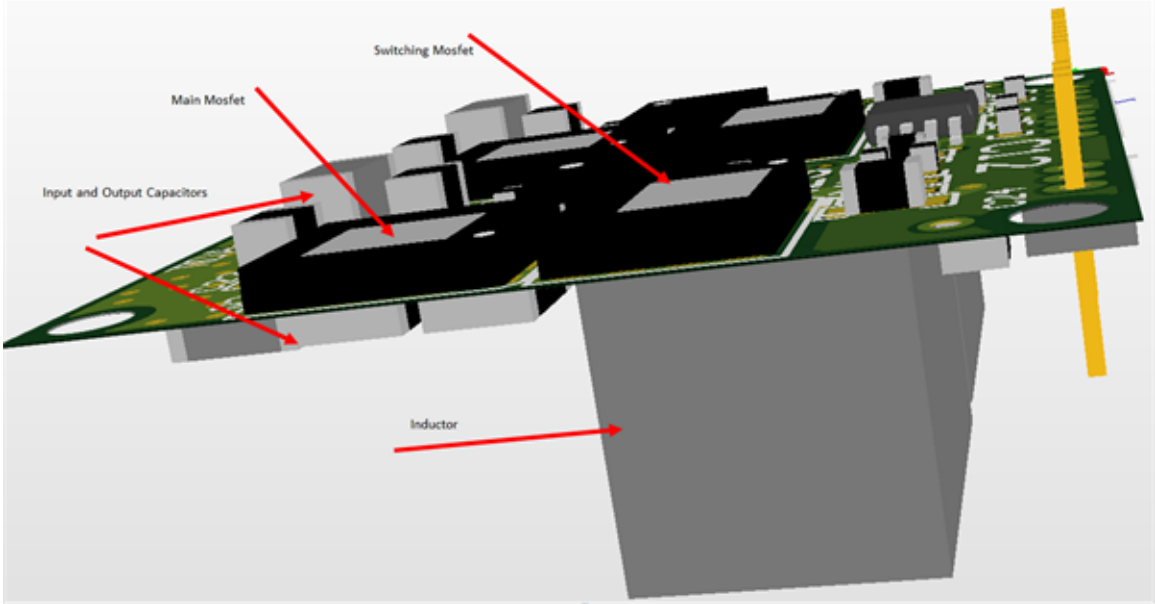

Figure 30. 3D Image Showing Placement of Components on TIDA-00705 Power Board

- Care must be taken to reduce the common source inductance as much as possible by reducing the distance between the MOSFET Q1 source and MOSFET Q2 drain. A high common source inductance reduces the switching speed and increases the switching losses on the MOSFET.

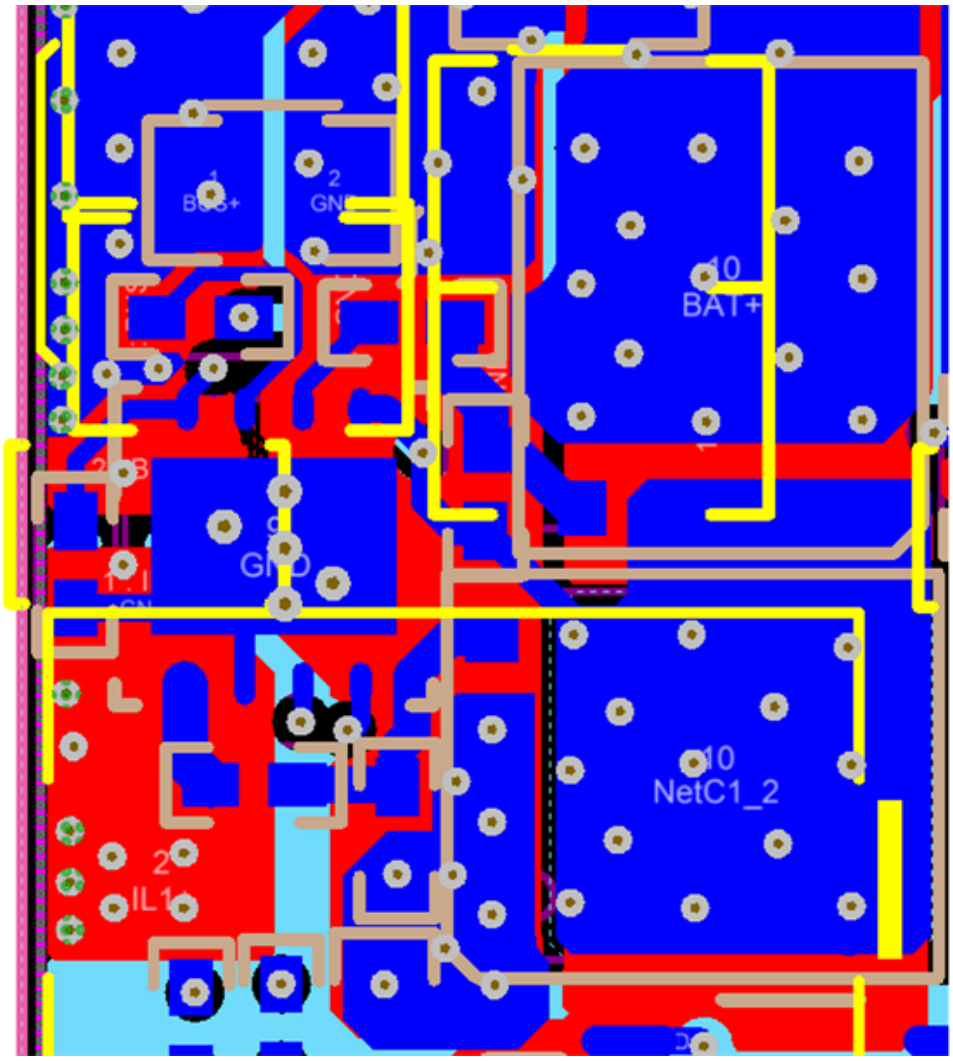

Figure 31. Switching Node Trace Connection Between Main FET and Synchronous FET

- The layout for both the half bridge phases needs to be symmetrical to ensure proper current sharing between the phases.
- Sufficient thermal via need to be provided on the MOSFET drain pads to remove the heat from the MOSFET.
- Due to the constrained dimension of the board, the copper areas on the PCB are not effective enough to transfer and remove heat from the MOSFET bottom pads. A heatsink attached to the MOSFET top pad (DualCool FETs) provides the major thermal conduction path.
- Care should be taken so no component is over 0.9 mm on the bottom side of the power stage board to provide a good thermal connection between the heat sink and the MOSFET top pads.
- Placement of the half bridge driver UCC27211A is critical to reduce the switching loss on the MOSFETs and also minimize the switching loop.
- The trace connecting the gate driver outputs and the MOSFET gates needs to be very short and thick enough to reduce the trace inductance.

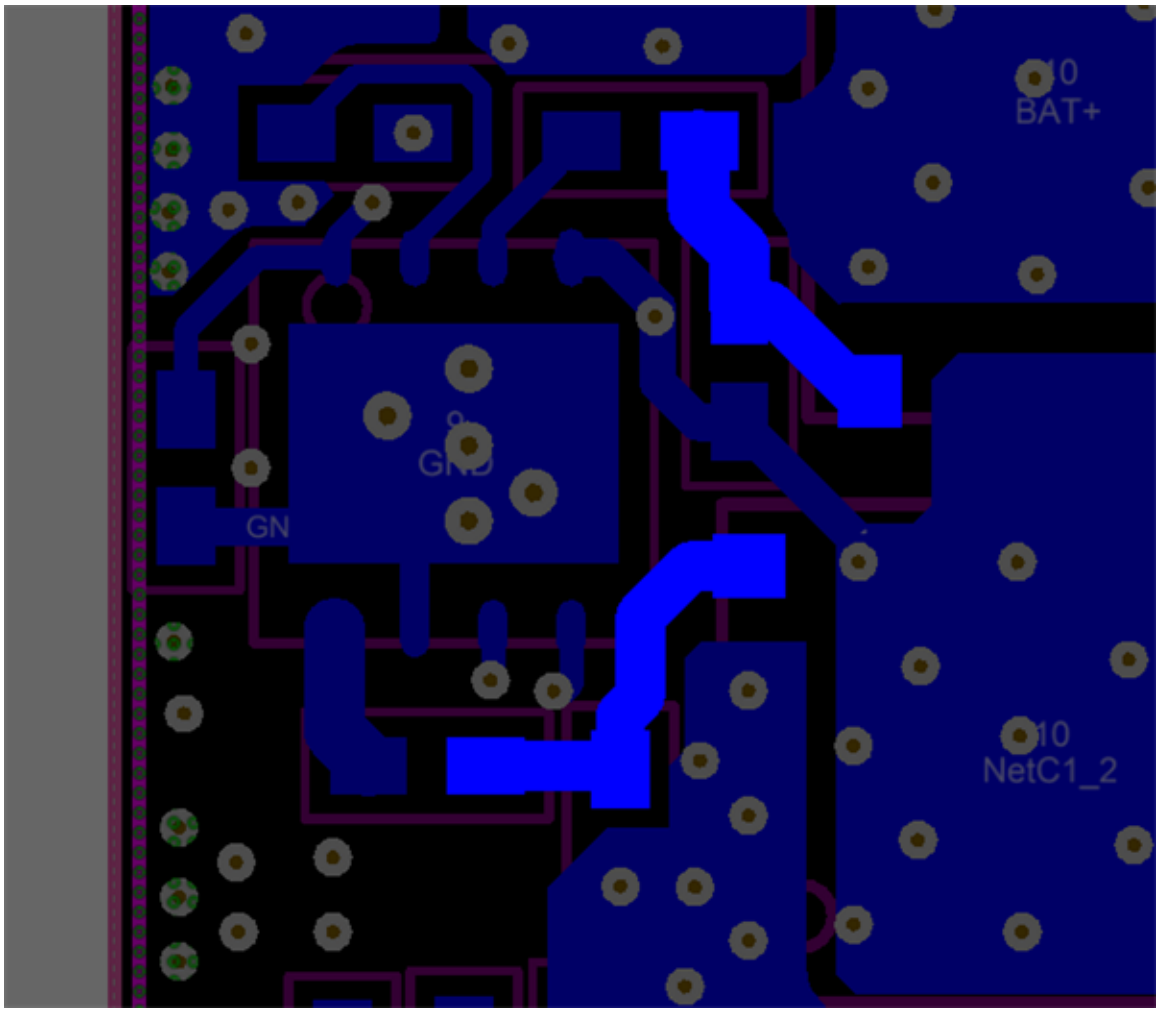

Figure 32. Connection Between MOSFET Gate and Gate Driver Highlighted

- The trace length between the ground of the gate driver and the synchronous FET must be minimized.

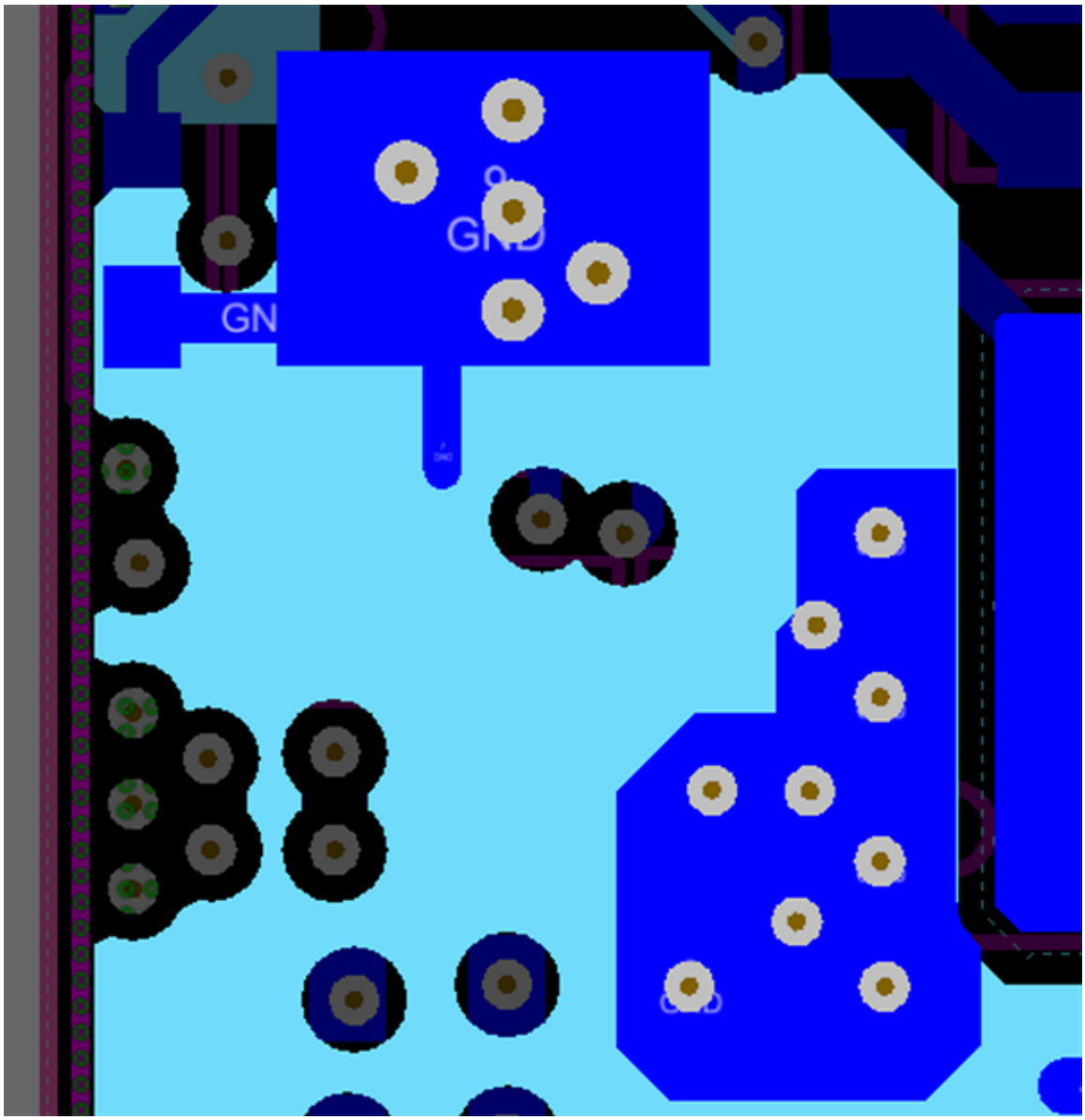

Figure 33. Connection Between The Gate Driver Ground and Synchronous MOSFET Source

- Place sufficient copper area on the PCB below the driver IC to remove the heat from the gate driver.
- The first stage amplifier for the current sense is placed on the power stage board. The traces connecting the current sense resistor and the amplifier should be taken in a differential pair.
- Because the trace between the current sense resistor and amplifier pass below the switching node, care should be taken to minimize the noise coupling in these traces.

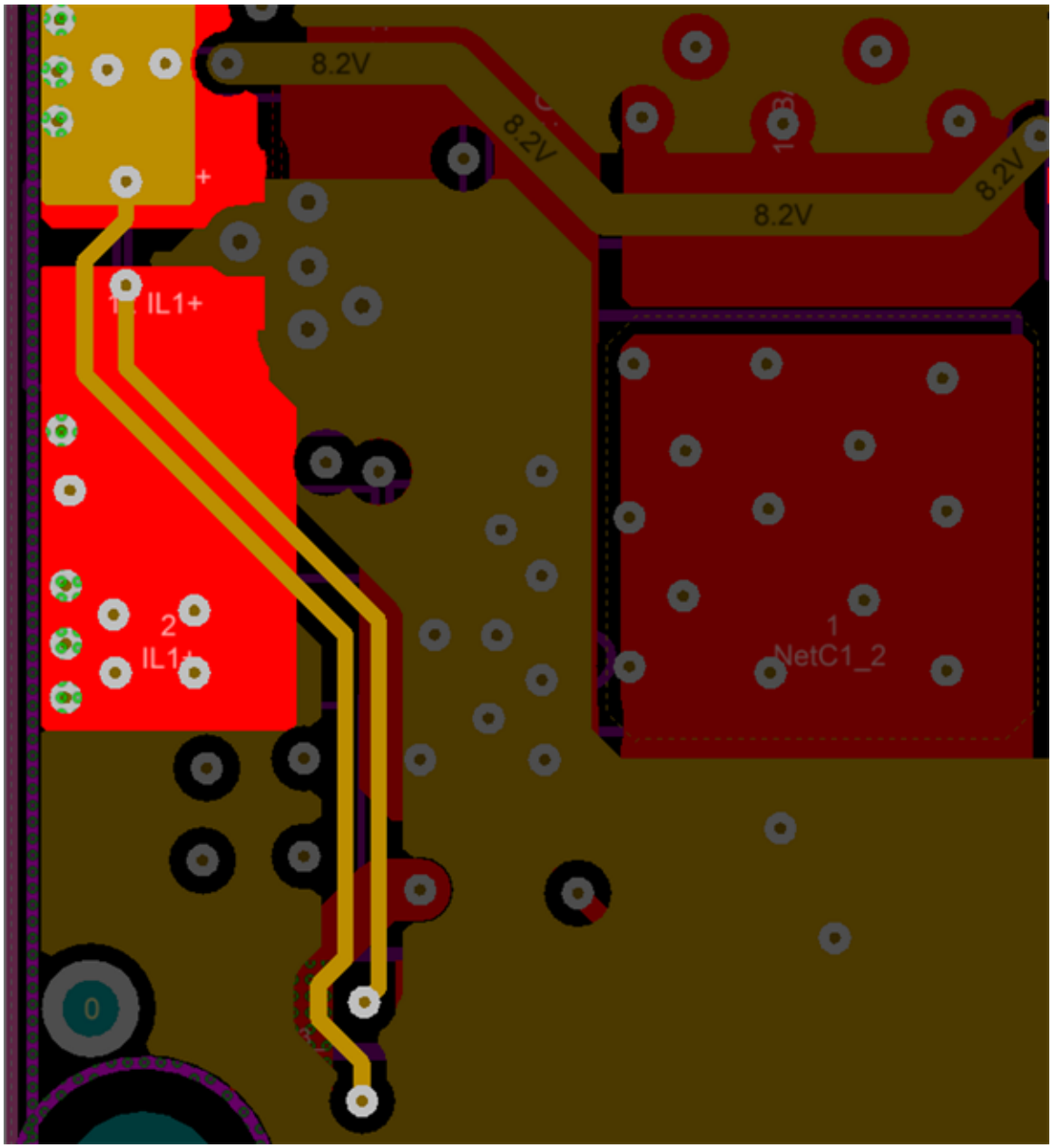

Figure 34. Current Sense Trace From Current Sense Resistor Highlighted

- The ground plane below the amplifier should be a quiet plane and it has to be connected to the noisy ground plane at only two points close to the gate drivers.
- The control board ground is connected to the quiet ground plane.
- The decoupling caps for the driver and the opamp must be placed close to them.

5.3.1 Controller Board Specific Guidelines

The following are key guidelines to route controller components and signal circuits:

- The UCD3138A is a highly integrated controller with a large number of mixed signals. To reduce noise coupling and prevent chip malfunction:
  1. Group each pin.
  2. Select good components.

3. Have an appropriate connection to each pin.
4. Make good placements on the PCB.

- To avoid chip malfunction:
  1. Group all digital circuitry and analog circuitry.
  2. Place digital circuitry close to each other.
  3. Place analog circuitry close to each other.
  4. Make trace connections among them.
- Locate all controller support components at specific signal pins close to their connection pin. Connect the other end of the component to the AGND or DGND, respectively, with shortest trace length.
- Find detailed recommendations of each pin connection and its associated component in the *UCD3138A Highly-Integrated Digital Controller for Isolated Power* data sheet.
- The second stage of the current sense amplifier is placed on the controller board. Place the opamp circuit close to the board connector so as to minimize the trace lengths.
- The bottom layer of the board should have a solid ground plane which can act as a shield. Use another inner PCB layer for the system GND plane.

5.3.2 Power Stage Board Specific Guidelines

Because the power stage switching frequency per phase is very high at 700 KHz and the MOSFET switching currents can be greater than 40 A, attention must be taken while designing the layout of the power stage to handle switching as well as thermal constraints. Few of the points are highlighted in this section.

5.3.3 Layout Prints

To download the layer plots, see the design files at TIDA-00705.

5.4 Altium Project

To download the Altium project files, see the design files at TIDA-00705.

5.5 Gerber Files

To download the Gerber files, see the design files at TIDA-00705.

5.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-00705.

6 Software Files

To download the software files, see the design files at TIDA-00705.

7 Related Documentation

1. Texas Instruments, *DualCool N-Channel NexFET Power MOSFETs*, CSD16325Q5C Data Sheet (SLPS237).
2. Texas Instruments, *UCC27211A 120-V Boot, 4-A Peak, High-Frequency High-Side and Low-Side Driver*, UCC27211A Data Sheet (SLUSBL4).
3. Texas Instruments, *LM4041-N-xx Precision Micropower Shunt Voltage Reference*, LM4041-N and LM4041-N0Q1 Data Sheet (SNOS641).
4. Texas Instruments, *OPAx192 36-V, Precision, Rail-to-Rail Input/Output, Low Offset Voltage, Low Input Bias Current Op Amp with e-trim*, OPA192, OPA2192, and OPA4192 Data Sheet (SBOS620).
5. Texas Instruments, *TPS62125 3-V to 17-V, 300-mA Step-Down Converter With Adjustable Enable Threshold and Hysteresis*, TPS62125 Data Sheet (SLVSAQ5).

6. Coiltronics™, *HIgh Frequency, HIgh Current Power Inductors Flat-Pac FP1208 Series*, Flat-Pac FP1208 Series Data Sheet.
7. Texas Instruments, *Basic Calculation of a Buck Converter's Power Stage*, Application Report (SLVA477).
8. Texas Instrument, *Understanding Buck Power Stages in Switchmode Power Supplies*, Application Report (SLVA057).

7.1 Trademarks

8 About the Author

RAMKUMAR S is a systems engineer at Texas Instruments where he is responsible for developing reference design solutions for the industrial segment. Ramkumar brings his diverse experience in analog and digital power supplies design to this role. Ramkumar earned his Master of Technology (M.Tech) from the Indian Institute of Technology in Delhi.

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Revision A History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (August 2016) to A Revision	Page
• Changed Figure 11.	18

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