Design Guide: PMP9778

Low Radiated EMI Boost Converter Reference Design With TPS61088

Design Overview

This reference design delivers a low radiated EMI solution with boost converter TPS61088. By minimizing the high di/dt critical path area, using an integrated ground plane next to the topside signal layer, placing an appropriate RC snubber at the SW node, this reference design can get more than 6dB margin in the EN55022 and CISPR22 class B radiation test. The output power capability of this reference design is 18 W. The whole solution size is only 4.6 cm^2.

Design Features

- 2.7V to 4.2V input voltage range
- 5V/3A, 9V/2A and 12V/1.5A output capability
- More than 6dB margin in EN55022 and CISPR22 class B radiation test
- Small solution size
- Ideal for power bank, blue-tooth speaker application, etc.

Design Resources

PMP9778	Design folder
TPS61088	Product Folder

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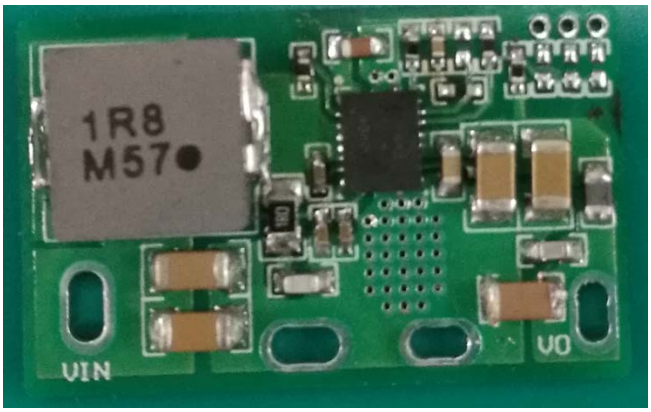

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1 Introduction

The Synchronous boost converter TPS61088 is an easy to use step-up DC-DC converter which provides a high efficiency and small size solution in portable systems. It is widely used in quick charge power bank, blue-tooth speaker, portable POS terminal, etc. Some customer fail the EN55022 and CISPR22 Class B radiated emission test though they have already used multi-layer PCB, added RC snubber and used enough decoupling caps in the circuit. By study, we found that almost all of the failures are caused by poor layout.

Good layout from first prototype at the beginning of the design does not add to cost. But actually it saves significant resources in mechanical shielding design, EMI filters selection and EMI testing, PCB layout and board assembly.

This reference design delivers a low radiated EMI solution with boost converter TPS61088.By minimizing the high di/dt critical path area, using an integrated ground plane next to the topside signal layer, placing an appropriate RC snubber at the SW node, this reference design can get higher than 6dB margin in the EN55022 and CISPR22 class B radiation test.

Figure 1 shows the EN55022 and CISPR22 class B radiated emission limit. To get higher than 6dB margin during the radiation test, the test result at 30-230MHz range should be lower than 34dBμV/m, at 230MHz-1GHz range should be lower than 41dBμV/m.

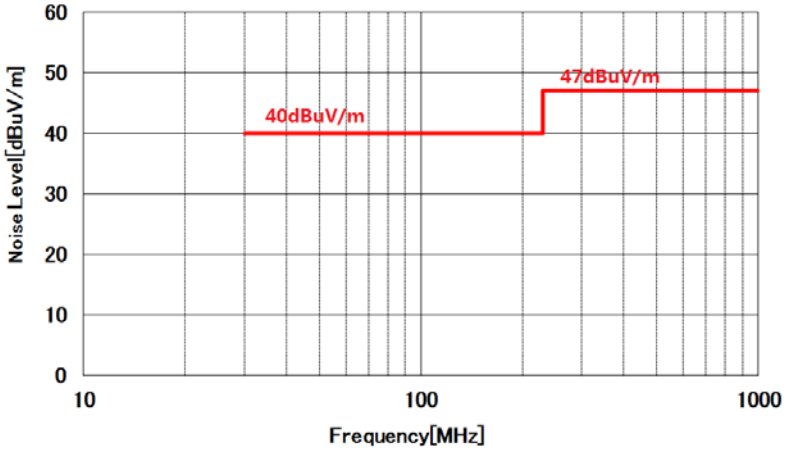

Figure 1. EN55022 and CISPR22 Class B Radiated Emission Limit

2 Specification

Table 1 gives out the performance specification of this reference design. Under the specified input voltage and output power range, the radiated emission margin should be higher than 6dB to the EN55022 and CSIPR 22 class B limit.

Table 1. Performance Specification

Input Voltage	Output Voltage/Output Current	Radiated Emission Margin
3V-4.2V	5V/3A, 9V/2A, 12V/1.5A	>6dB

3 Design Process

This section provides the PMP9778 layout notification and ferrite bead selection. Poor layout will lead to poor radiation EMI. Please refer to the application note SLVA790 for the method of layout optimization. For the power components and compensation network calculation, please refer to the TPS61088 datasheet.

3.1 Layout Notification

Figure 2 shows the topology and critical current path of the Boost converter. The current flowing through S2, S1 and the output capacitor Cout is a pulsating current (red loop). So we should minimize the area enclosed by this loop during the layout. The traces in connection of TPS61088's VOUT pin and the output decoupling capacitors should be short and wide.

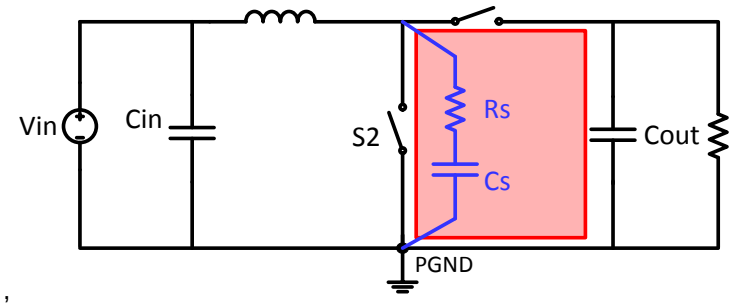

Figure 2. Critical Current Path of Boost Converter

Secondly, put a solid ground plane with minimum distance to the signal layer (in this reference design, top layer is the signal layer). We use a 1.2 mm thickness 4-layer PCB in this reference design, the ground plane is right under the signal layer. The distance from the ground plane to the signal layer is only 0.4mm.

Thirdly, add a RC snubber across the TPS61088's SW pin and power ground. The RC snubber can effectively damp out SW voltage ring, which helps reducing the radiated EMI levels. It should be placed as close as possible to the switch node and power ground.

Finally, put the main inductor L1 and the boost converter TPS61088 on the same layer. The copper plane in connection of L1 and TPS61088's SW pin should be small and on the same layer to avoid spreading high frequency noises to the other layers.

3.2 Ferrite Bead Selection

The output bead filter L01 (Figure 8) is an important component in this reference design. We need to select it carefully because all of the output DC current flows through this bead. An improper ferrite bead can't improve the radiation EMI and may even degrade the circuit performance.

Firstly, the noise frequencies must fall within the bead's resistive band. That is, we should carefully studying the impedance versus frequency characteristics when choosing a ferrite bead. Make sure the bead's resistive impedance is much higher than the reactive impedance in the noise frequency range.

Secondly, the ferrite bead's rated current should be at least 30% higher than the expected maximum current. Because the ferrite bead will become saturated in high current condition.

Thirdly, the ferrite bead's DC resistance should be as low as possible. Because the ferrite bead is in series with the power line, any DC current flowing through it will create a voltage drop proportional to the DC resistance. So high DC resistance may leads to poor load regulation and lower efficiency.

We choose Murata part BLM21PG300SN1 in this reference design. The DC resistance of this 4-A rating bead is only 14 mΩ. Its impedance versus frequency characteristic is shown in Figure 3. We can see that this bead provides optimum performance at noise frequencies from 100 MHz to 3 GHz range.

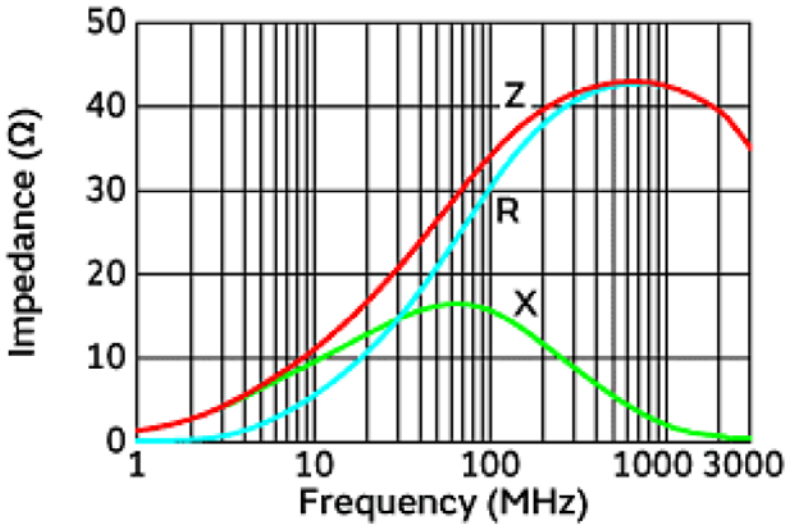

Figure 3. Impedance VS. Frequency Characteristics (BLM21PG300SN1)

4 Test Result

Figure 4 shows the setup of the radiated EMI test. The PCB board under the test should be put on the middle of the table border. The position of the input source, PCB board and the output load should keep unchanged in each test. The input source should use batteries instead of a DC power supply. Because the DC power supply itself will generate electromagnetic radiation during the test and make the test result much worse than the real circuit.

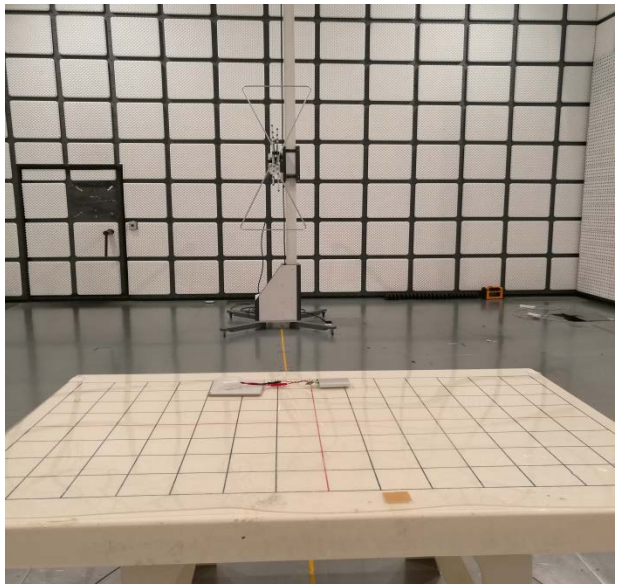

Figure 4. Setup of the Radiated EMI Test

Figure 5, figure 6 and figure 7 show the PMP9778 radiated EMI results at different output load conditions. These tests were performed in a third party certified 3 meter EMI chamber. We can see that all the tests passed the EN55022 and CISPR22 Class B limit, with higher than 6 dB margin.

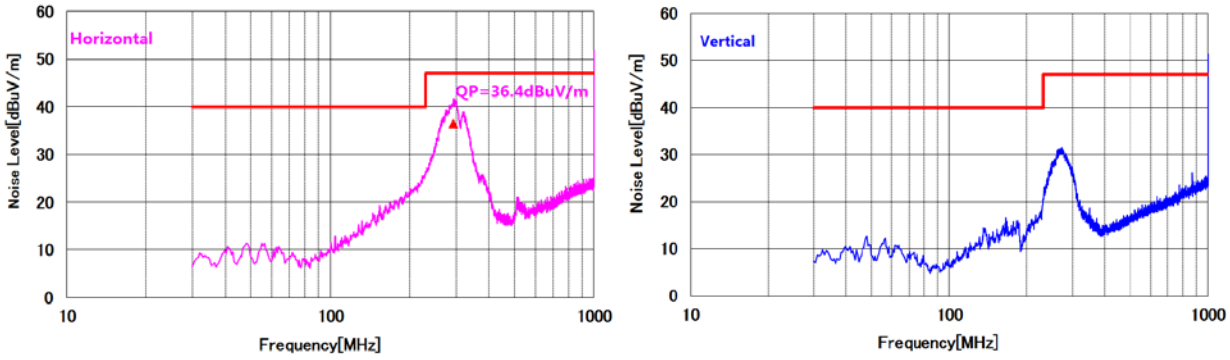

Figure 5. Radiated EMI Result (V_{IN}=3.3V, V_O=5V/I_O=3A)

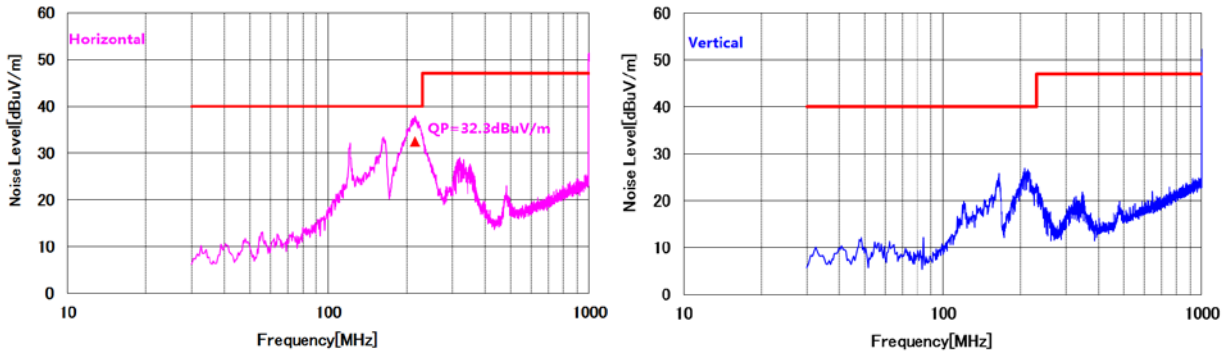

Figure 6. Radiated EMI Result (V_{IN}=3.3V, V_O=9V/I_O=2A)

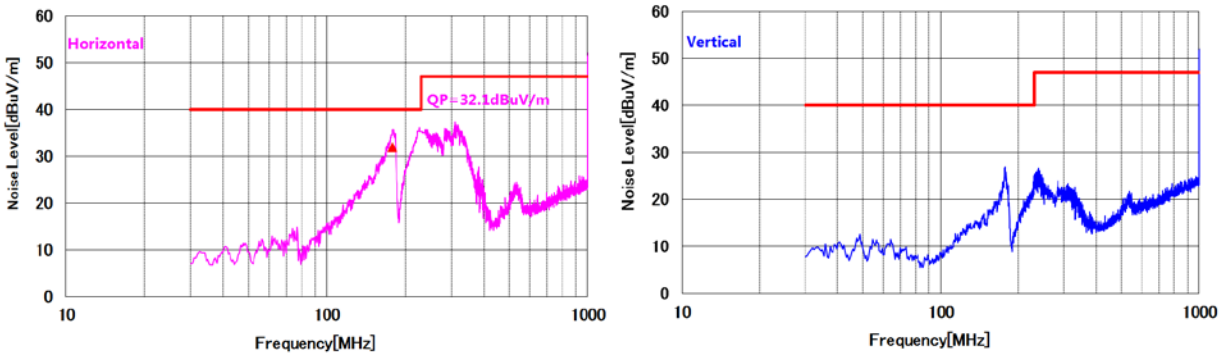

Figure 7. Radiated EMI Result (V_{IN}=3.3V, V_O=12V/I_O=1.5A)

5 Schematic, Bill of Materials and PCB Layout

This section provides the PMP9778 schematic, bill of materials (BOM) and board layout.

5.1 Schematic

Figure 8 illustrates the schematic of this reference design.

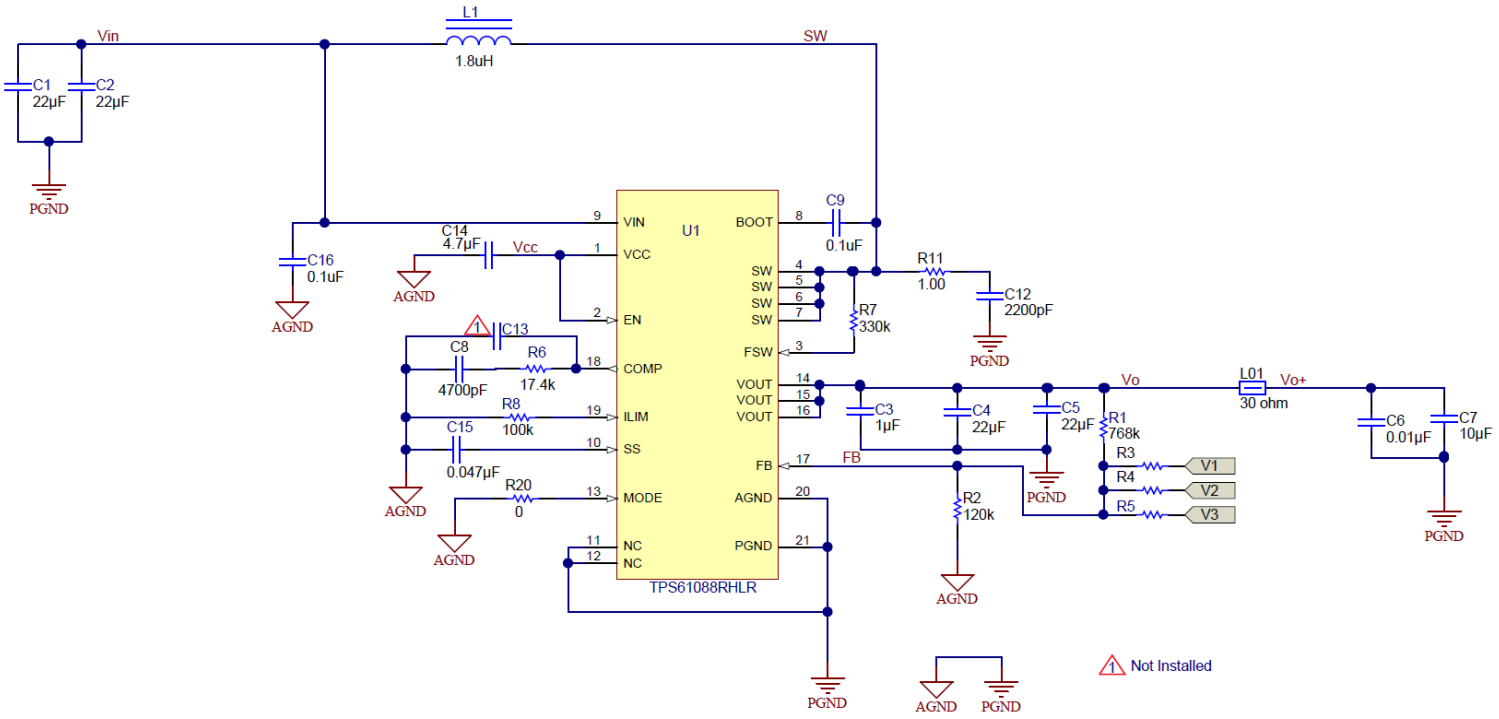

Figure 8. PMP9778 Schematic

5.2 Bill of Materials

Table 2 displays the PMP9778 bill of materials.

Table 2. PMP9778 Bill of Materials

Designator	QTY	Value	Description	Package	Part Number	MFG
C1, C2, C4, C5	4	22uF	CAP, CERM, 22 µF, 16 V, +/- 10%, X5R, 1206	1206	GRM31CR61C226KE15L	MuRata
C3	1	1uF	CAP, CERM, 1 µF, 25 V, +/- 10%, X7R, 0603	0603	GRM188R71E105KA12D	MuRata
C6	1	0.01uF	CAP, CERM, 0.01 µF, 25 V, +/- 10%, X7R, 0603	0603	GRM188R71E103KA01D	MuRata
C7	1	10uF	CAP, CERM, 10 µF, 25 V, +/- 10%, X5R, 0805	0805	GRM219R61E106KA12	MuRata
C8	1	4700pF	CAP, CERM, 4700 pF, 50 V, +/- 10%, X5R, 0402	0402	GRM155R61H472KA01D	MuRata
C9, C16	2	0.1uF	CAP, CERM, 0.1uF, 16V, +/-10%, X5R, 0402	0402	GRM155R61C104KA88D	MuRata
C12	1	2200pF	CAP, CERM, 2200 pF, 50 V, +/- 5%, C0G/NP0, 0603	0603	GRM1885C1H222JA01D	MuRata
C14	1	4.7uF	CAP, CERM, 4.7 µF, 25 V, +/- 10%, X5R, 0603	0603	GRM188R61E475KE11D	MuRata
C15	1	0.047uF	CAP, CERM, 0.047 µF, 16 V, +/- 10%, X7R, 0402	0402	GRM155R71C473KA01D	MuRata
L01	1	30 ohm	Ferrite Bead, 30 ohm @ 100 MHz, 3.5 A, 0805	0805	BLM21PG300SN1	MuRata
L1	1	1.8uH	Inductor, Shielded Drum Core, Metal Composite, 1.2 µH, 12.9 A, 0.007 ohm, SMD	9.5x8.7mm	CDMC8D28NP-1R2MC	Sumida
R1	1	768k	RES, 768 k, 1%, 0.063 W, 0402	0402	CRCW0402768KFKED	Vishay-Dale
R5, R8	2	100k	RES, 100k ohm, 1%, 0.063W, 0402	0402	CRCW0402100KFKED	Vishay-Dale
R6	1	17.4k	RES, 17.4k ohm, 1%, 0.063W, 0402	0402	CRCW040217K4FKED	Vishay-Dale
R7	1	330k	RES, 330 k, 5%, 0.063 W, 0402	0402	CRCW0402330KJNED	Vishay-Dale
R20	1	0	RES, 0, 5%, 0.063 W, 0402	0402	RC0402JR-070RL	Yageo America
U1	1		13.2-V Output, Synchronous Boost Converter with 10-A Switch, RHL0020A	RHL0020A	TPS61088RHLR	Texas Instruments
C13	0	47pF	CAP, CERM, 47 pF, 50 V, +/- 1%, C0G, 0402	0402	GRM1555C1H470FA01D	MuRata
R11	1	1.00	RES, 1.00, 1%, 0.125 W, 0805	0805	CRCW08051R00FKEA	Vishay-Dale

5.3 PCB Layout

Figure 9 through Figure 22 show the PMP9778 PCB layout.

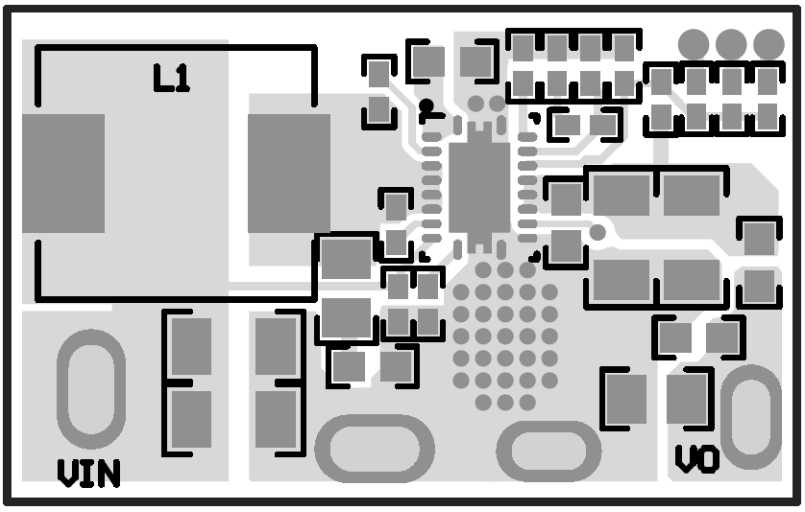

Figure 9. PMP9778 Top layer and Top Silkscreen

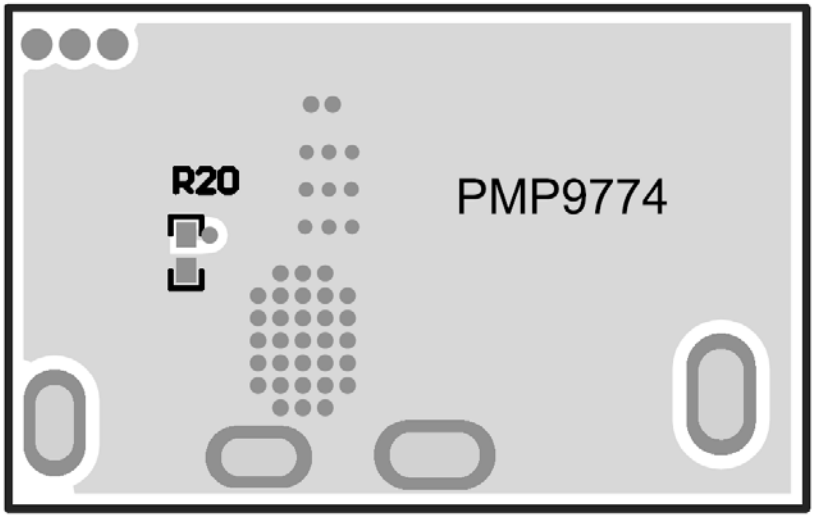

Figure 10. PMP9778 Bottom layer and Bottom Silkscreen

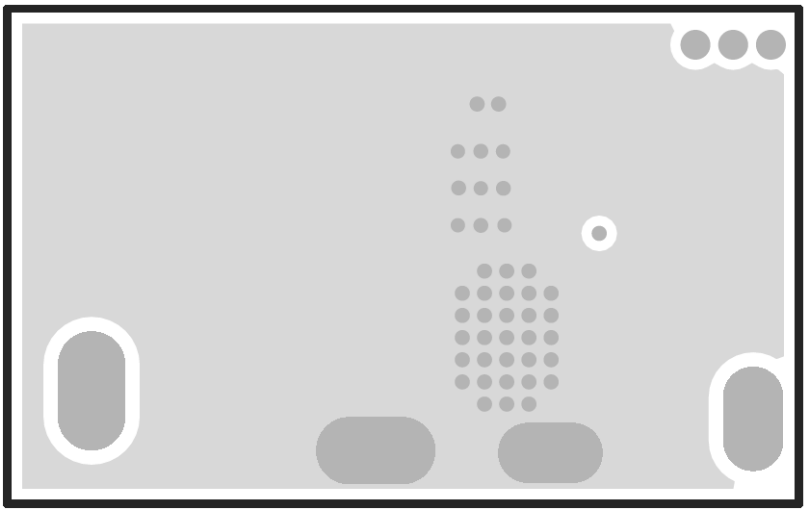

Figure 11. PMP9778 Internal Layer 1

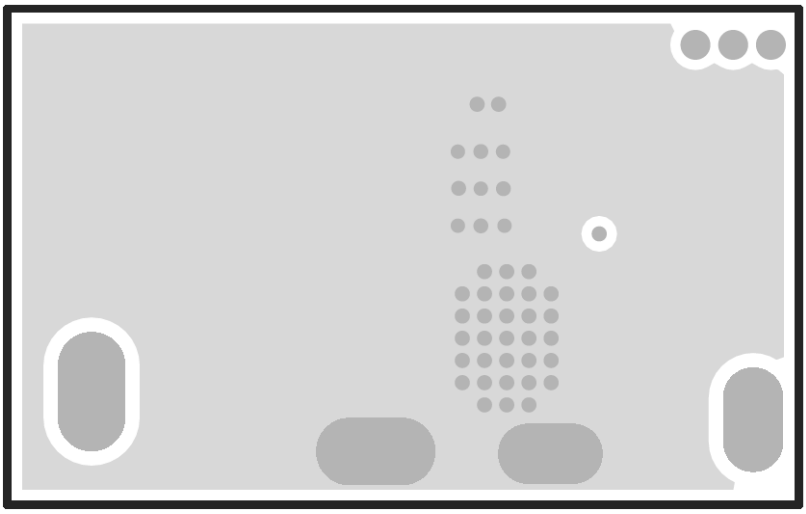

Figure 12. PMP9778 Internal Layer 2

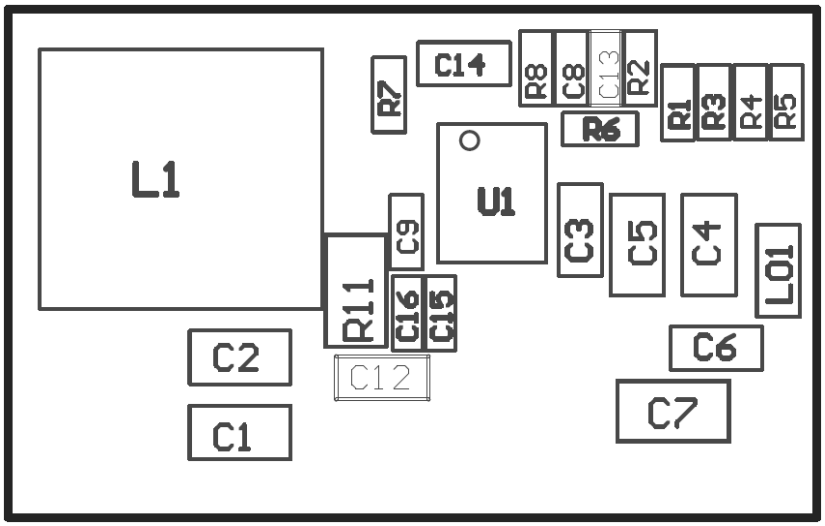

Figure 13. PMP9778 Assembly Drawing

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