*TI Designs*

# *Quad-Channel, 12-bit, 50-MSPS ADC Reference Design With Low-Noise, Low-Distortion, DC and AC Inputs*

## Designs

The TIDA-00799 reference design demonstrates how to implement a single-ended or differential input path, which can be AC coupled or DC coupled for an ADC3422 device. The TIDA-00799 design also showcases how to design a high-input impedance, DC-coupled input path for an ADC. This design implements the ADC3422, which is a quad-channel, 50-MSPS, 12-bit low power ADC. This reference design can be used for applications such as low-power data acquisition, portable instrumentation, insulated-gate bipolar transistor (IGBT) diagnostics, and MOSFET diagnostics.

## Resources

| | |
|---|---|
| TIDA-00799 | Design Folder |
| ADC3422 | Product Folder |
| THS4541 | Product Folder |
| OPA656 | Product Folder |
| TINA-TI™ | Product Folder |

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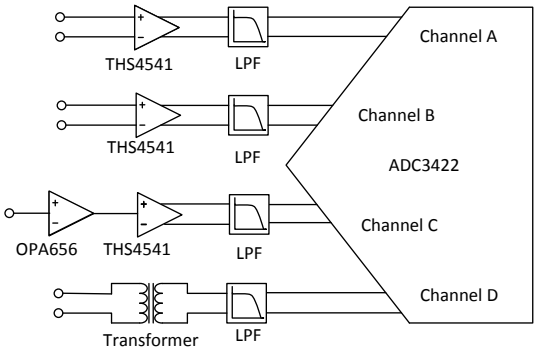
## Features

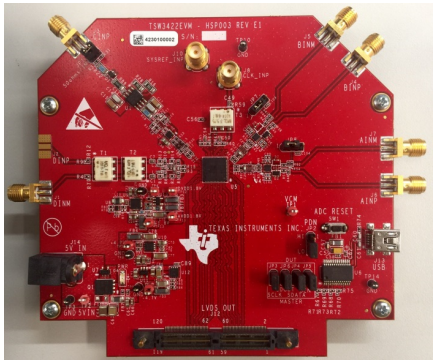
- Single-Ended to Differential Reference Design Using OPA656 and THS4541
- Channel A and Channel B DC-Coupled Using THS4541
- THS4541 and ADC Achieves 70-dB SNR and 96-dB SFDR
- Low-Power Operation Suitable for Battery-Powered Devices

## Applications

- Portable Instrumentation
- Low-Power Data Acquisition
- IGBT and MOSFET Diagnostics
- Motor Control
- Imaging





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# 1 Circuit Description

This TIDA-00799 TI Design is based on the quad-channel ADC3422. This design showcases an analog-to-digital converter (ADC) with three different input paths. The first and second channels have both been DC coupled using the THS4541 wideband, fully differential amplifier (FDA). Both channels can be configured for single-ended input or differential inputs with modifications to the bill of materials (BOM). Channel 3 can be used as a scope input because it uses the junction gate field-effect transistor (JFET) OPA656 as a high input impedance amplifier followed by the THS4541 fully differential amplifier. Channel 4 of the ADC has been configured as a passive path through a transformer (AC coupled). Channel 4 accepts single-ended inputs by default but can be modified to accept differential signals by doing a BOM modification.

# 2 ADC3422

The ADC3422 is a member of the ADC3xxx family. At the time of this writing, the ADC3xxx family features the lowest-power ADCs in the industry, capable of running 25 MSPS to 160 MSPS. The ADC3xxx family provides flexibility and scalability with 12- and 14-bit, 2- and 4-channel, and JESD204B and serial LVDS options ranging from 50 mW to 200 mW of power consumption per channel. The focus of this design is on the ADC3422, which is a quad-channel, 12-bit, 50-MSPS ADC; however, the same circuit can be applied across the entire ADC3xxx family with minimal modifications.

# 3 Channel 1 and Channel 2—DC Coupled

Channel 1 and channel 2 are DC coupled with the THS4541 fully-differential wideband amplifier. By default (jumper JP7 and JP8 at pin 1 and 2), both channels have been designed to accept 50-Ω impedance, single-ended inputs; however, these channels can be modified (jumper JP7 and JP8 at pin 2 and 3) to accept AC-coupled signals. This modification can be performed by installing J5 and D6 and removing the jumper JP7 for channel 1, followed by installing J7 and D7 and removing the jumper JP8 for channel 2 to accept differential inputs. The schematic design is shown in Figure 1.

Several methods are available for calculating the resistors around an FDA to convert from a single-ended input to differential output. The following assumptions simplify the results:

1. Start the design by selecting the feedback resistors and making them equal on both sides.
2. The DC and AC impedances from the summing junctions back to the signal source and the ground (or a bias voltage on the non-signal input side) are set to retain a feedback divider balance on each side of the FDA.

Using the feedback resistors, solve for $R_T$ (termination resistor to ground on the signal input side), $R_{G+}$ (input gain resistor for the signal path), and $R_{G–}$ (matching gain resistor on the non-signal input side). The same resistor solution can be applied to either AC or DC coupled paths. Adding blocking caps in the input signal chain is a simple option where adding it after the $R_T$ element has the advantage of removing any DC currents in the feedback path from the output $V_{OCM}$ to ground. Earlier approaches to the solutions for $R_T$ and $R_{G+}$ (when the input must be matched to the source impedance, $R_S$) have followed an iterative approach. This complexity arises from the active input impedance looking into the $R_{G+}$ element. When the FDA is used to convert a single-ended signal to differential, the common-mode input voltage at the FDA inputs must move with the input signal to generate the inverted output signal as a current in the $R_{G–}$ element, which is just one way to view the situation. Equation 1 shows a more recent solution where a quadratic in $R_T$ can be solved for an exact required value. This quadratic emerges from the simultaneous solution for a matched input impedance and target gain. The only required inputs are:

1. The selected $R_F$ value.
2. The target voltage gain ($A_V$) from the input of $R_T$ to the differential output voltage
3. The desired input impedance looking into $R_T$ and $R_{G+}$ to match the source impedance $R_S$

Solving this quadratic for $R_T$ starts the solution sequence (see Equation 1):

$$R_T^2 - R_T \times \frac{2R_S\left(2R_F + \frac{R_S}{2}A_V^2\right)}{2R_F(2+A_V) - R_S A_V(4+A_V)} - \frac{2R_F R_S^2 A_V}{2R_F(2+A_V) - R_S A_V(4+A_V)} = 0 \quad (1)$$

Being a quadratic, there are limits to the range of solutions. Specifically, when $R_F$ and $R_S$ have been chosen, there is physically a maximum gain that starts to solve for the negative $R_T$ values (if input matching is a requirement). With $R_F$ selected, check Equation 2 to verify that the maximum gain is less than the desired gain:

$$A_{V(max)} = \left(\frac{R_F}{R_S} - 2\right) \times \left(1 + \sqrt{1 + \frac{4 \times \frac{R_F}{R_S}}{\left(\frac{R_F}{R_S} - 2\right)^2}}\right) \quad (2)$$

If the achievable $A_{V\_MAX}$ is less than desirable, increase the $R_F$ value. As soon as $R_T$ has been derived from the preceding Equation 1, the $R_{G+}$ element can be calculated by the following Equation 3:

$$R_{G+} = \frac{2 \times \frac{R_F}{Av} - R_S}{1 + \frac{R_S}{R_T}} \quad (3)$$

Then the simplest approach is to use a single $R_{G-} = R_T \,||\, R_S + R_{G+}$ on the non-signal input side. These solutions are shown as separate elements here, but a single resistor to GND as given by Equation 4 is also acceptable. Equation 4 calculates a direct solution for $R_{G-}$.

$$R_{G-} = \frac{2 \times \frac{R_F}{Av}}{1 + \frac{R_S}{R_T}} \quad (4)$$

This design proceeds from a target input impedance matched to $R_S$, signal gain $A_V$, and a selected $R_F$ value. The nominal $R_F$ value for this THS4541 implementation is 402 Ω. Decreasing the $R_F$ value improves noise and phase margin but reduces the total output load impedance, which can degrade harmonic distortion. Increasing the value increases the output noise and may reduce the loop phase margin because of the feedback pole to the parasitic input capacitance back to the input pins; however, increasing the value also reduces the total loading on the outputs.

This design starts with a 402-Ω feedback resistor and has been designed for a DC-coupled, 50-Ω input match providing a gain of 2.35 V/V to the THS4541 output pins. The third order, inter-stage, low-pass filter provides a 20-MHz Bessel low-pass response with a 0.85-V/V insertion loss to the ADC, resulting in a net gain of 2 V/V from the board edge to the ADC inputs. Even though the THS4541 can absorb overdrives, an added external protection element has been added using the BAV99 low-capacitance diodes, as Figure 1 shows. Pin 1 and pin 2 can be jumpered together to enable DC-coupled testing. When the source is an AC-coupled, 50-Ω source, pin 2 and pin 3 are jumpered to maintain the differential balance. FFT testing normally uses a AC-coupled bandpass filter into the board and requires an AC-coupled connection at pin 2 and pin 3 of jumpers JP7 and JP8.

The results for this implementation use 1% standard resistor values: Choose $R_F$ = 402, Assume $R_S$ = 50, $A_V$ = 2.35 V/V, and then solve for $R_T$ = 61.9, $R_{G+}$ = 162, $R_{G-}$ = 190 (162 + 61.9 / 49.9 for balance).

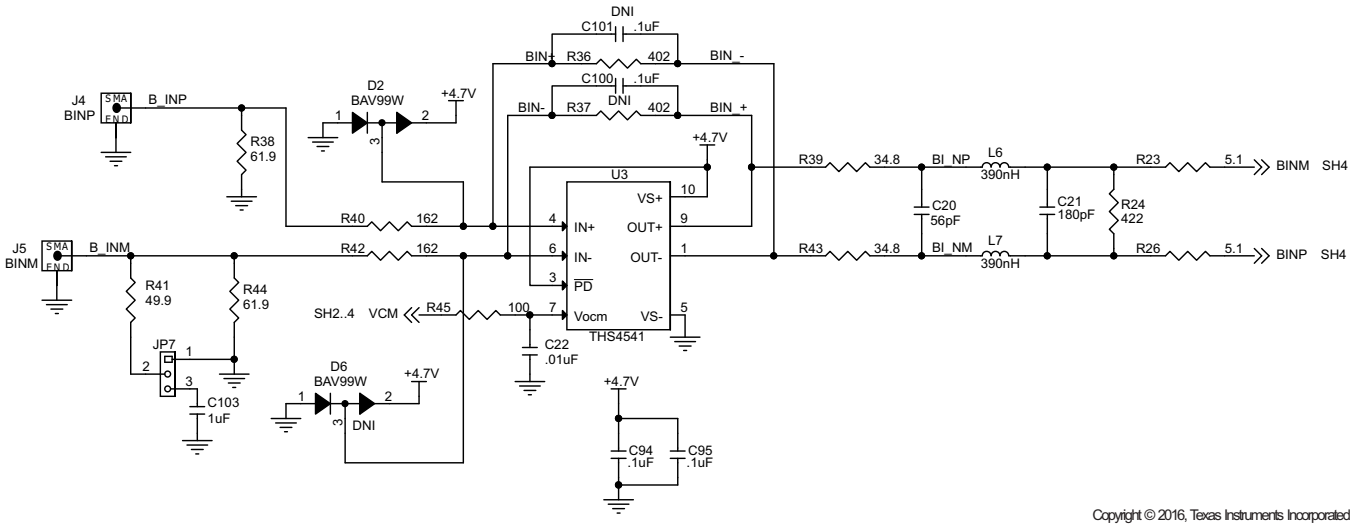


**Figure 1. THS4541 Circuit Implementation With 20-MHz Cutoff Bessel LPF Driving ADC3422**

## 4 THS4541 and ADC3422 Results

The results for the implementation of the THS4541 and ADC3422 show a good combined response. In a simple test in which a clean, filtered signal was fed into the THS4541 and ADC3422 circuit, the signal-to-noise ratio (SNR) was better than 70 dB, which is a slight degradation from the 70.3 dB of the ADC3244 device using a transformer interface. The spurious-free dynamic range (SFDR) that the following Figure 2 shows in the left-side measurement panel is slightly lower (3 dB) than the transformer interface input path (channel 4). In summary, a clean active interface can be implemented using the THS4541 device to drive the high-performance requirements of the 12- and 14-bit ADC3xxx data converter family. For applications below 5 MHz, consider the 1-mA precision THS4551 FDA. For applications above 50 MHz, consider the 2.8-GHz, low-noise LMH6554 FDA as a viable option.

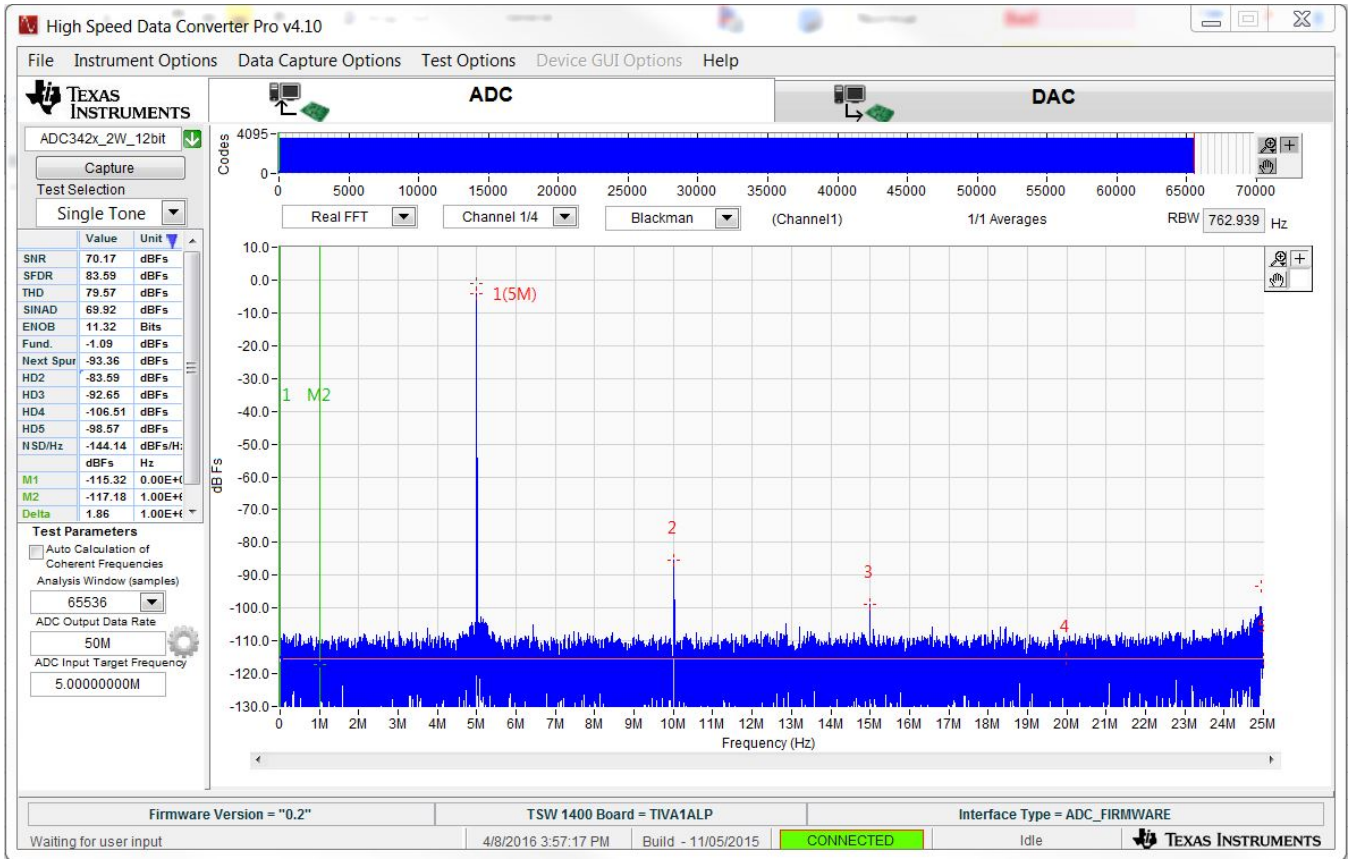


**Figure 2. FFT Performance of THS4541 and ADC3422 Active Interface**

## 5 Channel 3—High Input Impedance

Channel 3 has been designed with an OPA656 device which has a JFET input stage followed by a single-ended to differential amplifier (THS4541) and the second-order, low-pass (19-MHz) Bessel filter.

There are two main parameters to consider for channel 3:

1. The allowed maximum analog input voltage for the ADC is –1 dBFS (1.8 $V_{P-P}$).
2. The maximum first Nyquist zone bandwidth is 25 MHz.

Based on these requirements, the acceptable input signal can be 2 $V_{P-P}$. For this design, the user sets up the OPA656 device to accept ±1 V and with a gain of 2 V/V. This setup provides 4 $V_{P-P}$ to the fully differential amplifier (FDA) stage, which then decreases to 1.8 $V_{P-P}$ max for the ADC. The OPA656 device is used in a non-inverting configuration, where the gain of the non-inverting amplifier is shown in Equation 5 ($R_2$ = $R_1$ = 200 Ω, which results in a gain of 2 V/V and a 400-Ω load at the amplifiers output).

$$V_{OUT} = \left(1 + \frac{R_2}{R_1}\right) V_{IN} \tag{5}$$

The input has been designed to provide a 1-MΩ termination with an optional 50-Ω input resistance for a 50-Ω source. The input resistance can be selected by installing (50 Ω) and uninstalling (1 MΩ) a jumper (JP1) on the board. After the input termination resistors, a 150-Ω resistor in series is added to limit the current into the overdrive protection BAV99. The BAV99 diode pair is added after the 150-Ω series resistor on the positive input terminal, which is connected to the positive and negative supplies to protect the input. The BAV99 diode pair is capable of protecting against 300 mA of current and provides protection up to ±50-V input transients. The diodes add about 2.5 pF of capacitance to the circuit. A 50-Ω resistor is added after the BAV99 to ensure that the majority of any fault current flows into the protection diodes (BAV99) and not the internal electrostatic discharge (ESD) diodes of the OPA656 device. An external capacitance is added after the 50-Ω resistor at the positive input. This additional external capacitance provides a 100-MHz bandwidth into this stage from the source and limits the high-frequency signals and broadband noise.

Figure 3 and Figure 4 show the simulation circuit and transfer character for the OPA656 stage. As shown by the transfer function, the OPA656 provides the gain of 6 dB or 2 V/V and capacitor C1 provides the 100-MHz bandwidth.

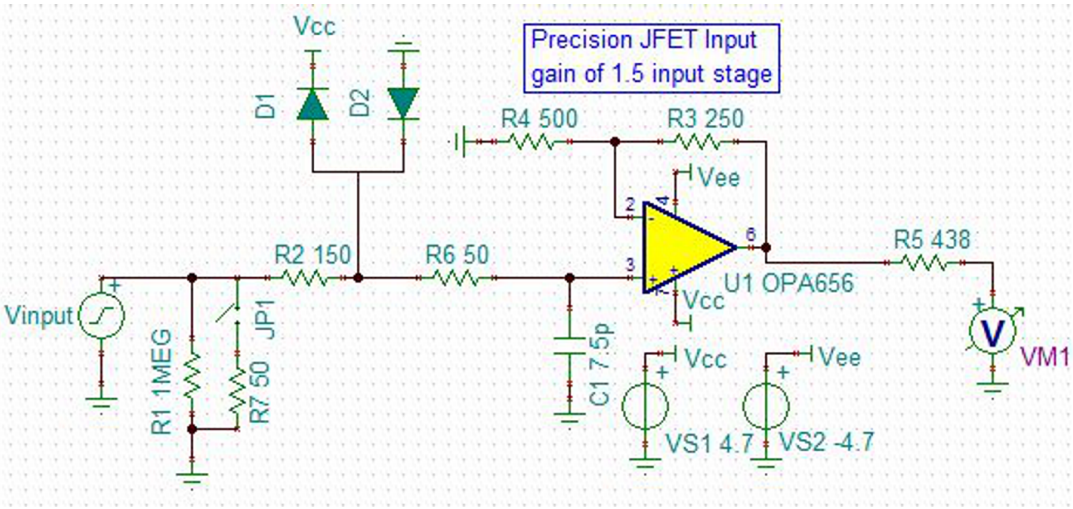


**Figure 3. Simulation Circuit for OPA656**

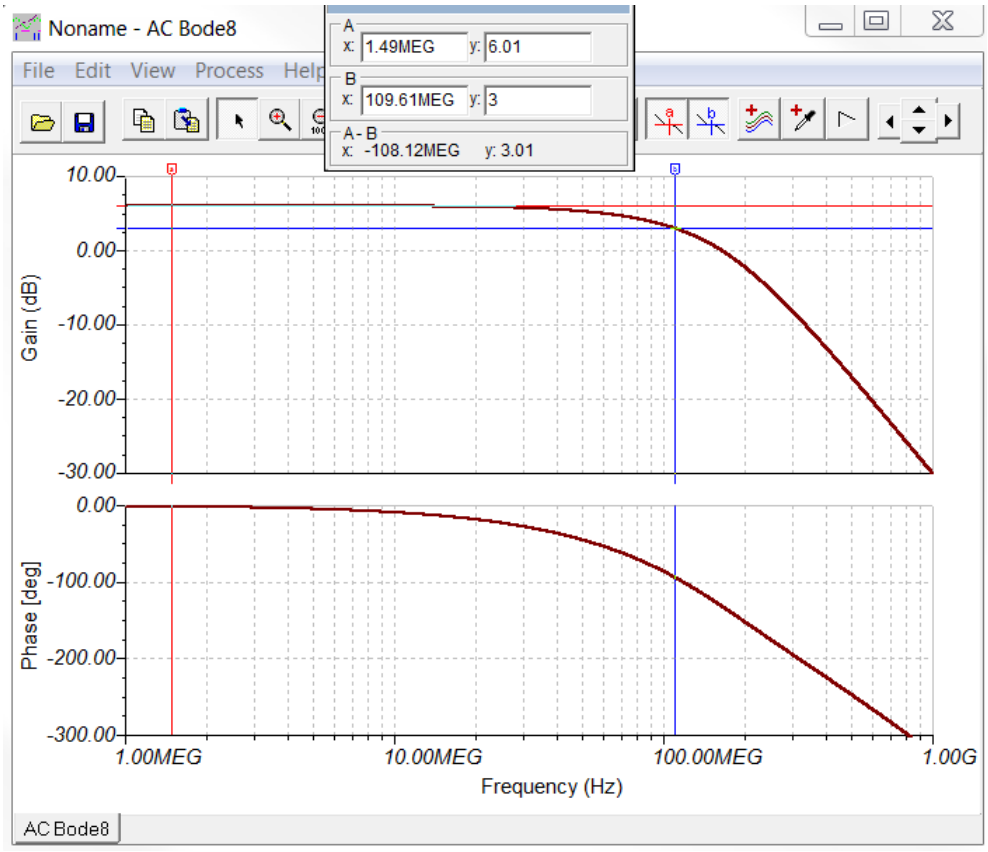


**Figure 4. Transfer Function for OPA656 Stage**

The fully differential amplifier (FDA) stage uses a THS4541 amplifier. To get from 4 $V_{P-P}$ to 1.8 $V_{P-P}$ a total insertion loss of 7 dB is required, as shown in Equation 6.

$$\text{Insertion loss} = 20 \times \log\left(\frac{1.8\ \text{V}}{4\ \text{V}}\right) = -6.93575 \tag{6}$$

Assuming a 2-dB insertion in the final RLC low-pass filter stage, the FDA stage must be designed for an insertion loss of 5 dB or a gain of 0.567 V/V. Figure 5 shows a simplified diagram of the FDA stage:

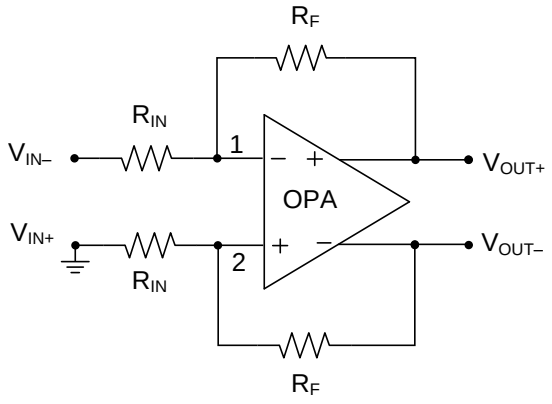


**Figure 5. Single-Ended to Differential Amplifier**

Figure 5 derives the relationship between input voltage ($V_{IN}$) and output voltage ($V_{OUT}$) and using the relationship between $V_{IN}$ and $V_{OUT}$, the values for $R_{IN}$ and $R_F$ can be calculated. Solving for voltage at node 1 shows the relationship between $V_{OUT+}$ and $V_{IN-}$, as Equation 7 shows. Solving for voltage at node 2 shows the relationship between $V_{OUT-}$ and $V_{IN+}$, as Equation 8 shows. To calculate the differential output voltage, $V_{OUT-}$ is subtracted from $V_{OUT+}$, as Equation 9 shows.

$$V_{OUT+} = -\left(\frac{R_F}{R_{IN}}\right) \times V_{IN-} \tag{7}$$

$$V_{OUT-} = -\left(\frac{R_F}{R_{IN}}\right) \times V_{IN+} \tag{8}$$

$$V_{OUT+} - V_{OUT-} = \left(\frac{R_F}{R_{IN}}\right) \times V_{IN-} - \left(\frac{R_F}{R_{IN}}\right) \times V_{IN+} \tag{9}$$

$$V_{OUT+} - V_{OUT-} = \left(\frac{R_F}{R_{IN}}\right) \times \left(V_{IN-} + V_{IN+}\right) \tag{10}$$

$$V_{OUT\_DIFF} = V_{OUT+} - V_{OUT-} = -\left(\frac{R_F}{R_{IN}}\right) \times V_{IN-} \tag{11}$$

$V_{IN+}$ is connected to ground which means $V_{IN+} = 0$; substitute $V_{IN+}$ into Equation 10 to further simplify the equation. Equation 11 represents the relationship between single-ended input voltage ($V_{IN-}$) and differential output voltage ($V_{OUT\_DIFF}$). The values of $R_F = 248\ \Omega$ and $R_{IN} = 438\ \Omega$ have been selected to calculate a gain of 0.567 V/V from the FDA stage. These output signals are offset to the $V_{OCM}$ control pin voltage.

Figure 6 and Figure 7 show the simulation circuit and transfer character for the FDA stage. As the transfer function shows, the THS4541 device provides a gain of –5 dB or 0.567 V/V. If the peaking is not desired, refer to the designing attenuations section of the THS4541 data sheet ([1]). The second-order RLC filter attenuates this peaking.

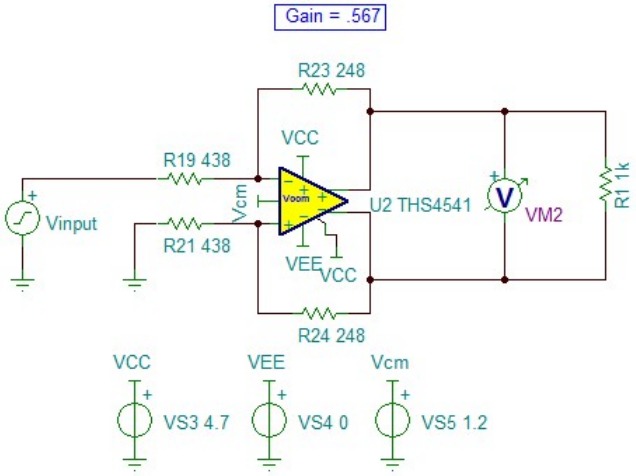


**Figure 6. Simulation Circuit for Single-Ended to Differential Amplifier**

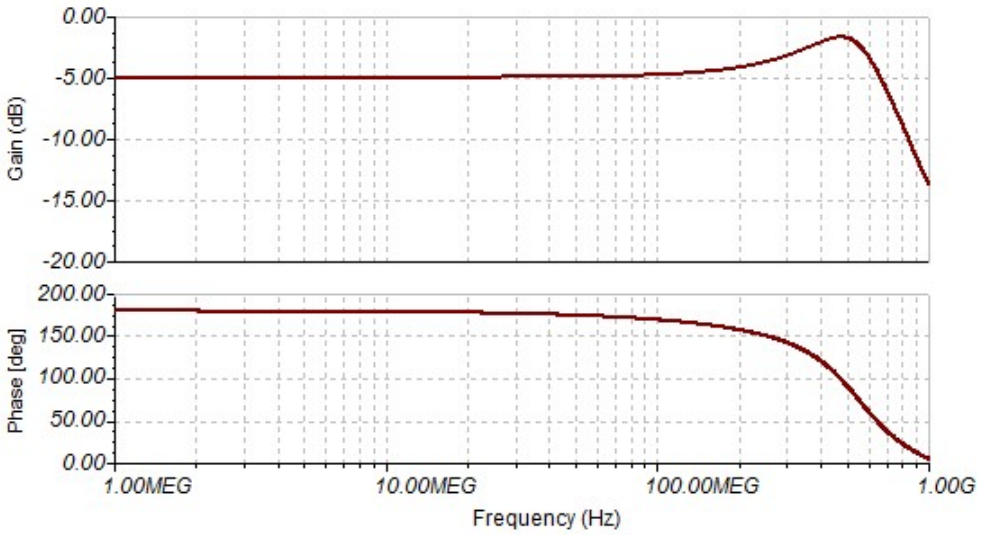


**Figure 7. Transfer Function for Single-Ended to Differential Amplifier**

The maximum input signal in the FDA stage is 4 $V_{P-P}$. With a gain of 0.567 V/V the output is 2.268 $V_{P-P}$, which means the signal swings ±1.134 V around the common-mode voltage ($V_{CM}$). To prevent –1.134 V from clipping into the negative rail (0 V), set $V_{CM}$ to 1.2 V. The common-mode voltage from the THS4541 output must be level-shifted from 1.2 V to 0.95 V in the low-pass filter stage to meet the input common requirements of the ADC.

The low-pass filter stage has been designed using a second-order, low-pass Bessel filter with the following parameters:

- $F_O$ (cutoff frequency) –3 dB = 19 MHz
- Q = 0.58
- DC gain (filter attenuation) = 0.8 V/V (–2 dB)

This filter design starts with a single-ended input and single-ended output to derive the equations to convert to differential at a later stage. The design begins with the use of an RLC filter, as Figure 8 shows.

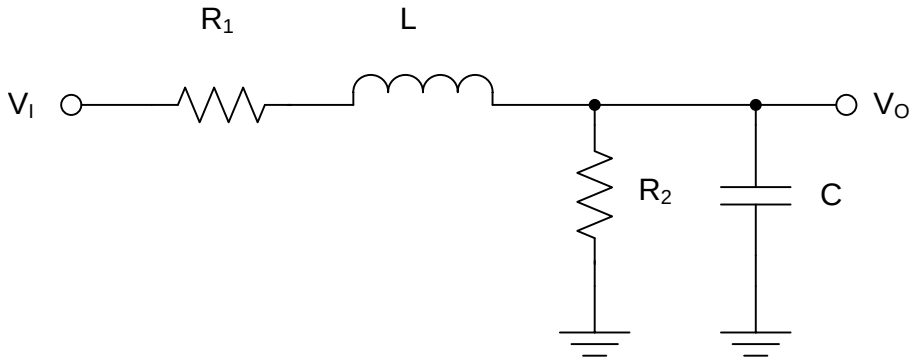


**Figure 8. Single-Ended, Low-Pass RLC Filter**

Equation 12 calculates the general Laplace transfer function for the circuit in Figure 8 . Refer to the *RLC Filter Design for ADC Interface Applications* application report for the full design details [2].

$$\frac{V_i}{V_o} = \frac{\frac{1}{LC}}{S^2 + S\left[\frac{1}{R_2C} + \frac{R_1}{L}\right] + \left(1 + \frac{R_1}{R_2}\right)\frac{1}{LC}} \tag{12}$$

Calculating the DC attenuation ($\alpha$) from Equation 12 results in Equation 13:

$$\alpha = \frac{R_2}{R_1 + R_2} \tag{13}$$

The total DC impedance that $V_I$ experiences is calculated using Equation 14:

$$R_T = R_1 + R_2 \tag{14}$$

Rewrite Equation 12 by substituting $\alpha$ and $R_T$ in the following Equation 15:

$$\frac{V_I}{V_O} = \frac{\frac{1}{LC}}{S^2 + S\left[\frac{1}{\alpha R_T C} + \frac{R_T(1-\alpha)}{L}\right] + \frac{1}{\alpha LC}} \tag{15}$$

From Equation 15, the key elements for the second-order filter can be derived, as the following Equation 16 and Equation 17 show:

$$Q = \frac{\sqrt{\frac{1}{\alpha LC}}}{S^2 + S\left[\frac{1}{\alpha R_T C} + \frac{R_T(1-\alpha)}{L}\right] + \frac{1}{\alpha LC}} \tag{16}$$

$$W_O = \sqrt{\frac{1}{\alpha LC}} \tag{17}$$

$W_O$ represents the cutoff frequency in radians and Q represents the quality factor. $W_O$ and Q describe the frequency response of the second-order filter. Start the design process by selecting $R_T$ and $\alpha$ according to design requirements and then solve for $R_1$, $R_2$ , L, and C for the provided values of $W_O$ and Q. Use Equation 16 and Equation 17 to solve for L. Two possible solutions are available for deriving L: a greater value and a lesser value solution, as Equation 18 and Equation 19 show, respectively. Using the greater value for L (from Equation 18) results in a decreased required C value, whereas using Equation 19 results in an increased C value.

$$L = \frac{R_T}{2W_O Q}\left[1 + \sqrt{1-(1-a)(2Q)^2}\right] \quad (18)$$

$$L = \frac{R_T}{2W_O Q}\left[1 - \sqrt{1-(1-a)(2Q)^2}\right] \quad (19)$$

Equation 17 can be rewritten to solve Equation 20. By using Equation 18 or Equation 19, the value of C can then be calculated.

$$C = \frac{1}{\alpha L (W_O)^2} \quad (20)$$

By using Equation 12 through Equation 20 and following the design requirements, the values for $R_1$, $R_2$, L, and C can be calculated.

- $R_1$ = 80 Ω
- $R_2$ = 320 Ω

**High L, low C solution**:

- L = 5.36 µH
- C = 16.4 pF

**Low L, high C solution**:

- L = 419 nH
- C = 209 pF

When all the required values have been calculated, the single-ended filter design can be converted to a differential filter. To convert the example filter design shown in Figure 8 to a differential filter, first refer to Figure 9, where each element has been duplicated.

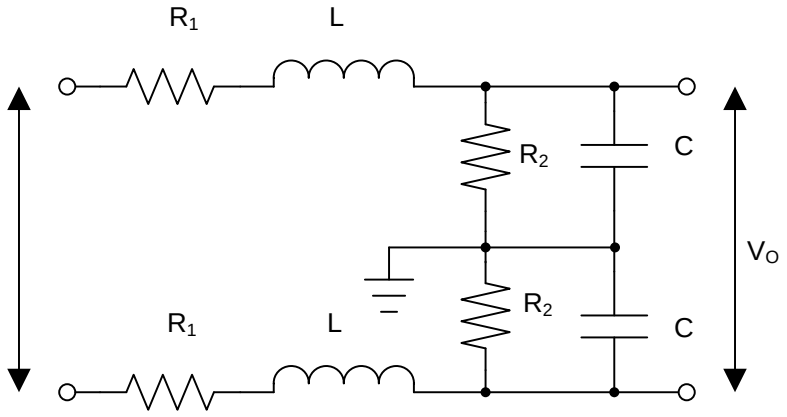


**Figure 9. Differential Low-Pass RLC Filter**

One important difference in understanding the operation of Figure 9 is to consider both the common-mode and differential-mode characteristics. For the differential signals, which matter most to the ADC input, this circuit is exactly the same as Figure 8 in that the midpoint ground for $R_2$ and C is transparent to the differential signal. The common-mode part of $V_I$ still experiences the DC load provided by $R_2$ and also has the same frequency response as the differential input signal.

Figure 10 shows a simpler solution for achieving DC biasing without common-mode filtering. In this diagram, the two-series capacitors are combined into one capacitor of equivalent series capacitance.

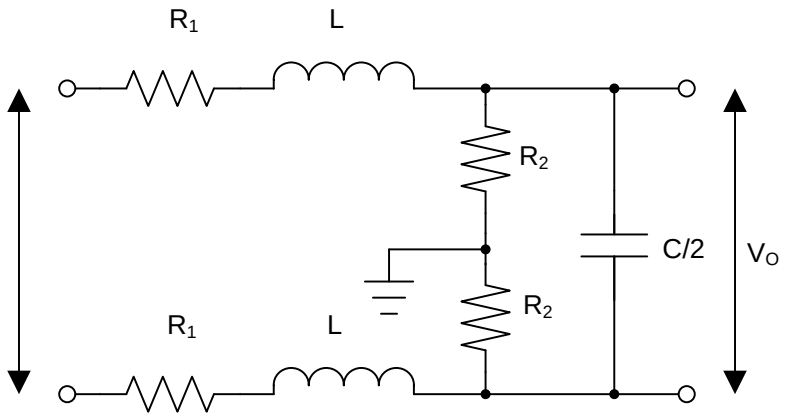


**Figure 10. Simplified Differential Low-Pass Filter**

The input common-mode signal still experiences a common-mode DC level shift through $R_2$, but now receives no filtering effect as a result of C. The differential capacitor now filters the differential signal and is transparent to any common-mode AC signal. This configuration is acceptable because $V_I$ only allows a limited presence of AC common-mode signal and modern differential input ADCs reject the common-mode very well over frequency.

In most cases an external capacitor C, as shown in Figure 10, designs the filter because the ADC internal capacitance specification is unknown. In some cases where the input capacitance of the ADC is known, this capacitor may be implemented by the input parasitic capacitance of the ADC itself and an external capacitor is not required. In other applications, the ADC input capacitance may exceed the requirement of the circuit in Figure 10. In that case, the alternate solution for L and C must be used to reduce the L but increase the C to the point where an implementation including the effect of the ADC input capacitance is possible.

The value of L and C have been modified such that standard available value of L and C can be used. A series 5-Ω resistor has been added before the ADC input. These resistors help with sampling glitch and damp out ringing caused by the package parasitic. Figure 11 shows the circuit with modified values and its transfer function. In the transfer function, the filter is providing a –2-dB attenuation in passband with a 19.5-MHz bandwidth.

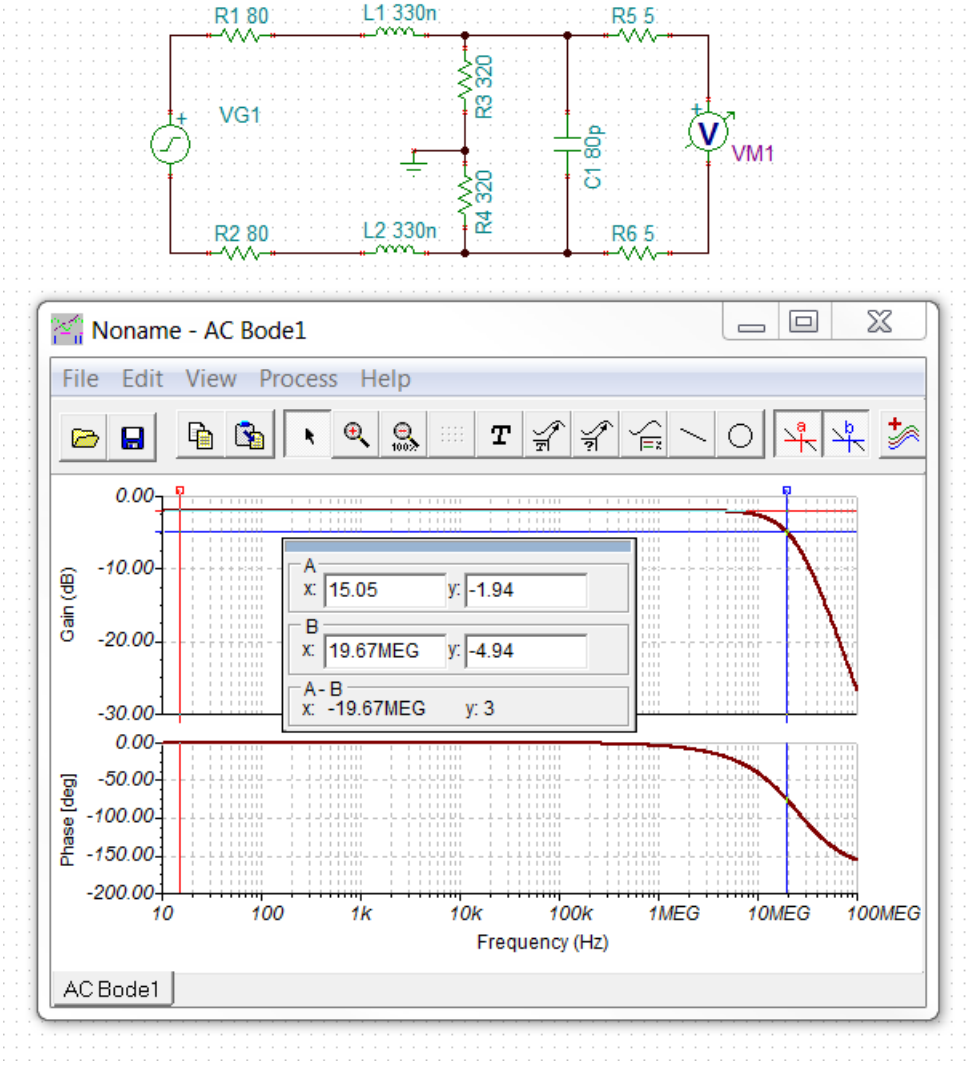


**Figure 11. Simulation Circuit and Transfer Function for RLC Low-Pass Filter**

Figure 12 is the simulation circuit for the single-ended-to-differential amplifier (THS4541) and the RLC low-pass filter. The ADC can accept an input common-mode voltage of 0.95 V ±0.025 V. As Figure 12 shows, the common-mode voltage at the ADC input is 0.96 V, which is within an acceptable range for the ADC.

Figure 13 shows the simulation of SNR performance for the THS4541 and RLC low-pass filter stages. Figure 13 also shows that the circuit in Figure 12 is capable of 90-dB SNR, so adding this stage does not impact the SNR of the ADC.

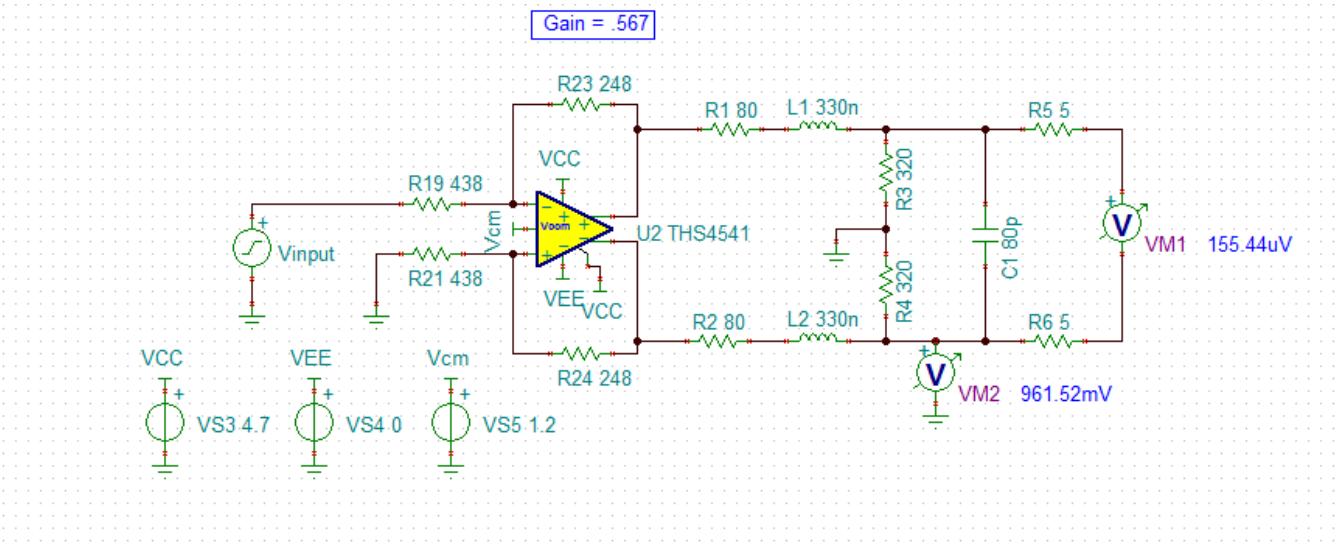


**Figure 12. Simulation Circuit Differential Amplifier With RLC Low-Pass Filter**

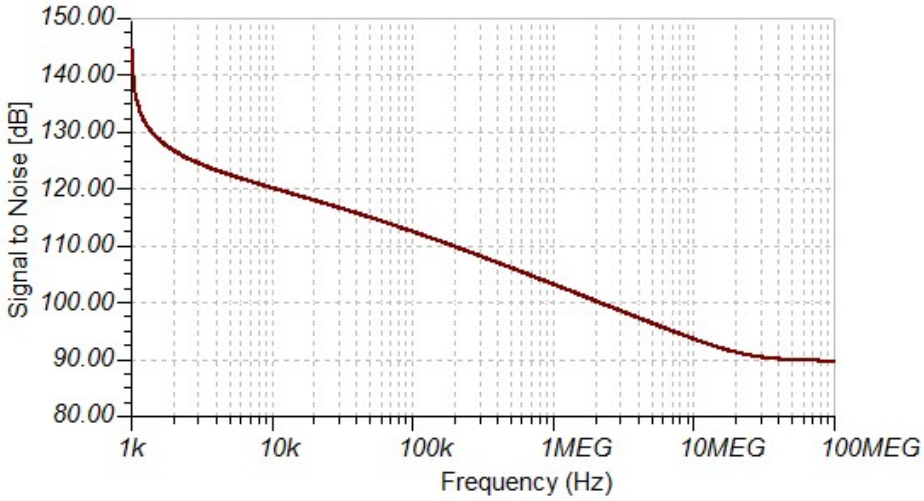


**Figure 13. SNR for Differential Amplifier With RLC Low-Pass Filter**

Figure 14 shows all three stages (OPA656, THS4541 and RLC low-pass filter) cascaded. Figure 15 shows the simulation of the SNR performance of the OPA656, THS4541, and the RLC low-pass filter stages. As Figure 15 shows, the input channel is capable of SNR at 80 dB, so the input channel does not significantly impact the SNR performance of the ADC.

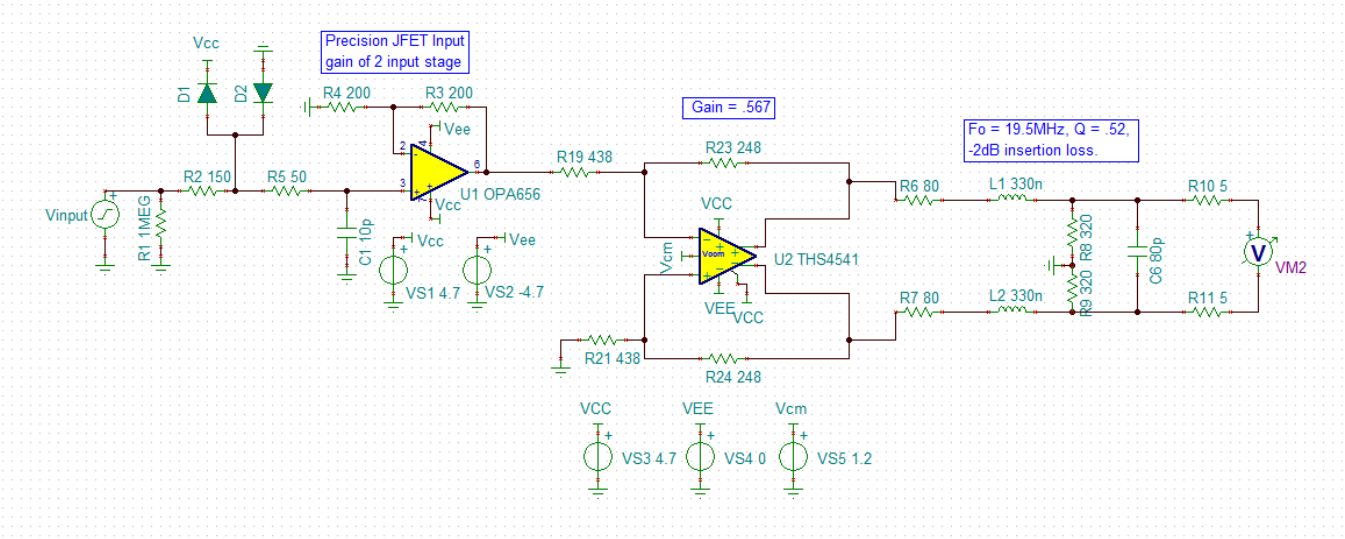


**Figure 14. Simulation Circuit for Complete Channel 3**

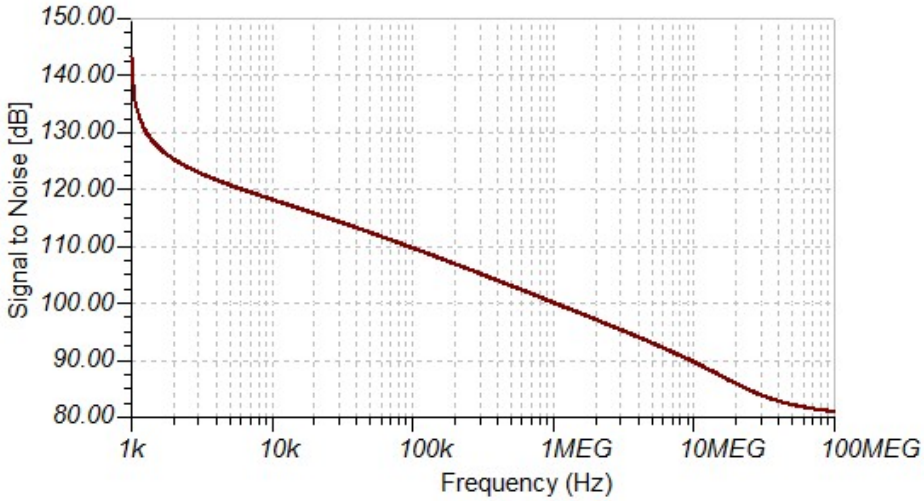


**Figure 15. SNR for Complete OPA656 (JFET), Differential Amplifier (THS4541) With RLC Low-Pass Filter**

The following Figure 16 shows the ±1-V input step (5-MHz square wave) and the correct differential amplitude of 1.8 $V_{P-P}$.

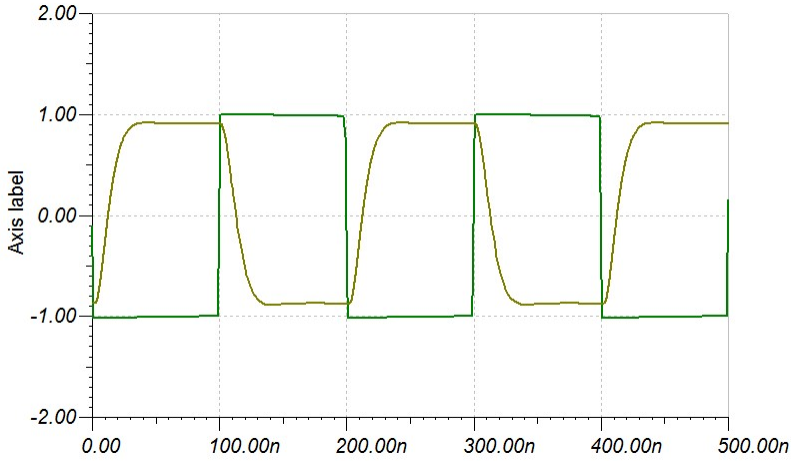


**Figure 16. Simulation With ±1-V, 5-MHz Input Square Wave**

## 6 OPA656, THS4541, and ADC3422 Results

The results for the implementation of the OPA656, THS4541, and ADC3422 devices show a good combined response. In a test where a clean filtered signal was fed into the combined circuit, the SNR was better than 70 dB, which is a slight degradation from the 70.6 dB of the ADC3244 device while using a transformer interface. The SFDR, as Figure 17 shows, is lower than expected. The SFDR is limited by the HD performance of the OPA656 device at a ±4-V output voltage swing parameter. Figure 18 shows the results when a 1-MHz ±1-V square wave has been applied at the input of channel 3. In summary, an active interface can be implemented using the OPA656 and THS4541 to drive the high performance requirements of the 12- and 14-bit ADC3xxx data converter family. For applications below 5 MHz, the 1-mA precision THS4551 FDA is a considerable option. For applications above 50 MHz, the 2.8-GHz, the low-noise LMH6554 FDA is a viable option.

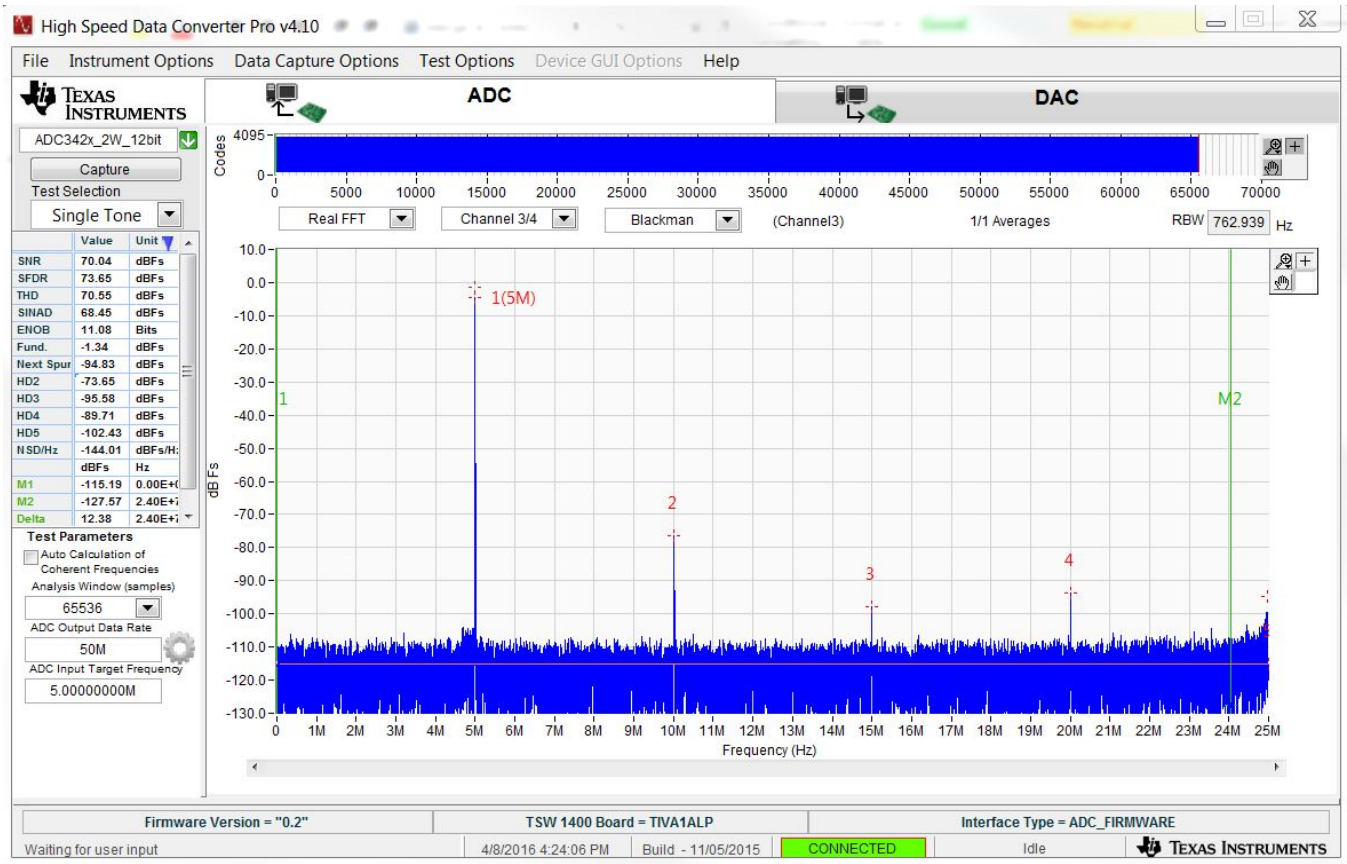


**Figure 17. FFT Performance of Combined OPA656, THS4541, and RLC Low-Pass Filter**

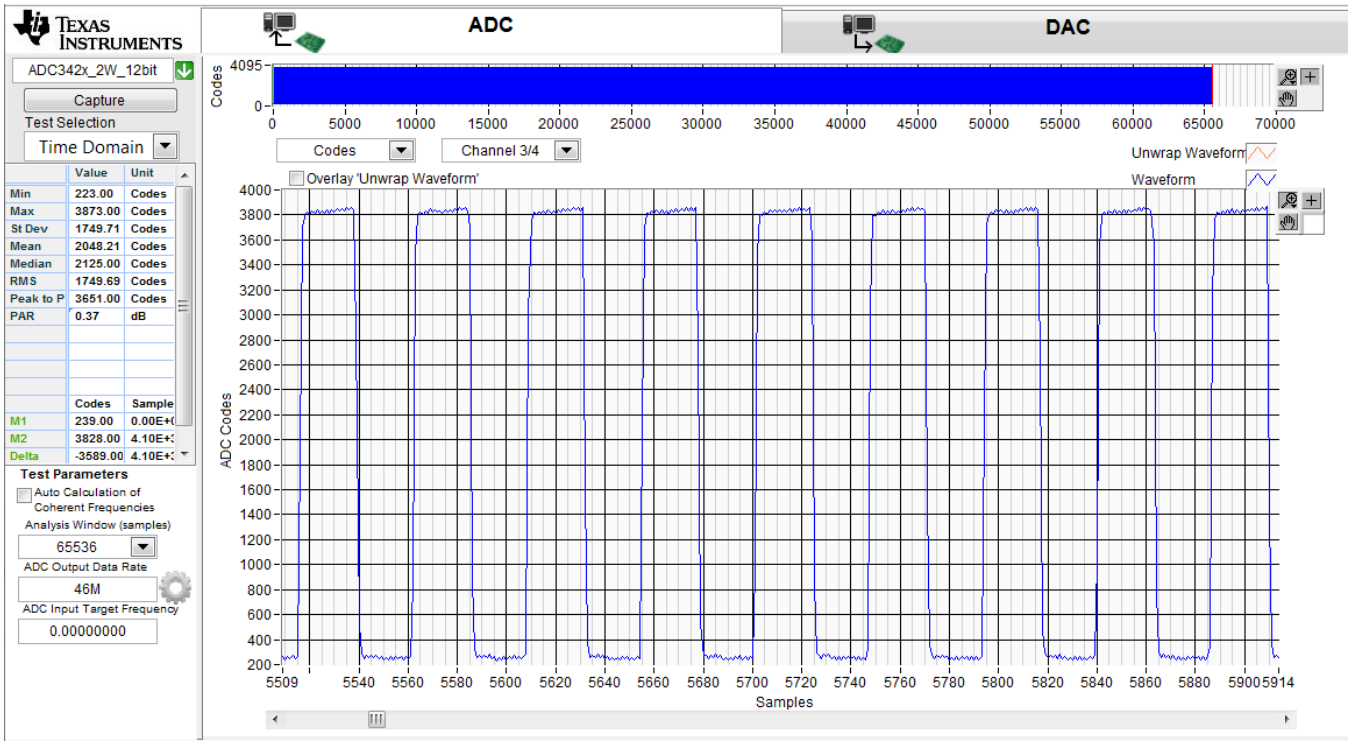


**Figure 18. 1-MHz, ±1-V Square Wave Input**

## 7 Channel 3 With Gain Redistribution Between OPA656 and THS4541 Stages

As the previous Section 6 shows, the SFDR performance is limited by the output swing parameter of the OPA656 device. The focus of this section is redistributing the gain through the OPA656 and THS4541 stages in such as way to improve the performance on HD2 and HD3. The overall gain of the path remains the same.

For this process, change the gain for the OPA656 stage from 2 V/V to 1.5 V/V. With the gain change, the OPA656 still accepts ±1 V at the input but outputs 3 $V_{P-P}$(max) instead of 4 $V_{P-P}$ to the FDA (THS4541). To implement the gain change in the circuit, update the values of R4 = 500 Ω and R3 = 250 Ω. The following Figure 19 shows the updated schematic.

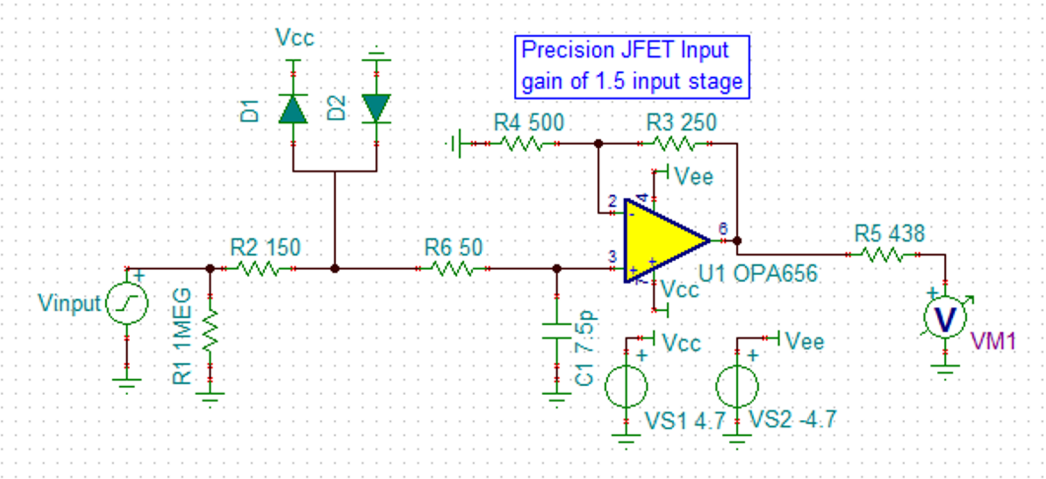


**Figure 19. Simulation Circuit for OPA656 With Updated Gain of 1.5 V/V**

To compensate for the lowered gain in the OPA656 stage, the gain for THS4541 must be increased (lower the insertion loss) to maintain the overall gain of the path, as in the preceding Section 6. Again, assuming a 2-dB insertion loss in the final RLC stage, the FDA stage must be designed for an insertion low of 2.5 dB or a gain of 0.750 V/V. Use Equation 11 to calculate the value of $R_F$ = 499 Ω and $R_{IN}$ = 665 Ω given the gain of 0.750 V/V. The following Figure 20 shows the updated schematic.

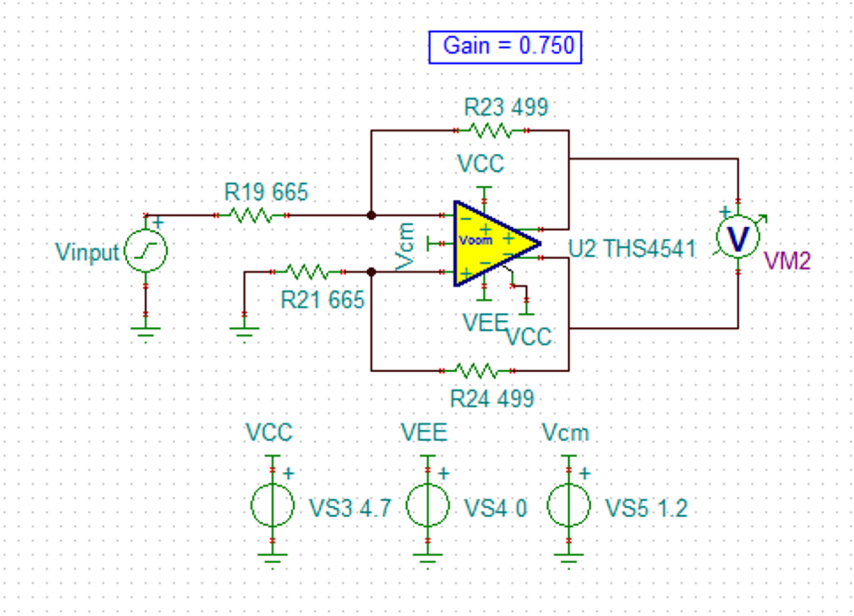


**Figure 20. Simulation Circuit for THS4541 With Updated Gain of 0.750 V/V**

### 7.1 OPA656, THS4541, and ADC3422 Results With Updated Gain

The results for updated gain for the OPA656, THS4541, and ADC3422 devices show a good combined response (see Figure 21). In this test a clean-filtered, 5-MHz single tone was fed into the combined circuit. The resulting SNR was 70.2 dB which is only a slight degradation in comparison to the 70.3 dB in the previous case; however, the SFDR improved by 6 dB. The HD2 improved by 6 dB and HD3 improved by 5 dB from a measured value of 95 dB. In summary, the SFDR performance can be improved by redistributing the gain through different stages without any significant reduction in SNR performance.

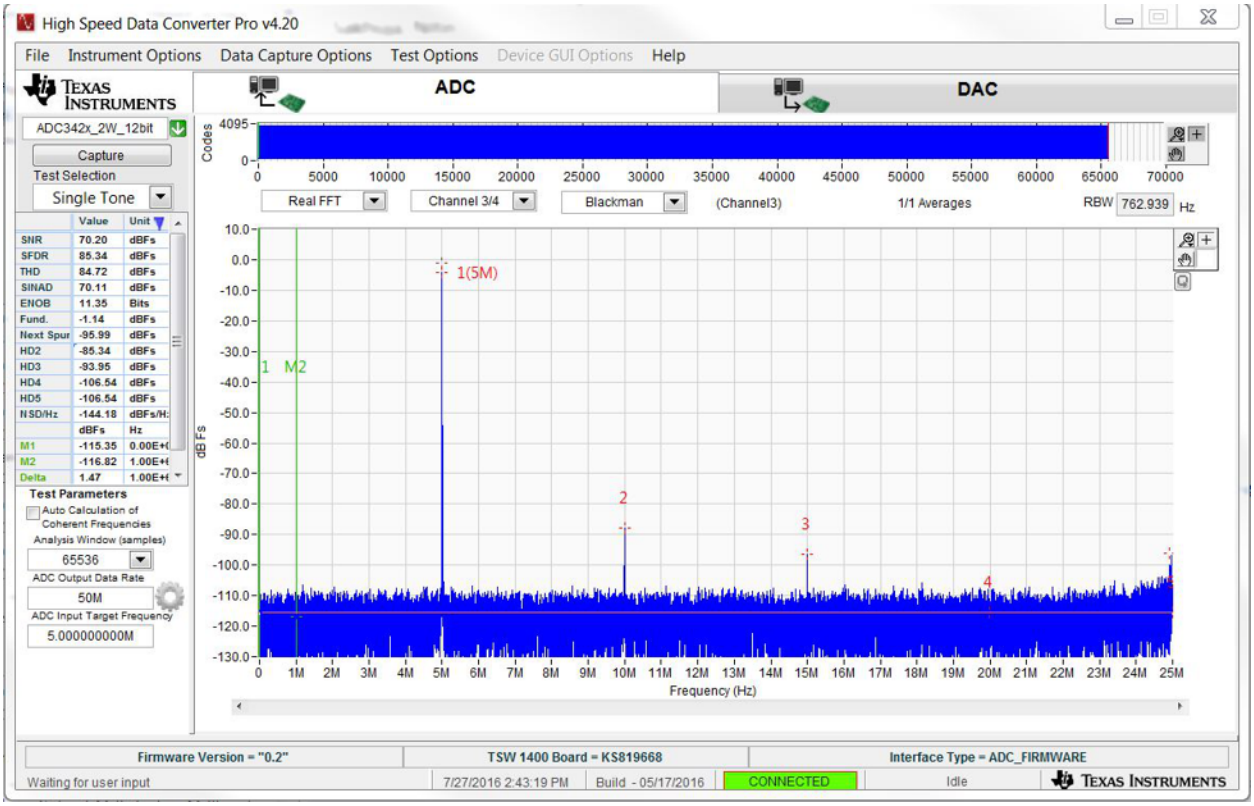


**Figure 21. FFT Performance of Combined OPA656, THS4541, and RLC Low-Pass Filter With Updated Gain**

# 8 Channel 3 With Gain Redistribution Between OPA656 and THS4541 Stages and Active Filtering on THS4541

This section addresses adding an active, second-order, multiple-feedback (MFB) low-pass filter stage as part of single-ended-to-differential (THS4541) amplifier design (see Figure 22). This stage provides a fourth-order Bessel filter for this path: two poles in the active MFB stage and two poles in the RLC low-pass filter stage.

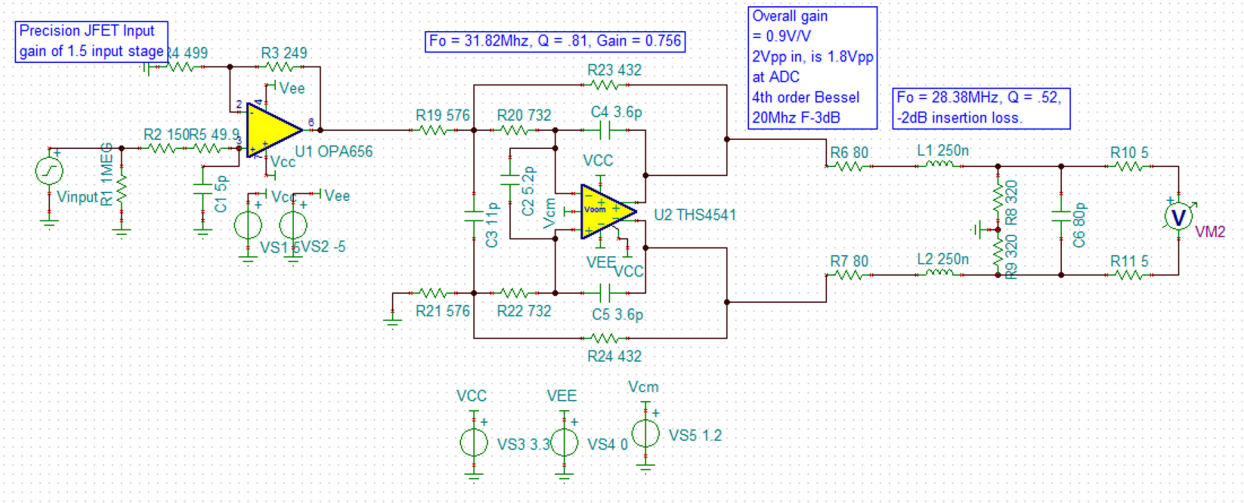


**Figure 22. Channel 3 With Active, Second-Order, MFB Low-Pass Filter Stage**

The schematic in Figure 22 shows that the precision JFET input stage is the same as the previous section and has a gain of 1.5 V/V. An active second-order filter with a cutoff frequency of 31.82 MHz is part of the single-ended-to-differential amplifier stage. The filter has been set up for a gain of 0.756 and a quality factor of 0.81. The passive low-pass filter stage is also the same as the previous section and has a cutoff frequency of 28.38 MHz and a quality factor of 0.52. As with the previous section, the input path has an overall gain of 0.9 V/V such that when inputting the 2 $V_{P-P}$ signal at JFET it becomes 1.8 $V_{P-P}$ by the time it reaches the ADC. For detailed information on how to design the active filter stage, view the *Design Methodology for MFB filters in ADC Interface Applications* application report [3].

The results for an active, second-order filter addition show a good combined response. In this test, a clean-filtered, 5-MHz single tone was fed into the combined circuit. The resulting SNR was 69.9 dB which is only a slight degradation in comparison to the 70.3 dB in the previous case; however, the SFDR shows a degradation of 3 dB. In summary, tests concluded that it is possible to implement the second active filter to provide a sharper filter response without much degradation of the overall performance (see Figure 23 and Figure 24).

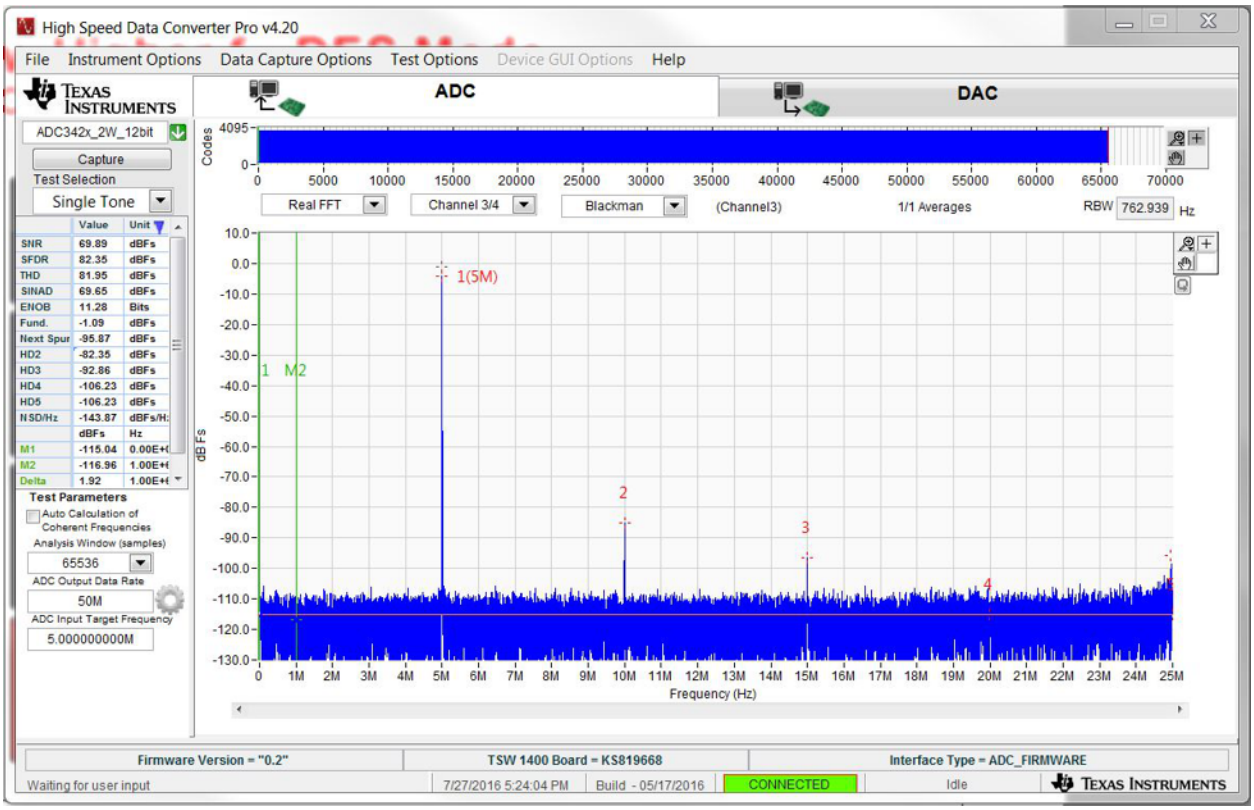


**Figure 23. FFT Performance of Combined OPA656, THS4541 With Second-Order Active Filter, and RLC Low-Pass Filter**

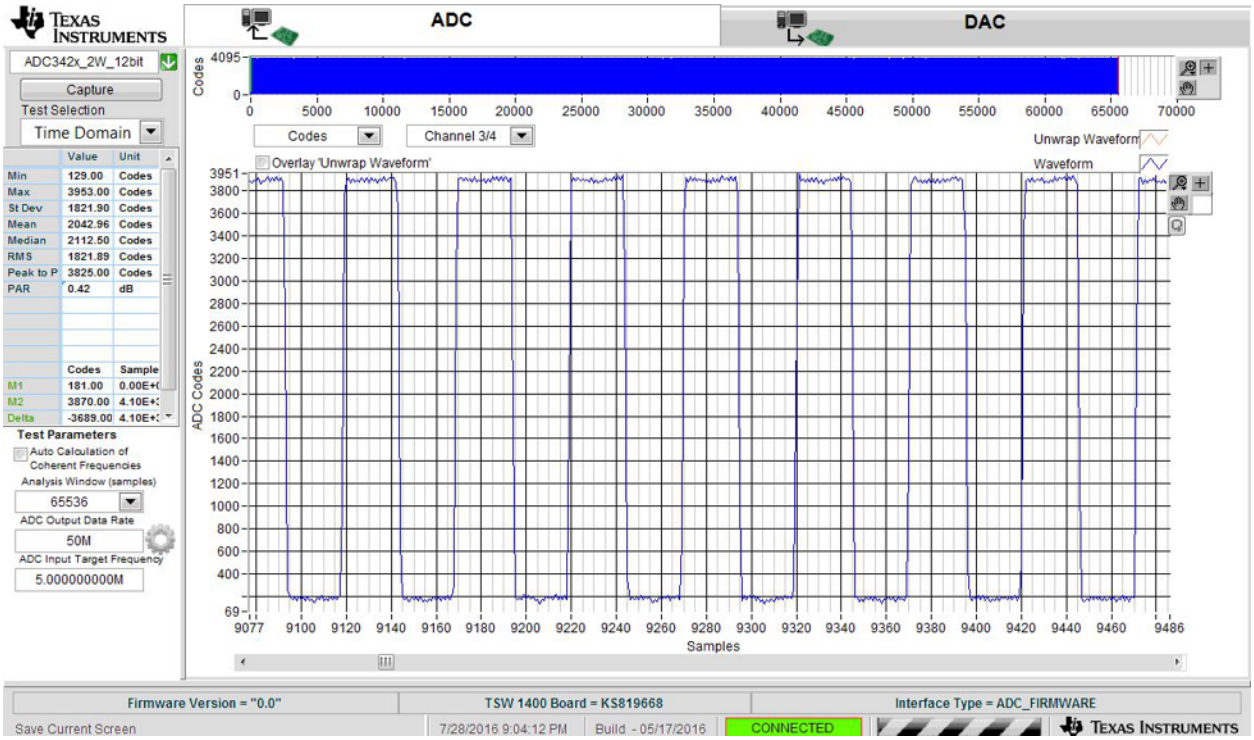


**Figure 24. 1-MHz, ±1-V Square Wave Input**

## 9 Channel 4—(Transformer)

Figure 25 shows the transformer-coupled input circuit of the ADC3422 ADC. Channel D has a dual, 1:1 impedance ratio transformer input circuit to achieve better phase and amplitude balance of the signal. The input termination is 50 Ω, which is formed by two 25-Ω resistors connected to the ADC $V_{CM}$ node.

Figure 26 shows the FFT for the transformer interface input path (channel 4). Channel 4 provides the SNR of 70.4 dB and SFDR of 87 dB.

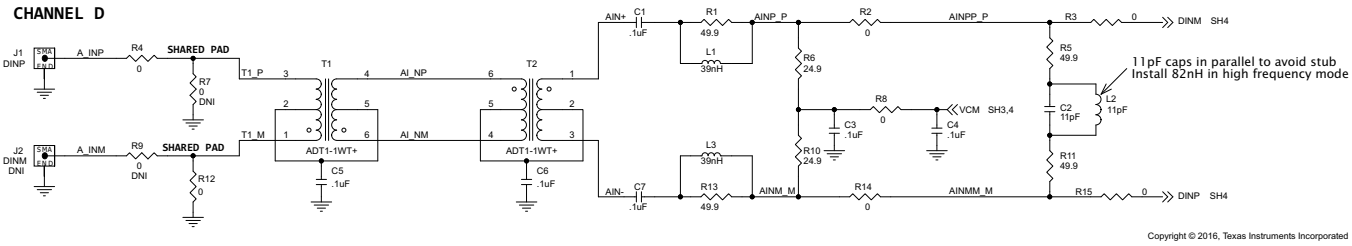


**Figure 25. Transformer Coupled Input (Channel 4)**

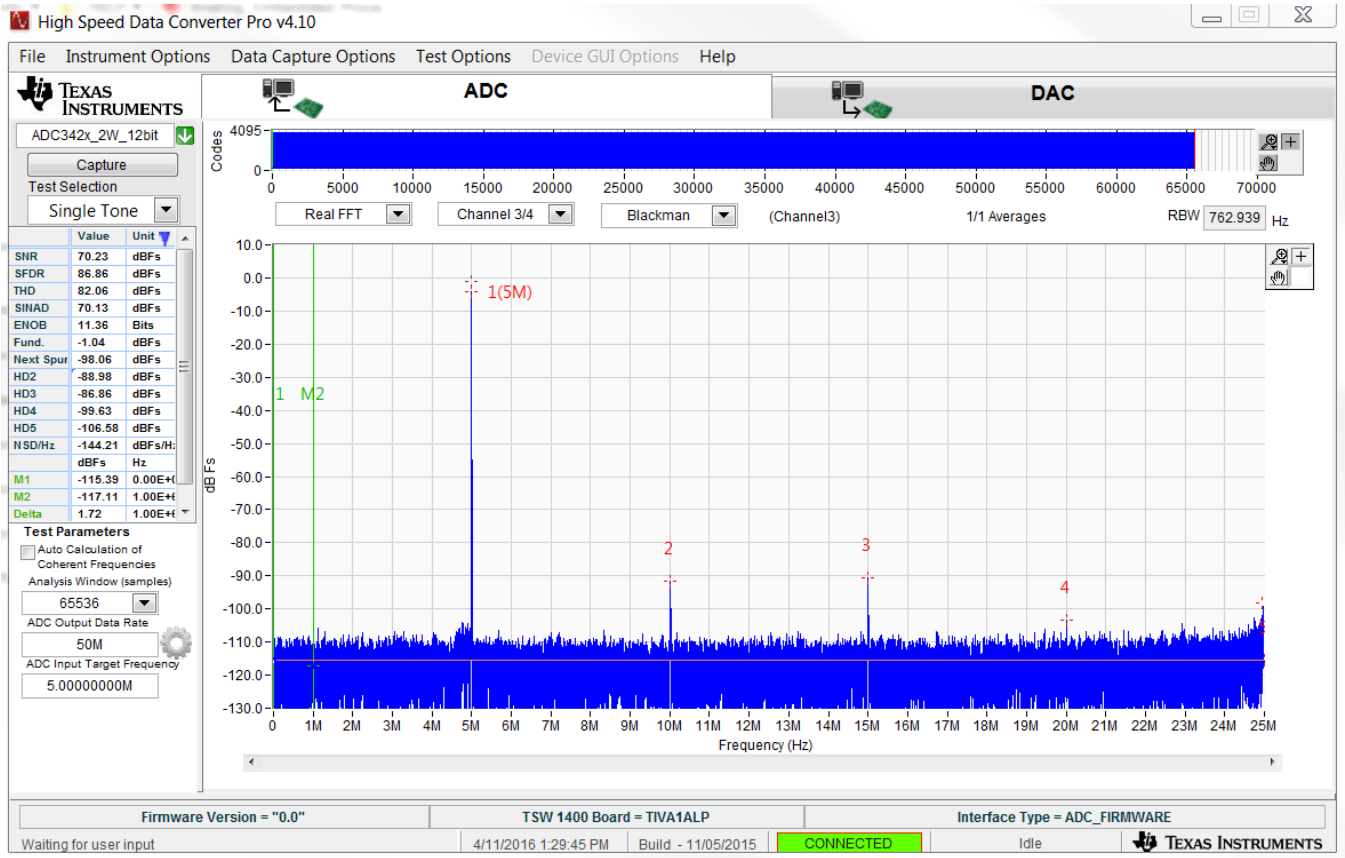


**Figure 26. FFT Performance of Transformer Input**

## 10 Power Supplies

The overall power supply networks for the TSW3422 is shown in Figure 27. The main rail for the entire EVM is a 5-V input through either a power brick connection to J14 or through test points TP2. The EVM design includes both DC-DC converters and low noise LDOs.

The ADC3422 requires 1.8 V for both analog (AVDD) and digital (DVDD) supply rails. The typical current for AVDD and DVDD is 71 mA and 56 mA, respectively. The TSW3422 board utilizes the TPS62234 (DC-DC converter), which is capable of providing 500 mA of current to convert from 5 V to 2.1 V. By using the TPS7A8300 LDO, this 2.1-V rail is brought down to 1.8 V.

An implementation of three THS4541 devices and one OPA656 device requires 4.7 V to power the combined positive supply rail ($V_{CC}$). The typical quiescent current for the THS4541 is 10.1 mA and the OPA656 requires 16.3 mA. The total current required for the 4.7-V rail is:
3 × 10.1 mA + 16.3 mA = 46.6 mA. For a 4.7-V supply rail, the TPS7A4901 is used to drop the voltage down from 5 V to 4.7 V and the device is capable of providing 150 mA of output current.

The OPA656 requires –4.7 V with 16.3 mA of current for its negative supply rail ($V_{EE}$). The TPS60403 converts 5 V to –5 V and then the TPS7A3001 delivers –4.7 V to power the $V_{EE}$ of the OPA656. Ferrite beads ($FB_x$) are added before each load to clean up high frequency signals.

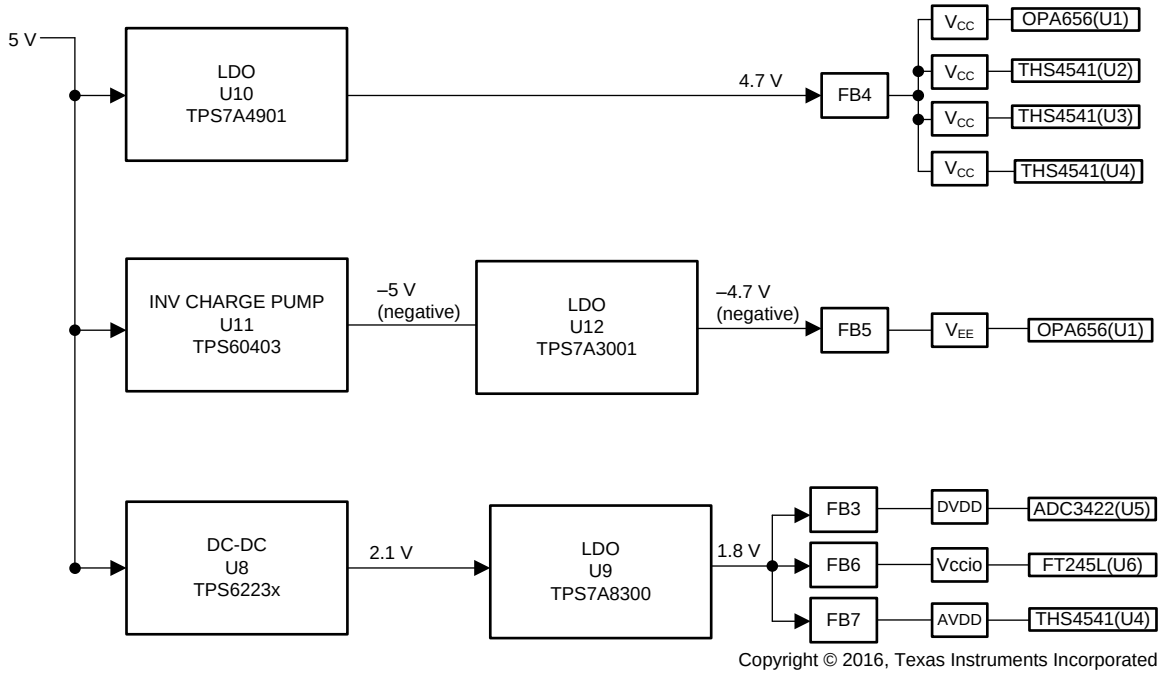


**Figure 27. Power Supply Tree**

# 11 Design Files

## 11.1 Schematics

To download the schematics, see the design files at TIDA-00799.

## 11.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00799.

## 11.3 PCB Layout Recommendations

To download detailed layout guidelines for each respective part, consult the respective data sheets.

### 11.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-00799.

## 11.4 Design Project

To download the design project files, see the design files at TIDA-00799.

## 11.5 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-00799.

## 11.6 Gerber Files

To download the Gerber files, see the design files at TIDA-00799.

# 12 Software Files

To download the software files, see the design files at TIDA-00799.

# 13 References

1. Texas Instruments, *THS4541 Negative Rail Input, Rail-to-Rail Output, Precision, 850-MHz Fully Differential Amplifier*, THS4541 Data Sheet (SLOS375)
2. Texas Instruments, *RLC Filter Design for ADC Interface Applications*, Application Report (SBAA108)
3. Texas Instruments, *Design Methodology for MFB Filters in ADC Interface Applications*, Application Report (SBOA114)
4. Texas Instruments, *High Performance Single Ended to Differential Active Interface for High Speed ADCs*, Reference Design (TIDU500)

# 14 About the Author

**NEERAJ GILL** is an Application Engineer in high speed catalog converters group at Texas Instruments. Neeraj received his BSEE from University of New Hampshire in 2011 and then his Masters in Electrical Engineering also from University of New Hampshire in 2013.

**KEN CHAN** is an Applications Engineer with the High Speed Products group. He has been working on communications and signal chain products for over 18 years. He received his B.Sc. and M.Sc EE from the University of Saskatchewan.

## Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Original (August 2016) to A Revision | Page |
|---|---|
| • Changed title from *Low-Power, Quad 12-Bit 50-MSPS ADC Reference Design With Low-Noise, Low-Distortion DC and AC Inputs* to *Quad-Channel, 12-bit, 50-MSPS ADC Reference Design With Low-Noise, Low-Distortion, DC and AC Inputs* | 1 |

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