TI Designs: TIDEP-0067

66AK2Gx DSP + ARM Processor Power Solution Reference Design

TI Designs

This TI Design is a power reference platform based on the K2G Multicore DSP + ARM® System-on-Chip (SoC) and companion TPS65911x power management integrated circuit (PMIC). This power solution design also includes the first stage buck converters to support a 12-V input and the DDR termination regulator for DDR3L memory. The reference design is tested and includes hardware reference (EVM), software (Processor SDK) and test data.

Design Resources

TIDEP0067	Tool Folder Containing Design Files
66AK2G12	Product Folder
TPS65911	Product Folder
TPS54620	Product Folder
TPS54429	Product Folder
K2G General Purpose EVM	EVM Tool Folder
K2G 1GHz GP EVM	EVM Tool Folder
Processor SDK for K2G	Download Software

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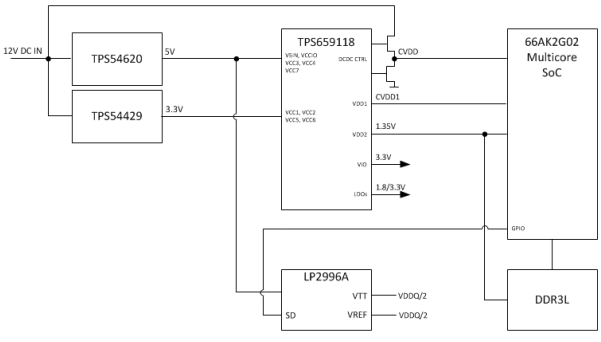
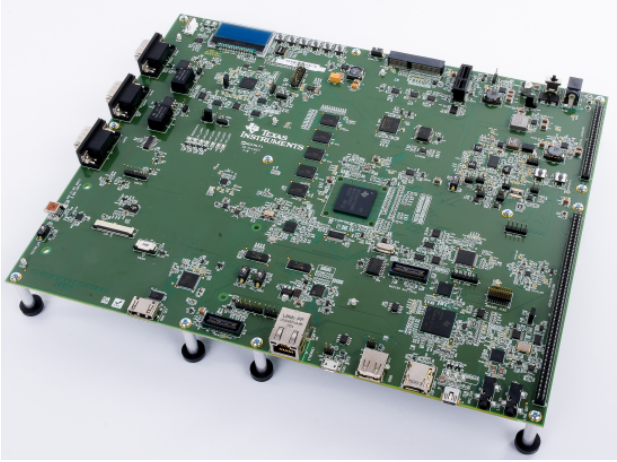
Features

- TPS54620 and TPS54429: The First Stage Buck Converters to Convert a 12-V input to 3.3-V and 5-V Outputs.
- TPS65911x Companion PMIC Supporting Power Sequencing and Power Supplies Required for the SoC and DDR3L Memory.
- The TPS65911x Offers an Integrated Real-Time Clock (RTC) for Time-Critical Applications.
- LP2996A DDR3L Termination Regulator.

Applications

- Automotive Audio Amplifiers
- Home Audio
- Professional Audio
- Power Protection





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1 Introduction

This TI Design is a power reference platform based on the K2G Multicore DSP + Arm® System-on-Chip (SoC) and companion TPS65911x power management integrated circuit (PMIC). This power solution design also includes the first stage buck converters to support a 12 V input and the DDR termination regulator for DDR3L memory. The reference design is tested and includes hardware reference (EVM), software (Processor SDK) and test data.

2 K2G GP EVM Power Solution Block Diagram

The first stage buck converter devices TPS54620 and TPS54429 convert the 12-V DC input of the EVM to 5 V and 3.3 V respectively. The 5-V output from the TPS54620 provides the inputs to TPS65911x and LP2996A. The 3.3-V output form TPS54429 provides the input to TPS65911x, and 3.3-V peripheral devices on the EVM. TPS65911x provides all power supplies required for the 66K2Gx Multicore SoC, except for the 3.3-V I/O power supply.

Figure 1 shows the block diagram of the power solution on the K2G GP EVM.

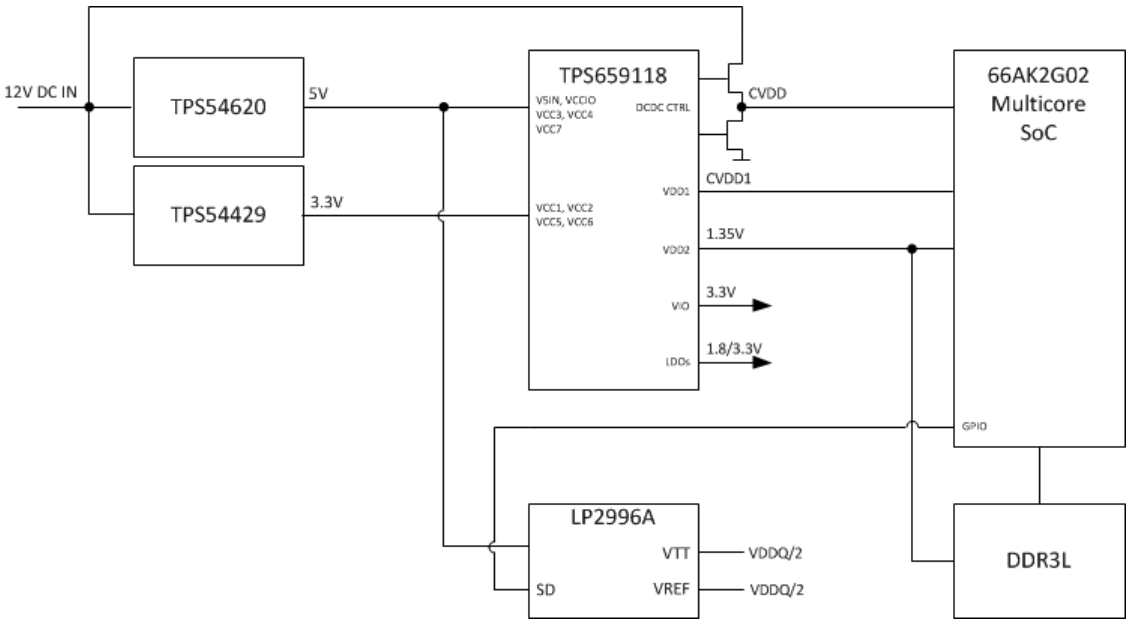

Figure 1. K2G General Purpose EVM Power Solution Block Diagram

3 K2G EVM Overview

The K2G GP EVM is intended to exercise the key interfaces on the K2G device. The K2G GP EVM includes the following features:

- Memory
  - 2 GB of DDR3L with ECC (32-bit data + 4-bit ECC)
  - 512 Mbit of QSPI Flash
  - 2 Gbit of NAND Flash
  - 128 Mbit of SPI Flash
  - 128 kByte of 12C EEPROM for Boot support from 12 C
  - 16 GByte eMMC
  - Micro-SD Card slot (32 GB micro-SD card included)
- Connectivity
  - Gbit Ethernet: RGMII through Micrel KSZ9031 PHY RJ45 jack
  - USB 2.0 × 2: Micro A/B connector, Host connector
  - PCIe Gen 2: Single lane card slot (root complex only)
  - COM8 connector for use with WiLink 8 modules
- Display
  - 4.3" Touch LCD display (sold seperately)
  - HDMI Tx
- Audio
  - AIC3106 stereo code
  - 3.5 mm stereo jack ×2 supports stereo analog input and output
  - All McASP signals routed to audio expansion connector
- General Purpose Serial
  - SPI and 12C ports not already used for memory, or control are routed to serial expansion connector
  - UART through RS232 chip and DB9 connector, UART over USB
- Automotive
  - MLB supported through expansion connector
  - DCAN supported through transceivers, DB9 connectors
- Emulation
  - Onboard XDS200 through mini-USB connector
  - MIPI-60 header for external emulators
  - TRACE is supported with some caveats (resistor-muxed with display signals)
- Power
  - Provided through TPS65911x PMIC – factory-programmed with K2G power-up sequence
    - 3 step-down DC–DC converters
    - 8 LDOs
    - 12C and enable signals
- Board Management Controller
  - Mainly intended for automated testing; not intended for end-products
  - May control boot modes, power-up, and more
  - Character display for system status
- Clocking
  - K2G is unique among K2 devices because the K2G generates most clocks internally, including audio frequency clocks. DDR, USB, Ethernet, and more. Clocks may be generated internally. This is the default mode on the EVM.

– A CDCM6209 is also included and generates SYSCLK, DDR ref clock, USB clcok, and PCIe clock.

Figure 2 shows the K2G general purpose EVM.

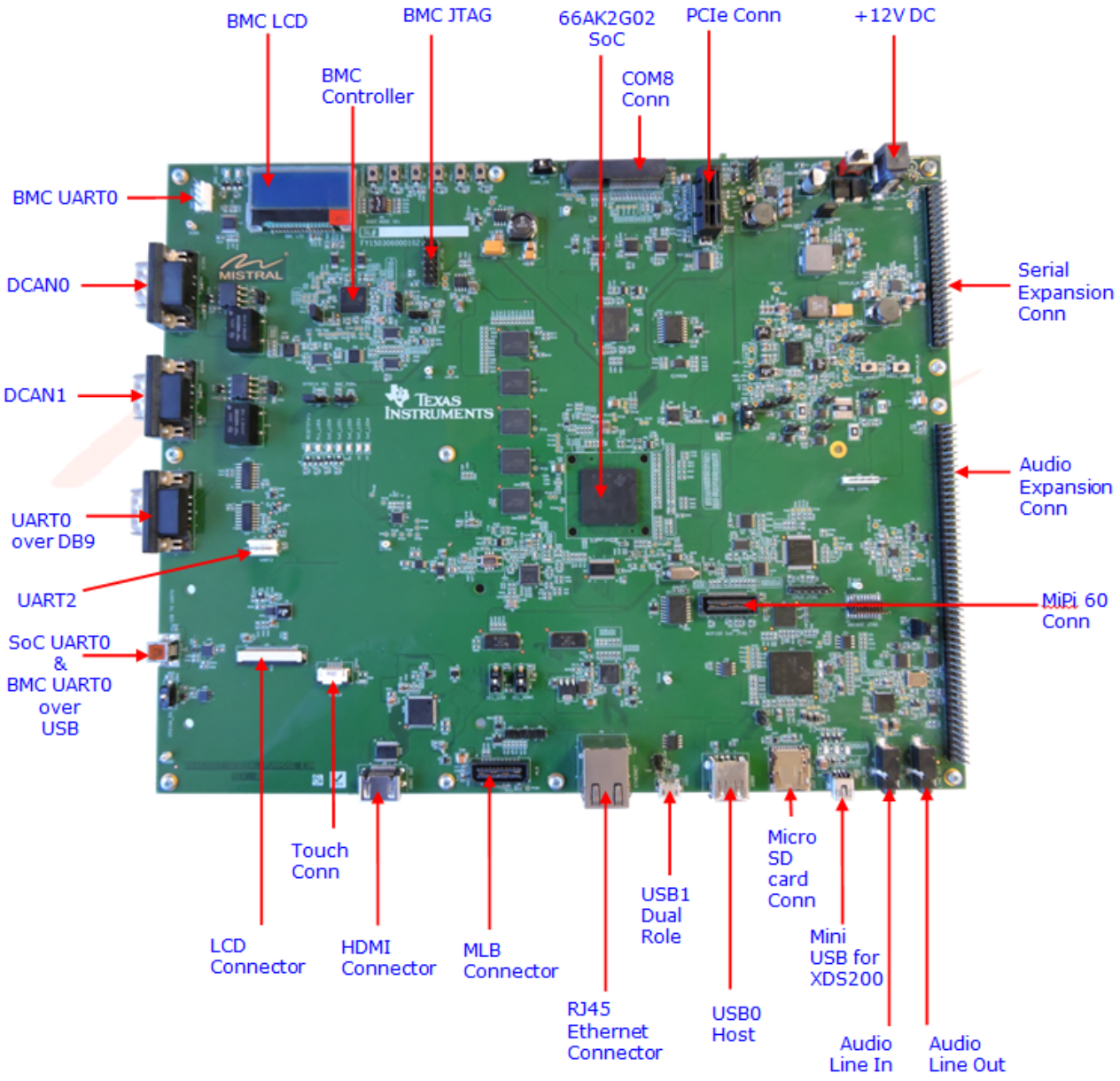

Figure 2. K2G General Purpose EVM

4 Software

Software for the K2G EVM is available by downloading the Processor SDK.

5 K2G EVM

The 66AK2Gx SoC supports the following features:

- Processor Cores and Memory
  - ARM Cortex A15 up to 1000 MHz
    - 32 KB L1D, 32 KB L1P, 512 KB, L2 cache
  - C66x DSP up to 1000 MHz
    - 32 KB L1D, 32 KB L1P, 1 MB L2
  - ECC on all memory
- Industrial and Control Peripherals
  - 2 Industrial Communication Subsystems enable cut through, real-time and low latency industrial Ethernet protocols
  - Programmable real-time I/O enables versatile field bus and control interfaces
- Security and Crypto
  - Standard secure boot with customer programmable OTP keys
  - Crypto
  - Package
    - 21 × 21 mm, 0.8-mm pitch BGA 625 pins

Figure 3 shows the 66AK2G12 diagram.

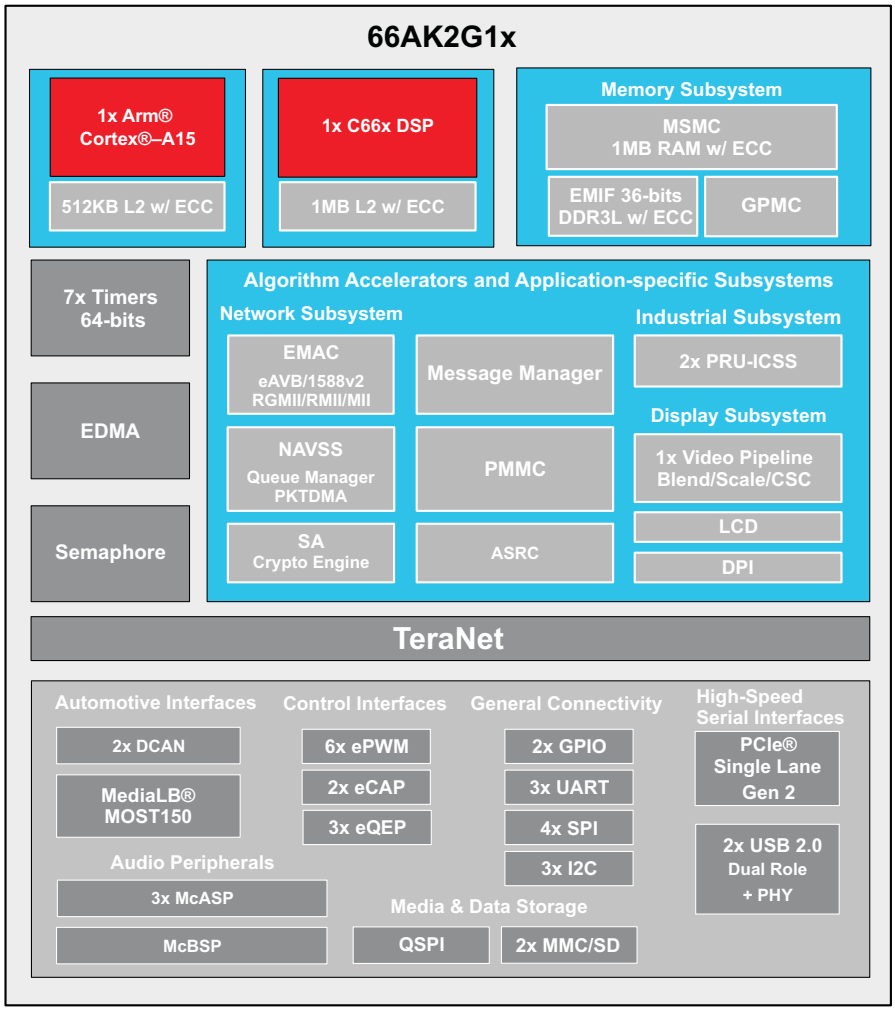

Figure 3. 66AK2G12 Diagram

6 TPS65911x Power Management Integrated Circuit (PMIC)

The TPS65911x is an integrated power management IC configured to operate with the 66AK2Gx SoC, combining three switch-mode buck converters, one switch-mode buck controller, and 8 linear regulators into a single BGA package. The PMIC handles power-supply sequencing and reset conditions, provides GPIO outputs for enabling external regulators or switches, and accepts i2c instructions from the processor for features such as voltage scaling and interrupt masking of various event or fault notifications. The TPS659118 is optimized to power a 66AK2G02 system, utilizing a one-time-programmable (OTP) memory configured with boot voltages, power sequencing, and other default conditions. The TPS65911A is optimized to power a 66AK2G12 system. The PMIC and processor must be connected correctly in order to meet the defined voltage, current, and sequencing requirements of the processor. A detailed lock diagram of the power management solution for the 66AK2Gx using the TPS65911x is shown in Figure 4. The *TPS659118 User's Guide to Power 66AK2G02* (SWCU176) describes these connections, as well as the OTP settings defined within the PMIC. The *TPS65911A User's Guide to Power 66AK2G12* (SWCU176)

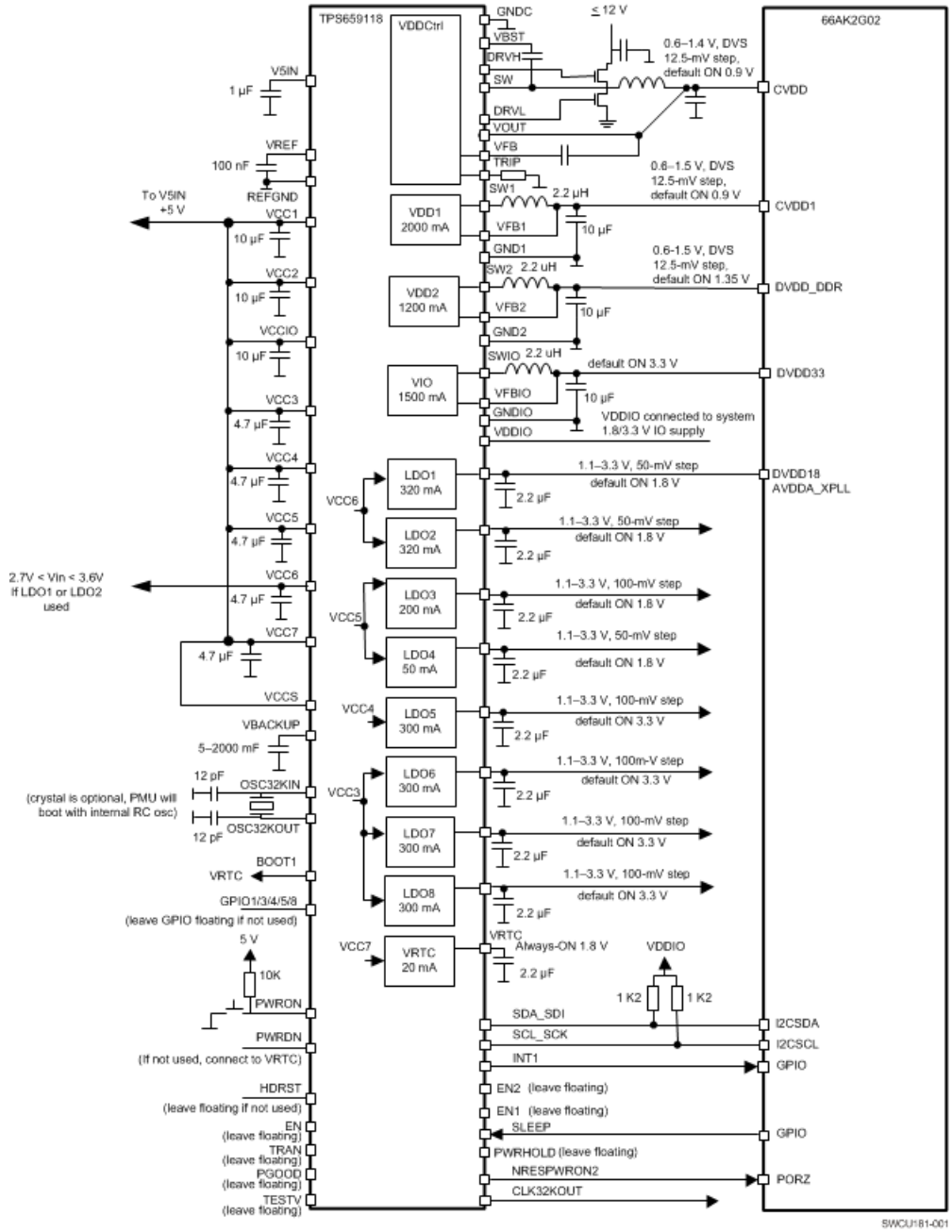

Figure 4. TPS659118 PMIC with 66AK2G02

7 Test Data

7.1 Power-Up Sequence Specification

Figure 5 shows the TPS65911x power-up sequencing timing.

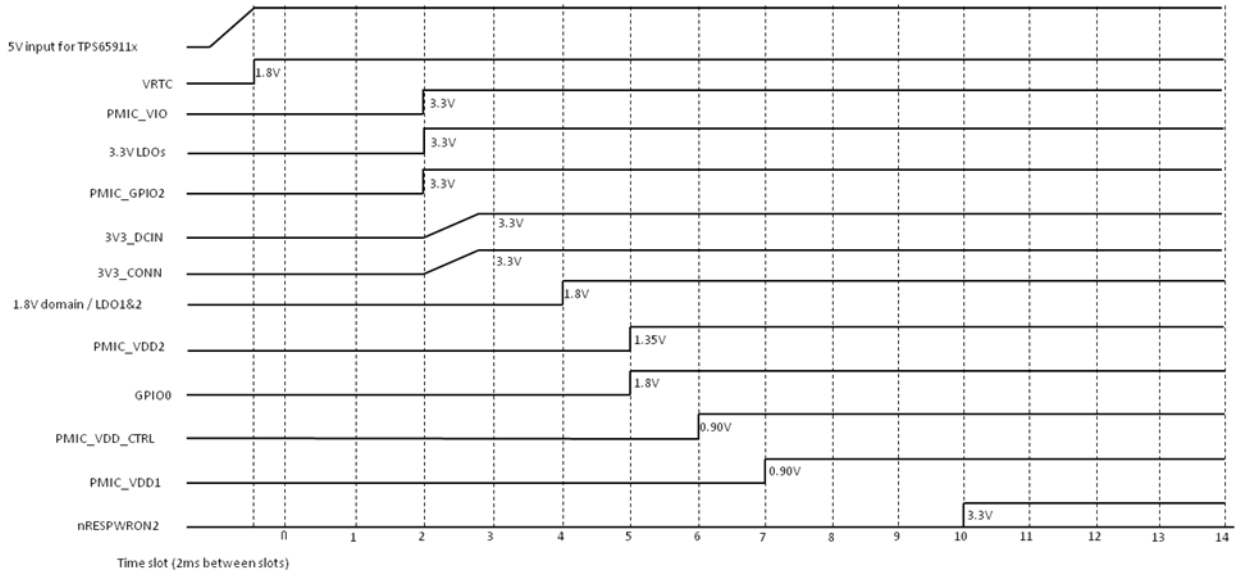

Figure 5. TPS65911x Power Sequencing

7.2 Power-Up Sequence Waveforms

The following waveforms demonstrate the power-on of the TPS65911x as required by the 66AK2Gx.

Figure 6 shows the power-on sequence for each of the output voltage rails and nRESPWRON2 signal respectively. The 3.3 V, 1.8 V, 1.35 V, CVDD, and CVDD1 rails turn sequentially and the nRESPWRON2 signal goes *HIGH* after all rails are *ON*.

Figure 6. Power-On Sequence for the TPS65911x

Table 1 lists the delay time for the 3.3 V, 1.8 V, and 1.35 V processor power supplies.

Table 1. Delay Time for the 3.3 V, 1.8 V, and 1.35 V Processor Power Supplies

PLOT	EXPECTED TIMING	ACTUAL TIMING
1 to 2	N/A	10.0 ms
2 to 3	4.0 ms	4.0 ms
2 to 4	6.0 ms	6.0 ms
3 to 4	2.o ms	2.0 ms

Figure 7 shows the power-on sequence for the TPS65911x with nRESPWRON2.

Figure 7. Power-On Sequence for the TPS65911x With nRESPWRON2

Table 2 lists the delay time for the CVDD and CVDD1 processor power supplies and power on reset (POR) signal.

Table 2. Delay Time for the CVDD and CVDD1 Processor Power Supplies and Power On Reset (POR) Signal

PLOT	EXPECTED TIMING	ACTUAL TIMING
1 to 2	N/A	18.4 ms
2 to 3	2.0 ms	2.0 ms
2 to 4	8 ms	8.0 ms
3 to 4	6 ms	6 ms

Figure 8 shows the 3.3 V VIO buck converter, 3.3 V LDO5 and 1.8 V LDO1 of the TPS65911x. The 3.3 V PMIC_VIO buck converter and the 3.3 V_LDO turn *ON* simultaneously.

Figure 8. Power-On Sequence for the TPS65911x Voltage Rails

8 Design Files

To download the design files for TIDEP0067, see the design files at http://www.ti.com/tool/TIDEP0067.

8.1 Trademarks

Arm is a registered trademark of ARM Limited.

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (May 2016) to A Revision	Page
• Added 66AK2G12 Product Folder.	1
• Added link to EVMK2GX Tool Folder (1GHz K2G GP EVM).	1
• Changed "at 600 MHz" to "up to 1000 MHz" for both Cortex-A15 and C66x cores.	5
• Changed 66AK2G02 block diagram to 66AK2G12 block diagram.	6
• Added distinction between TPS659118 and TPS65911A.	7

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