

TI Designs

9.8-GHz RF CW Signal Generator Using Integrated Synthesizer Reference Design With Spur Reduction



TI Designs

The TIDA-00626 is a 9.8-GHz wideband, low phase noise, integrated CW RF signal generator with a versatile spur reduction technique. The output level can be programmed from -31.5 to 9.4 dBm in 0.5 -dB steps. This signal generator can be used as a local oscillator for applications such as analog and vector signal generators and can also be used as a clock generator for RF ADCs. The TIDA-00626 can be controlled from any PC through the TI USB2ANY interface and also using the microcontroller MSP430F5529 LaunchPad™.

Design Resources

TIDA-00626	Design Folder
LMX2592	Product Folder
LP38798	Product Folder
LMK61E2	Product Folder
LM2776	Product Folder
TPS61170	Product Folder
SN74AHCT244	Product Folder
MSP-EXP430F5529	Tools Folder



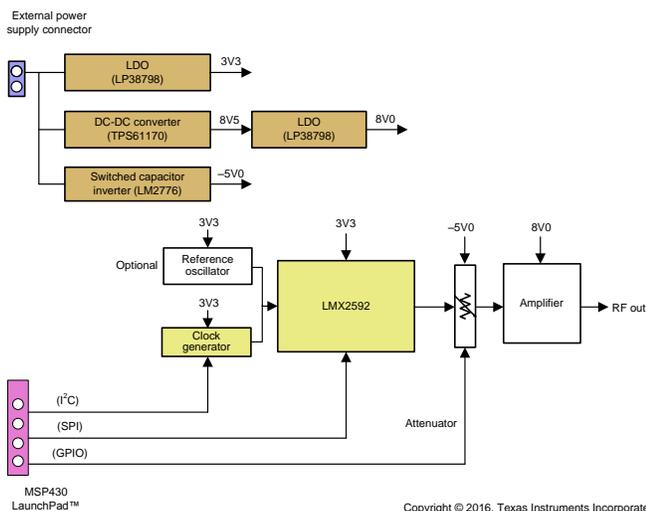
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Design Features

- Integrated Wide Band Frequency Synthesizer With Output Range of 0.02 to 9.8 GHz
- Excellent Phase-Noise Performance Synthesizer Phase Noise at 6 GHz
 - -111 dBc/Hz at 100-kHz offset
 - -133 dBc/Hz at 1-MHz offset
- Low Noise Synthesizer
 - In-Band Spurs (-75 dBc)
- Programmable Output Level -31.5 to 9.4 dBm in 0.5 -dB Steps
- Fine Output Frequency Resolution of 0.05 Hz
- Versatile Boundary Spur Reduction Using LMK61E2

Featured Applications

- Test and Measurement
- Wireless Communications
- Military, Aerospace
- Radar Detector
- Microwave Backhaul



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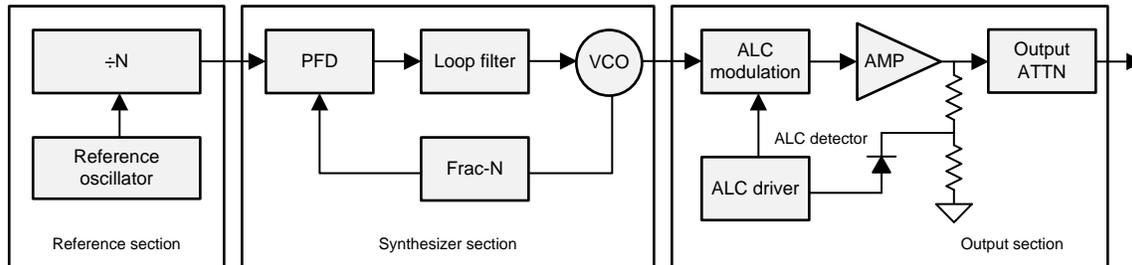
1 Key System Specifications

Table 1. Key System Specifications

PARAMETER	SPECIFICATION
Frequency range	20 MHz to 9.8 GHz
Frequency step size	0.05 Hz
Output maximum amplitude	9.4 dBm at 3 GHz
Output range	-31.5 to 9.4 dBm
Input reference frequency	5 to 1400 MHz
Phase noise maximum	-107.1 dBc/Hz at 9.8 GHz at an offset of 100 kHz
Non-harmonics spur	-75 dBc
Lock time	1 ms
Current consumption	750 mA at 5-V input

2 System Description

Signal generators are instruments that generate repeating or non-repeating signals used to develop, troubleshoot, and repair electronic or electroacoustic devices. Figure 1 shows the block diagram of an analog signal generator. An analog signal generator has a reference section to provide reference to the synthesizer. The synthesizer is a phase locked loop (PLL), which generates RF frequencies, and the output section is generally used to improve the dynamic output power range.



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Figure 1. Analog Signal Generator Block Diagram

RF signal generators are used in RF microwave laboratories to help develop RF systems and used for testing components, receivers, and systems in a wide variety of applications including cellular communications, Wi-Fi, WiMAX, GPS, satellite communication, radar, and electronic warfare. RF signal generators are also widely used in electronic manufacturing centers, service centers, and institutions of education. A signal generator has different variants available in the market including benchtop, modular PXI, modular USB, handheld, or portable.

The TIDA-00626 is a 9.8-GHz wideband, low phase noise, integrated continuous wave (CW) RF signal generator that uses a versatile spur reduction technique. The output level can be programmed from -31.5 to 9.4 dBm in 0.5-dB steps. The signal generator can be used as a local oscillator for analog or vector signal generators and could also be used as a clock generator for RF ADCs. This TI Design can be controlled from any Windows PC through a USB2ANY interface or by using the microcontroller MSP430F5529 LaunchPad or any similar controller. This TI Design is a good example for USB-based signal generators, modular signal generators, and handheld or portable signal generators where power, size, and cost are the key selection requirements.

An overall signal generator specification imposes significant requirements on size, power dissipation, voltage requirements, cost, and spectral purity. Of all the requirements, phase noise and noise across band such as spur are the most challenging to the designer. Phase noise is an indicator of the signal quality. An ideal signal spectrum representation shows its total energy is concentrated in a singular frequency. However, the real signals have a spectral distribution, and their energy is spread. The better the signal quality, the higher the energy concentrated close to the carrier. Phase noise is the measure of statistical spectral density measured relative to the signal's total power. A spur is the measure of the discrete, deterministic, periodic interference noise in the signal spectrum. Spurious signals are part of the signal's noise spectrum and represent any discrete spectral line not related to the signal itself. In a system, there are spurs due to various reasons; see the LMX2592 datasheet ([SNAS646](#)) for spur definitions and mitigation techniques.

The spurs in the synthesizer output are defined in the "Spur Definition Table" in the LMX2592 datasheet ([SNAS646](#)). The reference-VCO spur signal is the prominent spur that arises in the following manner. When in lock, the integer-N circuit's phase detector (being a digital part with limited speed) generates fast spikes that will leak and modulate the VCO control line, generating spurious signals at the reference frequency and its harmonics. The spikes are short, usually in the 1-ns range, thus generating a spectrum of lines with reference frequency being the first and the hardest to filter. Harmonics of the line will also appear if not filtered sufficiently. Higher harmonics are usually filtered out by the loop response.

The next prominent spur is the integer boundary spur (IBS). IBS arises, for example, if the desired output signal is 6001 MHz for a reference frequency of 100 MHz. The N divider value is 30.005. The fractional part results in a 500-kHz spur away from integer boundary.

The TIDA-00626 provides solution to mitigate the reference spur and IBS. This TI Design also reduces the system complexity in terms of size, power, and cost. Any spur due to OSCin can be reduced by using a programmable clock generator as reference. IBS can be reduced by the LMX2592 internal doubler and dividers or by adjusting the reference with programmable clock generator. This TI Design uses the LMK61E2 ultra-low noise programmable reference clock to reduce the spurs without affecting the integrated noise of the LMX2592. The LMK61E2 has an internal loop filter, which can be programmed to make the noise level to the acceptable limit. The device has very low phase noise, and a wide output range; therefore, this TI Design uses the LMK61E2 as a reference for LMX2592 to reduce spur.

3 System Design Theory

The system consists of an integrated synthesizer with a reference generated by a programmable clock generator. The output stage consists of an attenuator and RF amplifier to maintain the power level across the band and vary the power level. This TI Design also has a complete low-noise solution for the power supply.

The spur due to OSCin coupling is reduced with a programmable clock rather than a fixed oscillator as reference. Due to the VCO OSCin coupling, spurs that appear at an integer (for example, 1, 2, 3, 60, and 61) multiply the PLL reference frequency. For example, if the reference frequency is 100 MHz, there will be spurs at 100 MHz, 200 MHz (second harmonic), 300 MHz (third harmonic), 6000 MHz (60th harmonic), 6100 MHz (61st harmonic), and so on. If the desired output signal in a system is 6001 MHz, then there will be a spur at 6000 MHz that will appear at a 1-MHz offset from the desired output signal. Due to effective sampling in the PLL system, this 1-MHz offset is aliased to both sides of the desired signal. Therefore, when the desired output is 6001 MHz, spurious signals will be present at 6000 MHz and 6002 MHz, and $F_{vco}/OSCin$ will be the reference coupling.

Similarly for an output signal of 6000.1 MHz, the spur will appear at a 100-kHz offset from the desired signal and for 6000.01 MHz, spur will be at 10-kHz offset from the output signal. In the same manner, for 6000.2 MHz, the spur will be at the 200-kHz offset, and for 6000.02 MHz, the spur will be at the 20-kHz offset from the carrier.

The spur reduction technique can be explained by an example. If the output frequency is set at 6000.01 MHz, there is a spur at the 10-kHz offset if the reference frequency is provided by an oscillator of 100 MHz. These spurs are strongest if they fall in the PLL bandwidth. If the spur is at a lower offset, it will contribute to the integrated noise; if the spur is at a higher offset, it will modulate or demodulate the adjacent channel with the desired channel and distort the system. The spur can be attained based on the loop filter BW and the offset from the output frequency. Now this spur can be shifted to a higher offset frequency by changing the reference frequency. As an example, set the reference frequency at 102 MHz. The $F_{vco}/Oscin$ spur now shifts to 6017.99 MHz from the desired signal. Due to loop filter bandwidth roll-off, the spur that appears at 17.99-MHz will be attenuated. In the same manner, the spur at 100 kHz for 6000.1 MHz and the spur at 1 MHz for 6001 MHz can be shifted away from the carrier. The spur reduction algorithm can be implemented with the look-up table approach.

3.1 Frequency Synthesizer

The LMX2592 is a ultra-low noise 9.5-GHz synthesizer with integrated VCO supporting wide input reference range from 5 to 1400 MHz. The device accepts input frequencies up to 1.4 GHz, which combined with frequency dividers and programmable low noise multiplier allows flexible frequency planning. This feature enables the use of a programmable clock as an input signal to implement the spur reduction technique. Also, the phase detector (PFD) can take frequencies from 5 to 200 MHz, but also has extended modes down to 0.25 MHz and up to 400 MHz. This device requires only a single supply of 3.3 V, which further reduces the system complexity, power consumption, and cost. It is the lowest noise Frac-N synthesizer on the market with excellent in-band spurs (-75 dBc), and hence well suited for Test and Measurement applications. The critical design consideration in general for frequency generator application are lock time, frequency resolution, power resolution, phase noise, spur, and integrated noise. The LMX2592 has a lock time of 1 ms, which is well suited for benchtop test equipment. Its output power level resolution (less than 0.5 dB) is the best among the available integrated synthesizers. The device supports both fractional-N and integer-N modes with a 32-bit fractional divider, allowing a frequency selection of less than 0.05 Hz. An integrated noise of 49 fs for a 6-GHz output makes it an ideal low noise source. Combining a best-in-class PLL and integrated VCO noise with integrated LDOs, this device removes the need for multiple discrete devices in high performance systems. It uses a spur reduction technique to reduce the spur due to the OSCin VCO coupling, integer boundary spur, or any other spur due to reference coupling. The loop filter for this synthesizer is external to the device and a typical loop filter bandwidth is 100 kHz. See the LMX2592 datasheet ([SNAS646](#)) for recommended loop filter components for this device. Also, see the Platinum Sim for details on loop filter design, which can be programmed using SPI. This TI Design has options for reference as onboard fixed oscillator, external oscillator, and onboard programmable reference. The synthesizer is connected to the output section. The LMX2592 is connected only to a 3.3-V supply and consumes approximately 350 mA.

3.2 Programmable Clock Generator

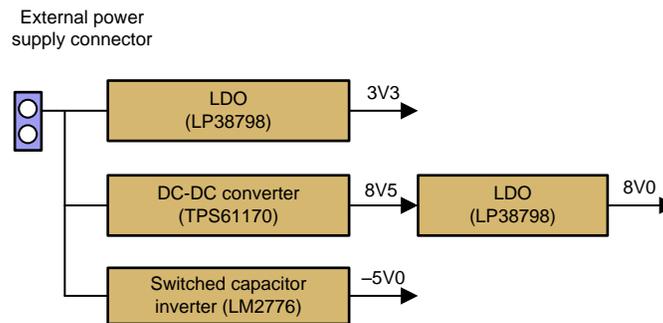
The TIDA-00626 uses the LMK61E2 as a programmable reference. Spur reduction can be enabled by the LMK61E2 as this device has output range matching with the wide input range of the LMX2592. The loop filter of the LMK61E2 is internal and can be programmed to get the best performance. This device has excellent power supply ripple rejection (PSRR) due to internal power conditioning. The registers can be programmed through I²C interface using CodeLoader 4 GUI. The passband noise of the LMK61E2 is very low, so the device is used as reference for the LMX2592. The LMK61E2 is connected to a 3.3-V supply and consumes approximately 162 mA. The LMK61E2 has a very good phase noise of -143 dBc/Hz for a 5-GHz VCO output at a 10-kHz offset; hence, it meets the phase noise requirement for the overall system. The device must be connected in LVPECL mode.

3.3 Output Section

The output section consists of an RF attenuator and an RF amplifier. The attenuator ensures the output amplifier does not get saturated at lower output frequencies. The RF attenuator can be programmed and has a wide attenuation range. The RF amplifier provides sufficient gain for higher frequencies such that the output power level can be maintained over the complete frequency range. For example, the LMX2592 output power varies from 8 dBm at 20 MHz to -2 dBm at 9.8 GHz.

By using the attenuator and amplifier, the output power level can be increased to 1.7 dBm; the attenuator has an insertion loss of 6 dB and the amplifier has a gain of 9.7 dB at 9.8 GHz. The attenuator is connected to a -5 -V supply, and the current consumption is approximately 17 mA. The RF amplifier is connected to the supply voltage of 8 V and consumes approximately 133 mA.

3.4 Power Supply



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Figure 2. Power Tree

The LP38798 is selected as the power supply for the LMX2592, LMK61E2, and CWX813-100 because of its very low noise and high PSRR feature. It can provide a maximum current of 800 mA and can be used for the RF applications.

The TPS61170 converts the 5-V input to 8.5 V. It can provide a maximum current of 1.2 A. An LDO is used at the output of 8.5 V to prevent the switching noise coupling into the RF circuit. 8 V is generated by the LP38798 LDO as a power supply for the RF amplifier.

The LM2776 is a switched capacitor inverter to provide -5 V to the attenuator. The switched capacitor inverter has very low switching noise compared to DC-DC converter. The LM2776 can provide a maximum current of 200 mA.

For better noise rejection, ferrite beads are used at the output of the 3V3 power supply.

3.5 Programming Interface

SPI is used to program the LMX2592. See the LMX2529EVM user's guide ([SNAU195](#)) to use the TICS Pro GUI to program the LMX2592 using USB2ANY. Also, there is option to program LMX2592 using MSP430F5529 LaunchPad or any other similar controller. See the LMX2592 datasheet ([SNAS646](#)) for programming.

An I²C interface is used to program the LMK61E2. See the LMK61E2 datasheet ([SNAS674](#)) for programming. Program the LMK61E2 by using the MSP430F5529 LaunchPad or any other similar controller. Also, there is an option to program the LMK61E2 using the CodeLoader 4 GUI with USB2ANY. See the CodeLoader 4 user's guide ([SNAU083](#)) on how to program the LMK61E2 using CodeLoader 4.

4 Block Diagram

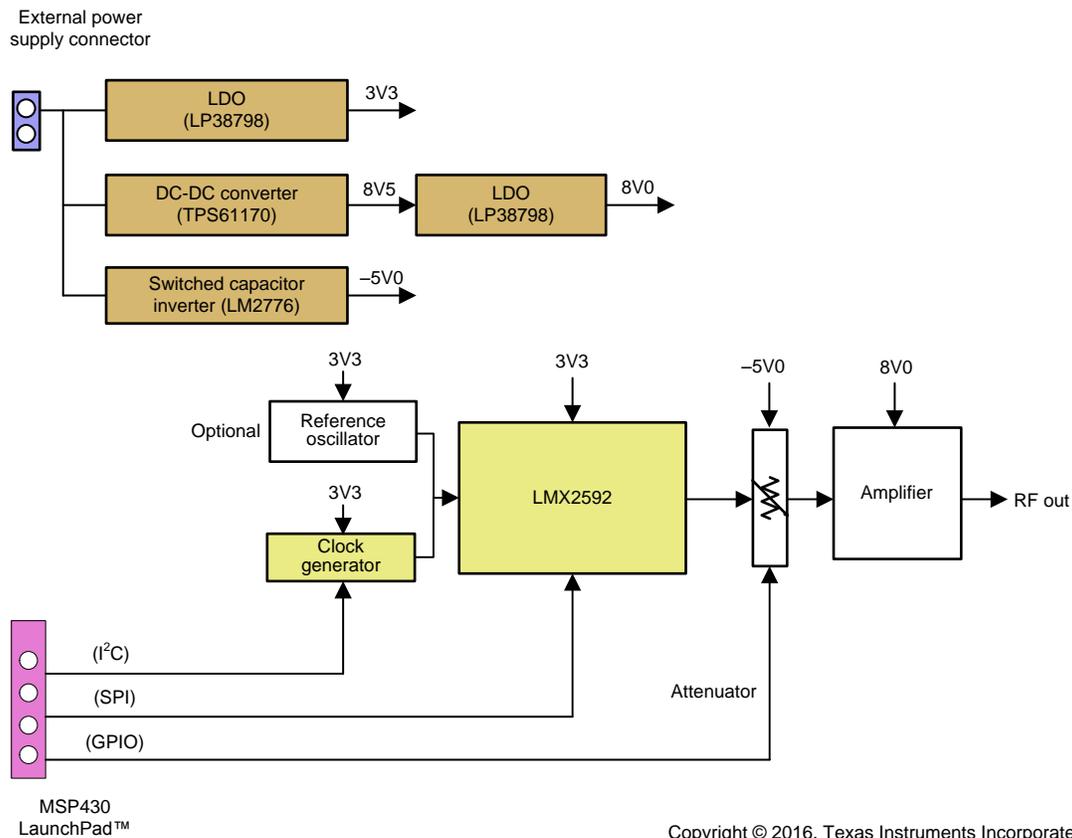


Figure 3. Block Diagram of CW RF Signal Generator (TIDA-00626)

4.1 Highlighted Products

4.1.1 LMX2592

The LMX2592 is a low-noise, wideband RF PLL with integrated VCO that supports a frequency range from 20 MHz to 9.8 GHz. The device supports both fractional-N and integer-N modes, with a 32-bit fractional divider allowing fine frequency selection. Its integrated noise of 49 fs for a 6-GHz output makes the device an ideal low noise source. Combining a best-in-class PLL and integrated VCO noise with integrated LDOs, this device removes the need for multiple discrete devices in high performance systems. The device accepts input frequencies up to 1.4 GHz, which combined with frequency dividers and programmable low noise multiplier allows flexible frequency planning. The additional programmable low noise multiplier lets users mitigate the impact of integer boundary spurs. In fractional-N mode, the device can adjust the output phase by a 32-bit resolution. For applications that need fast frequency changes, the device supports a fast calibration option, which takes less than 25 μ s. This performance is achieved by using a single 3.3-V supply. It supports two flexible differential outputs that can be configured as single-ended outputs as well. Users can choose to program one output from the VCO (or doubler) and the second from the channel divider. When not being used, each output can be muted separately.

4.1.2 LMK61E2

The LMK61E2 is an ultra-low jitter PLLatinum™ programmable oscillator with a fractional-N frequency synthesizer with integrated VCO that generates commonly used reference clocks. The outputs can be configured as LVPECL or LVDS or HCSL. The device features self-startup from on-chip EEPROM that is factory programmed to generate a 156.25-MHz LVPECL output. The device registers and EEPROM settings are fully programmable in-system through I²C serial interface. Internal power conditioning provides excellent PSRR, reducing the cost and complexity of the power delivery network. The device operates from a single 3.3-V \pm 5% supply. The device provides fine and coarse frequency margining options through I²C serial interface to support system design verification tests (DVT) such as standard compliance and system timing margin testing.

4.1.3 LP38798

The LP38798-ADJ is a high-performance linear regulator capable of supplying a 800-mA output current. Designed to meet the requirements of sensitive RF and analog circuitry, the LP38798-ADJ implements a novel linear topology on an advanced CMOS process to deliver ultra-low output noise and high PSRR at switching power supply frequencies. The LP38798SD-ADJ is stable with both ceramic and tantalum output capacitors and requires a minimum output capacitance of only 1 μ F for stability. The LP38798-ADJ can operate over a wide input voltage range (3 to 20 V), making it well suited for many post-regulation applications.

4.1.4 LM2776

The LM2776 CMOS charge-pump voltage converter inverts a positive voltage in the range of 2.7 to 5.5 V to the corresponding negative voltage. The LM2776 uses three low-cost capacitors to provide 200 mA of output current without the cost, size, and electromagnetic interference (EMI) related to inductor-based converters. With an operating current of only 100 μ A and operating efficiency greater than 90% at most loads, the LM2776 provides the ideal performance for battery-powered systems that require a high-power negative power supply. The LM2776 has been placed in TI's 6-pin SOT-23 to maintain a small form factor.

4.1.5 TPS61170

The TPS61170 is a monolithic, high-voltage switching regulator with integrated 1.2-A, 40-V power MOSFET. The device can be configured in several standard switching-regulator topologies, including boost and SEPIC. The device has a wide input-voltage range to support applications with input voltage from multi-cell batteries or regulated 5-V and 12-V power rails. The TPS61170 operates at a 1.2-MHz switching frequency, allowing the use of low-profile inductors and low-value ceramic input and output capacitors. External loop compensation components give the user flexibility to optimize loop compensation and transient response. The device has built-in protection features such as pulse-by-pulse overcurrent limit, soft start, and thermal shutdown. The FB pin regulates to a reference voltage of 1.229 V. The reference voltage can be lowered using a 1-wire digital interface (Easyscale™ protocol) through the CTRL pin. Alternatively, a pulse width-modulation (PWM) signal can be applied to the CTRL pin. The duty cycle of the signal reduces the feedback reference voltage proportionally. The TPS61170 is available in a 6-pin 2-mm \times 2-mm QFN package, allowing a compact power-supply solution.

4.1.6 SN74AHCT244

These octal buffers and drivers are designed specifically to improve both the performance and density of 3-state memory-address drivers, clock drivers, and bus-oriented receivers and transmitters.

4.1.7 MSP430F5529

The TI MSP430™ family of ultra-low-power microcontrollers consists of several devices featuring peripheral sets targeted for a variety of applications. The architecture, combined with extensive low-power modes, is optimized to achieve extended battery life in portable measurement applications. The microcontroller features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows the devices to wake up from low-power modes to active mode in 3.5 μ s (typical). The MSP430F5529, MSP430F5527, MSP430F5525, and MSP430F5521 microcontrollers have integrated USB and PHY supporting USB 2.0, four 16-bit timers, a high-performance 12-bit analog-to-digital converter (ADC), two universal serial communication interfaces (USCI), a hardware multiplier, DMA, a real-time clock (RTC) module with alarm capabilities, and 63 I/O pins. The MSP430F5528, MSP430F5526, MSP430F5524, and MSP430F5522 microcontrollers include all of these peripherals but have 47 I/O pins. The MSP430F5519, MSP430F5517, and MSP430F5515 microcontrollers have integrated USB and PHY supporting USB 2.0, four 16-bit timers, two universal serial communication interfaces (USCI), a hardware multiplier, DMA, an RTC module with alarm capabilities, and 63 I/O pins. The MSP430F5514 and MSP430FF5513 microcontrollers include all of these peripherals but have 47 I/O pins. Typical applications include analog and digital sensor systems, data loggers, and others that require connectivity to various USB hosts.

5 Getting Started Hardware

5.1 TIDA-00626 Connector Configuration

Figure 4 shows the TIDA-00472 connector configuration.

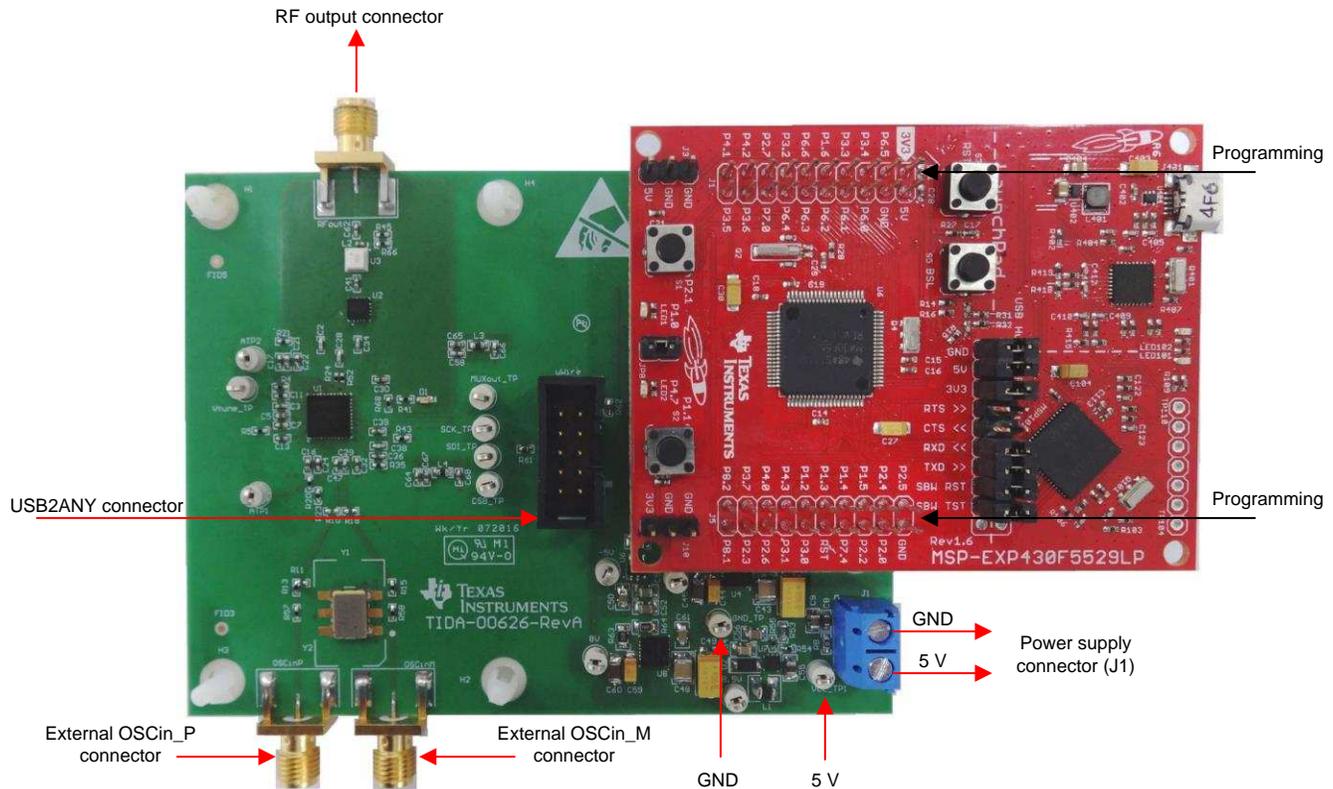


Figure 4. TIDA-00626 PCB Connectors

- Power**
 Power supply connector J1: This pin is used to connect the input power supply. Set the power supply to 5 V with a 1-A current limit.
- Input signal**
 Option 1: The onboard oscillator (Y1) is powered on and outputs a 100-MHz signal to OSCin_P (Pin 8) of the device input. While using Y1, disconnect the clock input from LMK61E2 (U5) by bypassing the resistors R13 and R15.
 Option 2: The onboard oscillator (U5) is powered on and factory programmed to generate a 156.25-MHz LVPECL output. While using input clock from U5, disconnect Y1 by bypassing R11. U5 can be programmed to generate different clock frequencies using an I²C interface.
 Option 3: Connect the external reference to External OSCin_P and OSCin_M connectors, while connecting external reference disconnect Y1 and U5 by bypassing R13, R15 and R11 resistors on board. Connect to OSCin_P or OSCin_M if you have a single ended signal. Connect to both if you have a differential signal.
- Output**
 Connect RF_{OUT} to a phase noise analyzer. It is a single-ended output.

- **Programming interface**

I²C interface for LMK61E2 (J3): Connect the I²C SDA (Pin 1), SCL (Pin 2), and GND (Pin 5) of the USB2ANY connector to the J3 connector on the board. See the USB2ANY datasheet for pin configurations. Connect the other end of the USB2ANY to the PC through any USB port.

Connections on J3 connector:

- SDA: Pin 19
- SCL: Pin 17
- GND: Pin 4

SPI for LMX2592 (USB2ANY interface): Connect USB2ANY to the USB2ANY connector shown in [Figure 4](#). Connect the other end of the USB2ANY to the PC through any USB port.

SPI for LMX2592 (using MSP430F5529): Make the connections as per J2 and J3 connector.

Connections on the J2 connector:

- SDI: Pin 12
- CSB: Pin 18

Connections on the J3 connector:

- SCK: Pin 13

Program the attenuator by using the MSP430F5529 or any other GPIO. The level translator, SN74AHCT244, is used onboard to translate the 3.3-V control voltage from the MSP430F5529 to 5 V for attenuation control bits.

6 Getting Started Firmware

6.1 LMX2592 Software Start-up Instruction

1. Download the TICS Pro GUI from TI.com: <http://www.ti.com/tool/TICSPRO-SW>.
2. To start the software, open TICS.exe from installed directory. Open the software as shown in Figure 5.

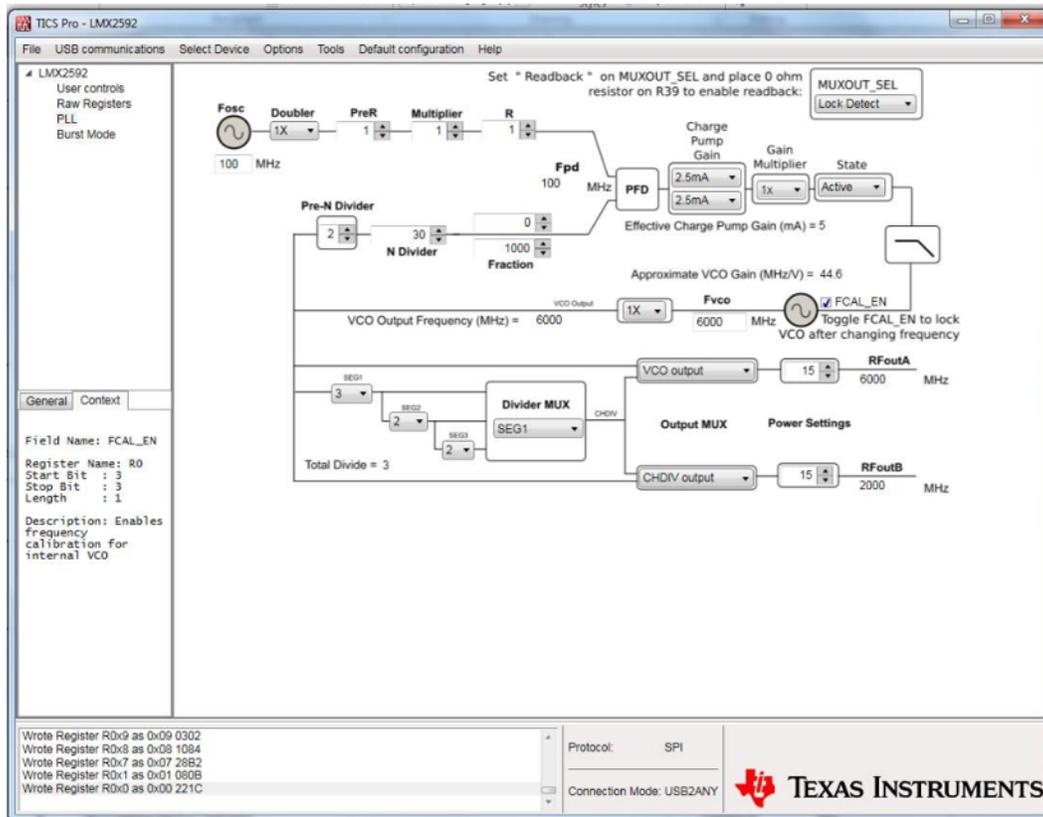


Figure 5. TICS PRO GUI Screenshot

The following describes the interface layout and their functions:

- Top menu
 - File: Load or save a setting and export or import the registers in HEX value.
 - USB communications: Check connections with the USB2ANY module (if there is new software, follow the on-screen instructions to upgrade). Load the device (the keyboard shortcut is CTRL+L), which programs all the registers into the device.
 - Default configuration: Load a pre-set setting file given to start from a known state.

To select the LMX2592, click Select Device on top menu. Then click PLL + VCO and select LMX2592.

- Left panel:
 - User controls: Configure registers, which are organized by function. Hover the mouse over a register and its information will appear in the "Context" tab on the left panel.
 - Raw registers: See the entire register map. Enter a HEX value in the Data cell then click Write Register to program that value.

To read registers, connect the MUXout pin (Pin 20) to the USB2ANY (by default, it is connected to the LED, switch R40 to R39 for readback). Also set MUXOUT_SEL = 0 for readback. Registers are also listed by name in the "Register/Field Name" section.

- PLL
 - F_{osc} : Enter the input signal frequency between 5 to 1400 MHz.
 - Doubler: Can double the input signal frequency (input must be 50% duty cycle to use this)
 - Pre-R divider: Divides frequencies up to 1400 MHz
 - Multiplier: Multiplies frequencies between 40 to 70 MHz and outputs between 180 to 250 MHz
 - R divider: Divides frequencies below 5 MHz for very low PFD
 - Charge pump gain: This tab will auto-update UP and DN to be equal. Go to the Bits/Pins section to force different values.
 - Gain multiplier: Multiplies the charge pump gain by a factor
 - State: Changes the charge pump output state
 - FCAL_EN: Every time the output frequency is changed, toggle this off and on to calibrate the device to the frequency.
 - Fvco: Sets the VCO frequency between 3550 to 7100 MHz
 - 1X or 2X: Enables the VCO doubler from 3550 to 4900 MHz for frequencies up to 9800 MHz
 - Divider MUX: Determines which of the three segments are included for a total division between 2 to 192
 - Output MUX: Selects the signal from the VCO output or the divider
 - Power Settings: Changes the output power (increase 0 to 31, then additional boost with 49 to 63)
- Burst Mode
 - Enter a register in "Load Register" or delay in seconds.
 - Runs and stops the commands in a single burst or continuous loop.

6.2 LMK61E2 Software Start-up Instruction

1. Download the CodeLoader 4 software from TI.com: <http://www.ti.com/tool/Codeloader4>
2. To start the software, open the Codeloader4.exe from the installed directory. Open the software as shown in Figure 6.

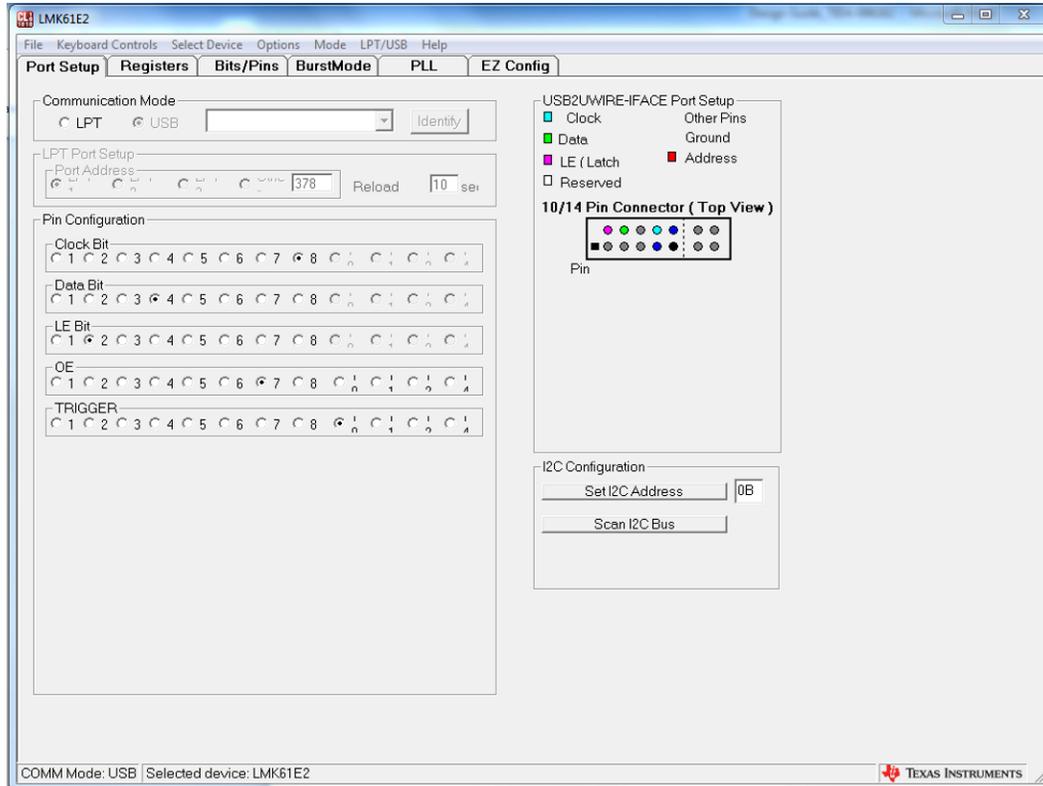


Figure 6. CodeLoader 4 GUI Screenshot

- To select the LMK61E2: Click Select Device on top menu. Then click clock conditioners and select LMK61E2. This opens the EZ Config tab.

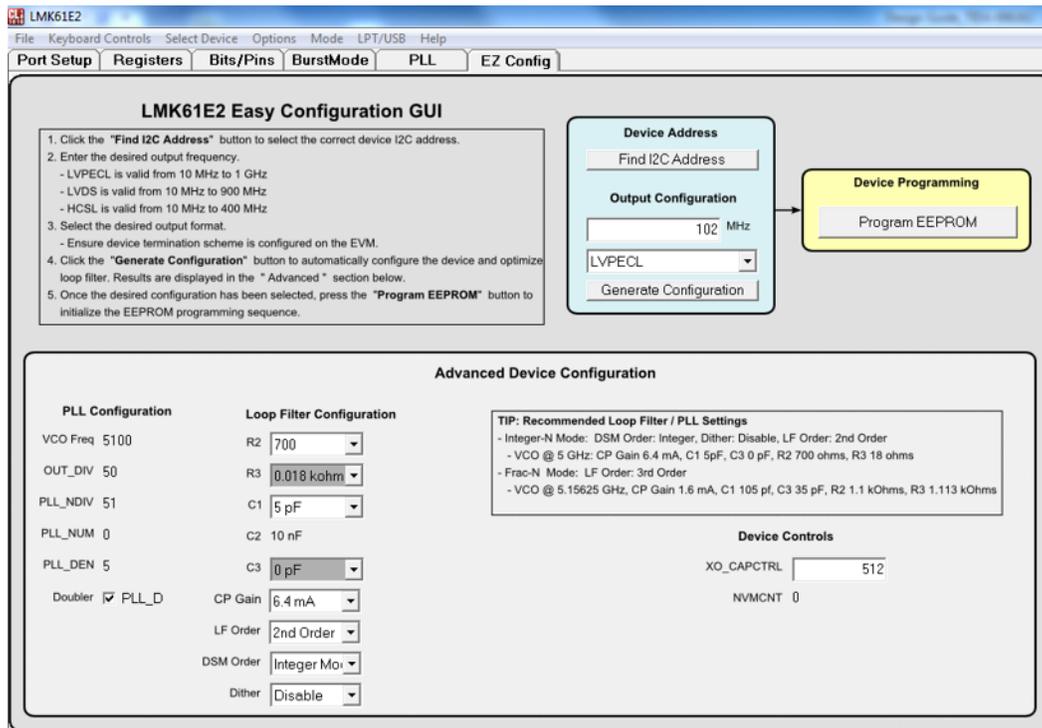


Figure 7. LMK61E2 Programming Using CodeLoader 4 GUI

- Follow the steps given in Figure 7 to program LMK61E2 registers. The LMK61E2 has a programmable internal loop filter. See Table 5 of the LMK61E2 EVM guide ([SNAU188](#)) to set the filter values for optimum output. See the CodeLoader 4 user's guide ([SNAU083](#)) for details on device programming using CodeLoader 4.

7 Test Setup

Figure 8 shows the test setup used in the lab to test the signal generator.

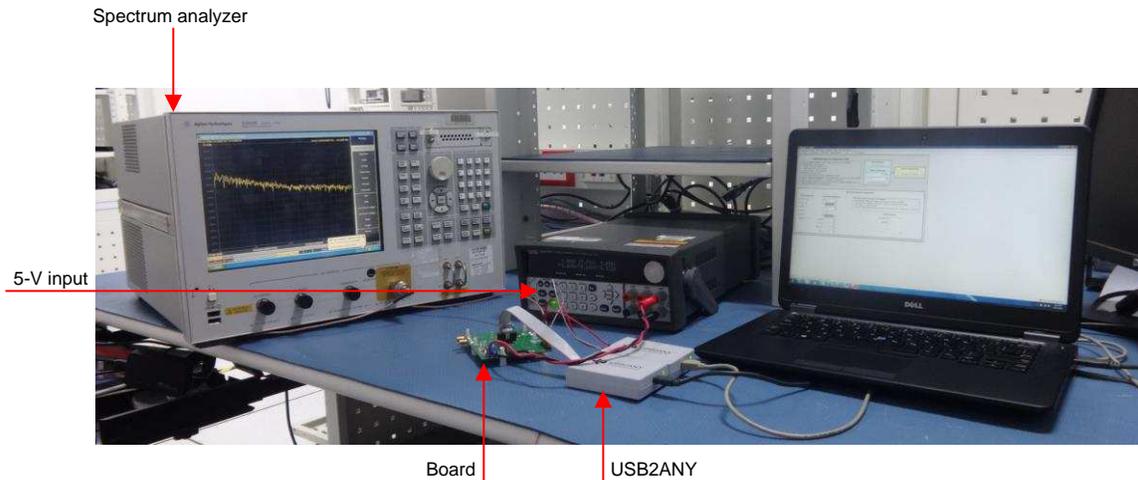


Figure 8. TIDA-00626 Test Setup

Figure 9 shows the connections for LMX2592 and LMK61E2 programming with TICS Pro GUI and CodeLoader 4 using USB2ANY.

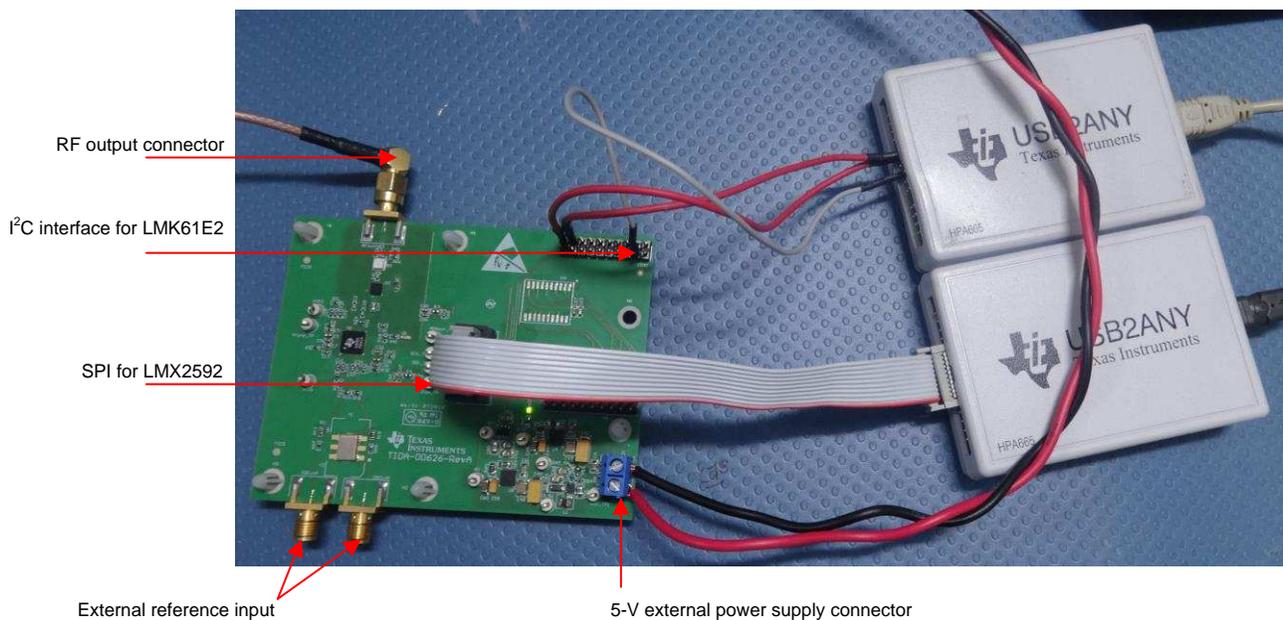


Figure 9. LMX2592 and LMK61E2 Programming Using TICS PRO GUI and CodeLoader 4 Using USB2ANY

8 Test Data

8.1 Output Power versus Frequency Range

Table 2 shows the output power results for the signal generator output frequencies. The maximum output power is 9.4 dBm at 3 GHz. The minimum power is 2 dBm at the highest frequency of 9.8 GHz.

Table 2. Output Power versus Frequency Range

OUTPUT FREQUENCY (dBm)	OUTPUT FREQUENCY (MHz)
7.9	20
8.1	100
8.9	1000
9.4	3000
6.0	6000
2.0	9800

8.2 Closed-Loop Phase Noise Performance

Table 3 shows the closed-loop phase noise performance of the signal generator for 1.24 GHz, 3 GHz, 6 GHz, and 9.8 GHz at an offset of 100 kHz, 1 MHz, 10 MHz, and 100 MHz, respectively. The maximum phase noise observed is -107.1 dBc/Hz at 6 GHz, 100-kHz offset. The results are as shown in Figure 10.

Table 3. Closed-Loop Phase Noise for Output Frequencies

OUTPUT	CONDITION	MIN	TYP	MAX	UNITS
1.24 GHz	100 kHz		-121.7		dBc/Hz
	1 MHz		-142.7		
	10 MHz		-149.6		
	100 MHz		-156.8		
3 GHz	100 kHz		-117.5		
	1 MHz		-139.7		
	10 MHz		-142.7		
	100 kHz		-153.5		
6 GHz	100 kHz		-111.3		
	1 MHz		-133.3		
	10 MHz		-150.8		
	100 MHz		-154.0		
9.8 GHz	10 kHz		-107.1		
	1 MHz		-127.2		
	10 MHz		-138.2		
	100 MHz		-139.5		

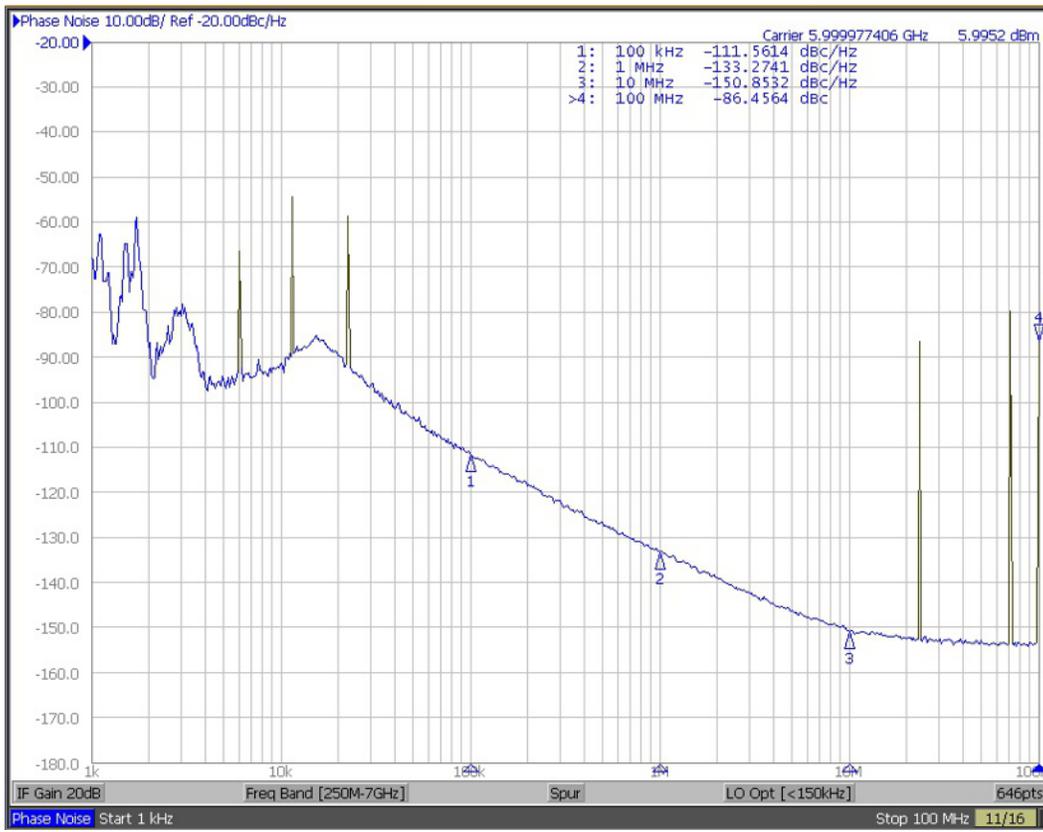


Figure 10. 6-GHz Output—Closed-Loop Phase Noise

8.3 Results for Spur Reduction Technique

Figure 11 shows the VCO OSCin coupling spur at a 10-kHz offset for a 6000.01-MHz signal with reference frequency of 100 MHz. The spur level is -32.01 dBc/Hz.

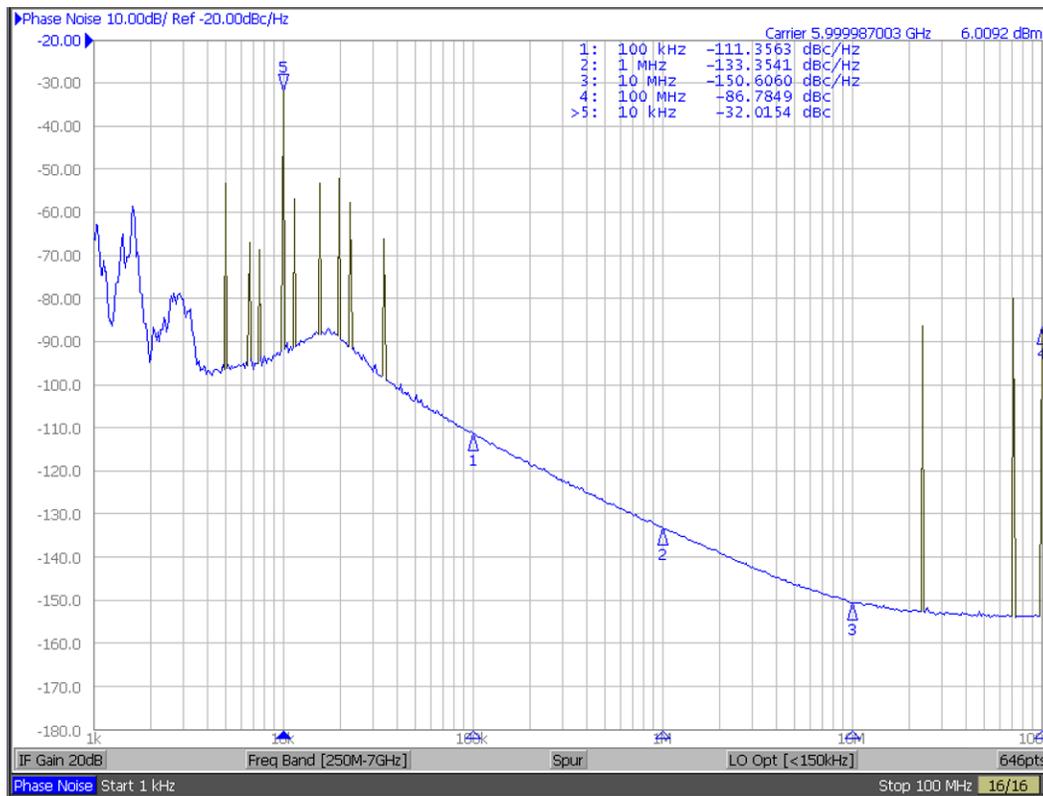


Figure 11. Spur at 10-kHz Offset From 6000.01-MHz Carrier due to VCO OSCin Coupling

Figure 12 shows the result of spur reduction technique by setting the reference to 102 MHz. VCO OScin coupling spur at 10-kHz offset for a 6000.01-MHz signal with a reference frequency of 100 MHz got shifted to 17.99 MHz from the carrier with a reduced spur level due to the loop filter roll-off.

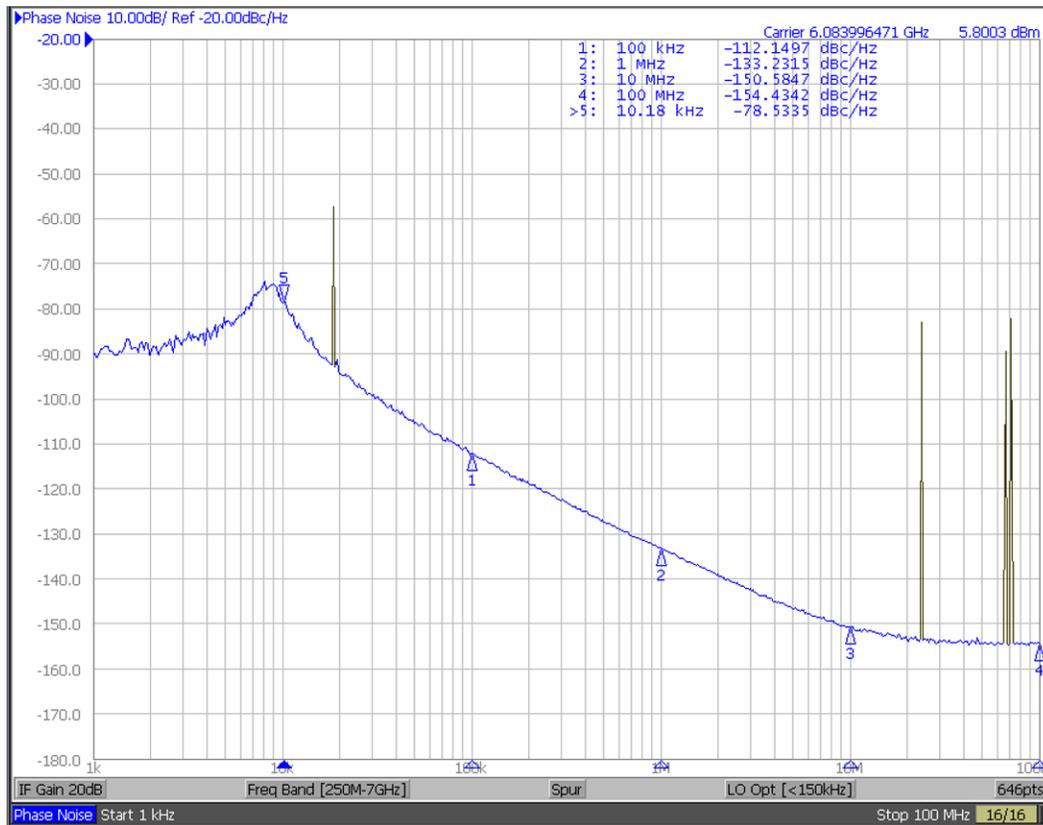


Figure 12. Spur Reduction by Setting the Reference Frequency to 102 MHz (No Spur at 10-kHz Offset)

Figure 13 shows the VCO OSCin coupling spur at a 100-kHz offset for a 6000.1-MHz signal with a reference frequency of 100 MHz. The spur level is -57.1 dBc/Hz.

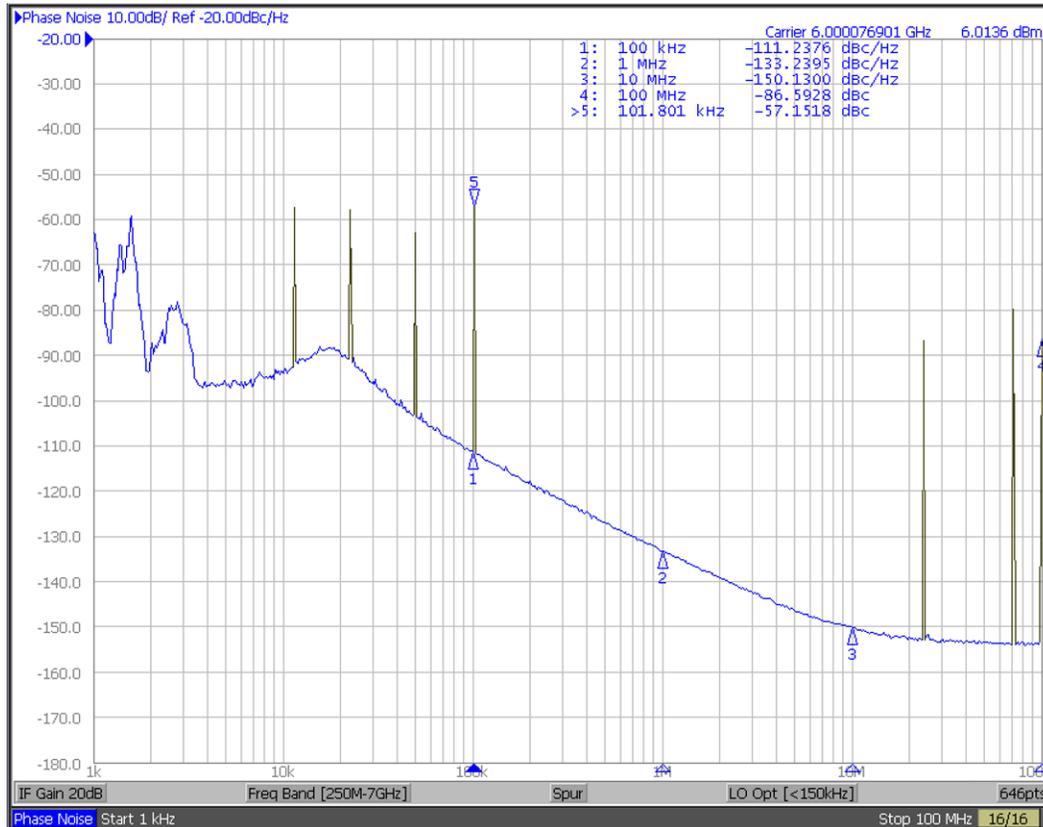


Figure 13. Spur at 100-kHz Offset From 6000.1-MHz Carrier due to VCO OSCin Coupling

Figure 14 shows the result of the spur reduction technique by setting the reference to 102 MHz. The VCO OScin coupling spur at a 100-kHz offset for a 6000.1-MHz signal with a reference frequency of 102 MHz got shifted to 17.9 MHz from the carrier with a reduced spur level due to the loop filter roll-off.

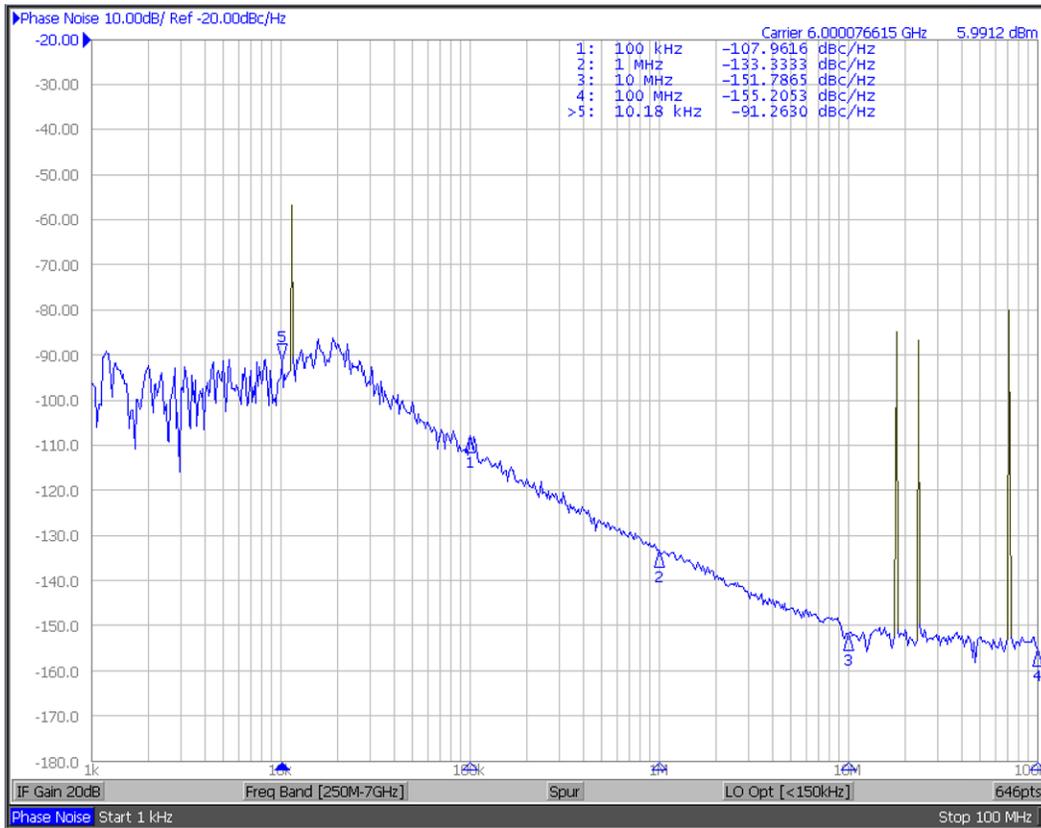


Figure 14. Spur Reduction by Setting the Reference Frequency to 102 MHz (No Spur at 100-kHz Offset)

Figure 15 shows the VCO OSCin coupling spur at a 1-MHz offset for a 6001-MHz signal with a reference frequency of 100 MHz. The spur level is -81.8dBc/Hz .

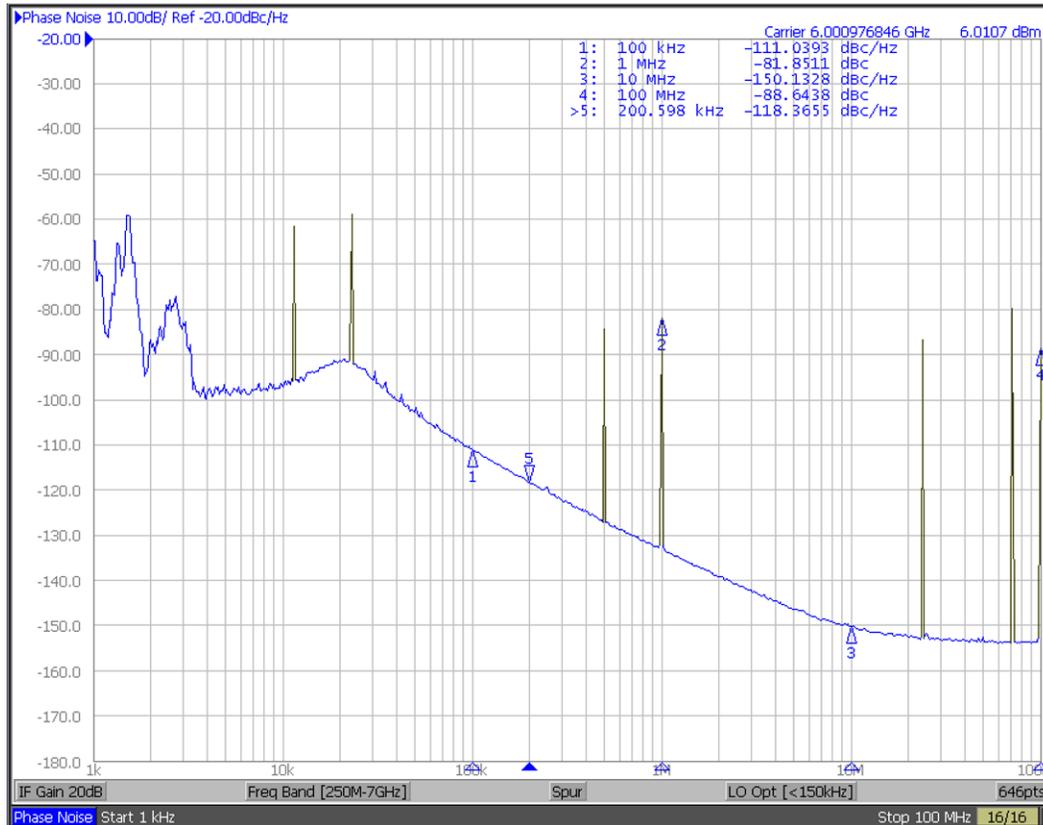


Figure 15. Spur at 1-MHz Offset From 6001-MHz Carrier due to VCO OSCin Coupling

Figure 16 shows the result of the spur reduction technique by setting the reference to 102 MHz. The VCO OScin coupling spur at a 1-MHz offset for a 6001-MHz signal with a reference frequency of 102 MHz got shifted to 17 MHz from the carrier with a reduced spur level due to the loop filter roll-off.

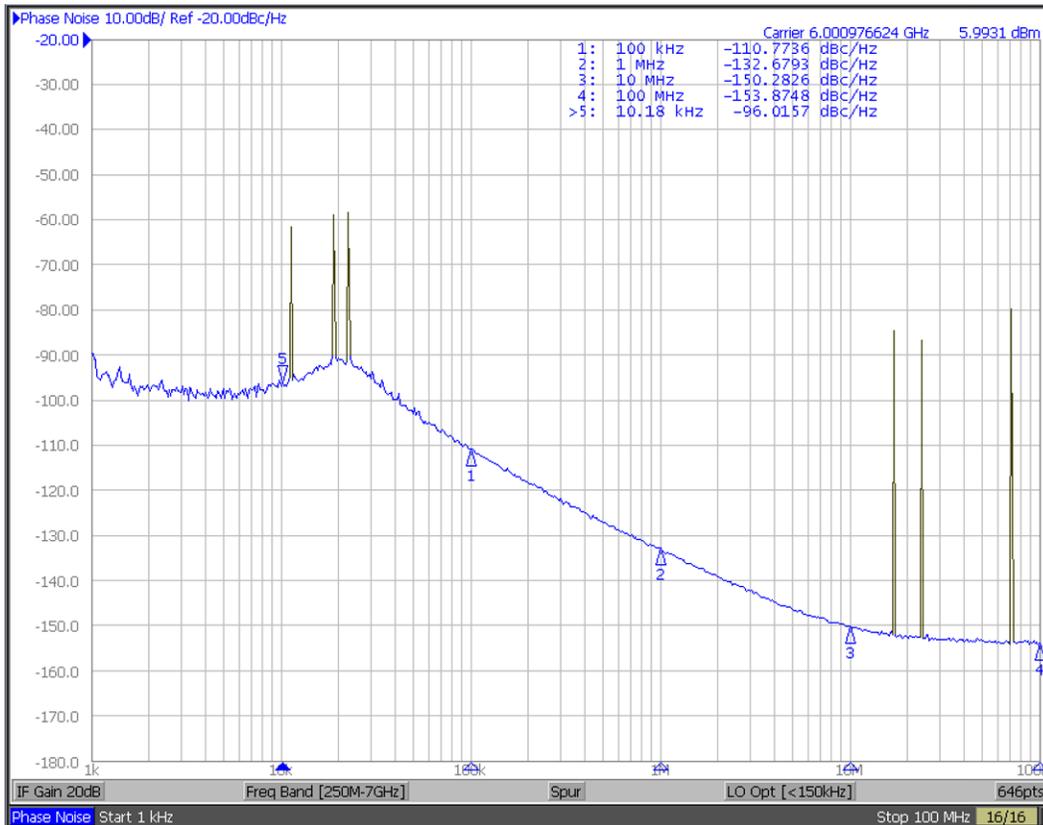


Figure 16. Spur Reduction by Setting the Reference Frequency to 102 MHz (No Spur at 1-MHz Offset)

9 Design Files

9.1 Schematics

To download the schematics, see the design files at [TIDA-00626](#).

9.2 Bill of Materials

To download the bill of materials (BOM), see the design files at [TIDA-00626](#).

9.3 PCB Layout Recommendations

In general, the following layout guidelines are similar to most other PLL devices:

- Place output pullup components close to the pin.
- Place capacitors close to the pins.
- Make sure the input signal trace is well matched.
- Do not route any traces that carry the switching signal close to the charge pump traces and external VCO.
- Also place all RF circuits in the output section away from the switching signal.

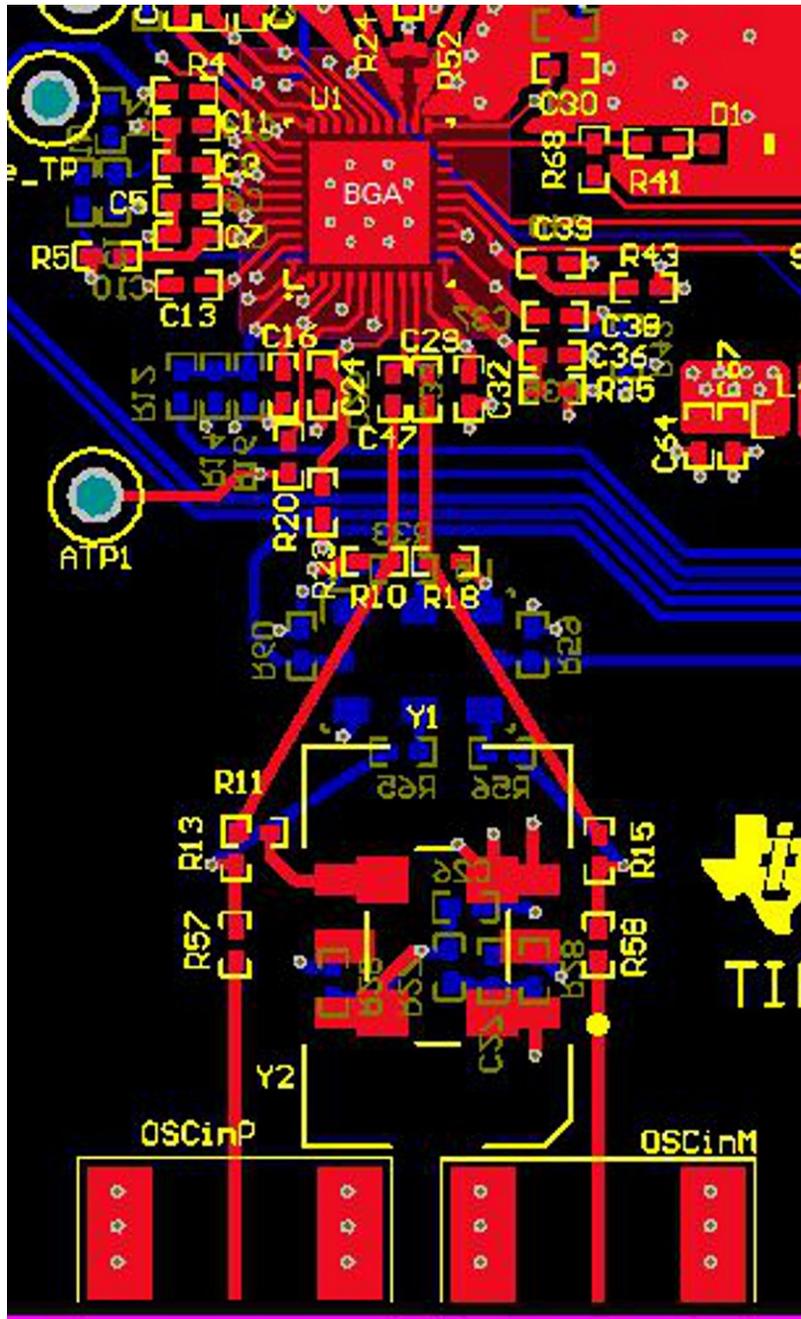


Figure 17. Layout Example for Input Reference and LMX2592

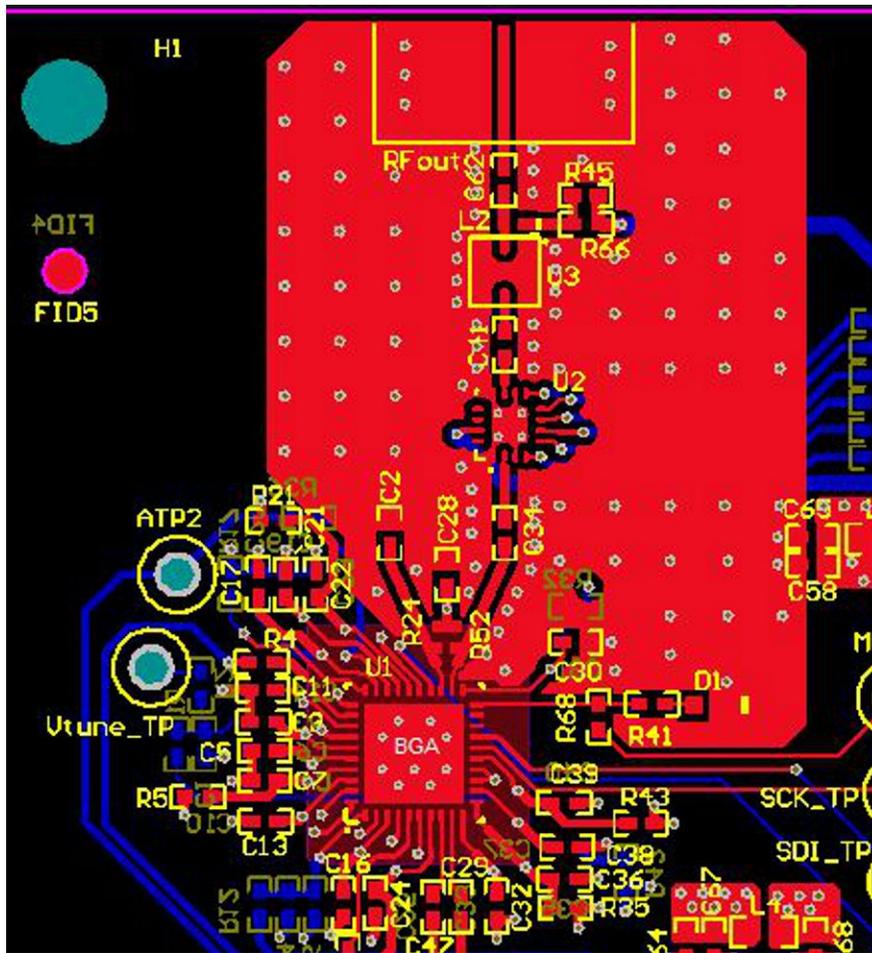


Figure 18. Layout Example for Output Section

Revision A History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (April 2016) to A Revision	Page
• Changed from preview page.....	1

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