TI Designs

Powering Xilinx™ Zynq® UltraScale+™ Based Remote Radio Head (RRH) or Backhaul (BH) Reference Design

Design Overview

The function of the PMP12004-HE TI Design is to provide a solution for the power supply of Xilinx Zynq® UltraScale+™ based remote radio heads (RRH). This power design only requires two regulator devices: the TPS6508640 power management integrated circuit (PMIC) and the TPS544C25 high-current, single-channel device. Using these devices reduces size, cost, and power loss by featuring integrated rails, high switching frequency, and separate rails for the core supplies. This design guide addresses the following topics: RRH power solutions and designing for maximum efficiency.

Design Resources

PMP12004-HE	Design Folder
TPS6508640	Product Folder
TPS544C25	Product Folder
CSD87331Q3D	Product Folder

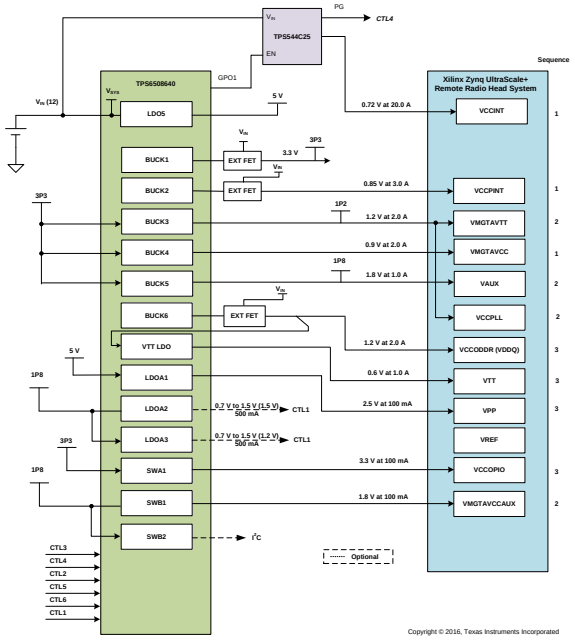
TI E2E™ Community — ASK Our E2E Experts

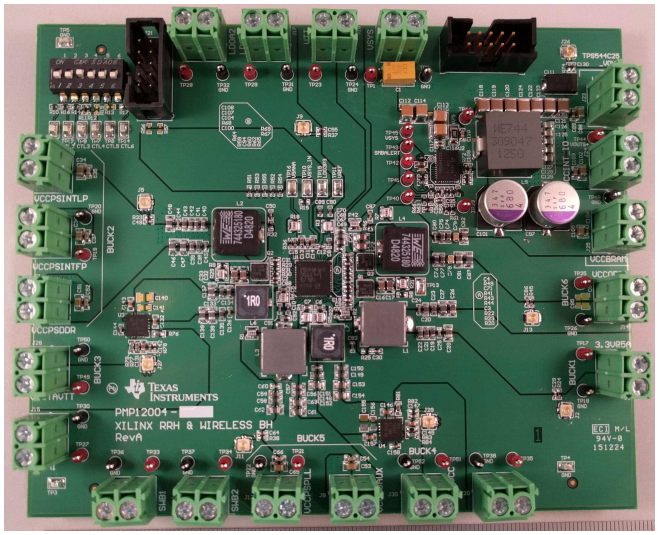
Design Features

- PMIC Reduces Solution Size by Integrating Several Rails Within Single Device
- PMIC Reduces Inductor Size by Having High Switching Frequency Converters and Controllers
- Separation of Core Option Saves Power With Estimated 2.6 W at Max Loading
- DVS Allows For Higher Power Savings by Reducing Output Power for Lower Operational Requirements

Featured Applications

- Remote Radio Head (RRH)
- Wireless Backhaul (BH)





1 Key System Specifications

Table 1. Key System Specifications

RAIL NAME	SUPPLIED BY	VOLTAGE	CURRENT	ADDITIONAL REQUIREMENTS
VCCINT	TPS544C25	0.72 V ±3%	20 A	AC error plus ripple < ±2% with max current step 6 A, DC error < ±1%
VCCPINT	TPS6508640 BUCK2	0.85 V ±3%	3 A	AC error plus ripple < ±2% with max current step 1 A, DC error < ±1%
VAUX	TPS6508640 BUCK5	1.8 V ±3%	1 A	AC error plus ripple < ±2% with max current step 500 mA, DC error < ±1%
VMGTAVCC	TPS6508640 BUCK4	0.9 V ±3%	2 A	Noise is to be less than 10 mV_{PP} over the band from 10 kHz to 80 MHz. For a 50% current step load with a slew of 10 A/us, the output voltage must not deviate by more than 3% of the set voltage.
VMGTAVCCAUX	TPS6508640 SWB1	1.8 V ±3%	100 mA	AC error plus ripple < ±2% with max current step 100 mA, DC error < ±1%. Noise is to be less than 10 mV_{PP} over the band from 10 kHz to 80 MHz.
VMGTAVTT	TPS6508640 BUCK3	1.2 V ±3%	2 A	Noise is to be less than 10 mV_{PP} over the band from 10 kHz to 80 MHz. For a 50% current step load with a slew of 10 A/us, the output voltage must not deviate by more than 3% of the set voltage.
VCCPLL				
VCCOPIO	TPS6508640 BUCK1	3.3 V ±5%	100 mA	—
VCCODDR	TPS6508640 BUCK6	1.2 V ±3%	2 A	AC error plus ripple < ±2% with max current step 500 mA, DC error < ±1%
VREF	Internal on UltraScale+	1.25 V ±2%	1 mA	—
VTT	TPS6508640 VTTLDO	VCCODDR / 2 ±3%	±1 A	—
VREFCA	TPS6508640 VTTLDO	VCCODDR / 2 ±3%	50 mA	—
VPP	TPS6508640 LDOA1	2.5 V ±5%	100 mA	—

2 System Description

The Xilinx Zynq® UltraScale+™ ZU9EG and ZU15EG are suitable multiprocessor system-on-chips (MPSoC) for remote radio heads and backhaul systems. These devices have been defined and optimized for a range of use cases in radio systems. The ZU9EG and ZU15EG are pin-compatible devices that address a range of requirements for wireless access and backhaul applications. The parts address the digital front end (DFE) requirements for 2×2-, 4×4-, and 8×8-radios with bandwidths ranging from 60 MHz to 100 MHz+.

Because of the unique and specific requirements of the Xilinx Zynq® UltraScale+™ devices, TI recommends using a PMIC to handle much of the power supplies and the sequencing of the system. See Figure 1 for an overview of the ZU9EG and ZU15EG power requirements. The TPS544C25 device has been paired with the TPS6508640 device to provide all of the necessary rails in a simple, complete, and efficient solution. The TPS6508640 has three integrated controllers which require external MOSFETs. This design uses the CSD87331Q3D dual channel MOSFETs, although alternative MOSFET selections have also been addressed in this guide.

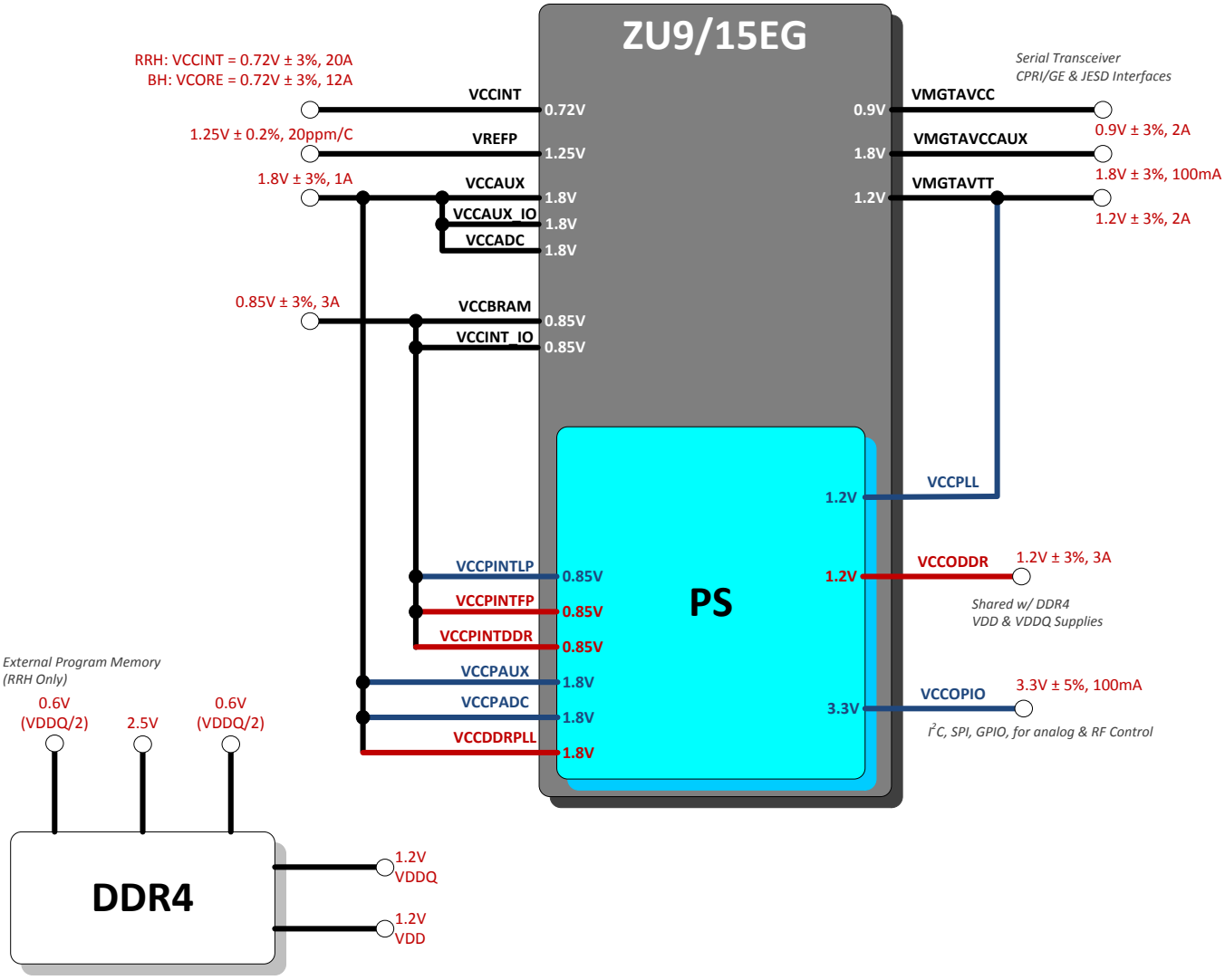


Figure 1. ZU9EG or ZU15EG RHH and Wireless BH DFE Power Supplies

2.1 TPS6508640

The TPS6508640 is a 13-channel PMIC with three buck controllers, three buck converters, four LDOs, and three load switches. The device integrates the complete sequencing and power good validation into the PMIC. The device can also use programmable outputs to control other devices in the system.

The TPS6508640 employs high-frequency DCAP2 controllers, which are extremely fast when responding to load transients. The flexible system rails and the fast response of the bucks make the TPS6508640 an excellent choice for highly-demanding field programmable gate arrays (FPGAs).

2.2 TPS544C25

The TPS544x25 devices are PMBus 1.2 compliant, non-isolated DC-DC converters with integrated field-effect transistors (FETs), which are capable of high-frequency operation and 20- or 30-A current output from a 5×7-mm package. High-frequency, low-loss switching, provided by an integrated NexFET™ technology and optimized drivers, allows for very high-density power solutions. The PMBus interface enables adaptive voltage scaling (AVS) through the VOUT_COMMAND and allows for a flexible converter configuration as well as the option to monitor key parameters, including output voltage, current, and an optional external temperature. Response to fault conditions can be set to restart, latch-off, or ignore depending on system requirements.

2.3 CSD87331Q3D

The CSD87331Q3D NexFET™ Power Block from TI is an optimized design for synchronous buck applications and offers high-current, high-efficiency, and high-frequency capabilities in a small 3.3×3.3-mm outline. Optimized for 5-V gate drive applications, this product offers a flexible solution capable of providing a high-density power supply after pairing with any 5-V gate drive from an external controller or driver.

3 Block Diagram

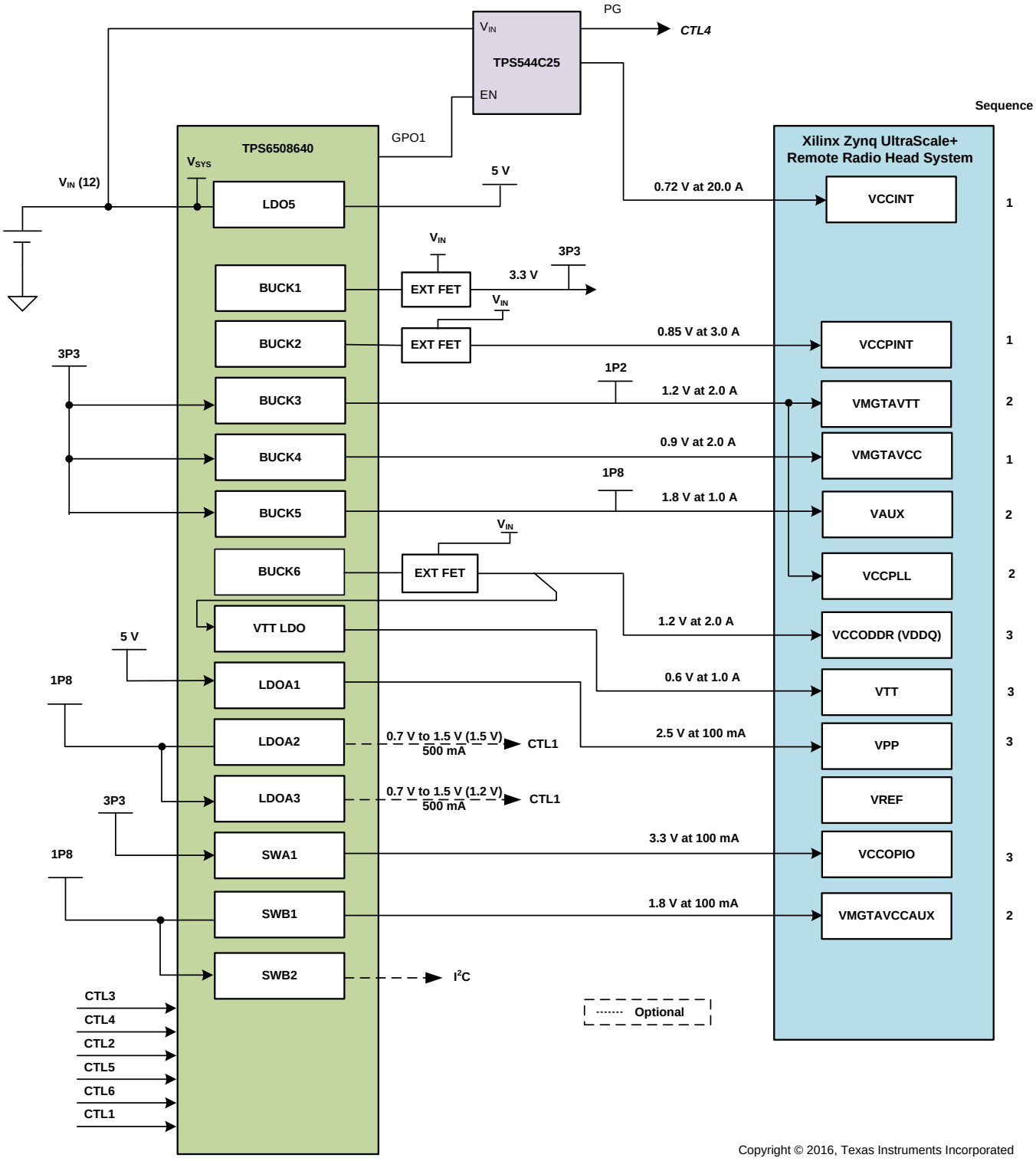


Figure 2. PMP12004-HE Block Diagram

3.1 Highlighted Products

The PMP12004-HE reference design features the following devices:

- TPS6508640
- TPS544C25
- CSD87331Q3D

For more information on each of these devices, see their respective product folders at www.ti.com.

3.1.1 TPS6508640 Features

- Wide V_{IN} range from 5.6 V to 21 V
- Three variable-output voltage synchronous step-down controllers with D-CAP2™ control topology
  - Scalable output current using external FETs with selectable current limit
  - I^2C dynamic voltage scaling (DVS) control from 0.41 V to 1.67 V in 10-mV steps or 1 V to 3.575 V in 25-mV steps
- Three variable-output voltage synchronous step-down converters with DCS-control topology
  - V_{IN} range from 3 V to 5.5 V
  - Up to 3 A of output current
  - I^2C DVS Control From 0.425 V to 3.575 V in 25-mV steps
- Three low dropout (LDO) regulators with adjustable output voltage
  - LDOA1: I^2C-selectable output voltage from 1.35 V to 3.3 V for up to 200 mA of output current
  - LDOA2 and LDOA3: I^2C-selectable output voltage from 0.7 V to 1.5 V for up to 600 mA of output current
- VTT LDO for DDR memory termination
- Three load switches with slew rate control
  - Up to 300 mA of output current with voltage drop less than 1.5% of nominal input voltage
  - Rds_{ON} < 96 mΩ at input voltage of 1.8 V
- 5-V fixed-output voltage LDO (LDO5)
  - Power supply for gate drivers of switched-mode power supplies (SMPS) and for LDOA1
- Built-in flexibility and configurability by factory OTP programming
  - Six general-purpose input (GPI) pins configurable to enable (CTL1 to CTL6) or sleep mode entry (CTL3 and CTL6) of any selected rails
  - Four general-purpose output (GPO) pins configurable to power good of any selected rails
  - Open-drain interrupt output pin
- I^2C interface supports:
  - Standard mode (100 kHz)
  - Fast mode (400 kHz)
  - Fast mode plus (1 MHz)

3.1.2 TPS544C25 Features

- PMBus 1.2 compliant converters: 20 A and 30 A
- Input voltage range: 4.5 V to 18 V
- Output voltage range: 0.5 V to 5.5 V
- 5×7-mm LQFN package
- Single thermal pad
- Integrated 5.5-mΩ and 2.0-mΩ stacked NexFET power stage
- 500-mV to 1500-mV reference for AVS and margining through PMBus
- 0.5% reference accuracy at 600 mV and above

- Lossless low-side MOSFET current sensing
- Voltage mode control with input feed-forward
- Differential remote sensing
- Monotonic start-up into pre-biased output
- Output voltage and output current reporting
- External temperature monitoring with 2N3904 transistor
- Programmable through the PMBus interface
  - VOUT_COMMAND and AVS VOUT transition rate
  - Overcurrent protection with thermal compensation
  - Undervoltage lockout (UVLO), soft-start, and soft-stop
  - PGOOD, overvoltage (OV), undervoltage (UV), and overtemperature (OT) levels
  - Fault responses
- Thermal shutdown
- Pin strapping for switching frequency: 200 kHz to 1 MHz
- Frequency synchronization to an external clock
- Footprint compatible 20-A, 30-A converters

3.1.3 CSD87331Q3D Features

- Half-bridge power block
- Up to 27-V V_{IN}
- Up to 15-A operation
- 91% system efficiency at 10 A
- High-frequency operation (up To 1.5 MHz)
- High density – SON 3.3×3.3-mm footprint
- Optimized for 5-V gate drive
- Low switching losses
- Ultra-low inductance package
- RoHS compliant
- Halogen free
- Pb-free terminal plating

4 System Design Theory

The PMP12004-HE TI Design for Xilinx Zynq® UltraScale+™ based RRHs has two main criteria: efficiency and size. This design focuses primarily on high efficiency, as denoted by the suffix HE. Consult Section 4.2 for a recommended, sized-down bill of materials (BOM).

The TPS6508640 device is controlled by the CTRL input pins. The TPS6508640 sequences all the internal rails and GPOs based on internal delay networks integrated on the CTRL inputs. The TPS6508640 GPO pins control the externally-supplied rails. The CTRL and GPO pins, if used properly, complete the entire sequence required for Xilinx Zynq UltraScale+ systems.

The TPS6508640 has been factory programmed to support both the voltages and sequences required for Xilinx UltraScale+ RRH designs. For the VMGTA rails, noise and ripple can be a constraint in a design. The amount of recommended capacitance C_{OUT} for BUCK3 and BUCK4 reduces the ripple below the minimum target and limits the noise. Filtering components may be added if desired, including passive filters or LDOs. If using an LDO, tying CTRL6 high selects a higher V_{OUT} on BUCK3 and BUCK4 to accommodate the LDO dropout.

4.1 BOM Selection for High Efficiency

4.1.1 Inductor Selection

When selecting inductors for high efficiency, select inductors that reduce the ripple current, which effectively minimize core losses, and with low DCR values (see Table 2). Using larger inductor sizes allow this DCR and core loss decrease at the expense of solution size, but can produce the highest efficiency possible. See Equation 1 to calculate the recommended inductance.

$$L = (V_{IN} - V_{OUT}) \times V_{OUT} / V_{IN} / f_{SW} / I_{OUT} / k_{IND} \quad (1)$$

Set k_{IND} between 20% to 30% for higher efficiency.

Table 2. High Efficiency Inductors Selected

RAIL	VENDOR	INDUCTOR
VCCINT	Würth	744309047
VCCPINT	Würth	744325180
VAUX	Würth	74437368022
VMGTAVCC	Würth	744777001
VMGTAVTT	Würth	744777001
VCCOPIO	Würth	74437368022
VCCODDR	Würth	744325180

4.1.2 MOSFET Selection

High-efficiency MOSFETs have low Rds_{ON}, gate capacitance, and forward-voltage drop for the body diode. Using dual-package MOSFETs reduces ringing on the switch node that decreases efficiency and causes excessive overshoots on the SW pins. Severe overshoots on the SW node can reach up to two times the typical V_{IN}, which can damage the MOSFETs or the PMIC. For an RRH high-efficiency design, TI recommends to select the CSD87331Q3D.

Calculators can be utilized to test the performance of a selected field-effect transistor (FET). See the MOSFET Power Loss Calculator for a calculation tool to assist with the selection of the lowest power loss FETs (http://www.ti.com/tool/mosfet-loss-calc).

4.1.3 Output Capacitor Selection

RRH designs with Xilinx Zynq® UltraScale+™ require high-performance transient responses, which means the output capacitance must be increased to hold the output voltage while the inductor current ramps up. Because the inductor current ramp slows with increased k_{IND}, extra capacitance is required.

4.2 Sized-Down BOM Selection

Refer to the preceding Section 4.1.1 for guidance when selecting the BOM for rails. To optimize the solution for a sized-down version, TI recommends setting k_{IND} to 50% for inductor calculations and to use the CSD85301Q2D device for lower load currents below 5-A DC (see Table 3).

Table 3. Sized-Down Inductor Recommendations

RAIL	VENDOR	INDUCTOR
VCCINT	Würth	744309047
VCCPINT	Würth	744383560056
VAUX	Würth	74438356010
VMGTAVCC	Würth	744383560056
VMGTAVTT	Würth	744383560056
VCCOPIO	Würth	74438356010
VCCODDR	Würth	74438356010

Using sized-down inductors and MOSFETs for lightly-loaded controllers can save an estimated 440 mm^2 of BOM area as compared to the HE variant design.

5 Getting Started Hardware

5.1 Hardware Setup

The reference design platform comprises three different pieces of hardware as follows:

1. PMP12004 reference design board
2. USB2ANY box – plugs into J21 on the PMP12004 board
3. USB-to-GPIO – plugs into J22 on the PMP12004 board

5.2 Power on

To power on, first set CTRL pin 3 and CTRL pin 5 to the open setting. These pins initiate the turnon sequence and turn on the VTTLDO after all the other required rails are valid. Next, (with the power off), plug in the V_{IN} supply to the VSYS jack J1. The design is best suited for 12-V inputs. Turn on the power supply to power on the entire system according to the sequence required for the Zynq UltraScale+.

6 Test Setup

6.1 Efficiency

The efficiency was measured with only the particular rail under test enabled and the I_Q of the board was subtracted from the I_{IN} of each efficiency sweep. For the controllers, the 5-V drive source was added to the P_{IN}.

6.2 Transients

The transients were tested with a simple power FET at the rail terminal blocks. The bypass caps recommended by the Xilinx Zynq UltraScale+ were placed near the terminal blocks, where applicable. The output voltage was measured across the output capacitor closest to the load. The tip and ring method was used to measure the output voltage. For more information on the best measurement techniques, consult the following guide: *Understanding, Measuring, and Reducing Output Voltage Ripple*.

6.3 Output Ripple

The tip and ring method was used to measure the output voltage. For more information on the best measurement techniques, consult the following: *Understanding, Measuring, and Reducing Output Voltage Ripple*.

6.4 Thermal

The thermal image was captured five minutes after 50% loading had been applied to all the output rails of the system. The measured ambient temperature was 23° C.

7 Test Data

Table 4. Available Test Data

TEST TYPE	TEST RAILS	TEST DEFINITIONS	TEST CONDITIONS	FIGURE
Efficiency	TPS544C25 - VCCINT	Efficiency versus I_{OUT}	V_{IN} = 12 V, V_{OUT} = 0.72 V, 744309047 Würth Inductor	Figure 3
	TPS6508640 BUCK1 - 3.3V	Efficiency versus I_{OUT}	V_{IN} = 12 V, V_{OUT} = 3.3 V, 74437368022 Würth Inductor	Figure 4
	TPS6508640 BUCK2 - VCCPINT	Efficiency versus I_{OUT}	V_{IN} = 12 V, V_{OUT} = 0.85 V, 744325180 Würth Inductor	Figure 5
	TPS6508640 BUCK3 - VMGTAVTT	Efficiency versus I_{OUT}	V_{IN} = 3.3 V, V_{OUT} = 1.4 V, 744777001 Würth Inductor	Figure 6
	TPS6508640 BUCK4 - VMGTAVCC	Efficiency versus I_{OUT}	V_{IN} = 3.3 V, V_{OUT} = 1.1 V, 744777001 Würth Inductor	Figure 7
	TPS6508640 BUCK5 - 1.8V AUX	Efficiency versus I_{OUT}	V_{IN} = 3.3 V, V_{OUT} = 1.8V, 74437368022 Würth Inductor	Figure 8
	TPS6508640 BUCK6 - VCCODDR	Efficiency versus I_{OUT}	V_{IN} = 12 V, V_{OUT} = 1.2 V, 744325180 Würth Inductor	Figure 9
Load transient	TPS544C25 - VCCINT	Ch1: I_{OUT} (1 V = 10 A), Ch4: SW node, Ch2: V_{OUT}	Load transient 0 A to 6 A	Figure 10
	TPS6508640 BUCK1 - 3.3V	Ch1: I_{OUT} (1 V = 10 A), Ch4: SW node, Ch2: V_{OUT}	Load transient 0 A to 2.5 A	Figure 11
	TPS6508640 BUCK2 - VCCPINT	Ch1: I_{OUT} (1 V = 10 A), Ch4: SW node, Ch2: V_{OUT}	Load transient 0 A to 1 A	Figure 12
	TPS6508640 BUCK3 - VMGTAVTT	Ch1: I_{OUT} (1 V = 10 A), Ch4: SW node, Ch2: V_{OUT}	Load transient 0 A to 1 A	Figure 13
	TPS6508640 BUCK4 - VMGTAVCC	Ch1: I_{OUT} (1 V = 10 A), Ch4: SW node, Ch2: V_{OUT}	Load transient 0 A to 1 A	Figure 14
	TPS6508640 BUCK5 - 1.8V AUX	Ch1: I_{OUT} (1 V = 10 A), Ch4: SW node, Ch2: V_{OUT}	Load transient 0 A to 0.5 A	Figure 15
	TPS6508640 BUCK6 - VCCODDR	Ch1: I_{OUT} (1 V = 10 A), Ch4: SW node, Ch2: V_{OUT}	Load transient 0 A to 0.5 A	Figure 16
Output ripple	TPS6508640 BUCK1 - 3.3V	Ch2: V_{OUT}, Ch4: SW node	V_{IN} = 12 V, I_{OUT} = 5 A	Figure 17
	TPS6508640 BUCK2 - VCCPINT	Ch2: V_{OUT}, Ch4: SW node	V_{IN} = 12 V, I_{OUT} = 3 A	Figure 18
	TPS6508640 BUCK3 - VMGTAVTT	Ch2: V_{OUT}, Ch4: SW node	V_{IN} = 3.3 V, I_{OUT} = 2 A	Figure 19
	TPS6508640 BUCK4 - VMGTAVCC	Ch2: V_{OUT}, Ch4: SW node	V_{IN} = 3.3 V, I_{OUT} = 2 A	Figure 20
	TPS6508640 BUCK5 - 1.8V AUX	Ch2 - V_{OUT}, Ch4: SW node	V_{IN} = 3.3 V, I_{OUT} = 1.1 A	Figure 21
	TPS6508640 BUCK6 - VCCODDR	Ch2: V_{OUT}, Ch4: SW node	V_{IN} = 12 V, I_{OUT} = 2 A	Figure 22
Sequence	Sequence from CTL3 SYSEN to VCCINT	—	—	Figure 23
	Sequence from VCCINT to VMTGAVCC	—	—	Figure 24
	Sequence from CTL4 to VMGTAVCCAUX	—	——	Figure 25
	Sequence from CTL4 to LDOA1	—	—	Figure 26
	Sequence CTL5 Enabling VTT	—	—	Figure 27
Thermal	All rails	Thermal image with FLIR during operation	All rails loaded 50% of max design to currents, ambient temperature = 23°C, soak time = 5 min	Figure 28

7.1 Efficiency

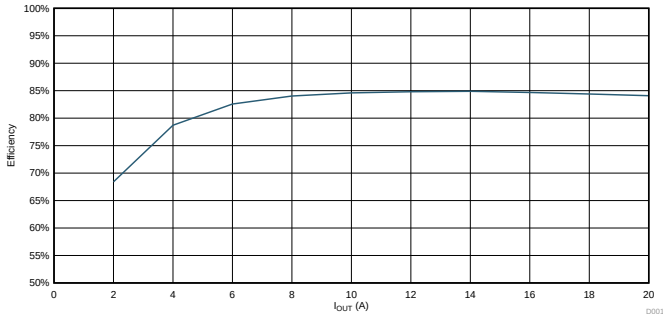


Figure 3. TPS544C25 – VCCINT Efficiency

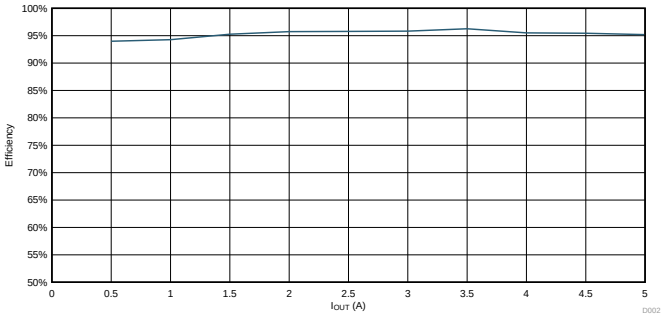


Figure 4. TPS6508640 BUCK1 – 3.3-V Efficiency

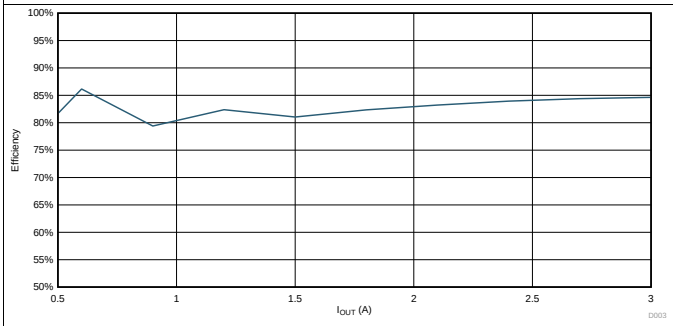


Figure 5. TPS6508640 BUCK2 – VCCPINT Efficiency

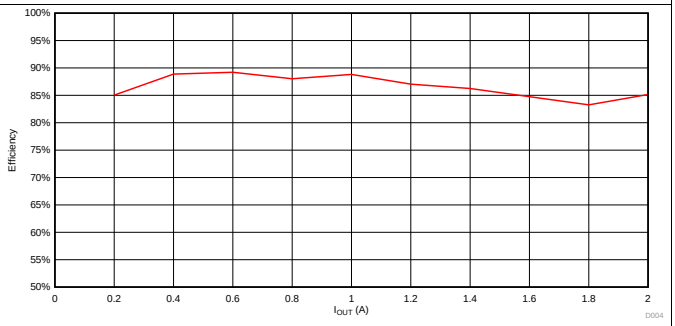


Figure 6. TPS6508640 BUCK3 – VMGTAVTT Efficiency

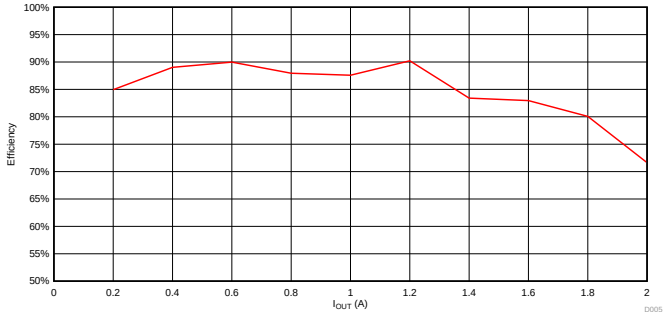


Figure 7. TPS6508640 BUCK4 – VMGTAVCC Efficiency

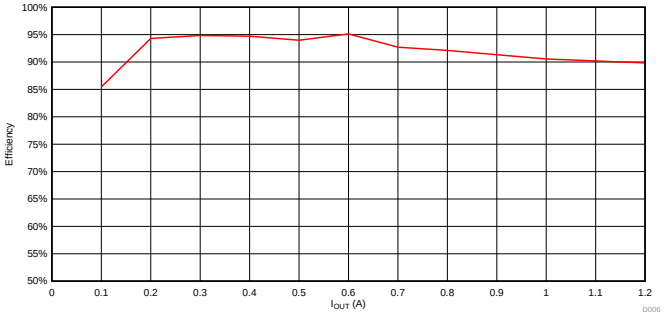


Figure 8. TPS6508640 BUCK5 – 1.8-V AUX Efficiency

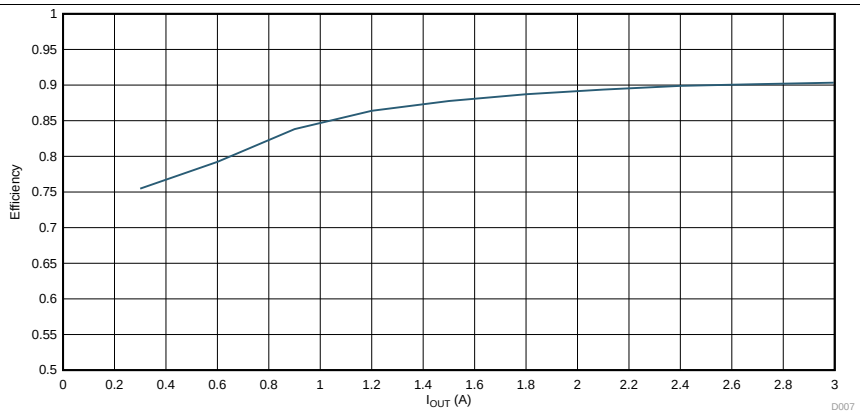


Figure 9. TPS6508640 BUCK6 – VCCODDR Efficiency

7.2 Transients

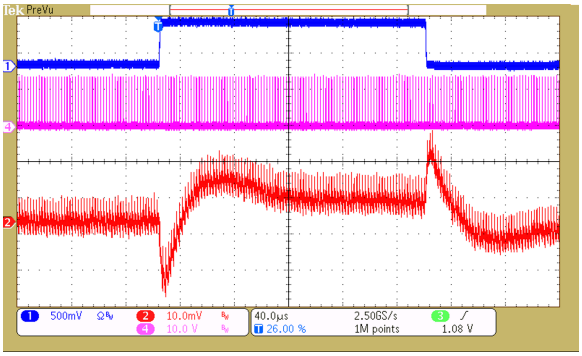


Figure 10. TPS544C25 – VCCINT

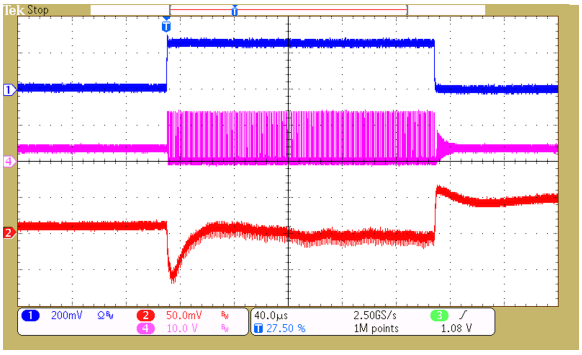


Figure 11. TPS6508640 BUCK1 – 3.3-V Load Transient

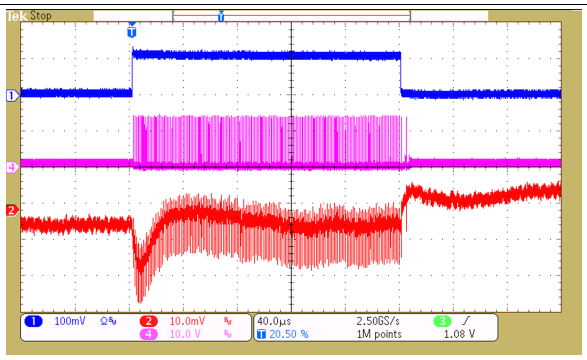


Figure 12. TPS6508640 BUCK2 – VCCPINT Load Transient

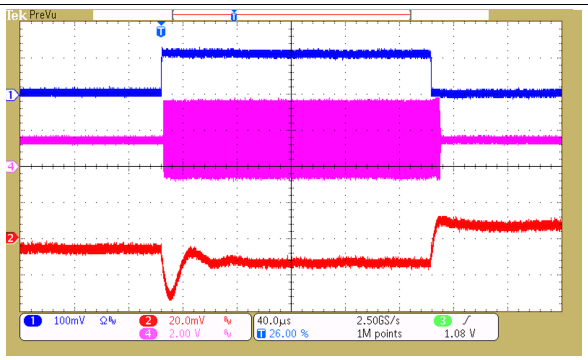


Figure 13. TPS6508640 BUCK3 – VMGTAVTT Load Transient

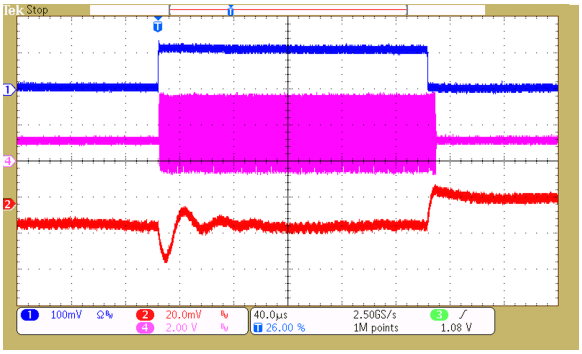


Figure 14. TPS6508640 BUCK4 – VMGTAVCC Load Transient

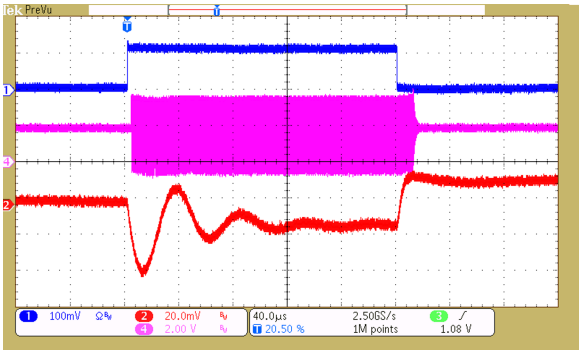


Figure 15. TPS6508640 BUCK5 – 1.8-V AUX Load Transient

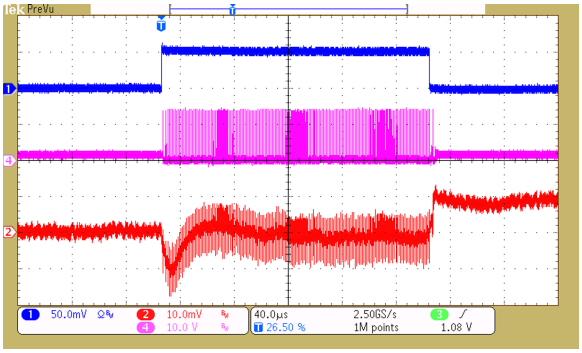


Figure 16. TPS6508640 BUCK6 – VCCODDR Load Transient

7.3 Output Ripple

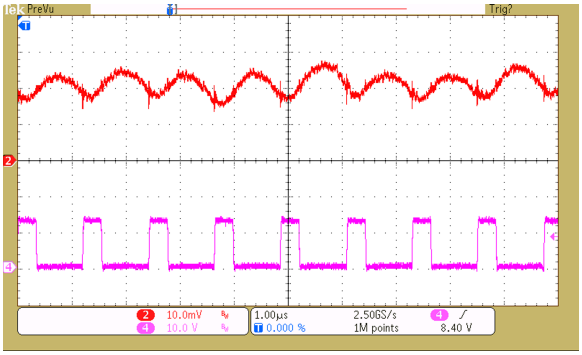


Figure 17. TPS6508640 BUCK1 – 3.3-V Output Ripple

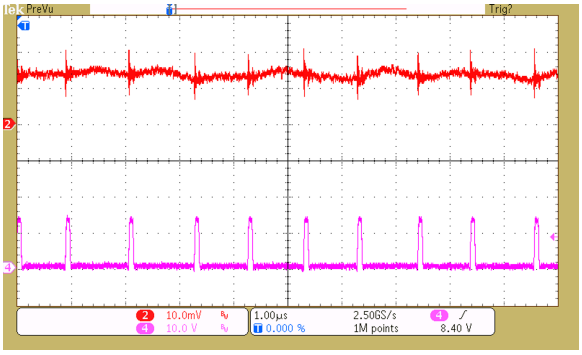


Figure 18. TPS6508640 BUCK2 – VCCPINT Output Ripple

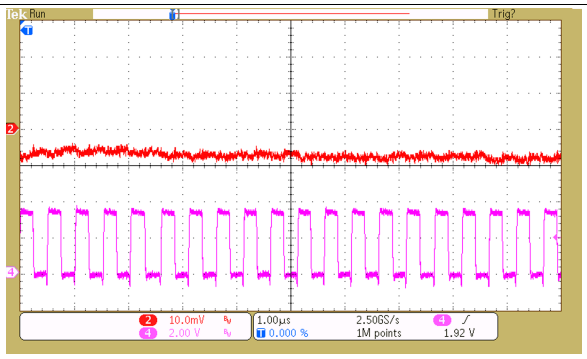


Figure 19. TPS6508640 BUCK3 – VGMTAVTT Output Ripple

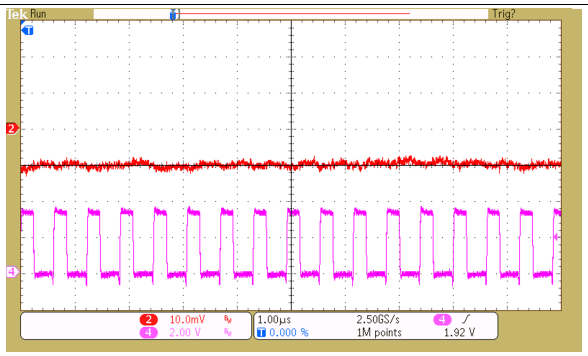


Figure 20. TPS6508640 BUCK4 – VMGTAVCC Output Ripple

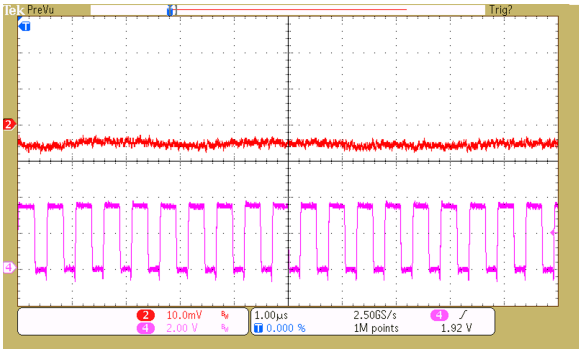


Figure 21. TPS6508640 BUCK5 – 1.8-V AUX Output Ripple

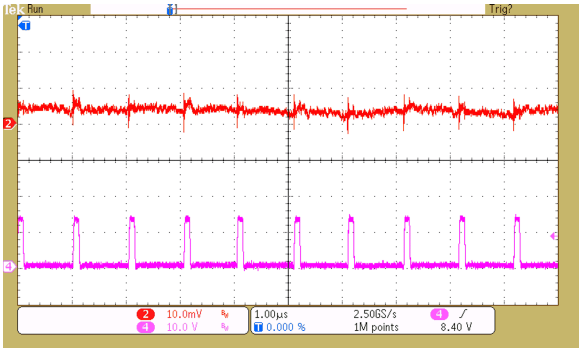


Figure 22. TPS6508640 BUCK6 – VCCODDR Output Ripple

7.4 Sequence

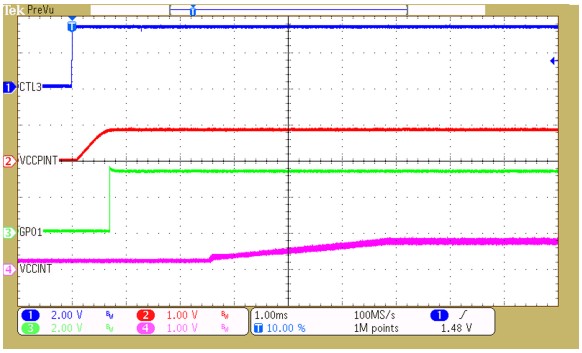


Figure 23. Sequence From CTL3 SYSEN to VCCINT

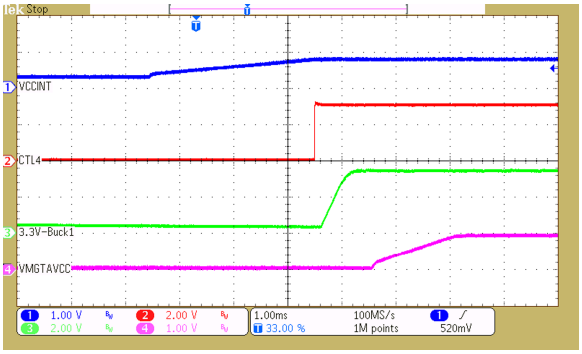


Figure 24. Sequence From VCCINT to VMTGAVCC

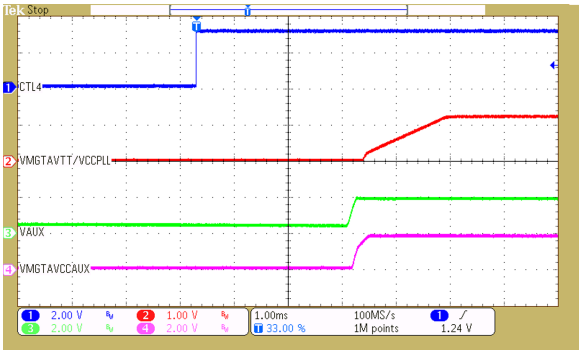


Figure 25. Sequence From CTL4 to VMGTAVCCAUX

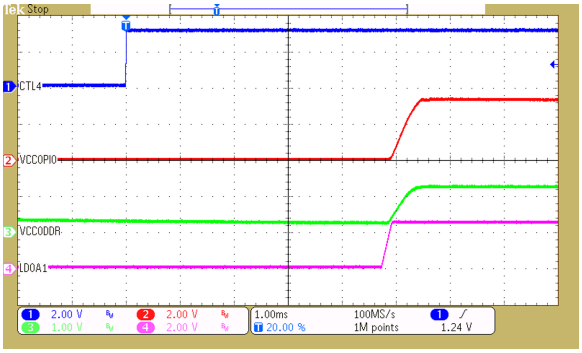


Figure 26. Sequence From CTL4 to LDOA1

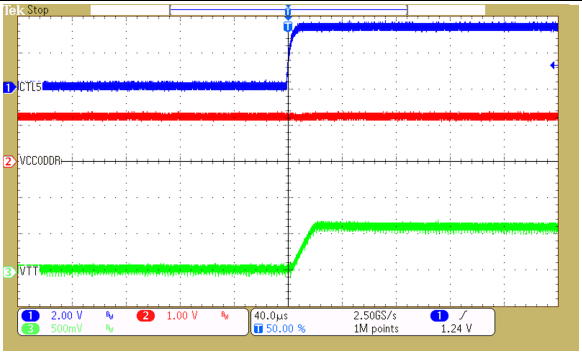


Figure 27. Sequence CTL5 Enabling VTT

7.5 Thermal Performance

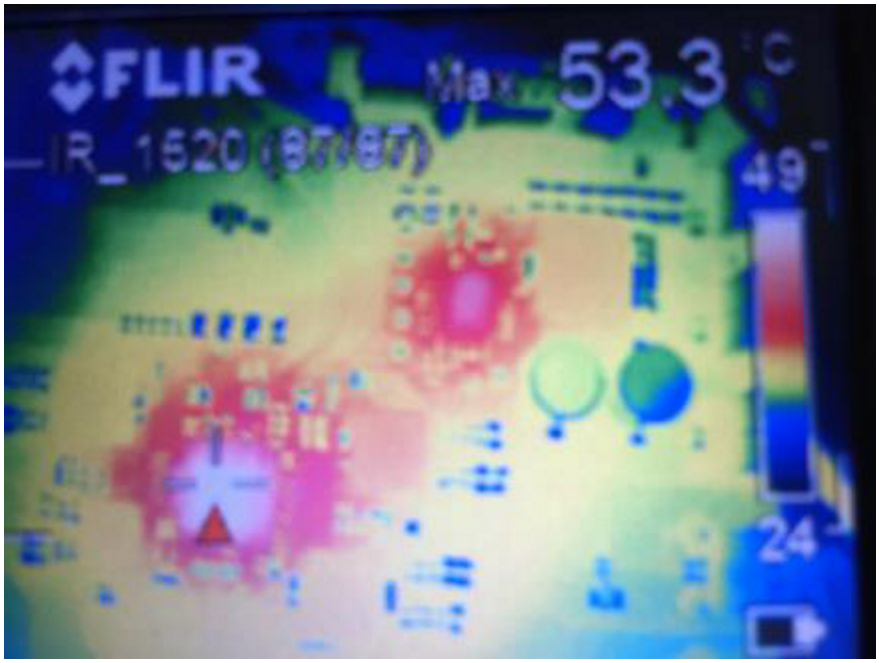


Figure 28. Thermal Performance of PMP12004-HE Design

8 Design Files

8.1 Schematics

To download the schematics, see the design files at PMP12004-HE.

8.2 Bill of Materials

To download the bill of materials (BOM), see the design files at PMP12004-HE.

8.3 PCB Layout Recommendations

For an example layout, refer to the PMP12004-HE board files at PMP12004-HE.

8.3.1 TPS6508640 and CSD87331Q3D

For all switching power supplies, the layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the regulator can have stability problems and EMI issues. Therefore, use wide and short traces for the main current path and for the power ground tracks. The input capacitors, output capacitors, and inductors must be placed as close as possible to the IC. Use a common-ground node for power ground and use a different, isolated node for control ground to minimize the effects of ground noise. Connect these ground nodes close to the AGND pin by one or two vias. Below is a list of other basic requirements and guidelines:

- Do not allow the AGND, PGNDSNSx, or FBGND2 to connect to the thermal pad on the top layer.
- To ensure proper sensing based on FET, the Rds_{ON} and PGNDSNSx must not connect to PGND until very close to the PGND pin of the FET.
- All inductors, input and output caps, and FETs for the converters and controller must be on the same board layer as the IC.
- To achieve the best regulation performance, place feedback connection points near the output capacitors and minimize the control feedback loop as much as possible.
- Bootstrap capacitors must be placed close to the IC.
- The internal reference regulators must have their input and output caps placed close to the IC pins.
- Route DRVHx and SWx as a differential pair. Ensure that there is a PGND path routed in parallel with DRVLx, which provides optimal driver loops.

8.3.2 TPS544C25

- As with any switching regulator, there are several signal paths that conduct fast switching voltages or currents. Minimize the loop area formed by these paths and their bypass connections
- Bypass the V_{IN} pins to GND with a low-impedance path. Power-stage input bypass capacitors should be as close as physically possible to the V_{IN} and GND pins. Additionally, a high-frequency bypass capacitor in 0402 package on the V_{IN} pins can help to reduce switching spikes, which can be tucked right underneath the IC on the other side of the PCB to keep a minimum loop.
- The BP6 bypass capacitor carries large switching current for gate driver. Bypassing the BP6 pin to GND with a low-impedance path is very critical to the stable operation of the TPS544x25 devices. Place BP6 high frequency bypass capacitors as close as possible to the device pins, with a minimum return loop back to ground.
- The VDD and BP3 also require good local bypassing. Place bypass capacitors as close as possible to the device pins, with a minimum return loop back to ground and this return loop should be kept away from fast switching voltage and main current path, as well as BP6 current path. Poor bypassing on VDD and BP3 can degrade the performance of the regulator.
- Keep signal components local to the device, and place them as close as possible to the pins to which they are connected. These components include the feedback resistors, the RT resistor, the VSET resistor, the SS resistor, as well as ADDR0 and ADDR1 resistors. These components should also be kept away from fast switching voltage and current paths. Those components can be terminated to GND with minimum return loop or bypassed to a separate low impedance analog ground (AGND) copper area, which is isolated from fast switching voltage and current paths and has a single

connection to PGND on the thermal tab through the AGND pin.

- The PGND pin (pin 26) must be directly connected to the thermal pad of the device on the PCB, with a low noise, low-impedance path to ensure accurate current monitoring.
- Minimize the SW copper area for the best noise performance. Route sensitive traces away from SW and BOOT, as these nets contain fast switching voltages, and lend easily to capacitive coupling.
- Snubber component placement is critical to its effectiveness of ringing reduction. These components should be on the same layer as the TPS544x25 devices and be kept as close as possible to the SW and GND copper areas.
- The V_{IN} and VDD pins must be the same potential for accurate short circuit protection, but high frequency switching noise on the VDD pin can degrade performance. VDD should be connected to V_{IN} through a trace from the input copper area. Optionally form a small low-pass R-C between V_{IN} and VDD, with the VDD bypass capacitor (1 µF) and a 0-2 Ω resistor between V_{IN} and VDD.
- Route the VOUTS+ and VOUTS– lines from the output capacitor bank at the load back to the device pins as a tightly coupled differential pair. Keeping these traces away from switching or noisy areas is critical, as they can add differential-mode noise.
- Routing of the temperature sensor traces is critical to the noise performance of temperature monitoring. Keep these traces away from switching areas or high current paths on the layout. TI also recommends to use a small 1-nF capacitor from TSNS/SS to AGND to improve the noise performance of temperature readings.

8.3.3 Layout Prints

To download the layer plots, see the design files at PMP12004-HE.

8.4 Altium Project

To download the Altium project files, see the design files at PMP12004-HE.

8.5 Gerber Files

To download the Gerber files, see the design files at PMP12004-HE.

8.6 Assembly Drawings

To download the assembly drawings, see the design files at PMP12004-HE.

9 References

1. Texas Instruments, *Understanding, Measuring, and Reducing Output Voltage Ripple*, TI E2E™ Online Community – SIMPLE SWITCHER® Wiki (http://e2e.ti.com/support/power_management/simple_switcher/w/simple_switcher_wiki/2243.understanding-measuring-and-reducing-output-voltage-ripple)

10 Terminology

Buck— A type of step down DC-DC regulator.

Converter— A DC-DC regulator with integrated FETs.

Controller— A DC-DC regulator that requires external FETs.

RRH— Remote radio head

BH— Backhaul

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (April 2016) to A Revision	Page
• Changed to updated block diagram	1
• Added improved diagram for ZU9EG/ZU15EG	3

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