TI Designs

Multi-Channel Analog Output Module With Multiplexed Single-Channel DAC for PLCs Reference Design

TI Designs

This multi-channel analog output module TI Design with a multiplexed single-channel digital-to-analog converter (DAC) for programmable logic controllers (PLCs) illustrates the design of a low-cost, high-speed, small form-factor, high-resolution PLC analog output module based on sequentially multiplexed sample and hold buffers.

Design Resources

TIDA-00760	Design Folder
DAC8760	Product Folder
MUX36S08	Product Folder
OPA188	Product Folder
XTR111	Product Folder

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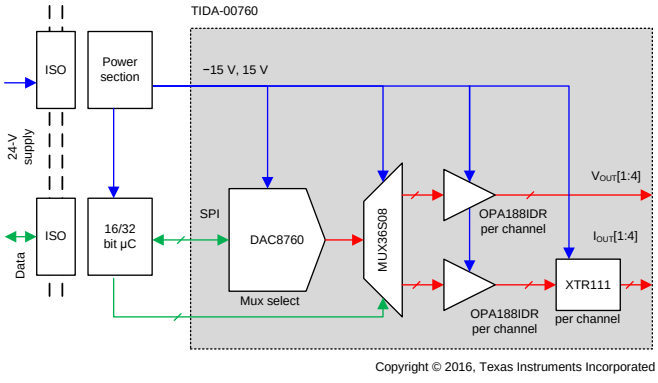
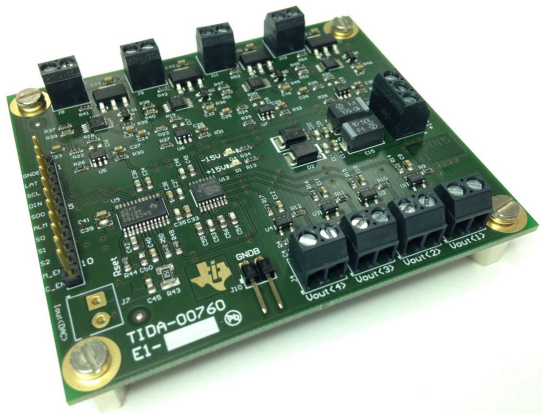
Design Features

- Multiplexed Eight Output Channels Module
  - Four Channels Voltage Output
  - Four Channels Current Output
- Single 16-Bit DAC (DAC8760)
- Effective Resolution
  - Voltage Output: 15 Bits
  - Current Output: 16 Bits
- Configurable Output Range
  - Voltage Output: ±10 V, 0 to 10 V, ±5 V, 0 to 5 V
  - Current Output: 0 to 20 mA, 4 to 20 mA, 0 to 24 mA
- Uncalibrated Output Accuracy
  - ±0.2% FS at 25°C
  - ±0.5% FS Over –40°C to 85°C
- Scan Time: 6 ms for Eight Channels
  - Conversion Time: 750 µs/Channel
- SPI I/O Controller Interface

Featured Applications

- PLC/DCS Analog/Mixed Output Modules
- Field Sensor and Process Transmitters





1 Introduction

In PLC systems, analog output (AO) modules are used to control actuators, valves, and motors in process control and factory environments. A generic reference diagram for PLC output module can be explored in the TI Analog Output Module Application page. Some exemplary PLC output modules are also available.

AO modules are defined mainly by features like output type (voltage or current), output range, load impedance range, number of channels supported, accuracy, resolution, settling time, and power.

Modern complex systems call for larger number of output channels per module; this typically translates into a higher cost and a larger module area. However, multi-channel output modules can be built at a lower cost with a small form factor. One way of reaching this goal is to use the concept of sample and hold (S&H) to generate multi-output from a single digital-to-analog converter (DAC).

The TIDA-00760 design provides an example of low-cost multi-channel output module solution based on the concept of S&H. The module uses a single DAC (DAC8760) in voltage output mode and a multiplexer followed by hold capacitors and buffer stages to make eight channels.

While a S&H concept based on capacitive storage elements is applied straight to voltage outputs, current outputs needs a conversion stage. This TI Design illustrates this conversion by providing four current outputs based on voltage-to-current conversion.

This design guide covers the major design steps in realizing the S&H multi-channel (voltage and current) output module including the concept, device selection, design choices, firmware, board design, and testing.

2 Design Specification

Table 1 shows the target specification set for this design. The parameters scan time, resolution, and accuracy are the most relevant to show the concept under consideration.

Table 1. Target Specification

ATTRIBUTE	VOLTAGE OUTPUT	CURRENT OUTPUT
AO channels	4	4
Output range	0 to 5 V 0 to 10 V –5 to 5 V –10 to 10 V	0 to 20 mA 4 to 20 mA 0 to 24 mA
Resolution	15 bits = 300 µV	14 bits = 1.2 µA
Output load impedance	> 2 kΩ 10 nF (with 0-Ω isolation) 20 nF (with 10-Ω isolation) 40 nF (with 20-Ω isolation) or 100 nF (with 100-Ω isolation)	< 600 Ω
Ambient operating temperature	–40°C to 85°C	
Uncalibrated accuracy at 25°C	0.2% FS	0.2% FS
Uncalibrated accuracy over –40°C to 85°C	0.5% FS	0.5% FS
Scan time (8 channels)	6 ms = 750 µs per channel	
Settling time	< 300 µs (V_{OUT} at 100-nF capacitive load)	
Power consumption (no load)	< 0.5 W for all channels	

Other design aspects like power supply requirements, power consumption, isolation, and protection are discussed already in detail in other designs. Check TIDA-00118 and TIDA-00231 for more information about aspects of isolation, protection, and power.

3 System Description

Like a generic PLC output module, the S&H multiplexed PLC output module contains galvanic isolation components for power and data, as well as output protection circuits.

The S&H multiplexed PLC output module has at the core a high-precision single-channel DAC driven by a microcontroller or microprocessor followed by a multiplexer that drives the S&H buffers to the voltage output directly, or succeeded by a voltage-to-current converters to the current outputs.

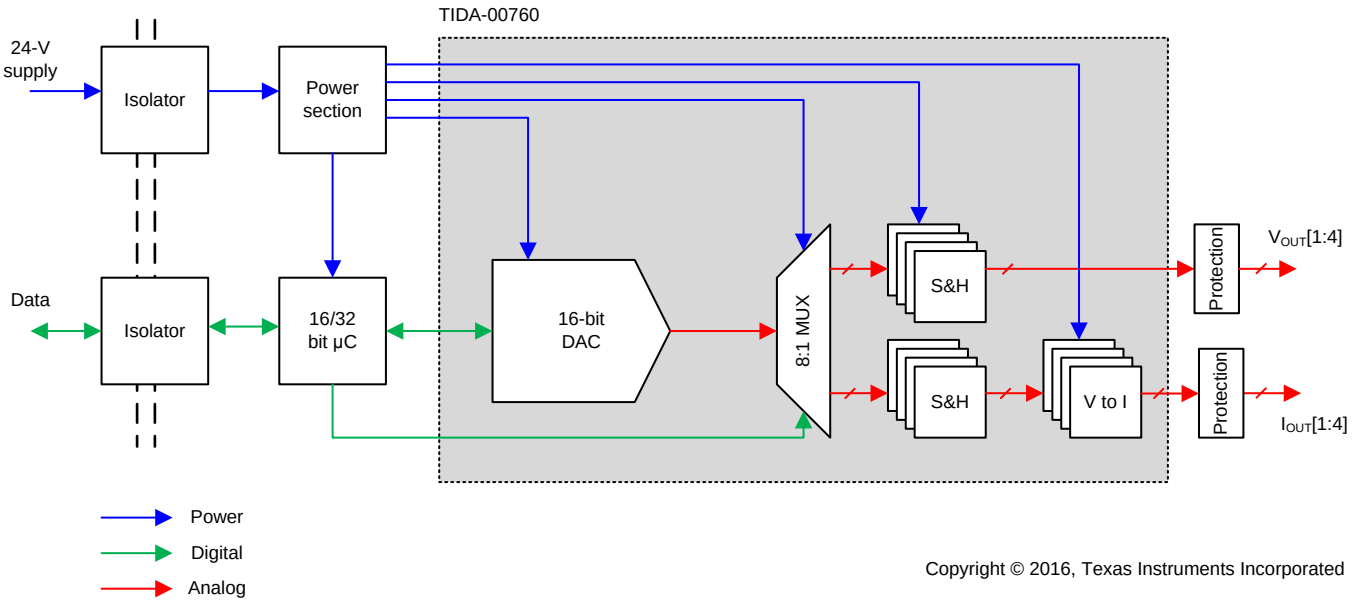


Figure 1. Generic S&H Multiplexed DAC PLC AO Module

The greyed area in Figure 1 shows the focus of this design (TIDA-00760). Separate voltage and current paths are targeted here for illustration, although a combined voltage/current path can easily be implemented as detailed in the TI Design TIPD155.

A 15-bit target resolution means at least a 16-bit DAC is required. This would also favor a 16- or 32-bit microcontroller.

Although most of TI's new generation of DACs provide both voltage and current outputs; in an S&H module, only voltage output is needed across all channels as capacitors are used as analog storage elements for voltage. The DAC only generates a voltage signal, and a voltage-to-current (V2I) converter is used to translate it for current outputs.

4 Component Selection

This section covers the recommended devices to ensure a higher performance and lowest possible cost.

4.1 Microcontroller Selection

TI's MSP430 versatile, low-cost microcontroller lends itself naturally to this application. The device is simple to code, affordable, and available in a wide range of packages and performance levels to give the designer the ability for future upgrade and scalability. The MSP430 had easily met our timing and processing requirements for this design (see the microcontroller selection guide).

Although the MSP430 is not a part of the TIDA-00760, the design was made with MSP430 selection in mind, as the firmware is an integral part of this design.

4.2 Supply Requirement

The ±10-V output requirement dictates a bipolar voltage supply of at least ±12 V.

Although the minimum power supply is preferred from power consumption perspective, the selected power supply would put a maximum limit to the resistive load of the current outputs. If 1 V is assumed as the voltage headroom for the current driver, a minimum of 15 V is required for a 24-mA output current and a 600-Ω load. A higher resistive load can be driven if a higher level supply is used.

$$R_{MAX} = \frac{V_{SUPPLY} - V_{HEADROOM}}{I_{MAX}} \quad (1)$$

This power level requirement is only applied to the output stage, The DAC and the MUX can be driven by a lower level supply as they have 10 V as the maximum output. However, it is much more convenient and simpler from power perspective to use the same supplies for the whole signal chain, including the DAC, the MUX, the S&H buffers as well as the V2I converters.

A unified dual rail supply of ±15 V is selected for this design. If the microcontroller is added to the board, it could be powered directly by a high efficiency LDO driven from the 15-V supply, or more efficiently from the DAC internally generated DVDD supply. Most modern TI DACs have an optional internal DVDD generator.

One possible realization of a ±15-V isolated power supply from a 24-V field supply is shown in Figure 2, which is based on the TPS54062 Buck converter, and the TPS7A49 (150 mA) and TPS7A30 (200 mA) linear regulators.

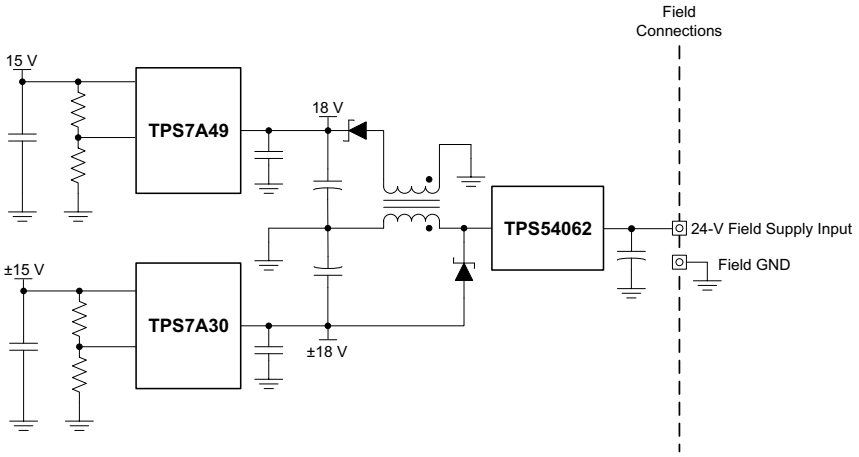


Figure 2. Isolated Power Supply for ±15-V Output

Another alternative for this power tree is to use the LM5017 step-down converter and the TPS7A30 for the positive rail regulation as explained in the TIDA-00118 reference design (TIDU189).

For a more elaborate search, use the TI Power Architect online power design tool.

Current consumption per current output is 24 mA/channel. Current consumption per voltage output is 5 mA/channel. Therefore, at least a current of 120 mA is required from the 15-V supply only for the loads. The –15-V requirement is less for this unipolar current output design. 20 mA is required for the loads from the –15-V supply. Add intrinsic current requirements on top of those load requirements.

4.3 DAC Selection

The DAC is the cornerstone for this application. Apart from meeting the resolution and accuracy requirements, the DAC must have a fast settling time to allow for a lower scan time. The DAC required for this application belongs to precision DACs (> 16 bits, < 10 MSPS). SPI is preferred for achieving higher speeds.

At least two TI DACs (Precision DAC selection page) fulfill this basic criteria with the industrial temperature range: DAC8871 and DAC8760. Both work from a dual supply up to 18 V and feature a pretty short settling time. The DAC8871, however, is unbuffered, meaning it would require a buffer stage. The DAC8760 enables more integration, a lower cost, and higher performance for this application.

4.4 Analog Multiplexer Selection

TI has a pretty rich multiplexer product portfolio. The most relevant specifications for this application is its low input and output capacitance and low ON impedance to enable short settling with larger hold capacitors. The MUX has to work with >±15-V supply as well with low leakage to reduce the voltage droop on the hold capacitor.

The MUX36S08 fulfills these requirements with a typical series resistance of 150 Ω. The MUX can work with a dual supply voltage up to 36 V, allowing extensions and upgrades. The four-channel version (MUX36D04) is also available for design variations requiring four channels.

4.5 V2I Converter Selection

In this application, the output current requirement is defined by the 4- to 20-mA loop requirements. A suitable choice for conversion is to use the 4- to 20-mA conditioner driven directly by the S&H buffer, meaning an input range of 0 to 12 V. The converter can be designed to work with a lower input range by reconfiguring the DAC range. The conditioner has to work with a dual supply ±15 V, and covers the industrial operating temperature range.

The XTR111 fulfills these requirements and offers a cost effective solution as well as a quite small form factor. If a bipolar current output or a combined voltage/current output is required, use the XTR300.

4.6 S&H Circuit Selection

S&H circuits consist of the MUX switch and the output hold capacitor plus a buffer to drive the output. To reduce the error contributed by the S&H buffer circuit, a low offset precision operational amplifier is used. A precision amplifier implies low leakage and low offset current as well as low noise. There is a handful of TI amplifiers that fulfill this criteria (Precision Amplifier Overview) and work from a dual supply of > 30 V, both in single and multi-amplifier packages. Single amplifier parts are considered for simplicity and higher channel-to-channel signal isolation.

The OPA188 is a very attractive choice for this design. It has an extremely low offset and offset drift over a very wide temperature range. The device also features low noise and adequate slew rate and is available in different package sizes for a low cost.

4.7 Summary

Figure 3 summarizes the components selected for this design.

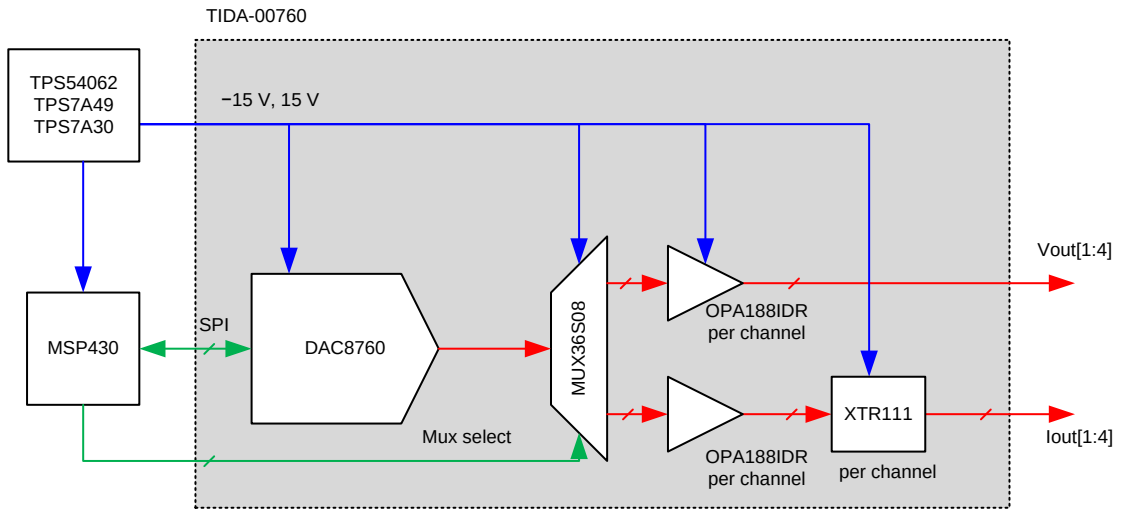


Figure 3. Component Selection for TIDA-00760

5 Circuit Description and Operation

5.1 Concept of Operation

In a multiplexed output module, the controller scans through all channels (or an arbitrary number of channels based on user configuration) by updating the DAC output for the desired channel output value and switches the MUX channel to connect to the desired output. This concept is illustrated in Figure 4 for three channels with three different static output levels. Static means that for one output, the voltage is not changing from one sample to the next.

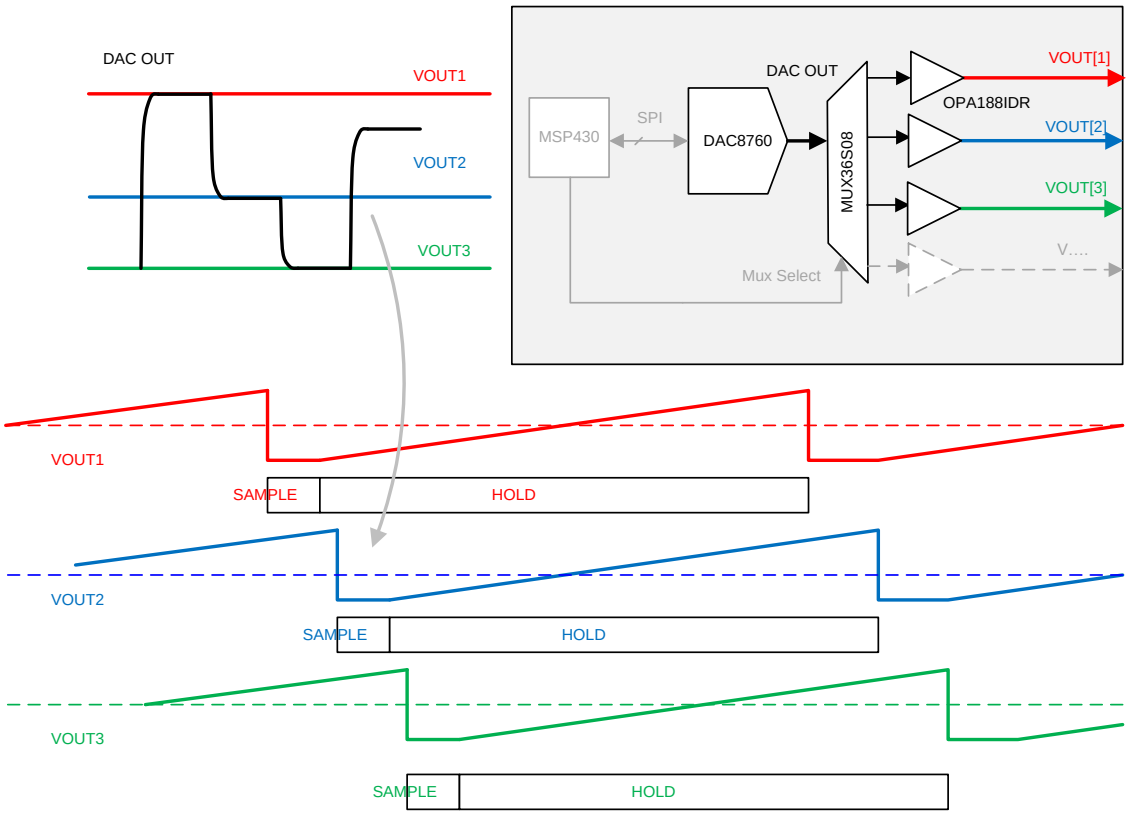


Figure 4. Concept of Multiplexed DAC S&H Outputs

Each channel goes through S&H cycles while DAC is continuously changing values. The hold circuit for each output channel is keeping the value while the channel is disconnected from the DAC output. The sampled value will drift due to leakage; in this circuit, the drift is upwards due to the nature of the MUX floating output. The effective output is the average voltage as indicated by the dashed line in Figure 4.

Peak-to-peak drift adds to the module inaccuracy, so minimizing this drift is a design target. Drift is a function of the hold capacitor and the sum of all leakage currents as well as the hold time.

5.2 Detailed Scan Cycle

If the MUX is switched to the desired channel and then the DAC value of that channel is updated, there can be huge spikes on static outputs if channel values are widely separated. To avoid these spikes, switch off the MUX while updating the DAC value, and wait long enough for the DAC output to settle. Then, the desired MUX channel is enabled before the MUX is switched on again.

This sequence ensures minimum impact from switching on static outputs. The downside is the dead time for the update, a slightly longer time for hold, and a shorter time for the hold capacitor to settle by taking a portion of the cycle for DAC output settling. However, with all these effects, the output of this sequence is the optimum trade-off between ensuring little disturbance of static outputs and allowing for one cycle settling of dynamic output.

A detailed scan cycle for one channel is shown in Figure 5. Note that the channel time slot (scan time divided by the number of channels) is divided into three portions: DAC update, DAC settling, and Sample or Refresh. This division shows that the actual sample time is a fraction of the channel scan time. It is desired to maximize this fraction and minimize the update time. The DAC settling time should be optimized; a too small DAC settling time would negatively affect static outputs and reduce system accuracy, while a too large DAC settling time would cannibalize the effective sample time.

The channel scan cycle goes as follows:

1. First, MUX is disabled to avoid corrupting the outputs [MUX_EN goes low].
2. The corresponding DAC value is sent through SPI to the DAC [SETOUT(X)].
3. In the meantime, or later, the MUX channel is selected [MUX_SEL].
4. Latch is asserted to update the DAC output with the new value [Latch].
5. Time is given to the DAC to settle the new value [DAC Settle until DAC out reaches Out(X)].
6. MUX is enabled, connecting the sample cap to the DAC output [MUX_EN goes high].
7. According to the difference between the previous value of the channel and Out(X), the DAC output might experience a disturbance, which does not appear on the output due to the large cap and filtering.
8. Finally, MUX is disabled for updating the next channel until the MUX cycles to the same channel again; the hold cap will keep the output value static.

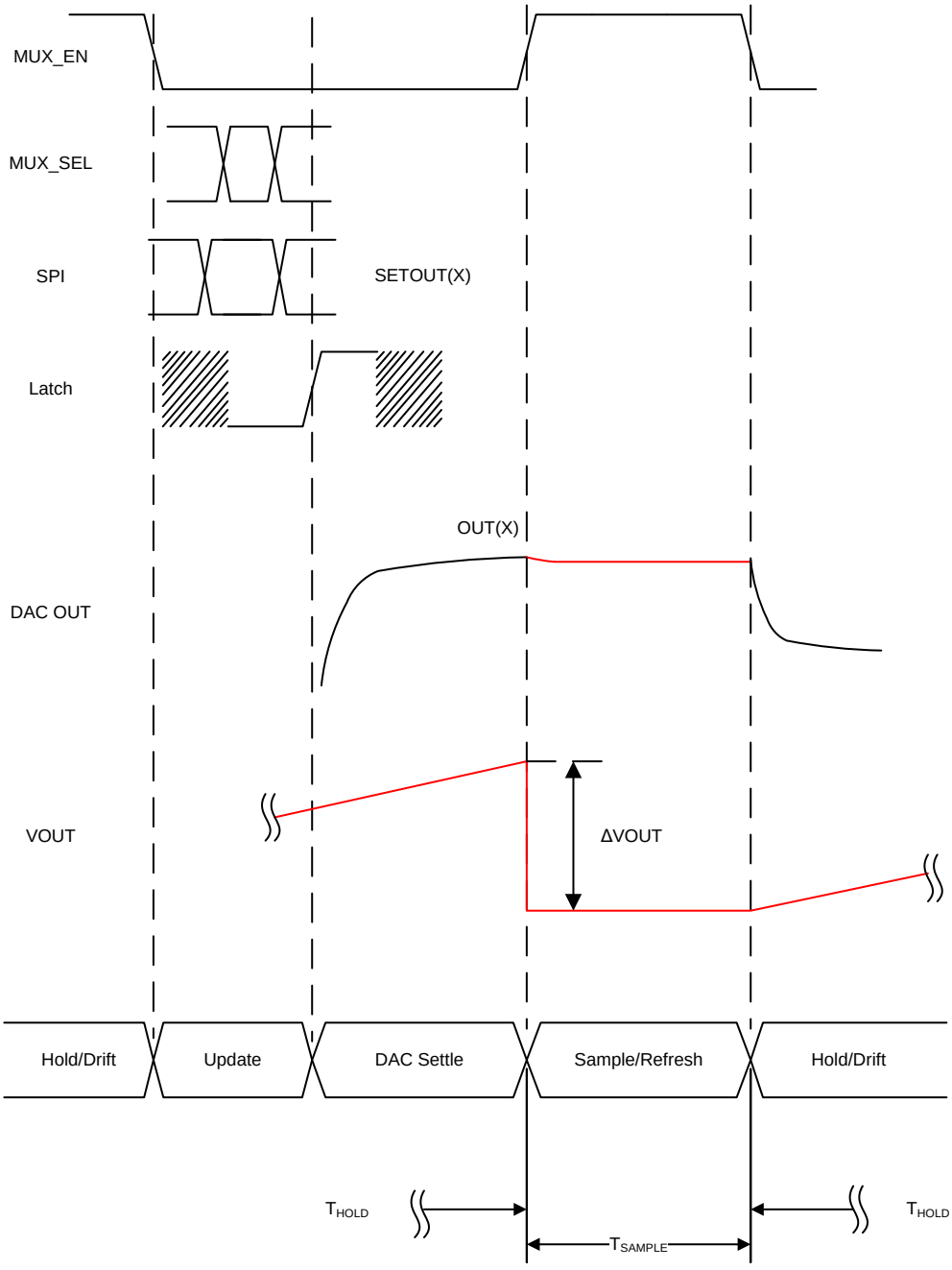


Figure 5. Detailed Channel Scan Cycle

6 Design Procedure

6.1 DAC Circuit

The DAC8760 is designed for industrial and process control applications. The DAC8760 can provide 4- to 20-mA, 0- to 20-mA, or 0- to 24-mA current outputs or 0- to 5-V, 0- to 10-V, ±5-V, or ±10-V voltage outputs with a 10% over range (0– to 5.5-V, 0– to 11-V, ±5.5-V, or ±11-V) capability. The DAC8760 internal block diagram is shown in Figure 6.

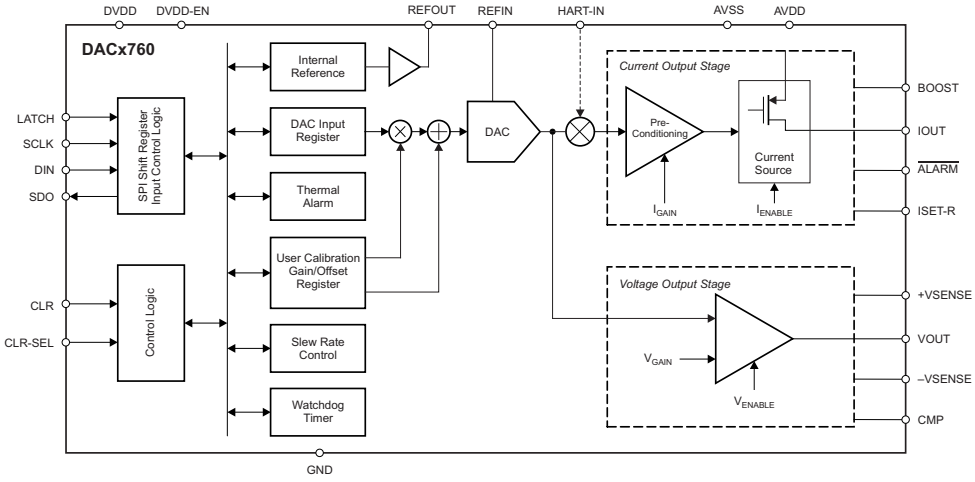


Figure 6. DAC8760 Internal Block Diagram

The TIDA-00760 only uses the voltage output. When The DAC8760 is configured for voltage output, the minimum load allowed is 1-kΩ minimum at 10 mA. For voltage output, the module uses 15 V and –15 V at power supply rails, thus providing 5 V of headroom.

The relation between input code and output voltage is given by

$$V_{OUT} = V_{REF} \times GAIN \times \frac{CODE}{2^N}, \text{ for unipolar output mode} \quad (2)$$

$$V_{OUT} = V_{REF} \times GAIN \times \frac{CODE}{2^N} - GAIN \times \frac{V_{REF}}{2^N}, \text{ for unipolar output mode} \quad (3)$$

where CODE is the decimal equivalent of the DAC data register, N = 16 is the resolution, V_{REF} = 0.5 V, and GAIN is automatically selected based on the selected range as in Table 2.

Table 2. Voltage Output Range versus Gain Setting

VOLTAGE OUTPUT RANGE	GAIN
0 to 5 V	1
0 to 10 V –5 to 5 V	2
–10 to 10 V	4

The DAC code is fed to the device by writing the DATA register. An overview of the device register map is shown in Table 3.

Table 3. DAC8760 Register Map

REGISTER / COMMAND	READ/WRITE ACCESS	DATA BITS (DB15:DB0)														
		15	14	13	12	11	10:9	8	7	6	5	4	3	2	1	0
Control	R/W	CLRSEL	OVR	REXT	OUTEN	SRCLK			SRSTEP			SREN	DCEN	RANGE		
Configuration	R/W	X					IOUT RANGE	DUAL OUTEN	APD	Reserved	CALEN	HARTEN	CRCEN	WDEN	WDPD	
DAC data	R/W	D15:D0														
No operation	—	X														
Read operation	—	X									READ ADDRESS					
Reset	W															RESET
Status	R	Reserved										CRC-FLT	WD-FLT	I-FLT	SR-ON	T-FLT
DAC gain calibration	RW	G15:G0, unsigned														
DAC zero calibration	RW	Z15:Z0, signed														
Watchdog timer	—	X														

Before writing to the DAC DATA register, the control/configuration registers should be written to set the range and other settings.

In case calibration is needed, the gain/zero calibration registers should be written as well. Different calibration values can be used for different channels. If the designer is sure that a signal path mismatch does not add much error, then a single set of calibration settings can be used during for the configuration step in each scan cycle once for all channels.

The register configuration is done through SPI communication. The DAC8760 is controlled over a versatile four-wire serial interface (SDI, SDO, SCLK, and LATCH) that can operate at clock rates of up to 31 MHz and is compatible with SPI, QSPI™, Microwire™, and digital signal processing (DSP) standards. The SPI communication command consists of a write address byte and a data word for a total of 24 bits.

The default frame is 24 bits wide and begins with the rising edge of SCLK, which clocks in the MSB. The subsequent bits are latched on successive rising edges of SCLK. The default 24-bit input frame consists of an 8-bit address byte followed by a 16-bit data word.

The host processor must issue 24 bits before it issues a rising edge on the LATCH pin. Input data bits are clocked in regardless of the LATCH pin and are unconditionally latched on the rising edge of LATCH. By default, the SPI shift register resets to 000000h at power on or after a reset.

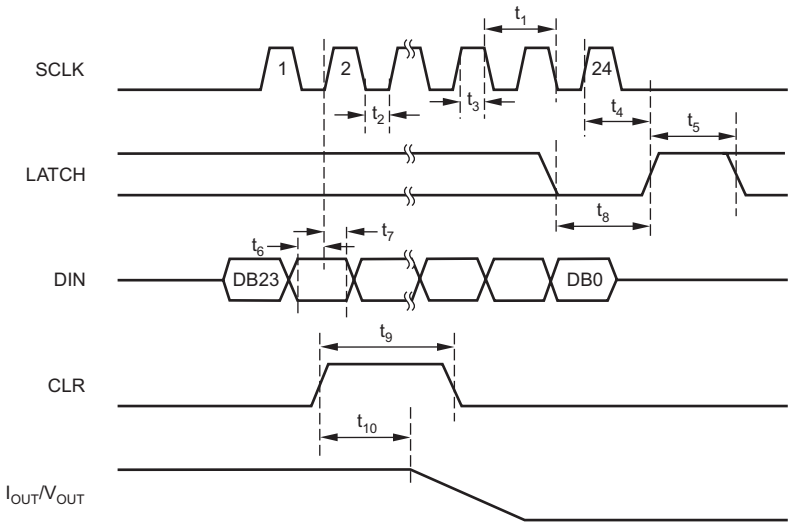


Figure 7. DAC8760 SPI Write Node Timing

DAC connectivity is pretty straightforward as shown in Figure 8:

- AVDD is connected to the 15-V supply; AVSS, PAD, and GND pins are connected to the –15-V supply.
- DVDD-EN is left floating to enable internal DVDD supply, which is required for low voltage SPI communication.
- An internal reference is used, which is why REFIN and REFOUT are tied together.
- SPI is connected to the SPI bus directly (LATCH,SCLK,DI, SDO).
- CLR-SEL and CLR are tied to ground as clear function is not used. HART-IN and BOOST are also left open as hart function is not used (same for the current boost function).
- Although a current output is not used, IOUT is connected for testing, and ISET-R reference resistor pin is connected to a 15-kΩ precision resistor for the user to check current output.
- VOUT is connected through 15 Ω, and the same value is used to connect to +VSENSE. These resistors are included as part of the protection scheme for the DAC8760. In an actual system, there are external clamp diodes and internal ESD structures, which resemble clamp diodes as well. These diodes conduct at different voltage, so series pass elements are included to help limit the current flow in each of them. Without this current limit, the forward voltage of the external clamp to rail diode would increase, making it a less effective clamp. The resistor between the external clamp and internal clamp reduces the current through the internal ESD cells.
- In a typical application, +VSENSE is preferably connected to the output node after the protection circuit. However, in this S&H application, it is not possible to connect the +VSENSE to the hold capacitors. The +VSENSE must be connected close to the DAC before the MUX input.

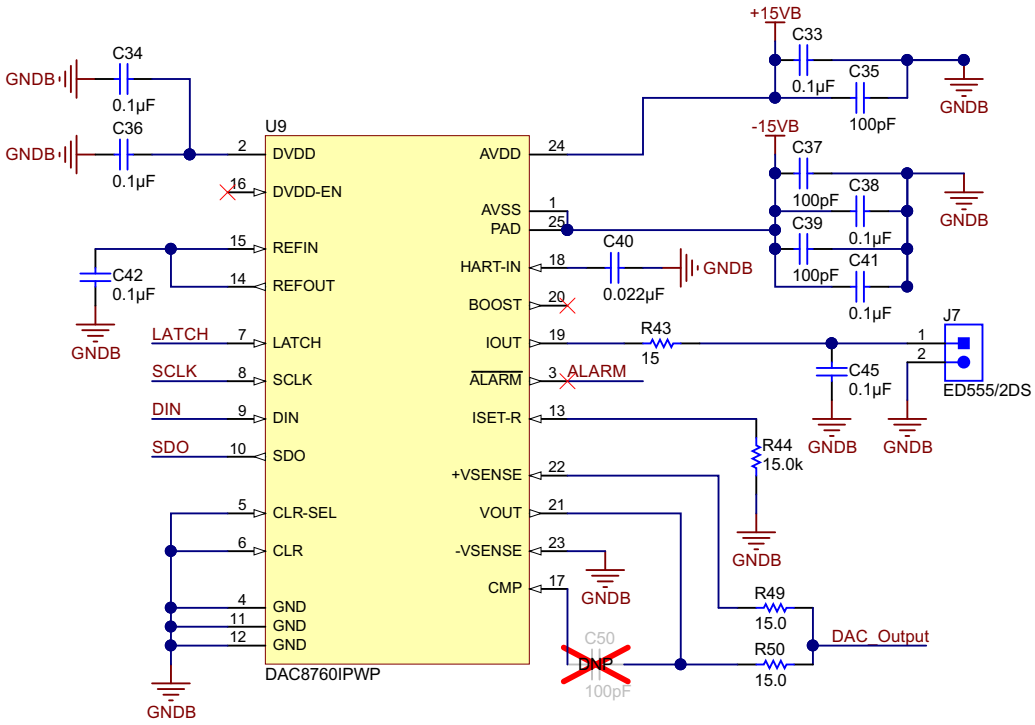


Figure 8. DAC8760 Schematic

- The most important element in a DAC circuit is the compensation capacitor connected between the VOUT and CMP pins. This cap enhances DAC output buffer stability, has a huge impact on the settling time of the DAC, and is chosen based on the capacitive load of the DAC. C50 is placed as a placeholder until an actual required cap is determined in the S&H block design. Figure 9 (from the DAC8760 datasheet) shows the relation between settling time for a 5-V step (with a bipolar supply of 36 V) against the load capacitor for 0-pF CMP cap value. C50 should be the C0G/NP0 cap to have a stable value over the temperature range. Here, a 0603 Ceramic 5%, 50 V is chosen.
- All bypass and current output filter caps are 0603 Ceramic X7R, 10%, 50-V capacitors.
- R44 accuracy determines the output current (test) accuracy. A 0603 0.1% resistor is selected.
- Pins R49 and R50 are selected as well as 0603 0.1% to achieve the best matching.

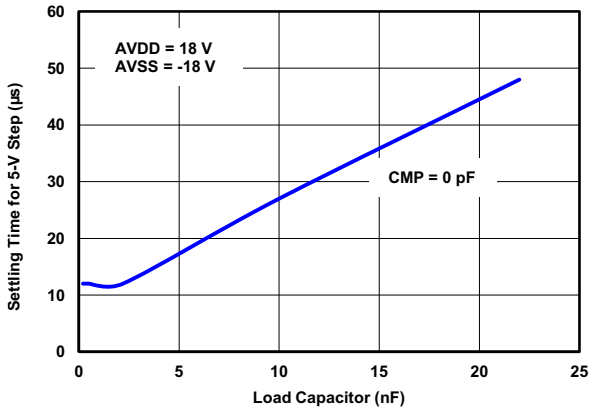


Figure 9. DAC V_{OUT} Settling Time versus Load (CMP = 0 pF)

6.2 S&H Circuit

The S&H circuit consists of the MUX representing the switch, a hold capacitor, and an active voltage follower driving the output.

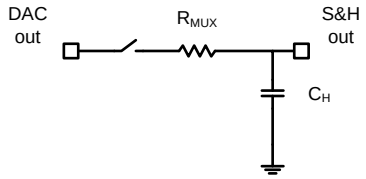


Figure 10. Simple S&H Circuit Model

Starting by the classical S&H circuit of first order RC filter shown in Figure 10 to leverage the full resolution of the 16-bit DAC, the settling time required is 11 RC.

The target specification allocates 750 µs per channel, and as discussed in Section 5.2, this time slot is divided into update, DAC settling, and sample (which includes hold cap settling). So, assume a certain time slot for the S&H settling out of the 750 µs. A conservative 110 µs for this settling brings a maximum value for the time constant (RC = 10 µs).

The maximum resistance of the MUX is 230 Ω. This value would give a maximum hold capacitor value possible—around 40 nF—if a 16-bit accuracy is to be achieved within 110 µs.

One aspect that makes the actual time for settling longer (in case of an output step) is the charge sharing and redistribution. As the MUX switch is shorting the DAC output (with the associated low MUX input cap) and the hold capacitor, the charge on the MUX input cap is redistributed partially to the much higher hold cap. This causes the DAC output to briefly change, and the DAC output will drive both back to the desired output through the normal settling. In the case of a negligible MUX input cap, this might end up in another DAC settling time on top of the first order settling. Using the DAC settling curves and assuming a 0-pF compensation capacitor brings another 200 µs worst case in case of a 20-V step. So, a minimum of 300 µs should be allocated to the sampling time from the channel slot of 750 µs.

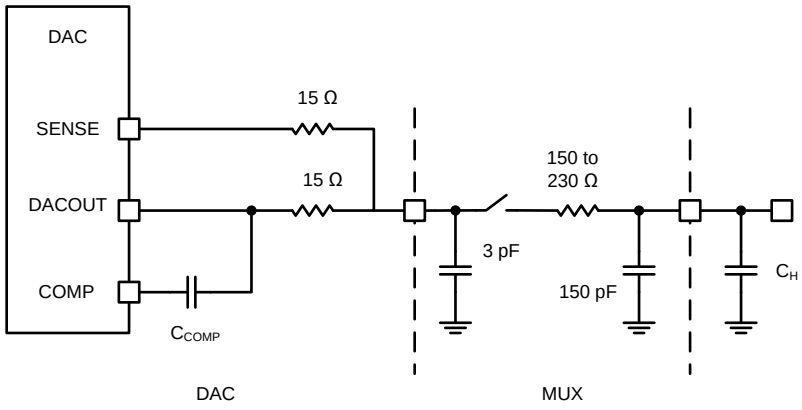


Figure 11. S&H Circuit Model

A unity gain buffer and voltage follower is needed to isolate the load from the hold capacitor and provide the driving strength for resistive loads.

Now, check that the voltage drift given in this value would result in an acceptable error. The hold cap has three paths for leakage:

1. Leakage into the amplifier input
2. Leakage through the capacitor parasitic resistance
3. Leakage through the MUX floating output

Take the worst case of maximum leakage current of each path, consider it constant through the hold time, and assume the maximum voltage at the capacitor (±10 V).

At worst, the OPA188 input leakage is ±8 nA over the whole temperature range up to 125°C. Assume a limit of ±2 nA if a temperature range up to 85°C is considered although around 1 nA in nominal case is to be expected.

Table 4. OPA188 Input Bias Current

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
I_B	Input bias current			±160	±1400	pA
		T_A = –40°C to 125°C			±8	nA
I_{OS}	Input offset current			±320	±2800	pA
		T_A = –40°C to 125°C			±4	nA

For MUX36S08, output leakage in an off-state is our value of interest, which is around ±0.5 nA over the temperature range of interest.

Table 5. MUX36S08 Output Leakage Current

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{S(OFF)}$	Input leakage current	Switch state is off, V_S = ±10 V, V_D = ±10 V(1)		–0.04	0.001	0.04	nA
			T_A = –40°C to 85°C	–0.15		0.15	
			T_A = –40°C to 125°C	–1.90		1.90	
I_D	Output leakage current	Switch state is off, S = ±10 V, D = ±10 V(1)		–0.10	0.005	0.10	nA
			T_A = –40°C to 85°C	–0.50		0.50	
			T_A = –40°C to 125°C	–2.00		2.00	
		Switch state is on, D = ±10 V, S = floating		–0.10	0.008	0.10	nA
			T_A = –40°C to 85°C	–0.50		0.50	
			T_A = –40°C to 125°C	–3.30		3.30	

(1) When V_S is positive, V_D is negative, and vice versa.

For a small value capacitor (< 47 nF), assume a 10-GΩ parallel resistance for the hold cap, leading to about 1 nA of leakage.

The aforementioned worst case leakage values do not necessarily have the same sign; they might partially cancel each other. However, for the purpose of estimating worst case drift, assume they are in the same direction, which gives a worst case leakage around 3.5 nA.

Voltage drift due to this leakage can be calculated with Equation 4, assuming constant leakage over the hold time of about 5.5 ms (6 ms – 0.5 ms):

$$\Delta V_H = \frac{I_{LEAKAGE} \times \Delta t_{HOLD}}{C_H} \quad (4)$$

If a 40-nF hold capacitor is to be used, this would bring a drift of about 480 µV. This value is exaggerated, which will be clear from the measurements. A smaller 22-nF capacitor is used as the settling time is believed to be a more limiting factor to achieve the speed and accuracy. This would lead to a ~1-mV maximum drift. The measurement, however, shows a much lower drift and shows that leakage from the MUX and op amp are cancelling each other partially in higher temperatures. To avoid this, set 0.5 mV as the maximum leakage.

The drift error is constant for all channels and is independent from the output voltage as measurement proves, so this error can be considered as a constant offset error for the system.

Charge injection from the MUX switch is 0.5 pC, which is negligible regarding charge variation due to leakage. Charge variation due to the leakage current is around 20 pC.

As the hold cap is determined, and by revisiting back the settling time against the load cap in Figure 9, assuming CMP = 0F compensation, the diagram indicates a 10-µs settling time corresponding to a 5-V step on a 3-pF load (MUX is off) with a 36-V supply span. Extrapolating under the assumption that settling is predominantly linear, with a 20-V step (±10 V), and with lower supply of 30 V (±15 V), the estimated DAC settling time then is about 5X this value. This gives an estimated DAC settling time value of 50 µs at 25°C; this number should be taken with great cautious as there is no characterization data related to this conditions, and some margin should be given for the full temperature range. The RC filter composed of the DAC output series resistor and MUX input cap has a time constant of about 50 ps, so 11RC time for first order settling is negligible compared to the intrinsic DAC settling time.

6.3 Buffer Circuit

An active voltage follower (unity gain amplifier) shown in Figure 12 is used to buffer the hold capacitor and provide load driving capability. Input and feedback resistance (R_{in} and R_f) help match the input impedance to the op amp and reduce the input bias current (this is minor though as the OPA188 already has a low bias current). The feedback resistor helps also in case of very fast input transients to prevent the input protection circuits from getting turning on. For a high capacitive load, the feedback capacitor (C_f) might be beneficial in maintaining the stability of the unity gain buffer. The actual circuit populated on the board does not have C_f, It is given as a placeholder for a generic circuit that can work for a wide variety of op amps.

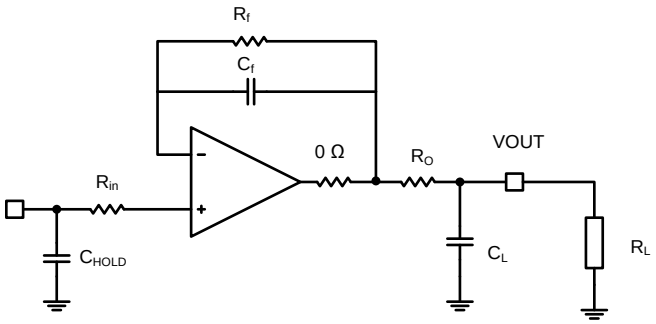


Figure 12. Buffer Circuit

Isolation resistance R_O mainly isolates high capacitive loads (represented by load capacitor C_L) from the op amp. High capacitive loads can affect the stability of low gain amplifiers. However, the output resistor is increasing the output impedance. The output impedance of the voltage output would result in a gain error due to the potential divider effect. This gain error can be corrected using gain calibration if the output impedance is known. Table 6 shows simulation results to determine the maximum capacitive load for different isolation resistance values; the criteria is to maintain gain margin better than 4 to 5 dB. Note that the 100-nF limit is dictated by the settling time within 750 µs, so a higher capacitive load is possible for longer scan cycles. In the testing section, a 100-Ω isolation, 100-nF, unloaded output is used.

NOTE: The actual measurement of 0 Ω gives 5 nF as the maximum stable load.

Table 6. Simulated Isolation Resistor R_O versus Capacitive Load C_L

ISOLATION RESISTOR (Ω)	MAXIMUM CAPACITIVE LOAD (nF)
0	5
10	20
20	40
100	100

Another role of the RC filter would be to limit the noise bandwidth; however, this is not a major issue as the output noise of the OPA188 is quite low. An RC filter with R = 100 Ω and C = 0.1 µF would have a 3-dB bandwidth of ~16 kHz. The integrated noise over this bandwidth is less than 1.5 μV_{PP}, which is negligible compared to 1 LSB value in any range. The output series resistor RO provides some protection against short circuit. The OPA188 already has a short circuit current limiter, but it would be beneficial if an op amp without protection is used.

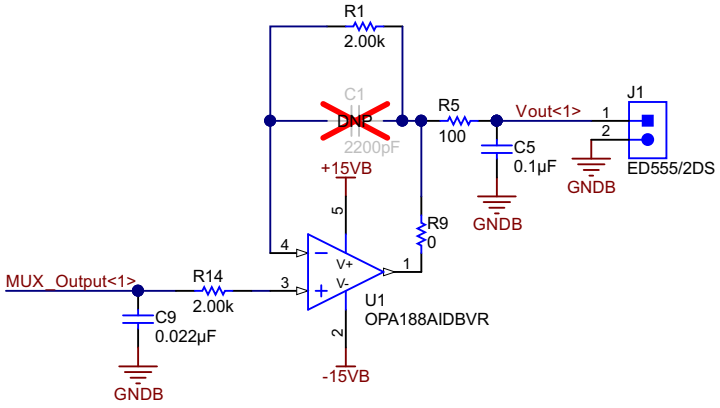


Figure 13. Buffer Circuit Schematic

6.4 Signal Path Model

The design choices made so far can be combined to make a signal path model (shown in Figure 14) that can be used to simulate and verify circuit performance.

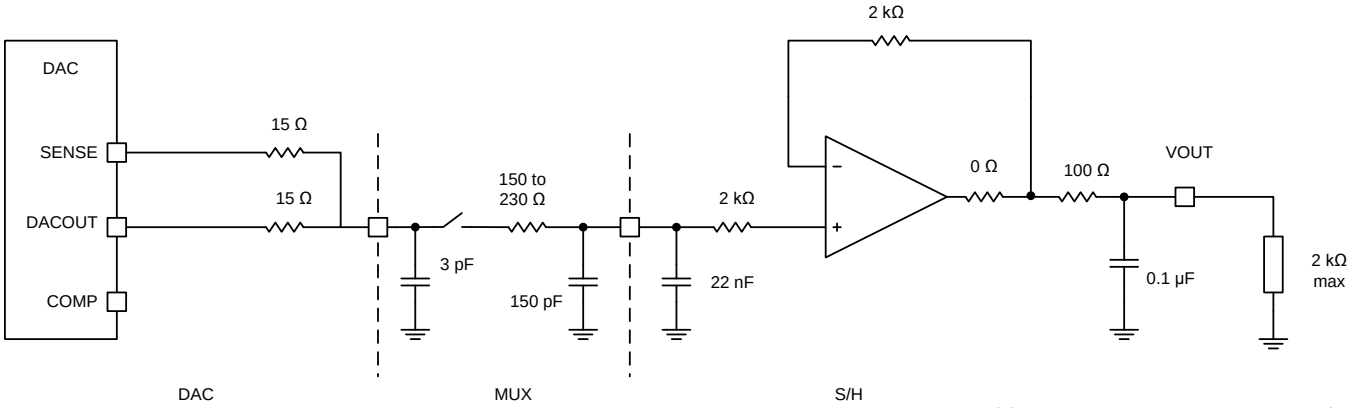


Figure 14. Signal Path Model (100-Ω Isolation Resistor)

Simulation results for the signal path model are shown in Figure 15 and Figure 16.

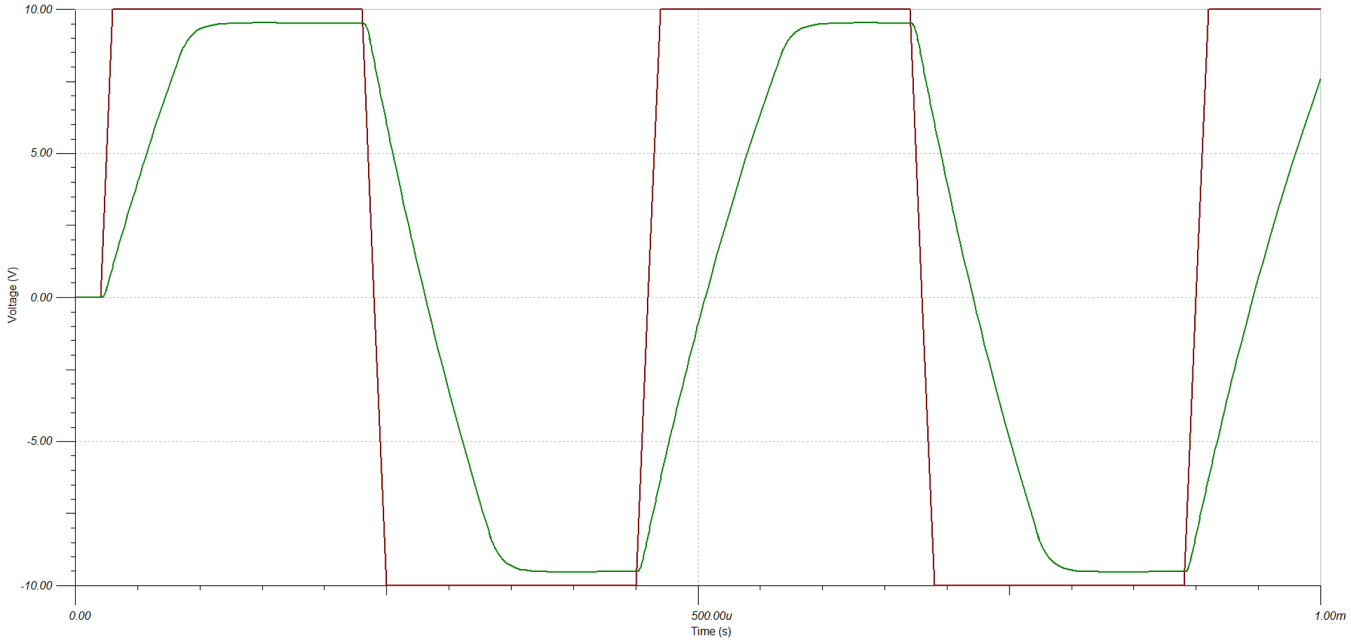


Figure 15. Transient Simulation Showing DAC Output and Buffer Output

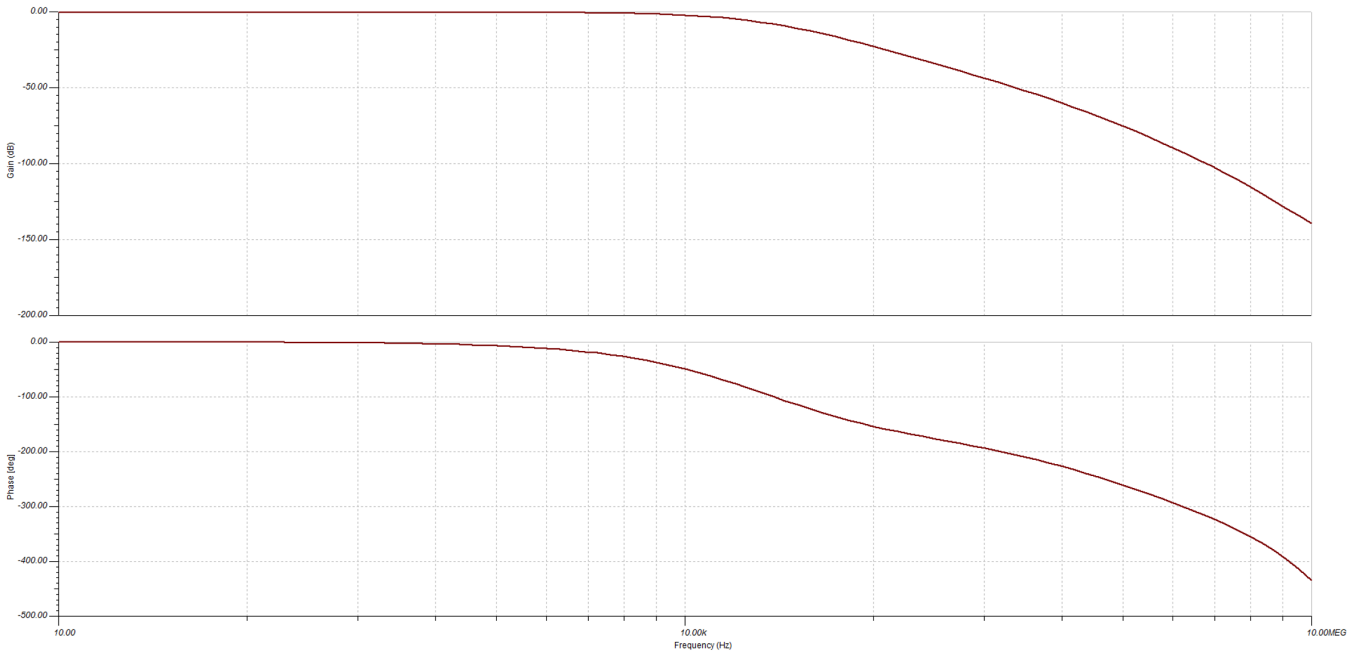


Figure 16. AC Transfer Function of S&H and Buffer Circuit

6.5 4- to 20-mA Conditioner Circuit

The XTR111 is a precision voltage to current converter for the standard 4- to 20-mA current loops. The device is designed to drive an external P-MOSFET to ensure high output resistance and broad compliance voltage range with only 2 V of headroom below the supply voltage, still keeping MOSFET heat dissipation away from the converter chip that helps to achieve target high precision.

The device shown in Figure 17 consists mainly of a high impedance input buffer and a current mirror with an external reference resistor that drives the external P-MOSFET gate through an output buffer.

An auxiliary adjustable regulator is available for additional circuitry, along with an output disable pin (enabled by default) and an output failure status pin. The device can work with a supply in the range of 8 to 40 V. An input voltage up to 12 V is possible.

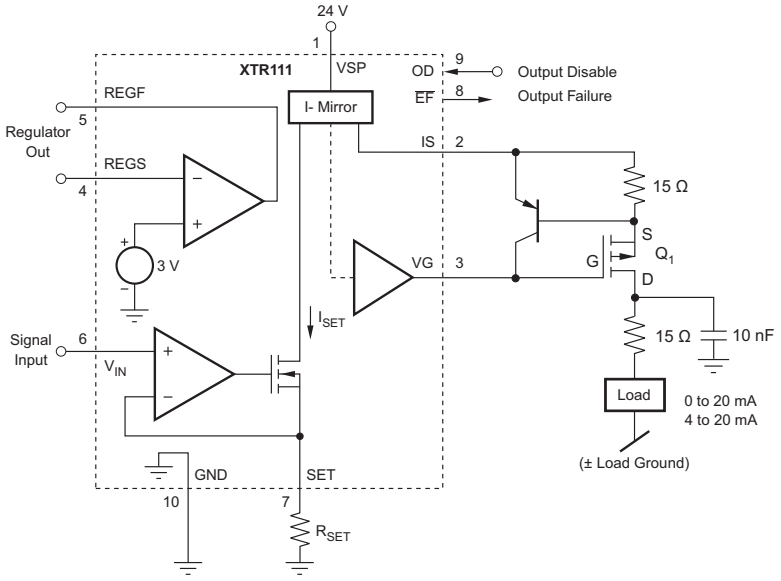


Figure 17. XT111 Block Diagram

The conversion gain of the XTR111 is set by the R_{SET} value.

$$I_{OUT} = 10 \frac{V_{VIN}}{R_{SET}} \quad (5)$$

The input signal is supposed to be driven from the DAC8760 through the MUX36S08 output directly. There are two options to generate 4 to 24 mA here:

1. V_{VIN} range up to 5 V; in this case a gain of ~5 mA/V is needed, resulting in an R_{SET} of 2 kΩ.
2. V_{VIN} range up to 10 V; in this case a gain of ~2.5 mA/V is needed, resulting in an R_{SET} of 4 kΩ.

Selecting the first option means the inputs should be limited to

- For 4 mA, V_{IN} = 0.8 V
- For 20 mA, V_{IN} = 4 V
- For 24 mA (overdrive), V_{IN} = 4.8 V

To achieve maximum resolution, the DAC range should be set to 0 to 5 V. Other ranges are still possible to use with reduced resolution. For example, using a range of –10 to 10 V means only a quarter of the range is used, which is equivalent to losing 2 bits of resolution.

Note that the XTR111 does not provide an internal current limit if the external FET is forced to low impedance. An external current limiter is necessary to protect the chip from excessive current in case of short circuit or low load conditions. One possible circuit (gate controlled current limiter), recommended by the datasheet, is shown in Figure 18. When an excessive current is flowing through Q1, the voltage on feedback resistor R6 increases and turns on Q2, hence limiting the MOSFET gate-source voltage and current. The 15-Ω series resistor (R6) will limit the current to 33 mA or 37 mA according to temperature. See the XTR111 datasheet (SBOS375) for different current limiting circuits.

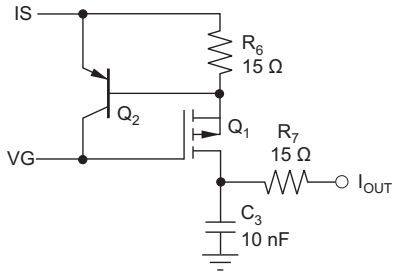


Figure 18. External Current Limit Circuit

The addition of Q2 and R6 still require time to discharge the gate of the external MOSFET. C3 and R7 are added for this reason as well as to limit the steepness of external distortion pulses.

The voltage-to-current converter circuit for one channel is shown in Figure 19.

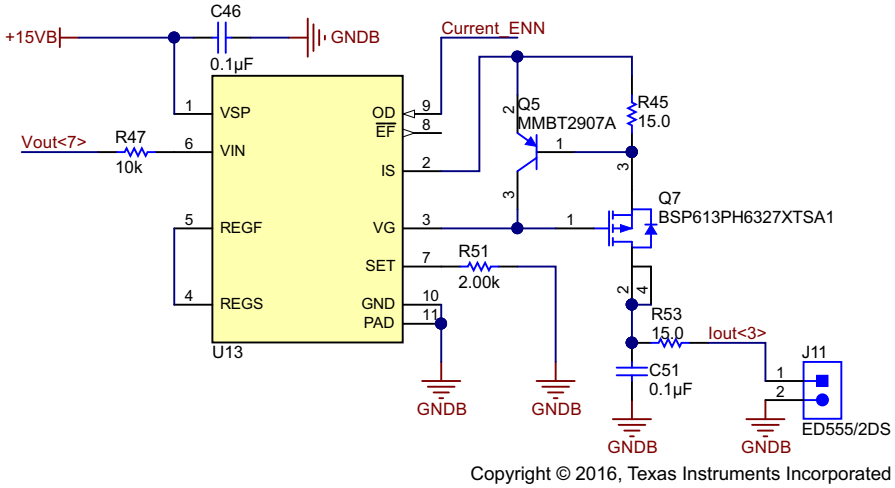


Figure 19. XTR111 Schematic

- VSP is connected to the 15-V supply, with GND and thermal PAD connected to GND.
- REGF and REGS are shorted; an internal regulator is not used here. Failure output is left open.
- BSP170P external P-MOSFET is used as recommended by the XTR111 datasheet. VIS should not be pulled below 6.5 V below the supply VSP. The internal clamp is protecting this node; this internal clamp circuit has a maximum current limit of 50 mA. An external current limiting circuit will complement this circuit and provide both voltage and current protection for the IS node.
- An MMBT2907A 60V PNP transistor is used for the current protection circuit. This circuit will limit the output current below 40 mA, which is lower than the maximum current capability of the XTR111 (50 mA).

  The collector leakage current of Q5 should be carefully examined as it would result in output current error. This is a systematic error though that can be compensated by an initial calibration. However, R_{SET} should be dominant if this current error is below 1 µA.
- R51 (2 kΩ) is used as R_{SET} to set the gain of the circuit to 5 mA/V as discussed. Note that V_{SET} should not exceed 14 V as this pin is not protected above this level.
- R51 accuracy is very important for output current accuracy. A 0.1% error in the resistance is directly transferred as an output error of 0.1%. The design objective is to have this error as the major contributor to the current output error. Remember that error is referred to the output value, meaning a lower percentage when referred to FS.
- Current_ENN (enable_not or disable) is routed to the controller through module connector. High on this node disables the current output. Note that all current converters disable pins are connected together for this design. Individual disable pins would allow more power saving in case some outputs are not used.
- V_{IN} is high impedance input (nominal 2.5 GΩ/30 pF). The R47 (10 kΩ) is placed in series to protect the clamping circuit in case of over- or undervoltage or input valid before the device is powered. A value equal to R_{SET} = 2 kΩ or higher is recommended to cancel the bias current. R47 is 0603 5% resistor.
- C51 = 0.51 µF is very important for reducing the current ripples during output settling, which lasts around 100 µs. In combination with the output load resistor, the ripples are greatly reduced. If more suppression of ripples is needed, an additional filtering can be employed as discussed in detail in the XTR111 datasheet.
- Filter cap C51 and bypass cap C46 are 0603 Ceramic X7R, 10%, 50-V capacitors.

The TI Design TIPD155 (TIDU434) shows how to use the XTR300 for a combined voltage and current output in case a bipolar or combined output is required for all outputs.

6.6 Accuracy and Error Estimation

All sources of error can be added to estimate the overall unadjusted accuracy of the system. A worst case range of 0 to 5 V is considered for the S&H leakage as the leakage is constant (see Section 6.2), which means it has higher effect on lower range. The maximum values in the datasheet are used in this estimation as shown in Figure 20. Total error for the voltage output is below 0.02%, and less than 0.03% for the case of current output.

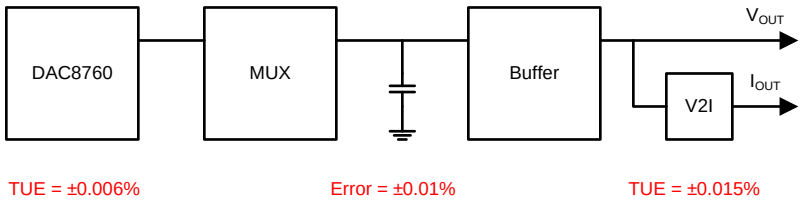


Figure 20. System Error Estimation

The output impedance of the voltage buffer will add error to that, which can be corrected by gain calibration if output load is known. A 10-Ω output impedance would result in 0.5% error for a 2-kΩ load. Protection circuits (TVS and clamp diodes) attached to the current output would also add to the total error of the system. A 10-µA maximum leakage protection diode at the current output stage would result in 0.05% FS error for a 20-mA maximum current. The leakage from protection circuits has more effect on lower values of output current. If a higher relative accuracy is required, take care when selecting protection devices.

6.7 Controller Interface

The signals routed to the controller are

- SPI signals: LATCH, SCLK, DIN, SDO, plus a local GND
- MUX channel select signals: Channel_Sel[2:1]
- MUX enable pin: MUX_EN
- Voltage-to-current converter disable pin: Current_ENN
- DAC ALARM signal

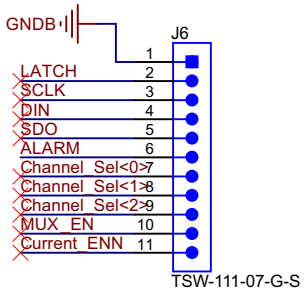


Figure 21. Controller Interface Schematic

In a real application, all failure output from the converter can be tied together or individually while an individual current output enable should be separated. So for four current outputs that are individually controllable, at least four other control pins are needed, which means 15 control lines are required. If all output failure pins are separate, the controller ends up with 18 control lines.

7 Controller Firmware

The MSP430FR4133 EVM is chosen to control the S&H output module. In this section, a simple and straightforward description of initializing and preparing the MSP430 to drive the DAC and the MUX is given as an example. For more details of MSP430 programming, see the following documents:

- MSP430FR4xx User's Guide [8]
- MSP430FR413x Datasheet [7]
- MSP430FR4133 LaunchPad EVM
- MSP430 DriverLib

7.1 Connectivity

Table 7 shows the connectivity between the MSP430 and the S&H module interface pins.

Table 7. MSP430 to TIDA-00760 Module Connection

TIDA-00760	MSP430
LATCH	P5.0
SCLK	P5.1 (SCL)
DIN	P5.2 (MOSI)
SDO	P5.3 (MISO)
S0 (Channel_SEL<0>)	P1.3
S1 (Channel_SEL<1>)	P1.4
S2 (Channel_SEL<2)	P1.5
MUX_EN	P1.0
Current_ENN	3.3-V supply

Port 5 can be configured to be connected to the internal USCI_B, which is used as an SPI master. MUX control is done through GPIO port 1.

7.2 Configuration

SPI communication runs with a 1-Mbps rate. The USCI_B unit is used as the SPI master. SMCLK is used as an input clock to the USCI_B unit running at 4 MHz. The scanning of channels is done through a timer interrupt. Timer_A running in UP_MODE is used to trigger that interrupt. An internal time reference of 1 µs is used for clarity of coding, meaning internal clock of 1 MHz clock as well. The same SMCLK is used as input to the timer as well.

An internal reference clock running at 32 MHz is used as a reference to generate SMCLK. FLL is used to ensure accurate frequency upon settling.

7.3 Initialization

The following libraries are to be used. The MSP430 includes definitions related to the controller while the DAC8760 is a custom header file containing definitions (named constants) for the DAC8760 modes and configurations. Driverlib is a high level library easing the programming of the MSP430 and allows for portable code among the MSP430 family.

```
#include <stdint.h>
#include <msp430.h>
#include "DAC8760.h"
#include "driverlib.h"

int main(void)
{
    WDT_A_hold(WDT_A_BASE);
    PMM_unlockLPM5();
```

The main function should start by holding the watchdog timer (WDT) to avoid restart during run and unlocking the output ports to be able to change port modes.

```
initPorts();
   initClocks(4000000);// Config clocks. MCLK=SMCLK=FLL=4MHz
   initTimers();
   DAC8760_Setup((DAC8760_RANGE_M10V_P10V + DAC8760_OUTEN),0,0,0);          // Config
   while (1){ __no_operation(); }
```

The ports, clocks, and timers are initialized before configuring the DAC for range setting, and then get into the no_operation loop. More details on the initializations are given in the following sections.

7.3.1 Ports

Port 5 is used as a peripheral output port while Port 1 is used as an output port as well as P5.0. All other pins can be set to low with port direction to output to avoid any floating pins. GPIO_set functions are defined in the driverLib.

```
#define GPIO_ALL    GPIO_PIN0|GPIO_PIN1|GPIO_PIN2|GPIO_PIN3| \
                    GPIO_PIN4|GPIO_PIN5|GPIO_PIN6|GPIO_PIN7

    GPIO_setOutputLowOnPin(GPIO_PORT_P1, GPIO_ALL);
    GPIO_setAsOutputPin(GPIO_PORT_P1, GPIO_ALL);

    GPIO_setOutputLowOnPin(GPIO_PORT_P5, GPIO_PIN0);
    GPIO_setAsOutputPin(GPIO_PORT_P5, GPIO_PIN0);

    GPIO_setAsPeripheralModuleFunctionOutputPin(
                    GPIO_PORT_P5,
                    GPIO_PIN1 + GPIO_PIN2 + GPIO_PIN3,
                    GPIO_PRIMARY_MODULE_FUNCTION
                    );
    GPIO_setOutputLowOnPin(GPIO_PORT_P4, GPIO_ALL);
    GPIO_setAsOutputPin(GPIO_PORT_P4, GPIO_ALL);
    ...
```

7.3.2 Clock

The clock initialization function is given the SMCLK frequency in Hz as a parameter, and sets clock reference as configuring the SMCLK frequency. CS_init functions are defined in driverLib.

```
void initClocks(uint32_t mclkFreq)
{
   CS_initClockSignal(
       CS_FLLREF,
       CS_REFOCLK_SELECT,
       CS_CLOCK_DIVIDER_1);

    CS_initClockSignal(
       CS_ACLK,
       CS_REFOCLK_SELECT,
       CS_CLOCK_DIVIDER_1);

    CS_initFLLSettle(
        mclkFreq/1000,
        mclkFreq/32768);
}
```

7.4 DAC and SPI Master Setup

The DAC8760_Setup function initializes the SPI USCI_B and write configuration registers if required.

```
void DAC8760_Setup (uint16_t controlReg, uint16_t configurationReg, uint16_t
gainCalReg, uint16_t zeroCalReg)
{
    DAC8760_SPISetupMaster();
    DAC8760_Reset();
    DAC8760_Nop();
    DAC8760_WriteReg (controlReg, DAC8760_WRITE_CONTROL_REGISTER);
    DAC8760_WriteReg (configurationReg, DAC8760_WRITE_CONFIGURATION_REGISTER);
    DAC8760_WriteReg (gainCalReg, DAC8760_WRITE_GAIN_CALIBRATION_REGISTER);
    DAC8760_WriteReg (zeroCalReg, DAC8760_WRITE_ZERO_CALIBRATION_REGISTER);
}

void DAC8760_SPISetupMaster(void)
{
    EUSCI_B_SPI_initMasterParam param = {0};
    param.selectClockSource= EUSCI_B_SPI_CLOCKSOURCE_SMCLK;
    param.clockSourceFrequency = 4000;
    param.desiredSpiClock = 1000;
    param.msbFirst= EUSCI_B_SPI_MSB_FIRST;
    param.clockPhase= EUSCI_B_SPI_PHASE_DATA_CAPTURED_ONFIRST_CHANGED_ON_NEXT;
    param.clockPolarity = EUSCI_B_SPI_CLOCKPOLARITY_INACTIVITY_LOW;
    param.spiMode = EUSCI_B_SPI_3PIN;

    EUSCI_B_SPI_initMaster(EUSCI_B0_BASE, &param);
    EUSCI_B_SPI_enable(EUSCI_B0_BASE);

}

void DAC8760_Reset (void)
{
    uint8_t outData[3];
    outData[0] = DAC8760_WRITE_RESET_REGISTER;
    outData[2] = DAC8760_RESET;

    DAC8760_SPIWrite (outData, RcvData);
}

void DAC8760_Nop (void)
{
    uint8_t outData[3];
    outData[0] = DAC8760_WRITE_NOP_REGISTER;
    DAC8760_SPIWrite (outData, RcvData);

}
```

7.5 DAC SPI Write

The DAC8760_WriteReg is an important function responsible for writing an SPI word (24 bits) into a specified DAC8760 register.

```
#define DAC8760_LATCH_PORTOUT    P5OUT

void DAC8760_WriteReg (uint16_t writeValues, uint8_t address)
{
    uint8_t outData[3];

    outData[0] = address;

    // Switch Endianess
    outData[1] = writeValues >> 8;
    outData[2] = writeValues & 0xff;

    DAC8760_LATCH_PORTOUT &= ~DAC8760_LATCH_PIN;

    EUSCI_B_SPI_transmitData ( EUSCI_B0_BASE, outData[0] );
    EUSCI_B_SPI_transmitData ( EUSCI_B0_BASE, outData[1] );
    EUSCI_B_SPI_transmitData ( EUSCI_B0_BASE, outData[2] );
    while (EUSCI_B_SPI_isBusy(EUSCI_B0_BASE))
      __no_operation();

    // Load DAC registers input.
    // A rising edge on the Latch pin loads the input shift register data into the
DAC
    DAC8760_LATCH_PORTOUT |= DAC8760_LATCH_PIN;
}
```

7.6 Timers

Timer_A is the heartbeat of the scan cycle. The timer is initialized using the intiTimers() function with SMCLK as a reference clock and divided by 4 to get a 1-MHz internal reference. timerPeriod = 750 sets the single channel cycle to 750 µs. This can be changed to test other channel time slots. timerPeriod is also used to test the voltage droop by extending this to a much higher timing to exaggerate the voltage drift value.

```
void initTimers(void)
{
    Timer_A_initUpModeParam initUpParam={0};
      initUpParam.clockSource = TIMER_A_CLOCKSOURCE_SMCLK;
      initUpParam.clockSourceDivider =  TIMER_A_CLOCKSOURCE_DIVIDER_4;  // 4M input
      initUpParam.timerPeriod = 750; // this is the signle channel time slot
      initUpParam.timerInterruptEnable_TAIE = TIMER_A_TAIE_INTERRUPT_DISABLE;
      initUpParam.captureCompareInterruptEnable_CCR0_CCIE =
                                TIMER_A_CCIE_CCR0_INTERRUPT_ENABLE;
      initUpParam.timerClear = TIMER_A_DO_CLEAR;
      initUpParam.startTimer = false;

    Timer_A_initUpMode( TIMER_A0_BASE, &initUpParam );

    Timer_A_initCompareModeParam initCompParam={0};
     initCompParam.compareRegister = TIMER_A_CAPTURECOMPARE_REGISTER_1;
     initCompParam.compareInterruptEnable =
                 TIMER_A_CAPTURECOMPARE_INTERRUPT_DISABLE;
     initCompParam.compareOutputMode = TIMER_A_OUTPUTMODE_OUTBITVALUE_LOW;
     initCompParam.compareValue = 60;

    Timer_A_clearTimerInterrupt( TIMER_A0_BASE );     // Clear TA0IFG
    Timer_A_clearCaptureCompareInterrupt(
       TIMER_A0_BASE,
      TIMER_A_CAPTURECOMPARE_REGISTER_0+TIMER_A_CAPTURECOMPARE_REGISTER_1 );

    Timer_A_startCounter(
        TIMER_A0_BASE,
        TIMER_A_UP_MODE
    );
}
```

7.7 Scan Cycle Implementation

The scan cycle is coded in the timer interrupt handler. Whenever an interrupt is triggered (due to the time reaching the 750 counter as set), the handler performs these actions:

1. De-assert the MUX EN pin.
2. Advance channel number (and cycle if maximum channel number is reached).
3. Write the desired output value to the DAC.
4. Set the MUX channel.
5. Wait long enough for the DAC to settle.
6. Enable the MUX.

Waiting is done using the delay_cycles function, which uses the cycle time of the reference clock (32 MHz). 1000 cycles equal about 30 µs, which is enough in this case.

The scan cycle code is where the user will put the required functionality of the module. There is definitely no standard implementation of such code. The following example shows the code to write different static values to different channels. test_dacval is written to test_ch, and other_dacval is written to the rest.

```
      #define max_ch 8                        // maximum channels to sweep upon
      #define max_ch_limit max_ch+1
      #define test_ch 2                       // set to the desired channel
      static int8_t channel=0;
      static int16_t dacval=0;
      #define      test_dacval 0x0000         //set to the desired dacval
      #define      other_dacval 0xFFFF        //set to the desired dacval

#pragma vector=TIMER0_A0_VECTOR
__interrupt void CCR0_ISR (void)
{

            P1OUT &=  ~GPIO_PIN0;
            channel++;
            if (channel>=max_ch_limit) channel=1;
            if (channel==test_ch) dacval=test_dacval; else dacval=other_dacval;
            DAC8760_WriteReg (dacval, DAC8760_WRITE_DATA_REGISTER);
            MUX_SET(channel);
            __delay_cycles(1000);
            P1OUT |=  GPIO_PIN0;
}
```

As only the TIMER0_A0 interrupt is used, it is always a good practice to associate unused interrupts to no_operation as in the following code.

```
#pragma vector=USCI_A0_VECTOR
#pragma vector=USCI_B0_VECTOR
... // fill in all unused interrupts
__interrupt void UNUSED_HWI_ISR (void)
{
      __no_operation();
}
```

Figure 22 and Figure 23 show the control signals (MUX_EN, Latch, and SPI CLK) with timing indicated and different portions of the 750-µs channel time slot. This is only showing the DATA register write. If a range setting or calibration data is written, the clocking portion should be extended and the 260-µs S&H portion is reduced.

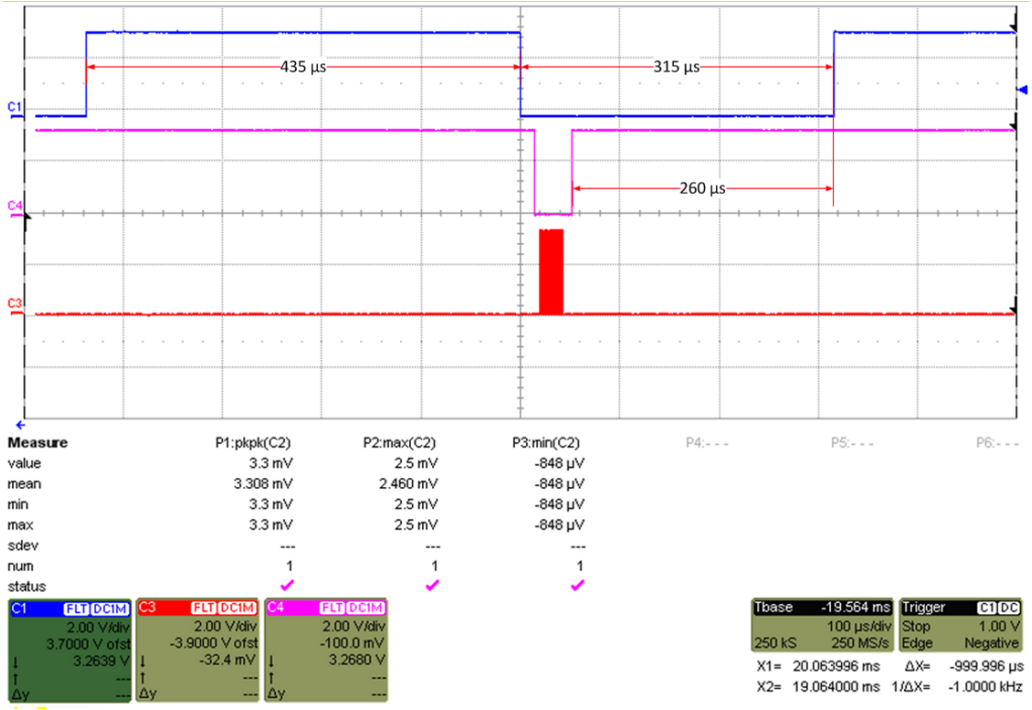


Figure 22. One Channel Update Cycle. C1: MUX_EN, C4: LATCH, C3: SPI_CLK

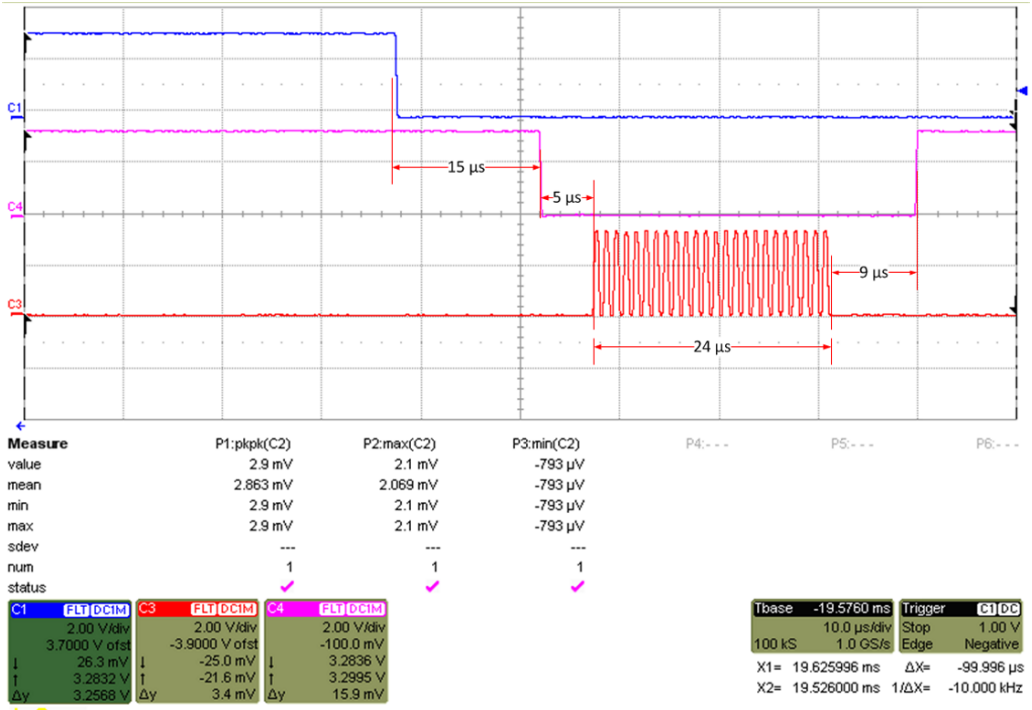


Figure 23. DAC Data Register Update (Zoomed in)

7.8 Current Output Channels

Current outputs are required to generate a 0- to 20-mA or 4- to 20-mA current. As the voltage-to-current conversion stage has a gain of 5 mA/V, to achieve the best resolution as discussed in Section 4.5, the output range should be set to 0 to 5 V, and output should be limited from 0.8 to 4 V for the 4- to 20-mA range.

```
DAC8760_Setup((DAC8760_RANGE_0V_5V + DAC8760_OUTEN),0,0,0);
```

The conversion function can be defined to convert current to DAC code. 0-V code is 0x0000, 0.8-V code is 0x28F5, 4-V code is 0xCCCC, and 5-V code is 0xFFFF.

Over-range can be implemented directly by writing values greater than 0xCCCC to the DAC data register.

8 Test Setup and Procedure

To measure the performance of the TIDA-00760 design, the module is powered by an Agilent E3631A power supply to provide the required ±15 V. Control is managed by the MSP430FR4133 LaunchPad programmed using Code Composer Studio™ v6.0. The dynamic measurements are done using a LeCroy Wavesurfer 454 digital scope, and high accuracy measurements are done using an HP34401A digital multimeter.

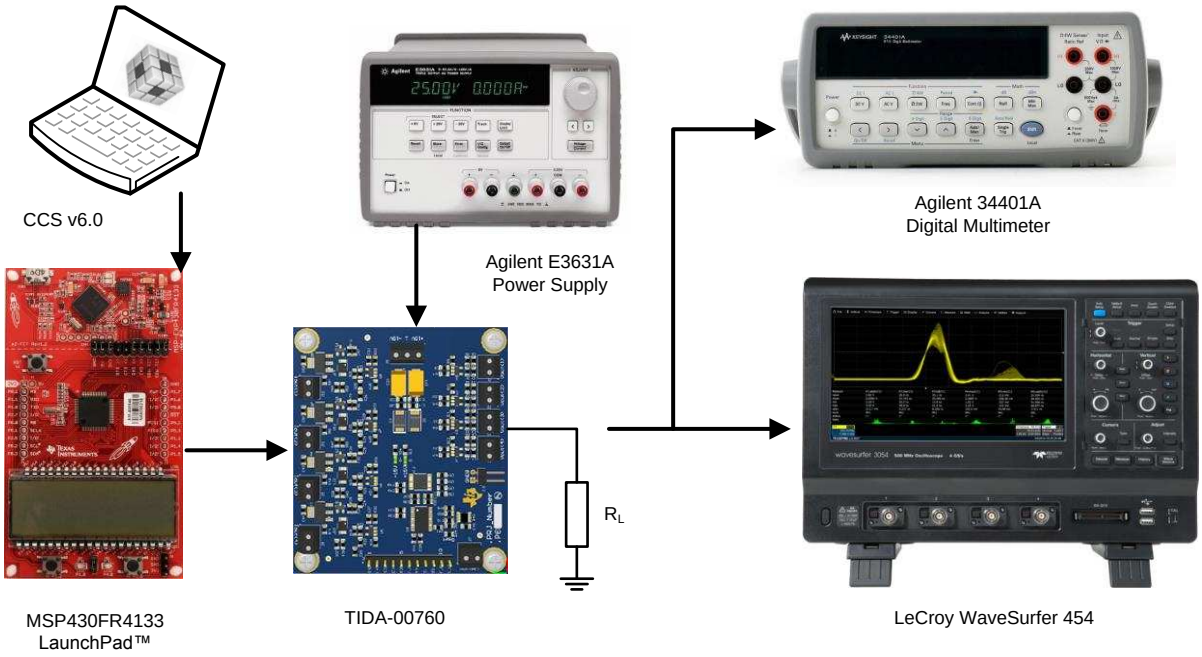


Figure 24. TIDA-00760 Test Setup

The tests carried out on the module include:

- Functional test: This test ensures the basic functionality of the design by testing different DAC ranges, dynamic DAC change, and MUX channel change.
- Resolution and monotonicity: This test ensures the DAC transfer function is monotonic over the output range. Min and max output values are recorded. In this test, the MUX channel is fixed and static, and the DAC output is ramped over a full or partial range.

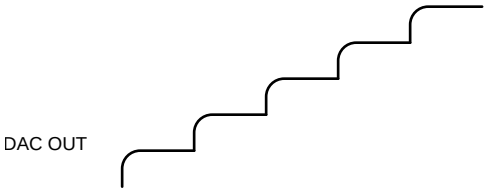


Figure 25. Module Monotonicity Test

- Accuracy for static output (same value for the outputs): This test scans MUX channels with the same output value for all channels and measures The accuracy of the channel. This test excludes the settling time for both the DAC output and sampling circuit. It only shows the drift of the hold capacitor and the kickback noise of the MUX switch.

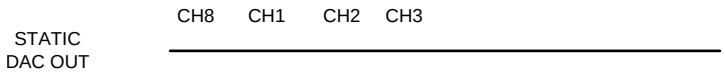


Figure 26. DAC Output in Case of Static Output Test

  - Channel-to-channel error: Output is checked for different channels, and error is compared to get a channel mismatch.
  - Different output values: Static DAC output is swept; channel error is recorded for different output values.
  - Different DAC ranges: For different DAC ranges, previous error measurements are conducted. Normally, the highest DAC range should result in the worst error and mismatch.
- Accuracy for static output (Different values for the outputs): In this measurement, all channels are static; however, the measured channel is different than all other channels. This shows the performance of DAC settling. Figure 27 shows two cases of selected CH1 values. The difference in both cases is the DAC full scale. The effect of the actual values of measured and other channels on the accuracy can be also measured by changing those values.

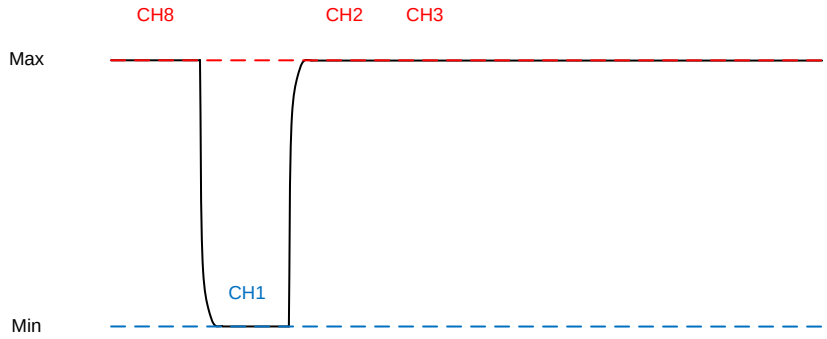


Figure 27. DAC Output in Output Test Where Channel 1 is Different Than Others

- Settling time for full-range swinging output: In this test, all channels have static output values except for the measured channel, which is toggled with a full swing of the DAC output range. This shows that the S&H circuit can handle the full-scale change of the channel voltage output. Settling time is also measured in this test.

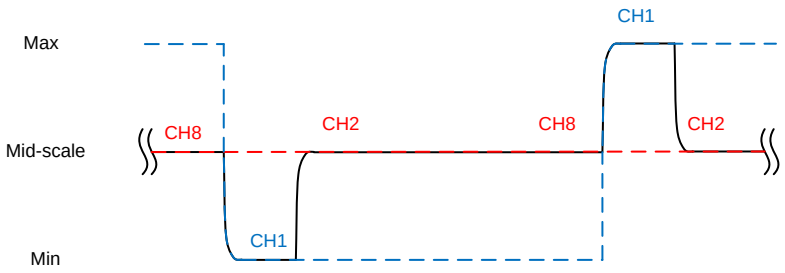


Figure 28. DAC Output in Full-Range Swinging Output Test

- Crosstalk from adjacent channels on static output: In this measurement, all channels are toggling between min and max of the DAC output, except for the measured channel, which is static. This shows the crosstalk effect including MUX isolation and residual charge as well as sample circuit and DAC output settling performance.

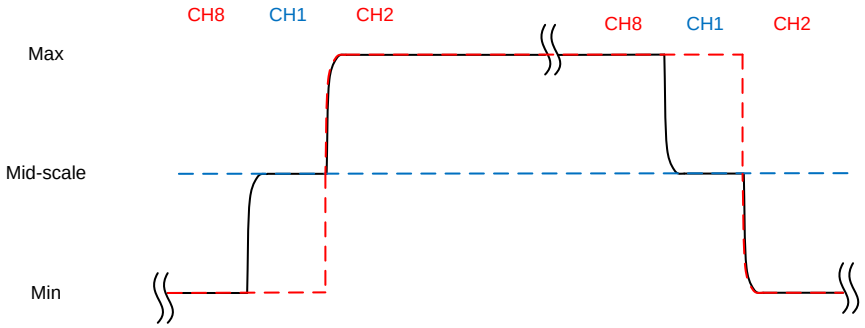


Figure 29. DAC Output in Crosstalk Output Test

9 Test Results

9.1 Monotonicity

The first basic test checks the monotonicity and linearity of the DAC with a static channel selected. This shows the static DAC and S&H buffer performance excluding the dynamic switching of the MUX.

The DAC input code is swept between 0x0000 and 0xFFFF to cover the full-scale range. Figure 30 shows the voltage output sweep while Figure 31 shows the sweep of the current output (with 500-Ω load) for the range 0x0000 to 0xCCCC equivalent to 0 to 20 mA.

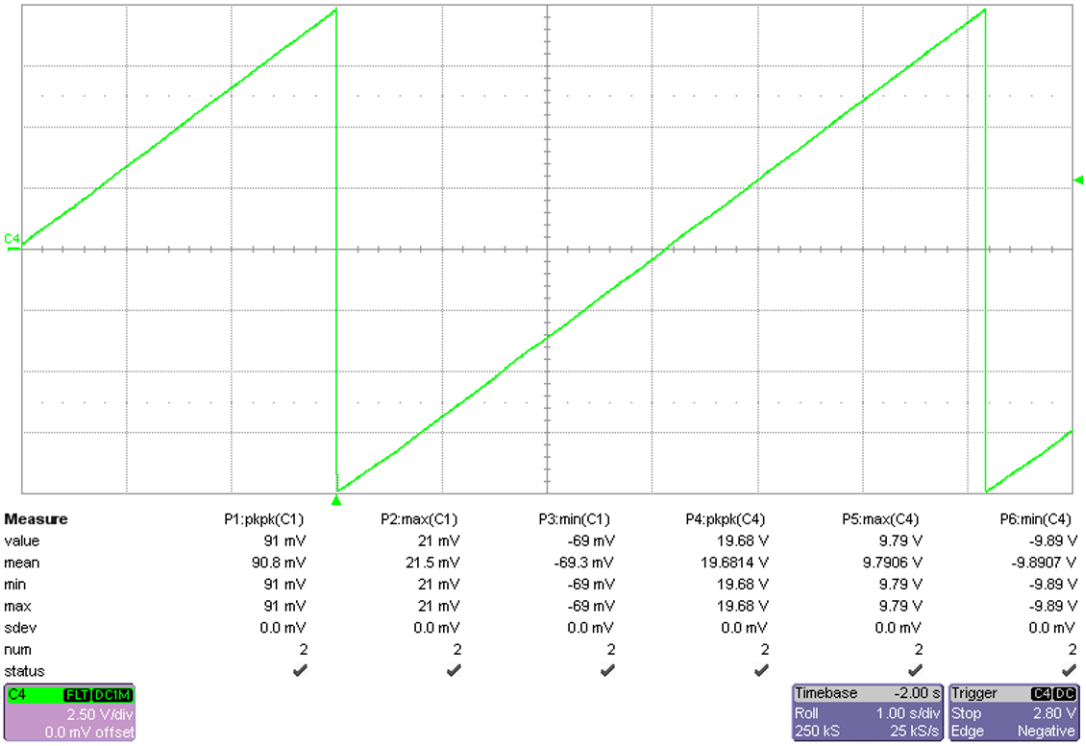


Figure 30. Monotonicity Check (Voltage Output)

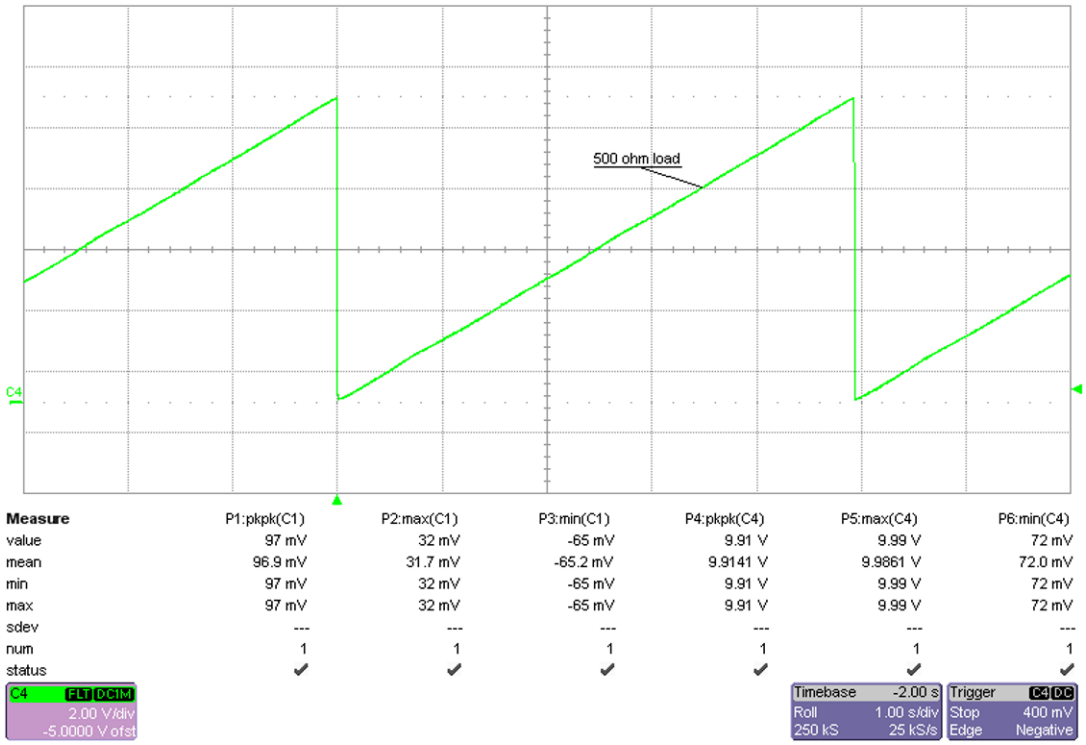


Figure 31. Monotonicity Check (Current Output)

At this range, the scope is not accurate enough to take the min and max measurements for sure. More accurate measurements of the min and max output values will follow in the following sections.

9.2 Static Output Accuracy

In this test, MUX channels are scanned with target speed of 6 ms/8 channels with two conditions.

1. The same DAC output value is set for all channels.
2. The measured channel is set to the max of FS range, and all other channels are set to the min of the full-scale range.

This test reveals the effect of S&H circuit leakage, excluding the dynamic performance of the S&H. The first condition shows only the drift of the hold capacitor voltage and excludes the settling time of the DAC, while the second condition adds the MUX switch kickback noise and the settling time of the DAC effect on the performance. There is hardly any difference in performance between these two cases. Figure 32 shows the output waveform for static output related to the FS min, FS max, and zero code input. Note that scope noise dominates the noise measurement here. The graphs illustrate the absence of spikes or noise from channel switching.

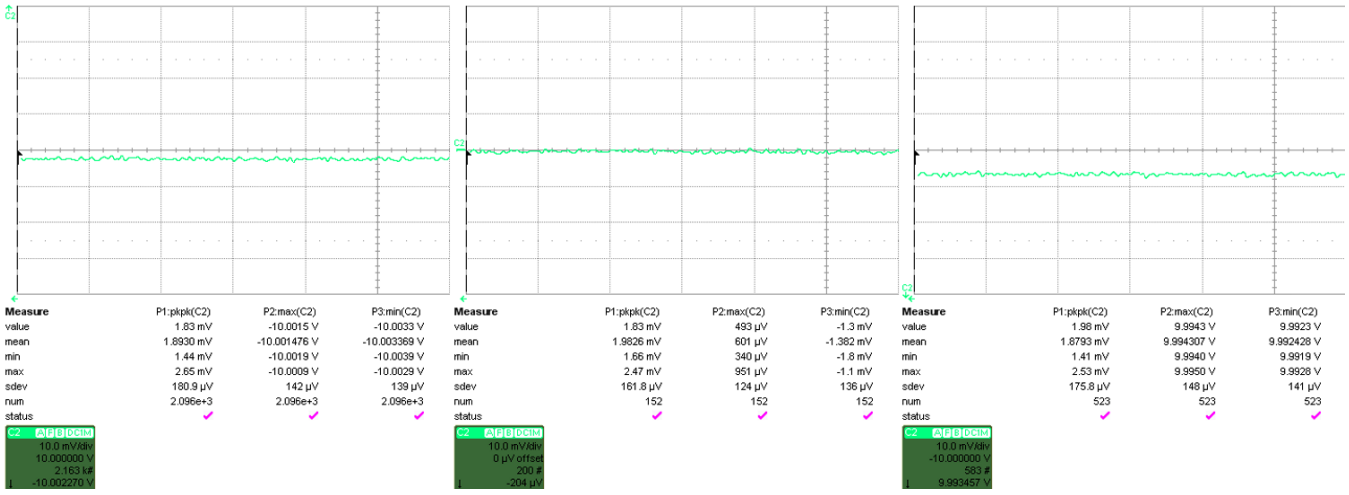


Figure 32. Static Output Voltage for Range Limits

The accurate measurement on the digital meter provided the following results:

Table 8. Values of –10- to 10-V Voltage Output at 25°C

DAC CODE	IDEAL VALUE (V)	MEASURED	ERROR (mV)	ERROR %
0x0000	–10	–10.003 V	–3	–0.015
0x6666	–2	–2.0013 V	–1.3	–0.0065
0x8000	0	–0.692 mV	–0.692	–0.0034
0xB000	3.7527	3.7503 V	–2.4	–0.012
0xFFFF	10	10.0013 V	4.3	0.0065

Table 9. Values of 0- to 25-mA Current Output at 25°C (500-Ω Resistor)

DAC CODE	IDEAL VALUE (mA)	IDEAL VALUE (V)	MEASURED (m)	ERROR (mV)	ERROR % (20-mA RANGE)
0x0000	0	0	–0.504	–0.504	0.00504
0x6666	10	5	5.0047	4.7	0.047
0xB000	17.18	8.5938	8.6042	10.4	0.104
0xCCCC	20	10	10.0127	12.7	0.127
0xFFFF	25	12.5	12.515	15	

The channel-to-channel error is also measured; a sample measurement between channel 2 and other channels shows negligible error. This is not a systematic error as all channels are identical; this is merely part-to-part variation and passive parts tolerance among different channel circuits.

Table 10. Channel-to-Channel Errors (Voltage)

CHANNELS	IDEAL VALUE	MEASURED ERROR (mV)	ERROR %
2 to 1	0	0.04	0.0002
2 to 3	0	0.16	0.0008
2 to 4	0	0.14	0.0007

Accuracy measurement over temperature is conducted using a temperature chamber for –35°C and 85°C.

Table 11. Values of –10- to 10-V Voltage Output at –35°C

DAC CODE	IDEAL VALUE (V)	MEASURED	ERROR (mV)	ERROR %
0x0000	–10	–10.001 V	–1.000	–0.00500
0x8000	0	–0.250 mV	–0.250	–0.00125
0xFFFF	10	10.0008 V	0.800	0.00400

Table 12. Values of –10- to 10-V Voltage Output at 85°C

DAC CODE	IDEAL VALUE (V)	MEASURED	ERROR (mV)	ERROR %
0x0000	–10	–9.9952 V	4.8	0.0240
0x8000	0	3.9 mV	3.9	0.0195
0xFFFF	10	10.0045 V	4.5	0.0225

9.3 Settling Time

The output settling time is a function of the output load capacitor. With a 100-Ω RC output resistor, 200-nF load capacitor, and no resistive load, the full scale (–10 to 10 V) positive step settling time is less than 200 µs as in Figure 33, and negative step settling time less than 160 µs as in Figure 34. These figures show also the change in the DAC output when the MUX is switched on due to charge sharing. This does not affect the settling time much. The settling time over temperature is measured within 200 µs.

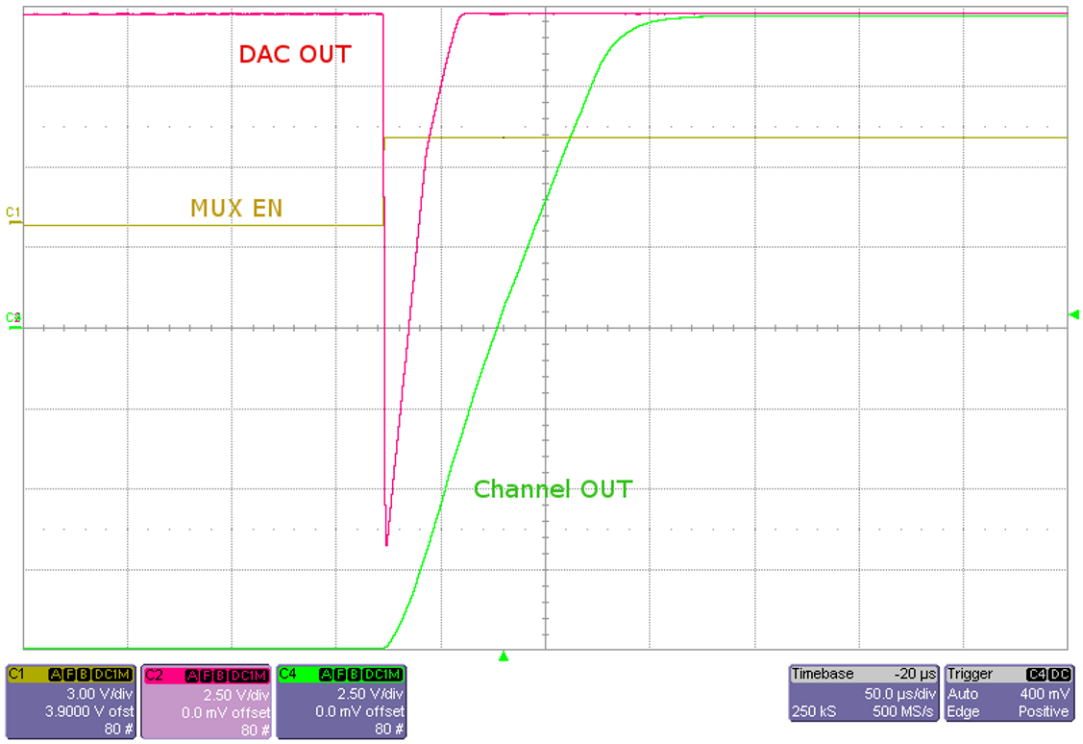


Figure 33. Positive Step Output Rise Time

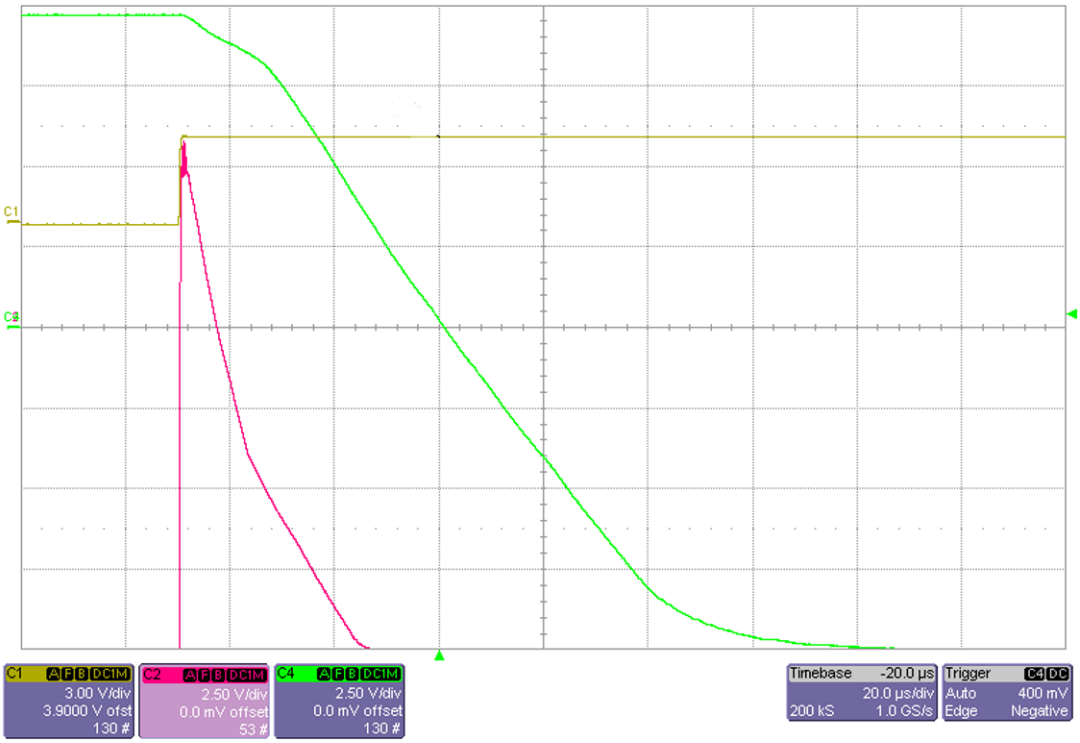


Figure 34. Negative Step Output Settling Time

The DAC settling time is faster; Figure 35 and Figure 36 show measurements of both the positive and negative step are below 120 µs. The most settling occurs in 50 µs as predicted in Section 6.2.

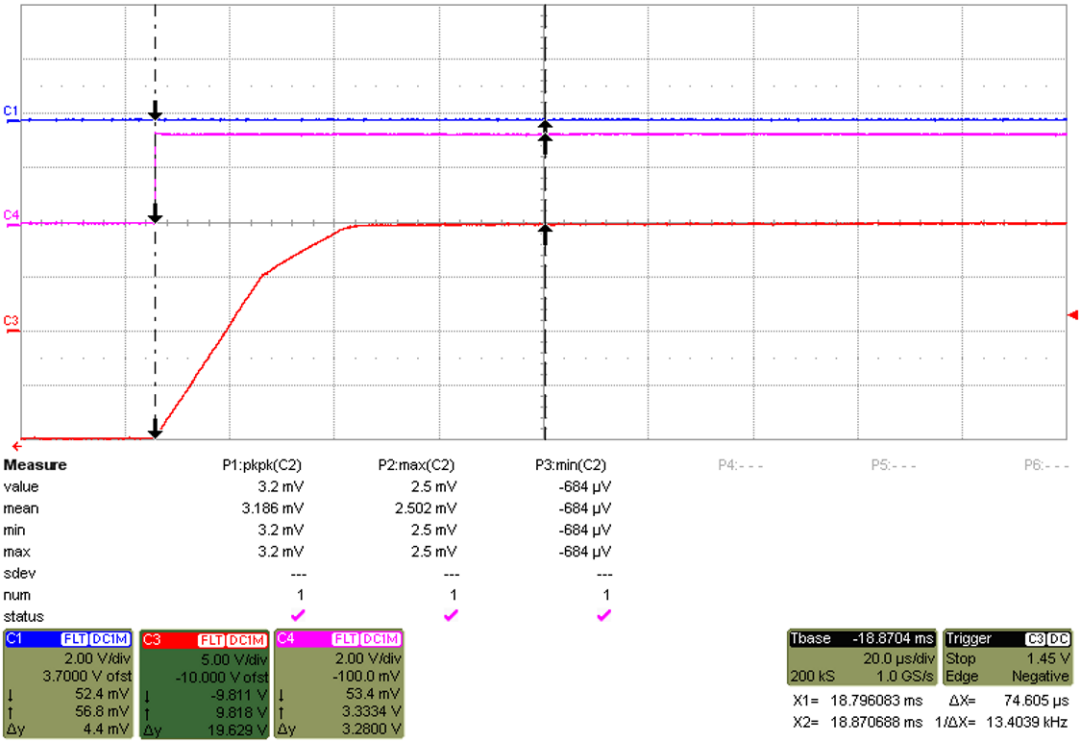


Figure 35. DAC Settling Time for Positive Step

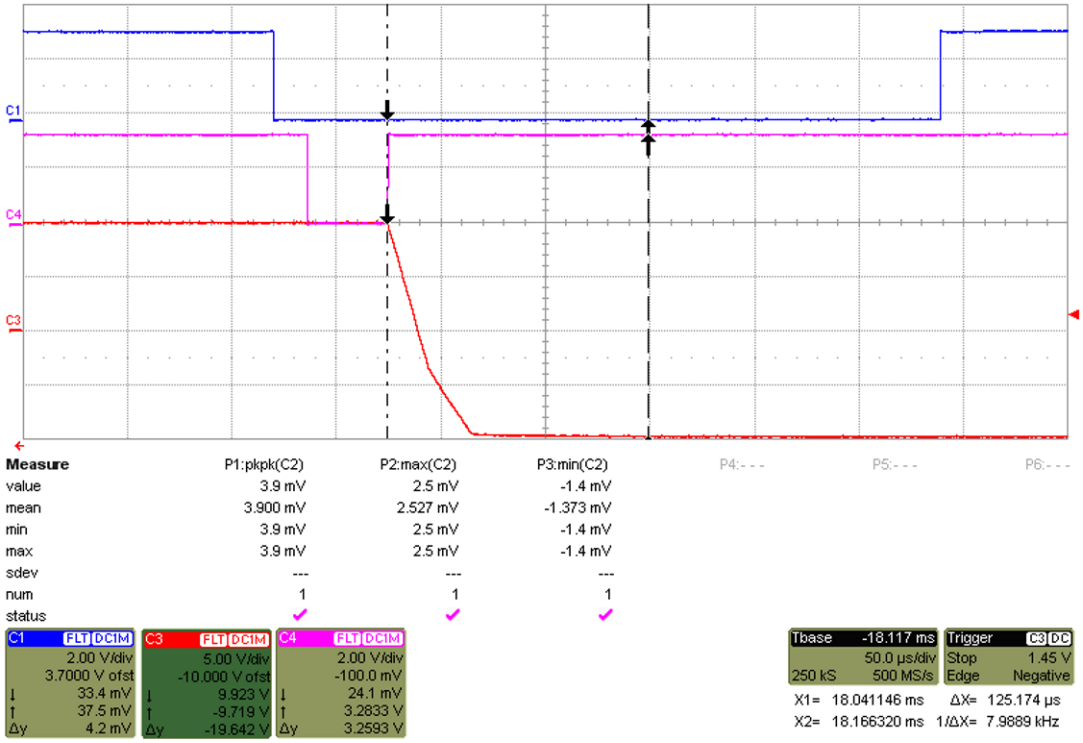


Figure 36. DAC Settling Time for Negative Step

Figure 37 shows the dynamic test, which shows the full-scale swing of the output voltage of one channel.

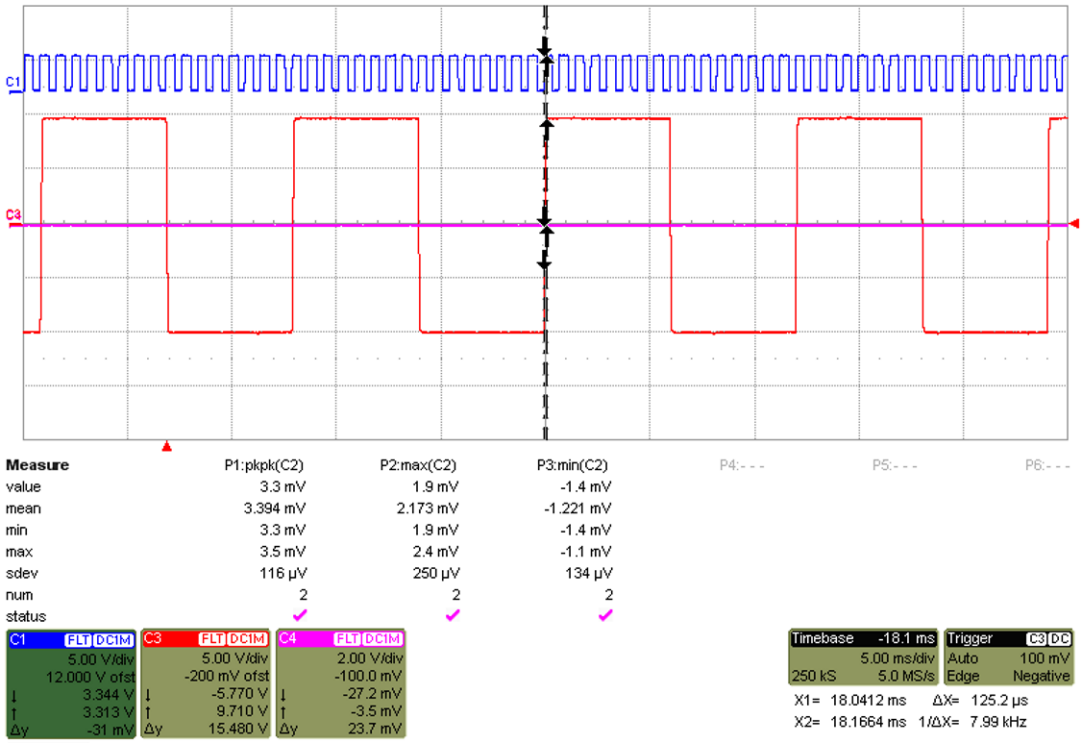


Figure 37. Voltage Output in Full-Scale Swing

9.4 Droop Rate of Hold Capacitor

The output change during the 5.5-ms hold time is so small that no change was seen on the scope. To be able to see the change due to leakage; the hold time is extended to 440 ms. The measured droop rate is 20 mV / 440 ms = 45 mV/s. This means ~250 µV in a channel time slot of 5.5 ms. This value does not change with output voltage as measures show. This value is well below the 1 LSB = 300 µV for the 14-bit 0 to 5 range (current output), and the 1 LSB = 600 µV for the 15-bit –10- to 10-V range (voltage output).

The measurement shows a lower droop at 85°C, which can be attributed to the leakage nature around the hold capacitor. The higher temperature increases the positive leakage in the capacitor and the op amp input, which somehow compensates the higher negative leakage from the MUX floating output. This comes as a benefit for using this S&H circuit.

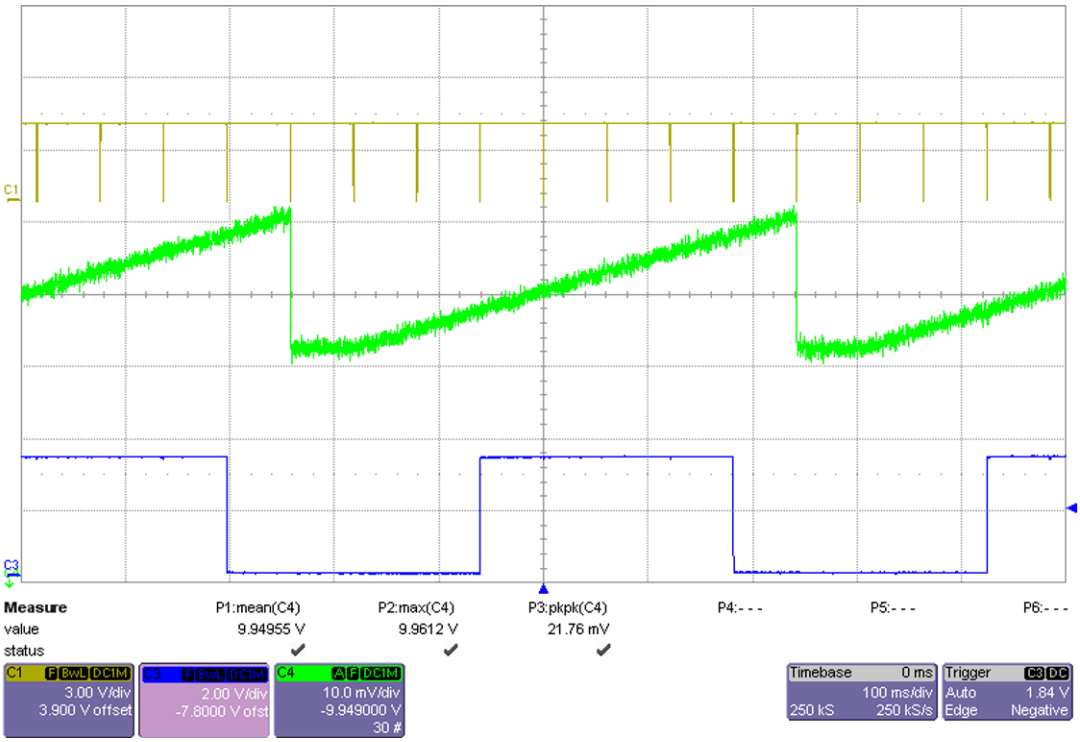


Figure 38. Droop Rate at 25°C With Exaggerated Hold Time

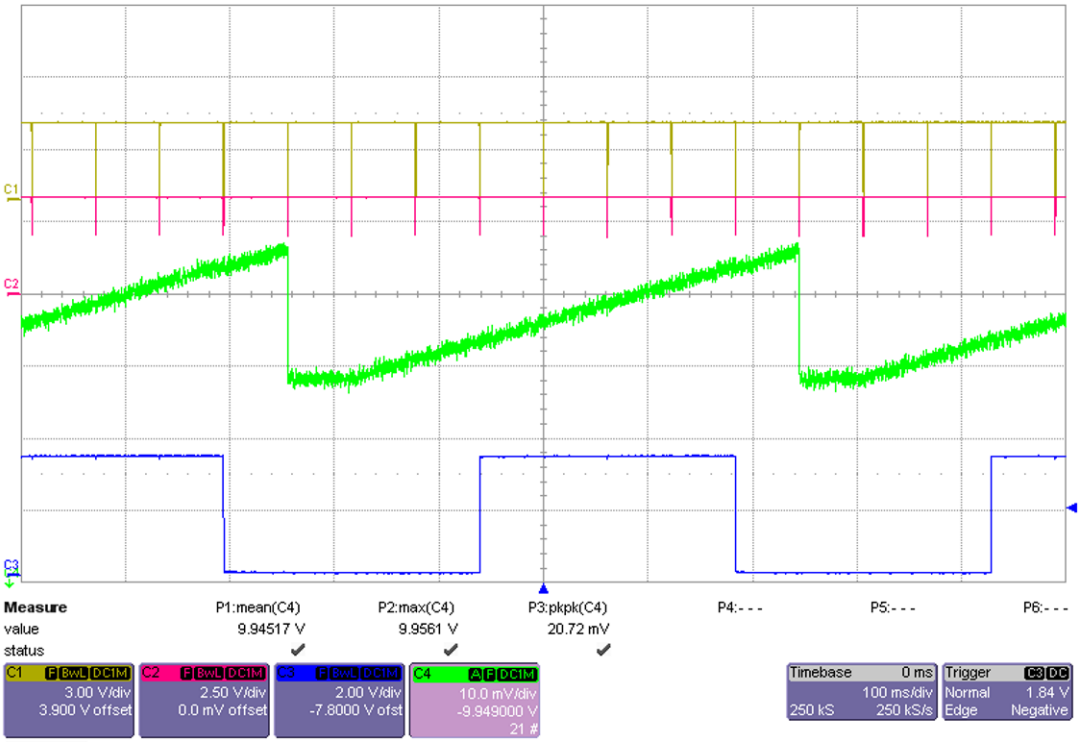


Figure 39. Droop Rate at –35°C

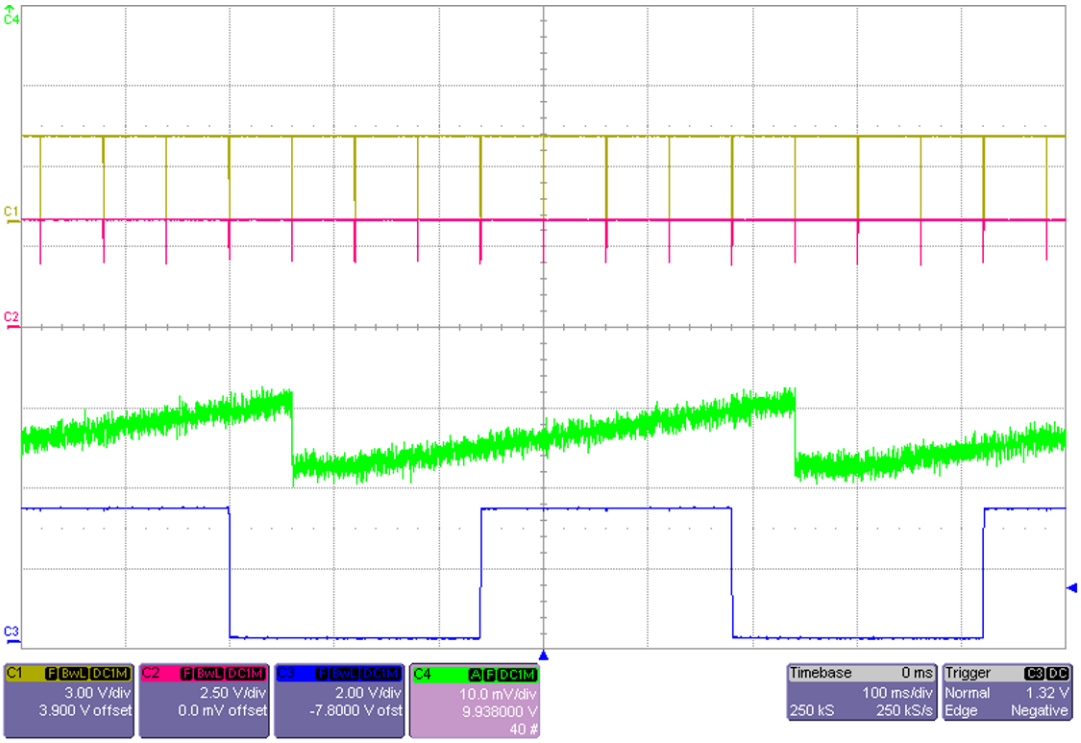


Figure 40. Droop Rate at 85°C

9.5 Crosstalk

Crosstalk measurement showed minor effects on the average value of static output when a nearby channel is experiencing full-scale toggling. Table 13 compares the measurements of a 0-V output in –10- to 10-V range, once with nearby channels static on the same 0-V level and with a ±10-V toggle on the nearby channels. It hardly affects the measured values.

Table 13. Crosstalk Effect on Static Outputs

0x8000 INPUT	AVG (µV)	MIN (µV)	MAX (µV)	STD DEV (µV)
No crosstalk	–255	–300	–211	15
With crosstalk	–237	–290	–180	15

Figure 41 shows little spikes appearing on the static channel output in response to nearby channel switching. The scope measures ~±3.5 mV for a short period of about 100 µs each. Do not eliminate errors due to scope accuracy. The –85-dB channel-to-channel isolation of the MUX is supposed to generate ~±1.2-mV spikes during transition. For any process or sensor relying on the average value of the voltage output, these short-time spikes would be negligible as Table 13 proves.

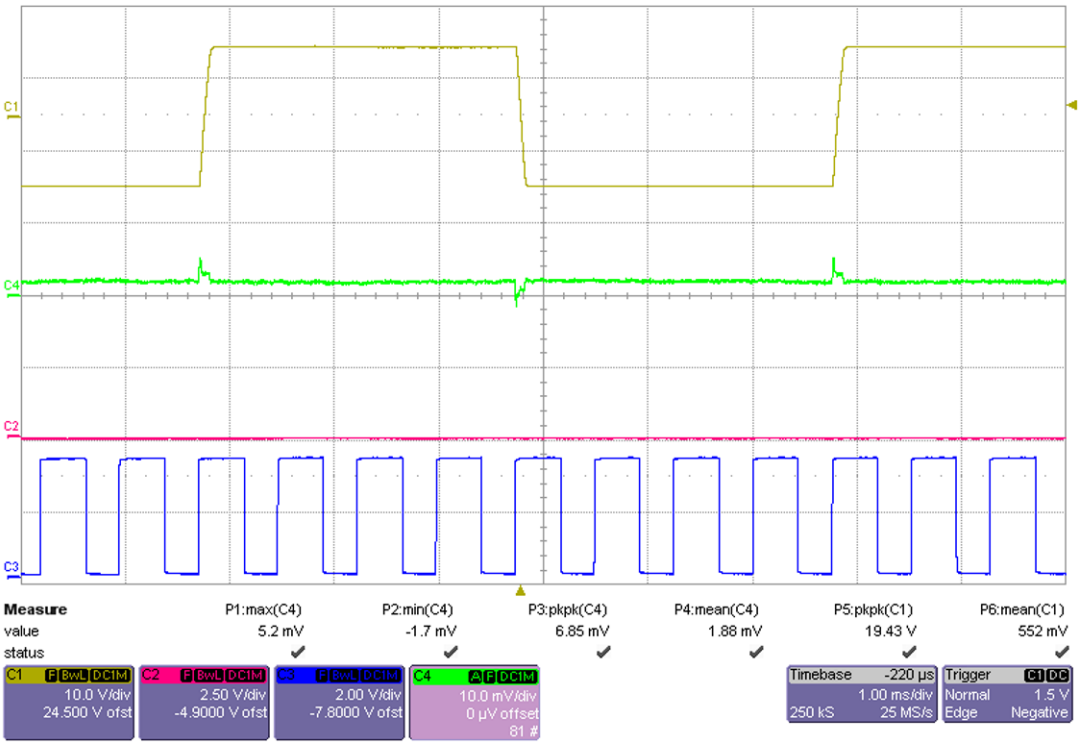


Figure 41. Waveform of Static Channel Affected by Nearby Toggling Channel

9.6 Power Consumption

With all current converters turned on, without any load, and with a scan cycle of 8 ms, the module consumes 17 mA out of the 15-V supply and 8 mA from the –15-V supply. This sums up as 25 mA from a 15-V supply = 375 mW. For a fully loaded module, each current output is added (maximum 20 mA per channel) and each voltage output (maximum 10 V/2 kΩ = 5 mA per channel).

10 Design Files

10.1 Schematics

To download the schematics, see the design files at TIDA-00760.

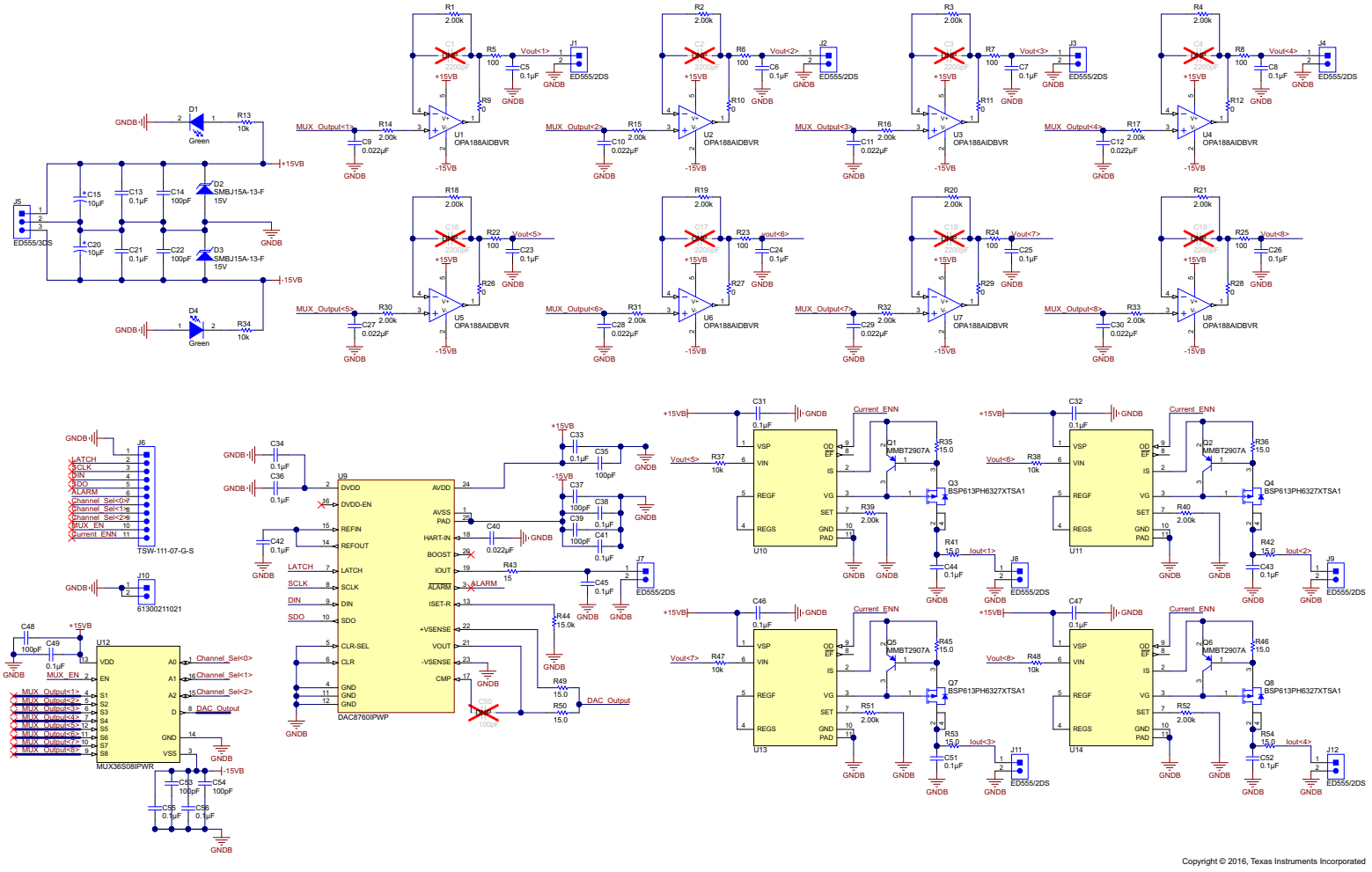


Figure 42. TIDA-00760 Schematic

10.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00760.

Table 14. BOM

ITEM	DESIGNATOR	QTY	VALUE	PARTNUMBER	MANUFACTURER	DESCRIPTION	PACKAGE REFERENCE
1	C5, C6, C7, C8, C13, C21, C23, C24, C25, C26, C31, C32, C33, C34, C36, C38, C41, C42, C43, C44, C45, C46, C47, C49, C51, C52, C55, C56	28	0.1uF	GRM188R71H104KA93D	MuRata	CAP, CERM, 0.1 µF, 50 V, +/- 10%, X7R, 0603	0603
2	!PCB1	1		TIDA-00760	Any	Printed Circuit Board	
3	H5, H6, H7, H8	4		1902C	Keystone	Standoff, Hex, 0.5"L #4-40 Nylon	Standoff
4	J1, J2, J3, J4, J7, J8, J9, J11, J12	9		ED555/2DS	On-Shore Technology	Terminal Block, 6A, 3.5mm Pitch, 2-Pos, TH	7.0x8.2x6.5mm
5	J5	1		ED555/3DS	On-Shore Technology	Terminal Block, 6A, 3.5mm Pitch, 3-Pos, TH	10.5x8.2x6.5mm
6	D2, D3	2	15V	SMBJ15A-13-F	Diodes Inc.	Diode, TVS, Uni, 15 V, 600 W, SMB	SMB
7	D1, D4	2	Green	LTST-C190KGKT	Lite-On	LED, Green, SMD	1.6x0.8x0.8mm
8	C15, C20	2	10uF	293D106X9050E2TE3	Vishay-Sprague	CAP, TA, 10 µF, 50 V, +/- 10%, 0.8 ohm, SMD	7343-43
9	H1, H2, H3, H4	4		NY PMS 440 0025 PH	BandF Fastener Supply	Machine Screw, Round, #4-40 x 1/4, Nylon, Philips panhead	Screw
10	C40	1	0.022uF	C1608X7R1H223K	TDK	CAP, CERM, 0.022 µF, 50 V, +/- 10%, X7R, 0603	0603
11	C9, C10, C11, C12, C27, C28, C29, C30	8	0.022uF	C0603X223K5RACTU	Kemet	CAP, CERM, 0.022 µF, 50 V, +/- 10%, X7R, 0603	0603
12	C14, C22, C35, C37, C39, C48, C53, C54	8	100pF	06035A101JAT2A	AVX	CAP, CERM, 100 pF, 50 V, +/- 5%, C0G/NP0, 0603	0603
13	J6	1		TSW-111-07-G-S	Samtec	Header, 100mil, 11x1, Gold, TH	11x1 Header
14	J10	1		61300211021	Wurth Elektronik	Header, 2.54 mm, 2x1, Gold, R/A, TH	Header, 2.54 mm, 2x1, R/A, TH
15	Q1, Q2, Q5, Q6	4	60 V	MMBT2907A	Fairchild Semiconductor	Transistor, PNP, 60 V, 0.8 A, SOT-23	SOT-23
16	Q3, Q4, Q7, Q8	4	-60V	BSP613PH6327XTSA1	Infineon Technologies	MOSFET, P-CH, -60 V, -2.9 A, SOT-223	SOT-223

Table 14. BOM (continued)

ITEM	DESIGNATOR	QTY	VALUE	PARTNUMBER	MANUFACTURER	DESCRIPTION	PACKAGE REFERENCE
17	R1, R2, R3, R4, R14, R15, R16, R17, R18, R19, R20, R21, R30, R31, R32, R33, R39, R40, R51, R52	20	2.00k	CPF0603B2K0E	TE Connectivity	RES, 2.00 k, 0.1%, 0.063 W, 0603	0603
18	R5, R6, R7, R8, R22, R23, R24, R25	8	100	CRCW0603100RFKEA	Vishay-Dale	RES, 100, 1%, 0.1 W, 0603	0603
19	R9, R10, R11, R12, R26, R27, R28, R29	8	0	CRCW06030000Z0EA	Vishay-Dale	RES, 0, 5%, 0.1 W, 0603	0603
20	R13, R34, R37, R38, R47, R48	6	10k	CRCW060310K0JNEA	Vishay-Dale	RES, 10 k, 5%, 0.1 W, 0603	0603
21	R35, R36, R41, R42, R45, R46, R49, R50, R53, R54	10	15.0	CRCW060315R0FKEA	Vishay-Dale	RES, 15.0, 1%, 0.1 W, 0603	0603
22	R43	1	15	RPC2512JT15R0	Stackpole Electronics	RES 15 OHM 1W 5% 2512	2512
23	R44	1	15.0k	RT0603BRD0715KL	Yageo America	RES, 15.0 k, 0.1%, 0.1 W, 0603	0603
24	U1, U2, U3, U4, U5, U6, U7, U8	8		OPA188AIDBVR	Texas Instruments	Precision, Low-Noise, Rail-to-Rail Output, 36 V, Zero-Drift Operational Amplifiers, DBV0005A	DBV0005A
25	U9	1		DAC8760IPWP	Texas Instruments	Single-Channel, 16-Bit Programmable Current Output and Voltage Output DIGITAL-TO-ANALOG CONVERTER for 4-mA to 20-mA Current Loop Applications, PWP0024J	PWP0024J
26	U10, U11, U13, U14	4		XTR111AIDGQT	Texas Instruments	Precision Voltage-to-Current Converter/Transmitter, DGQ0010D	DGQ0010D
27	U12	1		MUX36S08IPWR	Texas Instruments	Fault-Protected, 8-Channel, Single-Ended Multiplexer, PW0016A	PW0016A
28	C1, C2, C3, C4, C16, C17, C18, C19	0	2200pF	GRM1885C1H222JA01D	MuRata	CAP, CERM, 2200 pF, 50 V, +/- 5%, C0G/NP0, 0603	0603
29	C50	0	100pF	06035A101JAT2A	AVX	CAP, CERM, 100 pF, 50 V, +/- 5%, C0G/NP0, 0603	0603
30	FID1, FID2, FID3	0		N/A	N/A	Fiducial mark. There is nothing to buy or mount.	N/A

10.3 Altium Project

To download the Altium project files, see the design files at TIDA-00760.

10.4 Gerber Files

To download the Gerber files, see the design files at TIDA-00760.

10.5 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-00760.

11 References

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12 About the Authors

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Revision A History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (March 2016) to A Revision	Page
• Changed from preview page	1

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