TI Designs

IO-Link Adapter Reference Design for Sensors With Analog 4- to 20-mA Output

TI Designs

This TI Design is an IO-Link adapter, which evaluates the binary or analog 4- to 20-mA output signal of sensors in the industrial environment and forwards the results to the PLC through IO-Link. This design fits in a 6-mm wide PCB compatible with the industry standard M12 connector.

Design Resources

TIDA-00457	Design Folder
MSP430FR5738	Product Folder
SN65HVD101	Product Folder
ADS1220	Product Folder
TIDA-00648	Tools Folder
TIDA-00188	Tools Folder
TIDA-00339	Tools Folder

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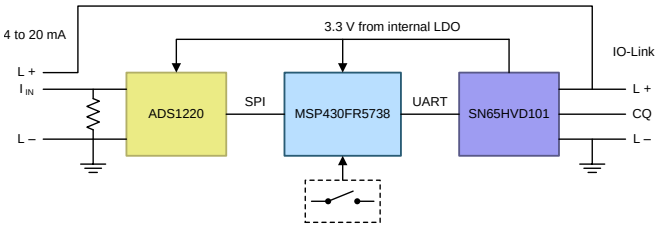
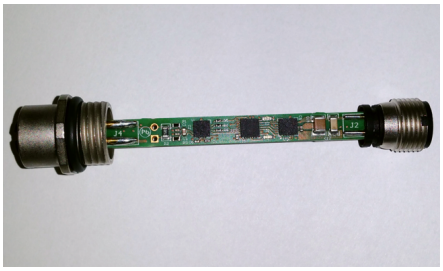
Design Features

- IO-Link v1.1 and v1.0 Connectivity
- Connects With Sensor Transmitter in 2- or 3-Wire Technology
- One Analog and One Binary Input
- Current Range: 4 to 20 mA
- Small Form Factor (6-mm Board Width)
- Loop-Error Detection and Reporting
- Supply Through IO-Link Interface

Featured Applications

- Factory Automation and Process Control
- Building Automation
- Sensors and Field Transmitters
- Portable Instrumentation
- Field Actuators





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1 Key System Specifications

Table 1. Key System Specifications

PARAMETER		SPECIFICATION
IO-Link	IO-Link version	V1.1 (compatible to V1.0)
	SIO mode	Supports SIO mode
	Baud rate support	COM1, COM2, COM3
4- to 20-mA sensor input	Input signal	4- to 20-mA current loop according to NAMUR NE-43
	Supply voltage	9 to 30 V
	Error input currents	Low: 3.375 mA (typical) High: 21.75 mA (typical)
	Burden resistor	75 Ω
	Resolution	24 bit
Operating temperature		–40°C to 85°C
Interface connectors		M12

2 System Description

Monitoring and maintaining process variables at the appropriate levels is extremely critical in industrial automation and process control. A sensor in the industrial environment is either continuously or periodically measuring vital parameters such as temperature, pressure, flow, and so forth. In industrial instruments, analog 4- to 20-mA current loops are commonly used for analog signaling today, with 4 mA as the lowest measured value of a sensor and 20 mA as the highest. This reference design is an IO-Link device that converts these analog signals (4 to– 20 mA) into the IO-Link protocol. Therefore, it offers the option of acquiring the signals of analog sensors through an IO-Link master.

IO-Link is the first standardized IO technology worldwide (IEC 61131-9) to communicate with sensors and actuators. IO-Link answers the need of these digital and analog sensors and actuators to exchange process data, diagnosis information, and parameters with a controller (PC or PLC) using a low-cost, digital communication technology. The connection between the IO-Link master and device is established through a (at maximum) 20-m long 3-wire cable. The wiring is standardized on the basis of M5, M8, and M12. The vast majority of IO-Link devices are equipped with M12 connectors, which can be used without any restrictions for IO-Link's switching mode and communication mode. Each port of an IO-Link master is capable of processing binary switching signals and analog values (for example, 8 bits, 12 bits, 16 bits). Serial IO-Link communication takes place through the same port. Easy wiring, automated parameter setting, and extended diagnosis are but a few advantages of IO-Link.

The design files include schematics, bill of materials (BOM), layer plots, Altium files, and Gerber files.

3 System Design Theory

The TIDA-00457 IO-Link Adapter Reference Design is an IO-Link device that converts analog 4- to 20-mA signals into the IO-Link protocol. Therefore, it offers the option of acquiring the signals of analog sensors through an IO-Link master. Converting analog signals directly at the measurement location and digital transmission through unshielded cables simplify installation and result in interference-free transmissions of measured values.

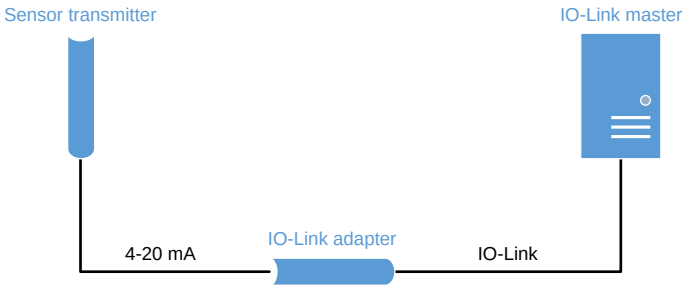


Figure 1. System Overview

Design features are:

- 1 IO-Link interface through M12 connector
- 1 analog input (4 to 20 mA) through M12 connector
- Connection of the sensor in 2- and 3-wire technology
- Binary input
- Small form factor
- Supply of the module electronics and the sensor through the IO-Link interface of the IO-Link master

In the IO-Link Demonstrator setup (Figure 27), the TI-Design TIDA-00648 is used as an analog 4- to 20-mA current loop transmitter.

3.1 4- to 20-mA Current Loop Input

A typical current-loop system basically consists of four components as Figure 2:

- Sensor (temperature, pressure, and so forth)
- 4- to 20-mA current loop transmitter
- Loop power supply
- Loop receiver

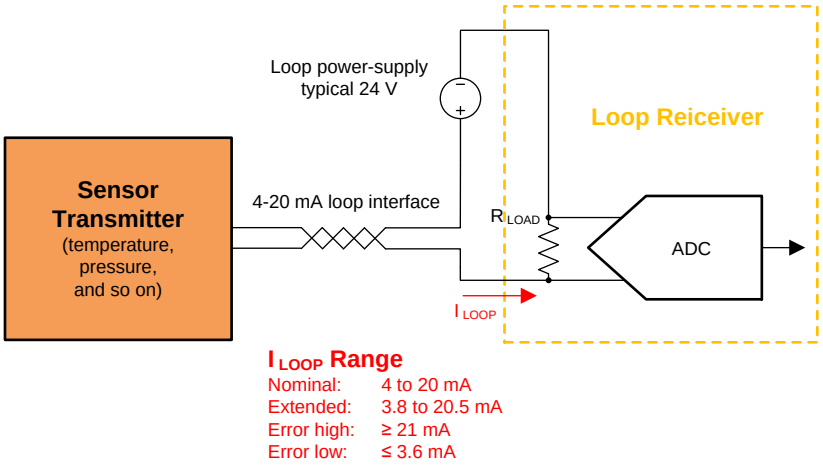


Figure 2. Typical Current-Loop System

By regulating the current supplied by the loop power supply, the transmitter converts the output of a sensor to a proportional 4- to 20-mA DC current. The zero-value process variable is represented by 4 mA. The full scale process variable is represented by 20 mA. Therefore, a 16-mA span is available to represent the entire measurement information range.

The sensor transmitter can be connected in 2- or 3-wire technology through the M12 connector to the TIDA-00457 reference design. In 2-wire technology, the current returns back to the power supply after flowing through a precision load resistor of the loop receiver (Figure 3).

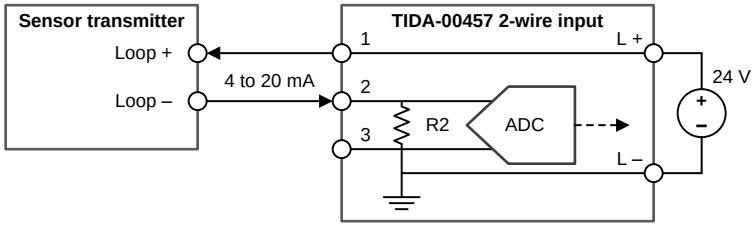


Figure 3. 2-Wire Transmitter

The L+ signal of the IO-Link is used to power the sensor transmitter. The power source forms together with the loop receiver and with the two-wire loop powered transmitter, the current loop. A 2-wire cable is sufficient for the electrical connection. Those two wires power the transmitter as well as transmit the signal by controlling the loop current, which equals the total current consumption of the transmitter.

On the loop receiver side of the system, the loop current causes a voltage drop across the load resistance R2 inside the receiver (Figure 4). This voltage drop is measured using the ADS1220.

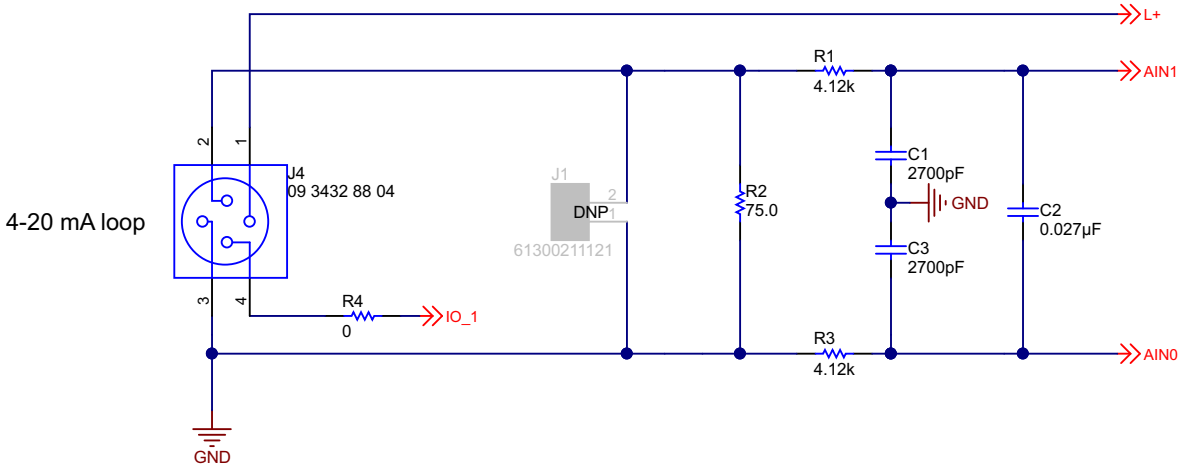


Figure 4. Analog Input

Typical load resistance levels range from some tens of Ω to some hundreds of Ω. In this application, the load resistor R2 is 75 Ω, which is exemplary; the voltage drop across this resistor changes from 300 mV to 1.5 V for loop currents of 4 to 20 mA.

If the loop current is not sufficient to power the transmitter, a third wire can be added for separate power supply. 3-wire transmitters use two wires for the power supply and output the signal through a third separate wire. The reference potential is the GND wire (Figure 5).

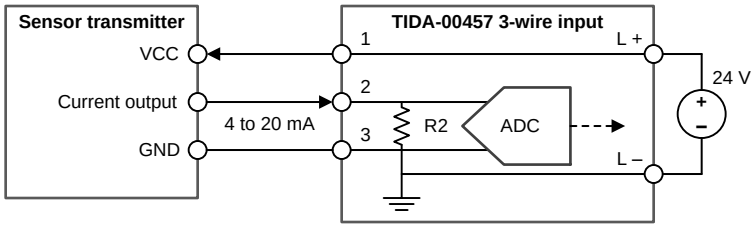


Figure 5. 3-Wire Transmitter

Additional values or value ranges for the loop current are specified, for example, in the NAMUR recommendation [8], extending the working range from 3.8 to 20.5 mA to support activities like adjustment, calibration, and the detection of range overflow. Furthermore, loop currents below 3.6 mA or above 21 mA are recommended for failure detection.

Choosing current instead of voltage as an information carrier is generally preferential for the following reasons:

- Current loops have inherent immunity against noise.
- Transmitting current signal over long distances does produce the voltage drop (also known as voltage loss or loop drop) across the loop because of wiring resistance. However, the magnitude of signaling is not affected when the loop power supply is high enough to compensate for these losses and still meets the compliance voltage requirement at the transmitter for the transmitter's proper operation. Basic circuit theory shows that current is the same along the signal line, which means the same amount of current supplied by the loop power supply always returns back to the source.
- The residual 4-mA current at zero point allows easy detection of a wire-break condition. The residual 4-mA current at zero point also allows the transmitter to be powered up if the current requirement is within 4 mA. The current exceeds 20 mA for a short-circuit condition; therefore, current loops are self-monitoring.
- Choosing current instead of voltage minimizes the cost and simplifies the installation because signal current and transmitter power-supply current share the same pair of conductors.

3.2 Introduction to IO-Link Interface

IO-Link is targeted for machine automation with up to 20 meters in data communication link. The advantage for analog (that is, 4 to 20 mA) is for long-distance communication typically used for process automation. The disadvantage is the complexity leading to increased hardware and software design costs such as expensive shielded cabling.

3.2.1 IO-Link

CAUTION

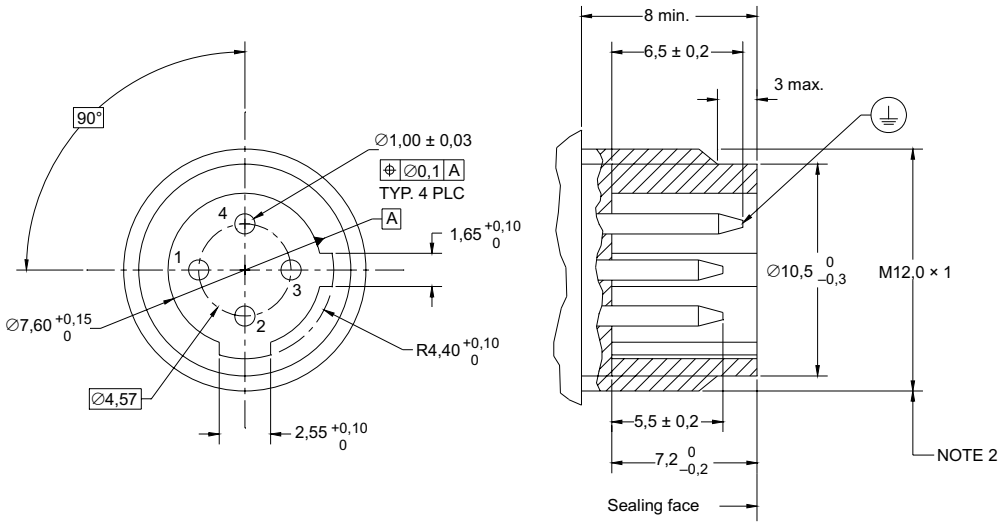
To facilitate a ground-up IO-Link device project, this section provides a quick overview of the IO-Link interface. This section should, under no condition, be considered a reference. Only the reference documents should be used after the initial phase of the project.

IO-Link [(1)] is a simple and cheap point-to-point protocol (standardized as IEC 61131-9) for the industrial automation and control applications.

Though the IO-Link clearly states that a master can have several ports, each of which can have a unique device connected to it, the rest of this document refers to a connection between the master and the device to avoid a heavy "master-port" naming of a potentially misleading "port" denomination.

3.2.1.1 IO-Link Physical Connectors

The IO-Link connectors pin assignment is based on IEC60947-5-2 with extensions specified in *IO-Link Interface and System Specification v1.1.2* [5]. Figure 6 is a capture of the M12 connector selected for this project from IEC60947-5-2.



NOTE 1 Pin identification numbering is not necessary.

NOTE 2 For a provisional period, the use of 1/2"-20UNF-2A is permissible as an alternative to M12 on a.c. proximity switches.

NOTE 3 The protective earth pin shall be omitted for class II proximity switches.

Figure 6. M12 ∅ 4-Pin Integral Connector (Defined by IEC 60947.5.2)

(1) IO-Link is a trade name of the *IO-Link Community*. This information is given for the convenience of users of this international standard and does not constitute an endorsement by IEC of the trade name holder or any of its products. Compliance to this standard does not require use of the registered logos for IO-Link. Use of the registered logos for IO-Link requires permission of the *IO-Link Community*. [5]

The electrical connections are described in Table 2 and shown in Figure 7, both extracted from *IO-Link Interface and System Specification v1.1.2* [5].

Table 2. M12 4-Pin Assignments

PIN	SIGNAL	DESTINATION	REMARK
1	L+	Power supply (+)	See Table 7 from source [5]
2	I/Q P24	NC/DI/DO (port class A) P24 (port class B)	Option 1: NC (not connected) Option 2: DI Option 3: DI, then configured DO Option 4: Extra power supply for power devices (port Class B)
3	L–	Power supply (–)	See Table 7 from source [5]
4	C/Q	SIO/SDCI	Standard I/O mode (DI/DO) or SDCI See Table 6 from source [5] for electrical characteristics of DO.
5	NC N24	NC (port class A) N24 (port class B)	Option 1: Shall not be connected on the master side Option 2: Reference to the extra power supply (port Class B)

NOTE: M12 is always a 5-pin version on the master side (female).

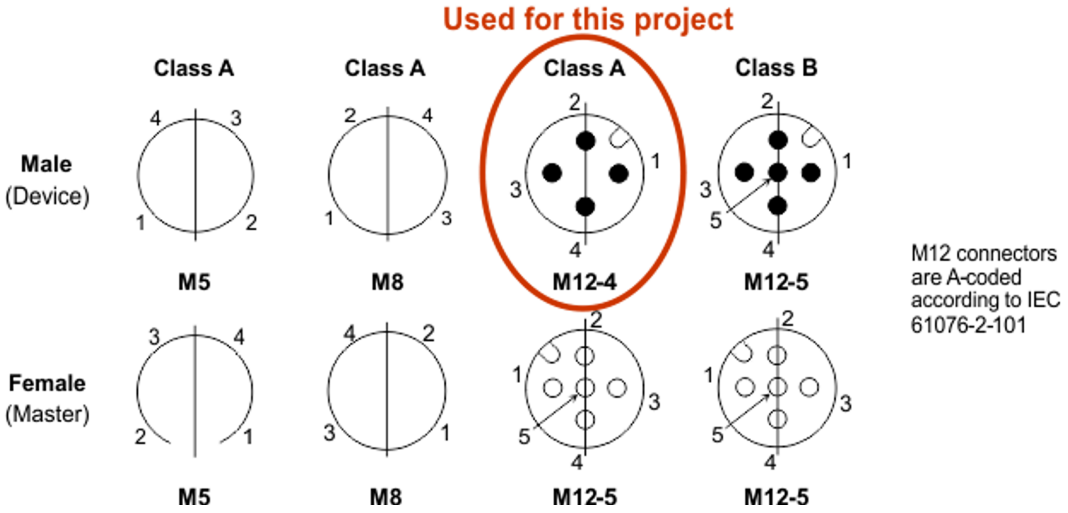


Figure 7. M12 4-Pin Layout

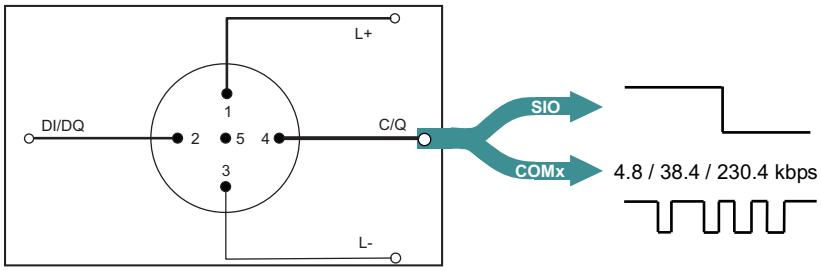
According to *IO-Link Interface and System Specification v1.1.2* [5], the current project is only using the port Class A definition. Cables are also specified by *IO-Link Interface and System Specification v1.1.2*, with a maximum length of 20 m and associated maximum resistance and capacitance.

3.2.1.2 IO-Link Device Power

The IO-Link device (Class A) can draw its power from the L+ line and is only allowed to draw up to 200 mA from a voltage, which varies between 18 and 30 V. The IO-Link device must be functional less than 300 ms after the supply passes the 18-V threshold. [5]

3.2.1.3 IO-Link Communication Layer

The IO-Link communication can be seen as having two modes. The first mode is a back-up, quasi-static mode that ensures backward compatibility with standard I/O (SIO) mode specified in IEC61131-2. The second mode is the newly defined dynamic mode for bi-directional communication (SDCI) defined by *IO-Link Interface and System Specification v1.1.2* [5]. A good overview is provided by Figure 8 (combined from [5] and *Programmable Controllers – Part 2: Equipment Requirements and Tests*).



Pin	Signal	Definition	Standard
1	L+	24 V	IEC 61131-2
2	I/Q	Not connected, DI, or DO	IEC 61131-2
3	L-	0 V	IEC 61131-2
4	Q	"Switching signal" DI (SIO)	IEC 61131-2
	C	"Coded switching" (COM1, COM2, COM3)	IEC 61131-9

Figure 8. SIO versus SDCI (or IEC61131-9 versus IEC61131-2)

The switch between SIO mode and SDCI is master initiated.

The master issues a wake-up command to the device, which consists in shorting the 80-µs CQ line with at least 500 mA (IQPKHM) [5]. The device must be ready for communication in less than 500 µs (TREN).

After the wake-up request (WURQ), the master waits for the device to be enabled for TREN [5]. The master then tries to identify the highest transmission rate supported by the device by sending a test message (M-sequence type 0). See Section 3.2.1.3.2 for details.

Following the wake-up attempt, should communication fail, the device switches back to SIO mode within a time window of 60 to 300 ms (TDSIO) [5].

If communication is successful, it occurs on a frame basis.

3.2.1.3.1 Physical Layer

Handshake

The master issues a wake-up command to the device, which consists in shorting the CQ line for 80 µs with at least 500 mA (IQPKHM) [5]. The device must be ready for communication in less than 500 µs (TREN).

The short from the master will be made in such a way that the master shorts the CQ line to the opposite value driven by the device to ensure the device senses the current surge the master is driving on the CQ line (see Figure 9).

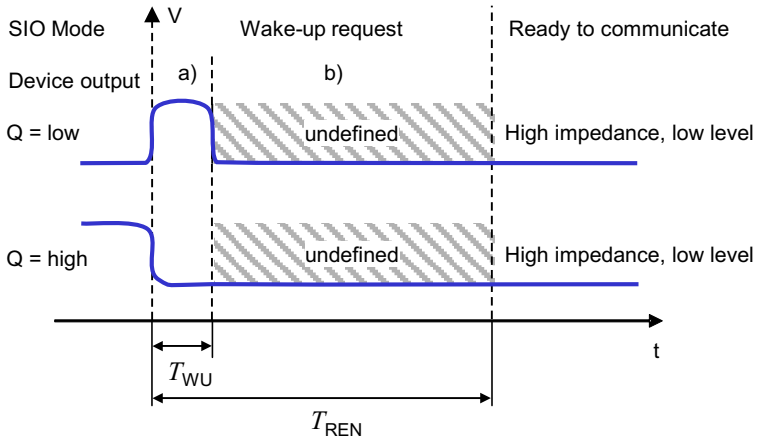


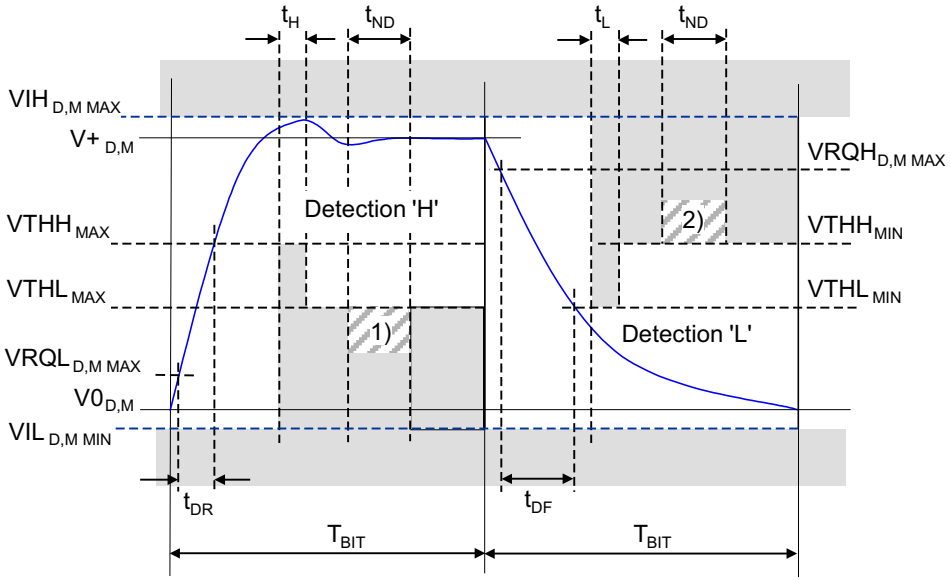
Figure 9. Wake-Up Request

Modulation

Communication is done with a universal asynchronous receiver or transmitter (UART) frame consisting of 11 bits (1 start bit + 8 bit data + 1 bit parity + 1 STOP bit).

Bits are transmitted over the CQ line with a simple non-return-to-zero, or NRZ (that is, a logical '0' is 24 V between CQ and L–, and a logical '1' is 0 V between CQ and L–).

Bit durations are defined by the transmission rate (the highest transmission rate at which the device can detect the test message sent by the master). The eye diagrams are illustrated by Figure 10 and Figure 11.



In the figure, 1) = no detection 'L'; and 2) = no detection 'H'

Figure 10. Eye Diagram for the 'H' and 'L' Detection

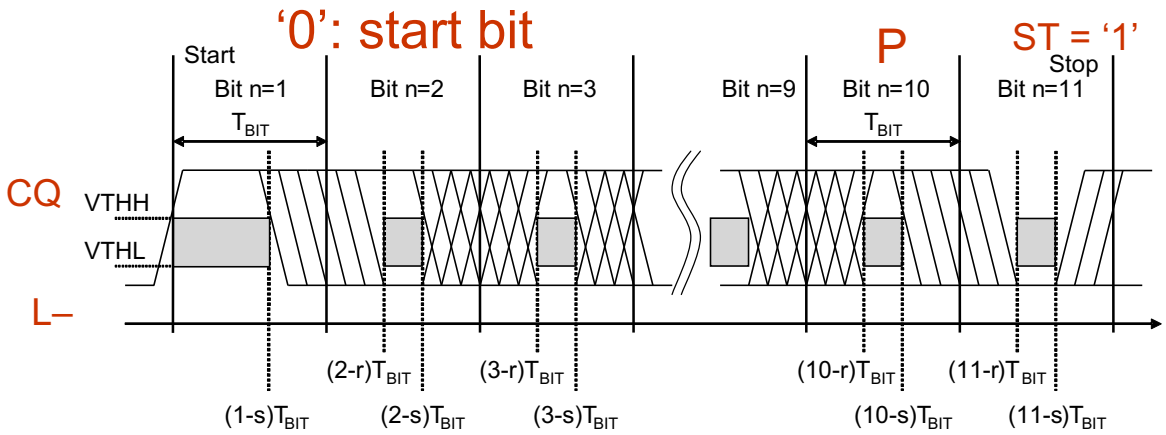


Figure 11. Eye Diagram for the Correct Detection of a UART Frame

3.2.1.3.2 Data Link Layer

Transmission Frame

Communication between a master and its associated device takes place in a fixed schedule, called the message sequence (M-sequence) time ($t_{M\text{-sequence}}$) defined in *IO-Link Interface and System Specification v1.1.2* [5] of which Figure 12 is an extract.

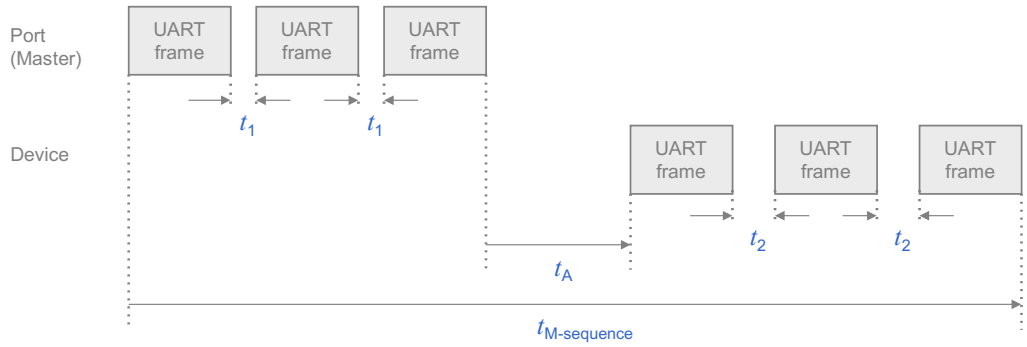


Figure 12. M-Sequence Timing

Transmission Rate Negotiation

After the WURQ, the master sends a test message with M-sequence TYPE_0 and should the device be capable of deciphering, the device should answer within t_A to the master (see Figure 13 and Figure 14).

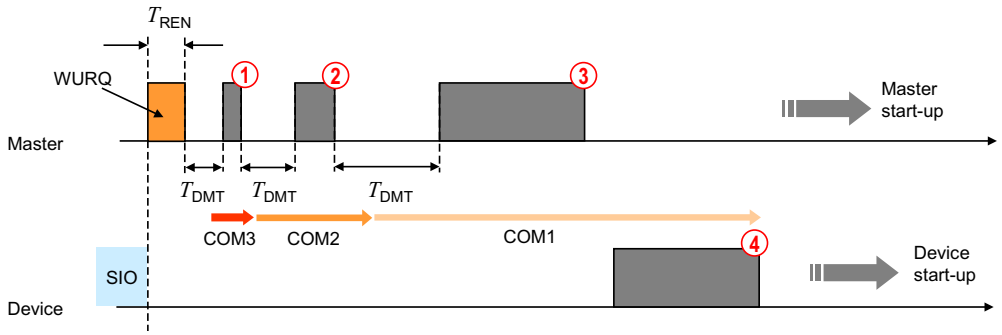


Figure 13. Example of Successful Transmission Rate Negotiation

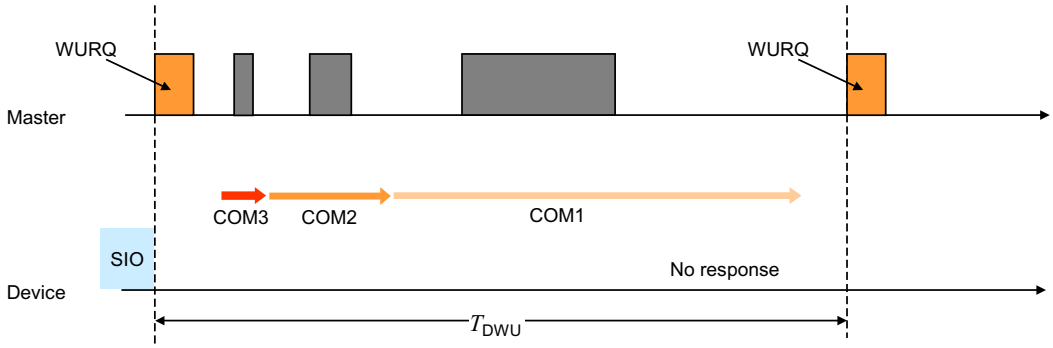


Figure 14. Example of Failed Transmission Rate Negotiation

Data Link Layer Services

Once established, the master and devices have access to services summarized in Table 3.

Table 3. Service Assignments Within Master and Device

SERVICE NAME	MASTER	DEVICE
DL_ReadParam	R	I
DL_WriteParam	R	I
DL_ISDUTransport	R	I
DL_ISDUAbort	R	I
DL_PDOutputUpdate	R	
DL_PDOutputTransport		I
DL_PDInputUpdate		R
DL_PDInputTransport	I	
DL_PDCycle	I	I
DL_SetMode	R	
DL_Mode	I	I
DL_Event	I	R
DL_EventConf	R	
DL_EventTrigger		R
DL_Control	I / R	R / I
DL_Read	R	I
DL_Write	R	I
Key		
I	Initiator of a service (towards the layer above)	
R	Receiver (responder) of a service (from the layer above)	

3.2.1.3.3 Application Layer

Once established, the master can then access the structure and services of the device application layer as illustrated by Figure 15.

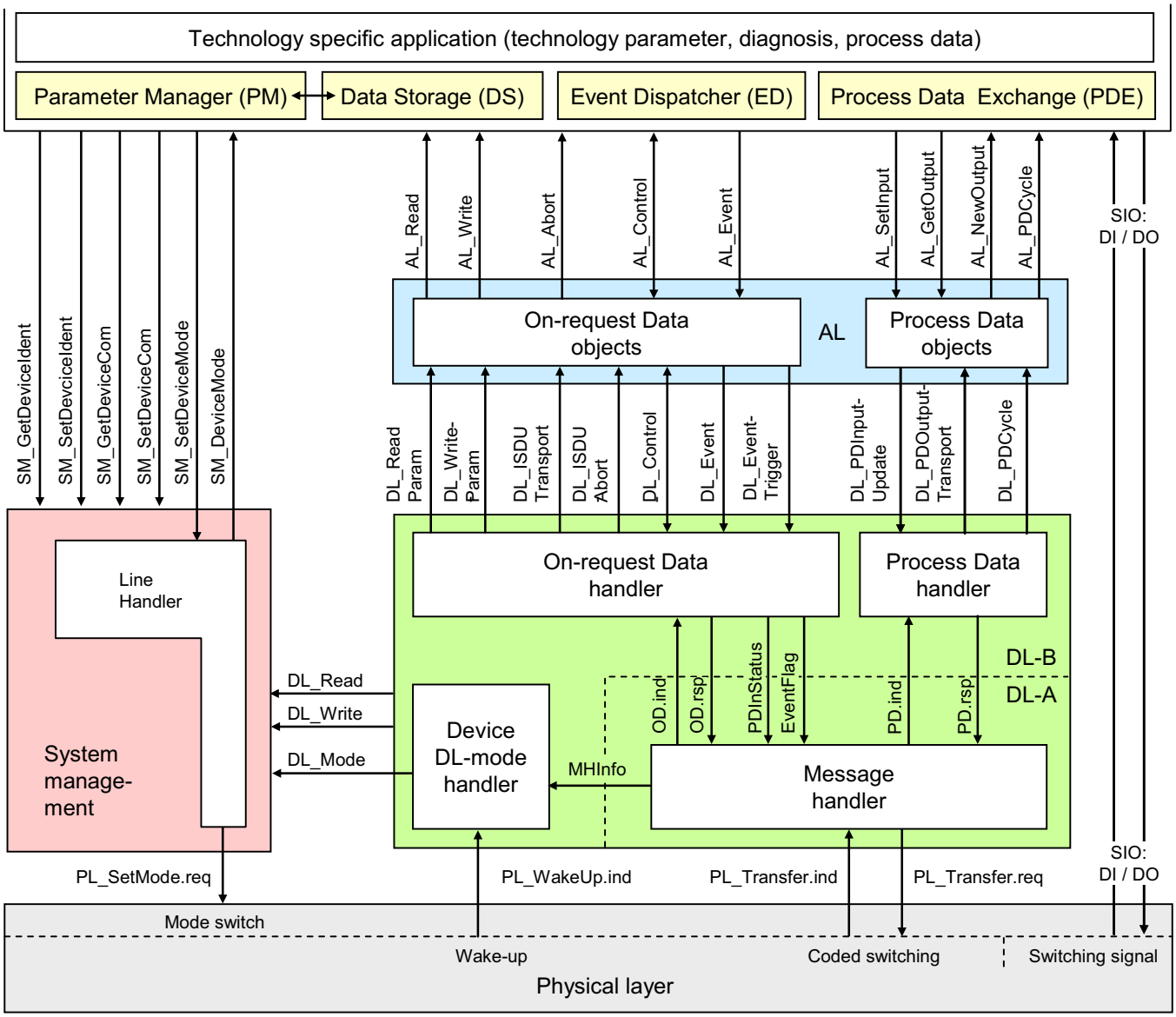


Figure 15. Structure and Services of the Device Application Layer

4 Block Diagram

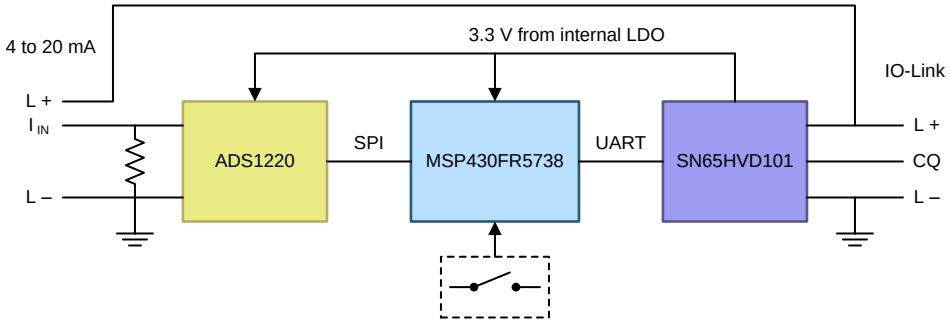


Figure 16. TIDA-00457 System Block Diagram

4.1 Highlighted Products

The system leverages the following semiconductor integrated circuits:

- MSP430FR5738: features embedded ferroelectric RAM (FRAM) nonvolatile memory, which brings unique capabilities for field updates and logging
- SN65HVD101: a dedicated interface product for IO-Link buses which provides a full PHY support and LDO to power the rest of the system
- ADS1220: offers low-power analog-to-digital converter (ADC) with SPI to read back the MCU

4.1.1 MSP430FR5738

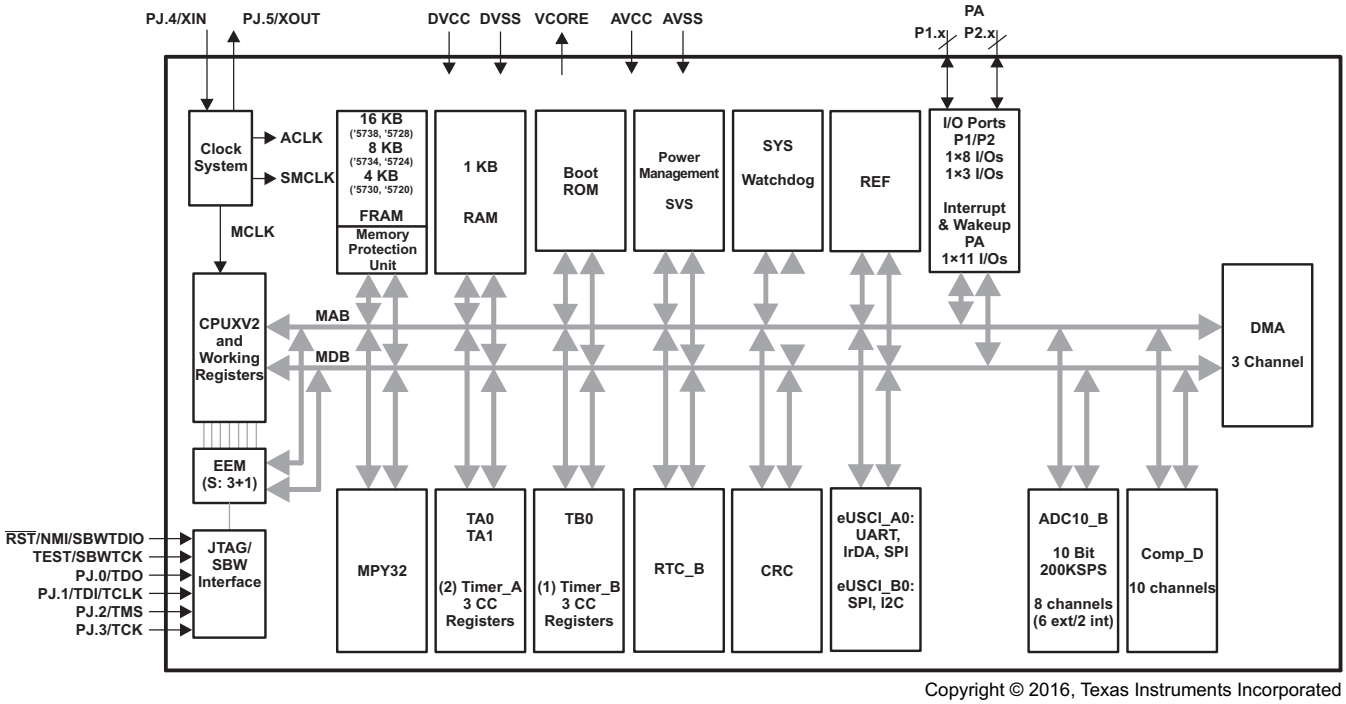


Figure 17. Functional Block Diagram MSP430FR5738

The MSP430™ ULP FRAM platform is used in the TIDA-00457 reference design. The MSP430 combines a uniquely embedded FRAM and a holistic ULP system architecture, allowing innovators to increase performance at lowered energy budgets. FRAM is much faster to write to than flash and has near infinite endurance, which means that in a remote sensor, data could be written more often for improved data accuracy, or it could collect data for longer. Due to the lack of a charge pump, FRAM enables lower average and peak power during writes. Writing to FRAM does not require a setup sequence or additional power when compared to reading from FRAM. The FRAM read current is included in the active mode current consumption numbers already.

The bitwise programmable memory can be used at the programmer's convenience for data or program storage. It also does not require things like pre-erasing segments before a write. FRAM also offers advantages in security. It is inherently more secure due to its makeup, and de-layering is not effective. FRAM is also resistant to alpha radiation and SER effects. There are two main differences between FRAM and SRAM:

- FRAM is nonvolatile; that is, it retains contents on loss of power.
- The embedded FRAM on MSP430 devices can be accessed (read or write) at a maximum speed of 8 MHz

In comparison to MSP430 flash, FRAM:

- Is very easy to use
- Requires no setup or preparation such as unlocking of control registers
- Is not segmented and each bit is individually erasable, writable, and addressable
- Does not require an erase before a write
- Allows low-power write accesses (does not require a charge pump)
- Can be written to across the full voltage range (1.8 to 3.6 V)
- Can be written to at speeds close to 8MBps (maximum flash write speed including the erase time is approximately 14 kBps)
- Writing to FRAM does not require additional power when compared to reading from FRAM. The FRAM read current is included in the active mode current consumption numbers already.

Table 4 summarizes the FRAM advantage versus other memory technologies.

Table 4. FRAM Advantages

SPECIFICATION	FRAM	SRAM	FLASH
Write speed per word	125 ns	< 125 ns	85 µs
Erase time	No pre-erase required	No pre-erase required	23 ms for 512 bytes
Bitwise programmable	Yes	Yes	No
Write endurance	10^{15} write per erase cycle	N/A	10^{5} write per erase cycle
Nonvolatile	Yes	No	Yes
Internal write voltage	1.5 V	1.5 V	12 to 14 V (charge pump required)

4.1.1.1 MSP430FR5738 Features

- Embedded microcontroller
  - 16-bit RISC architecture up to 24-MHz clock
  - Wide supply voltage range (2 to 3.6 V)
  - –40°C to 85°C operation
- Optimized ultra-low-power modes
  - Active mode: 81.4 µA/MHz (typical)
  - Standby (LPM3 With VLO): 6.3 µA (typical)
  - Real-time clock (LPM3.5 with crystal): 1.5 µA (typical)
  - Shutdown (LPM4.5): 0.32 µA (typical)

- Ultra-low-power FRAM
  - Up to 16KB of nonvolatile memory
  - Ultra-low-power writes
  - Fast write at 125 ns per word (16KB in 1 ms)
  - Built-in error correction coding (ECC) and memory protection unit (MPU)
  - Universal memory = Program + data + storage
  - 10^{15} write cycle endurance
  - Radiation resistant and nonmagnetic
- Intelligent digital peripherals
  - 32-bit hardware multiplier (MPY)
  - 3-channel internal DMA
  - RTC with calendar and alarm functions
  - Five 16-bit timers with up to three capture/compare registers
  - 16-bit cyclic redundancy checker (CRC)
- High-performance analog
  - 16-channel analog comparator with voltage reference and programmable hysteresis
  - 14-channel 10-bit ADC with internal reference and sample and hold
    - 200 ksps at 100-µA consumption
- Enhanced serial communication
  - eUSCI_A0 and eUSCI_A1 support:
    - UART with automatic baud-rate detection
    - IrDA encode and decode
    - SPI at rates up to 10 Mbps
  - eUSCI_B0 supports:
    - I^2C with multiple slave addressing
    - SPI at rates up to 10 Mbps
  - Hardware UART bootstrap loader (BSL)
- Power management system
  - Fully integrated LDO
  - Supply voltage supervisor for core and supply voltages with reset capability
  - Always-on zero-power brownout detection
  - Serial onboard programming with no external voltage needed
- Flexible clock system
  - Fixed-frequency DCO with six selectable factory-trimmed frequencies (device dependent)
  - Low-power low-frequency internal clock source (VLO)
  - 32-kHz crystals (LFXT)
  - High-frequency crystals (HFXT)
- Development tools and software
  - Free professional development environment (Code Composer Studio™ IDE)
  - Low-cost full-featured kit (MSP-EXP430FR5739)
  - Full development kit (MSP-FET430U40A)
  - Target board (MSP-TS430RHA40A)

For complete module descriptions, see the MSP430FR57xx Family User's Guide (SLAU272).

4.1.2 SN65HVD101

The SN65HVD101 and SN65HVD102 IO-Link PHYs implement the IO-Link interface for industrial point-to-point communication. When the device is connected to an IO-Link master through a 3-wire interface, the master can initiate communication and exchange data with the remote node while the SN65HVD10X acts as a complete physical layer for the communication. The IO-Link driver output (CQ) can be used in push-pull, high-side, or low-side configurations using the EN and TX input pins. The PHY receiver converts the 24-V IO-LINK signal on the CQ pin to standard logic levels on the RX pin. A simple parallel interface receives and transmits data and status information between the PHY and the local controller. The SN65HVD101 and SN65HVD102 implement protection features for overcurrent, overvoltage, and over-temperature conditions. The IO-Link driver current limit can be set using an external resistor. If a short-circuit current fault occurs, the driver outputs are internally limited, and the PHY generates an error signal (SC). These devices also implement an over-temperature shutdown feature that protects the device from high-temperature faults. The SN65HVD102 operates from a single external 3.3-V or 5-V local supply. The SN65HVD101 integrates a linear regulator that generates either 3.3 V or 5 V from the IO-Link L+ voltage for supplying power to the PHY as well as a local controller and additional circuits. The SN65HVD101 and SN65HVD102 are available in the 20-pin RGB package (4-mm×3.5-mm QFN) for space-constrained applications.

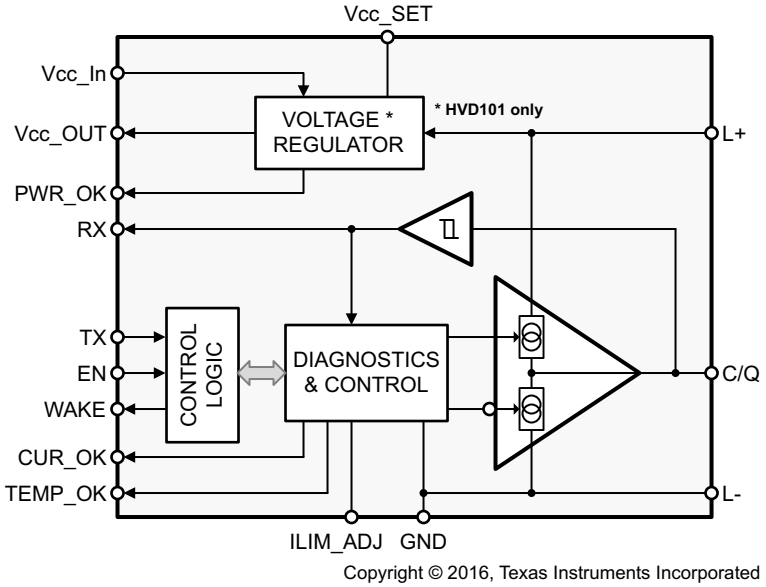


Figure 18. Functional Block Diagram SN65HVD101

4.1.2.1 SN65HVD101 Features

- Configurable CQ output: Push-pull, high-side, or low-side for SIO mode
- Remote wake-up indicator
- Current limit indicator
- Power Good indicator
- Over-temperature protection
- Reverse polarity protection
- Configurable current limits
- 9- to 36-V supply range
- Tolerant to 50-V peak line voltage
- 3.3-V or 5-V configurable integrated LDO (SN65HVD101 only)
- 20-pin QFN package: 4 mm × 3.5 mm

4.1.3 ADS1220

The ADS1220 is a precision, 24-bit ADC that offers many integrated features to reduce system cost and component count in applications measuring small sensor signals. The device features two differential or four single-ended inputs through a flexible input multiplexer (MUX), a low-noise, programmable gain amplifier (PGA), two programmable excitation current sources, a voltage reference, an oscillator, a low-side switch, and a precision temperature sensor. The device can perform conversions at data rates up to 2000 samples per second (SPS) with single-cycle settling. At 20 SPS, the digital filter offers simultaneous 50-Hz and 60-Hz rejection for noisy industrial applications. The internal PGA offers gains up to 128 V/V. This PGA makes the ADS1220 ideally suited for applications measuring small sensor signals such as resistance temperature detectors (RTDs), thermocouples, thermistors, and resistive bridge sensors. The device supports measurements of pseudo- or fully-differential signals when using the PGA. Alternatively, the device can be configured to bypass the internal PGA while still providing high-input impedance and gains up to 4 V/V, allowing for single-ended measurements.

Power consumption is as low as 120 µA when operating in duty-cycle mode with the PGA disabled. The ADS1220 is offered in a leadless VQFN-16 or a TSSOP-16 package and is specified over a temperature range of –40°C to 125°C.

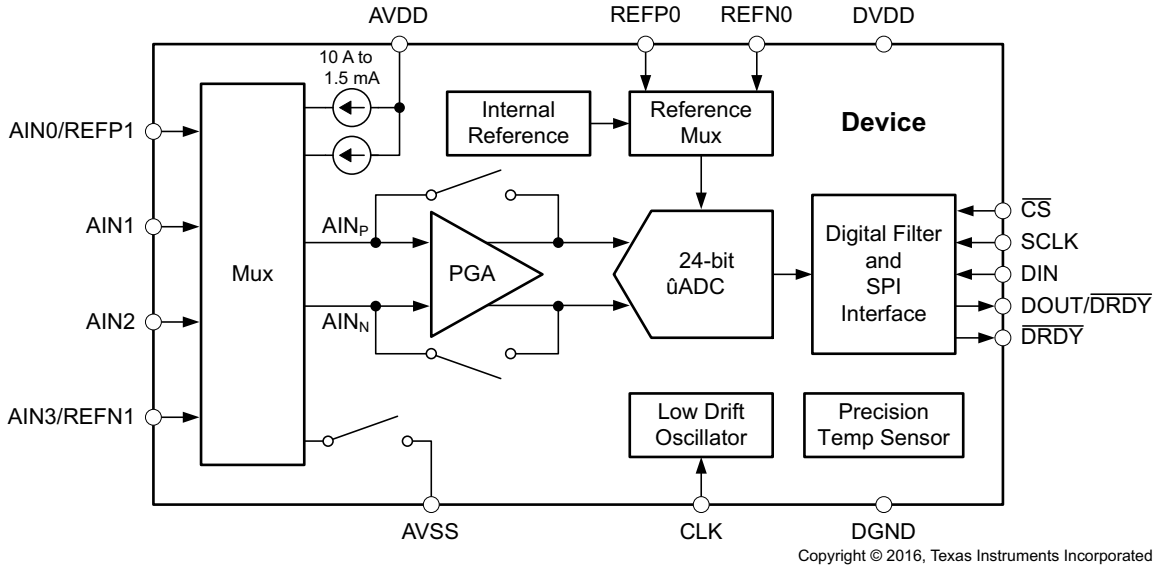


Figure 19. Functional Block Diagram ADS1220

4.1.3.1 ADS1220 Features

- Low current consumption: As Low as 120 µA (typ) in duty-cycle mode
- Wide supply range: 2.3 to 5.5 V
- Programmable gain: 1 to 128 V/V
- Programmable data rates: Up to 2 kSPS
- Up to 20-bit effective resolution
- Simultaneous 50-Hz and 60-Hz rejection at 20 SPS with single-cycle settling digital filter
- Two differential or four single-ended inputs
- Dual matched programmable current sources: 10 µA to 1.5 mA
- Internal 2.048-V reference: 5 ppm/°C (typ) drift
- Internal 2% accurate oscillator
- Internal temperature sensor: 0.5°C (typ) accuracy
- SPI™-compatible interface (Mode 1)
- Package: 3.5-mm×3.5-mm×0.9-mm VQFN

5 Getting Started Hardware

5.1 Headers and Jumpers Locations

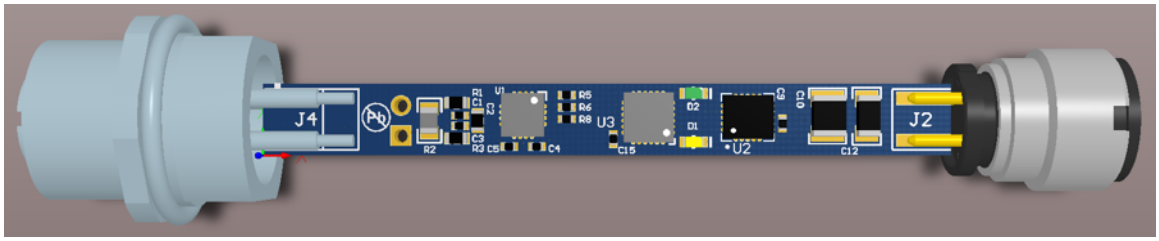


Figure 20. TIDA-00457 Board Front

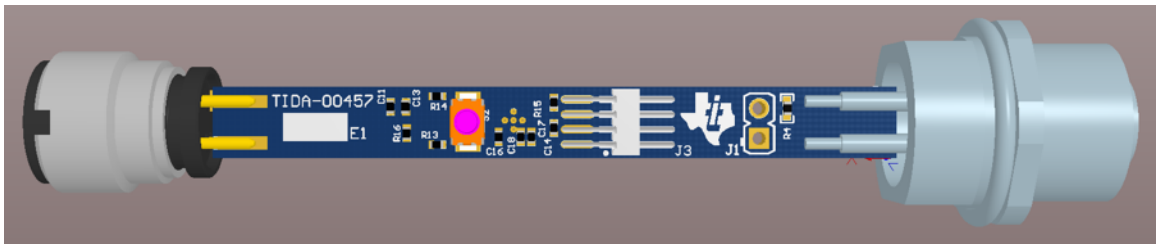


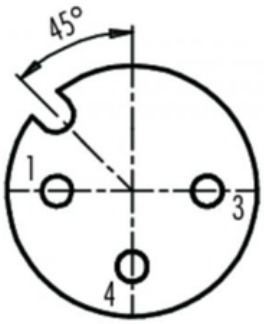
Figure 21. TIDA-00457 Board Back

Table 5 shows the different functions of the headers on the board.

Table 5. Header Functions

HEADER	DESCRIPTION
J1	Analog input test point
J2	IO-Link connector
J3	JTAG connector
J4	4- to 20-mA analog input port

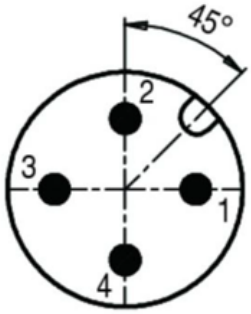
In addition to the analog input, this reference design has one extra digital input on pin 4 of connector J4. Figure 22 shows the pin assignment of connector J4.



PIN	FUNCTION
1	L+
2	AIN1
3	AIN0
4	IO_1

Figure 22. Pin Assignment of Connector J4

Figure 23 shows the pin assignment of the IO-Link connector J2.



PIN	FUNCTION
1	L+
2	Not connected
3	L–
4	C/Q

Figure 23. Pin Assignment of Connector J2

5.2 Powering the Board

The board is powered from the L+ line on the IO-link connector J2. The SN65HVD101 integrates a linear regulator that generates 3.3 V (VCC) from the IO-Link L+ voltage (9 to 30 V) for supplying power to the PHY as well as to the additional circuit on the board. The IO-Link L+ voltage is also used to power the sensor transmitter, which can be connected in 2- or 3-wire mode (see Section 3.1 for more details) on connector J4.

6 Getting Started Firmware

The demo software is a complete implementation according to IO-Link specification V1.1.2 and test specification V1.1. The IO-Link demo software supports data storage, block parameterization, and device access locks. The button on the board can be used to for teaching function. For more information on the IO-Link stack software contact TMG: http://www.tmgte.de/en/io-link-component/io-link-products-device-starter-kit-ti-tida-00339.html.

6.1 Software Update

For MSP430 Firmware updates, Code Composer Studio™ (CCS) is recommended. CCS is an integrated development environment (IDE) for Texas Instruments (TI) embedded processor families. CCS comprises a suite of tools used to develop and debug embedded applications. It includes compilers for each of TI's device families, source code editor, project build environment, debugger, profiler, simulators, real-time operating system, and many other features. The intuitive IDE provides a single user interface that goes through each step of the application development flow. For programming and debugging the MSP430FR5738 implements an embedded emulation module (EEM). It is accessed and controlled through either 4-wire JTAG mode or Spy-Bi-Wire™ mode. This TI Design only supports Spy-Bi-Wire mode. For more details on how the features of the EEM can be used together with CCS, see *Advanced Debugging Using the Enhanced Emulation Module* (SLAA393). The 2-wire interface is made up of the SBWTCK (Spy-Bi-Wire test clock) and SBWTDIO (Spy-Bi-Wire test data input/output) pins. The SBWTCK signal is the clock signal and is a dedicated pin. In normal operation, this pin is internally pulled to ground. The SBWTDIO signal represents the data and is a bidirectional connection. To reduce the overhead of the 2-wire interface, the SBWTDIO line is shared with the RST/NMI pin of the device. For programming and debugging purposes, the SBWTCK, SBWTDIO, VCC, and GND from the debugger needs to be connected on J3.

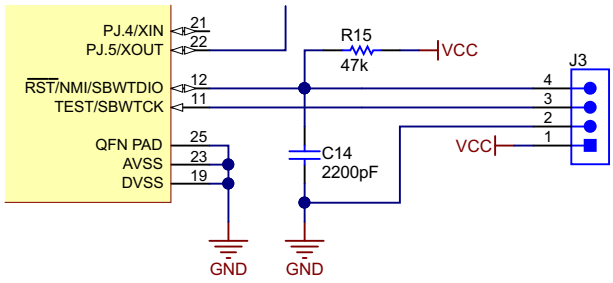


Figure 24. JTAG Connection

With the proper connections, an MSP430 debugger interface (such as the MSP-FET, http://www.ti.com/tool/msp-fet) can be used to program and debug code on this design.

6.2 Power During Debug

CAUTION

Take care during debug to avoid damages due to different power domain in conflicts (IO-Link power and debugger tools power). Read the following section carefully.

The SN65HVD101 integrates a linear voltage regulator that supplies 3.3 V to the IO-Link demo board if voltage from 9 to 30 V is supplied to L+. Normally, the MSP430FR5738 is powered from this 3.3-V supply.

If this local 3.3-V supply from the SN65HVD101 is used during debug, make sure the VCC_Target pin from the MSP-FET debugger interface is connected to VCC. If there is no local power and power from the debugger interface is used, make sure the VCC_Tool pin from the debugger interface is connected to VCC and disconnect the VCC_Target pin (see Figure 25).

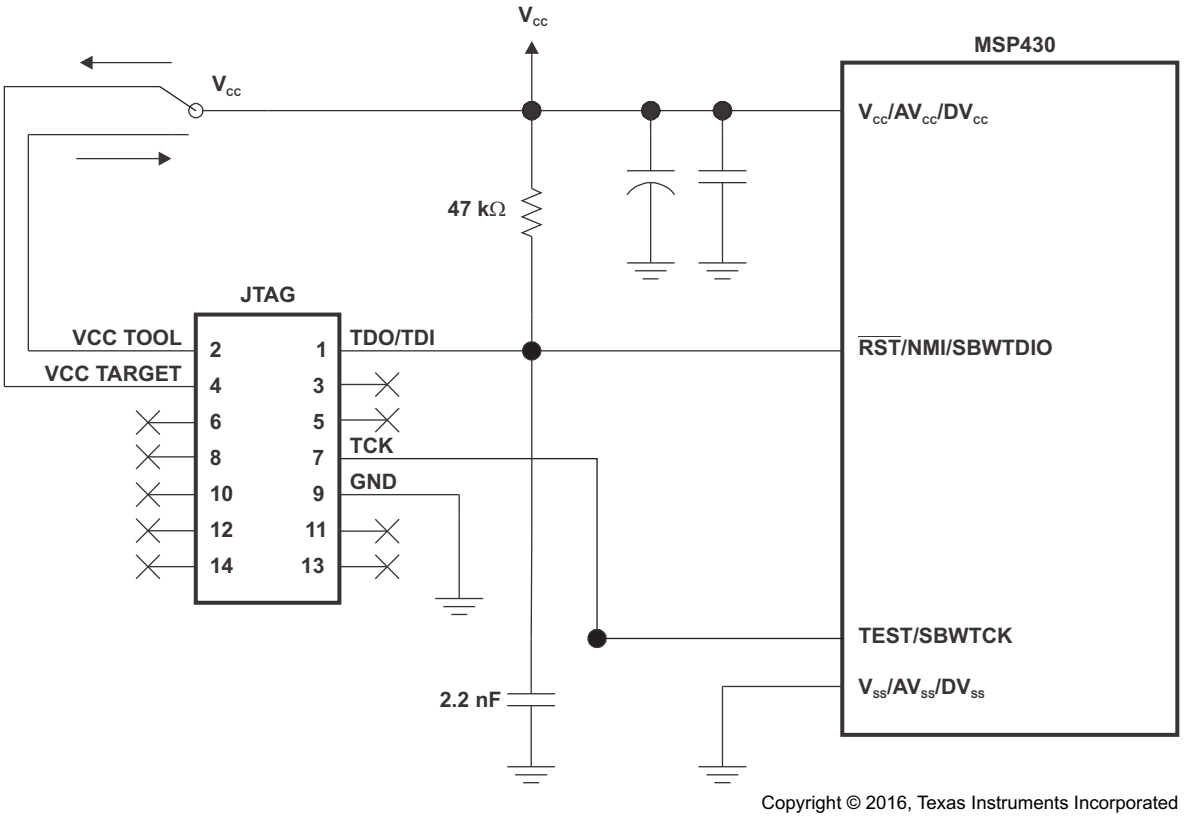


Figure 25. Signal Connections for 2-Wire JTAG Communication (Spy-Bi-Wire) – View From Debugger Interface

7 IO-Link Demonstrator

7.1 Hardware and Software Requirements

For the initial setup, the following hardware and software is required:

- TIDA-00457
- TIDA-00648 (or any other 4- to 20-mA sensor transmitter)
- USB IO-Link master (this design uses the TMG – USB IO-Link Master V2 SE)
  - GUI for USB IO-Link master (this design uses the TMG IO-LINK Device Tool V4.0)
- M12 cables
- USB cable

7.2 USB-IO-Link Master Software Installation

See the user manual of the USB IO-Link master in use for further details on its software installation and how to import the IODD folder. The following steps use the USB IO-Link Master V2 SE software from TMG (www.tmgte.com). The user manual is available after installing the software, which is delivered along with the hardware. The user manual describes the steps involved in importing the IODD files.

7.3 Getting Started

1. Connect the M12 cable (female) to the M12 connector J2 of the TIDA-00457.
2. Connect the other end of the M12 cable (male) to the M12 connector of the USB – IO-Link Master.
3. Connect the USB – IO-Link Master through a USB cable to the PC.
4. Launch the USB – IO-Link Master Software on the PC.
5. Follow the steps of the *IO-Link Master's User's Manual* to connect to the IO-Link Master and import the IODD.
6. After establishing the connection, the screen shown in Figure 26 is visible.
7. Connect any 4- to 20-mA sensor transmitter on connector J4 and read the data in the Process Data tab. In this IO-Link demo setup, the TIDA-00648 (4- to 20-mA Current Loop Transmitter Reference Design) has been used (see Figure 27).

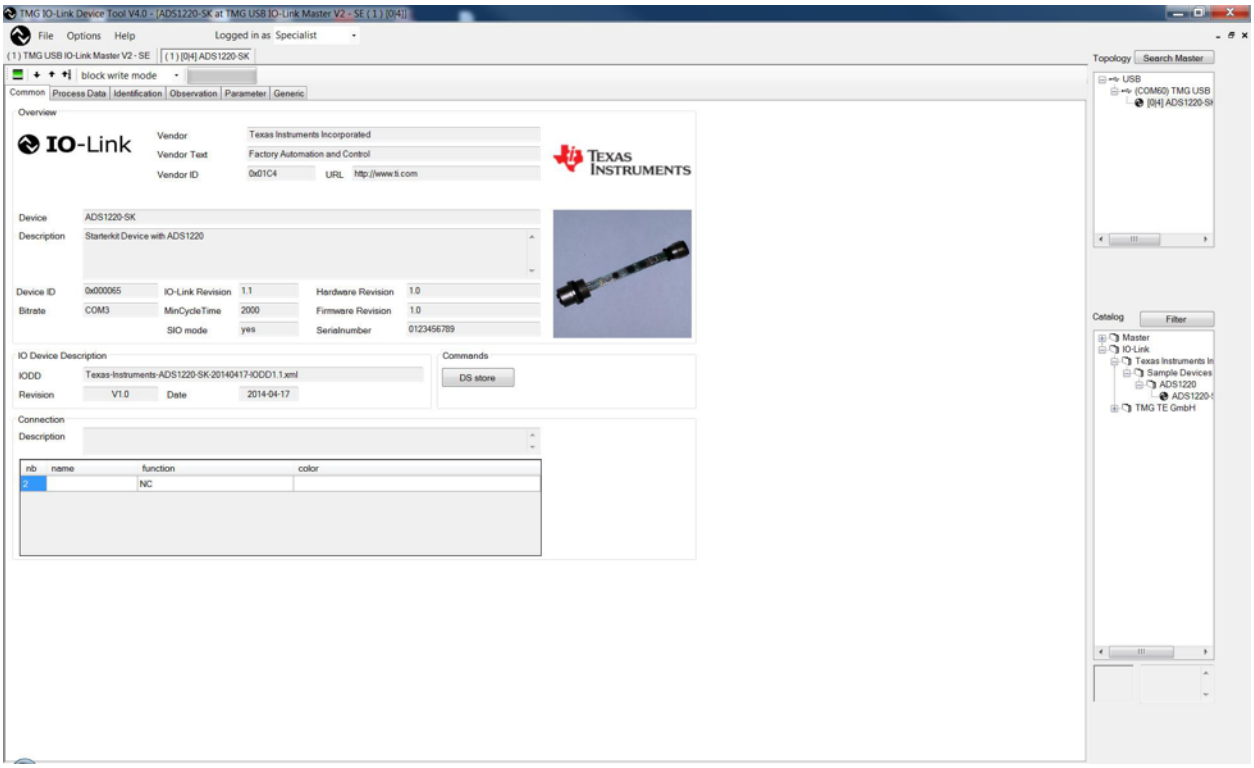


Figure 26. IO-Link Master GUI

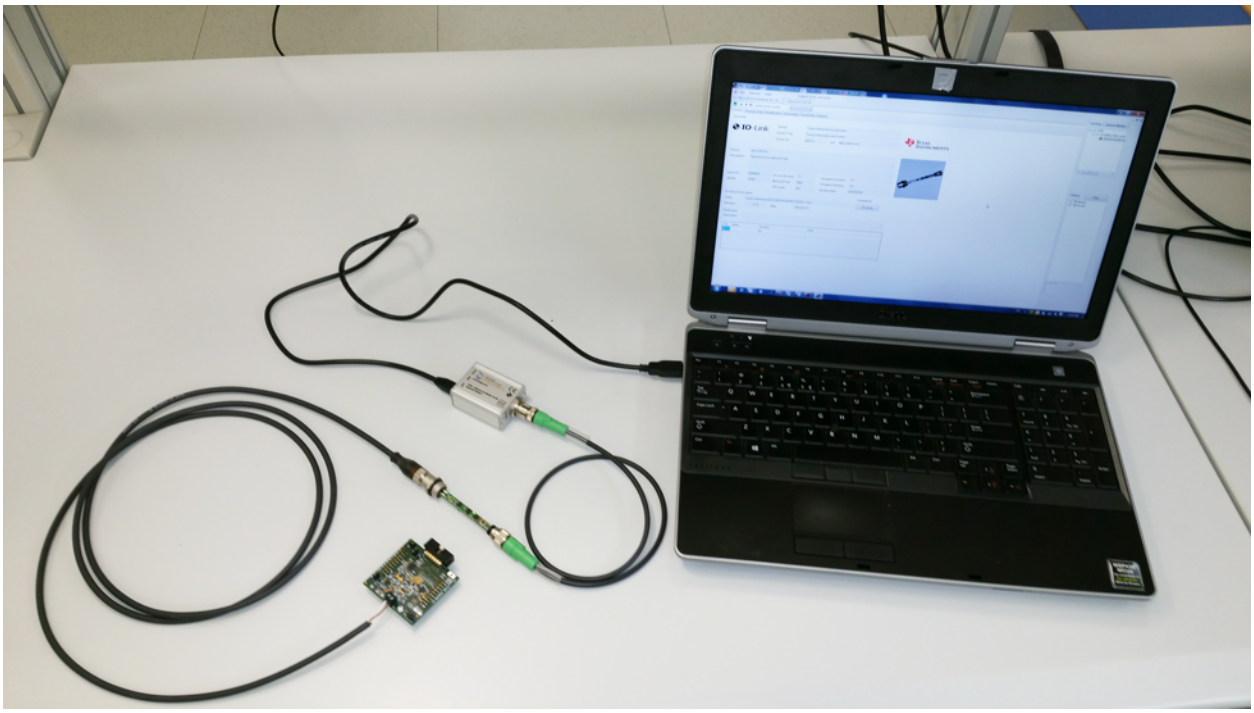


Figure 27. IO-Link Demo Setup

8 Analog 4- to 20-mA Input Test Setup

The test setup measures the analog performance of the 4- to 20-mA input. Figure 28 shows the test setup. For the analog 4- to 20-mA input test, a Keysight B2912A Precision Source / Measure Unit (SMU) has been used. The SMU has the capability to source and measure both voltage and current.

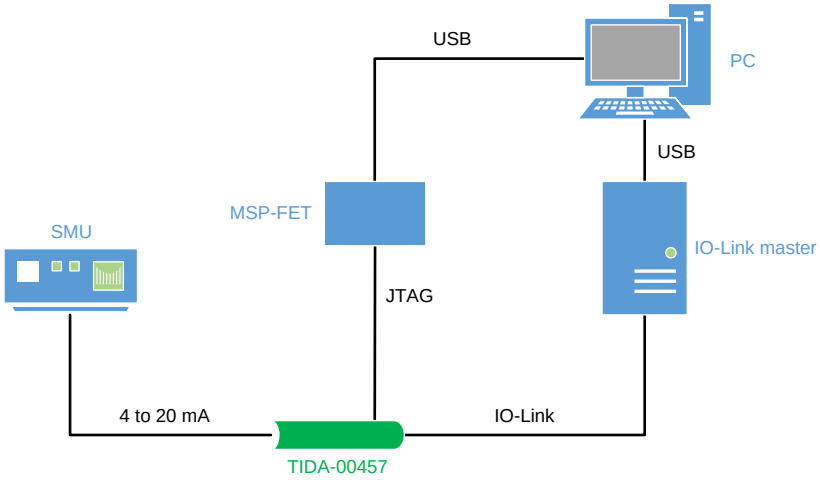


Figure 28. Analog 4- to 20-mA Test Setup

9 Test Data

NOTE: The test data in the following sections was measured with the system at room temperature unless otherwise noted.

The ADS1220 was configured for continuous-conversion mode at a 20-SPS data rate in the software. Then 1024 samples were recorded by the MSP430 MCU to generate the histogram plots shown in Figure 29 for the 4-mA input current and in Figure 30 for the 20-mA input current. The plotted raw ADC values are without any offset calibration or gain calibration. The recorded data were read out using the MSP-FET.

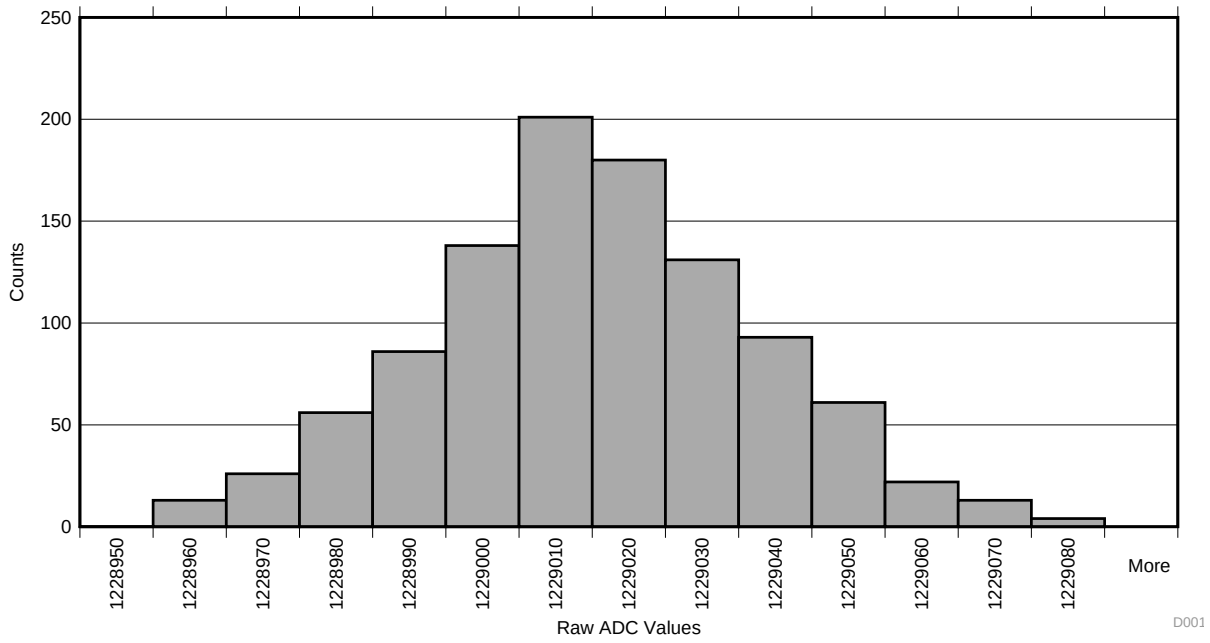


Figure 29. Raw ADC Code Distribution for 4-mA Input

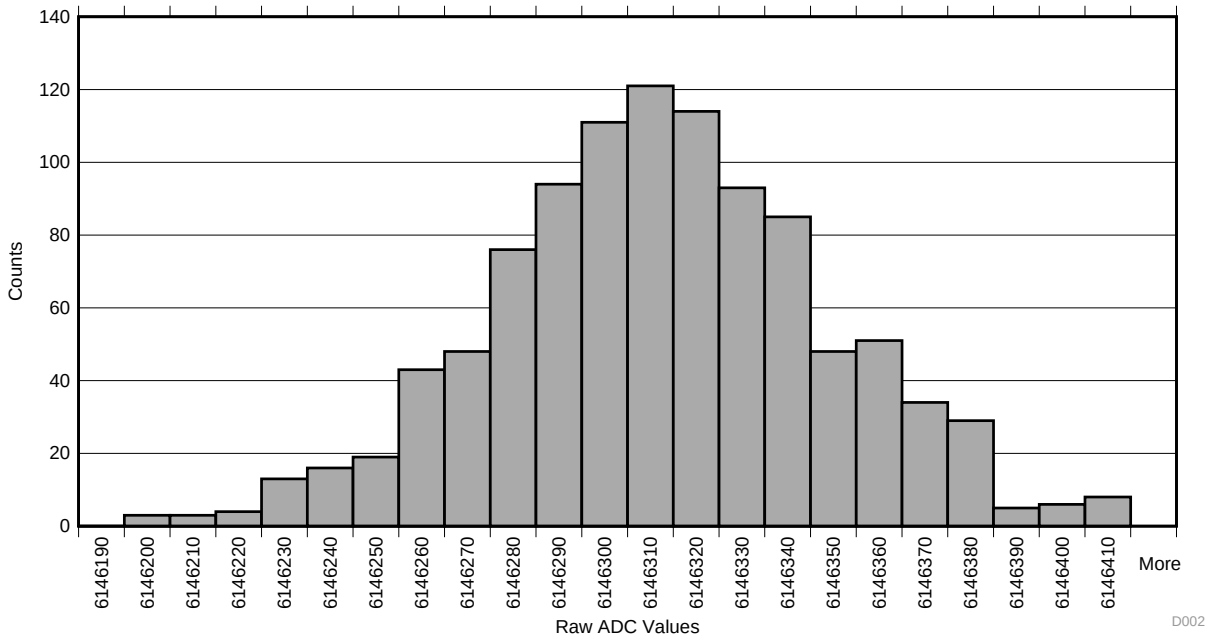


Figure 30. Raw ADC Code Distribution for 20-mA Input

The peak-to-peak spread of the codes in the histograms is around 120 codes for 4 mA and 210 codes for 20 mA. Equation 1 calculates the least-significant bit (LSB) size, which is then used to translate the peak-to-peak noise voltage as given by Equation 1 for 4 mA and Equation 1 for 20 mA.

$$1\ \text{LSB} = \frac{V_{ref}}{\left(2^{24}-1\right)\times R} = \frac{2048\ \text{mV}}{\left(2^{24}-1\right)\times 75\ \Omega} = 1.6\ \text{nA} \quad (1)$$

Input referred noise at 4 mA (pp) = [spread of RAW ADC codes × LSB] = 120 × 1.6 nA = 0.19 µA
Input referred noise at 20 mA (pp) = [spread of RAW ADC codes × LSB] = 210 × 1.6 nA = 0.34 µA

The noise can be further reduced by implementing additional averaging or filtering in the software.

10 Design Files

10.1 Schematics

To download the schematics, see the design files at TIDA-00457.

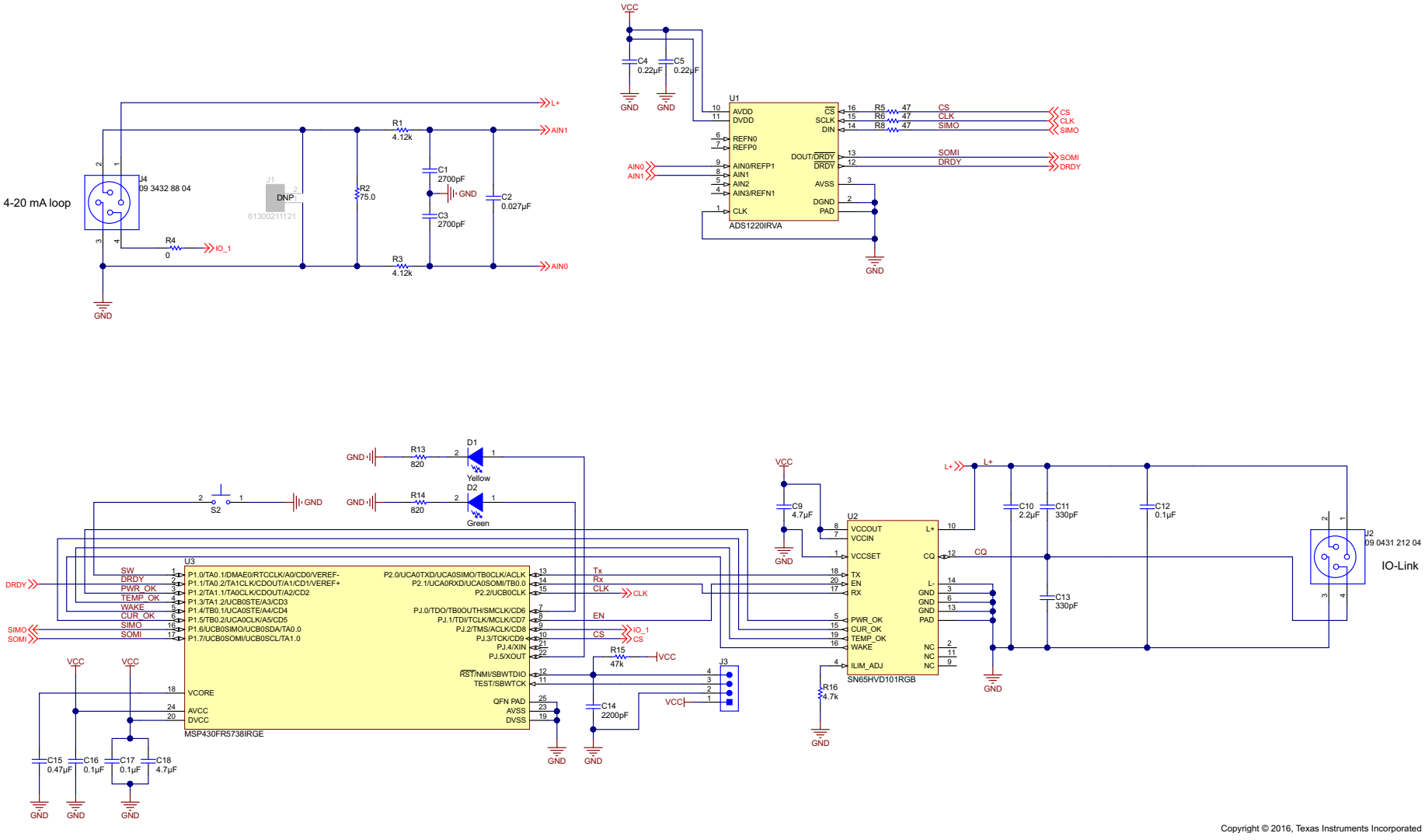


Figure 31. TIDA-00457 Schematics

10.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00457.

Table 6. BOM

ITEM	DESIGNATOR	QTY	VALUE	PARTNUMBER	MANUFACTURER	DESCRIPTION	PACKAGE REFERENCE
1	!PCB1	1		TIDA-00457	Any	Printed Circuit Board	
2	C1, C3	2	2700pF	GRM155R72A272KA01D	MuRata	CAP, CERM, 2700pF, 100V, +/-10%, X7R, 0402	402
3	C2	1	0.027uF	C0603C273K1RACTU	Kemet	CAP, CERM, 0.027uF, 100V, +/-10%, X7R, 0603	603
4	C4, C5	2	0.22uF	GRM155R60J224KE01D	MuRata	CAP, CERM, 0.22uF, 6.3V, +/-10%, X5R, 0402	402
5	C9, C18	2	4.7uF	C1005X5R0J475M050BC	TDK	CAP, CERM, 4.7uF, 6.3V, +/-20%, X5R, 0402	402
6	C10	1	2.2uF	GRM32ER72A225KA35L	MuRata	CAP, CERM, 2.2uF, 100V, +/-10%, X7R, 1210	1210
7	C11, C13	2	330pF	GRM155R72A331KA01D	MuRata	CAP, CERM, 330pF, 100V, +/-10%, X7R, 0402	402
8	C12	1	0.1uF	12061C104JAT2A	AVX	CAP, CERM, 0.1uF, 100V, +/-5%, X7R, 1206	1206
9	C14	1	2200pF	GRM155R70J222KA01D	MuRata	CAP, CERM, 2200pF, 6.3V, +/-10%, X7R, 0402	402
10	C15	1	0.47uF	GRM155R60J474KE19D	MuRata	CAP, CERM, 0.47uF, 6.3V, +/-10%, X5R, 0402	402
11	C16, C17	2	0.1uF	C1005X5R0J104K	TDK	CAP, CERM, 0.1uF, 6.3V, +/-10%, X5R, 0402	402
12	D1	1	Yellow	LY L29K-J1K2-26-Z	OSRAM	LED, Yellow, SMD	LED, 1.3x0.65x0.8mm
13	D2	1	Green	LG L29K-G2J1-24-Z	OSRAM	LED, Green, SMD	1.7x0.65x0.8mm
14	J2	1		09 0431 212 04	Binder-Connector	M12 Socket, 4Pos, TH	M12 Conn D12x14.3
15	J3	1		850-10-004-40-001000	Mill-Max	Header, 4x1, 50mil, R/A, SMT	Header, 50mil, R/A,SMT
16	J4	1		09 3432 88 04	Binder-Connector	M12-A Socket, 4Pos, TH	M12-A Socket, 4Pos, TH
17	R1, R3	2	4.12k	RG1608P-4121-B-T5	Susumu Co Ltd	RES, 4.12k ohm, 0.1%, 0.1W, 0603	603
18	R2	1	75	RN73C2A75RBTDF	TE Connectivity	RES, 75.0, 0.1%, 0.1 W, 0805	805
19	R4	1	0	CRCW04020000Z0ED	Vishay-Dale	RES, 0 ohm, 5%, 0.063W, 0402	402

Table 6. BOM (continued)

ITEM	DESIGNATOR	QTY	VALUE	PARTNUMBER	MANUFACTURER	DESCRIPTION	PACKAGE REFERENCE
20	R5, R6, R8	3	47	CRCW040247R0JNED	Vishay-Dale	RES, 47 ohm, 5%, 0.063W, 0402	402
21	R13, R14	2	820	CRCW0402820RJNED	Vishay-Dale	RES, 820 ohm, 5%, 0.063W, 0402	402
22	R15	1	47k	CRCW040247K0JNED	Vishay-Dale	RES, 47k ohm, 5%, 0.063W, 0402	402
23	R16	1	4.7k	CRCW04024K70JNED	Vishay-Dale	RES, 4.7k ohm, 5%, 0.063W, 0402	402
24	S2	1		SKRKAEE010	Alps	Switch, Push Button, SMD	2.9x2x3.9mm SMD
25	U1	1		ADS1220IRVA	Texas Instruments	Low-Power, Low-Noise, 24-Bit Analog-to-Digital Converter for Small Signal Sensors, RVA0016A	RVA0016A
26	U2	1		SN65HVD101RGB	Texas Instruments	IO-LINK PHY for Device Nodes, RGB0020A	RGB0020A
27	U3	1		MSP430FR5738IRGE	Texas Instruments	24 MHz Mixed Signal Microcontroller, 1024 B SRAM and 17 GPIOs, -40 to 85 degC, RGE0024G	RGE0024G
28	J1	0		61300211121	Wurth Elektronik	Header, 2.54 mm, 2x1, Gold, TH	Header, 2.54mm, 2x1, TH

10.3 Layout Prints

To download the layer plots, see the design files at TIDA-00457.

10.4 Altium Project

To download the Altium project files, see the design files at TIDA-00457.

10.5 Gerber Files

To download the Gerber files, see the design files at TIDA-00457.

10.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-00457.

11 Software Files

To download the software files, see the design files at TIDA-00457.

12 References

1. Texas Instruments, *MSP430FR573x Mixed Signal Microcontrollers*, MSP430FR5738 Datasheet (SLAS639)
2. Texas Instruments, *SN65HVD10x IO-Link PHY for Device Nodes*, SN65HVD101 Datasheet (SLLSE84)
3. Texas Instruments, *Low-Power, Low-Noise, 24-Bit, Analog-to-Digital Converter for Small-Signal Sensors*, ADS1220 Datasheet (SBAS501)
4. Texas Instruments, *Advanced Debugging Using the Enhanced Emulation Module (EEM) With Code Composer Studio Version 6*, EEM Application Report (SLAA393)
5. IO-Link, *IO-Link Interface and System Specification v1.1.2* (PDF)
6. IO-Link, *IO-Link Test Specification v1.1*, (PDF)
7. NAMUR, *NAMUR NE 043:2003 Standardization of the Signal Level for the Failure Information of Digital Transmitters* (Worksheets)

Revision A History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (April 2016) to A Revision	Page
• Changed from preview page	1

IMPORTANT NOTICE FOR TI REFERENCE DESIGNS

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