TI Designs

10.8-V/250-W, 97% Efficient, Compact Brushless DC Motor Drive With Stall Current Limit Reference Design

TI Designs

The TIDA-00771 is a 20-A_{RMS} drive for a three-phase brushless DC (BLDC) motor in power tools operating from a 3-cell Li-ion battery with a voltage range of 5 to 12.6 V. The design is a 45-mm×50-mm compact drive, implementing sensor-based trapezoidal control. The design uses a discrete compact MOSFET-based three-phase inverter that delivers 20-A_{RMS} continuous (70-A peak for 1 second) winding current without any external cooling or heat sink. The slew rate control and triple charge pump of the gate drive ensures maximum inverter efficiency over 5 to 12.6 V and optimum EMI performance. The cycle-by-cycle overcurrent protection feature protects the power stage from large stall currents and the board can work up to 55°C ambient.

Design Resources

TIDA-00771	Design Folder
CSD17576Q5B	Product Folder
DRV8305	Product Folder
MSP430G2553	Product Folder
SN74LVC126A	Product Folder
LMT87	Product Folder
TPD1E10B06	Product Folder
DRV5013	Product Folder

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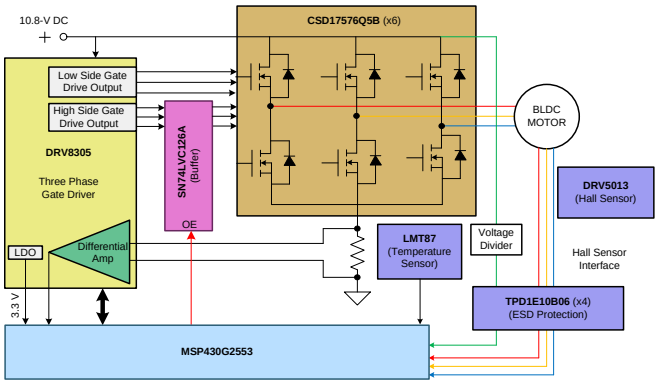
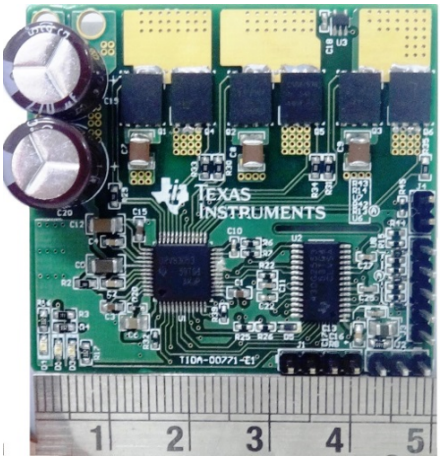
Design Features

- 250-W Drive for BLDC Motor Supporting Sensor-Based Trapezoidal Control
- Designed to Operate From 3-Cell Li-ion Battery Voltage Ranging From 5 to 12.6 V
- Delivers up to 20-A_{RMS} Continuous Motor Current Without Heat Sink or Airflow
- 70-A Peak Current Capability for 1 Second
- Small PCB Form Factor of 45 mm × 50 mm Using 30-V/400-A_{PEAK},1.7-mΩ R_{DS_ON}, SON5x6 Package MOSFETs
- Optimum Inverter Efficiency and EMI Performance Using the Slew Rate Control of Gate Driver
- Three-Phase Gate Driver With Internal Charge Pump Ensures Maximum Inverter Efficiency Even at 5-V DC
- Cycle-by-Cycle Overcurrent and Motor Stall Current Non-Latching Limit
- Short Circuit Latch Protection by V_{DS} Sensing
- Shoot-Through, Undervoltage, Overtemperature, and Blocked Rotor Protection
- Operating Ambient: –20°C to 55°C

Featured Applications

- Power Tools
- Garden Tools
- Mower Robots
- Vacuum Cleaning Robots





1 Key System Specifications

Table 1. Key System Specifications

PARAMETERS	SPECIFICATIONS
Input voltage	10.8-V DC (4.5 -V min to 12.6-V max) — 2- or 3-cell Li-ion
Rated input power	250 W
RMS winding current	20 A
Peak winding current	70 A (for 1 second)
Control method	Sensor-based trapezoidal
Inverter switching frequency	20 kHz (adjustable from 5k to 100k)
Motor electrical frequency	300 Hz max (for example, a motor with 9000 RPM and 4 poles)
Feedback signals	DC bus voltage, Hall sensor, low-side DC bus current
Protections	Cycle-by-cycle overcurrent, input undervoltage, over temperature, and blocked rotor
Cooling	Natural cooling only, no heat sink
Operating ambient	–20°C to 55°C
Board specification	45 mm × 50 mm, 4-layer, 2-oz copper
Efficiency	> 97%

2 System Description

Power tools are used in various industrial and household applications such as drilling, grinding, cutting, polishing, driving fasteners, various garden tools, and so on. The most common types of power tools use electric motors while some use internal combustion engines, steam engines, or compressed air. Power tools can be either corded or cordless (battery powered). Corded power tools use the mains power (the grid power) to power up the AC or DC motors. The cordless tools use battery power to drive DC motors.

Most of the cordless tools use lithium-ion batteries, the most advanced in the industry. Lithium-ion batteries have high energy density, low weight, and greater life. These batteries have relatively low self-discharge (less than half that of nickel-based batteries) and can provide a very high current for applications like power tools.

Cordless tools use brushed or BLDC motors. The brushless motors are more efficient and have less maintenance, low noise, and longer life. Power tools have requirements on form factor and thermal performance. Therefore, high-efficient power stages with a compact size are required to drive the power tool motor. The small form factor of the power stage enables flexible mounting, better PCB layout performance, and low cost design. High efficiency provides maximum battery duration and reduces cooling efforts. The high-efficiency requirement in turn asks for switching devices with a low drain-to-source resistance (R_{DS_ON}). The power stage should also take care of protections like motor stall or any other chances of high current.

The design uses CSD17576Q5B NexFETs featuring a very low R_{DS_ON} of 1.7 mΩ in a SON5x6 SMD package, which results in a very small form factor of 45 mm × 50 mm. The three-phase gate-driver DRV8305 is used to drive the three-phase MOSFET bridge, which can operate from 4.5 to 45 V and support programmable gate current with maximum setting of 1.25-A sink / 1-A source. The DRV8305 includes three current shunt amplifiers for accurate current measurements that support bi-directional current sensing with adjustable gain. The DRV8305 has an integrated voltage regulator and controller to support a MCU or additional system power needs. The SPI provides detailed fault reporting and flexible parameter settings such as gain options for the current shunt amplifier, slew rate control of the gate drivers, and various protection features.

The MSP430G2553 microcontroller is used to implement the control algorithm. The CBC overcurrent protection uses the internal comparator of the MSP430G2553 and external buffer.

The test report evaluates the RMS current capability, peak current capability, and thermal performance of the board and overcurrent protection features such as cycle-by-cycle control and latch control of the DRV8305. The test results also show the improved RMS current capability of the board with different air flow.

3 System Design Theory

Compared to their brushed motor counterpart, permanent magnet brushless motors are gaining importance because of their high efficiency, high torque to weight ratio, low maintenance, high reliability, low rotor inertia, low noise, and so on. A brushless permanent magnet synchronous motor (PMSM) has a wound stator and a permanent magnet rotor assembly. These motors generally use internal or external devices to sense rotor position. The sensing devices provide position information for electronically switching the stator windings in the proper sequence to maintain rotation of the magnet assembly.

The electronic drive is required to control the stator currents in a brushless permanent magnet motor. The electronic drive consists of:

- Power stage with a three-phase inverter having the required power capability
- MCU to implement the motor control algorithm
- Position sensor for accurate motor current commutation
- Gate driver for driving the three-phase inverter
- Power supply to power up the MCU

3.1 Brushless Permanent Magnet Motors

Permanent magnet motors can be classified based on Back-EMF (BEMF) profiles: a BLDC motor and a PMSM. Both BLDC motors and PMSMs have permanent magnets on the rotor but differ in the flux distributions and BEMF profiles. In a BLDC motor, the BEMF induced in the stator is trapezoidal, and in a PMSM, the BEMF induced in the stator is sinusoidal. Implementing an appropriate control strategy is required to obtain the maximum performance from each type of motor.

The BLDC motor or the trapezoidal BEMF motor has the ampere conductor distribution of the stator, which ideally remains constant and fixed in space for a fixed interval known as the commutation interval. For a three-phase winding, the commutation interval is 60° electrical. At the end of each commutation interval, the ampere conductors are commutated to the next position. These motors use a two-phase ON control, where two phases of the motor will be energized at a time and the third winding will be open. The principle of the BLDC motor is, at all times, to energize the phase pair, which can produce the highest torque. The combination of a direct current with a trapezoidal BEMF makes it theoretically possible to produce a constant torque. In practice, the current cannot be established instantaneously in a motor phase as a consequence the torque ripple is present at each 60° phase commutation. Figure 1 describes the electrical waveforms in the BLDC motor in the two phases ON operation.

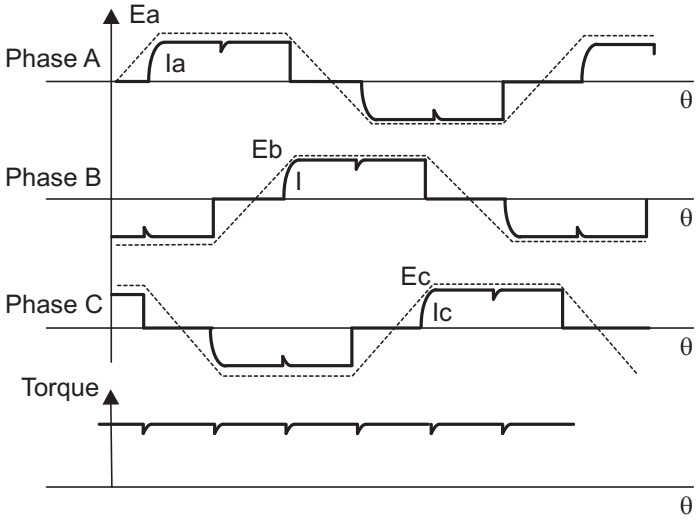


Figure 1. Electrical Waveforms in Two-Phase ON Control of BLDC Motor and Torque Ripple

A trapezoidal control has the following advantages:

- Only one current at a time needs to be controlled.
- Only one current sensor is necessary (or none for speed loop only).
- The positioning of the current sensor allows the use of low cost sensors as a shunt.

For more details about trapezoidal control, see the application report *Sensorless Trapezoidal Control of BLDC Motors* (SPRABQ7).

3.2 Power Stage Design—Battery Power Input to Board

The battery power input section is shown in Figure 2. The input bulk aluminum electrolytic capacitors C19 and C20 provide the ripple current and its voltage rating is de-rated by 50% for better life. These capacitors are rated to carry high ripple current. C21 and C24 are used as bypass capacitors to GND. D2 is the transient voltage suppression (TVS) having breakdown voltage of 30 V and maximum supply voltage of 30 V.

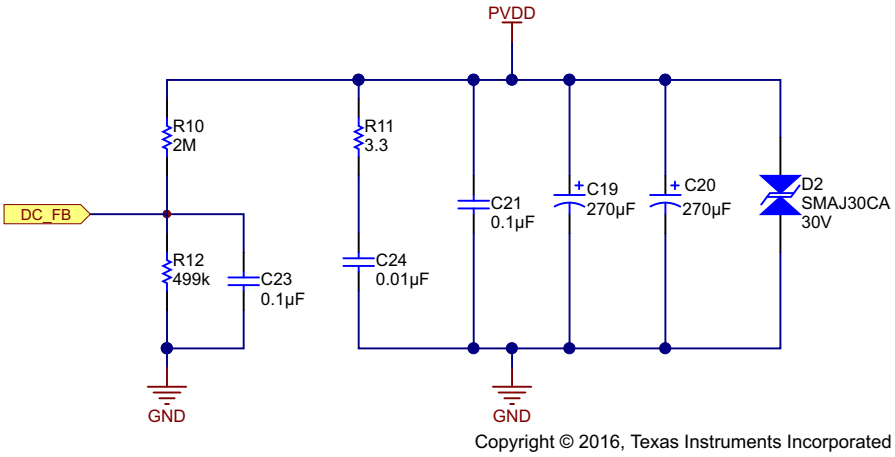


Figure 2. Schematic of Battery Power Input Section

The input supply voltage PVDD is scaled using the resistive divider network, which consists of R10, R12, and C23, and fed to the MCU. Considering the maximum voltage for the MCU ADC input as 3.3 V, the maximum DC input voltage measurable by the MCU is calculated as in Equation 1.

$$V_{DC}^{max} = V_{ADC\_DC}^{max} \times \frac{(499\ k\Omega + 2000\ k\Omega)}{499\ k\Omega} = 3.3 \times \frac{(499\ k\Omega + 2000\ k\Omega)}{499\ k\Omega} = 16.5\ V \quad (1)$$

Considering a 20% headroom for this value, the maximum recommended voltage input to the system is 16.5 × 0.8 = 13.2. So for a power stage with maximum operating voltage of 12.6 V, this voltage feedback resistor divider is ideal. Also, this choice gives optimal ADC resolution for a system operating from 5 to 12.6 V.

3.3 Power Stage Design—Three-Phase Inverter

The three-phase inverter circuit shown in Figure 3 consists of a three-leg MOSFET bridge. The DC bus current is measured using the current sensor resistors R5 and R18 mounted on the DC bus return path. The sensed currents are fed to the MCU through the current shunt amplifiers. C7, C8, and C9 are the decoupling capacitors connected across each inverter leg.

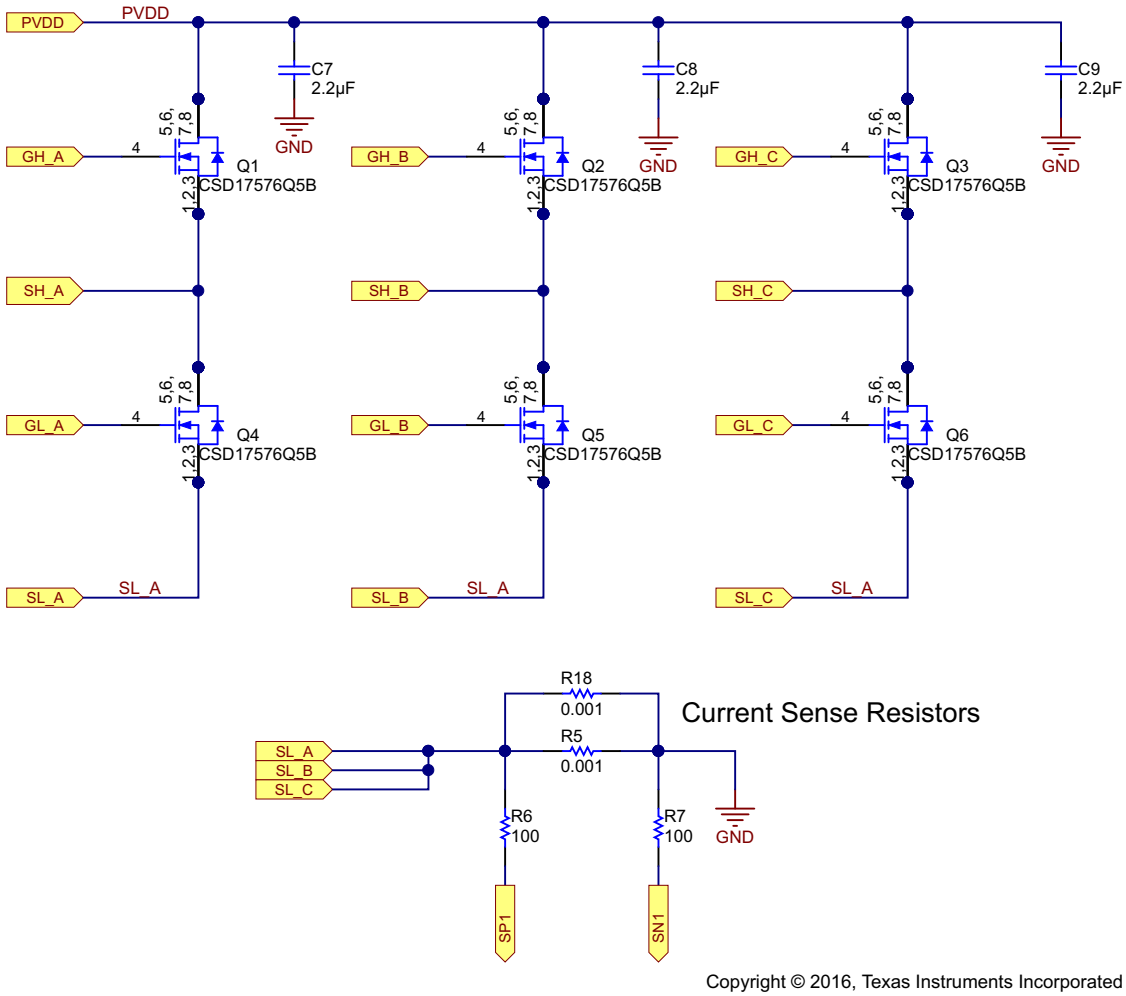


Figure 3. Schematic of Three-Phase MOSFET Inverter and Current Sense Resistors

NOTE: Connect the decoupling capacitors very near to the corresponding MOSFET legs for better decoupling (see Section 9.3). An improper layout or position of the decoupling capacitors can cause undesired V_{DS} switching voltage spikes.

3.3.1 Selecting MOSFET

The board is designed to operate from a 3-cell Li-Ion battery voltage ranging from 5 to 12.6 V, meaning the maximum input DC voltage in the application is 12.6 V. Considering the safety factor and switching spikes, a MOSFET with voltage rating greater than or equal to 30 V is suitable for this application.

The current rating of the MOSFET depends on the peak winding current. The power stage has to provide a 20-A_{RMS} nominal continuous current to the motor winding and 70-A peak current for 1 second. Considering the peak current capability with a 20% margin, a MOSFET with a 100-A continuous rating can be selected. The package size of the MOSFET must be very small to design a very small form factor PCB.

For better thermal performance, select the MOSFETs with very low R_{DS_ON}. In the reference design, the MOSFET CSD17576Q5B is selected, which is a 30-V N-channel NexFET power MOSFET with a very low R_{DS_ON} of 1.7 mΩ and requires very low total gate charge. It has a continuous drain current capacity (package limited) of 100 A and a peak current capacity of 400 A. The MOSFET is available at a very small package size of 5 mm × 6 mm.

3.3.2 Selecting Sense Resistor

Power dissipation in sense resistors and the input offset error voltage of the op amps are important in selecting the sense resistance values. The sense resistors are carrying a total nominal RMS current of 20 A with a peak current of 70 A for 1 second. A high sense resistance value increases the power loss in the resistors. The internal current shunt amplifiers of the DRV8305 have a DC input offset of 4 mV. The DRV8305 has the DC offset voltage calibration feature. In case the amplifier is used without offset calibration, it is required to select the sense resistor such that the sense voltage across the resistor is sufficiently higher than the offset error voltage to reduce the effect of the offset error.

Selecting a 0.5-mΩ resistor as the sense resistor, the power loss in the resistor at 30-A_{RMS} is given by Equation 2:

$$\text{Power loss in the resisitor} = I_{RMS}^2 \times R_{RENSE} = 20^2 \times 0.0005 = 0.2 \text{ W} \quad (2)$$

At 70-A peak current, using Equation 2, the power loss in the resistor = 2.45 W (for 1 second). In this reference design, two 1-mΩ, 3-W resistors are used in parallel.

3.4 Power Stage Design—DRV8305 Gate Driver

Figure 4 shows the schematic of the DRV8305 gate driver. C1 and C3 are the AVDD and DVDD decoupling capacitors, which must be placed close to the IC. PVDD is the DC supply input; in this case, it is the battery voltage of 10.8 V. A 4.7-µF capacitor (C5) is used as the PVDD capacitor. C12 and C15 are charge pump capacitors for the low-side and high-gate driver, respectively. The EN_GATE of DRV8305 is connected to the MCU and the same is pulled down by R32. This helps the MCU to enable or disable the gate drive outputs of the DRV8305. C2 and C4 are the flying capacitors for charge pumps. For the voltage rating selection of these capacitors, see the DRV8305 datasheet (SLVSCX2). The WAKE pin of the DRV8305 is tied to 3.3 V. To control the wake through the MCU, connect the pin to any digital I/O of the MCU.

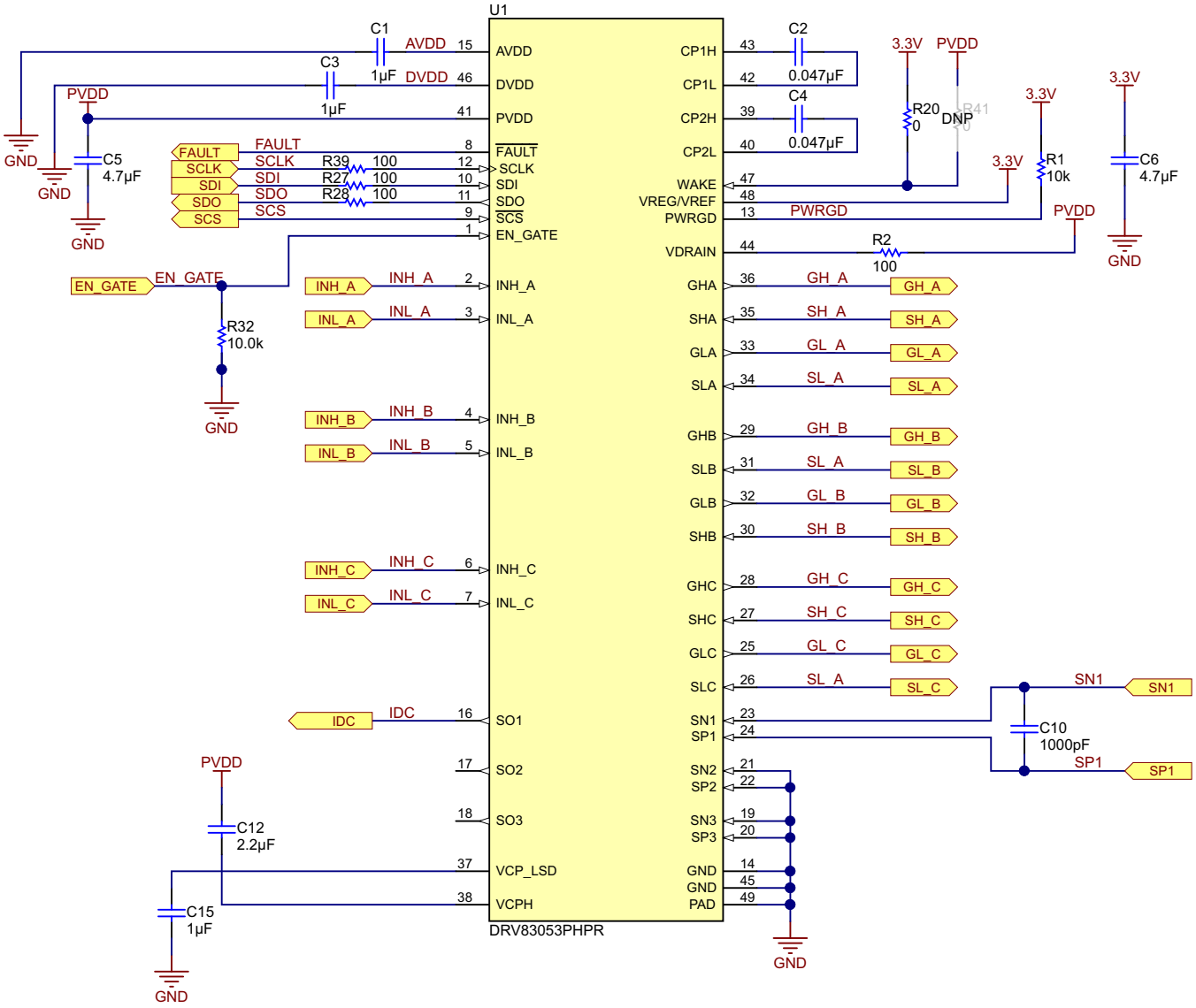


Figure 4. Schematic of DRV8305 Gate Driver

3.4.1 Gate Drive Features of DRV8305

The DRV8305 gate driver uses a complimentary push-pull topology for both the high-side and the low-side gate drivers. Both the high side (GHx to SHx) and the low side (GLx to SLx) are implemented as floating gate drivers to tolerate switching transients from the half-bridges.

3.4.1.1 IDRIVE—Gate Driver Output Current

The first component of the gate drive architecture implements adjustable current control for the gates of the external power MOSFETs. This feature allows the gate driver to control the V_{DS} slew rate of the MOSFETs by adjusting the gate drive current. The DRV8305 provides 12 adjustable source and sink current levels for the high-side (the high sides of all three phases share the same setting) and low-side gate drivers (the low sides of all three phases share the same settings). The gate drive levels are adjustable through the SPI registers in both the standby and operating states. This flexibility allows the system designer to tune the performance of the driver for different operating conditions through software alone.

The current source architecture helps eliminate the temperature, process, and load-dependent variations associated with internal and external series limiting resistors. Beyond that, internal switches are adjusted to create the desired settings up to the 1.25-A (sink) or 1-A (source) settings.

Control of the gate current during the MOSFET Miller region is a key component for adjusting the MOSFET V_{DS} rise and fall times. MOSFET V_{DS} slew rates are a critical parameter for optimizing emitted radiations, energy and duration of diode recovery spikes, dV/dt related turnon leading to shoot-through, and voltage transients related to parasitics.

3.4.1.2 TDRIVE—Gate Driver State Machine

The DRV8305 gate driver uses an integrated state machine (TDRIVE) in the gate driver to protect against excessive current on the gate drive outputs, shoot-through in the external MOSFET, and dV/dt turnon due to switching on the phase nodes. The TDRIVE state machine allows for the design a robust and efficient motor drive system with minimal overhead.

The state machine incorporates internal handshaking when switching from the low-side to the high-side external MOSFET or vice-versa. The handshaking is designed to prevent the external MOSFETs from entering a period of cross conduction, also known as shoot-through. The internal handshaking uses the V_{GS} monitors of theDRV8305 to determine when one MOSFET has been disabled and the other can be enabled. This allows the gate driver to insert an optimized dead time into the system without the risk of cross conduction. Any dead time added externally through the MCU or SPI register will be inserted after the handshake process.

The state machine also incorporates a gate drive timer to ensure that under abnormal circumstances such as a short on the MOSFET gate or the inadvertent turnon of a MOSFET V_{GS} clamp, the high peak current through the DRV8305 and MOSFET is limited to a fixed duration.

Select a t_{DRIVE} time that is longer than the time needed to charge or discharge the gate capacitances of the external MOSFETs. The TDRIVE SPI registers must be configured so the MOSFET gates are charged completely within t_{DRIVE} during normal operation. If t_{DRIVE} is too low for a given MOSFET, then the MOSFET may not turn on completely. Tune these values in-system with the required external MOSFETs to determine the best possible setting for the application. A good starting value is a t_{DRIVE} period that is 2x the expected rise or fall times of the external MOSFET gates. Note that TDRIVE does not increase the PWM time and simply terminates if a PWM command is received while it is active.

VCPH Charge Pump—High-Side Gate Supply

The DRV8305 uses a charge pump to generate the proper gate to source voltage bias for the high-side N-channel MOSFETs. Similar to the often used bootstrap architecture, the charge pump generates a floating supply voltage used to enable the MOSFET.

To support low-voltage operation, a regulated triple charge pump scheme is used to create a sufficient V_{GS} to drive standard and logic level MOSFETs during the low-voltage transient. Between 4.4 to 18 V, the charge pump regulates the voltage in a tripler mode. Beyond 18 V and until the maximum operating voltage, the charge pump switches over to a doubler mode to improve efficiency. The charge pump is continuously monitored for undervoltage and overvoltage conditions to prevent underdriven or overdriven MOSFET scenarios.

VCP_LSD LDO—Low-Side Gate Supply

The DRV8305 uses a linear regulator to generate the proper gate to source voltage for the low-side N-channel MOSFETs. The linear regulator generates a fixed 10-V supply voltage with respect to GND. To support low-voltage operation, the input voltage for the VCP_LSD linear regulator is taken from the VCPH charge pump. This allows the DRV8305 to provide a sufficient V_{GS} to drive standard and logic level MOSFETs during the low voltage transient. The VCP_LSD regulator is continuously monitored for undervoltage conditions.

3.4.2 Current Shunt Amplifier in DRV8305

The DRV8305 includes three high-performance low-side current shunt amplifiers for accurate current measurement using low-side shunt resistors in the external half-bridges. They are commonly used to measure the motor phase current to implement overcurrent protection, external torque control, or external commutation control through the application MCU.

The current shunt amplifiers have the following features:

- Can be programmed and calibrated independently
- Can provide output bias up to 2.5 V to support bidirectional current sensing
- May be used for either individual or total current shunt sensing
- Four programmable gain settings through SPI registers (10, 20, 40 and 80 V/V)
- Programmable output bias scaling. The scaling factor k can be programmed through SPI registers (1/2 or 1/4).
- Programmable blanking time of the amplifier outputs.
- Minimizes DC offset and drift through temperature with DC calibrating through SPI register.

The output of current shunt amplifier can be calculated as:

$$V_O = \frac{V_{REF}}{k} - G \times \left(SN_X - SP_X\right) \tag{3}$$

where

- V_{REF} is the reference voltage from the VREG pin
- G is the gain setting of the amplifier
- k = 2 or 4
- SN_X and SP_X are the inputs of channel x

Figure 5 shows the current amplifier simplified block diagram.

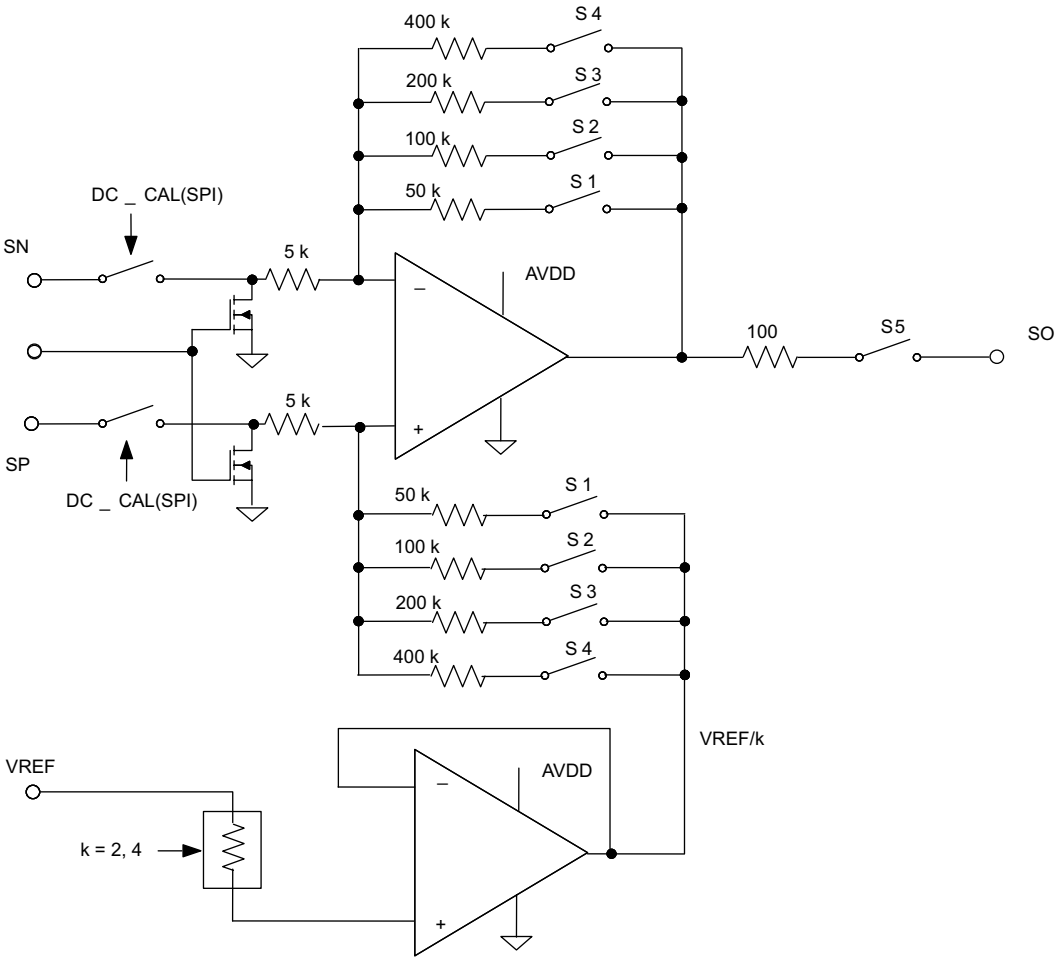


Figure 5. DRV8305 Current Shunt Amplifier Simplified Block Diagram

3.4.3 Protection Features in DRV8305

3.4.3.1 MOSFET Shoot-Through Protection (TDRIVE)

The DRV8305 integrates analog handshaking and digital dead time to prevent shoot-through in the external MOSFETs.

- An internal handshake through analog comparators is performed between each high-side and low-side MOSFET switching transition to avoid cross conduction.
- A minimum dead time (digital) of 40 ns is always inserted after each successful handshake. This digital dead time is programmable through the DEAD_TIME SPI register setting in addition to the time taken for the analog handshake.

3.4.3.2 MOSFET Overcurrent Protection (VDS_OCP)

To protect the system and external MOSFET from damage due to high current events, V_{DS} overcurrent monitors are implemented in the DRV8305. The V_{DS} sensing is implemented for both the high-side and low-side MOSFETs through the following pins:

- High-side MOSFET: V_{DS} measured between VDRAIN and SHx pins
- Low-side MOSFET: V_{DS} measured between SHx and SLx pins

Based on the R_{DS_ON} of the power MOSFETs and the maximum allowed I_{DS}, a voltage threshold can be calculated, which when exceeded, triggers the V_{DS} overcurrent protection feature. The voltage threshold level is programmable through the SPI VDS_LEVEL setting.

The V_{DS} overcurrent monitors implement adjustable blanking and deglitch times to prevent false trips due to switching voltage transients. The different V_{DS} sensing protection modes are:

- V_{DS} Latched Shutdown Mode: When a V_{DS} overcurrent event occurs, the device will pull all gate drive outputs low and report through nFAULT and SPI registers.
- V_{DS} Report Only Mode: In this mode, when the overcurrent event is detected, the device will take no action related to the gate drivers and will report through nFAULT and SPI registers.
- V_{DS} Disabled Mode: The device ignores V_{DS} overcurrent event detections and does not report them.

MOSFET dV/dt Turnon Protection (TDRIVE)

Parasitic dV/dt turnon can occur when charge couples into the gate of the low-side MOSFET during a switching event. If the charge induces enough voltage to cross the threshold of the low-side MOSFET, shoot-through can occur in the half-bridge. To prevent this, the TDRIVE state machine turns on a strong pulldown during switching. After the switching event has completed, the gate driver switches back to a lower hold off pull down to improve efficiency.

MOSFET Gate Drive Protection (GDF)

The DRV8305 uses a multilevel scheme to protect the external MOSFET from V_{GS} voltages that could damage it.

The first stage uses integrated V_{GS} clamps that will turn on when the GHx voltage exceeds the SHx voltage by a value that could be damaging to the external MOSFETs.

The second stage relies on the TDRIVE state machine to detect when abnormal conditions are present on the gate driver outputs. After the TDRIVE timer has expired, the gate driver performs a check of the gate driver outputs against the commanded input. If the two do not match, a gate drive fault (FETXX_VGS) is reported. This can be used to detect a gate short to ground or gate short to supply event.

The third stage uses undervoltage monitors for the low-side gate drive regulator (VCP_LSD_UVLO2), the high-side gate drive charge pump (VCPH_UVLO2), and an overvoltage monitor for high-side charge pump (VCPH_OVLO). These monitors detect if any of the power supplies to the gate drivers have encountered an abnormal condition.

Low-Side Source Monitors (SNS_OCP)

In additional to the V_{DS} monitors across each MOSFET, the DRV8305 directly monitors the voltage on the SLx pins with respect to ground. If high-current events such phase shorts cause the SLx pin voltage to exceed 2 V, the DRV8305 shuts down the gate driver, puts the external MOSFETs into a high impedance state, and reports a SNS_OCP fault error on the nFAULT pin and corresponding SPI status bit.

Undervoltage Warning (UVFL), Undervoltage Lockout (UVLO), and Overvoltage (OV) Protection

Undervoltage is monitored for on the PVDD, AVDD, VREF, VCPH, and VCP_LSD power supplies. Overvoltage is monitored for on the PVDD and VCPH power supplies.

Overtemperature Warning (OTW) and Shutdown (OTSD) Protection

A multi-level overtemperature detection is implemented in the DRV8305.

MCU Watchdog

The DRV8305 incorporates an MCU watchdog function to ensure that the external controller that is instructing the device is active and not in an unknown state.

VREG Undervoltage (VREG_UV)

The DRV8305 has an undervoltage monitor on the V_{REG} output regulator to ensure the external controller does not experience a brownout condition. The V_{REG} undervoltage level can be set through the SPI setting.

For more details on the protections, and SPI monitoring, see the DRV8305 datasheet (SLVSCX2).

3.5 Power Stage Design—Microcontroller MSP430

Figure 6 shows the schematic for configuring the MSP430G2553 MCU. C16 and C17 are the decoupling capacitors. The resistor R8 is used to limit the dV/dt at the supply pin of the MSP430G2553. TI recommends using a 4.7- µF capacitor (minimum) at the DVCC pin. The TIDA-00771 reference design uses a 10-µF capacitor at the DVCC pin. A 0.1-µF capacitor has been added to obtain the best performance at a high frequency.

The Timer A of the MCU is used for PWM generation. The TA1.2 instance of the timer and the corresponding pins are mapped to the high-side switch PWM. The TA1.1 instance of the timer and the corresponding pins are mapped to the low-side switch PWM. The TIDA-00771 reference design uses unipolar, trapezoidal BLDC control where the high-side switches switching at a high frequency. The low-side switches switch at the electrical frequency of the motor current, which is much lower and the same will switch at a high frequency (complimentary to high-side switch) during the freewheeling period to enable active freewheeling and hence low losses. All the feedback signal voltages including the DC bus voltage, current sense amplifier output, potentiometer voltage for speed control, and temperature sensor output are interfaced to the 10-bit successive approximation (SAR) ADC channels of the MCU. The current sense amplifier output is also connected to the comparator input. An external reference is used to set the comparator reference using the resistors R23 and R24.

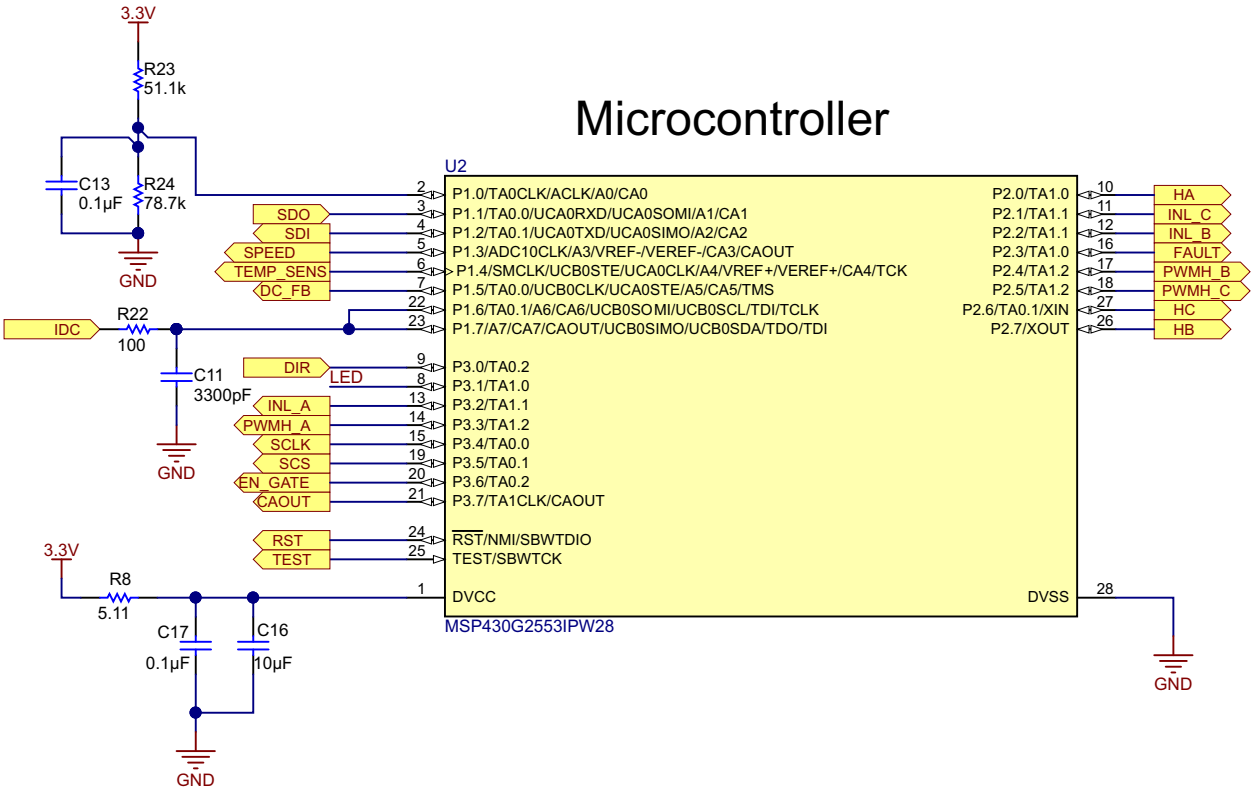


Figure 6. Schematic of MSP430G2553

3.6 Power Stage Design—Cycle-By-Cycle Overcurrent Protection

The cycle-by-cycle overcurrent protection is implemented using the current sense amplifier in the DRV8305, the comparator A+ in the MSP430G2553, and the buffer SN74LVC126A. The overcurrent protection circuit is shown in Figure 7.

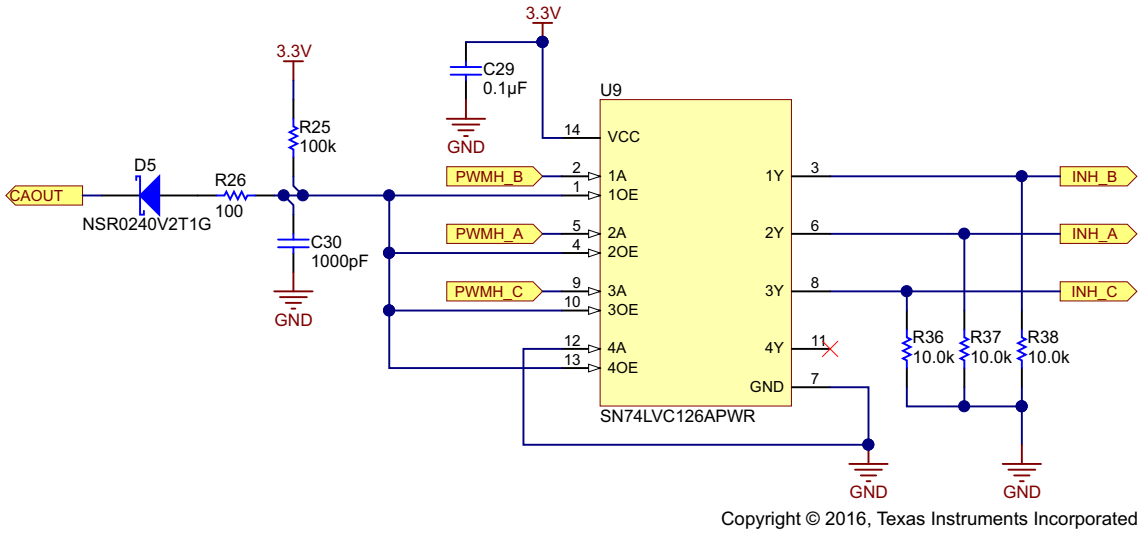


Figure 7. Schematic of Cycle-by-Cycle Overcurrent Protection Circuit Using SN74LVC126A

3.6.1 Comparator_A+

The Comparator_A+ module is an analog voltage comparator that features the following:

- Inverting and non-inverting terminal input multiplexer
- Software selectable RC-filter for the comparator output
- Interrupt capability
- Selectable reference voltage generator
- Comparator and reference generator can be powered down
- Input multiplexer

The comparator compares the analog voltages at the non-inverting (+) and inverting (–) input terminals. If the non-inverting terminal is more positive than the inverting terminal, the comparator output CBOUT is high. The comparator can be switched on or off using the control bit CBON.

The output of the comparator can be used with or without internal filtering. When control bit CBF is set, the output is filtered with an on-chip RC filter. The delay of the filter can be adjusted in four different steps. Selecting the output filter can reduce errors associated with comparator oscillation.

The comparator can be used with internal or external reference voltages. The TIDA-00771 uses external reference.

3.6.2 PWM Shutoff Using SN74LVC126A

The SN74LVC126A, a quadruple bus buffer gate, features independent line drivers with 3-state outputs. Each output is disabled when the associated output enable (OE) input is low. To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver. Inputs can be driven from either 3.3-V or 5-V devices.

In the TIDA-00771 design, all the high-side PWM signals are connected through the buffer. Whenever a current limit happens, all the high-side PWMs will shut off by pulling down the OE of the buffer.

The OE of the buffer is connected to the comparator output through a diode D5 and the current limiting resistor R26. When the DC bus current reaches the set current limit reference, the comparator output goes low, which causes the capacitor C30 to discharge through the resistor R26 and D5. Once the capacitor discharges below the V_{IL} of buffer, all the buffer outputs will tristate. This means all the high-side PWMs are off and the current falls down. As the current goes below the overcurrent reference threshold, the comparator output goes high (3.3 V), and as the OE voltage is lower, the diode D5 will be reverse biased.

Now the capacitor C30 will charge through the resistor R25. When C30 reaches the V_{IH} of the buffer, the buffer output will be enabled and the high-side PWMs goes high. The value of C30 and R25 are designed such that, once the OE is disabled, the next enable will be after approximately 50 µs.

The value of C30 has to be low to make sure that C30 discharges immediately through R26, and this affects the response time of the current limit action.

3.7 *Power Stage Design—Hall Sensor Interface*

Figure 8 shows the Hall sensor interface from the motor to the board. The 3.3 V generated by the DRV8305 is used as the power supply for the Hall sensor. Usually, the Hall sensors have an open drain or open collector configuration. R13, R14, and R15 are used as the pullup resistors. R42, R43, and R44 along with C14, C26, and C27 form noise filters at the Hall sensor input.

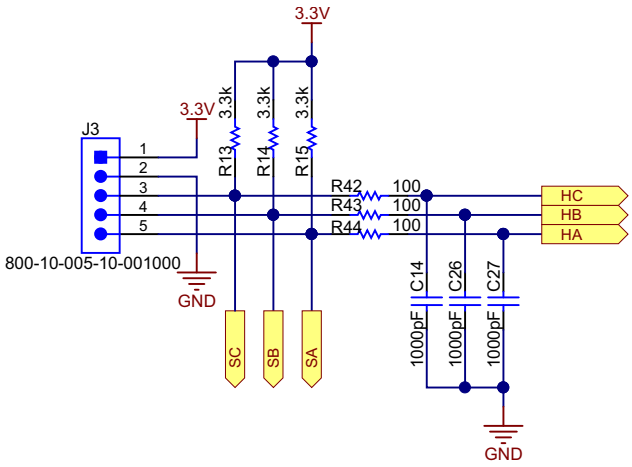


Figure 8. Schematic of Hall Sensor Connector

NOTE: The Hall sensor connection should match with the winding connection for proper operation of the BLDC motor.

3.8 Power Stage Design—External Interface Options and Indications

3.8.1 ESD Protection

The DC-bus voltage lines and the hall sensor signal interfaces are externally protected using ESD devices, as Figure 9 shows. The TPD1E10B06 diode is used for ESD protection. The TPD1E10B06 is a single-channel, ESD, transient-voltage-suppression (TVS) diode, which offers ±30-kV contact ESD, ±30-kV IEC air-gap protection, and has an ESD clamp circuit with a back-to-back TVS diode for bipolar or bidirectional signal support.

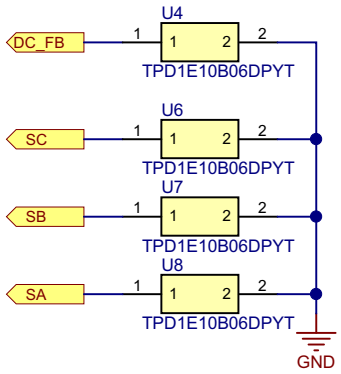


Figure 9. Schematic of ESD Protection

3.8.2 Speed Control of Motor

The speed control is done using a potentiometer (POT), and the POT voltage is fed to the ADC of the MSP430G2553. The circuit is shown in Figure 10. The POT is supplied from the 3.3 V generated by the DRV8305. A 20k POT can be connected externally to the jumper J2. Connect the fixed terminals of the POT to terminal 1 and 3 of J2 and mid-point to terminal 2 of J2.

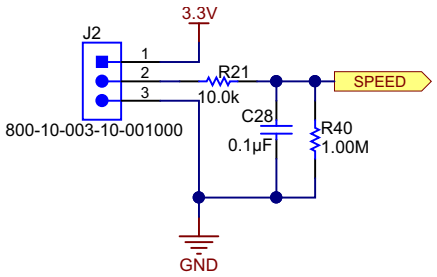


Figure 10. Schematic of Potentiometer Connection for Speed Control

The resistor R40 is used to ensure that the speed control reference is zero if the POT terminal is open.

3.8.3 Direction of Rotation—Digital Input

The jumper J4 (shown in Figure 11) is used to set the direction of rotation of the motor. Close or open the jumper to change the direction of rotation.

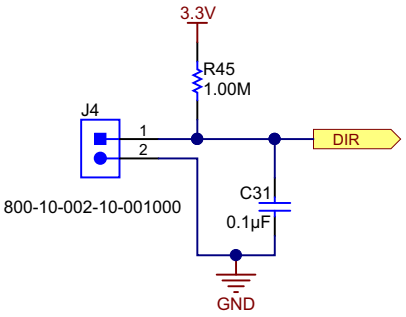


Figure 11. Schematic of Digital Input to Change Direction of Rotation

3.8.4 Temperature Sensing

Figure 12 shows the temperature sensor circuit used to measure the PCB temperature. The LMT87 is an analog output temperature sensor. The temperature sensing element is comprised of a simple base emitter junction that is forward biased by a current source. The temperature sensing element is then buffered by an amplifier and provided to the OUT pin. The amplifier has a simple push-pull output stage, thus providing a low-impedance output source. The average output sensor gain is 13.6 mV/°C.

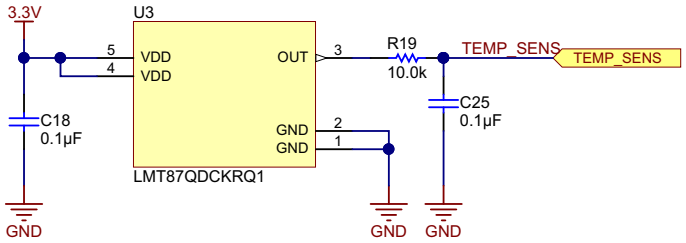


Figure 12. Schematic of Temperature Sensor

3.8.5 LED Indications

Figure 13 shows the LED indications provided in the board. The LED D4 indicates the 3.3 V in the board, D1 is tied to FAULT signal from DRV8305, and D3 is driven by a digital I/O in the MSP430G2553.

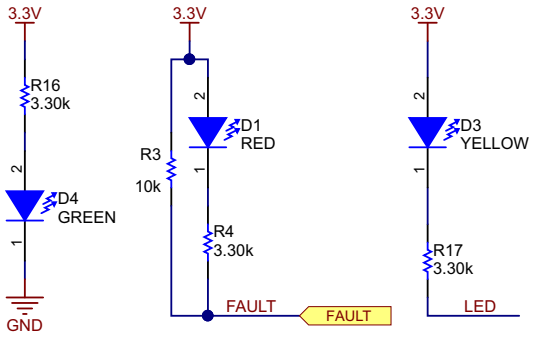


Figure 13. Schematic of LED Indications

4 Block Diagram

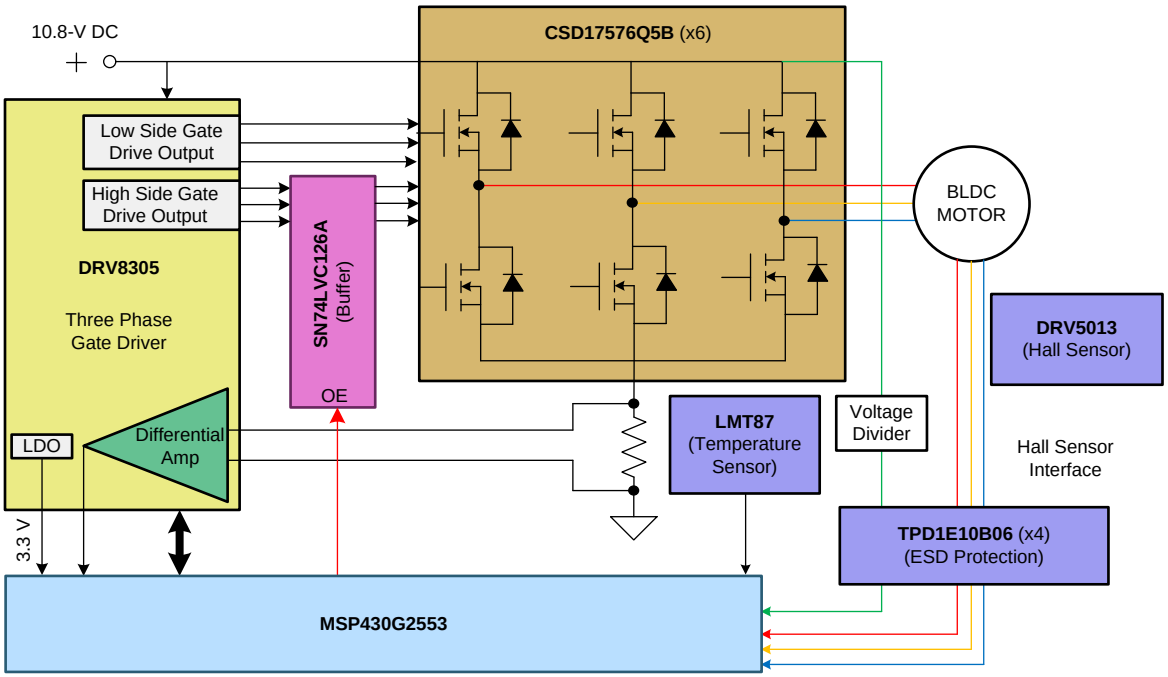


Figure 14. Block Diagram of TIDA-00771

4.1 Highlighted Products

4.1.1 CSD17576Q5B

The CSD17576Q5B is a 30-V N-channel NexFET Power MOSFET with a very low R_{DS_ON} of 1.7 mΩ and features very low total gate charge requirement. The CSD17576Q5B is available in very small package, SON 5×6 mm with a peak current rating of 400 A.

4.1.2 DRV8305

The DRV8305 is a gate driver IC for three-phase motor drive applications. It provides three high-accuracy trimmed and temperature compensated half-bridge drivers, each capable of driving a high-side and low-side N-type MOSFET. The DRV8305 includes three current shunt amplifiers for accurate current measurements, supports 100% duty cycle and have multiple levels of protection. The gate driver is programmable through SPI.

4.1.3 MSP430G2553

The Texas Instruments MSP430™ family of ultra-low-power microcontrollers consists of several devices featuring different sets of peripherals targeted for various applications. The architecture, combined with five low-power modes, is optimized to achieve extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows wake-up from low-power modes to active mode in less than 1 µs.

The MSP430G2x13 and MSP430G2x53 series are ultra-low-power mixed signal microcontrollers with built-in 16-bit timers, up to 24 I/O capacitive-touch enabled pins, a versatile analog comparator, and built-in communication capability using the universal serial communication interface. In addition, the MSP430G2x53 family members have a 10-bit analog-to-digital (A/D) converter.

4.1.4 SN74LVC126A

This quadruple bus buffer gate is designed for 1.65- to 3.6-V VCC operation. The SN74LVC126A features independent line drivers with 3-state outputs. Each output is disabled when the associated OE input is low. Inputs can be driven from either 3.3-V or 5-V devices.

4.1.5 LMT87

The LMT87 is a precision CMOS integrated-circuit temperature sensors with an analog output voltage that is linearly and inversely proportional to temperature. It can operate down to a 2.7-V supply with a 5.4-µA power consumption. Package options including through-hole TO-92 package allows the LMT87 to be mounted onboard, off-board, to a heat sink, or on multiple unique locations in the same application. A class-AB output structure gives the LMT87 and LMT87-Q1 strong output source and sink current capabilities that can directly drive up to 1.1-nF capacitive loads. This means it is well suited to drive an analog-to-digital converter sample-and-hold input with its transient load requirements. It has accuracy specified in the operating range of −50°C to 150°C.

4.1.6 TPD1E10B06D

The TPD1E10B06 device is a single-channel electrostatic discharge (ESD) TVS diode in a small 0402 package. This TVS protection product offers ±30-kV contact ESD, ±30-kV IEC air-gap protection, and has an ESD clamp circuit with a back-to-back TVS diode for bipolar or bi-directional signal support. The 12-pF line capacitance of this ESD protection diode is suitable for a wide range of applications supporting data rates up to 400 Mbps.

5 Getting Started Hardware

5.1 Connector Configuration of TIDA-00771

Figure 15 shows the TIDA-00771 connector configuration, which the following list details:

- Two-terminal input for power supply: This pin is used to connect the input DC supply from the battery. The positive and negative terminals can be identified as shown in Figure 15.
- Three-terminal output for motor winding connection: The phase output connections for connecting to the three-phase BLDC motor winding, marked as PHASE U, PHASE V, and PHASE W as shown in Figure 15.
- Four-pin connector J1: This is the programming connector for the MSP430G2553 MCU. The two-wire Spy-Bi-Wire protocol is used to program the MSP430G2553 MCU.
- Three-pin connector J2: This connector can be used to interface an external potentiometer for speed reference. The two fixed terminals of the potentiometer should be connected to 3V3 pin and GND pin. The mid-point of the potentiometer should be connected to the POT pin of the connector.
- Five pin connector J3: This is the interface for connecting the Hall position sensors from the motor.
- Two-pin connector J4: This connector is used for the motor direction change. Externally shorting or opening this connector will change the direction of rotation of the motor.

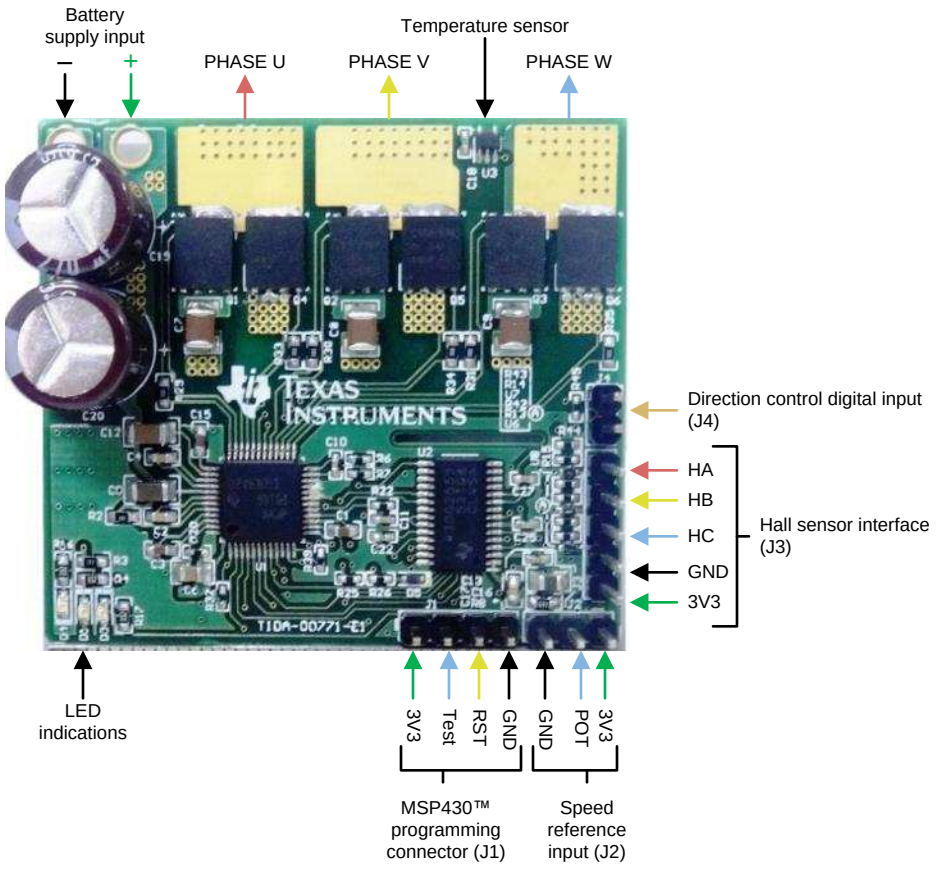


Figure 15. TIDA-00771 PCB Connectors

5.2 Programming MSP430G2553

The two-wire Spy-Bi-Wire protocol is used to program the MSP430G2553 MCU. Figure 16 shows the four-pin programming connector provided in the TIDA-00771 board.

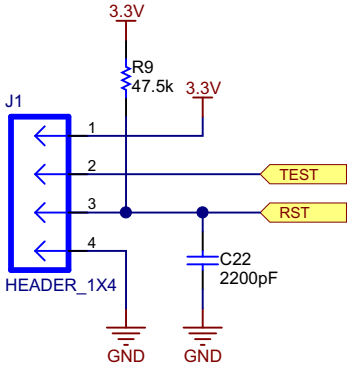


Figure 16. Schematic of MSP430G2553 Programming Connector

See the development tools on the MSP430G2553 product page for programming options with an external JTAG interface (http://www.ti.com/product/MSP430G2553/toolssoftware#devtools).

The following list outlines the steps to program the MSP430G2553 MCU when the programming supply voltage is provided by the board itself:

1. Remove the motor connections from the board and power on the input DC supply. Make sure that a minimum of 5-V DC input is applied and 3.3 V is generated in the board.
2. Connect the programmer to the board.
3. Open the CCS software and then build and debug the code to program the MSP430G2553.

5.3 Procedure for Board Bring-up and Testing

The following list details the procedure for board bring-up and testing:

1. Remove the motor connections from the board and power on the input DC supply. Make sure that a minimum of a 5-V DC input is applied and the 3.3 V is generated in the board.
2. Program the MCU as detailed in Section 5.2.
3. Remove the programmer, and switch off the DC input supply.
4. Connect the inverter output to the motor winding terminals. Connect the position Hall sensor inputs to the connector J3, and make sure that the winding connection and Hall sensor connections match.
5. Connect the POT at the interface J2 and set the speed reference.
6. Use a DC power supply with current limit protection and apply 5-V DC to the board. If the Hall sensors and winding are connected properly in the matching sequence, then the motor will start running at a speed set by the POT.
7. If the motor is not rotating and takes high current or rotates and draw distorted peak winding current waveform (proper waveform shape is as shown in Figure 31), then check the winding and Hall sensor connection matching and, if wrong, correct it.
8. Adjust the POT voltage for change in speed.
9. To change direction, switch off the DC input, close the jumper J4, and switch on the DC input.

6 Getting Started Firmware

6.1 System Features

The TIDA-00771 firmware offers the following features and user controllable parameters:

- Trapezoidal control of BLDC motor using digital position Hall sensor feedback
- Overcurrent protection using the internal comparator of the MSP430G2553 MCU
- Latch protection using the V_{DS} sensing feature of DRV8305

Table 2 shows the TIDA-00771 firmware system components.

Table 2. System Components

SYSTEM COMPONENT		DESCRIPTION
Development and emulation		Code Composer Studio™ v5.5
Target controller		MSP430G2553
PWM frequency		20-kHz PWM (default), programmable for higher and lower frequencies
PWM mode		Asymmetrical
Interrupts		Port 2 interrupt for Hall sensor change CPU Timer A implements 20-kHz ISR execution rate ADC interrupt
Peripherals used	PWM generation: Timer configuration	High-side PWM: TIMER A1.2, 16-MHz clock, OUTMOD[2:0] = 2, PWM frequency set for 20 kHz Low-side PWM: TIMER A1.1, 16-MHz clock, OUTMOD[2:0] = 6, PWM frequency set for 20 kHz
	Position feedback: Hall sensor signals	P2.0 → HA P2.7 → HB P2.6 → HC
	Comparator configuration for overcurrent protection	CA0/P1.0 → VREF (+ve input of comparator) CA7/P1.7 → CSA output (–ve input of comparator) CAOUT/P3.7 → Comparator output
	ADC channel assignment	A3 → Speed reference from the external potentiometer A4 → PCB or FET temperature feedback A5 → DC bus voltage sensing A6 → Low-side DC bus current sensing
	DRV8305: SPI programming pins connection	P1.1 → SDO P1.2 → SDI P3.4 → SCLK P3.5 → SCS
	DRV8305: Digital I/Os	P3.6 → EN_GATE P2.3 → FAULT
	MCU Digital I/Os	P3.0 → Direction of motor rotation P3.1 → LED3

6.2 Customizing Reference Code

To modify the firmware, the end user must have CCS installed as well as the MSP430G2553 configuration files. The following sections describe the different user-adjustable parameters and how to select an optimized value for a specific application.

Open CCS and load the reference project "TIDA-00771_Firmware _V1.0". Note that if this project is in a .zip or .rar compressed format, the user must extract this file.

6.2.1 Customizing Reference Code in MSP430™ (main.c)

Select the "main.c" file. Parameters exist at the top of the file that can be optimized and are included as the configuration variables. The following section of code shows these parameters:

```
#define PWM_PERIOD      400 //      PWM Frequency (Hz) = 16MHz/((2*PWM_PERIOD)-1)
#define MAX_DUTYCYCLE   400 //      relative to PWM_PERIOD
#define MIN_DUTYCYCLE   50  //      relative to PWM_PERIOD
#define ACCEL_RATE      500 //      Ramp up time to full scale duty cycle =
(Full scale duty cycle) * ACCEL_RATE * PWM_PERIOD/PWM_Frequency
#define DEAD_TIME       1   //      Dead time from MSP430 = DEAD_TIME* 0.0625 uS
(for 16MHz clock)
#define Block_Rotor_Duration  800 //Blocked_rotor shut off time(s) =
                                    Block_Rotor_Duration*30000/clock frequency
```

6.2.1.1 PWM_PERIOD

PWM_PERIOD sets the value in capture and compare register 0 of Timer_A. The Timer_A is initialized to operate at 16 MHz; see Equation 4 to calculate the PWM frequency. The TIMER_A PWM is configured in up-down mode.

$$\text{PWM Frequency}(\text{Hz}) = \frac{16\ \text{MHz}}{((\text{PWM\_PERIOD}) - 1)} \tag{4}$$

For example, with PWM_PERIOD = 401:

$$\text{PWM Frequency}(\text{Hz}) = \frac{16\ \text{MHz}}{(401 - 1)} = 20\ \text{kHz}$$

6.2.1.2 MAX_DUTYCYCLE

MAX_DUTYCYCLE sets the maximum duty cycle the user can set. Every time the duty cycle input command is compared to the MAX_DUTYCYCLE. If the duty cycle input command exceeds the MAX_DUTYCYCLE, the target duty cycle is set to the MAX_DUTYCYCLE. This number is relative to the PWM_PERIOD.

6.2.1.3 MIN_DUTYCYCLE

MIN_DUTYCYCLE sets the minimum duty cycle that can be applied to the motor. This number is relative to the PWM_PERIOD.

6.2.1.4 ACCEL_RATE

ACCEL_RATE defines how fast the motor will accelerate. For a motor with greater inertia or if it needs a longer time to accelerate, set this number to a high value such as 2000. Motors that can quickly ramp up can use a smaller ACCEL_RATE to decrease the startup time.

In the application program, the start ramp-up time and the ACCEL_RATE required can be calculated using Equation 5 and Equation 6.

$$\text{Ramp-up time to full scale duty cycle} = \frac{\text{Full scale duty cycle} \times \text{ACCEL\_RATE} \times \text{PWM\_PERIOD}}{\text{PWM frequency}} \tag{5}$$

$$\text{ACCEL\_RATE} = \frac{\text{Ramp-up time to full scale duty cycle} \times \text{PWM frequency}}{\text{Full scale duty cycle} \times \text{PWM\_PERIOD}} \tag{6}$$

For example: To ramp up from 0% to 100% duty cycle (Full scale duty cycle = 1) in 10 seconds, provided the PWM frequency = 20 kHz, the ACCEL_RATE can be calculated as such:

$$\text{ACCEL\_RATE} = \frac{10\ \text{s} \times 20\ \text{kHz}}{1 \times 400} = 500$$

6.2.1.5 Block_Rotor_Duration

Block_Rotor_Duration defines the time duration in which the motor blocked rotor condition is allowed before the controller turns off all the PWM. The time taken to turn off all the PWM when the motor is blocked can be calculated using Equation 7.

$$\text{Blocked rotor PWM turn off time}(s) = \frac{\text{Block\_Rotor\_Duration} \times 30000}{16\ \text{MHz}} \quad (7)$$

where 16 MHz is the TIMER_A clock frequency.

For example, if the user wants to turns off the motor if a blocked rotor condition is observed for 1.5 seconds, then:

$$\text{Block\_Rotor\_Duration} = 1.5 \times \frac{16\ \text{MHz}}{30000} = 800 \quad (8)$$

6.2.2 Configuring DRV8305 Registers (drv8305.c)

The register settings of the DRV8305 can be modified by selecting and modifying the file "drv8305.c".

See the function "drv8305_init()" to initialize the DRV8305 with modified values. The code snippet of the function is given as follows.

```
void drv8305_init(void)
{
      //setup drv8305 via SPI commands
      WriteRegister(0x05, (TDRIVEN_2000NS + IDRIVEN_HS_1000MA +
      IDRIVEP_HS_1000MA));

      delay_1ms(1);
      WriteRegister(0x06, (TDRIVEP_2000NS + IDRIVEN_LS_1000MA +
      IDRIVEP_LS_1000MA));

      delay_1ms(1);
      WriteRegister(0x07, (COMM_OPTION_ACTIVE_FW + PWM_MODE_6_INDEPENDENT +
      DEAD_TIME_40NS + TBLANK_0US + TVDS_2US));

      delay_1ms(1);
      WriteRegister(0x09, (FLIP_OTS_ENABLE + DIS_VPVDD_UVLO2_DISABLE +
      DIS_GDRV_FAULT_ENABLE + EN_SNS_CLAMP_ENABLE + WD_DLY_20MS +
      DIS_SNS_OCP_ENABLE + WD_EN_DISABLE + SLEEP_AWAKE + CLR_FLTS_NORMAL +
      SET_VCPH_UV_4D9V));

      delay_1ms(1);
      WriteRegister(0x0A, (DC_CAL_CH3_NORMAL + DC_CAL_CH2_NORMAL +
      DC_CAL_CH1_NORMAL + CS_BLANK_0NS + GAIN_CS3_10VV + GAIN_CS2_10VV +
      GAIN_CS1_10VV));

      delay_1ms(1);
      WriteRegister(0x0B, (VREF_SCALING_K4 + SLEEP_DLY_10US + VREG_UV_LEVEL_10P));

      delay_1ms(1);
      WriteRegister(0x0C, (VDS_LEVEL_0D175V + VDS_MODE_REPORT));
}
```

The function "`WriteRegister(uint8_t, uint16_t)`" is used to write to the DRV8305 registers, and the function "`ReadRegister(uint8_t)`" is used to read the DRV8305 register content.

The register map of the DRV8305 is given in Table 3, which is taken from the DRV8305 datasheet (see the DRV8305 datasheet SLVSCX2 for a detailed understanding of register settings).

Table 3. Register Map of DRV8305

ADDRESS	NAME	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0x1	Warnings & Watchdog Reset	FAULT	*RSVD*	TEMP_FLAG4	PVDD_UVFL	PVDD_OVFL	VDS_STATUS	VCPH_UVFL	TEMP_FLAG1	TEMP_FLAG2	TEMP_FLAG3	OTW
0x2	OV/VDS Faults	VDS_HA	VDS_LA	VDS_HB	VDS_LB	VDS_HC	VDS_LC	*RSVD*		SNS_C_OCP	SNS_B_OCP	SNS_A_OCP
0x3	IC Faults	PVDD_UVLO2	WD_FAULT	OTSD	RSVD	VREG_UV	AVDD_UVLO	VCP_LSD _UVLO2	*RSVD*	VCPH_UVLO2	VCPH_OVLO	VCPH_OVLO _ABS
0x4	VGS Faults	VGS_HA	VGS_LA	VGS_HB	VGS_LB	VGS_HC	VGS_LC	*RSVD*				
0x5	HS Gate Drive Control	*RSVD*	TDRIVEN		IDRIVEN_HS			IDRIVEP_HS				
0x6	LS Gate Drive Control	*RSVD*	TDRIVEP		IDRIVEN_LS			IDRIVEP_LS				
0x7	Gate Drive Control	*RSVD*	COMM_OPTION	PWM_MODE		DEAD_TIME		TBLANK		TVDS		
0x8	Reserved	*RSVD*										
0x9	IC Operation	FLIP_OTSD	DIS_PVDD _UVLO2	DIS_GDRV _FAULT	EN_SNS _CLAMP	WD_DLY		DIS_SNS_OCP	WD_EN	SLEEP	CLR_FLTS	SET_VCPH_UV
0xA	Shunt Amplifier Control	DC_CAL_CH3	DC_CAL_CH2	DC_CAL_CH1	CS_BLANK		GAIN_CS3		GAIN_CS2		GAIN_CS1	
0xB	Voltage Regulator Control	*RSVD*	VREF_SCALE		*RSVD*			SLEEP_DLY		DIS_VREG _PWRGD	VREG_UV_LEVEL	
0xC	VDS Sense Control	*RSVD*			VDS_LEVEL					VDS_MODE		

6.2.3 Initializing the SPI Communication Between DRV8305 and MSP430 (drv8305.h)

The register initialization for the DRV8305 is done by means of SPI communication. The SPI communication pins are connected to the ports of the MSP430G2553.

See "drv8305.h" to assign and initialize the ports of the MSP430G2553 for SPI communication. The TIDA-00771 reference design uses the following port connections.

Table 4. SPI Communication Interface Between DRV8305 and MSP430™

DRV8305 PIN	MSP430G2553 PIN
SDO	P1.1
SDI	P1.2
SCLK	P3.4
SCS	P3.5

Modify the SPI GPIO settings as per the hardware mapping. For the TIDA-00771, the mapping is shown in the following code snippet.

```
#define CPU_FREQ_MHZ    (16)

/*****************************************************************************
 * SPI GPIO Settings (Modify according to hardware mapping)
 *****************************************************************************/
#define M1_SCLK_HIGH    (P3OUT |= BIT4)
#define M1_SCLK_LOW     (P3OUT &= ~BIT4)

#define M1_SDI_HIGH     (P1OUT |= BIT2)
#define M1_SDI_LOW      (P1OUT &= ~BIT2)

#define M1_SDO_LEVEL    ((P1IN &= BIT1)?(1):(0))

#define M1_nSCS_HIGH    (P3OUT |= BIT5)
#define M1_nSCS_LOW     (P3OUT &= ~BIT5)
```

6.3 Running the Project in CCS™

To run this project in CCS:

1. Install CCS.
2. Import the project "TIDA-00771_Firmware _1.0".
3. Read through Section 6.2 to customize the code.
4. Power up the board with external supply as described in Section 5.2 and connect the programmer.
5. Build and debug the modified project to download the code to the MSP430F5132.

7 Test Setup

Figure 17 shows the load setup used to test the motor. The load is an electrodynamometer type load by which the load torque applied to the motor can be controlled.

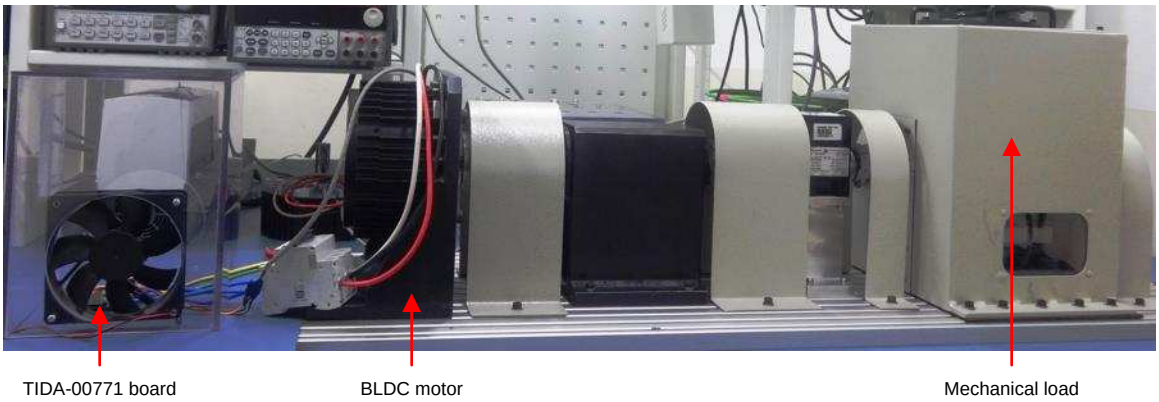


Figure 17. Board and Motor Test Setup

8 Test Data

8.1 Functional Tests

8.1.1 3.3-V Power Supply From DRV8305

The internal LDO of the DRV8305 generates the 3.3 V over a wide DC supply input voltage down to 4.5 V. Figure 18 shows the 3.3 V generated from the DRV8305 at a DC input voltage of 10.8 V. Figure 19 shows the 3.3 V generated from the DRV8305 at a lower DC input voltage of 5 V.

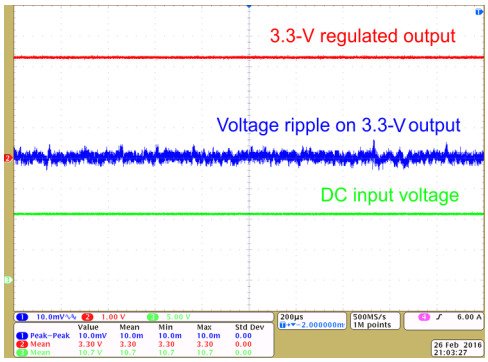


Figure 18. 3.3-V Regulator Output at 10.8-V DC Input

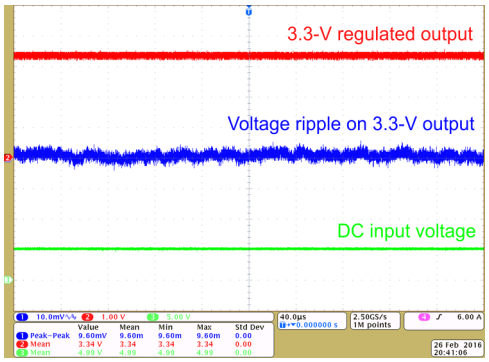


Figure 19. 3.3-V Regulator Output at 5-V DC Input

8.1.2 PWM Signal From MCU and Gate Drive Output From DRV8305

Figure 20 shows the high-side and low-side PWM signals from the MSP430G2553 and the corresponding gate drive output waveforms from DRV8305 at a DC input voltage of 10.8 V. The gate drive output voltage is approximately 10 V.

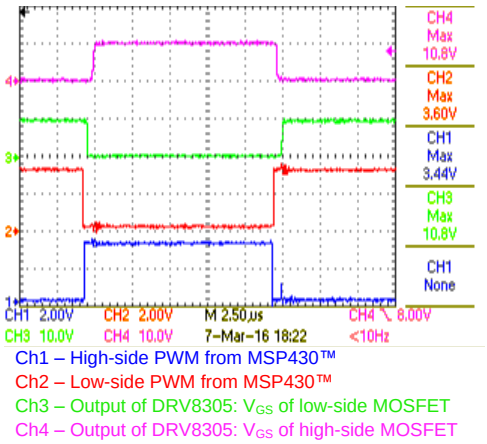


Figure 20. PWM Signals From MSP430G2553 and Corresponding Gate Drive Output From DRV8305

8.1.3 Dead Time From DRV8305

Figure 21 shows the high-side and low-side gate source voltage from the DRV8305. Figure 22 shows the dead time inserted by the DRV8305 at the both the edges of the PWM. The minimum dead time after hand shaking (td_min) from the DRV8305 is 280 ns. The dead time in addition to td_min is set using the register bit DEAD_TIME. The waveform is taken with DEAD_TIME bits set for 35 ns. Therefore, the total dead time would be 280 ns + 35 ns = 315 ns.

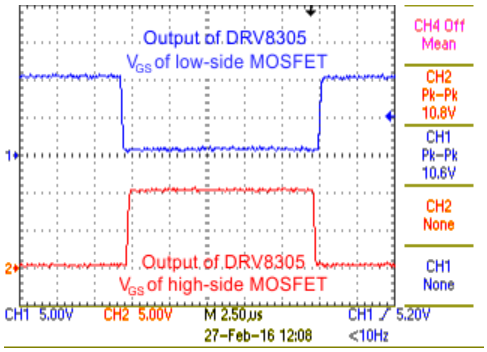


Figure 21. High-Side and Low-Side Gate Source Voltage From DRV8305

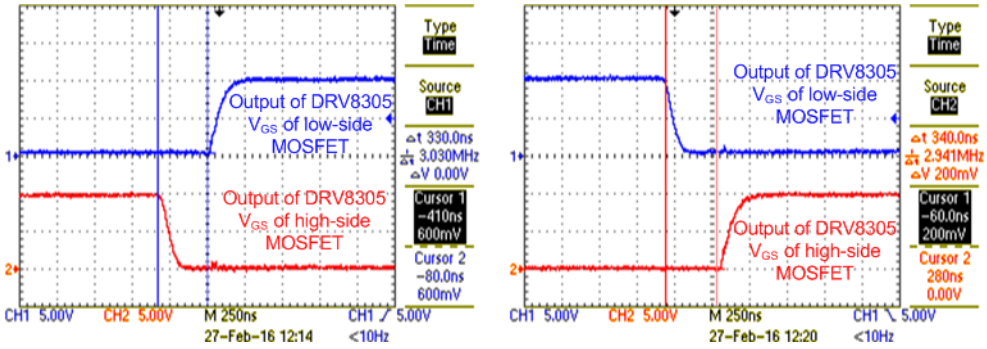


Figure 22. Dead Time Provided by DRV8305 at Both Edges of PWM

8.1.4 Maximum Gate Drive Voltage From DRV8305 Ensures High-Efficiency Inverter

Figure 23 shows the gate drive output waveforms when the input DC supply voltage is 5 V. The low-side gate drive output voltage is approximately 10 V and the high-side gate drive output voltage is approximately 7.5 V. The internal triple-charge pump of the DRV8305 ensures the availability of higher gate drive output voltage and hence improves the efficiency of the inverter. The more the available gate drive voltage V_{GS}, the less will be the R_{DS_ON} of the FETs and hence better efficiency.

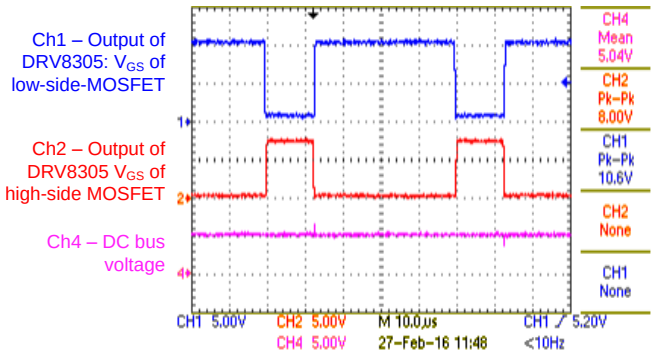


Figure 23. High-Side and Low-Side Gate Drive Output From DRV8305 at DC Input Voltage of 5 V

Figure 24 shows the gate drive output waveforms when the input DC supply voltage is 10.8 V. The low-side and high-side gate drive output voltage is approximately 10 V, which drives the inverter at its maximum efficiency.

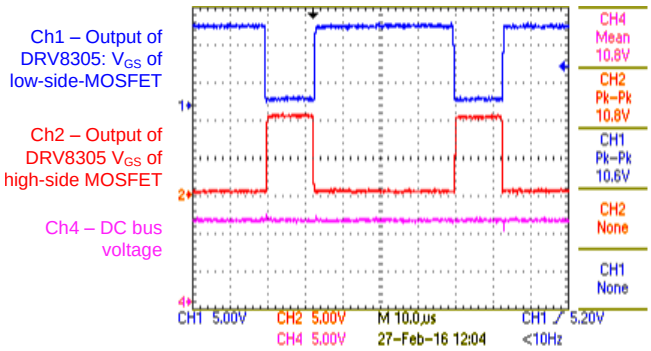


Figure 24. High-Side and Low-Side Gate Drive Output From DRV8305 at DC Input Voltage of 10.8 V

8.1.5 MOSFET Switching Waveforms

Figure 25 through Figure 28 show the V_{DS} and V_{GS} waveforms of the low-side and high-side MOSFETs. The t_{DRIVE} and I_{DRIVE} features in the DRV8305 help to set the optimum gate drive current to achieve the optimum EMI and inverter efficiency performance.

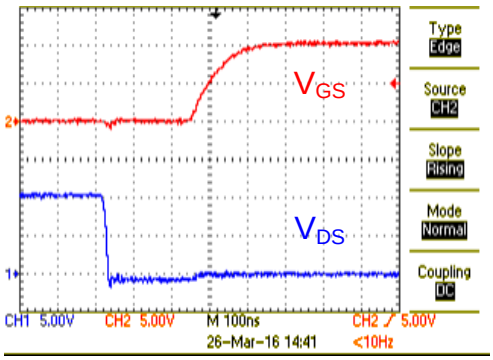


Figure 25. Low-Side FET Turn ON Waveforms

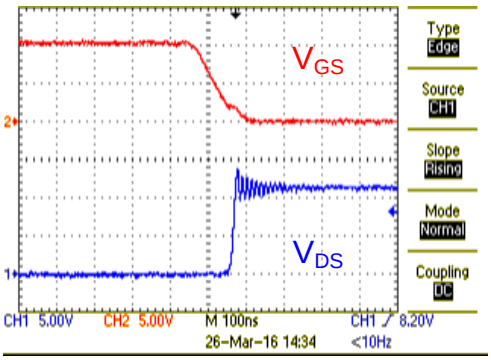


Figure 26. Low-Side FET Turn OFF Waveforms

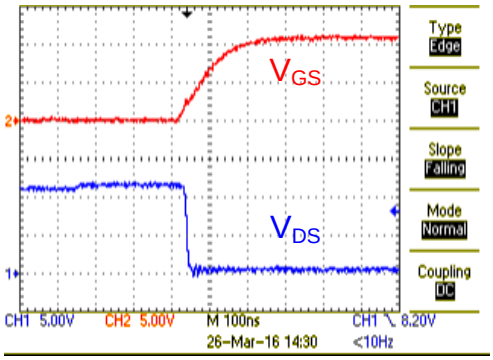


Figure 27. High-Side FET Turn ON Waveforms

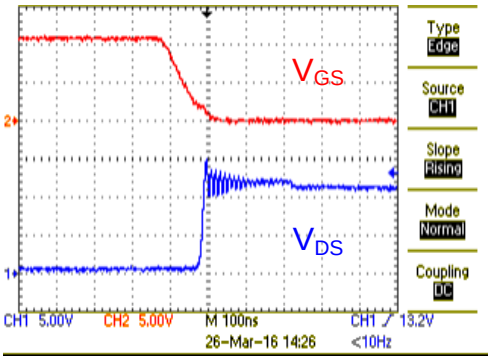


Figure 28. High-Side FET Turn OFF Waveforms

Figure 29 and Figure 30 show the effects of IDRIVE on the performance of the inverter stage. Figure 29 shows the V_{DS} and V_{GS} waveforms with a 250-mA sink current setting. Figure 30 shows the V_{DS} and V_{GS} waveforms with a 500-mA sink current setting. The dV/dt (slew rate) of the V_{DS} rise waveform is controlled with a different gate sink current setting.

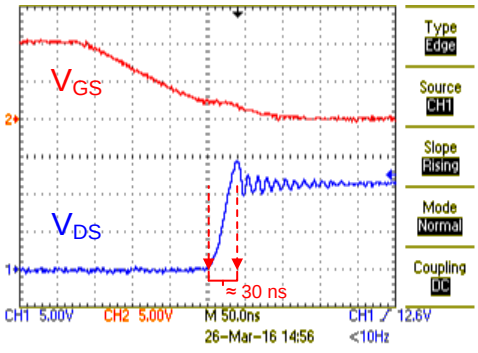


Figure 29. Low-Side FET Turn OFF Waveform (250-mA Sink Current)

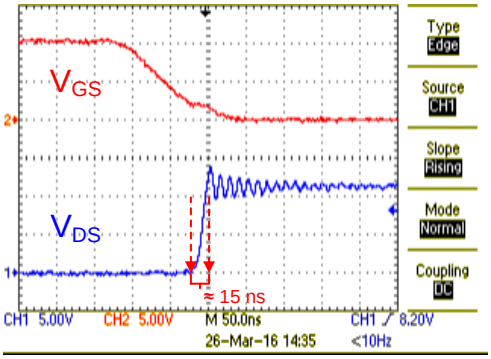


Figure 30. Low-Side FET Turn OFF Waveform (500-mA Sink Current)

8.2 Load Test

The TIDA-00771 board is tested with external BLDC motor and load.

Figure 31 shows the motor winding current and winding voltage waveforms at a 5-V DC input and a 20-A_{RMS} winding current. The testing is done at 100% duty cycle. Figure 32 shows the steady state thermal image of the board at the same condition, captured after 15 minutes of continuous running. The maximum FET temperature observed is 76.3°C.

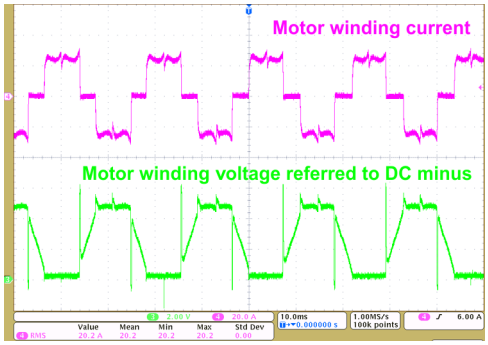


Figure 31. Load Test Results at 5-V DC Input, 20-A_{RMS} Winding Current, 100% Duty Cycle

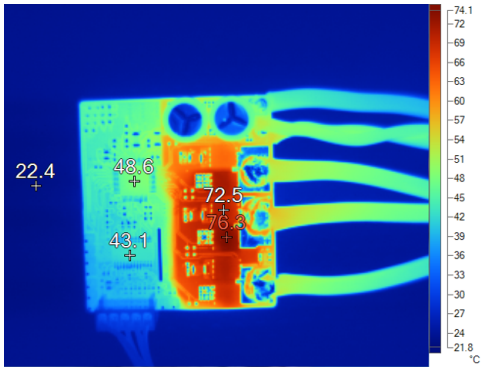


Figure 32. Thermal Image at 5-V DC Input, 20-A_{RMS} Winding Current, 100% Duty Cycle

Figure 33 shows the motor winding current and winding voltage waveforms at a 10.8-V DC input and a 20-A_{RMS} winding current. The testing is done at 100% duty cycle. Figure 34 shows the steady state thermal image of the board at the same condition, captured after 15 minutes of continuous running. The maximum FET temperature observed is 78.5°C.

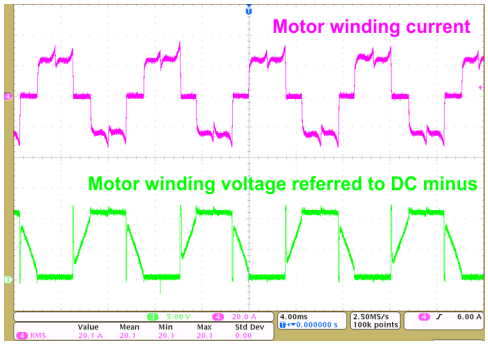


Figure 33. Load Test Results at 10.8-V DC Input, 20-A_{RMS} Winding Current, 100% Duty Cycle

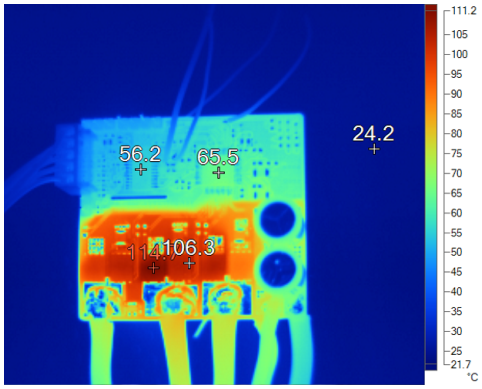


Figure 34. Thermal Image at 10.8-V DC Input, 20-A_{RMS} Winding Current, 100% Duty Cycle

The board is also tested at a DC input voltage of 12.6 V, which is the maximum voltage available from a 3-cell Li-ion battery (4.2 V max per cell). Figure 35 shows the motor winding current and winding voltage waveforms at 12.6-V DC input and 20-A_{RMS} winding current. The testing is done at 100% duty cycle. Figure 36 shows the steady state thermal image of the board at the same condition, captured after 15 minutes of continuous running. The maximum FET temperature observed is 79.4°C.

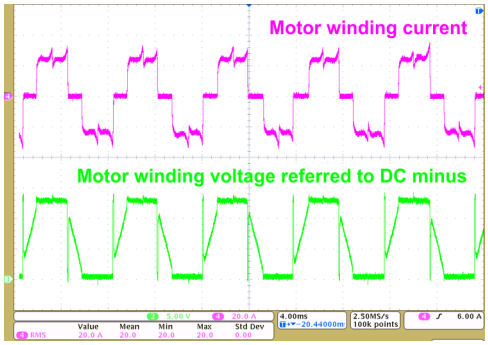


Figure 35. Load Test Results at 12.6-V DC Input, 20-A_{RMS} Winding Current, 100% Duty Cycle

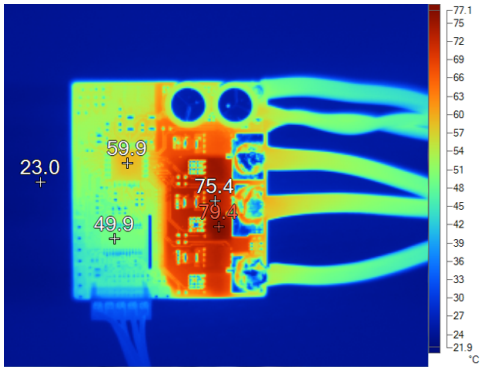


Figure 36. Thermal Image at 12.6-V DC Input, 20-A_{RMS} Winding Current, 100% Duty Cycle

Figure 37 shows the motor winding current and winding voltage waveforms at a 10.8-V DC input and 20-A_{RMS} winding current at 50% duty cycle. Figure 38 shows the steady state thermal image of the board at the same condition, captured after 15 minutes of continuous running. The maximum FET temperature observed is 86.6°C, which is observed on a low-side FET. The maximum temperature observed on the high-side FET is 75.1°C. The PWM is configured as an active freewheeling unipolar PWM.

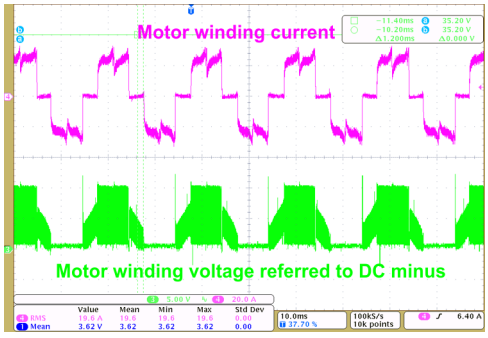


Figure 37. Load Test Results at 10.8-V DC Input, 20-A_{RMS} Winding Current, 50% Duty Cycle

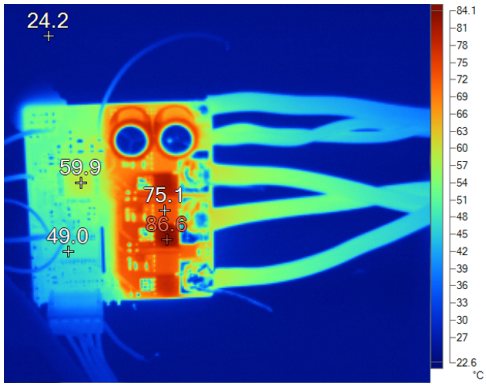


Figure 38. Thermal Image at 10.8-V DC Input, 20-A_{RMS} Winding Current, 50% Duty Cycle

The TIDA-00771 board is also tested for higher currents. Figure 39 shows the test results when the board is delivering a 25-A_{RMS} current to the motor winding. The maximum temperature observed on the MOSFET is 114.7°C. Figure 40 shows the winding current and voltage waveforms at a 30-A_{RMS} current.

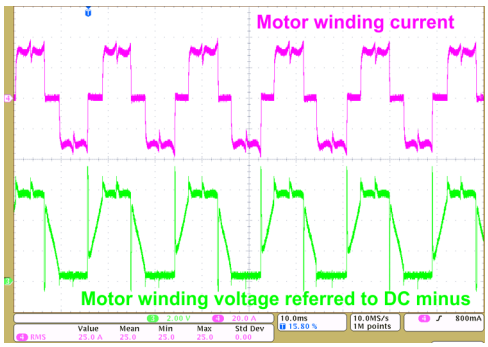


Figure 39. Load Test Results at 6-V DC Input, 25-A_{RMS} Winding Current, 100% Duty Cycle

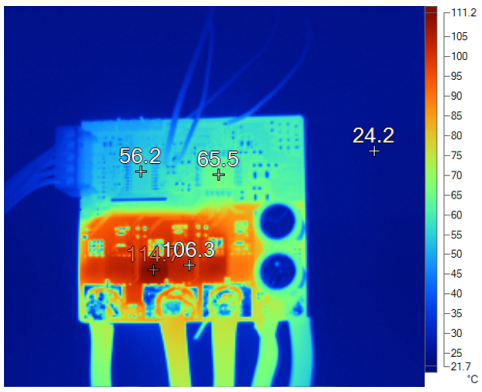


Figure 40. Thermal Image at 6-V DC Input, 25-A_{RMS} Winding Current, 100% Duty Cycle

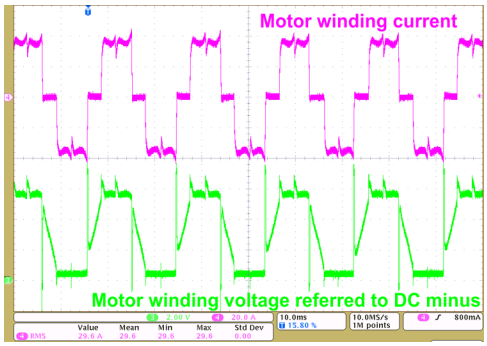


Figure 41. Load Test Results at 6-V DC Input, 30-A_{RMS} Winding Current, 100% Duty Cycle

The maximum steady state temperature on the FET with different winding current is shown in Figure 42.

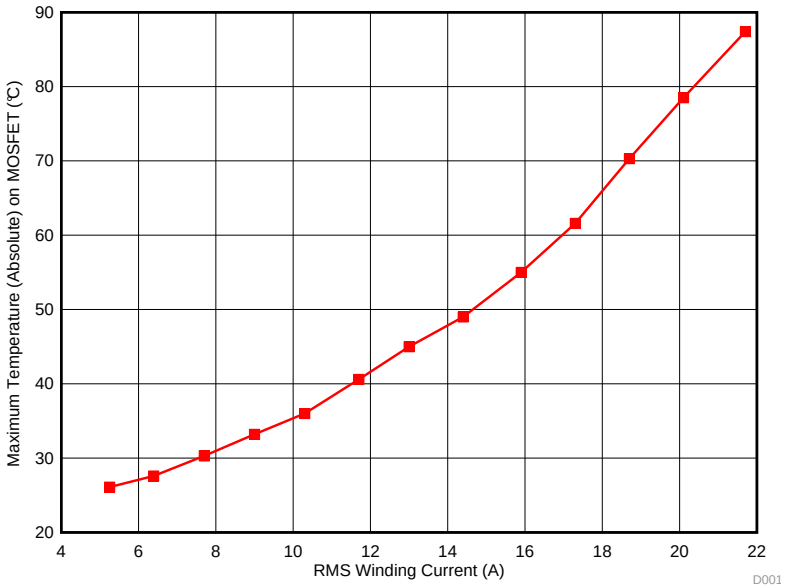


Figure 42. Maximum Steady State Temperature on FET With Different Winding Current

8.3 Inverter Efficiency Test

The inverter efficiency is experimentally tested with a load setup as shown in Figure 17. The test results are tabulated in Table 5 and the efficiency variation with inverter output is shown in Figure 43.

Table 5. Inverter Efficiency Test Results

INPUT DC VOLTAGE (V)	INPUT DC CURRENT (A)	RMS WINDING CURRENT (A)	DC INPUT POWER (W)	INVERTER OUTPUT POWER (W)	INVERTER EFFICIENCY (%)
10.754	5.224	4.265	54.46	53.64	98.50
10.809	8.292	6.810	88.76	87.28	98.33
10.739	11.668	9.587	124.60	121.96	97.88
10.797	15.082	12.417	162.00	158.20	97.65
10.772	18.470	15.228	197.80	192.36	97.25
10.772	21.858	18.044	233.89	227.20	97.14
10.768	24.424	20.175	260.98	253.40	97.10

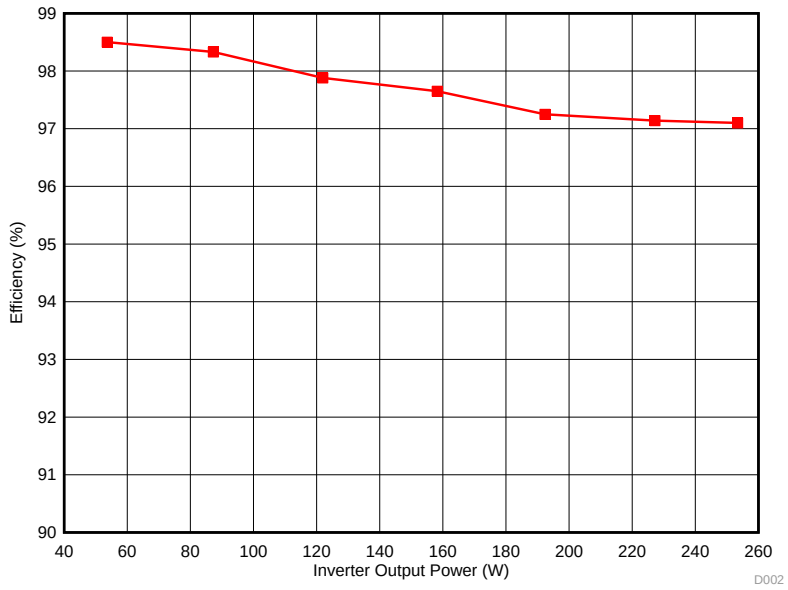


Figure 43. Inverter Efficiency vs Output Power

8.4 Effect of Gate Current on Inverter Efficiency

The source and sink gate current affect the performance of the inverter. The switching loss in the MOSFETs can be reduced by increasing the gate current. The IDRIVE capability of DRV8305 helps to achieve the maximum inverter efficiency by reducing the switching losses. Figure 44 and Figure 45 show the thermal image of the board when it is delivering 20-A_{RMS} to the motor winding at 90% duty cycle and at a 10.8-V DC supply. The MOSFETs are switching at 20 kHz. Figure 44 shows the steady state thermal image of the board (after 15 minutes of continuous running), when the gate drive source and sink current is set at 1 A. Figure 45 shows the steady state thermal image of the board (after 15 minutes of continuous running), when the gate drive source current is set at 125 mA and the sink current is set at 80 mA. The temperature rise is more with lower gate current setting because of more switching losses. The I_{DRIVE} feature of the DRV8305 helps to optimize the gate current, which gives the best efficiency.

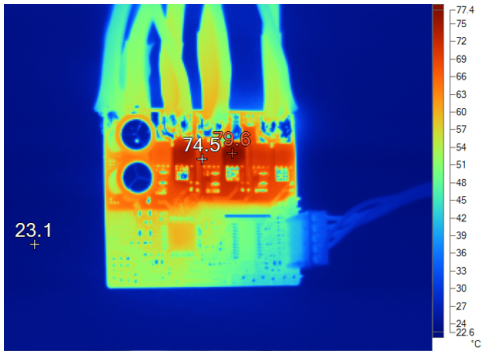


Figure 44. Steady State Thermal Image of Board When Gate Drive Source and Sink Current are Set to 1 A

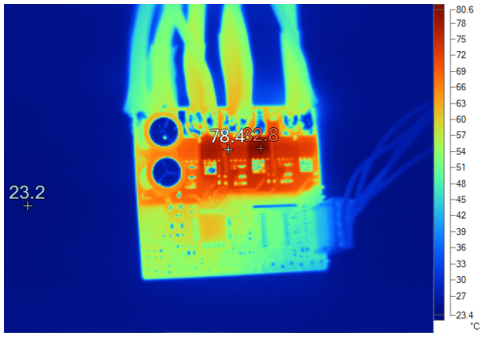


Figure 45. Steady State Thermal Image of Board When Gate Drive Source Current is Set at 125 mA and Sink Current is Set at 80 mA

8.5 Thermal Rise Test

In power tool applications, the peak current capability for short duration of time is important to drive the motor to deliver peak torque. Figure 46 shows the temperature rise of the MOSFETs with time when the board is delivering 20 A_{RMS} to the winding. The results are taken at an ambient temperature of 22°C. The curve shows that the steady state absolute temperature observed on the FET is 80°C. It means that the board can deliver 20 A_{RMS} continuously even at an ambient temperature of 55°C and the MOSFET junction temperature will be in the safe operating limit.

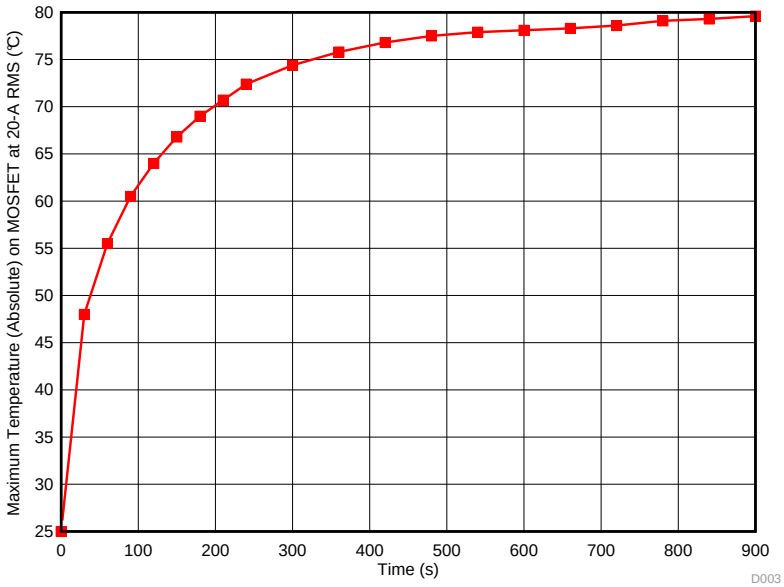


Figure 46. MOSFET Temperature Rise at 10.8-V DC Input, 20-A_{RMS} Winding Current, 100% Duty Cycle

Figure 47 shows the temperature rise of the MOSFETs with time when the board is delivering 25-A_{RMS} to the winding. The results are taken at an ambient temperature of 22°C. The curve shows that the steady state absolute temperature observed on the FET is 117°C. The results show that the board can deliver 25-A_{RMS} continuously at an ambient of temperature of 22°C. But at a higher ambient temperature, for example 55°C, the board can deliver 25-A_{RMS} for almost 1 minute and the FET junction temperature will be in a safe operating limit.

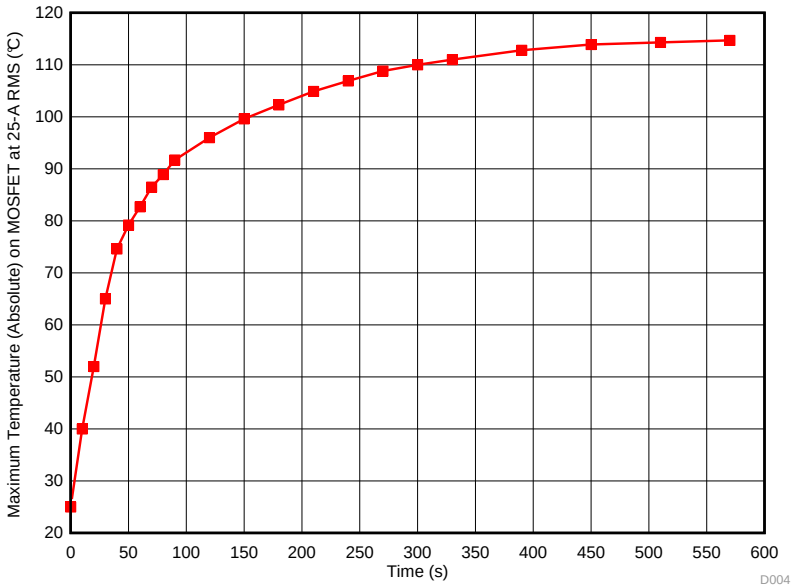


Figure 47. MOSFET Temperature Rise at 10.8-V DC Input, 25-A_{RMS} Winding Current, 100% Duty Cycle

Figure 48 shows the temperature rise of the MOSFETs with time when the board is delivering 30 A_{RMS} to the winding. The results are taken at an ambient temperature of 22°C. The results show that at a higher ambient temperature, for example 55°C, the board can deliver 30-A_{RMS} for almost 30 seconds and the FET junction temperature will be in a safe operating limit.

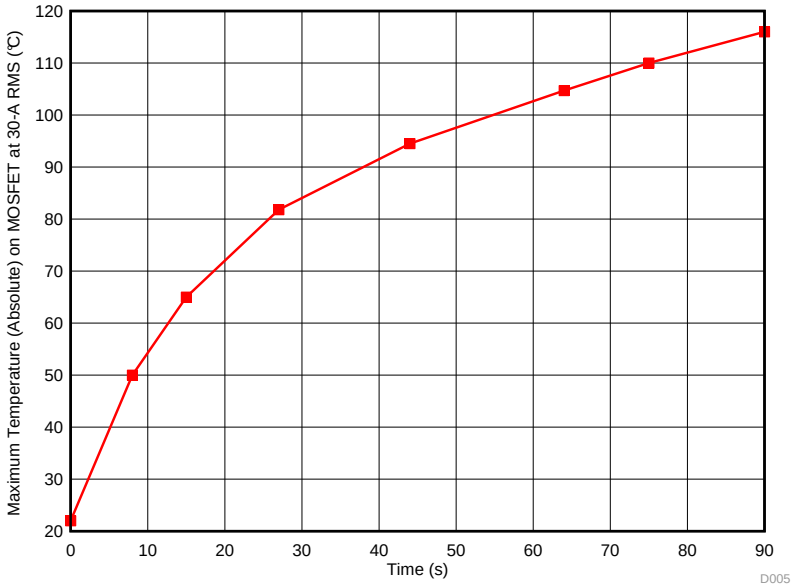


Figure 48. MOSFET Temperature Rise at 10.8-V DC Input, 30-A_{RMS} Winding Current, 100% Duty Cycle

8.6 Overcurrent and Short Circuit Protection Test

8.6.1 Effect of Amplifier Blanking Time in Current Sensing

In BLDC motor current sensing using shunt resistors, the sense resistor voltage can have transient noise voltage due to reasons such as:

- Inductive coupled noise when the MOSFETs are switching
- Voltage drop across the small inductance of the sense resistors during high di/dt

The DRV8305 current sense amplifiers have programmable blanking time at the amplifier outputs. The blanking time is implemented from any rising or falling edge of gate drive outputs. The blanking time is applied to all three current sense amplifiers equally. In case the current sense amplifiers are already being blanked when another gate driver rising or falling edge is seen, the blanking interval will be restarted at the edge. Note that the blanking time options do not include delay from internal amplifier loading or delays from the trace or component loads on the amplifier output. The programmable blanking time may be overridden to have no delay (default value).

Figure 49 and Figure 50 show the noise rejection in current sense amplifiers by using the blanking time feature of DRV8305 current sense amplifier.

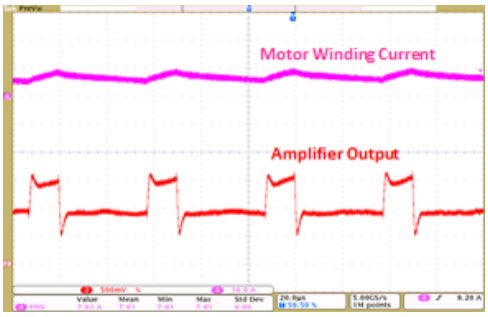


Figure 49. Amplifier Output Without Blanking

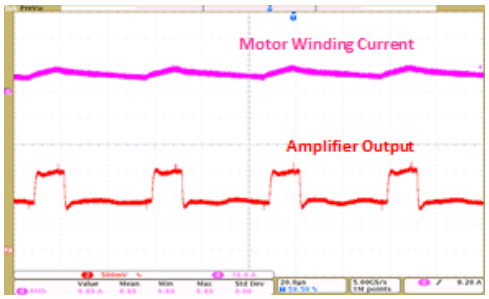


Figure 50. Amplifier Output With 500-ns Blanking

8.6.2 Cycle-by-Cycle Overcurrent Protection

Figure 51 and Figure 52 show the overcurrent test results with the following configurations and the motor is loaded to draw high current:

- Amplifier gain (G) = 40
- Amplifier blanking time = 500 ns
- Offset reference in DRV8305 (V_{REF}/k)= 0.825 V
- Comparator reference (V_{COMP_REF})= 1.6 V
- Shunt resistance (R_{SENSE}) = 0.5 mΩ

The theoretical overcurrent limit (I_{CL}) can be found using Equation 9.

$$I_{CL} = \frac{\left(V_{COMP\_REF} - \left(\frac{V_{REF}}{k}\right)\right)}{R_{SENSE} \times G} \tag{9}$$

$$I_{CL} = \frac{1.6 - 0.825}{0.0005 \times 40} = 38.75 \text{ A}$$

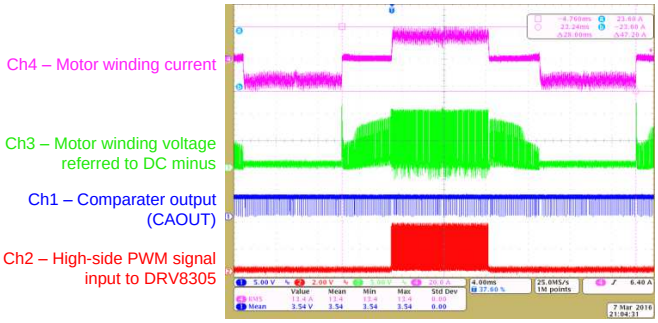


Figure 51. Cycle-by-Cycle Overcurrent Protection by Loading

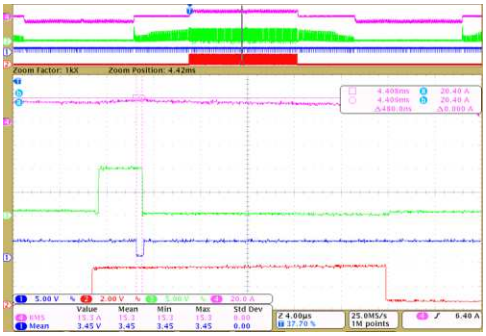


Figure 52. Response Time of Cycle-by-Cycle Overcurrent Protection

Figure 52 shows a zoomed-in view of Figure 51; once the comparator output goes low, the high-side PWM is immediately turned off by the buffer even though the PWM signal is high at the output of the MCU. The response time from the comparator goes low to the high-side switch turning off is less than 1 µs.

8.6.3 Cycle-by-Cycle Stall Current Protection

Figure 53 shows the test setup to simulate a stall current. The inverter output is shorted with thick wire. Shorting the inverter output terminals would cause a high current to be generated in the power stage. The high current is seen in the top-side MOSFET of a single leg and the bottom-side MOSFET of another leg. This situation would be similar to a stall condition where high current would exist in the motor limited only by the motor resistance.

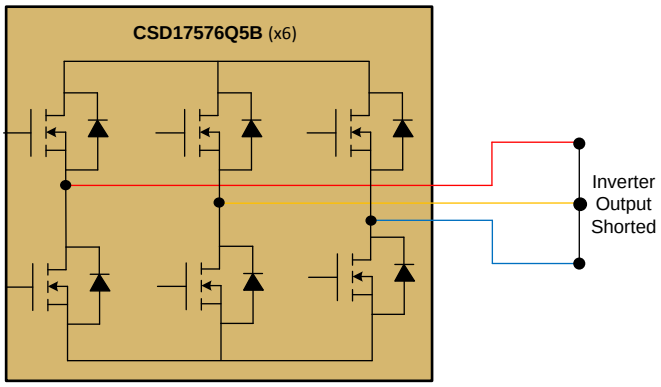


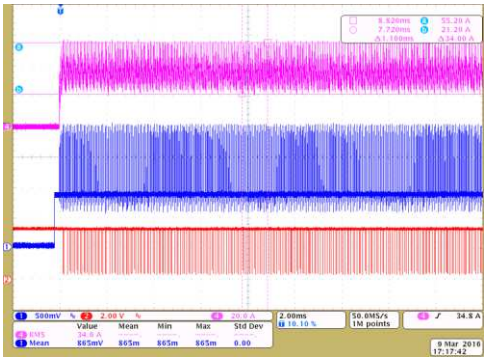
Figure 53. Test Setup to Simulate Stall Current With Inverter Output Shorted

Figure 54 and Figure 55 show the overcurrent test results with the following configurations:

- Amplifier gain (G) = 20
- Amplifier blanking time = 500 ns
- Offset reference in DRV8305 (V_{REF}/k) = 0.825 V
- Comparator reference (V_{COMP_REF}) = 2 V
- Shunt resistance (R_{SENSE}) = 0.5 mΩ

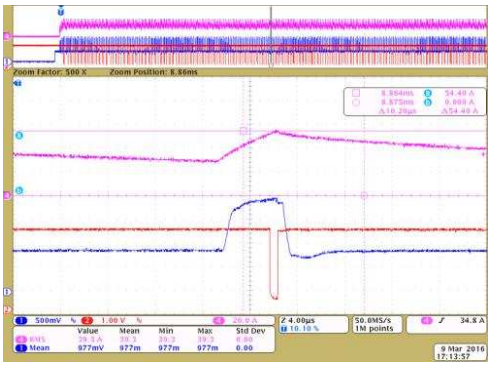
Using Equation 9, the theoretical overcurrent limit is

$$I_{CL} = \frac{2 - 0.825}{0.5 \times 0.001 \times 20} \approx 110 \text{ A}$$



Ch1 – Comparator output (CAOUT)
Ch2 – High-side PWM signal input to DRV8305
Ch4 – Motor winding current

Figure 54. Cycle-by-Cycle Overcurrent Protection With Inverter Output Shorted



Ch1 – Comparator output (CAOUT)
Ch2 – High-side PWM signal input to DRV8305
Ch4 – Motor winding current

Figure 55. Zoomed-In View of Cycle-by-Cycle Overcurrent Protection With Inverter Output Shorted

Figure 55 shows a zoomed-in view of Figure 54; once the amplifier output reaches 2 V, the comparator output goes low and the high-side PWM is immediately turned off by the buffer.

NOTE: Under short-circuit condition, the rate of change of current is very high. In this case, from the current waveform, the current is raising to 54 A in approximately 8 µs. The inductance of the sense resistor creates additional voltage across the sense resistor at such high di/dt and affects the op amp output. Calculate the reference threshold for current limit by considering the inductance of the sense resistor also.

Figure 56 shows the test setup to simulate a stall current when the motor is rotating. S1 is a single-throw, double-pole switch connect between the motor terminals. This is used to create a motor winding to a winding short.

Before S1 is closed, the motor was rotating at a steady speed. Figure 57 and Figure 58 show the waveforms obtained when the switch S1 is closed. When S1 is closed, S1 carries the short circuit current; the maximum value of the short circuit current is approximately 38 A. During this condition the motor stops, which causes the Hall state to continue at the current commutation state; therefore, the controller continues to generate the PWM corresponding to this commutation state.

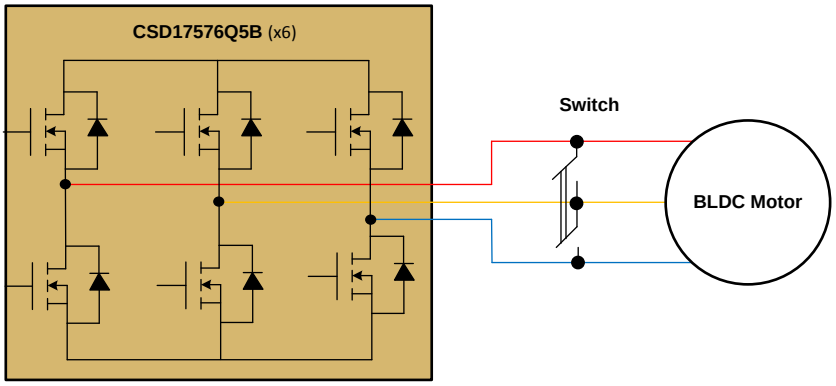


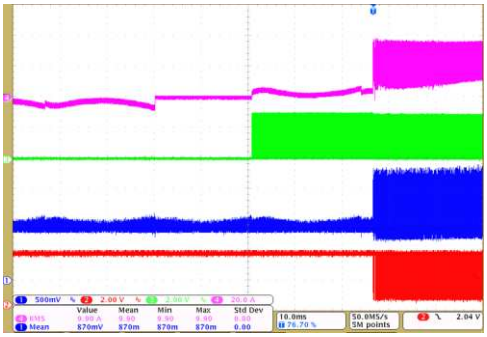
Figure 56. Test Setup to Simulate Stall Current When Motor is Running

Figure 57 and Figure 58 show the test results with the following configurations:

- Amplifier gain (G) = 20
- Amplifier blanking time = 500 ns
- Offset reference in DRV8305 (V_{REF}/k) = 0.825 V
- Comparator reference (V_{COMP_REF}) = 1.6 V
- Shunt resistance (R_{SENSE}) = 0.5 mΩ

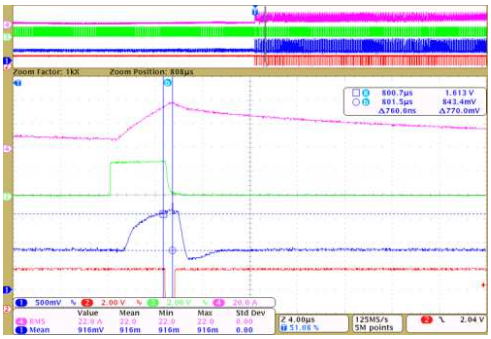
Using Equation 9, the theoretical over current limit is

$$I_{CL} = \frac{1.6 - 0.825}{0.5 \times 0.001 \times 20} \approx 77\,A$$



Ch1 – Comparater output (CAOUT)
Ch2 – High-side PWM signal input to DRV8305
Ch3 – Motor winding voltage referred to DC minus
Ch4 – Motor winding current

Figure 57. Cycle-by-Cycle Overcurrent Protection With Motor Stall



Ch1 – Comparater output (CAOUT)
Ch2 – High-side PWM signal input to DRV8305
Ch3 – Motor winding voltage referred to DC minus
Ch4 – Motor winding current

Figure 58. Zoomed-In View of Cycle-by-Cycle Overcurrent Protection With Motor Stall

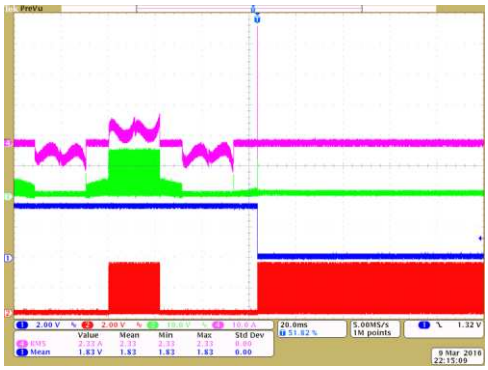
Figure 58 shows a zoomed-in view of Figure 57, once the amplifier output reaches 1.6 V, the comparator output goes low and the high-side PWM is immediately turned off by the buffer. The response time from the comparator goes low to the high-side switch turn off is less than 1 µs.

8.6.4 Stall Current Latch Protection by DRV8305 V_{DS} Sensing

The same test setup in Figure 56 is used for the stall current protection. The V_{DS} reference used is 0.123 by writing in the register of the DRV8305. The latch protection acted at 38.2 A.

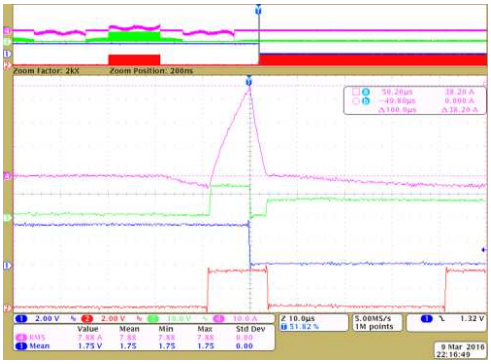
```
WriteRegister(0x0C, (VDS_LEVEL_0D123V + VDS_MODE_LATCH));
```

Figure 59 shows the test results with latch protection by V_{DS} sensing. When a V_{DS} overcurrent event occurs, the device will pull all gate drive outputs low to put all six external MOSFETs into high impedance mode. The fault will be reported on the nFAULT pin with the specific MOSFET in which the overcurrent event was detected is reported through the SPI status registers.



Ch1 – Comparator output (CAOUT)
Ch2 – High-side PWM signal input to DRV8305
Ch3 – Motor winding voltage referred to DC minus
Ch4 – Motor winding current

Figure 59. Overcurrent Latch Protection With Motor Stall by V_{DS} Sensing



Ch1 – Comparator output (CAOUT)
Ch2 – High-side PWM signal input to DRV8305
Ch3 – Motor winding voltage referred to DC minus
Ch4 – Motor winding current

Figure 60. Zoomed-In View of Overcurrent Latch Protection With Motor Stall by V_{DS} Sensing

Figure 61 shows the test results of latch protection, when the inverter output is shorted. The same test setup in Figure 56 is used for the short circuit simulation. The V_{DS} reference used is 0.175 V by writing in the register of the DRV8305. The latch protection acted at 73 A.

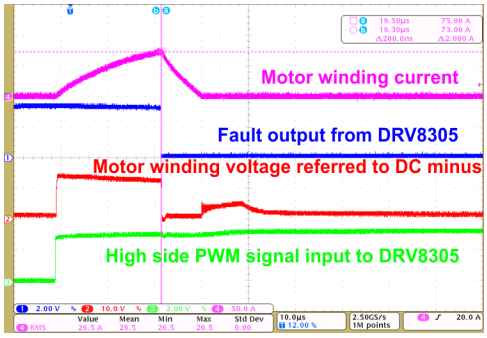


Figure 61. Overcurrent Latch Protection With Inverter Output Shorted

8.7 Testing With External Airflow

The board is tested with external airflow. The test setup and direction of air flow is shown in Figure 62. The maximum temperature observed on the MOSFETs at different winding currents is shown in Figure 63. The testing is done at different airflow from no forced airflow, 100 to 500 LFM. The board can continuously deliver 30 A at a 500-LFM airflow and the steady state maximum temperature on the MOSFET is approximately 90°C. The testing is done at an ambient temperature of 23°C.

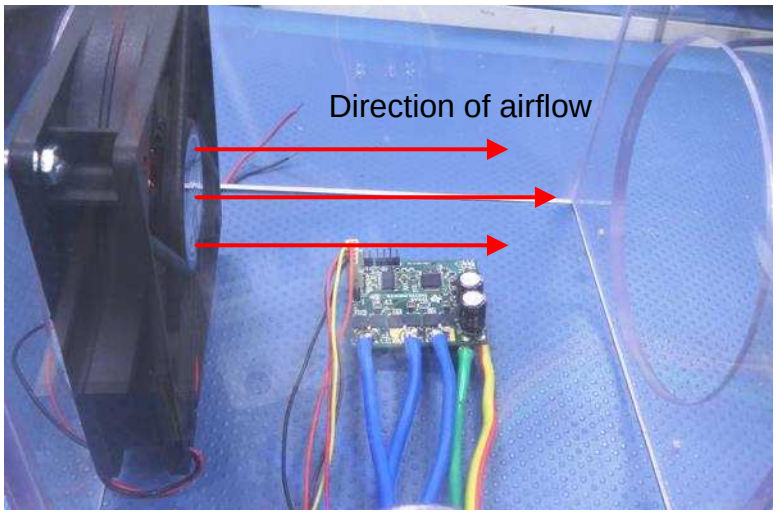


Figure 62. Test Setup and Direction of Airflow

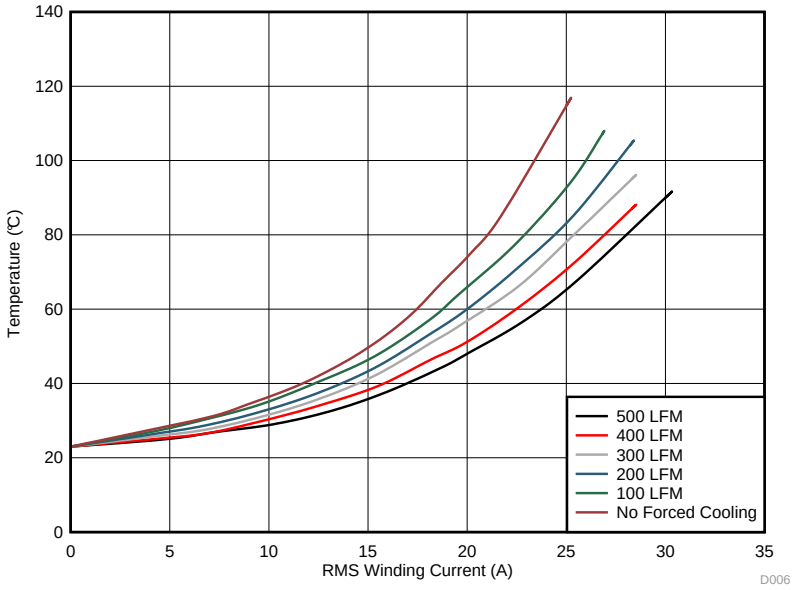


Figure 63. Maximum Steady State Temperature on MOSFETs With Different Airflow

8.8 Testing for Peak Current Capability

The board is tested with 70-A peak current for 1 second. Figure 64 shows the winding current of 73.6 A when the motor is stalled for 1.4 seconds. Figure 65 shows the thermal image of the board after 1.4 seconds. The high peak current capability ensures that in power tool applications, the power stage aids the motor to deliver high peak torque. If the stall current continues to be high, over temperature or blocked rotor protection will act to shut off the system.

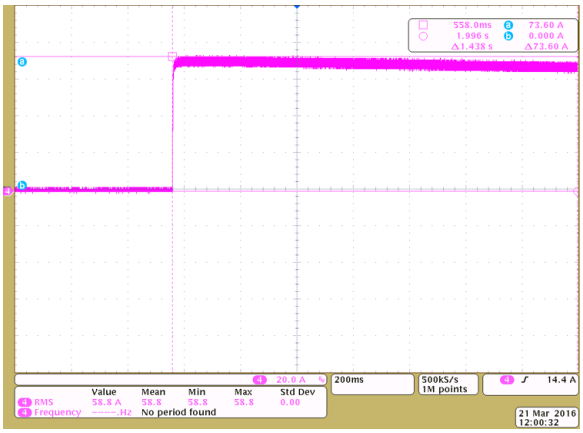


Figure 64. 73.6-A Peak Current in Motor Winding During Motor Stall

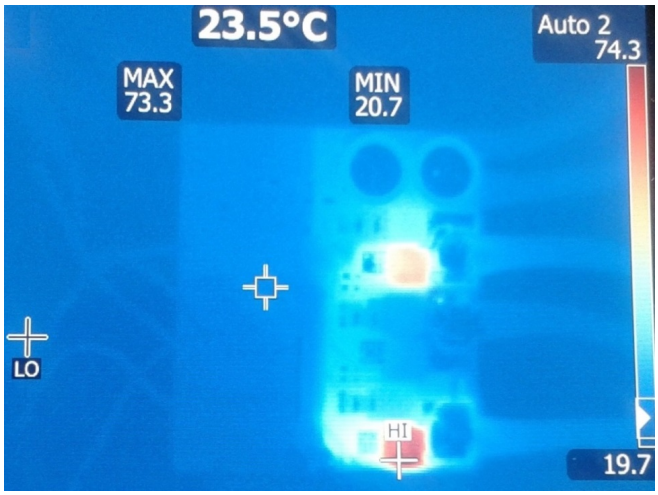


Figure 65. Thermal Image of Board After 1.4 Seconds With 73.6-A Peak Current in Motor Winding

9 Design Files

9.1 Schematics

To download the schematics, see the design files at TIDA-00771.

9.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00771.

9.3 PCB Layout Recommendations

Use the following layout recommendations when designing a PCB for the DRV8305. An example layout is given in Figure 66.

- Connect the DVDD and AVDD 1-µF bypass capacitors directly to the adjacent GND pin to minimize loop impedance for the bypass capacitor.
- Place the CP1 and CP2 0.047-µF flying capacitors directly next to the DRV8305 charge pump pins.
- Place the VCPH 2.2-µF and VCP_LSD 1-µF bypass capacitors close to their corresponding pins with a direct path back to the DRV8305 GND net.
- Place the PVDD 4.7-µF bypass capacitor as close as possible to the DRV8305 PVDD supply pin.

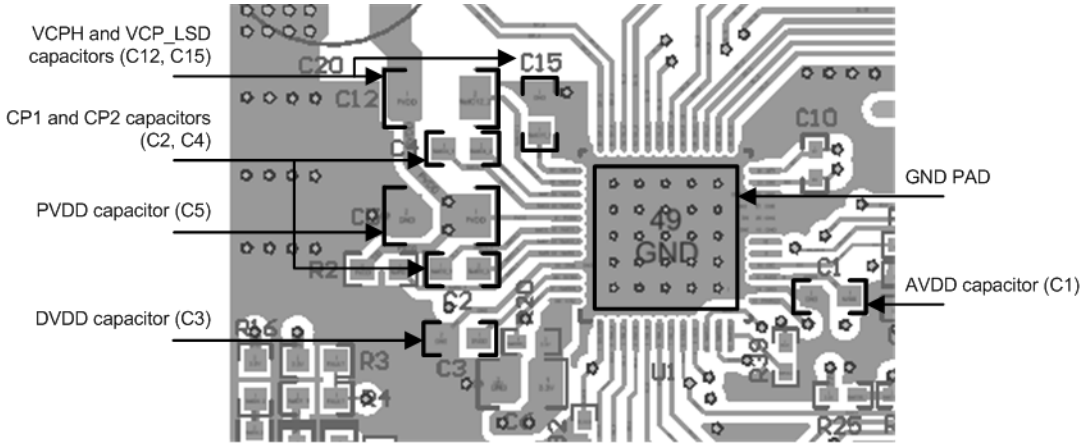


Figure 66. Layout Recommendations for Decoupling Capacitors of DRV8305

- Minimize the loop length for the high-side and low-side gate drivers. The high-side loop is from the DRV8305 GH_X to the power MOSFET and returns through SH_X. The low-side loop is from the DRV8305 GL_X to the power MOSFET and returns through SL_X. Example layout is shown in Figure 67.

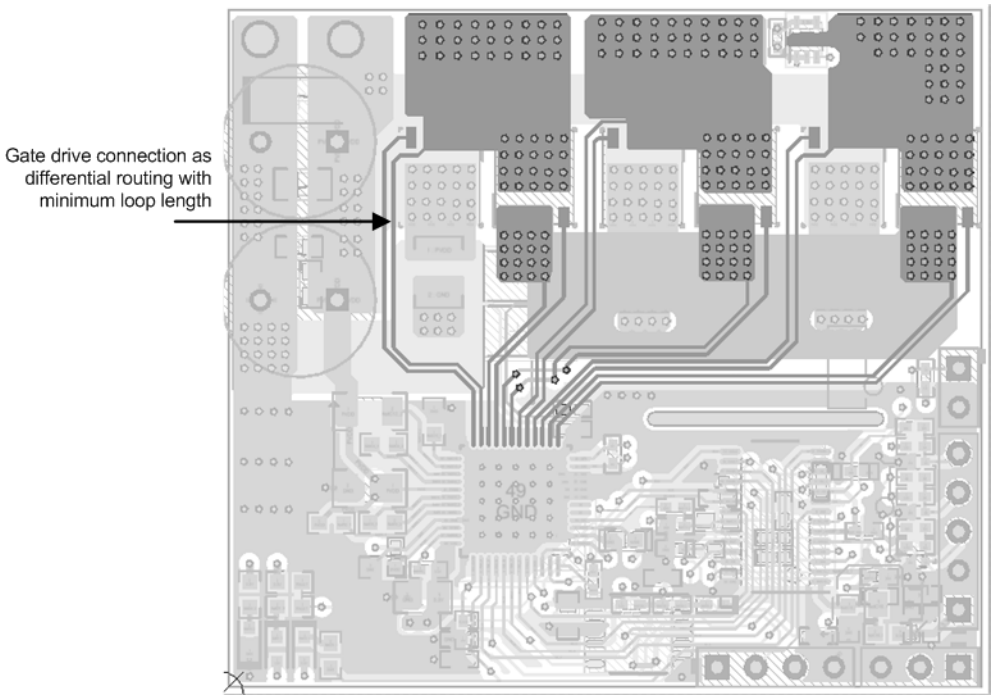


Figure 67. Gate Drive Connection From DRV8305 as Differential Routing With Minimum Loop Length

- Route the track for sensing the V_{DS} of the MOSFET as a differential track.
- In the reference design, the PCB is a four-layer layout with 2-oz (70-micron) copper thickness in every layer. The power tracks are made wide to carry a high current. Figure 68 shows the current carrying track from the power input point. The tracks are repeated in different layers and are connected by arrays of stitching vias.
- A GND star point is defined in the PCB from where the GND path for the DRV8305 and other signal circuits in the board is tapped.

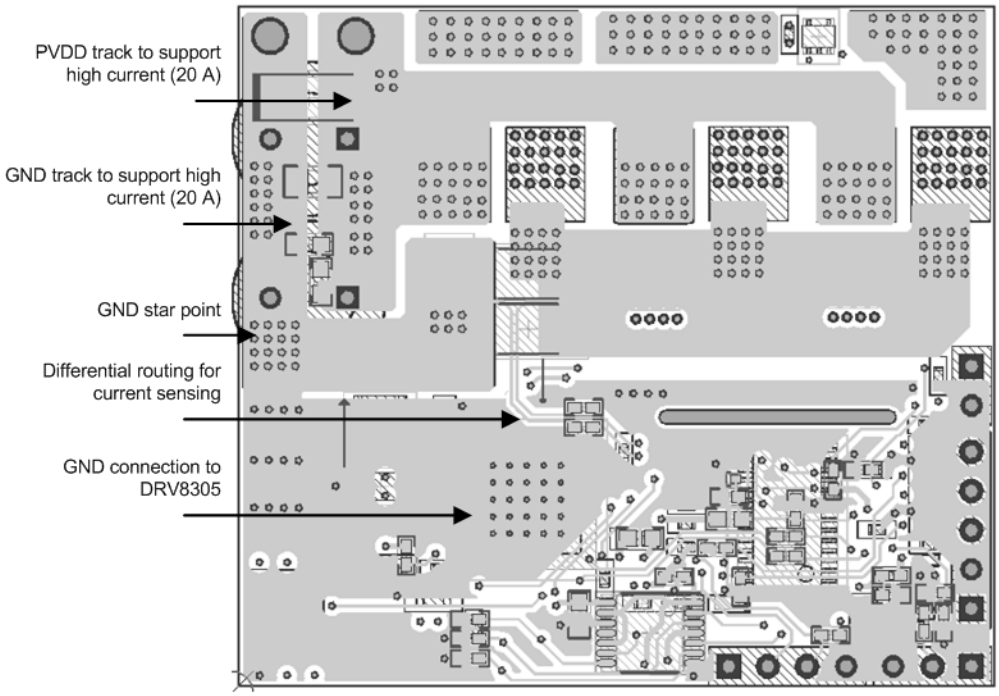


Figure 68. Bottom Layer of PCB Showing Power Tracks and GND Star Connection

- For better thermal dissipation from the MOSFET to the PCB, increase the copper area around the MOSFET pad as much as possible. Use arrays of vias under the drain pad of the MOSFET, which will dissipate heat better through the bottom surface copper area. Add a small heat sink or copper bars to the bottom surface of PCB to aid heat dissipation.
- Carefully consider the placement of the decoupling capacitors. Place these capacitors near to each MOSFET. The return path of the decoupling capacitors should be through a thick track, and the return path length should be as short as possible to improve the decoupling.

- Use the slot provided in the PCB above the MCU to limit the heat spread to the MCU as shown in Figure 69.

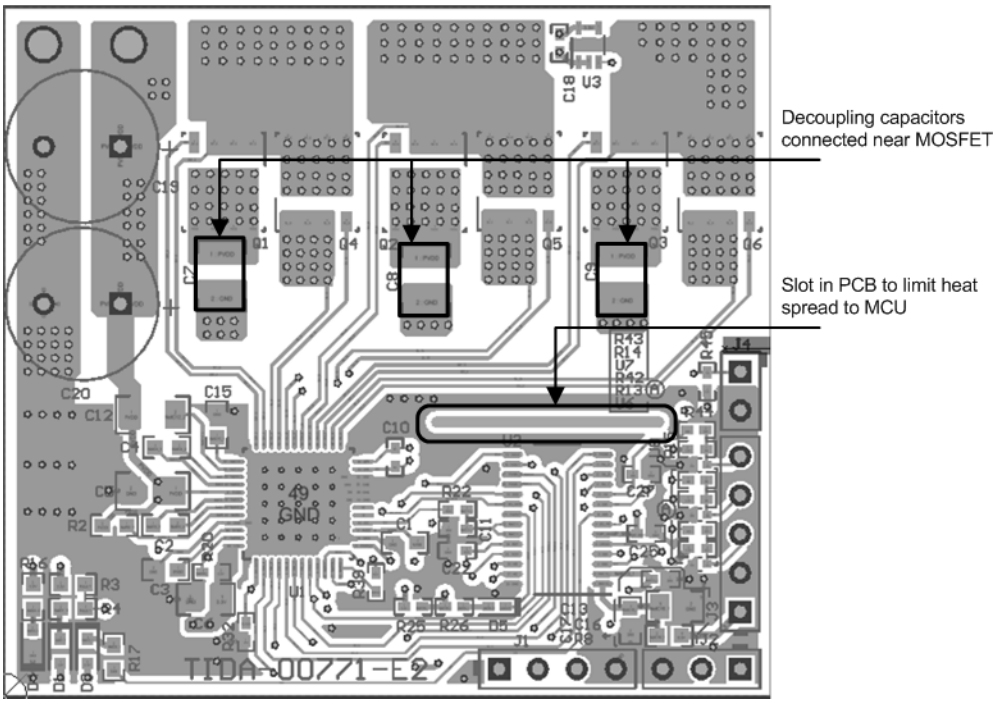


Figure 69. Placement of Decoupling Capacitors for Inverter Legs

- The board has the provision for the bottom side heat sink. Use a thermally conductive and electrically insulated thermal pad between the PCB bottom side and heat sink. Figure 70 shows the space for the bottom side heat sink.

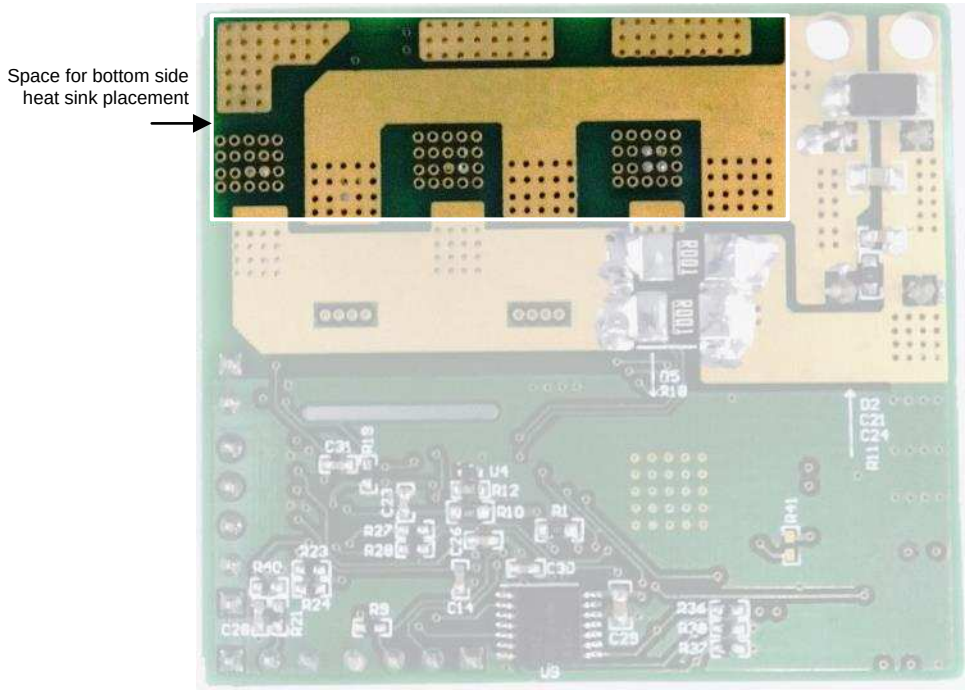


Figure 70. Space for Bottom-Side Heat Sink

9.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-00771.

9.4 Altium Project

To download the Altium project files, see the design files at TIDA-00771.

9.5 Gerber Files

To download the Gerber files, see the design files at TIDA-00771.

9.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-00771.

10 Software Files

To download the software files, see the design files at TIDA-00771.

11 References

1. Texas Instruments, *Understanding IDRIVE and TDRIVE in TI Motor Gate Drivers*, DRV8305 Application Report (SLVA714)
2. Texas Instruments, *Sensored 3-Phase BLDC Motor Control Using MSP430*, MSP430G2553 Application Report (SLAA503)

12 Terminology

SPI— Serial Peripheral Interface

PWM— Pulse Width Modulation

BLDC— Brushless DC motor

MCU— Microcontroller unit

FETs, MOSFETs—Metal–oxide–semiconductor field-effect transistor

ESD— Electrostatic Discharge

RPM— Rotation per Minute

RMS— Root Mean Square

13 About the Author

MANU BALAKRISHNAN is a systems engineer at Texas Instruments where he is responsible for developing subsystem design solutions for the Industrial Motor Drive segment. Manu brings to this role his experience in power electronics and analog and mixed signal designs. He has system level product design experience in permanent magnet motor drives. Manu earned his bachelor of technology in electrical and electronics engineering from the University of Kerala and his master of technology in power electronics from National Institute of Technology Calicut, India.

Revision A History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (April 2016) to A Revision	Page
• Changed from preview page	1

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