TI Designs

16-Bit 1-MSPS Data Acquisition System With Isolated Inputs for High-Voltage Common-Mode Rejection

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Design Resources

TIDA-00106	Tool Folder Containing Design Files
TINA-TI™	SPICE Simulator
ADS8681	Product Folder
ISO7640	Product Folder
SN74AUC17	Product Folder
SN6501	Product Folder
TPS7A4901	Product Folder
TPS22929	Product Folder
TLV3012	Product Folder

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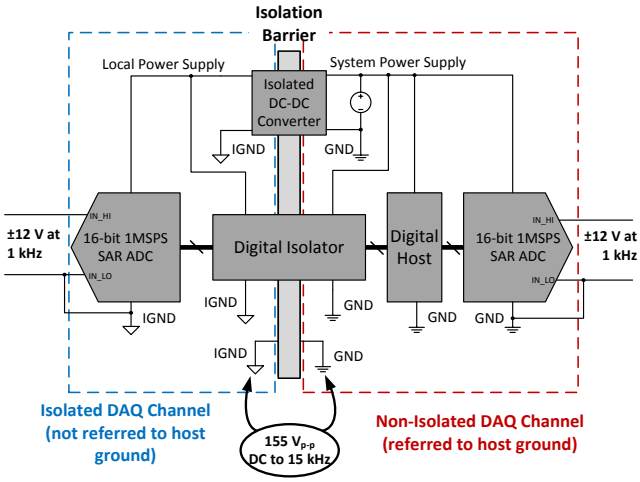
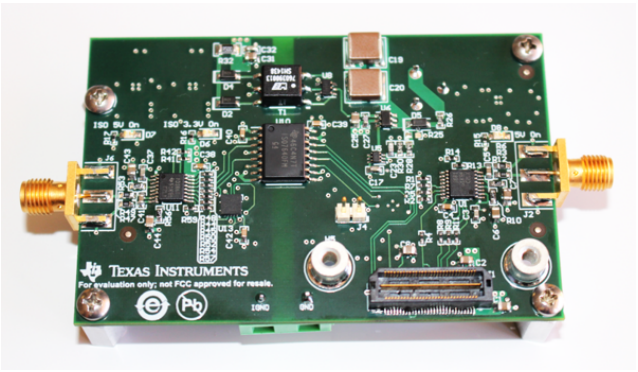
Circuit Description

The circuit represents a high-performance data acquisition (DAQ) solution suitable for processing input signals (up to ±12 V) superimposed on large common-mode offsets (tested up to 155 V_{p-p} from dc to approximately 15 kHz) relative to the ground potential of the systems main power supply. Common-mode rejection is achieved by generating an isolated power supply to allow the analog signal chain to float with the input common-mode signal. The analog signal chain consists of a high-performance, 16-bit, 1-MSPS SAR ADC with an integrated analog front end (AFE) offering high input impedance and a wide ±12-V input voltage range. Relevant application areas include PLC analog input modules with channel-to-channel isolation, automotive battery pack monitoring, power monitoring in ac motor drives, thermocouple measurements, and so forth.





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1 Design Summary

The TIDA-00106 design consists of two separate data acquisition blocks or channels: a non-isolated channel powered by supplies that are referred to the same ground potential as the host controller (GND) and an isolated channel, which is powered by supplies that are referred to a potential IGND that floats relative to GND.

The functions of the design are to:

1. Measure the common-mode rejection ratio (CMRR) and ac performance of the isolated DAQ channel
2. Demonstrate that for valid dc common-mode (CM) signals the isolated DAQ block delivers the same ac performance as the non-isolated DAQ block

The test conditions are as follows:

- Input signal:
  - Non-isolated channel: ±12-V sinusoid at 1 kHz superimposed on dc common-mode signal
  - Isolated channel: ±12-V sinusoid at 1 kHz superimposed on 155-V_{p-p} (frequency swept between dc and 15 kHz) common-mode signal relative to the ground potential of the host controller
- Power supply:
  - Non-isolated channel: 5-V analog and 3.3-V digital relative to host controller ground (GND)
  - Isolated channel: 5-V analog and 3.3-V digital relative to the ground potential of the isolated power supply (IGND)

  ADC sampling rate: 1 MSPS on both isolated and non-isolated channels
- Digital I/O:
  - Non-isolated channel: Serial peripheral interface (SPI) over direct connection to host controller
  - Isolated channel: SPI over isolated interface to host controller

Table 1 summarizes the performance goals.

Table 1. Comparison of Design Goals and Measured Performance

PARAMETER	GOAL	ISOLATED CHANNEL	NON-ISOLATED CHANNEL
CMRR at ≤ 15-kHz f_{CM} (dB)	> 100	120	—
THD at 1-kHz f_{IN} (dBc)	≤ 104	–109 (with dc CM)	–108
SNR at 1-kHz f_{IN} (dBc)	> 90	91.6 (with dc CM)	91.7

Figure 1 and Figure 2 show the measured ac performance and CMRR characteristics of the isolated channel, respectively. The ac performance curve matches that of the non-isolated channel.

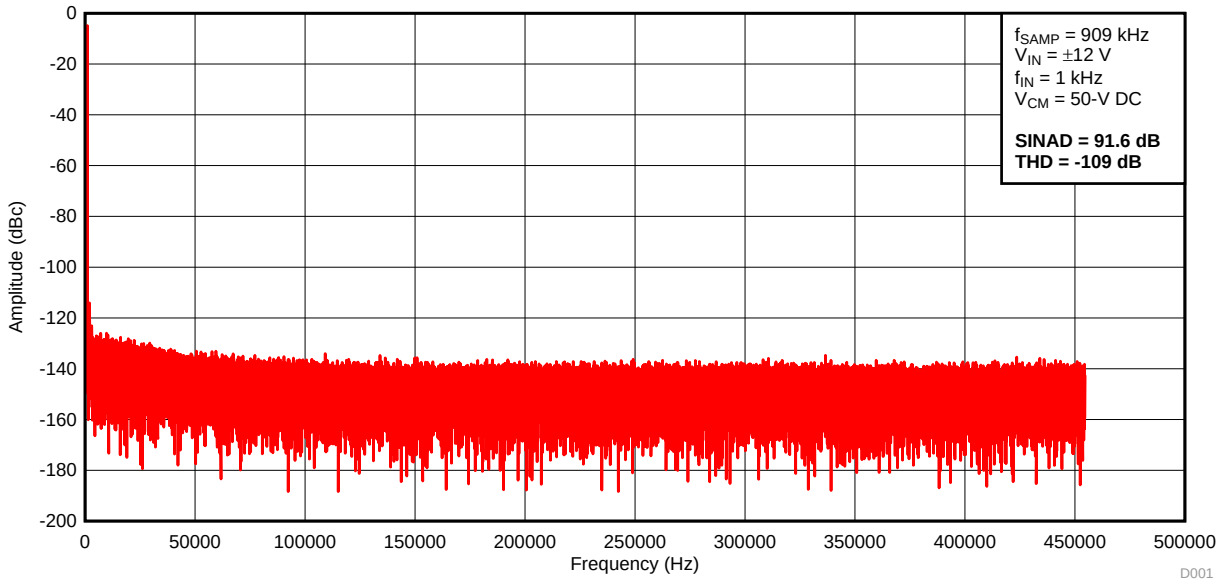


Figure 1. FFT of Isolated DAQ Channel Output and Measured AC Performance With DC Common Mode

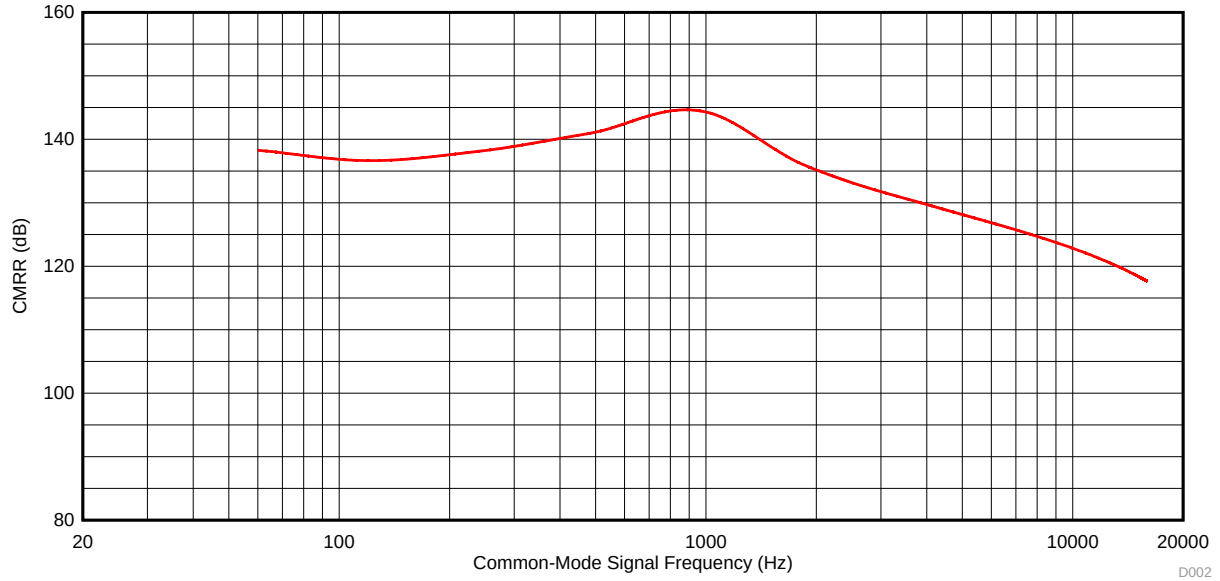
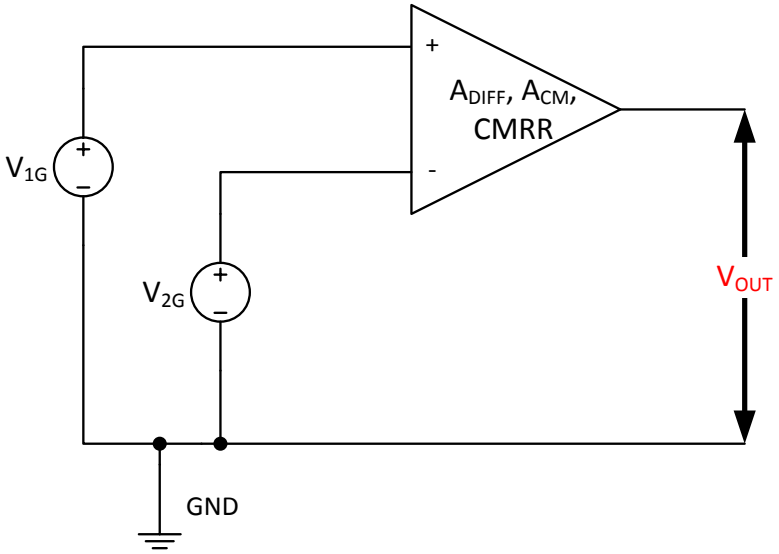


Figure 2. Measured CMRR of Isolated DAQ Channel for ≈155-V_{p-p} AC CM Signal

1.1 Equations

Figure 3 shows a generalized measurement system that takes a voltage input and provides a voltage output. V_{1G} and V_{2G} are non-zero single-ended voltages relative to a common reference point (GND) and V_{OUT} is the output of the system, which is also with respect to GND. Equation 1 through Equation 7 describe the input and output relationships of the system.



$V_{OUT} = V_{DIFF} \times A_{DIFF} + V_{CM} \times A_{CM}$

➔ $V_{OUT} = A_{DIFF} \times (V_{DIFF} + A_{CM}/A_{DIFF} \times V_{CM})$

$V_{OUT} = A_{DIFF} \times (V_{DIFF} + 1/CMRR \times V_{CM})$

Figure 3. Block Diagram of Generalized Voltage Measurement System

Differential voltage (V), $V_{DIFF} = V_{1G} - V_{2G}$ (1)

Common mode voltage (V), $V_{CM} = \frac{(V_{1G} + V_{2G})}{2}$ (2)

Common mode gain (V/V), $A_{CM} = \frac{\Delta V_{OUT}}{\Delta V_{CM}}$ (3)

Differential gain (V/V), $A_{DIFF} = \frac{\Delta V_{OUT}}{\Delta V_{DIFF}}$ (4)

Common mode rejection ratio, $CMRR = \frac{A_{DIFF}}{A_{CM}}$ (5)

CMRR in dB units, $CMRR\ (dB) = 20 \times \log_{10} CMRR$ (6)

Output voltage (V), $V_{OUT} = A_{DIFF} \times \left(V_{DIFF} + \frac{1}{CMRR} \times V_{CM} \right)$ (7)

2 Theory of Operation

2.1 Voltage-Mode Processing for Data Acquisition

Data acquisition systems (DAQs) primarily measure voltage signals. Many physical processes and sensors generate voltage outputs, but there are also those that generate current or resistance outputs. However, in general, current and resistance signals ultimately must be represented as proportional voltage signals at the inputs of analog-to-digital converters (ADCs). This representation is necessary because most ADCs use capacitors to store the instantaneous value of an input voltage signal for subsequent data conversion. Therefore, in general, driving the analog input of an ADC requires a voltage source.

For example, Figure 4 shows a typical current-sensing application that uses a resistor (known as a shunt) of a known value in the path of the current signal to generate a proportional voltage drop that is then measured by a DAQ. The value of the current is subsequently recalculated using the measured voltage drop and shunt resistance.

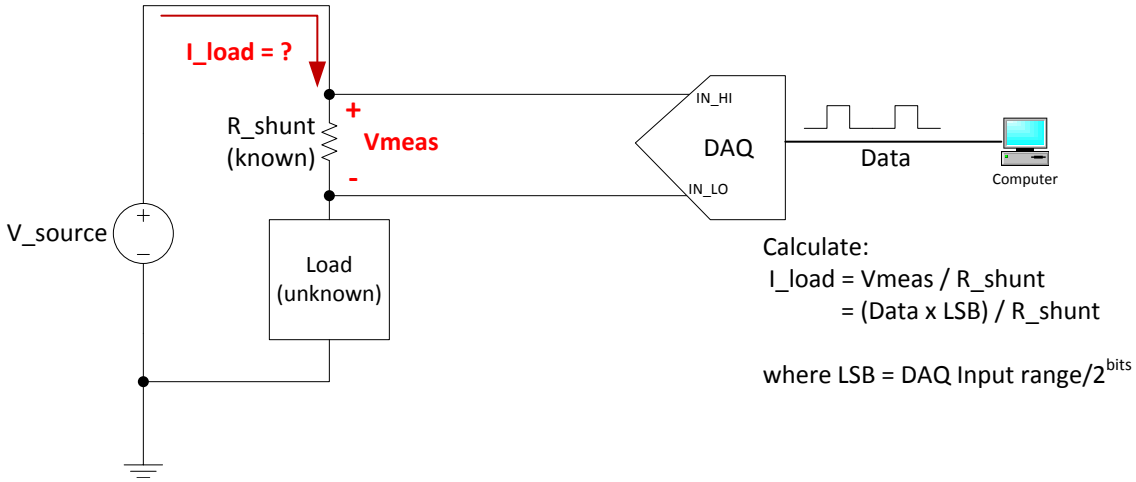


Figure 4. Current Measurement Using Shunt Resistor of Known Value

Another example is temperature measurement using temperature-dependent resistive elements such as thermistors or resistance temperature detectors (RTDs) as sensors. Resistance changes of the sensor over temperature are converted to voltage signals by passing a reference current (a known value) through the sensor. The resistance (and corresponding temperature) is then derived using the DAQ measurement of the voltage drop and the excitation current. Figure 5 shows a representative circuit diagram.

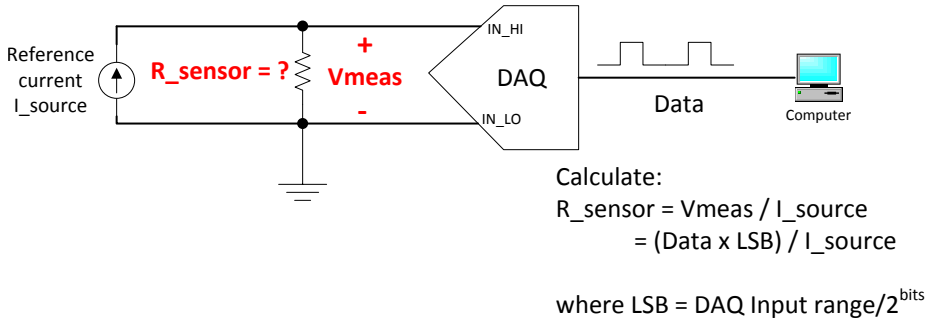


Figure 5. Temperature Measurement Using Resistive Sensor

Figure 4 and Figure 5 show a simplified, conceptual representation of the data acquisition process. In practice, making voltage measurements as shown is much more complex. The inputs of the DAQ module cannot be arbitrarily connected across any two points in a circuit because there are practical limits on how large the input common-mode voltage can be, as well as the common-mode rejection capability of the DAQ module. Violating these limits may lead to erroneous operation and even cause permanent damage to the device. To understand the meaning and significance of the common-mode voltage, it is important to first discuss the various ways in which a voltage signal can be presented to a DAQ system.

2.2 Types of Voltage Measurement: Single-Ended vs Differential

Voltage is always measured as a potential difference between two points in a circuit. A voltage measurement can be single-ended or differential depending on the signal of interest. If the signal of interest is the voltage between a single node and circuit ground (usually the low side of the signal source), the measurement is single-ended. Alternatively, if the signal of interest is between two circuit nodes, with neither one being circuit ground, then the measurement is differential. For example, Figure 4 shows a differential voltage measurement and Figure 5 shows a single-ended voltage measurement. Similarly, a voltage measurement across the load in the Figure 4 circuit can also be considered a single-ended measurement.

2.3 What is Common-Mode Voltage?

A common-mode voltage is a single-ended voltage and is generally more relevant when making a differential measurement. A differential measurement is essentially just the difference of the single-ended voltages at two nodes of interest in a circuit, as defined by Equation 1. The average value of the single-ended voltages is called the common-mode voltage (V_{CM}) as defined by Equation 2 and the term refers to the average amount by which each single-ended voltage is offset from the circuit ground. For a single-ended measurement, the common-mode voltage is the input signal itself. V_{CM} can be a dc or ac signal. V_{CM} is a dc signal when the single-ended signals have the same frequency and opposite phase and V_{CM} is ac when the single-ended signals differ in frequency or phase (see Figure 6).

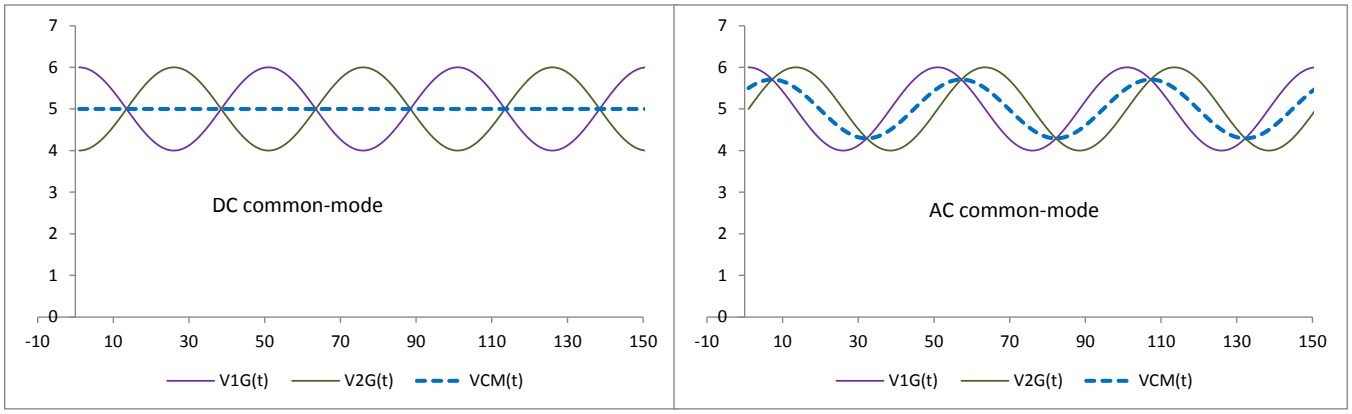


Figure 6. Common-Mode Voltage Can Be DC or AC

2.4 Why Reject Common-Mode Voltage?

The most important reason for rejecting the common-mode voltage is to provide the safety and reliability of the measurement system and its users. Every electronic device has absolute maximum and minimum ratings on the single-ended voltages that can be applied to its inputs. For long-term reliability, the single-ended voltages at the device inputs must lie within these limits at all times. As noted earlier, violating the absolute maximum ratings can cause irreversible damage to the device.

As an example, Figure 7 shows the *Absolute Maximum Ratings* section from the ADS8881 datasheet (SBAS547).

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
AINP to GND or AINN to GND		–0.3	REF + 0.3	V
AVDD to GND or DVDD to GND		–0.3	4	V
REF to GND		–0.3	5.7	V
Digital input voltage to GND		–0.3	DVDD + 0.3	V
Digital output to GND		–0.3	DVDD + 0.3	V
Operating temperature, T_A	ADS8881C	0	70	°C
	ADS8881I	–40	85	
Storage temperature, T_{stg}		–65	150	°C

Figure 7. Determining Absolute Maximum Ratings From Datasheet

AINP and AINN are the input pins of the ADS8881 device and for a valid reference voltage of 5 V, the safe operating range for AINP and AINN is –0.3 V to 5.3 V. Figure 8 shows a case where the signals on both input pins violate the absolute maximum ratings of the device.

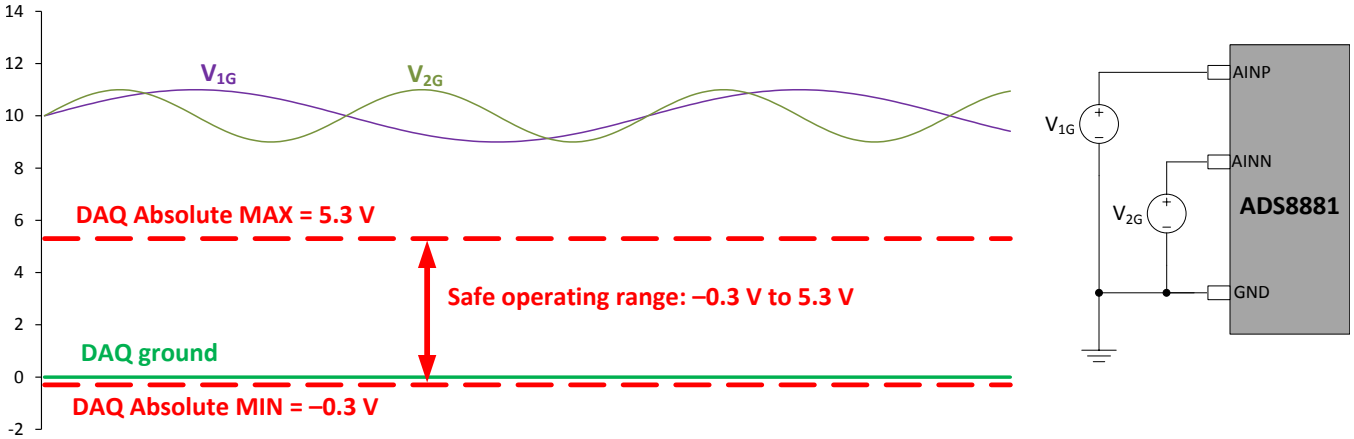


Figure 8. Single-Ended Inputs That Violate Absolute Maximum Ratings

Another important reason for rejecting the input common-mode voltage is measurement accuracy. Ideally, a differential measurement simply cancels out the common-mode signal at each time instant and preserves only the differential signal of interest in the system output. However, practical measurement systems have an input offset voltage (V_{OS}), which make the process of common-mode subtraction flawed and a corresponding output error is generated. More important to consider, however, is how V_{OS} varies with V_{CM}, thereby limiting the common-mode rejection of the system. In other words, the input offset voltage changes by ΔV_{OS} for a ΔV_{CM} change in the input common-mode voltage, as Figure 9 shows (which models a generic differential voltage measurement system). This change in V_{OS} causes the output error to increase by $\Delta V_{OUT} = A_{DIFF} \times \Delta V_{OS}$. As $\Delta V_{OUT} \neq 0$, the common-mode gain, $A_{CM} = \Delta V_{OUT} / \Delta V_{CM} \neq 0$ and therefore CMRR = A_{DIFF} / A_{CM} is finite. In summary, changes in the input common-mode produce output errors and minimizing these errors for a given input common-mode range requires improving the common-mode rejection capability of the system.

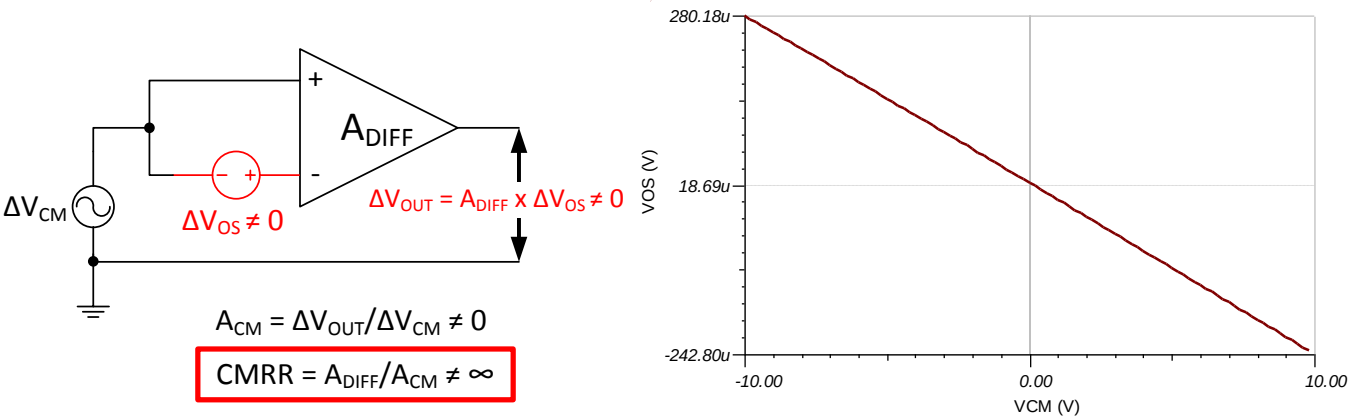


Figure 9. V_{OS} Varies With V_{CM} to Produce Finite CMRR

2.5 Quantifying Common-Mode Rejection Capability

The ability of a measurement system to reject the input common-mode signal is reflected by its common-mode rejection ratio (CMRR) specification, as defined by Equation 5 and Equation 6. As Section 2.4 addresses, practical measurement systems have a finite CMRR; nevertheless, a CMRR must be as high as possible to minimize input common-mode-related error components in the system output. Figure 10 shows the effect of a finite CMRR on the system output, as described by Equation 7.

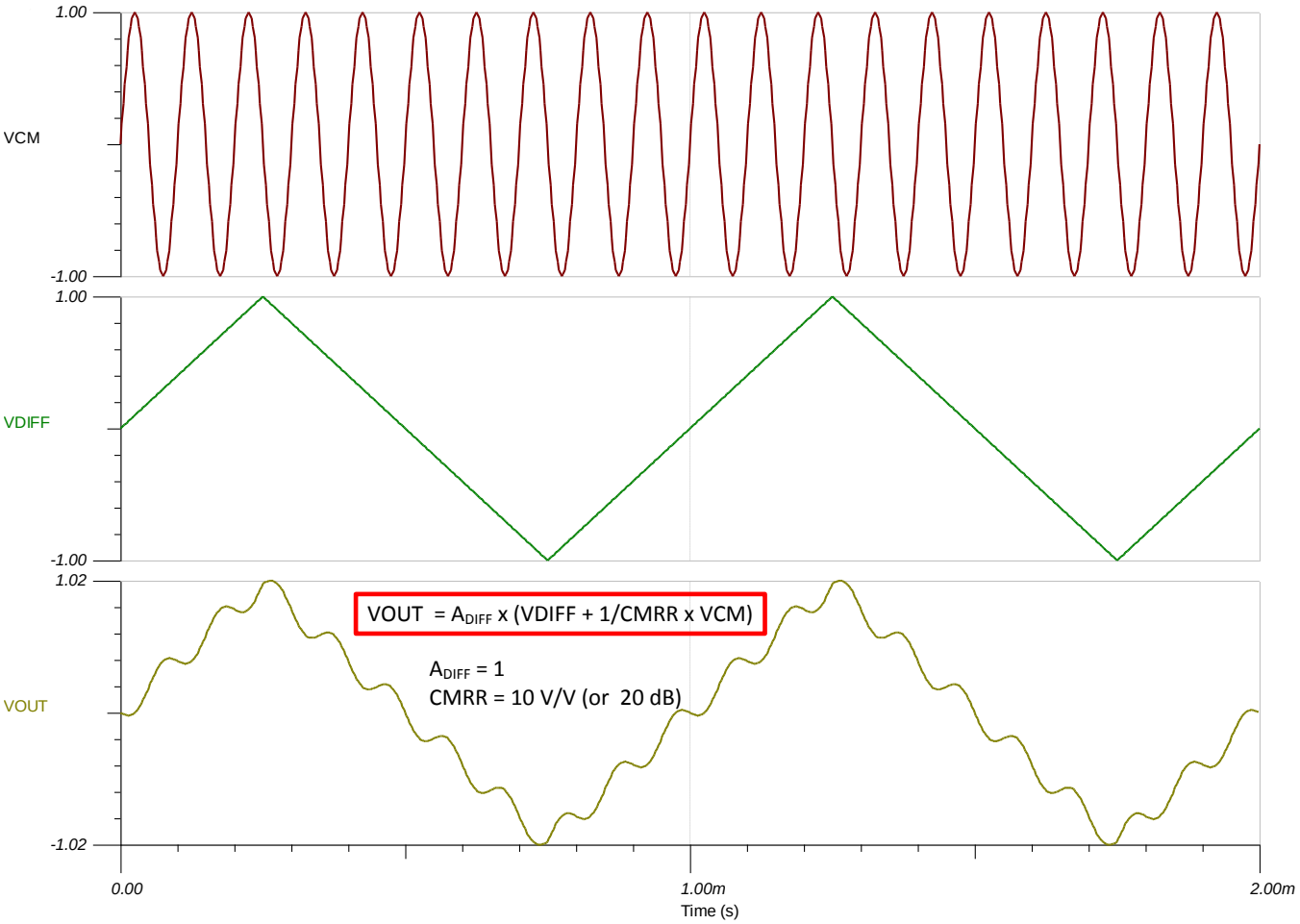


Figure 10. CMRR-Induced Output Error

Because common-mode signals can be dc or ac, CMRR is generally specified over frequency (see Figure 11). Most DAQ systems have a high CMRR at dc and show degradation as the common-mode frequency increases. Consequently, the system becomes more sensitive to any high frequency changes in the input common-mode signal and the error in the output signal increases.

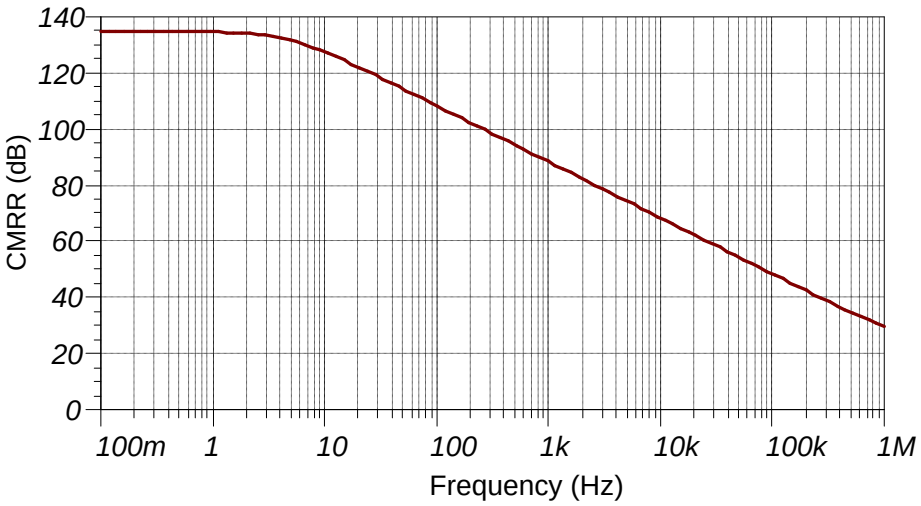


Figure 11. CMRR Typically Specified Over Frequency

2.6 Options for Rejecting High Common-Mode Voltages

This section discusses various options for rejecting large common-mode voltages. Suitability depends largely on the frequency content of the common-mode signal, which affects CMRR.

2.6.1 Difference Amplifier

Figure 12 shows a difference amplifier circuit in which the resistor dividers attenuate the single-ended inputs to fit into the valid input range of the op amp. The circuit then relies on the CMRR of the op amp to minimize the common-mode error component in the amplifier output.

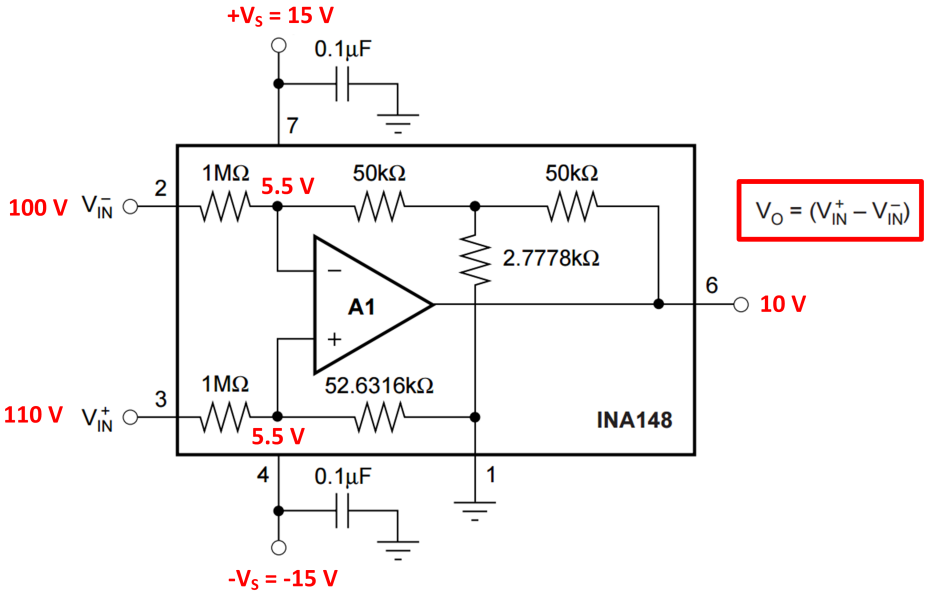


Figure 12. Block Diagram of INA148 Difference Amplifier

As Section 2.5 explains, the CMRR (of A1 in this case) is typically high at low frequencies and degrades at higher frequencies; therefore, this method of rejecting common-mode voltages may be more effective for lower bandwidth common-mode signals. Therefore, this topology is not to be used in this design as the goal is to achieve a high CMRR (> 100 dB) over a wide frequency range.

2.6.2 AC (Capacitive) Coupling

Capacitive coupling of the single-ended signals to the system inputs is another good option for rejecting dc or low-frequency common-mode signals.

The impedance of a capacitor varies inversely with frequency (see Figure 13). At low frequencies, the high impedance of the capacitor in the path of the input current causes a large attenuation or drop in the common-mode voltage before the signal appears at the system inputs, thus providing rejection.

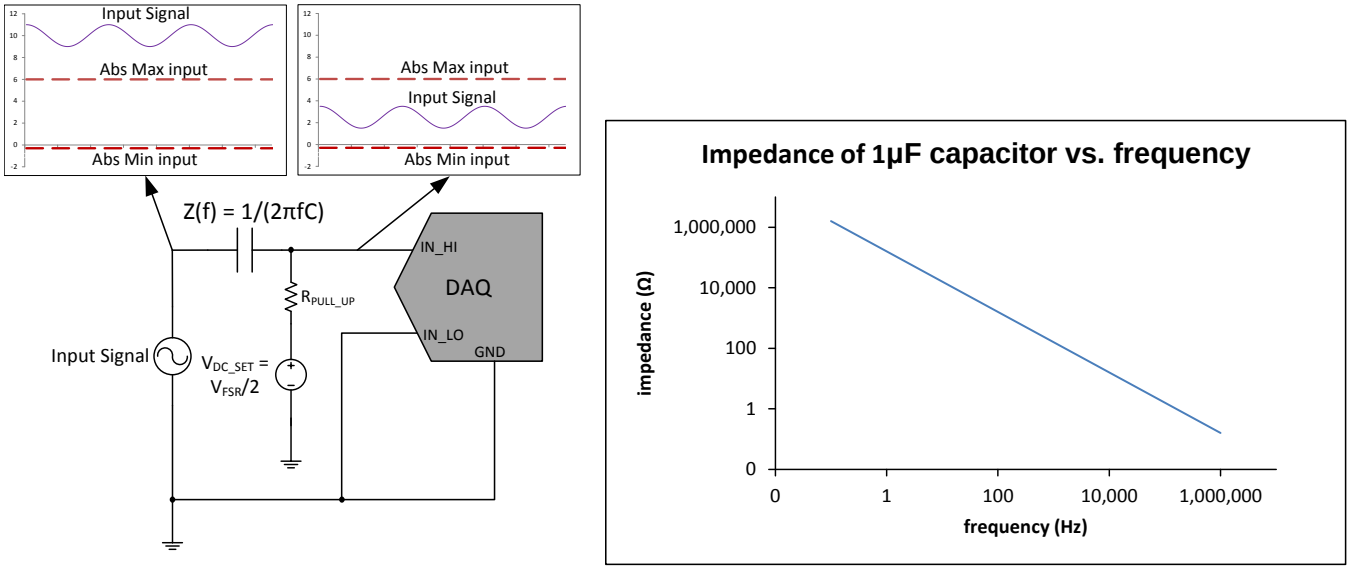
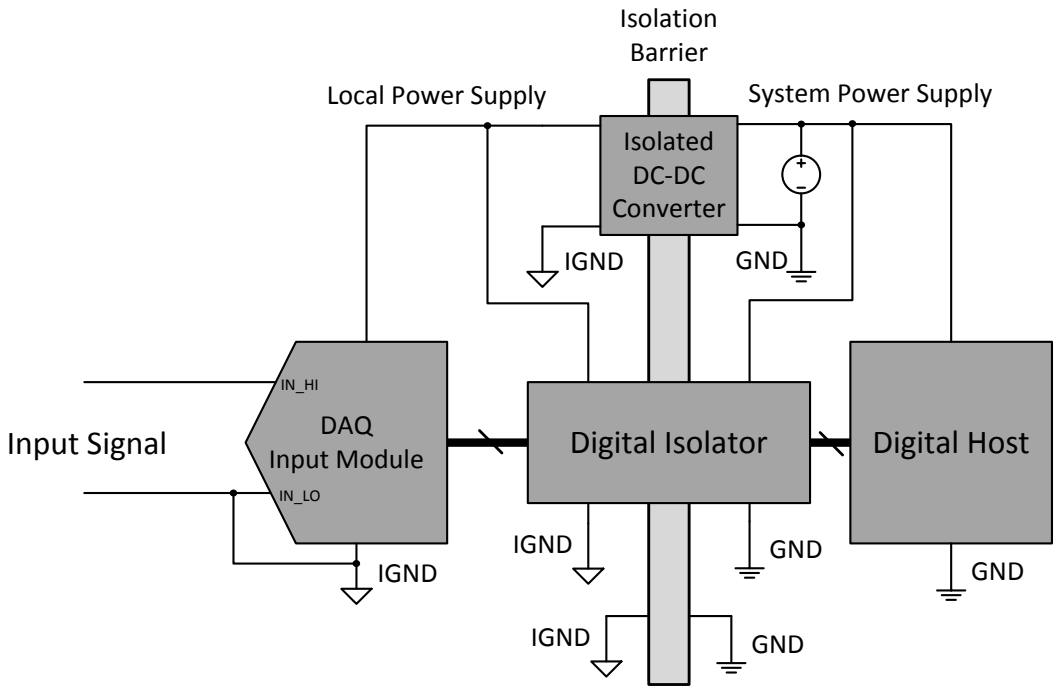


Figure 13. Capacitive Input Coupling for DC Common-Mode Rejection

The obvious drawback of ac coupling the inputs is that it does not work when the differential input signal to be measured is a dc or low frequency signal. As the input frequency decreases, the capacitance required to couple the input signal to the DAQ input without attenuation becomes progressively larger until it becomes impractical. This method is not to be used in this design because the system is required to process dc input signals.

2.6.3 Galvanic Isolation

The use of galvanic isolation is perhaps the most robust option for achieving a good dc and ac common-mode rejection. Galvanic isolation relies on a non-conductive barrier to eliminate all current paths (forward and return) between the input of the DAQ system and its power source (see Figure 14).



NOTE: The potential difference between IGND and GND may be as high as the barrier breakdown voltage (often thousands of volts)

Figure 14. Block Diagram Showing DAQ Input Isolated From System Power Supply

The resulting high impedance between the input ground reference (IGND) and system or host ground (GND) allows the two nodes to float with respect to each other. The advantage of this relationship is that it makes it possible to level-shift IGND relative to GND. Note that the voltage between the grounds appears directly across the isolation barrier and can be made as high as the dielectric breakdown voltage, which is the point at which the isolation barrier ceases to be an insulator. By connecting IGND to the low side of the input signal source, IGND can be made to track the input common-mode voltage. Thus, when the input common-mode signal changes, IGND also changes by the same amount; therefore, the only signal the system inputs sense is the differential signal between the nodes of interest. Hence this scheme provides good common-mode rejection at high frequencies as well as dc and is the topology chosen for this design.

2.7 System Design Details

This subsection discusses the circuit design details and component selection criteria for each block in the system. Figure 15 shows the various system blocks and the order in which they're addressed, as indicated by the circled numbers. Note that the digital host controller details are not addressed, as they are beyond the scope of this document.

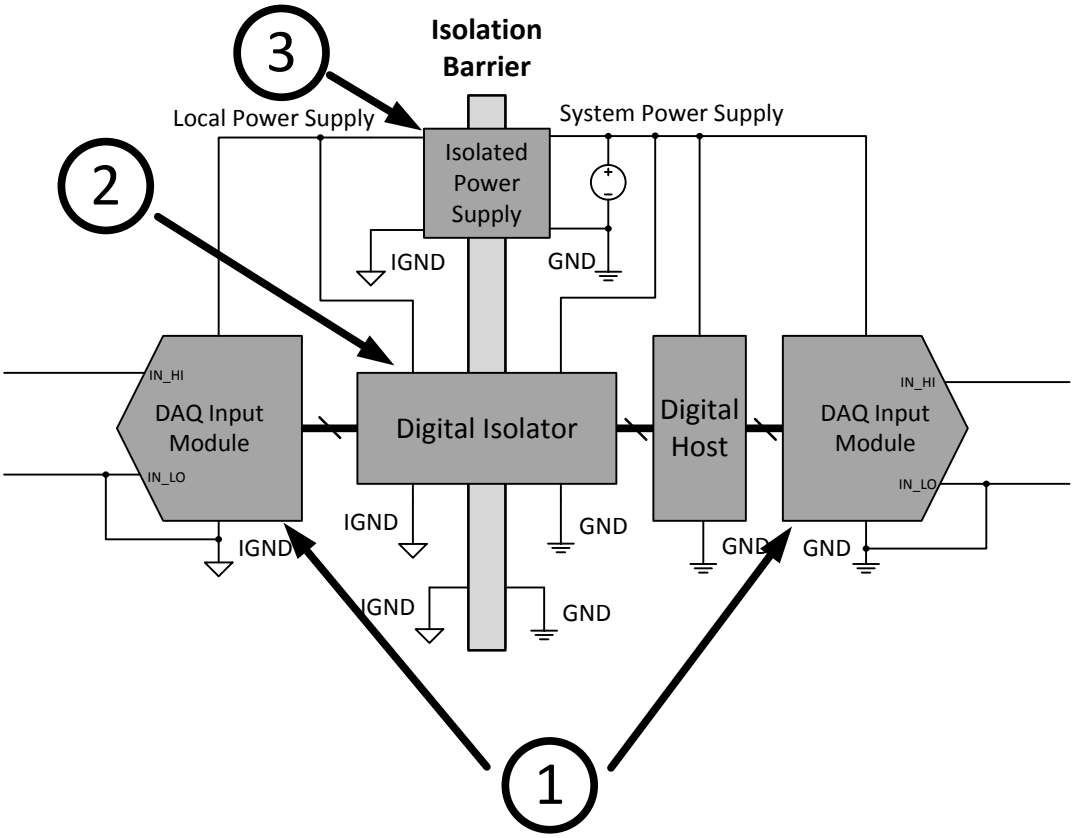


Figure 15. System Block Diagram

2.7.1 Block 1: DAQ Input Module

One of the goals of this design is to compare the ac performance of a DAQ module operating on a floating power supply to that of an identical module powered by the system main supply. This means that the same circuit topology is used to implement the input signal chains on both DAQ channels. Figure 16 shows a typical DAQ input signal path.

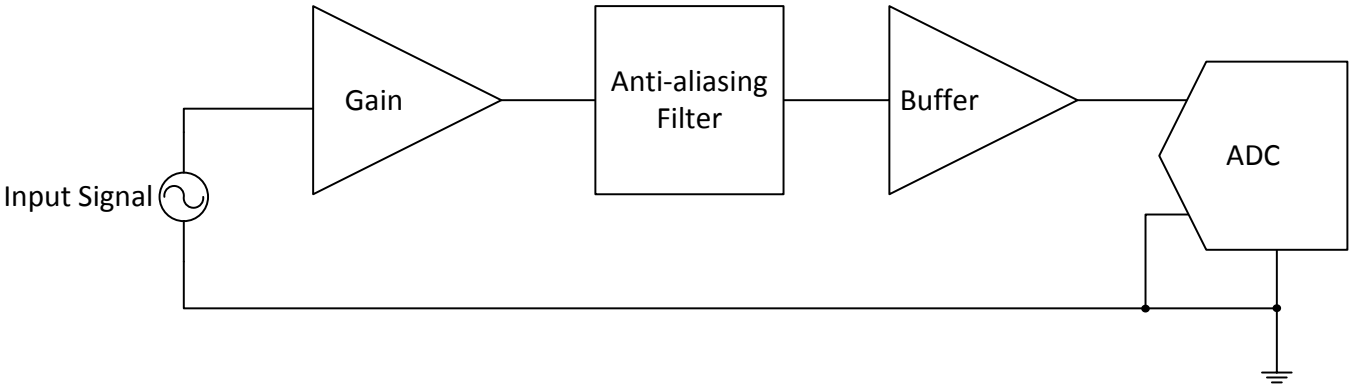


Figure 16. Block Diagram of Typical DAQ Input Signal Path

The first step in designing the input signal path is to select an ADC that has sufficient resolution to satisfy the stipulated ac performance requirements. The required ADC resolution is determined by the effective number of bits (ENOB) parameter that is calculated from the desired signal-to-noise ratio (SNR) and total harmonic distortion (THD) requirements (Equation 8 and Equation 9).

$$ENOB = \frac{SINAD\_dB - 1.76}{6.02} \quad (8)$$

$$\text{where } SINAD\_dB = 10 \times \log_{10}\left(\frac{1}{10^{\frac{-SNR\ dB}{10}} + 10^{\frac{THD\ dB}{10}}}\right) \quad (9)$$

Referring to the design requirements summarized in Table 1, THD_dB = –104 dB and SNR_dB = 90 dB can be substituted into Equation 9, resulting in SINAD_dB = 89.83 dB. Equation 8 can now be solved and the ENOB = 14.63 bits.

Based on the ENOB and the other ADC requirements such as input range, sampling rate, and supply voltage stipulated in Section 1, the SAR ADC architecture is a natural choice. SAR ADCs easily support greater than 14 bits of resolution and have high input bandwidths suitable for acquiring ac signals accurately. Achieving ENOB = 14.63 for a 1-kHz input frequency is realistic using an SAR ADC with ≥ 16 bits of resolution. TI's SAR ADC products support up to 18 bits of resolution at the time of this writing and include products with integrated analog front ends featuring programmable gain, filtering, buffering, and so forth while supporting the required performance levels on a single 5-V power supply. In the interest of design simplicity and minimizing component count, this design uses a suitable integrated SAR ADC.

Table 2 summarizes the ADC selection criteria for this design.

Table 2. Selection Criteria for ADC

CRITERIA	SPECIFICATION
ADC architecture	SAR
Resolution	≥ 16 bits
Input range	±12 V
THD at 1-kHz f_{IN}	≤104 dBc
SNR at 1-kHz f_{IN}	>90 dBc
Sampling rate	1 MSPS
Supply voltages	5 V, 3.3 V
Other features	Integrated signal chain

2.7.2 Block 2: Digital Isolator

Facilitating communication between the digital host processor and an ADC operating on isolated power supplies requires using digital isolators to transfer data across the isolation barrier between the ADC and the host processor. Figure 17 shows the simplified schematic of a digital isolator that uses capacitive coupling to transmit data between different power supply domains referred to GND and IGND.

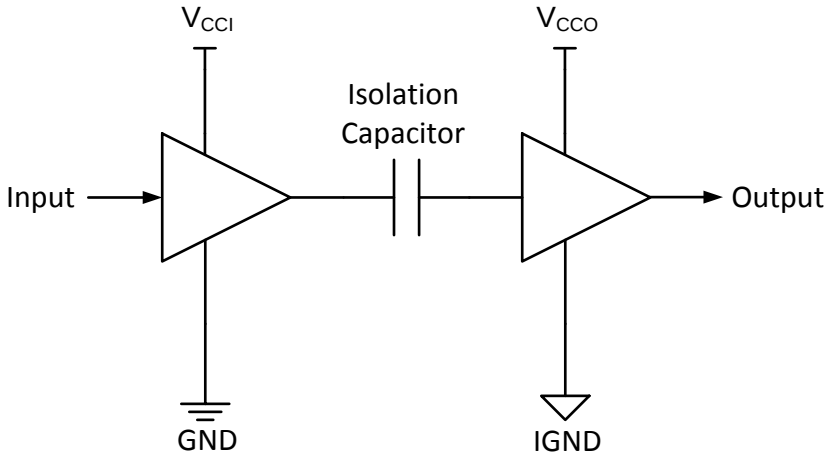


Figure 17. Simplified Schematic of Capacitor-Coupled Digital Isolator

The key selection criteria for digital isolators are:

- *Supply voltage ranges*: The supply voltage ranges on either side of the isolation barrier must be wide enough to accommodate the input/output (I/O) logic levels of the ADC interface and host controller. For example, if the ADC digital interface requires 5-V logic levels but the digital host controller only supports 3.3-V levels, the digital isolator must be able to handle at least a 5-V supply voltage range on the ADC side of the isolation barrier and 3.3 V on the controller side. However, in this design, the ADC and MCU both use 3.3-V logic levels and only require 3.3-V digital supplies.
- *Signaling rate*: The maximum signaling rate of the digital isolator must be at least as high as the highest frequency interface signal. For example, in standard SPI the highest frequency signal is the serial clock (SCLK) and an SCLK frequency of 25 MHz requires a signaling rate of 25 Mbps or higher from the digital isolator.
- *Number of channels*: The standard SPI is a four-wire interface and requires excellent delay matching (or minimal skew) between critical signal pairs (namely SCLK/SDO, SCLK/SDI, and CS/SCLK) on both sides of the isolation barrier to operate reliably at high data rates. Using a multi-channel isolator for each signal pair provides good delay matching between channels and minimizes timing skew.

  The requirement for delay matching at high data rates has special consequences for SCLK, which must be looped back to the SPI master (MCU) across the isolation barrier, as Figure 18 shows.

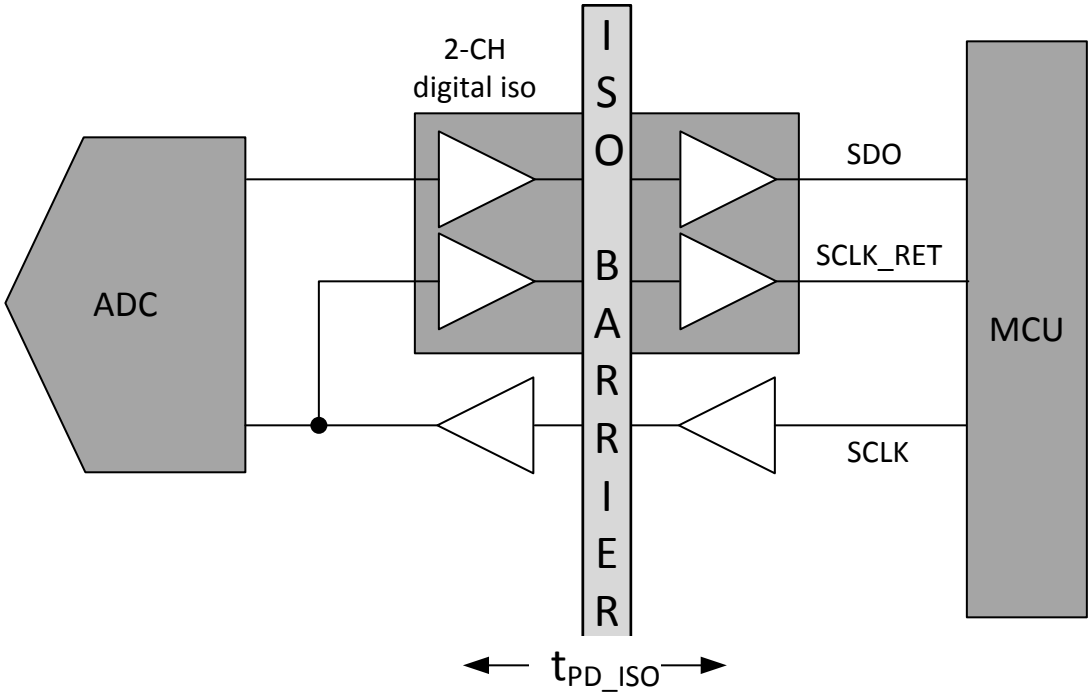


Figure 18. MCU Must Read SDO Relative to SCLK_RET Instead of SCLK

Because the ADC and MCU are on opposite sides of the isolation barrier, the SCLK signal experiences a delay, t_{PD_ISO}, as it travels from the MCU to the ADC. The ADC responds to the delayed version of SCLK with an SDO signal that experiences an additional delay of t_{PD_ISO} as it arrives at the MCU. Therefore, the total skew between the SCLK edge and the corresponding ADC data bit at the MCU is ($2 \times t_{PD\_ISO}$). This delay is acceptable as long as the data bit arrives at the MCU before the MCU performs a read operation. In standard SPI, a read event occurs on the opposite SCLK edge relative to the SCLK edge corresponding to a write event. Therefore, assuming a 50% duty cycle on SCLK, the following condition in Equation 10 must be true to avoid any data capture errors:

$$2 \times t_{PD\_ISO} \le \frac{1}{4 \times f_{SCLK}} - \max\left(t_{SU\_SDO\_SCLK}\right)$$

$$\Rightarrow t_{PD\_ISO} \le \frac{1}{4 \times f_{SCLK}} - \frac{\max\left(t_{SU\_SDO\_SCLK}\right)}{2} \quad (10)$$

The parameters f_{SCLK} and $t_{SU\_SDO\_SCLK}$ in Equation 10 denote the SCLK frequency and the required setup time between SDO and SCLK, respectively.

The user can infer from Equation 10 that for large values of f_{SCLK}, the t_{PD_ISO} requirement becomes challenging to meet. To mitigate this issue, an additional delay of t_{PD_ISO} is introduced in the already delayed version of SCLK by routing SCLK back across the isolation barrier to the MCU along with the SDO signal of the ADC through a multi-channel isolator. This rerouting results in minimal skew between the SDO and SCLK_RET so that the MCU can capture SDO relative to SCLK_RET without error.

- *Propagation delay and inter-signal timing skew*: To avoid any SPI data capture errors, the propagation delay of the digital isolator must be less than half the period of SCLK.
  In addition, the skew of a digital isolator is generally specified at a maximum capacitive load. If larger capacitive loads must be driven, a multi-channel buffer is required to prevent additional skew from being introduced as a result of degraded rise and fall times.
- *Isolation voltage rating*: Referring to Figure 14, the isolation voltage rating of the device must be greater than the maximum expected voltage of IGND relative to GND.

Table 3 summarizes the selection criteria for digital isolators to be used in this design. Note that f_{SCLK} can be determined only after a suitable ADC has been chosen. Therefore, the selection of the digital isolator is contingent upon the selection of a suitable ADC.

Table 3. Selection Criteria for Digital Isolator

CRITERIA	SPECIFICATION
Number of channels per IC	≥ 2
Supply voltages	3.3 V (MCU side), 3.3 V (ADC side)
Signaling rate (Mbps)	> f_{SCLK}
Propagation delay (ns)	< 1 / (2 × f_{SCLK})
Isolation voltage rating	> 200 V

2.7.3 Block 3: Isolated Power Supply

Achieving a good ac performance and high voltage common-mode rejection from the isolated DAQ block requires stable, low-noise isolated power supplies that support a sufficient, high-isolation voltage rating. Galvanic isolation from host ground (GND) is achievable by using a transformer-based switching power supply. However, for low noise, the switching power supply output must undergo filtering and linear regulation before powering the ADC. The push-pull power supply architecture used for the isolated DAQ block is shown in Figure 19.

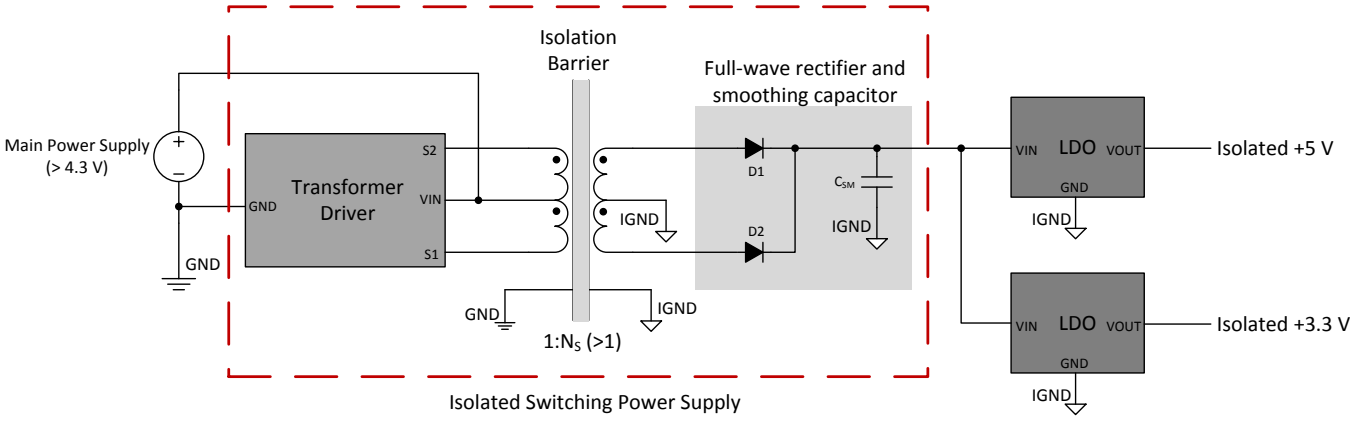


Figure 19. Isolated Power Supply Architecture

The discrete switching power supply architecture in Figure 19 has been chosen for its relatively low input voltage requirement, simplicity, small form factor, and low cost and flexibility (particularly as it relates to selecting a suitable isolation voltage rating). This key parameter is determined by the isolation voltage rating between the coils of the discrete transformer, which can be customized to an application. The following subsections detail the individual components of the isolated power supply.

2.7.3.1 Main Power Supply

In this design the isolated switching power supply is generated using the USB supply available on the host side of the PC. The USB supply voltage (V_{USB}) has a nominal value of 5 V and can vary by as much as ±0.5 V across PCs. The USB supply current limit in this design is approximately 150 mA; to overcome these USB supply limitations, an external supply option has also been provided.

2.7.3.2 Push-Pull Transformer Driver

The push-pull transformer driver uses the dc output of the USB supply to generate a switching waveform for inductive coupling across the isolation barrier. The transformer driver consists of two switches (S1 and S2 in Figure 19) with complementary, break-before-make timing to push or pull current between V_{USB} and GND through the upper and lower sections of a center-tapped transformer. The relative timing between S1 and S2 and the resulting single-ended waveforms at the upper and lower transformer terminals are shown in Figure 20.

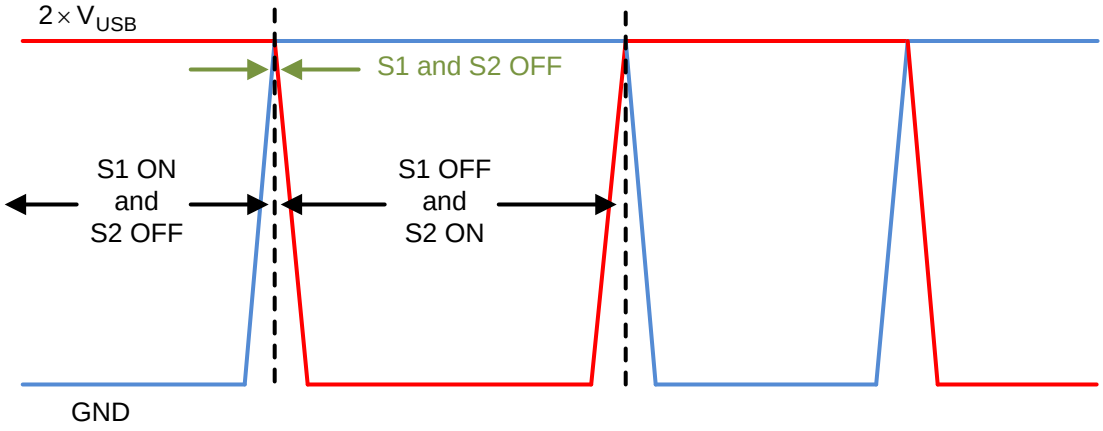


Figure 20. Push-Pull Timing and Single-Ended Waveforms Relative to GND at Transformer Primary

The main selection criteria for the transformer driver are small size, low pin count, and a minimum input voltage requirement of less than 4.5 V, which is the minimum observed value of the USB supply voltage.

2.7.3.3 Center-Tapped Transformer

Three primary requirements exist for selecting the center-tapped transformer:

1. The transformer must support the minimum isolation voltage rating required for the application.
2. The transformer must have a turns-ratio with $N_S > 1$ so that the voltage at the input of the low dropout regulator (LDO) is sufficiently greater than its output to maintain linear regulation of the isolated supply, even when the USB supply voltage is at its minimum value (4.5 V). In particular, the turns-ratio must account for the voltage drop across the rectifier diode (V_{DIODE}) and the maximum drop-out voltage of the LDO (V_{DO_LDO}). Therefore, in the following Equation 11, N_S can be estimated as:

$$N_S > \frac{V_{LDO} + V_{DO\_LDO} + V_{DIODE}}{V_{USB}} \quad (11)$$

Figure 21 shows the single-ended waveforms that appear on the transformer secondary terminals relative to IGND, which is the secondary center-tap terminal.

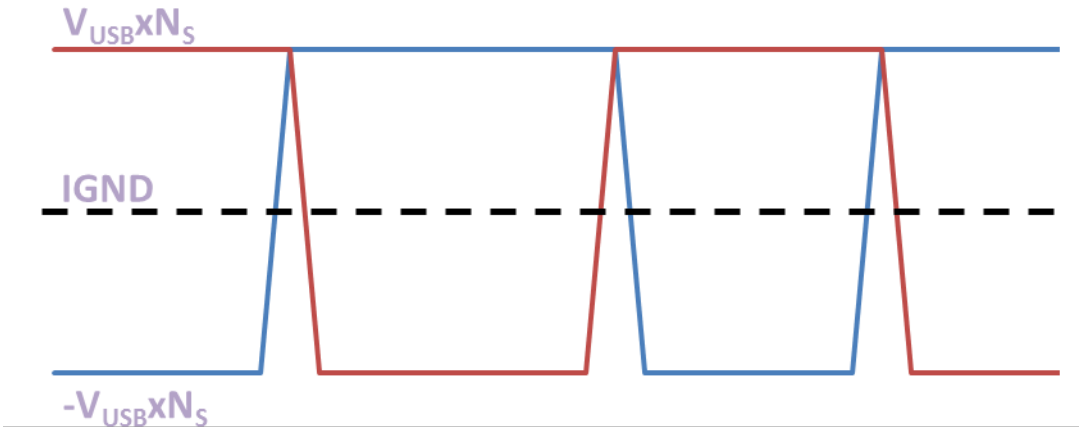


Figure 21. Single-Ended Waveforms Relative to IGND at Transformer Secondary Terminals

3. The Vt product of the transformer must be greater than the Vt product of the magnetic field applied by the transformer driver so that the transformer core does not saturate. The maximum value of the Vt product applied by the transformer driver is the product of the maximum voltage across the primary coil and the maximum duration for which that voltage is applied, which is half the period of the minimum transformer driver switching frequency at the specified input voltage. Therefore, in Equation 12:

$$Vt_{TRANSFORMER} > \frac{\max\left(V_{USB}\right)}{2 \times \min\left(f_{TRANSFORMER\_DRIVER}\right)} \quad (12)$$

2.7.3.4 Full-Wave Rectifier and Smoothing Capacitor

The full-wave rectifier and smoothing capacitor (C_{SM}) operate on the voltage across the transformer secondary to produce a low-ripple waveform at the LDO input. Figure 22 shows the signal across C_{SM}.

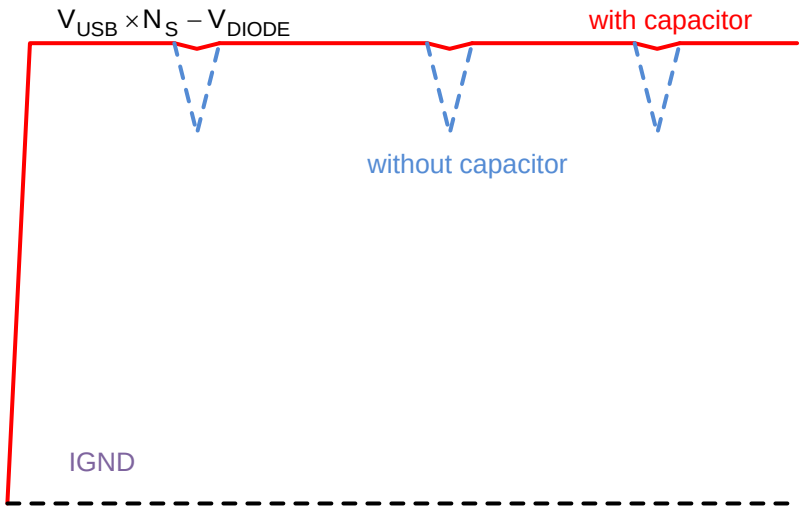


Figure 22. Rectified and Smoothed Signal at LDO Input

The rectifier diodes D1 and D2 introduce a voltage drop (V_{DIODE}) whenever they conduct. From Equation 11 it is evident that larger values of V_{DIODE} necessitate higher values for the transformer turns-ratio so that the LDO is able to maintain line regulation. Because power is conserved across the transformer, a higher turns-ratio translates to a higher primary current, which may potentially exceed the drive capability of the transformer driver. To avoid this undesirable condition, D1 and D2 must be Schottky diodes so that the V_{DIODE} is as low as possible.

Figure 22 also shows that the ripple in the rectified waveform cannot be totally eliminated, but it can be attenuated by using a large enough smoothing capacitor. Ripple attenuation is important because the LDO has a finite power supply rejection ratio (PSRR) and as a result the input ripple propagates to the LDO output. For a good performance, the peak amplitude of the LDO output ripple must be less than its broadband output noise ($V_{BBNoise\_RMS\_LDO}$). The peak ripple amplitude is given by Equation 13:

$$V_{RIPPLE} = \frac{I_{LOAD}}{f_{RIPPLE} \times C_{SM}} \tag{13}$$

In Equation 13, I_{LOAD} is the total dc load current on the LDO output and f_{RIPPLE} is the ripple frequency. Note that $f_{RIPPLE} = (2 \times f_{TRANSFORMER\_DRIVER})$.

To calculate the required value of C_{SM}, the following condition from Equation 14 can now be imposed:

$$V_{RIPPLE} \leq V_{BBNoise\_RMS\_LDO} \times PSRR\left(f_{RIPPLE}\right) \tag{14}$$

In Equation 14 the PSRR (f_{RIPPLE}) is the PSRR of the LDO at the ripple frequency.

Combine Equation 13 and Equation 14 to calculate the C_{SM} in Equation 15:

$$C_{SM} \geq \frac{I_{LOAD}}{f_{RIPPLE} \times V_{BBNoise\_RMS\_LDO} \times PSRR\left(f_{RIPPLE}\right)} \tag{15}$$

Note that the C_{SM} can be calculated only after a suitable LDO has been selected and I_{LOAD} has been estimated, which requires selection of the ADC and digital isolators.

2.7.3.5 LDO Regulator

Clean power supplies are extremely important for SAR ADCs because of their high sensitivity to high-frequency power supply fluctuations. Any high frequency ripple or noise appearing on SAR ADC supply pins (both analog and digital) propagates to the output with little attenuation and degrades the SNR. Therefore, because of their excellent PSRR and noise characteristics, linear LDOs are much more suitable than switching regulators for powering SAR ADCs. A low-noise LDO is used to power the isolated ADC block in this design.

The output noise contribution of the LDO must be negligible compared to that of the ADC. According to Table 2, the ADC must provide an SNR > 90 dB on a full-scale input range (FSR) of ±12 V. Therefore, the RMS output noise of the ADC can be calculated as the following Equation 16:

$$V_{BBNoise\_RMNS\_SDC} \leq 10^{\frac{-SNR(dB)}{20}} \times \frac{FSR}{2\sqrt{2}}$$

$$\Rightarrow V_{BBNoise\_RMS\_ADC} < 10^{\frac{-SNR(dB)}{20}} \times \frac{FSR}{2\sqrt{2}}$$

$$\Rightarrow V_{BBNoise\_RMS\_ADC} < 268\ \mu V \tag{16}$$

The broadband ADC noise can be used to select a low noise LDO using Equation 17:

$$V_{BBNoise\_RMS\_LDO} \leq 10\% \times V_{BBNoise\_RMS\_ADC}$$

$$\Rightarrow V_{BBNoise\_RMS\_LDO} \leq 26\ \mu V \tag{17}$$

Additionally, the LDO must have a low dropout voltage and be able to provide the required output voltage.

Table 4 summarizes the key selection criteria for the components of the isolated power supply topology shown in Figure 19.

Table 4. Selection Criteria for Isolated Power Supply Components

PARAMETERS		SPECIFICATIONS
LDO	Output voltages, V_{LDO}	5 V, 3.3 V
	Dropout voltage, V_{DO_LDO}	< 0.3V
	RMS noise, $V_{BBNoise\_RMS\_LDO}$	26 µV
Full-wave rectifier	Ripple amplitude, V_{RIPPLE} (V)	Equation 14
	Smoothing capacitor, C_{SM} (F)	Equation 15
	Schottky diode drop, V_{DIODE}	0.25 V
Center-tapped transformer	Isolation rating	> 200 V
	V-t product, $Vt_{TRANSFORMER}$ (V-s)	Equation 12
	Turns-ratio, 1:N_S	Equation 11
Transformer driver	Input voltage	≤ 4.5 V
	Other features	Small size, low pin count
Main supply voltage		≥ 4.3

3 Component Selection

The selection criteria from Section 2.7 can now be applied to select the suitable components for implementing blocks 1, 2, and 3 of the system block diagram shown in Figure 15.

3.1 Block 1: DAQ Input Module

The ADS8681 is a self-contained DAQ input module consisting of a 16-bit 1-MSPS SAR ADC with integrated AFE for precision signal conditioning that simplifies ADC input and reference driving. The input signal chain also features a PGA that offers high 1-MΩ input impedance and supports up to ±12.28-V inputs on a single unipolar 5-V supply. The pinout and block diagram of the ADS8681 shown in Figure 23 provide additional details.

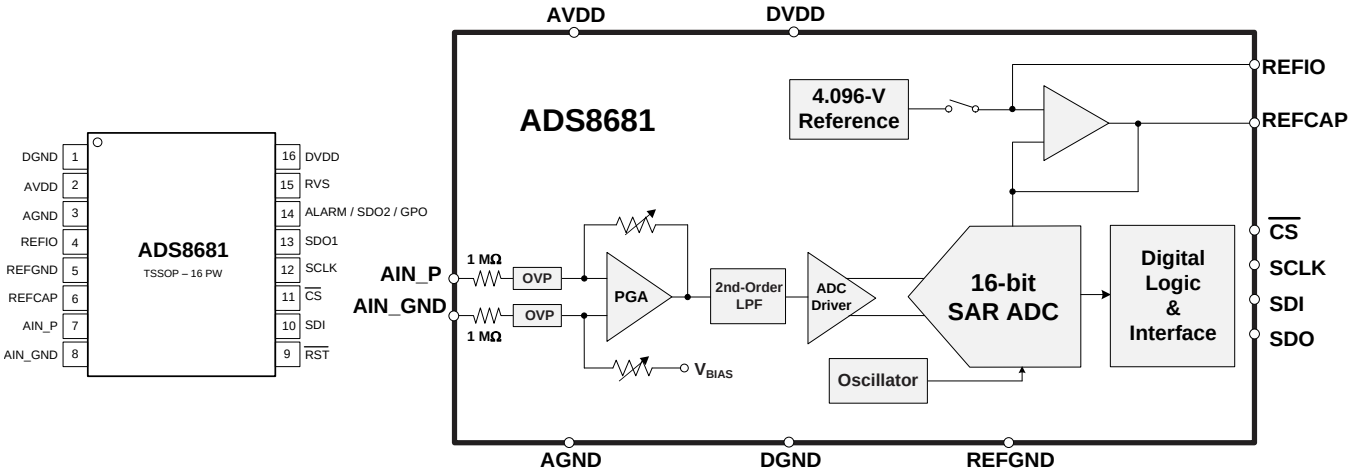


Figure 23. Pinout and Block Diagram of ADS8681

The ADS8681 also includes multi-SPI™ technology from TI, which is an enhanced SPI-compatible interface that makes enables achieving high sampling rates at lower SCLK frequencies. To summarize, the multi-SPI™ makes the ADS8681 device amenable to systems that may be using slower, less capable host controllers.

The ADS8681 also offers excellent ac performance with an SNR ≥ 90 dB and THD ≤ –105 dB for a 1-kHz input at its maximum 1-MSPS throughput rate.

Based on the DAQ input module requirements summarized in Table 2, the ADS8681 is an optimal choice for this design.

3.2 Block 2: Digital Isolator

Table 5 summarizes the requirements for digital isolators. Performing a parametric search for suitable devices requires knowing the value of f_{SCLK}, which can now be estimated based on the timing specifications of the ADS8681. The ADS8681 datasheet requires an SCLK frequency of at least 50 MHz to be able to support a 1-MSPS throughput rate using a standard SPI. If the non-zero roundtrip delay across the isolation barrier has been considered, the minimum SCLK frequency required to support 1 MSPS is higher than 50 MHz. With this information, the unknown quantities in Table 5 can now be populated:

Table 5. Selection Criteria for Digital Isolator

PARAMETER	SPECIFICATION
Number of channels per IC	≥ 2
Supply voltages	3.3 V (MCU side), 3.3 V (ADC side)
Signaling rate	> 50 Mbps
Propagation delay	< 10 ns
Isolation voltage rating	> 200 V

A parametric search on TI.com with the contents of Table 5 yields the following hits in Table 6:

Table 6. Results of Parametric Search for Digital Isolators on TI.com

PART NUMBER	NO. OF CHANNELS	PROPAGATION DELAY (TYP)	SPEED (MAX)	FORWARD/REVERSE CHANNELS	VCC (MIN)	VCC (MAX)	UL 1577 ISOLATION VOLTAGE (SINGLE)
ISO7640FM	4	7 ns	150 Mbps	4/0	2.7 V	5 V	4200 V_{RMS}
ISO7420E	2	7 ns	50 Mbps	2/0	3.3 V	5 V	2500 V_{RMS}
ISO7420FE	2	7 ns	50 Mbps	2/0	3.3 V	5 V	2500 V_{RMS}

The ISO7640 meets all the requirements of Table 5 and is the natural choice for this design. The ISO7420xx devices are marginal in terms of speed; however, they each support just two channels, which is a drawback for this design. Based on the pinout of the ADS8681 shown in Figure 23, SDO1, SDO2, and RVS (ADC digital outputs) must be synchronized with SCLK_RET while /CS and SDI (ADC inputs) must be synchronized with SCLK. Therefore, this design requires only two ISO7640 units instead of eight or more ISO7420xx units to fulfill this requirement, which is another reason why the ISO7640 is a better option for this design.

An important caveat associated with the ISO7640 is that while its typical propagation delay (t_{PD_ISO}) is about 7 ns, the maximum propagation delay of a single channel using 3.3-V supplies on both sides of the isolation barrier is 14 ns, based on the datasheet. Given that the ADS8681 requires an SCLK period of 20 ns or lower to sustain a 1-MSPS throughput rate and the one-way isolator delay (on SCLK and other digital signals) is greater than half an SCLK period, achieving a 1-MSPS throughput under these conditions is not possible without implementing one of the following options:

- Use both SDO channels available on the ADS8681 device to read two bits on each SCLK_RET edge. This approach increases the maximum tolerable SCLK period to 40 ns so that the isolator delay is now less than half an SCLK cycle. Note that this approach consumes an extra I/O pin on the MCU.
- Use an SCLK period lower than 20 ns if possible to compress the read phase of the ADC cycle by the round-trip isolator delay of 28 ns. Figure 24 shows the resulting changes in SPI timing that yield a 1-MSPS throughput rate.

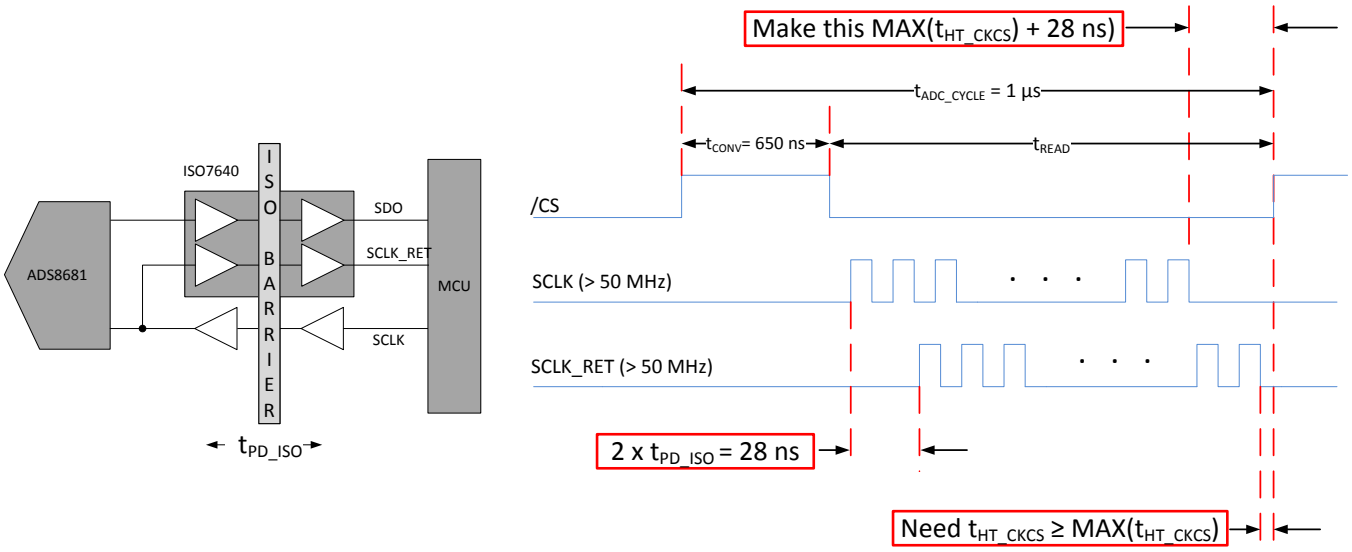


Figure 24. Compensating SPI Timing for t_{PD_ISO} to Achieve 1-MSPS Operation From ADS8681

Additionally, the delay specifications of the ISO7640 are only rated for a 15-pF capacitive load, which is marginal considering that the stray capacitances of package pins can be 10 pF or more. Driving larger capacitive loads degrades rise and fall times and contributes additional delay. Therefore, the outputs of the ISO7640 must be buffered with a high-speed multi-channel device such as the SN74AUC17, which has timing delays and skews that are characterized using much greater capacitive loads.

3.3 Block 3: Isolated Power Supply

Table 4 specifies the component requirements of the isolated power supply block. The main power supply, LDO, and transformer driver have the most complete set of requirements and can be chosen before the other components.

3.3.1 Main Power Supply

As noted in Section 2.7.3.1, there are two options available on the non-isolated side of the circuit from which the isolated power supply can be generated:

1. The USB supply of the PC with a voltage that may be as low as 4.5 V (perhaps even lower)
2. An optional external source such as an ac wall adapter or lab power supply for greater reliability

The PJ-102A is a standard PCB mount barrel connector that can also be used as a switch and is ideal for this application. The switch functionality of the connector and connection diagram are shown in Figure 25.

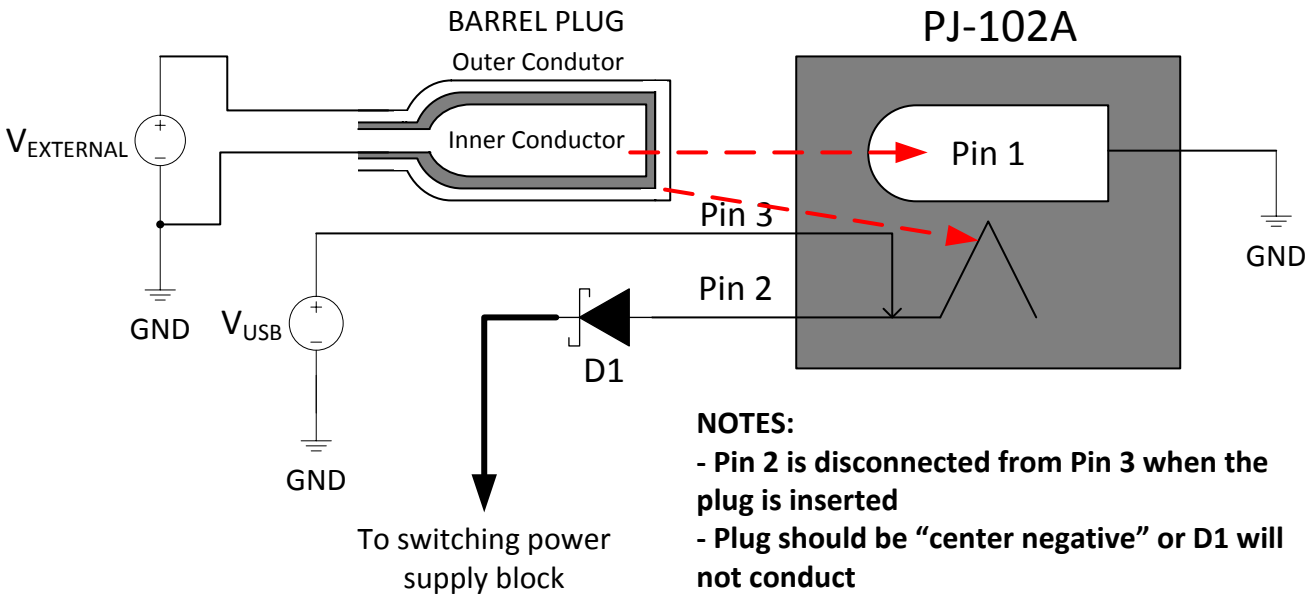


Figure 25. PJ-102A as Switch Between USB and External Power Supply

As Figure 25 shows, pin 2 and pin 3 of the PJ-102A are typically connected. When the plug has been inserted, pin 2 becomes connected to the outer conductor of the plug instead of pin 3. Thus, pin 2 acts as a switch between pin 3 and the outer conductor of the plug. Because a positive supply voltage is required at pin 2, the plug must be “center-negative”, which means that the outer conductor of the plug must be connected to the high side of the external supply. If the polarities are reversed, the inputs of the switching power supply that are connected to pin 2 are driven below GND (pin 1) and may sustain permanent damage. D1 protects against this condition by always directing current to flow from pin 2 to pin 1 and not the other way around.

To be effective, D1 must have a sufficiently high reverse breakdown voltage (approximately > 10 V), a low forward voltage drop (< 300 mV), and be able to dissipate > 50 mW of power (250 mV at 200 mA). The MBR0520LT1G is a suitable Schottky diode with a 20-V reverse breakdown voltage that is capable of conducting over 250 mA with a forward voltage drop of less than 300 mV (at 25ºC).

3.3.2 LDO Selection

Table 7 summarizes the parametric search results for LDOs capable of producing a 5-V output with less than 26 µV (see Equation 16) of RMS broadband noise. The list is sorted in increasing order of the specified noise values.

Table 7. LDO Options From TI.com Sorted By Increasing Noise

PART NUMBER	V_{DO} (TYP)	ACCURACY	NOISE	PSRR AT 100 kHz	I_{OUT} (MAX)	I_q (TYP)
TPS7A49	260 mV	2.5%	15 μV_{RMS}	54 dB	0.15 A	0.06 mA
TPS79101-Q1	38 mV	2%	15 μV_{RMS}	45 dB	0.1 A	0.17 mA
TPS79101-EP	38 mV	2%	15 μV_{RMS}	45 dB	0.1 A	0.17 mA
TPS791	38 mV	2%	15 μV_{RMS}	45 dB	0.1 A	0.17 mA
TPS717-Q1	170 mV	3%	20.7 μV_{RMS}	67 dB	0.15 A	0.045 mA
TPS7A8101-Q1	250 mV	3%	23 μV_{RMS}	60 dB	1 A	0.06 mA
TPS7A8101	170 mV	3%	23 μV_{RMS}	60 dB	1 A	0.06 mA
REG101	60 mV	2.7%	23 μV_{RMS}	46 dB	0.1 A	0.4 mA

There are several excellent options in Table 7 that can work perfectly well in this design but the TPS7A49 device is a well-rounded choice because it provides low noise as well as high PSRR at high frequencies, both of which are key parameters in this design.

3.3.3 Push-Pull Transformer Driver Selection

The key parameters for selecting the transformer driver are its dimensions and minimum input voltage, which must align with the minimum output voltage of the main power supply. Referring to Section 3.3.1, the minimum value of the main supply voltage may be as low as 4.3 V after accounting for the approximately 200-mV drop because of the reverse protection diode (D1 in Figure 25). Table 8 shows the results of a parametric search on TI.com for isolated dc-dc converter products with input voltages less than 4.3 V.

Table 8. Isolated DC-DC Converter Products With Minimum Input Below 4.3 V Sorted by Size

PART NUMBER	V_{IN} (MIN)	V_{IN} (MAX)	V_{OUT} (MIN)	V_{OUT} (MAX)	SWITCHING FREQUENCY (MAX)	ESTIMATED PACKAGE SIZE (WxL)
TPS55010	2.95 V	6 V	3.3 V	20 V	2000 kHz	16WQFN: 3 x 3: 9 mm2
SN6505A	2.25 V	5.5 V	0 V	16 V	600 kHz	6SOT-23: 1.6 x 2.9: 10 mm2
SN6505B	2.25 V	5.5 V	0 V	16 V	1600 kHz	6SOT-23: 1.6 x 2.9: 10 mm2
SN6501	3 V	5.5 V	0 V	11 V	620 kHz	5SOT-23: 1.6 x 2.9: 10 mm2
LM5015	4.25 V	75 V	1.26 V	37 V	750 kHz	14HTSSOP: 4.4 x 5: 32 mm2

Of the options listed in Table 8, only the SN65xx devices support the push-pull topology that was selected for this design (see Figure 19). The SN6501 has ultimately been chosen for its lower cost, although the SN6505 is an excellent alternative that provides a number of useful features that enable output switching noise control, overdrive protection, and controlled start-up.

A peripheral circuit consisting of a comparator, voltage reference, and load switch has been designed to facilitate a more predictable start-up of the isolated switching power supply. Figure 26 shows the schematic and operation of the circuit.

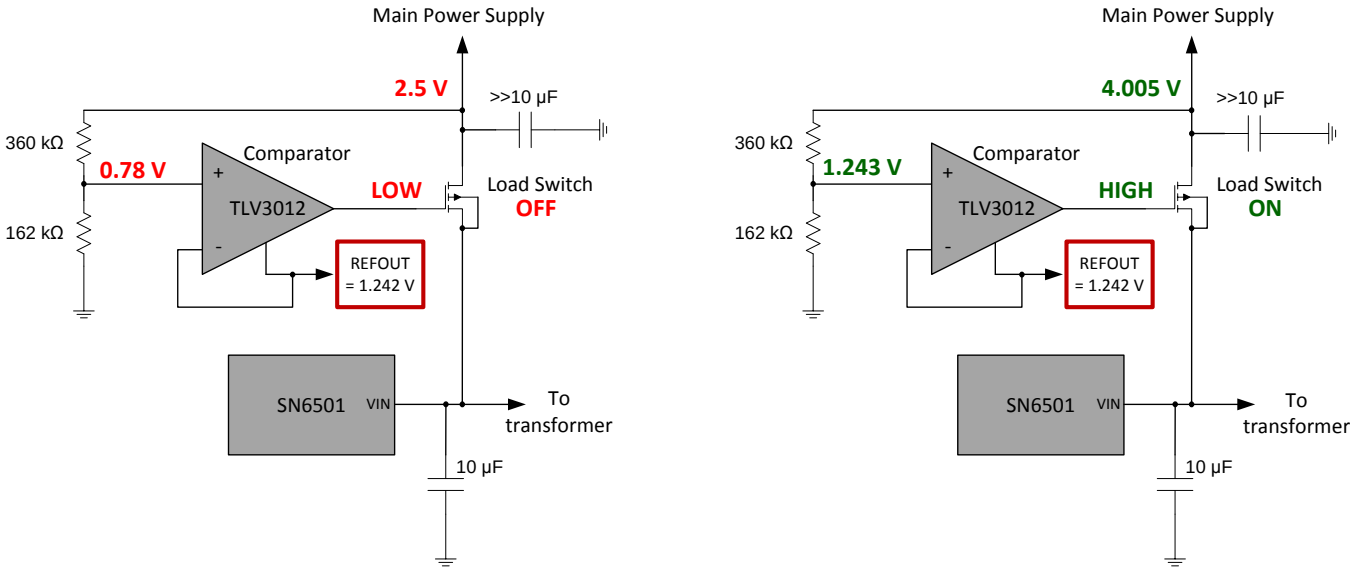


Figure 26. Start-up Circuit for Switching Power Supply

The SN6501 device starts switching when its input voltage increases to about 2.4 V. At this point, there may not be enough charge stored in the bypass capacitor at the main power supply output to satisfy the transient load current demand. As a result of this insufficient charge, the system behavior may become unpredictable For example, the main supply output may take a long time to settle, oscillate, or the SN6501 device may not function correctly. The circuit in Figure 26 has been designed to keep the SN6501 device in a powered-down state until the voltage across the bypass capacitor is > 4 V, allowing the system to start up in a consistent manner.

3.3.4 Full-Wave Rectifier Diode and Smoothing Capacitor

Equation 15 determines the value of the smoothing capacitor:

$$C_{SM} \geq \frac{I_{LOAD}}{f_{RIPPLE} \times V_{BBNoise\_RMS\_LSDO} \times PSRR(f_{RIPPLE})}$$

Because the LDO and transformer driver have already been selected, the values of f_{RIPPLE} and the LDO PSRR(f_{RIPPLE}) can be estimated using information from the datasheet.

The maximum switching frequency of the SN6501 device on a 5-V power supply is 620 kHz. After full-wave rectification, the ripple frequency is double the converter switching frequency, that is f_{RIPPLE} = 1.24 MHz.

Figure 27 shows the PSRR of the TPS7A49 over frequency.

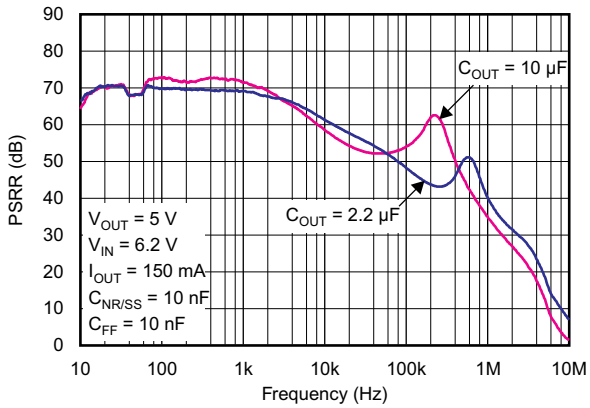


Figure 27. PSRR of the TPS7A49 LDO

With an output bypass capacitor of 10 µF, the PSRR at 1.24 MHz is approximately 35 dB or 56.2 V/V.

Evaluating C_{SM} also requires the total load current (I_{LOAD}), which is estimated by adding the quiescent currents of each system block, as Table 9 shows. Note that the high-frequency load current demand is mostly fulfilled by the supply bypass capacitors and is not considered when calculating I_{LOAD}.

Table 9. Estimate of I_{LOAD}

COMPONENT	I_q
ADS8681	8 mA
Two ISO7640s	12 mA
Two TPS7A49s	0.2 mA
SN6501	0.7 mA
Total	**20.9 mA**

A more conservative estimate to make for I_{LOAD} is I_{LOAD}= 25 mA.

Solving with $V_{BBNoise\_RMS\_LDO}$ = 26 µV, I_{LOAD} = 25 mA, f_{RIPPLE} = 1.24 MHz, and PSRR(f_{RIPPLE}) = 56.2 V/V yields $C_{SM} \geq$ 13 µF. A value of C_{SM} = 10 µF is reasonable.

With regard to selecting the rectifier diode, a Schottky diode is preferable to minimize the voltage drop across the rectifier circuit. The SN6501 datasheet recommends selecting the MBR0520L diode, for which Figure 28 shows the V-I characteristic.

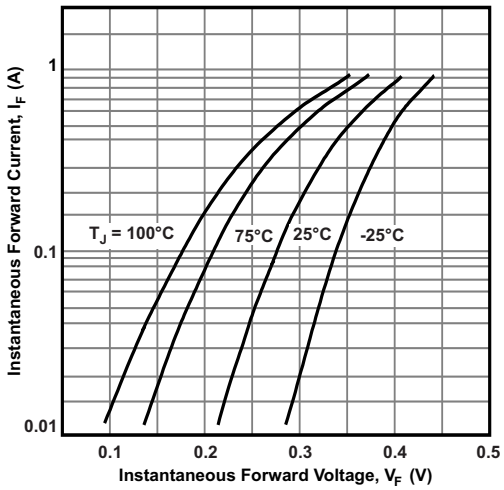


Figure 28. V-I Characteristics of MBR0520L

Based on Figure 28, the forward voltage drop (V_{DIODE}) of the MBR0520L at 25°C when conducting 30 mA is less than 250 mV; therefore, the MBR0520L is a suitable Schottky diode for this design.

3.3.5 Center-Tapped Transformer Selection

A suitable transformer can be selected based on the required turns-ratio and Vt product. Equation 11 determines the transformer turns-ratio:

$$N_S > \frac{V_{LDO} + V_{DO\_LDO} + V_{DIODE}}{V_{USB}}$$

The only unknown quantity in Equation 11 is V_{DO_LDO}, which is the LDO dropout voltage that can be obtained from the datasheet of the TPS7A49 device. Figure 29 shows the dropout voltage of the TPS7A49 versus the load current.

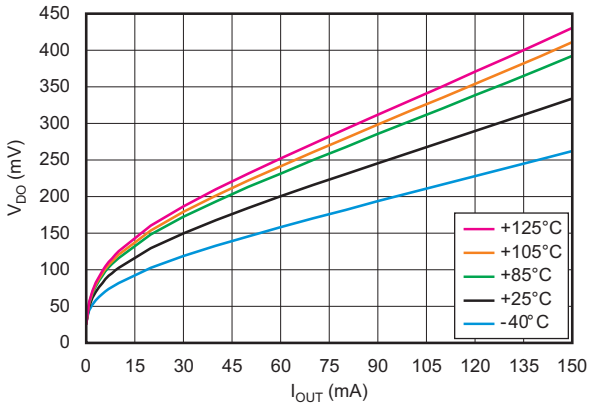


Figure 29. Dropout Voltage vs. Load Current of TPS7A49

From Figure 29, the TPS7A49 has a typical dropout voltage (V_{DO_LDO}) of less than 250 mV across its rated temperature range for a 30-mA load. Solve Equation 11 using V_{LDO} = 5 V, V_{DO_LDO} = 0.25 V, V_{DIODE} = 0.25 V, and V_{USB} = 4.5 V yields N_S > 1.22.

The minimum Vt product requirement of the transformer can be calculated from Equation 12, but that is not necessary in this case because the SN6501 datasheet provides a list of recommended isolation transformers for use with the SN6501 device. Part number 760390014 from Wurth Electronics/Midcom has a turns-ratio of 1:1.3 and an isolation rating of 3125 V_{RMS}, which make it a suitable choice for this design.

4 Verification and Measured Performance

Figure 30 shows the test setup used to measure the ac performance of the isolated DAQ channel in the presence of a high-voltage, ac input, common-mode signal. The source of the low distortion input signal must also float so that it can be dc-coupled to the input of the isolated ADS8681 device. The common-mode signal injected between IGND and GND is generated by using a step-up transformer to amplify the output of a signal generator. The transformer does not have a constant gain characteristic over frequency; therefore, to calculate the CMRR at each frequency, the common-mode voltage at that frequency must be measured. So a digital multimeter (DMM) is inserted between IGND and GND to read the RMS common-mode amplitude.

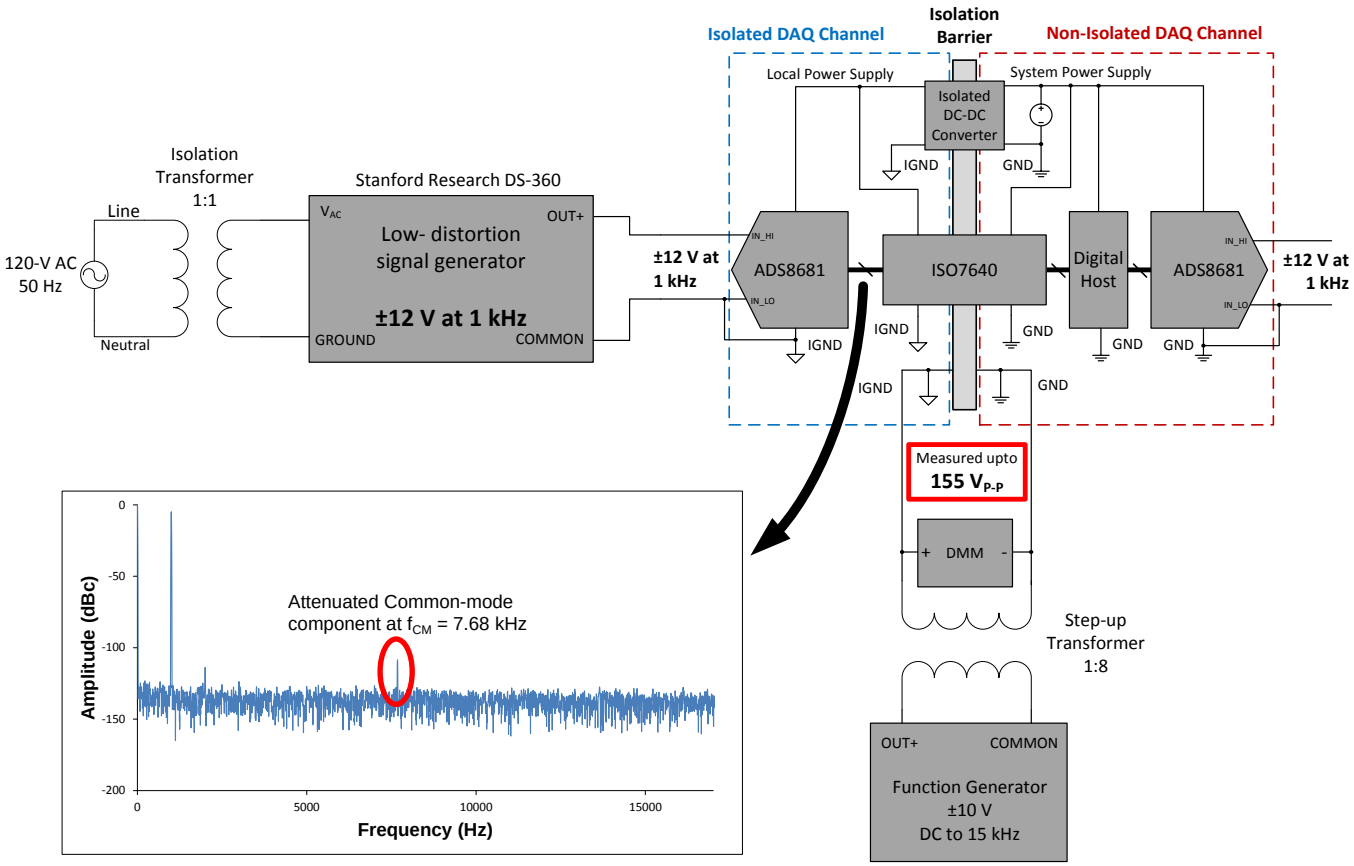


Figure 30. Test Setup for Measuring HV CMRR and AC Performance on Isolated DAQ Channel

The CMRR is calculated using the following method:

1. Based on the peak-to-peak amplitude, V_{IN_PP} of the 1-kHz sinusoidal input signal calculate the RMS amplitude: $V_{IN\_RMS} = V_{IN\_PP} / 2 / \sqrt{2}$
2. Based on the number of samples, N (which must be a power of 2) and the sampling frequency, f_{SAMP}, calculate the frequency resolution, f_{RES}, which is the bandwidth of each FFT bin: $f_{RES} = f_{SAMP} / N$
3. For each common-mode frequency applied (f_{CM}), acquire N-digital samples of the 1-kHz input signal and generate the FFT of the sample set
4. Record the common-mode RMS voltage value (V_{CM_I}) by reading the DMM
5. Calculate the fast Fourier transform (FFT) bin number corresponding to f_{CM}: $BIN[f_{CM}] = ROUND(f_{CM} \times f_{RES})$
6. Record the FFT amplitude value in dB, dB_CME, of the common-mode error signal by looking up the value corresponding to $BIN[f_{CM}]$ on the FFT plot
7. Calculate the RMS amplitude corresponding to dB_CME as: $V_{CM\_E} = V_{IN\_RMS} \times 10^{(dB\_CME\ /\ 20)}$
8. Assuming $A_{DIFF} = 1$ V/V (for the 1-kHz signal component), calculate CMRR (in dB units) using Equation 5 and Equation 6 as: $CMRR(dB) = 20 \times \log_{10} \times (V_{CM\_I} / V_{CM\_E})$

For an example on computing ac performance parameters using the FFT of the ADC output, refer to the TIPD113 TI Precision Design (SLAU513).

4.1 Characteristic Curves

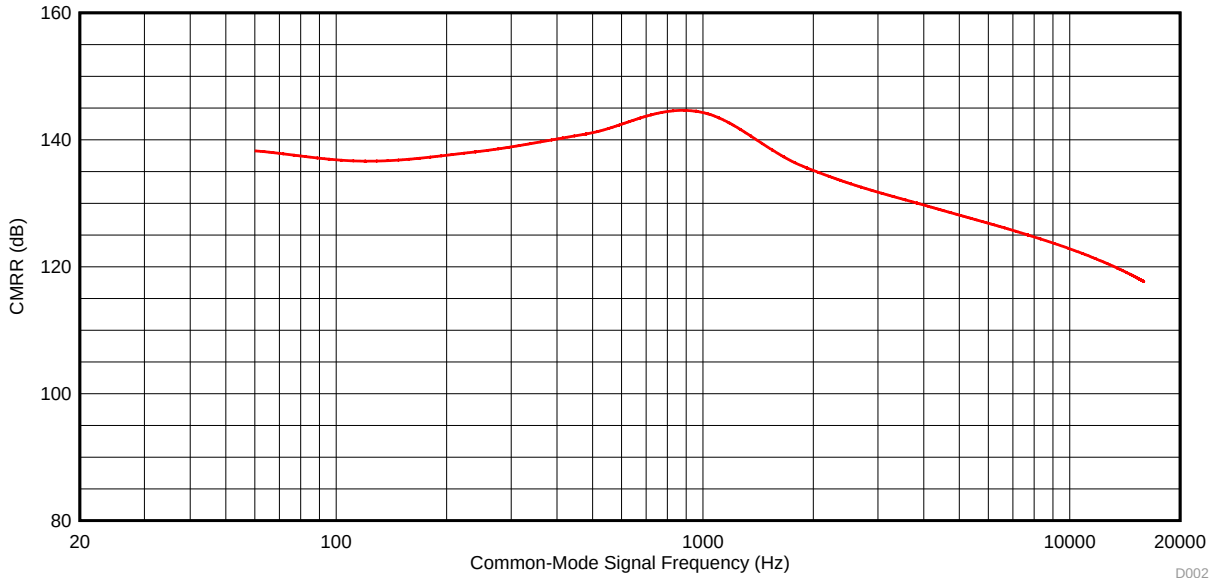


Figure 31. CMRR vs Frequency of Isolated DAQ Block

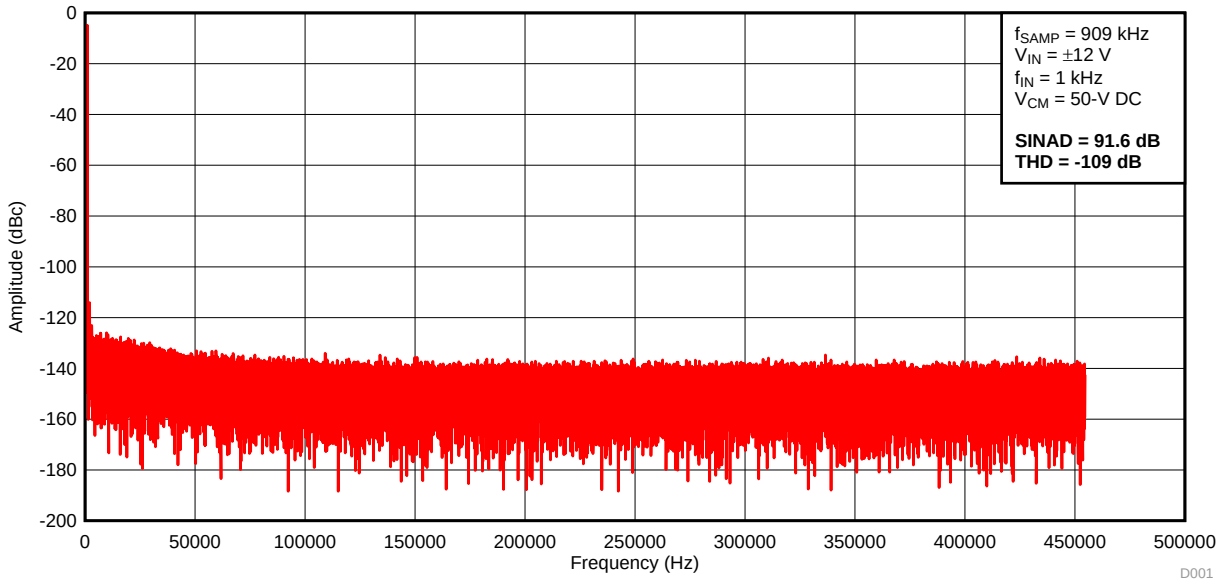


Figure 32. AC Performance of Isolated DAQ Channel at DC Common Mode

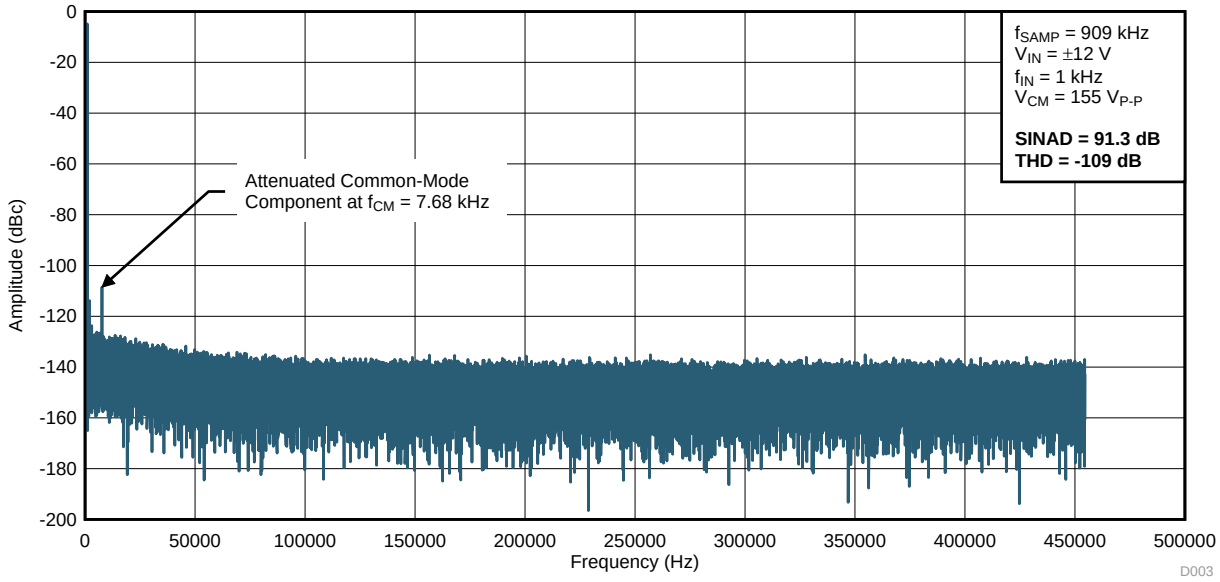


Figure 33. AC Performance of Isolated DAQ Channel at 7.68-kHz Common Mode

5 Modifications

5.1 ADC

The ADS8681 provides excellent dynamic range for acquiring lower bandwidth signals, but the input bandwidth is limited to 15 kHz by an integrated second-order low-pass filter. If the input signal frequency is several tens or hundreds of kHz, then a high-performance SAR ADC such as the ADS8860 is still a great option; however, a discrete signal path must be designed. For a detailed example of precision signal chain design for the 18-bit 1-MSPS acquisition of a 10-kHz input signal, refer to the TIPD113 TI Precision Design (SLAU513).

5.2 Digital Isolator

As explained in Section 3.2, it may be possible to tolerate a lower signaling rate and higher propagation delay while still achieving a 1-MSPS throughput rate if both SDO channels of the ADS8681 can be used (along with delay compensation if necessary). This task requires an extra I/O channel on the MCU, but the tradeoff may be worth the simpler timing requirements and the possible reduction in component costs relative to the isolator and perhaps even the MCU itself. Possible alternatives to the ISO7640 may include the ISO7140 and ISO7240 devices.

5.3 Transformer Driver

The SN6505 device is a compelling alternative to the SN6501 device because of the features outlined in Section 3.3.3. TI also recommends the TPS55010, but the device requires a different topology than the one used in this design.

6 Design Files

6.1 Schematics

To download the schematics, see the design files at TIDA-00106.

6.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00106.

6.3 Layout Guidelines

To download the layout guidelines, see the design files at TIDA-00106.

6.3.1 PCB Layout

In general, device-specific layout recommendations are clearly specified in the EVM user's guide or datasheet associated with the device. Because these recommendations have been tried and tested through rigorous performance validation, TI recommends replicating the recommended layout structures as closely as possible.

In addition, TI recommends emulating the following best practices:

- Analog and digital routing must be kept physically separated on the board to minimize cross-talk
- Connect bypass capacitors to their loads through short, low impedance traces
- Use multiple vias to connect bypass capacitors to the ground plane; this helps minimize inductance in the path of the return current (and reduces noise)
- Do not place a via in the path of another current loop; this elongates the current path and increases inductance
- For good common-mode rejection, differential input paths should be routed as symmetrically as possible so that the input impedances of the individual paths are closely matched

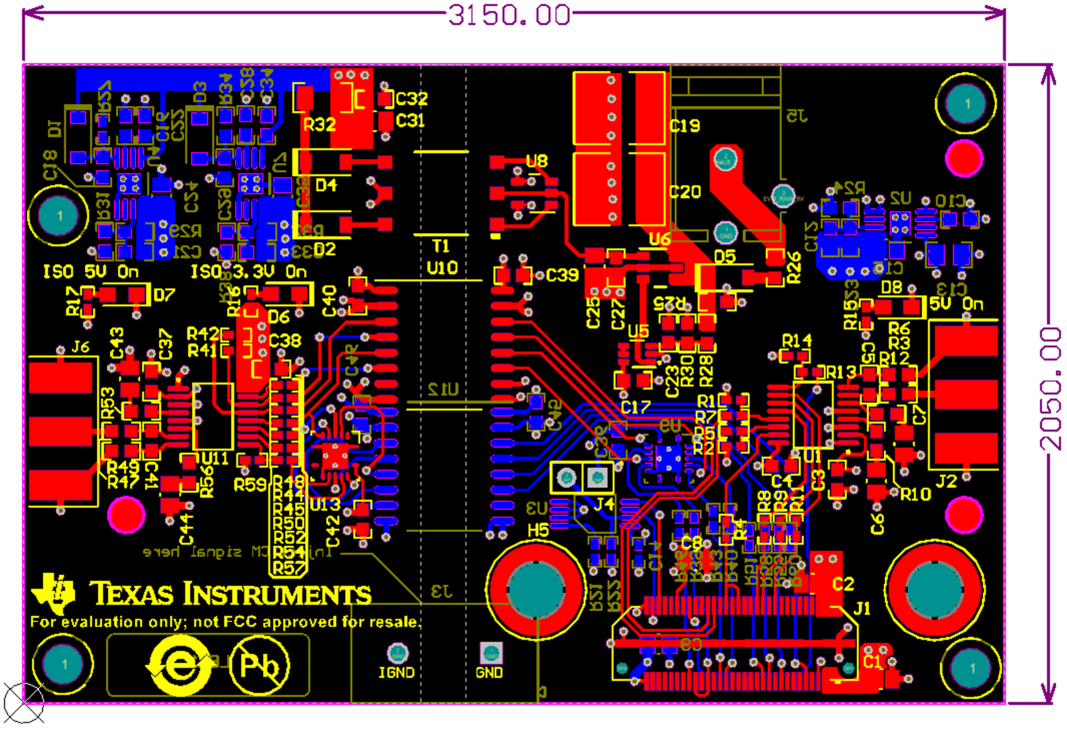


Figure 34. PCB Layout

6.4 Gerber Files

To download the Gerber files, see the design files at TIDA-00106.

6.5 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-00106.

6.6 Software Files

To download the software files, see the design files at TIDA-00106.

7 References

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9 About the Author

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