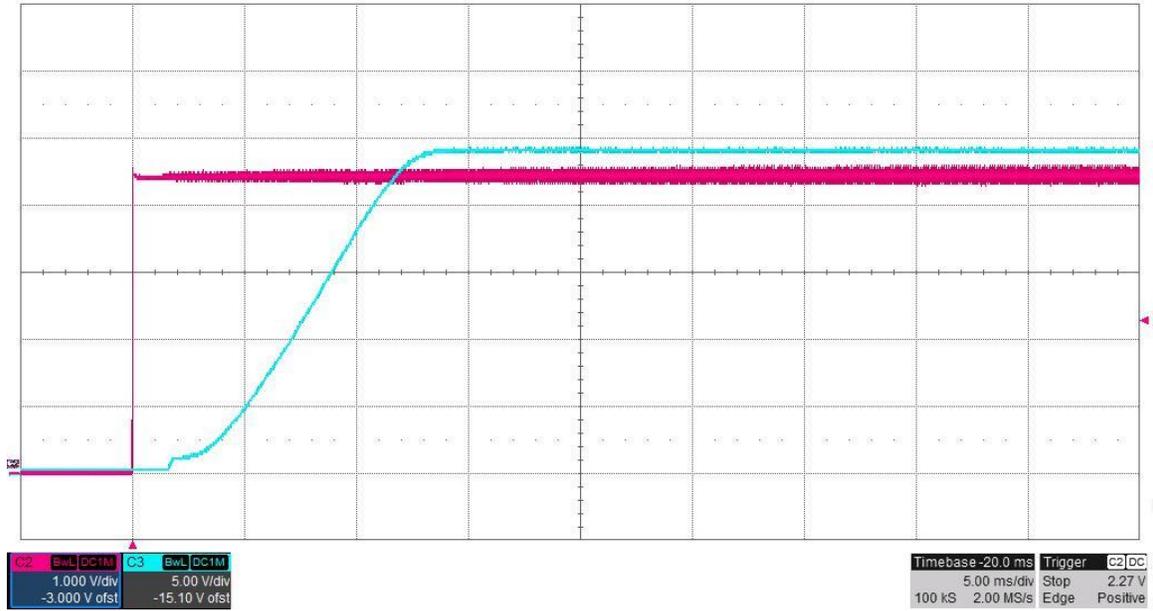
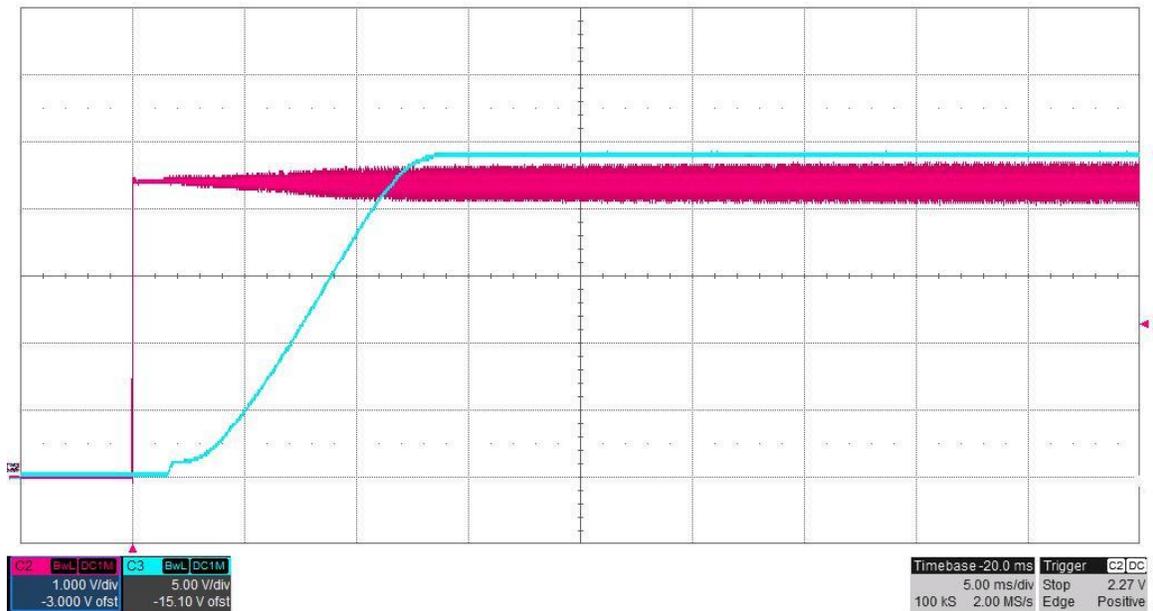


1 Startup

The photo below shows the 24V output voltage startup waveform after the removal of ENABLE jumper J2. $V_{in} = 48V$, $I_{out} = 0A$. ($V_{out}: 5V/DIV$, Enable J2-1: $1V/DIV$, $5mS/DIV$)

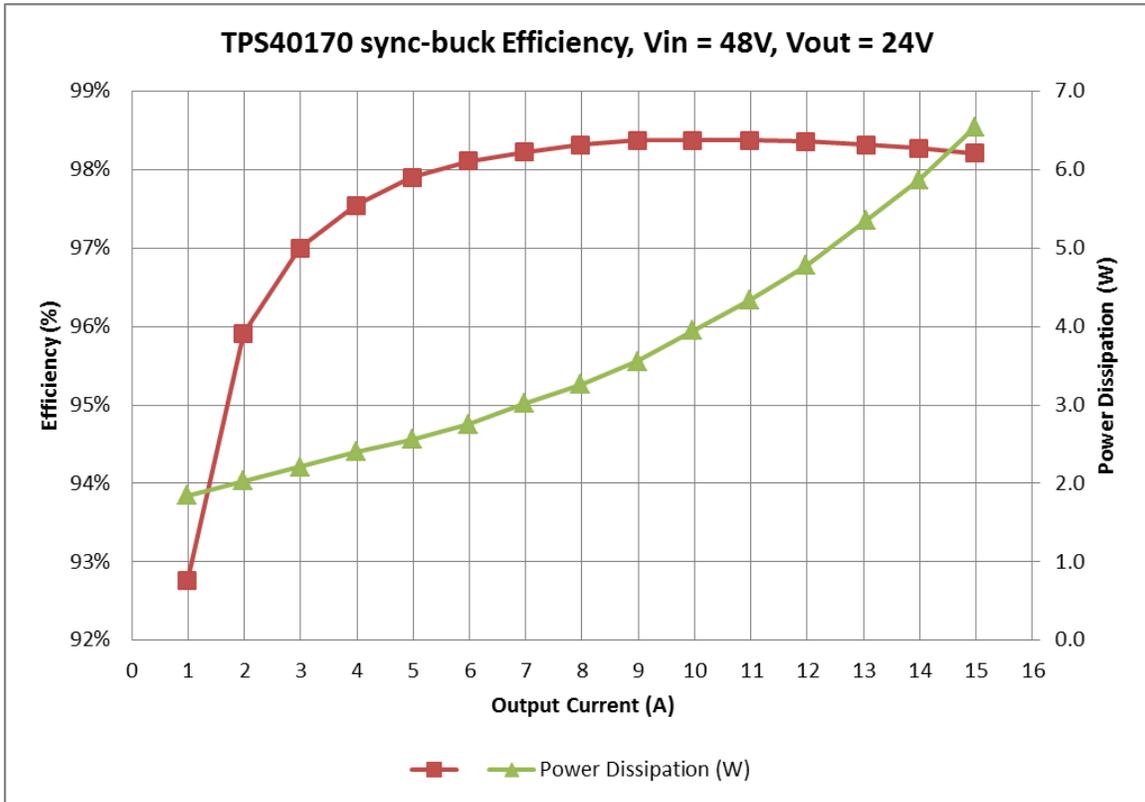


The photo below shows the 24V output voltage startup waveform after the removal of ENABLE jumper J2. $V_{in} = 48V$, $I_{out} = 12A$. ($V_{out}: 5V/DIV$, Enable J2-1: $1V/DIV$, $5mS/DIV$)



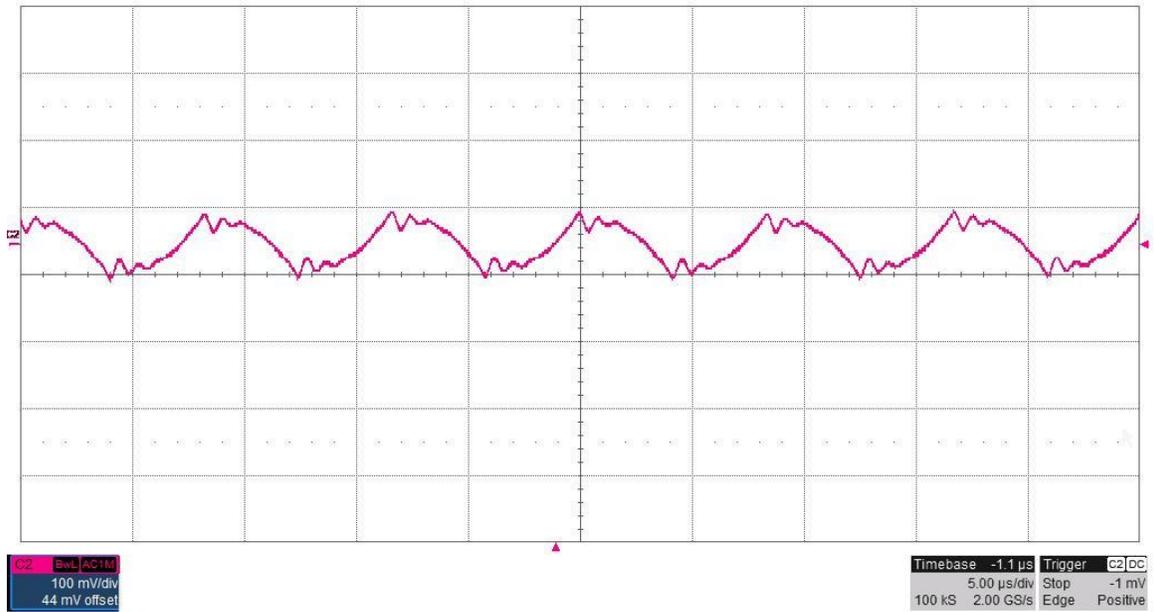
2 Efficiency

The converter efficiency is shown in the figure below.



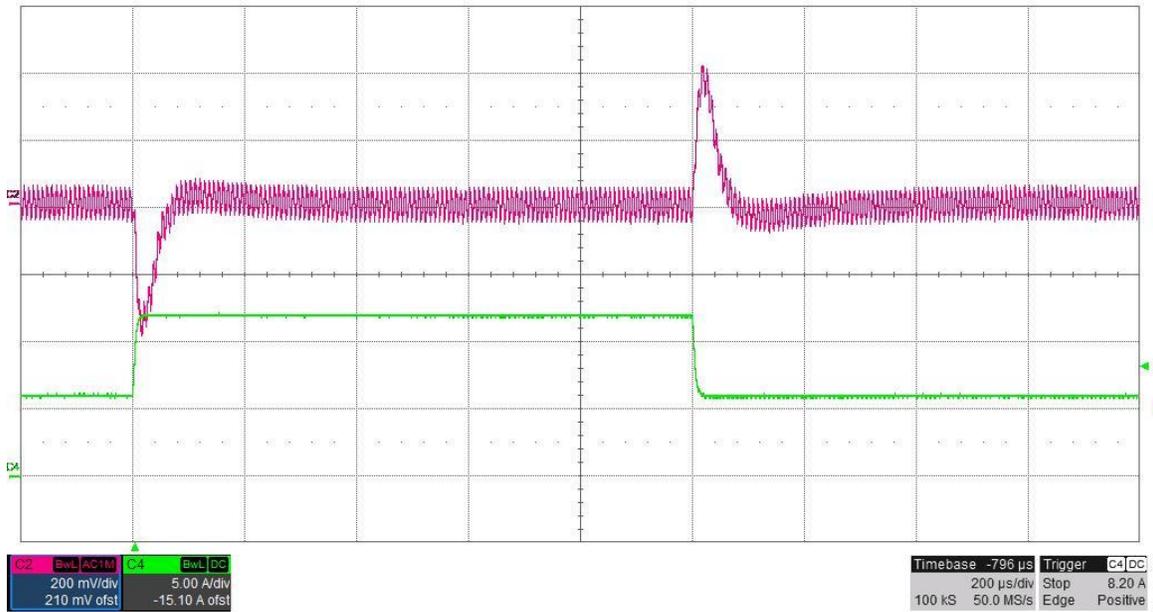
3 Output Ripple Voltage

The output ripple voltage is shown in the figure below. The image was taken with the 24V output loaded to 15A and the input voltage set to 48V. (100mV/DIV, 5uS/DIV)

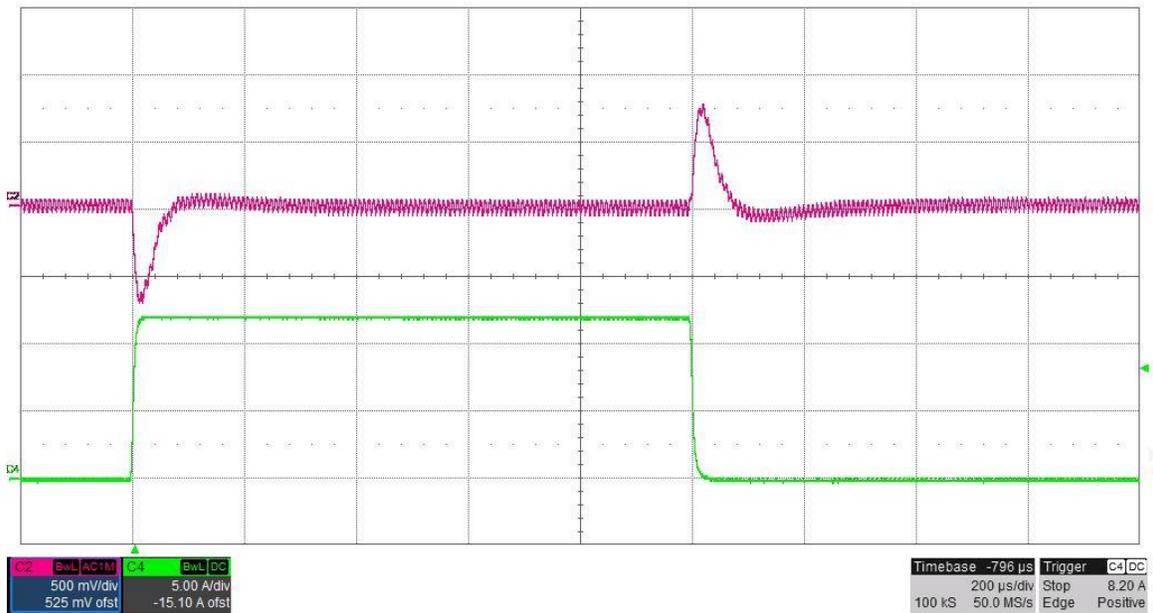


4 Load Transients

The photo below shows the 24V output voltage (ac coupled) when the load current is stepped between 6A and 12A. $V_{in} = 48V$.
(200mV/DIV, 5A/DIV, 200uS/DIV)

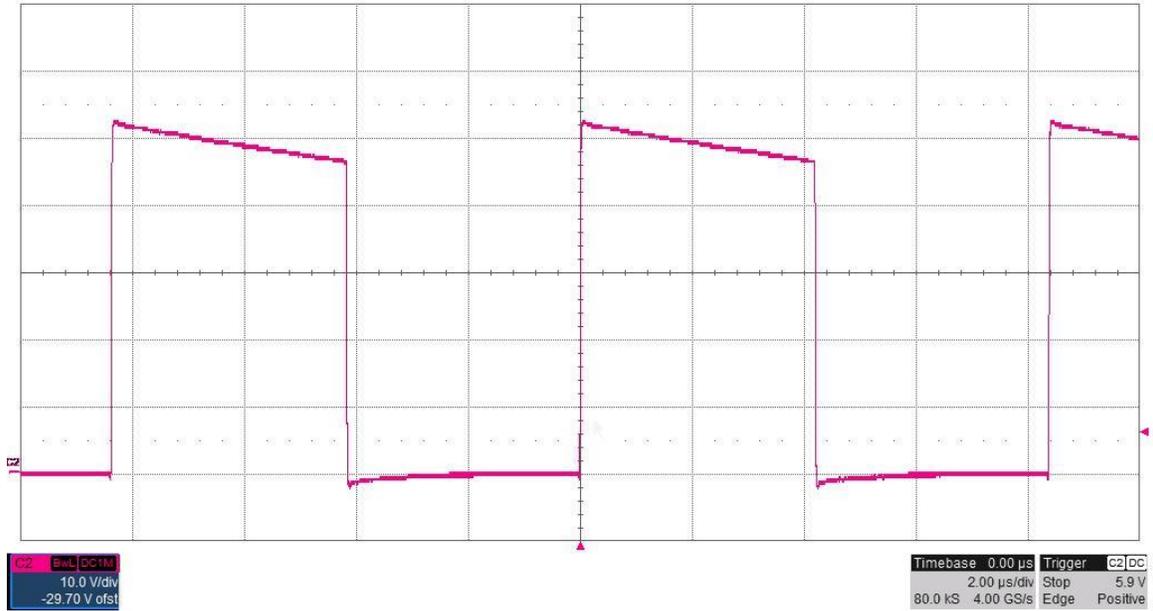


The photo below shows the 24V output voltage (ac coupled) when the load current is stepped between 0A and 12A. $V_{in} = 48V$.
(500mV/DIV, 5A/DIV, 200uS/DIV)

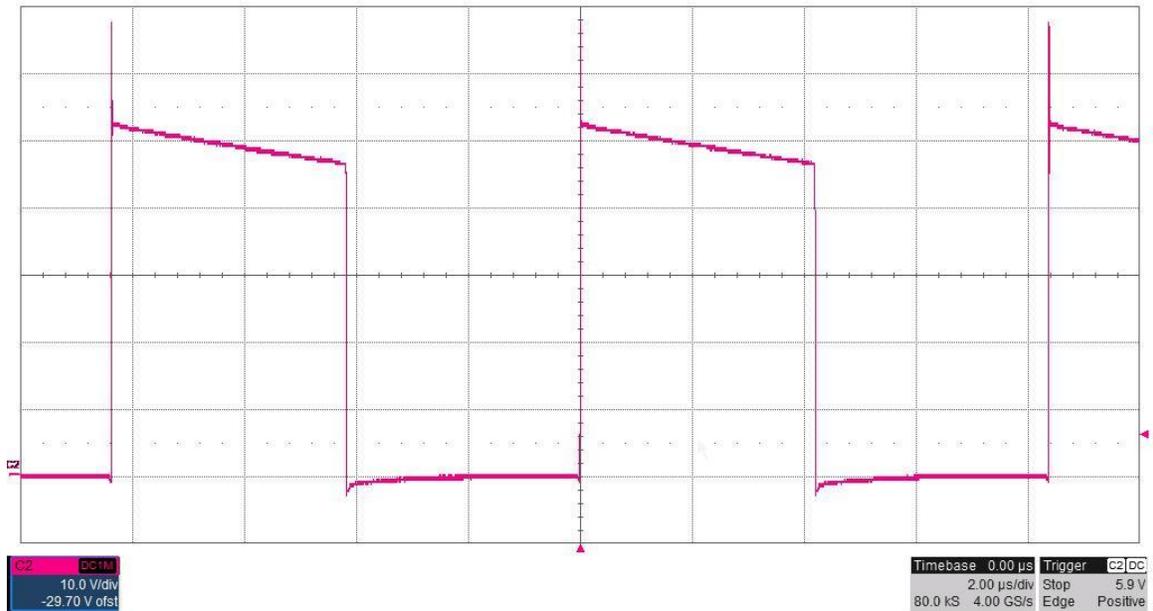


5 Switch Node Waveforms

The photo below shows the switch node voltage. The input voltage is 48V and the 24V output is loaded to 15A, BWL = 20MHz (10V/DIV, 2uS/DIV)



The photo below shows the switch node voltage. The input voltage is 48V and the 24V output is loaded to 15A, BWL = 500MHz (10V/DIV, 2uS/DIV)



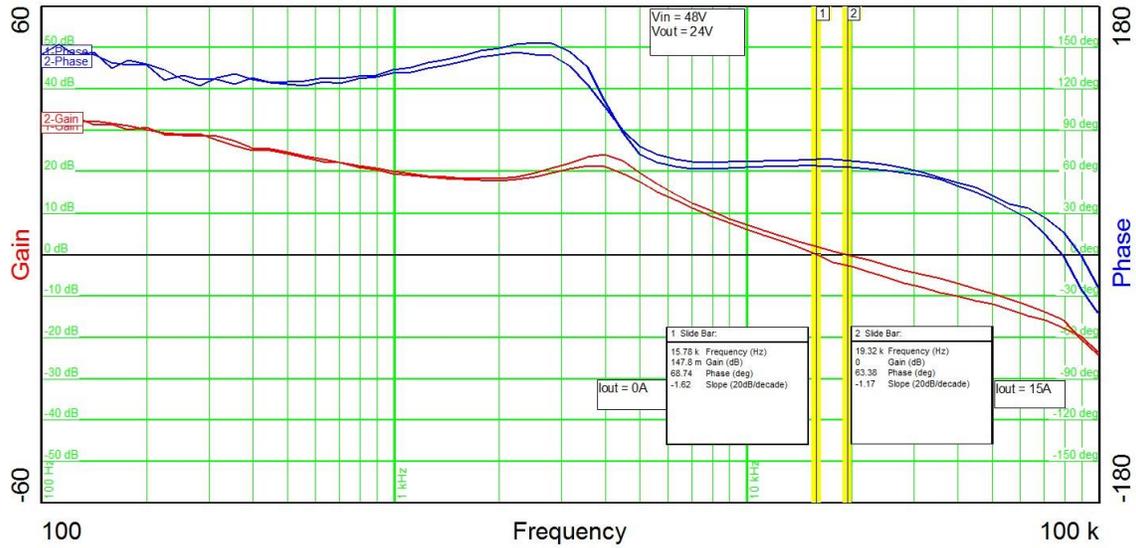
6 Control Loop Gain / Stability

The plot below shows the converter's loop gain and phase margin for $V_{in} = 48V$.

$I_{out} = 15A$
 $I_{out} = 0A$

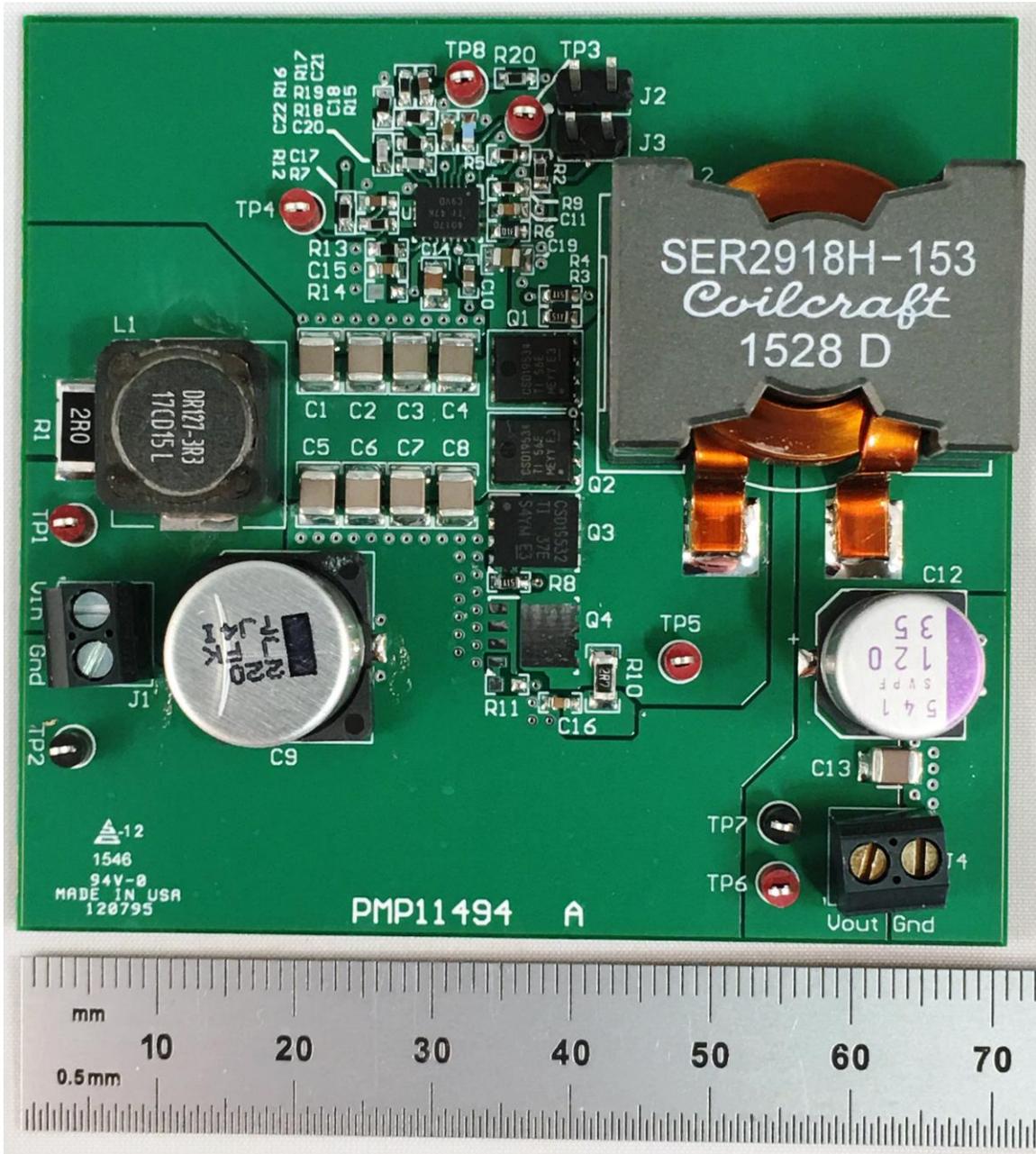
Band Width = 19.3KHz
Band Width = 15.8KHz

Phase Margin = 64 degrees
Phase Margin = 69 degrees



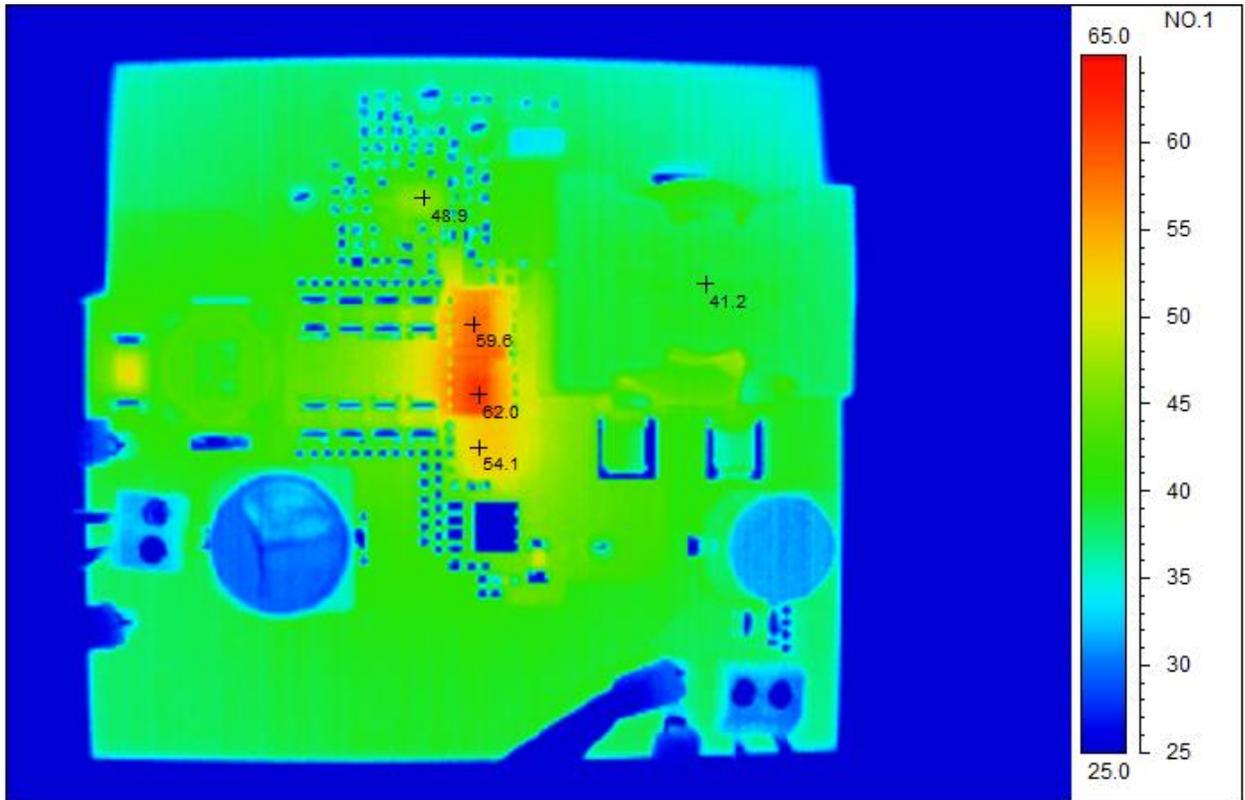
7 Photo

The photo below shows the PMP11494 REVA evaluation board.



8 Thermal Image

The thermal image below shows operation at 48V input and 24V@12A output with no airflow.



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