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Synchronized Multi-Transmitter Design: Method of Time-Aligning Multiple DAC3xJ8xs in JESD204B Environment

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Design Resources

TIDA-00996	Tool Folder Containing Design Files
TSW14J56 EVM	Tool Folder
DAC38J84 EVM	Tool Folder
LMK04828	Product Folder
DAC39J84	Product Folder
DAC39J82	Product Folder
DAC38J84	Product Folder
DAC38J82	Product Folder
DAC37J84	Product Folder
DAC37J82	Product Folder

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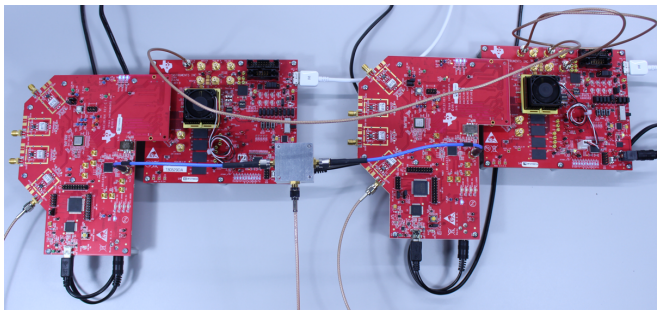
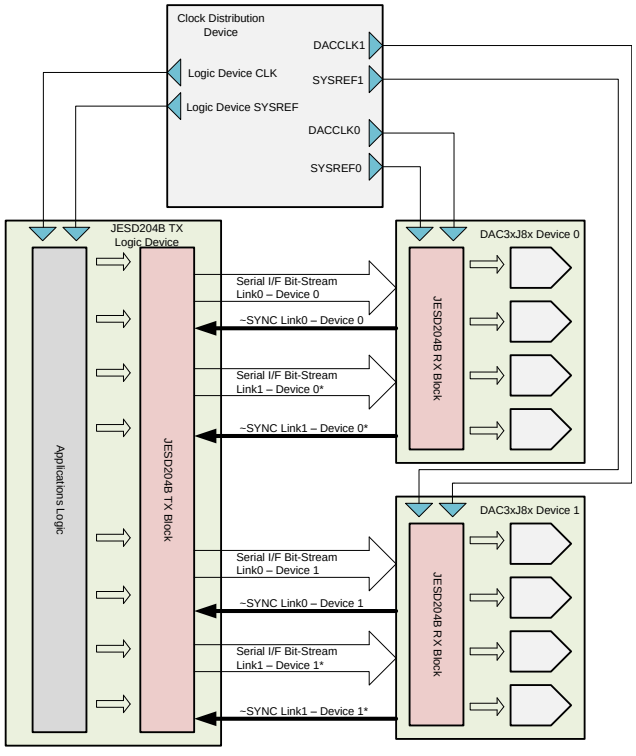


Design Features

- High-Speed Data Transfer
- High Sample Rate Digital-to-Analog Conversion
- JESD204B Subclass 1 Support
- Multi-Device Synchronization
- Synchronized Clock Distribution

Featured Applications

- Multiple Input Multiple Output (MIMO)
- Beam-Forming Antenna



*Link1 usage is optional for the DAC3xJ8x

1 System Description

To further increase the range, data rate, and reliability of modern mobile communications systems, system designers continue to place more emphasis on multiple-antenna transmitter systems to achieve combinations of spatial diversity and spatial multiplexing. Such implementations can further compensate for path loss and the multipath effect of transmission mediums. These implementations can also potentially increase range and data rate and improve reliability. Multiple-antenna systems with beamforming techniques also allows for better focus of transmitter energy and the system can potentially reduce the size of an antenna while increasing the transmitter range. More mobile communications systems and radar systems are starting to adopt multiple-antenna transmitters in their designs.

For such multiple-antenna transmitter implementations, each individual transmitter requires digital-to-analog converters (DACs) for the digital bits to RF transmission. Multiple transmitters and the associated antenna must also be synchronized in time. The design may utilize JESD204B subclass 1 type DAC3xJ8x, which has the capability to achieve multiple DAC3xJ8x device synchronization. The DAC3xJ8x is a high-speed 16-bit DAC with up to 2.8 GSPS of sample rate. All of the capabilities of DAC3xJ8x simplify device synchronization and facilitate the design of a multiple-antenna transmitter system.

Demonstrating the multiple-antenna transmitter system with multiple DAC3xJ8x device output synchronization requires two DAC3xJ8x EVMs and two TSW14J56 EVMs, which have been configured with delay matched DACCLK and SYSREF signals. The two TSW14J56 evaluation modules (EVMs) function as field-programmable gate array (FPGA) based pattern generator cards, which can be configured to provide a simultaneous triggered output with the SYSREF signals to the synchronized TSW14J56 EVMs.

1.1 DAC3xJ8x JESD204B Interface High-Speed DAC Family

The DAC3xJ8x family of DACs consists of low-power, 16-bit, dual-channel or quad-channel DACs with up to 2.8 GSPS of digital-to-analog conversion rate (see Figure 1). The digital data input is JESD204B subclass 1 based and the device supports up to eight configurable serial JESD204B lanes running up to 12.5 Gbps. The interface allows SYSREF-based deterministic latency for JESD204B subclass 1 and full synchronization of multiple devices.

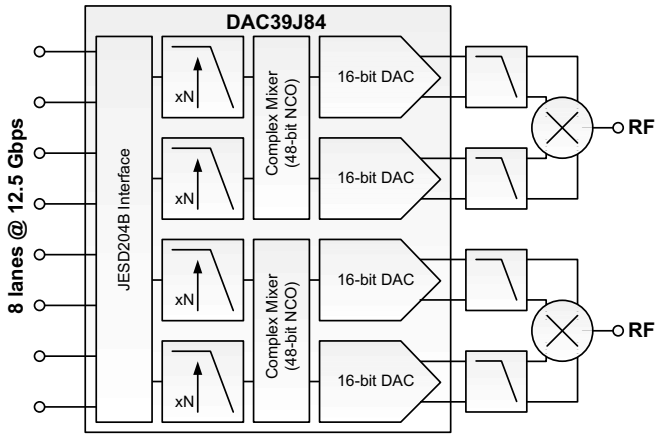


Figure 1. Typical Application Environment of DAC3xJ8x

1.2 LMK0482x JESD204B Family of Compliant Clock Jitter Cleaners

The LMK0482x family is the industry's highest performance clock conditioner with JESD204B support. With up to 14 clock outputs from the low jitter synthesizer, the output can be configured to support JESD204B with up to seven JESD204B converters and logic devices with both logic clock and SYSREF signal. Figure 2 shows the typical applications environment of the LMK0482xB device.

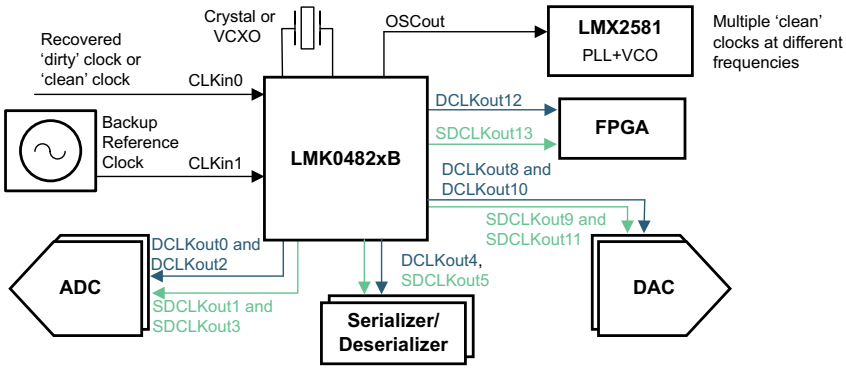


Figure 2. LMK0482xB Simplified Schematic

2 Block Diagram

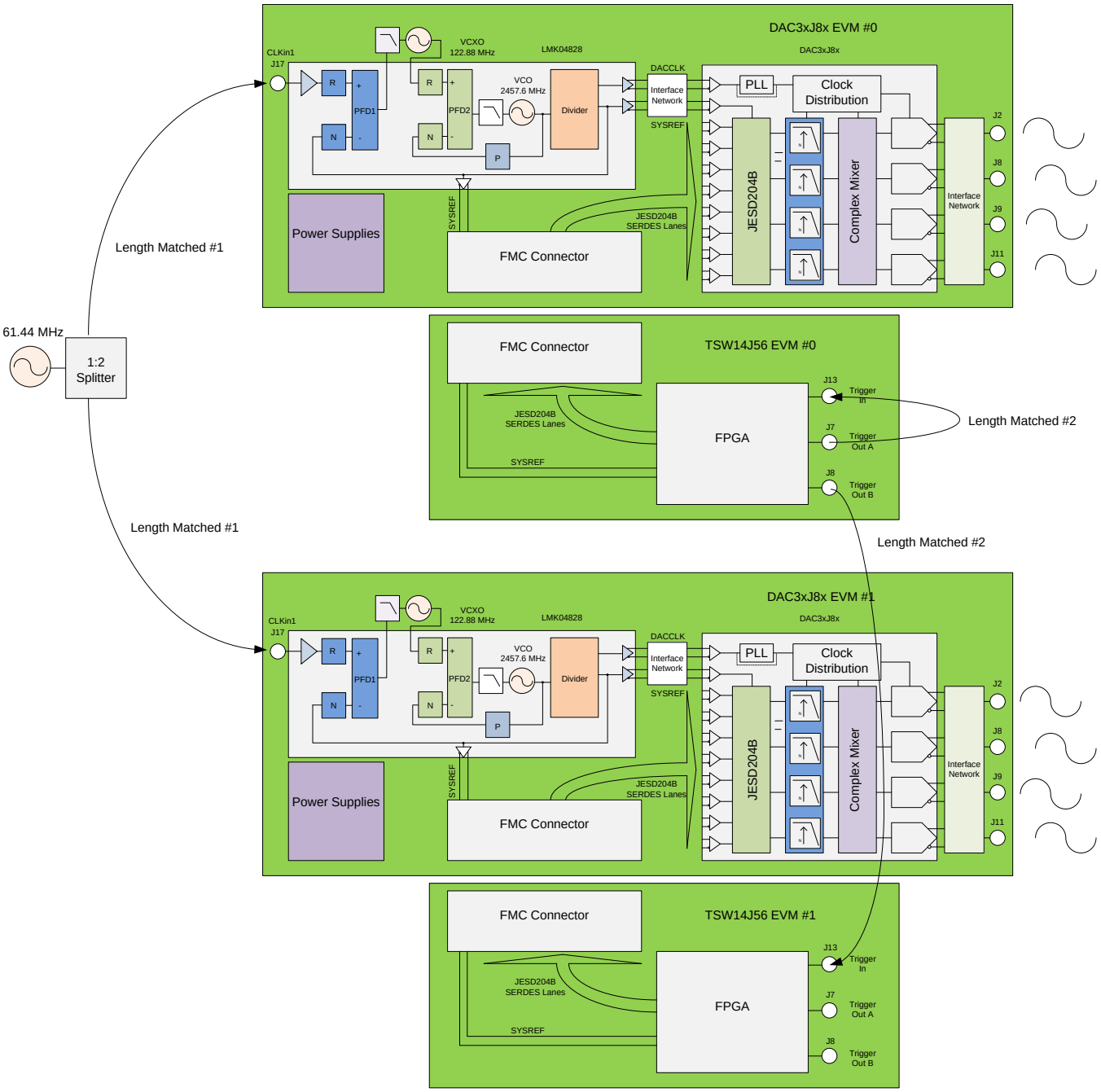


Figure 3. Overall Measurement Setup to Achieve Multiple DAC3xJ8x Device Synchronization

3 Highlighted Products

3.1 DAC37J82, DAC37J84, DAC38J82, DAC38J84, DAC39J82, and DAC39J84

For more information on these devices, view the respective datasheet at www.ti.com.

3.2 LMK04821, LMK0486, and LMK04828

For more information on these devices, view the respective datasheet at www.ti.com.

3.3 TSW14J56 EVM

For more information on the TSW14J56, view the tool folder at http://www.ti.com/tool/tsw14j56evm.

3.4 TRF3705, TRF37T05, and TRF3722

For more information on these devices, view the respective datasheet at www.ti.com.

4 System Design Theory

4.1 Multiple JESD204B DAC Synchronization

4.1.1 Introduction to JESD204B Interface

As the throughput of data converters increase as a result of increasing channel count and sample rates, conventional low-voltage differential signaling (LVDS) and complementary metal-oxide semiconductor (CMOS) interface technologies struggle to efficiently deliver (or receive) the payload data to digital signal processors (FPGA or ASIC). The inefficiencies exist in the power consumption and board area used by LVDS or CMOS interfaces. A JESD204B interface solves this efficiency problem by using a multi-gigabit transceiver technology to interface between a data converter and an FPGA or ASIC (see Figure 4).

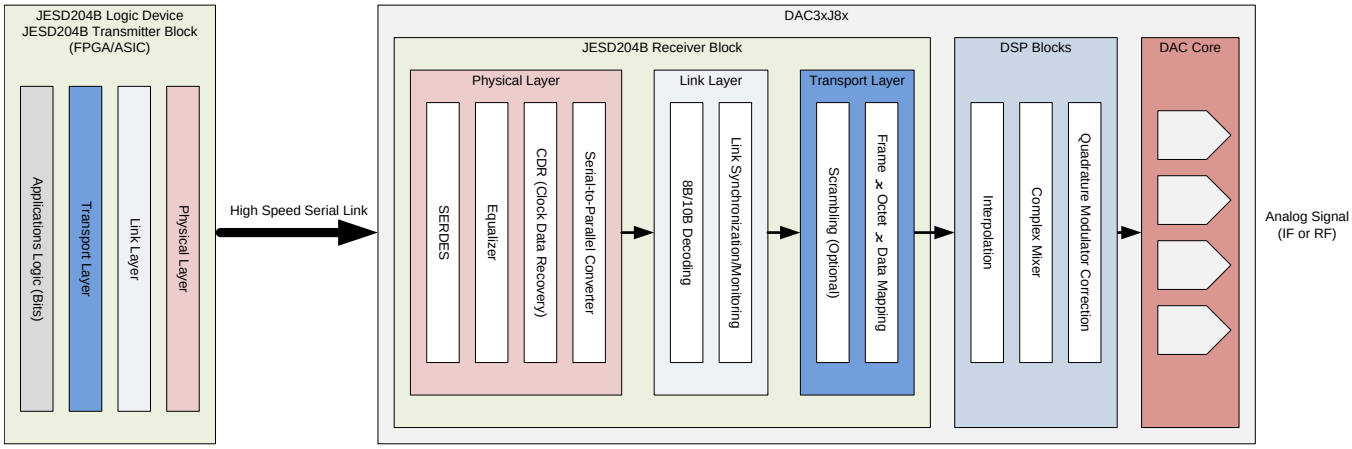


Figure 4. DAC3xJ8x JESD204B Receiver Block and Overall JESD204B Environment

Figure 4 shows the JESD204B receiver block of the DAC3xJ8x and the interface with the JESD204B logic device (that is, FPGA or ASIC). The various layers that make up the interface include the physical layer, link layer, and transport layer. The data sample that transfers through a high-speed serial link from the JESD204B logic device first travels through the physical layer of the DAC3xJ8x JESD204B block. The physical layer includes eight pairs of high-speed receivers to accept the high-speed serial data, enhances the signal through an equalizer to compensate the loss through the PCB traces, and performs internal serial-to-parallel conversion. The data link layer then decodes the encoded data in 8B/10B decoding fashion. After the decoding process, the transport layer then unpacks the data stream into bits, which then go through additional digital signal processing logics. Finally, the processed signal is converted into an analog signal through the DAC core.

4.1.2 Frame Clock, Local Multiframe Clock, and SYSREF Signal

Because the JESD204B RX block operates in a serial-to-parallel fashion for data transfer, the data streams are packed in frames of octets (defined as “F”). The logic includes a frame clock to ensure the serial-to-parallel conversion occurs at the correct rate. Because the DAC3xJ8x also supports deterministic latency (mandatory for JESD204B subclass 1 devices) and multiple lanes, the internal data is also arranged in multiples of frames or multiframes (defined as “K”). The multiframes are aligned to the edges of the local multiframe clock (LMFC), which is internal to the JESD204B receiver block.

The concept of the LMFC and the associated alignment requirements are critical in applications that require deterministic latency and multiple device synchronization. In a JESD204B system environment, both the JESD204B TX and JESD204B RX have their own LMFC. The key to achieving deterministic latency, multiple device synchronization, or both is to ensure that the LMFC of each JESD204B device in the JESD204B system environment are aligned. The end result of the LMFC alignment is that the data transfer is performed in a synchronized manner throughout the link. The JESD204B subclass 1 standard has the following requirements for achieving an LMFC alignment:

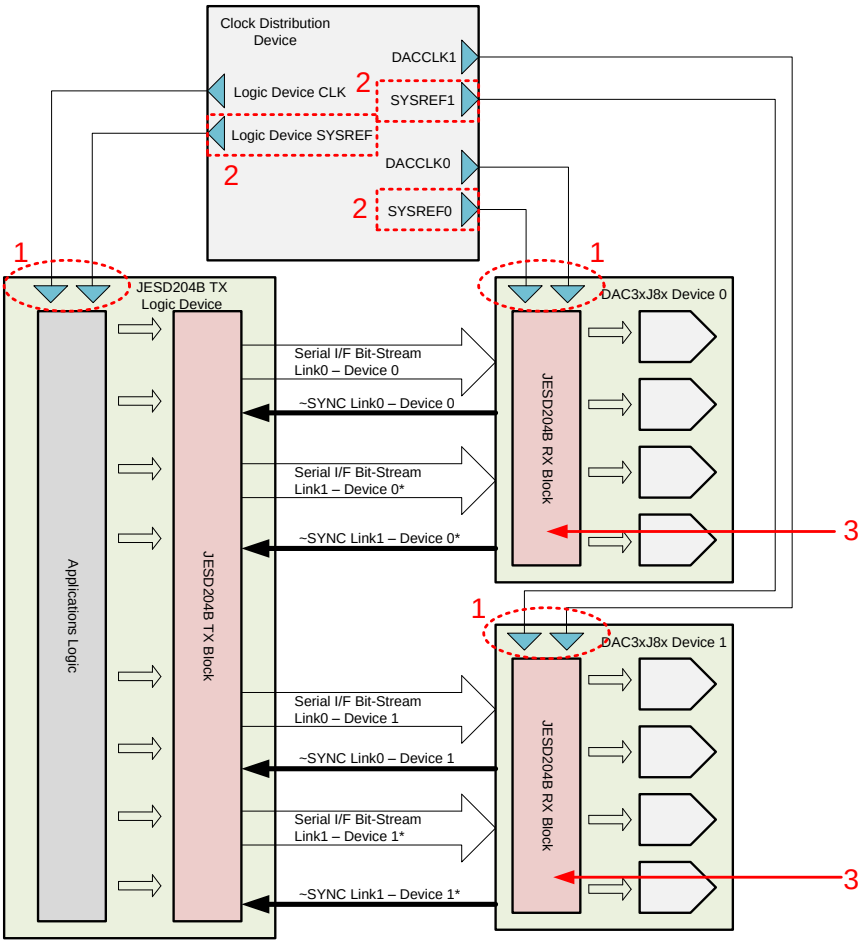
1. The JESD204B standard specifies that the frame period and multiframe period must be identical in both the JESD204B TX and JESD204B RX. This qualification implies that all the data packing and transfers must occur in the same fashion.
2. The LMFC clock in each JESD204B subclass 1-specific device is aligned through a synchronized timing reference (SYSREF) signal, which is globally distributed throughout the JESD204B system environment. The standard recommends that SYSREF be generated from the same clock distribution device producing the JESD204B TX and JESD204B RX clocks.
3. If the LMFCs of all the JESD204B devices in the system are aligned, then the data transfer occurs at the same rate and the same instant, which means that the devices are synchronized.

Note that the above requirements are a summary of the JESD204B standard. For more details, refer to the JESD204B standard documentation.

4.1.3 Theory of Synchronization Across JESD204B Links

The alignment of LMFC through global SYSREF in a JESD204B subclass 1 system environment simplifies the synchronization of multiple devices. Figure 5 shows a typical subclass 1 type system for JESD204B TX and JESD204B RX. The DAC3xJ8x device supports up to eight JESD204B lanes and up to two JESD204B RX links (that is, link 0 and optional link 1). Each JESD204B subclass 1 device has a device clock and SYSREF signal routed globally from a clock distribution device.

As Figure 5 shows, the system design must meet the following three main requirements to successfully synchronize multiple JESD204B devices.



*Link1 usage is optional for the DAC3xJ8x

Figure 5. Typical Setup for Multiple JESD204B Links for DAC3xJ8x Devices

1. *Phase align device clocks at each converter or logic element:*
   This step is critical because all clocks, such as the sampling clock, frame clock, character clock, bit clock, and LMFC, are generated from this common source. Ensuring that the distribution of the device clock to all devices is well matched is a necessary condition to guarantee a deterministic phase relationship.
2. *Generate and capture the proper SYSREF signal to all the devices:*
   The SYSREF is used to align the phase of the clock dividers and multipliers used to generate all of the internal clocks. This timing reference can be provided through the SYSREF receiver input of the DAC3xJ8x. The SYSREF signal aligns the internal LMFC of each JESD204B device such that the data transfer throughout the link is synchronized.
3. *Achieve multiple device synchronization by choosing an appropriate elastic buffer release point:*
   Besides synchronized data transfer, the data transfer delay as a result of device-to-device routing must be compensated. The third requirement for synchronization is to select a proper elastic buffer release point in the JESD204B receiver, which is the key to achieve deterministic latency. The buffer absorbs variations in the propagation delays of the serialized data as the data travels from the transmitter to the receiver. A proper release point is one that provides sufficient margin against variations in the delays. An incorrect release point results in a latency variation of one LMFC period. Choosing a proper release point requires knowing the average arrival time of data at the elastic buffer (referenced to an LMFC edge) and the total expected delay variation for all devices. With this information the region of invalid release points within the LMFC period can be defined, which stretches from the minimum to maximum delay for all lanes. Essentially, the designer must guarantee that the data for all lanes arrives at all devices before the release point occurs.
   For instance, if the data path delay from the JESD204B TX logic device to the DAC3xJ8x device 0 is larger than the path to DAC3xJ8x device 1, the data transfer, although synchronized, is offset by the delta of the data path delay. The JESD204B RX logic has an internal built-in deterministic latency mechanism, which is a long buffer that can absorb large variations in data trace lengths (multiple inches) to compensate the delay delta among the data paths. The RX buffer for both DAC3xJ8x device 0 and DAC3xJ8x device 1 will have the same release point such that the released data for both devices will be the same at the same time instance. This requirement relaxes and eliminates requirements for any SERDES trace length matching for all data paths.

Figure 6 demonstrates this requirement by using a timing diagram that shows the data for two DAC3xJ8xs: DAC0 and DAC1. The DAC1 has a longer routing distance than DAC0 and results in a longer link delay. First, the invalid region of the LMFC period is marked off as determined by the data arrival times for all devices. Then, the release point is set by using the release buffer delay (RBD) parameter to shift the release point an appropriate number of frame clocks from the LMFC edge so that it occurs within the valid region of the LMFC cycle. In Figure 6, the LMFC edge (RBD = 0) is a good choice for the release point because there is sufficient margin on each side.

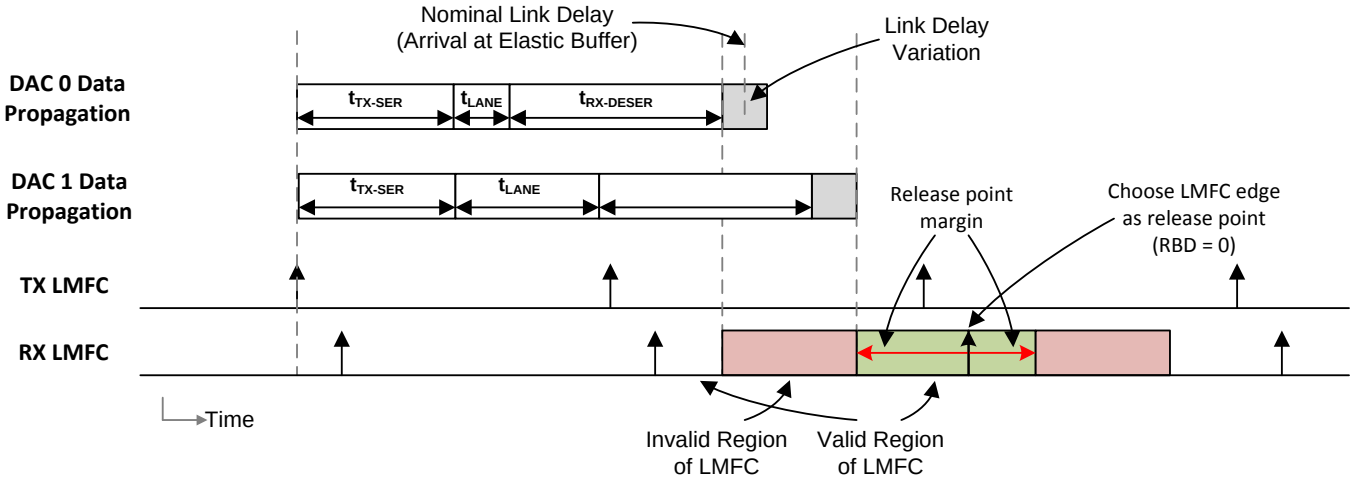


Figure 6. RBD Selection for the DAC3xJ8x JESD204B RX Link

The end result is that the DAC0 has more data stored in the RX buffer than the DAC1 RX buffer and has effectively absorbed the delay difference of the data paths. Basically the DAC0 RX logic waits and buffers data until the DAC1 RX logic has sufficient data before both buffers are released at the same time for the first sample stream.

4.2 Hardware Implementation of Multi-Transmitter System

4.2.1 Overview and Goal

The overall hardware setup requires two DAC3xJ8x EVMs and two TSW14J56 EVMs (see Figure 7). The goal of the multiple DAC3xJ8x device synchronization is to fix the latency across the interface from the FPGA and through the DAC signal processing. Each DAC3xJ8x device will have the sampling instant aligned at each DAC channel output.

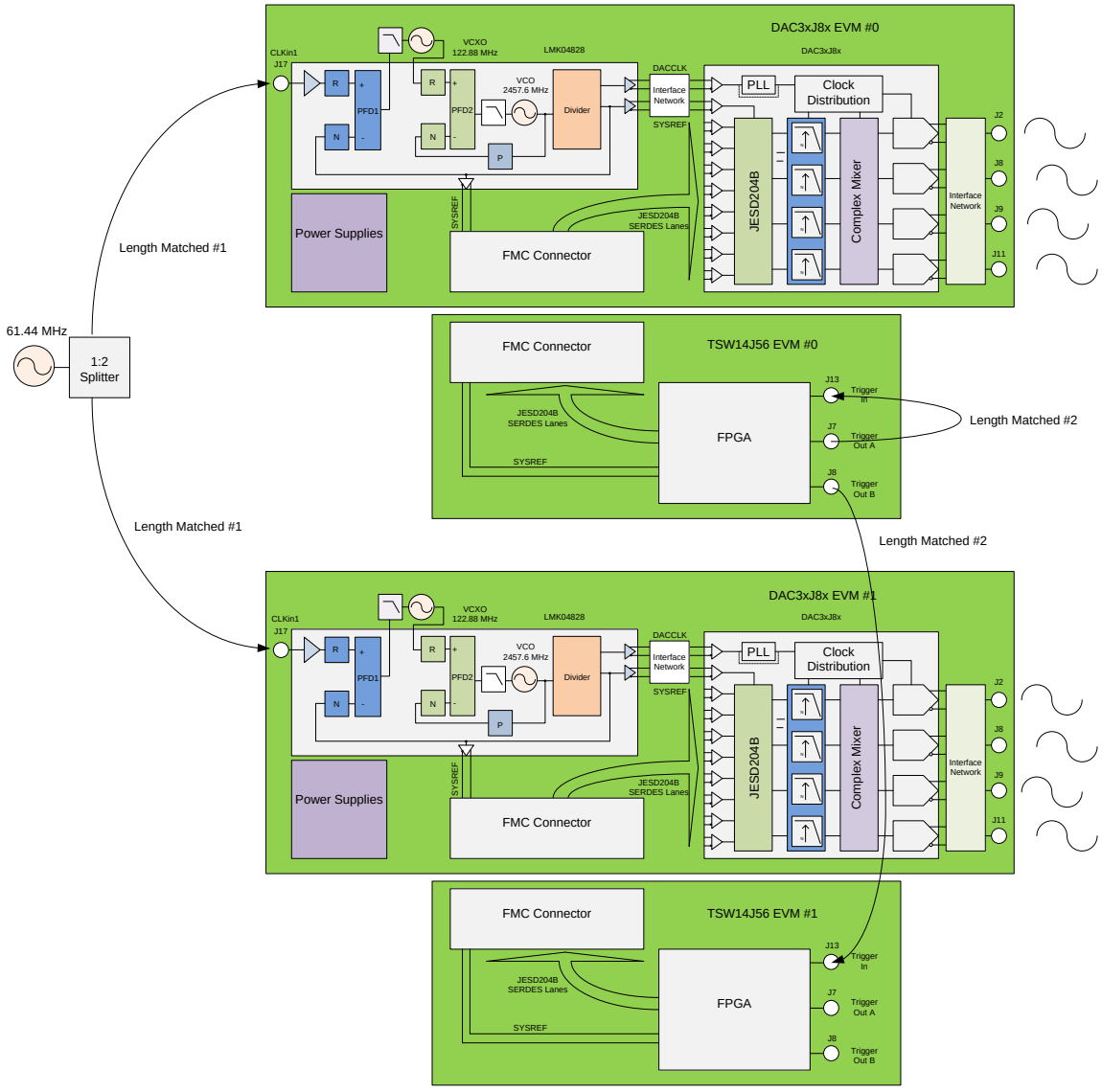


Figure 7. Overall Measurement Setup

4.2.2 Corresponding Configurations and Setup for Multi-DAC Synchronization Across JESD204B Links

1. *Phase align device clocks at each converter/logic element:*
   Phase alignment can be achieved by matching clock trace lengths to each device, or use programmable clock delays in clock chip. Each DAC3xJ8x EVM has an on-board LMK04828 clock distribution/PLL circuit. The LMK04828 provides the DACCLK and SYSREF to the DAC3xJ8x on the same board through matched differential PCB traces. It also provides the TSW14J56 FPGA the logic clock and SYSREF through FMC connector. Because the two DAC3xJ8x EVMs are identical, all the device clocks and SYSREF have the same delay; therefore, the phase alignments of the clock signals are matched by design. The LMK04828 also includes additional delay tuning settings, both digital tune and analog delay if additional adjustments are required.
2. *Generate and capture proper synchronized timing reference (SYSREF) signal to all the devices:*
   The LMK04828 is configured in nest 0-Delay to provide matched delay SYSREF to two DAC3xJ8x SYSREF receivers. See Section 4.3.2 for further details.
3. *Achieve multiple device synchronization by choosing an appropriate elastic buffer release point:*
   The details of choosing RBD value for the JESD204B RX logics have been described in earlier sections. The SERDES traces traveling through both DAC3xJ8x EVMs are identical and delay matched by design; therefore, both DAC3xJ8x can have the same RBD value without impacting the output delay.

4.3 LMK04828 Setup Concept

4.3.1 Synchronize Multiple SYSREF Outputs on Multiple LMK04828 Devices

Each DAC3xJ8x EVM has an LMK04828 clock synthesizer and distribution device. The LMK04828 can output the SYSREF signal to the DAC3xJ8x device on the EVM to achieve multiple DAC3xJ8x device synchronization. To achieve multiple DAC3xJ8x device synchronization, each DAC3xJ8x device must have a synchronized SYSREF and DACCLK signal. One approach to providing a synchronized SYSREF and DACCLK on multiple LMK04828 devices is to configure the LMK04828 in the nested 0-delay dual loop mode.

4.3.2 LMK04828 Nested 0-Delay Dual Loop Mode

Figure 8 shows the use case of a nested, cascaded, 0-delay dual loop mode. Note that the feedback for the overall PLL1 and PLL2 loop comes from the internal SYSREF output after the divider logic. Through the phase adjustment of the PLL1 and PLL2 negative feedback loop, the SYSREF output after the divider adjusts according to the CLKin path. In this configuration, the R-1 divider and N-1 divider before the PLL1 stage must be set to divide-by-1 mode. This setting ensures that the CLKin phase and the SYSREF phase remain the same through negative feedback. The important concept is that the phase detector of PLL1 (PFD1) ensures that the phases of positive phase input and negative phase input remain the same through negative feedback. Because both the R-1 divider and N-1 divider before the PLL1 stage are set to divide-by-1 mode, the phases among CLKin, positive phase input, SYSREF, and negative phase input are the same, which indicate that CLKin and SYSREF phases are also the same.

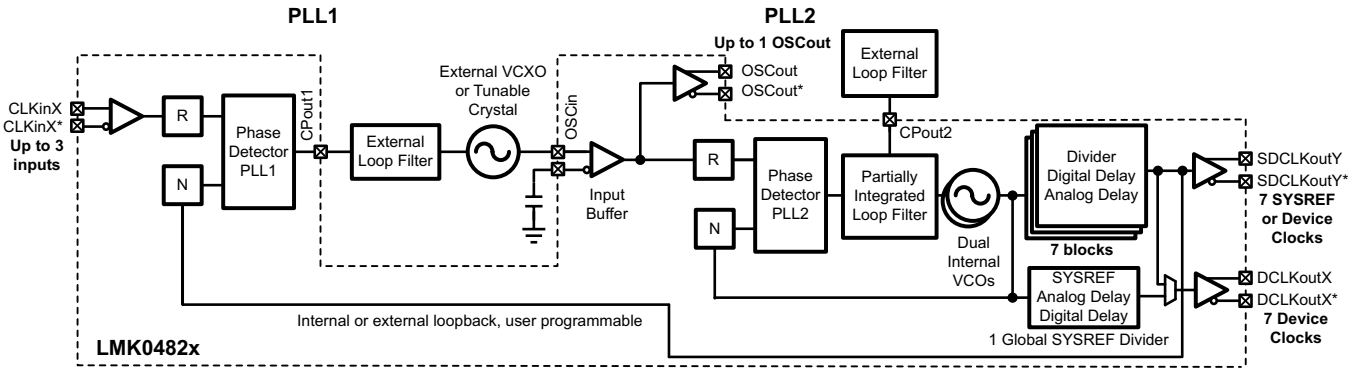


Figure 8. Simplified Functional Block Diagram for Nested 0-delay Dual Loop Mode (From LMK04828 Datasheet)

If these two dividers have not been set to divide-by-1 mode, then the actual phase between CLKin and SYSREF may vary. The R-1 divider and N-1 divider have a non-synchronous divide operation and cannot be initialized to be synchronous. Because every divide operation creates phase variations (meaning divide-by-2 creates 0° and 180° of the divide-by-2 clock and divide-by-4 creates 0°, 90°, 180°, and 270° variants of the divide-by-4 clock), the phase after the divide operation is non-deterministic. Even though the positive phase input and negative phase input of PFD1 are the same through negative feedback, the actual phase between CLKin and SYSREF is different because of the non-synchronous R-1 and N-1 divider. Any phase variations between the CLKin and SYSREF translate to delay variations and this behavior impacts synchronous initialization of multiple DAC3xJ8x devices.

5 Getting Started Hardware

5.1 Required Hardware

1. Two TSW14J56 EVMs Revision D
2. Two DAC3xJ8x EVMs Revision D
3. PC with DAC3xJ8x EVM graphical user interface (GUI) and High Speed Data Converter (HSDC) Pro GUI installed
4. 61.44-MHz reference clock split equally into two matched delay paths to subminiature version A (SMA) connectors
5. One pair of delay matched SMA cables (length matched #1)
6. Another pair of delay matched SMA cables (length matched #2); note that both length matched #1 pair and length matched #2 pair can also be matched if the conditions so require

5.2 DAC3xJ8x EVM Setup

5.2.1 DAC3xJ8x JESD204B Setup

Each DAC3xJ8x EVM has the DAC38J84 device installed. This EVM is the quad-channel version of the DAC3xJ8x family and operates up to 2.5 GSPS. The JESD204B setting is configured as a JESD204B LMF setting of 442 mode. This setting indicates that the DAC operates in four JESD204B lanes, four DAC devices, and two octets per frame. The K factor is set as 10, which indicates 10 frames per multiframe. The RBD value for both DACs is set at nine, which indicates that the JESD204B RX buffer is released right before the end of the LMFC period.

Each input channel has an effective data rate of 614.4 MSPS. With four times the interpolation ratio, the final DAC38J84 output sample rate is 2457.6 MSPS. The SERDES line rate (for each of the four lanes) is at 12.288 Gbps. With the LMF and K setting, the corresponding SYSREF frequency is 61.44 MHz (see Figure 9).

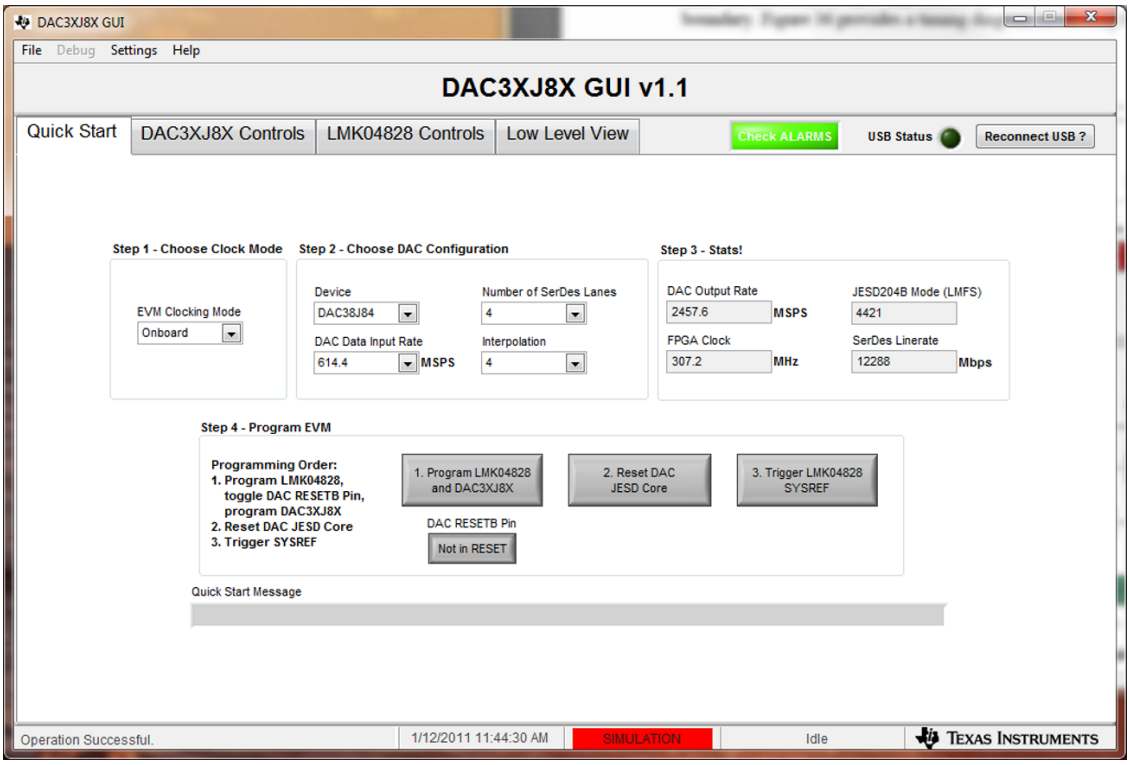


Figure 9. DAC38J84 Setting

5.2.2 LMK04828 Nested 0-Delay Dual Loop Setting

A single 61.44-MHz reference with equal power split and delay-matched cable length connects to the input of the LMK04828. The LMK04828 devices on the two DAC3xJ8x EVMs have been configured in nested 0-delay dual loop mode; therefore, the SYSREF outputs for the two LMK04828 devices have the same phase and delay relationship as the 61.44-MHz reference input.

The final DACCLK output of the LMK04828 is set to 2457.6 MHz and the SYSREF frequency is set to 61.44 MHz (see Figure 10).

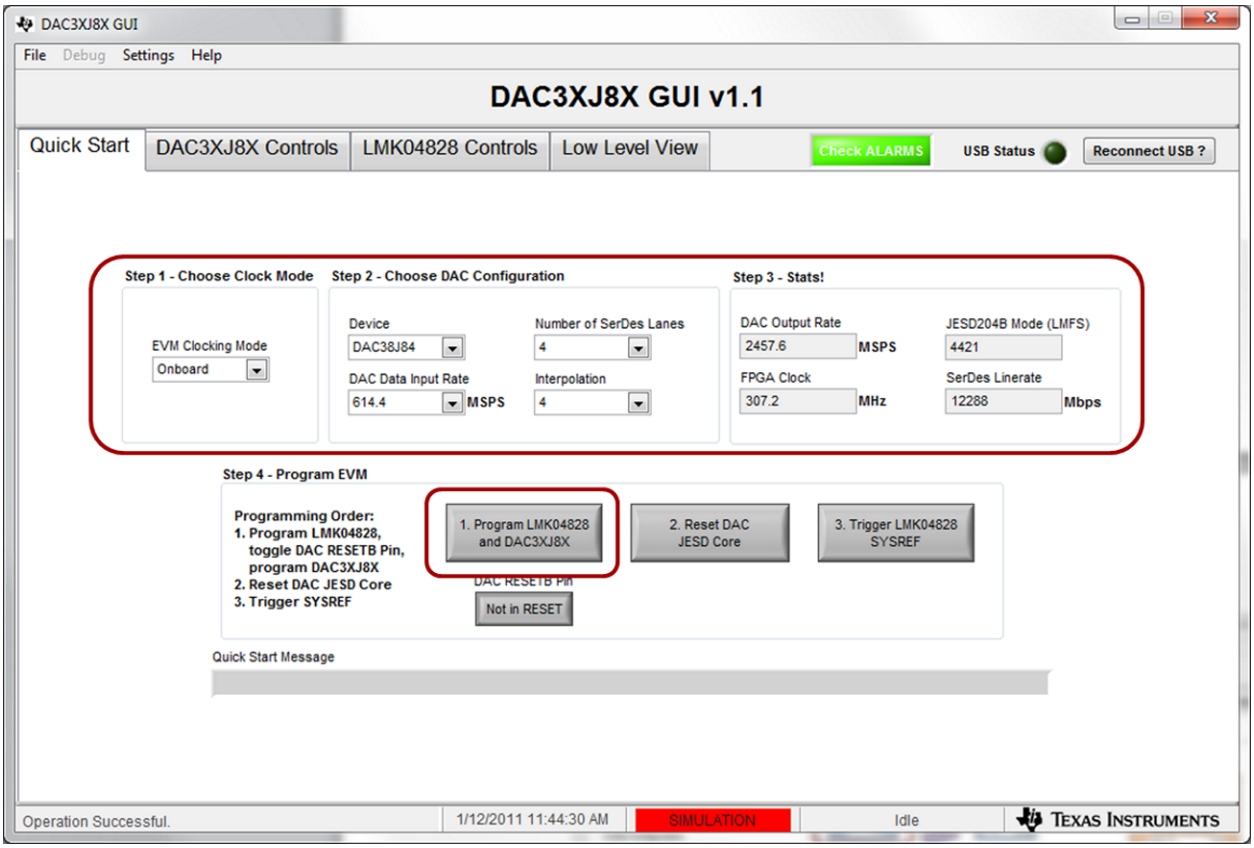


Figure 10. Two LMK04828 Nested 0-Delay Dual Loop Settings

5.3 TSW14J56 EVM Setup

5.3.1 Master/Slave Triggering

Because each TSW14J56 EVM can only establish a single JESD204B link, multiple JESD204B link synchronization requires multiple TSW14J56 EVMs. Note that if the JESD204B TX logic device platform supports multiple JESD204B links the master and slave triggering functionality is not required.

To ensure the alignment of the JESD204B link and alignment of output data, the two TSW14J56 EVMs are set up in master and slave mode (see Figure 11). The master board generates the main trigger signal to trigger both itself and the slave board. The cables routing from the trigger signal output from the master to its own trigger signal input and the slave board trigger signal input are delay matched. This delay match ensures accurate timing for the triggering mechanism.

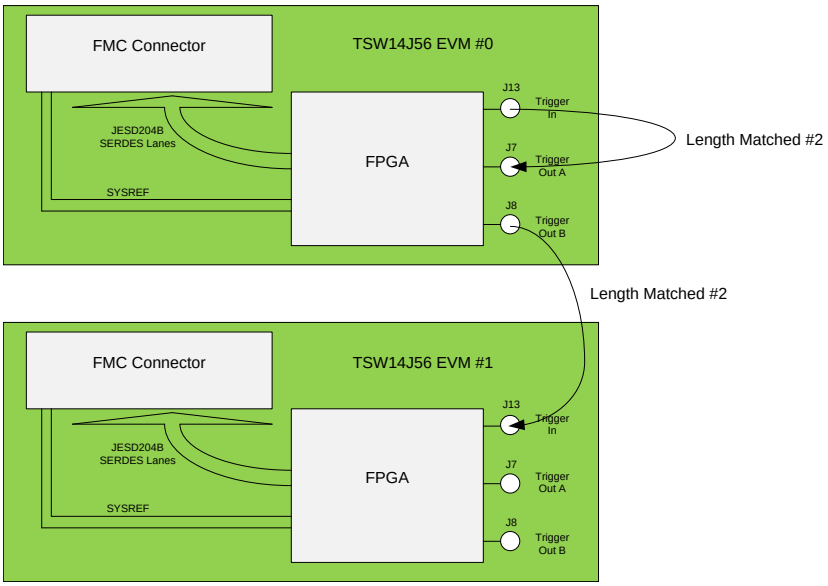


Figure 11. TSW14J56 EVM Master and Slave Trigger Setup

As Figure 11 shows, the TSW14J56 EVM0 is in master mode, while the TSW14J56 EVM1 is in slave mode. Each EVM has a “Trigger In” port at J13 and “Trigger Out A” port at J7. The TSW14J56 EVM0 has an SMA cable connected from its “Trigger Out A” port to its “Trigger In” port and the intention is to have this EVM configured in master mode so as to self-trigger with its own trigger signal. From the TSW14J56 EVM0 “Trigger Out B” port at J9, the trigger signal output from the master is routed to the trigger signal input of the slave for TSW14J56 EVM1. All cables have been delay matched.

5.3.2 Sample Alignment Mechanism

With the triggering mechanism of the TSW14J56 EVM, the data samples can be loaded onto the memory of the EVM and released upon the triggering signal at the same time. This mechanism ensures that the data samples are aligned to the trigger signal edge. Figure 12 shows the sequence of the triggering mechanism.

Upon receiving an asynchronous command to start the trigger mechanism (controlled through HSDC PRO GUI), the TSW14J56 EVM0 master board provides the triggering signal to both itself and to the slave board. The trigger signal outputs are duplicated on both “Trigger Output A” and “Trigger Output B” ports. These output signals are delay matched at the FPGA.

Both the master board and slave board capture the equivalent input trigger signal because the trigger output signal travels through the delay matched cables. The data stream for both master and slave boards are released upon the first LMFC edge that captures the input trigger signal. As a result, the sample streams of both master board and slave board are aligned in time.

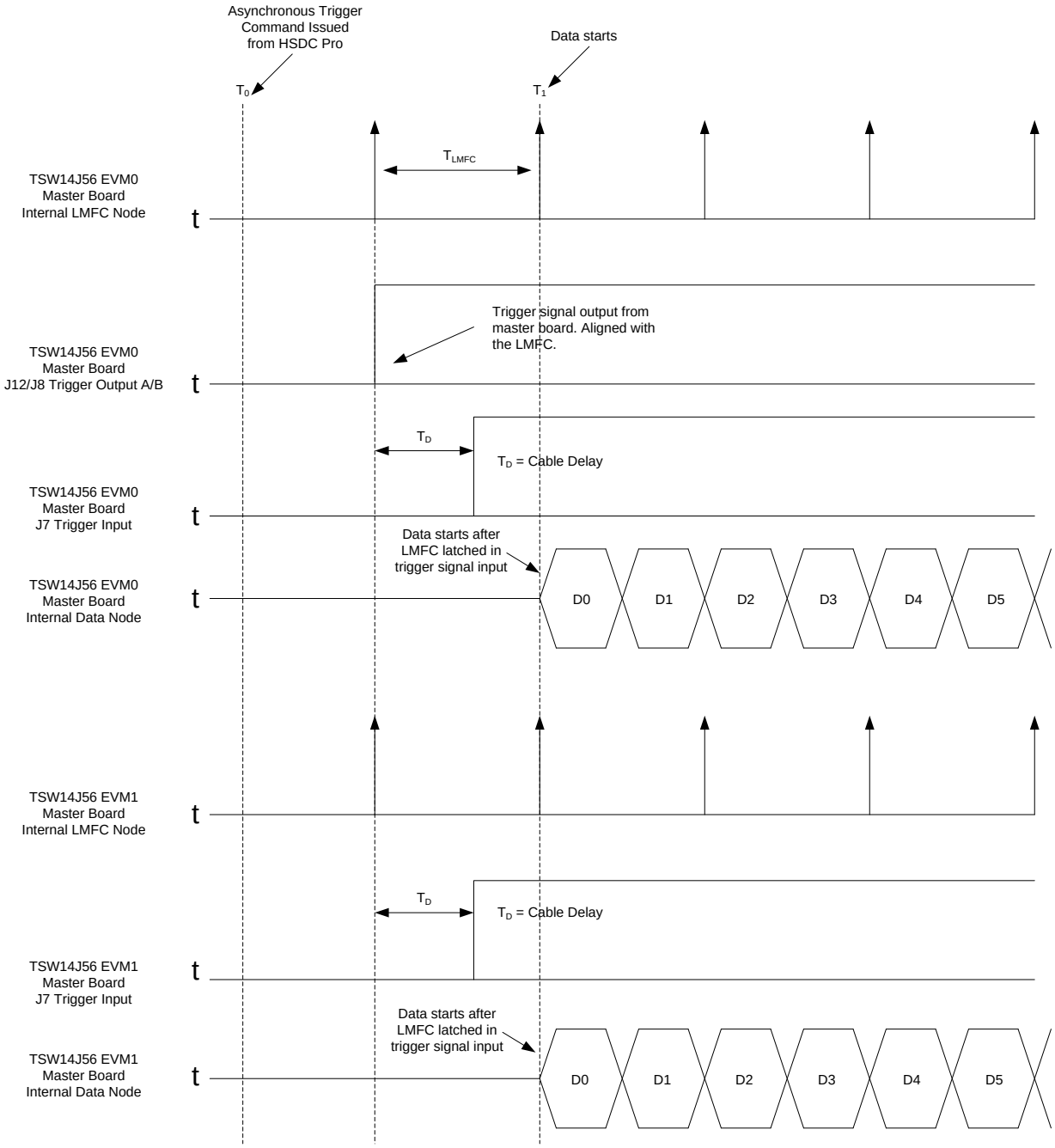


Figure 12. TSW14J56 EVM Sample Alignment in Trigger Mode

6 Getting Started Software

6.1 Required Software

- DAC3xJ8x EVM GUI:
  This software allows the user to configure the DAC3xJ8x EVM and is available for download from TI.com together with the user's guide http://www.ti.com/tool/dac38j84evm.
- High Speed Data Converter Pro Software (HSDC-PRO):
  Installing the HSDC-PRO software is important and required to obtain the relevant FTDI USB drivers required by the main user interface for controlling the TSW14J56 device and the triggering or arming settings http://www.ti.com/tool/dataconverterpro-sw.

6.2 DAC3xJ8x EVM GUI

This subsection provides guidelines to program the DAC3xJ8x EVM GUI step-by-step. The user may adjust the setting to match their system requirements.

1. Program the DAC3xJ8x and LMK04828 devices from the main menu (see Figure 13). This step ensures that the user programs the DAC3xJ8x in the correct JESD204B setting and the LMK04828 in a known PLL2 locking condition.

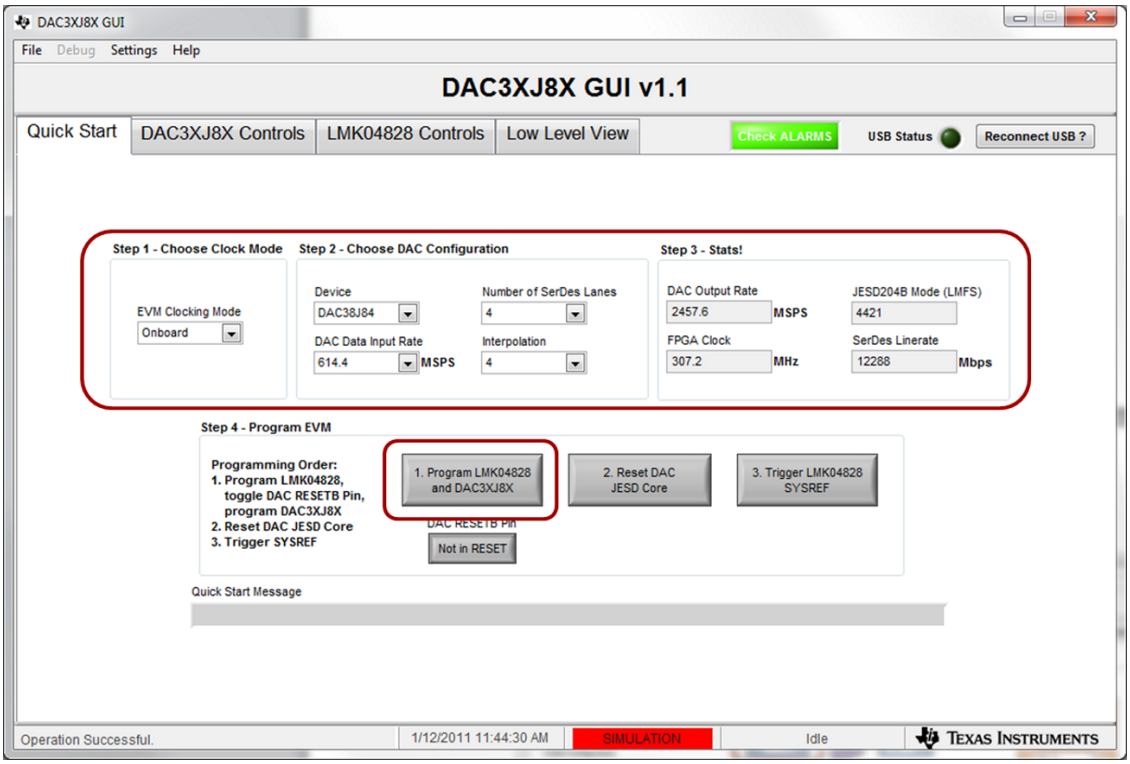


Figure 13. DAC3xJ8x GUI—Quick Start Menu

2. Set the clock divider initializer to look for all SYSREF pulses in a continuous SYSREF environment (see Figure 14).

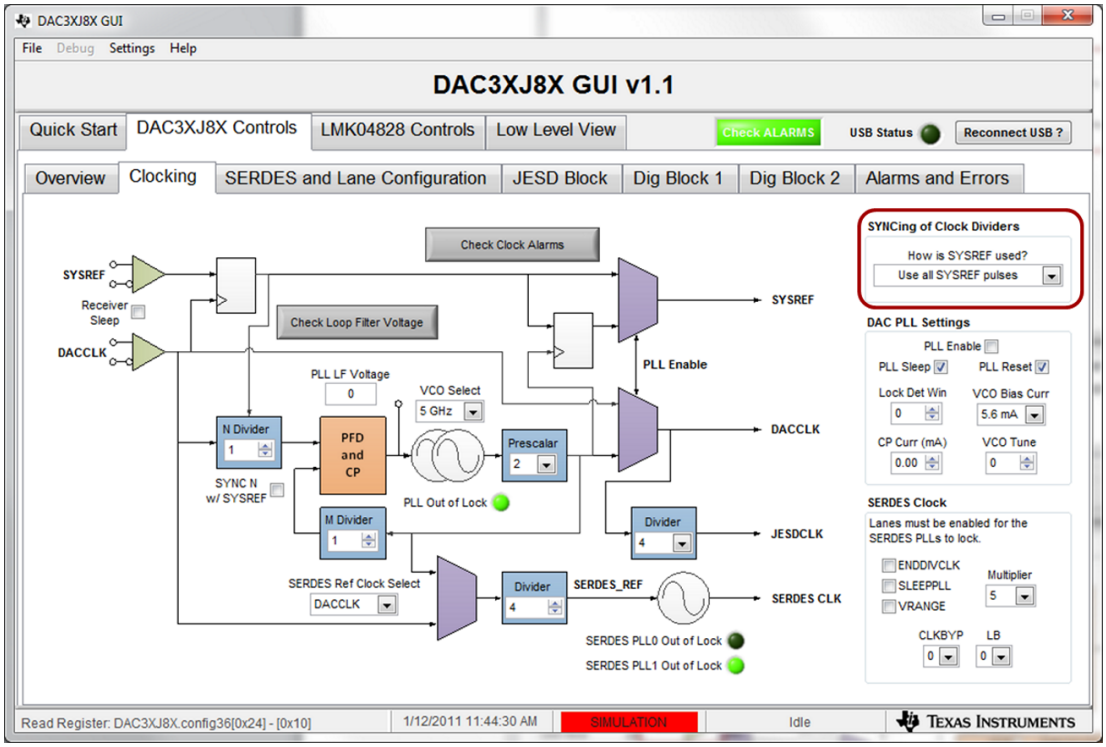


Figure 14. DAC3xJ8x GUI—Setting Clock Divider

3. Set the JESD204B link 0 initializer to look for all SYSREF pulses in a continuous SYSREF environment (see Figure 15).

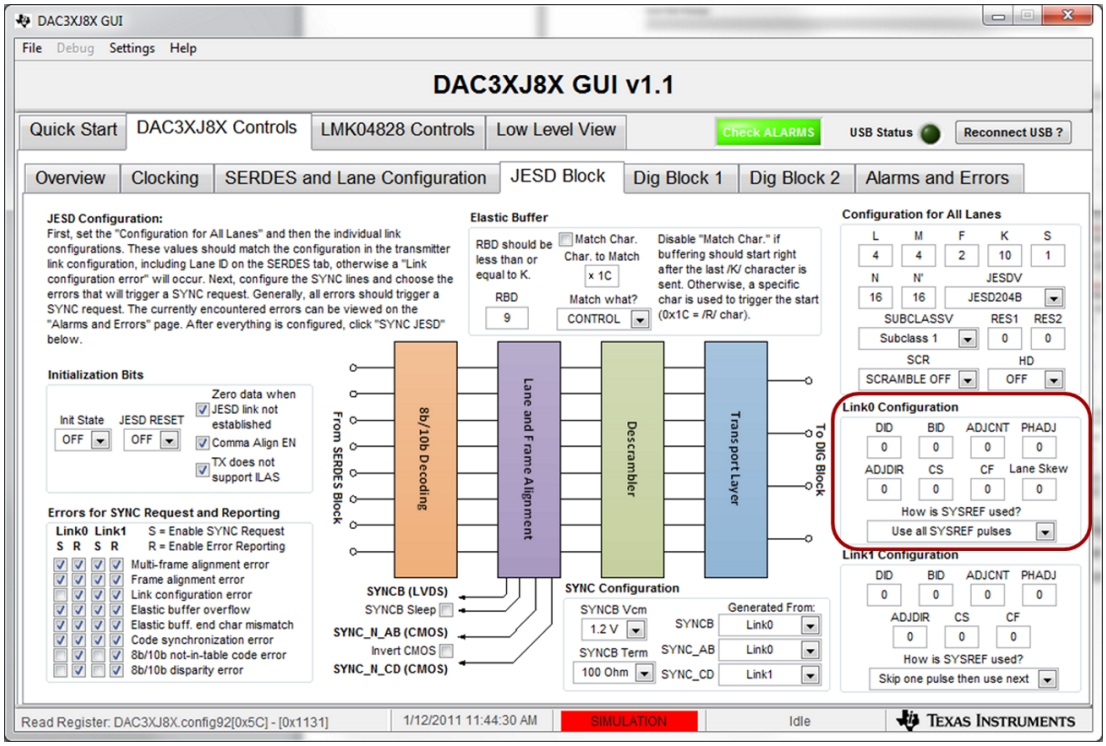


Figure 15. DAC3xJ8x GUI—Setting Link0 SYSREF Option

4. Configure the PLL1 stage of the LMK04828 in nested 0-delay dual loop mode (see Figure 16).

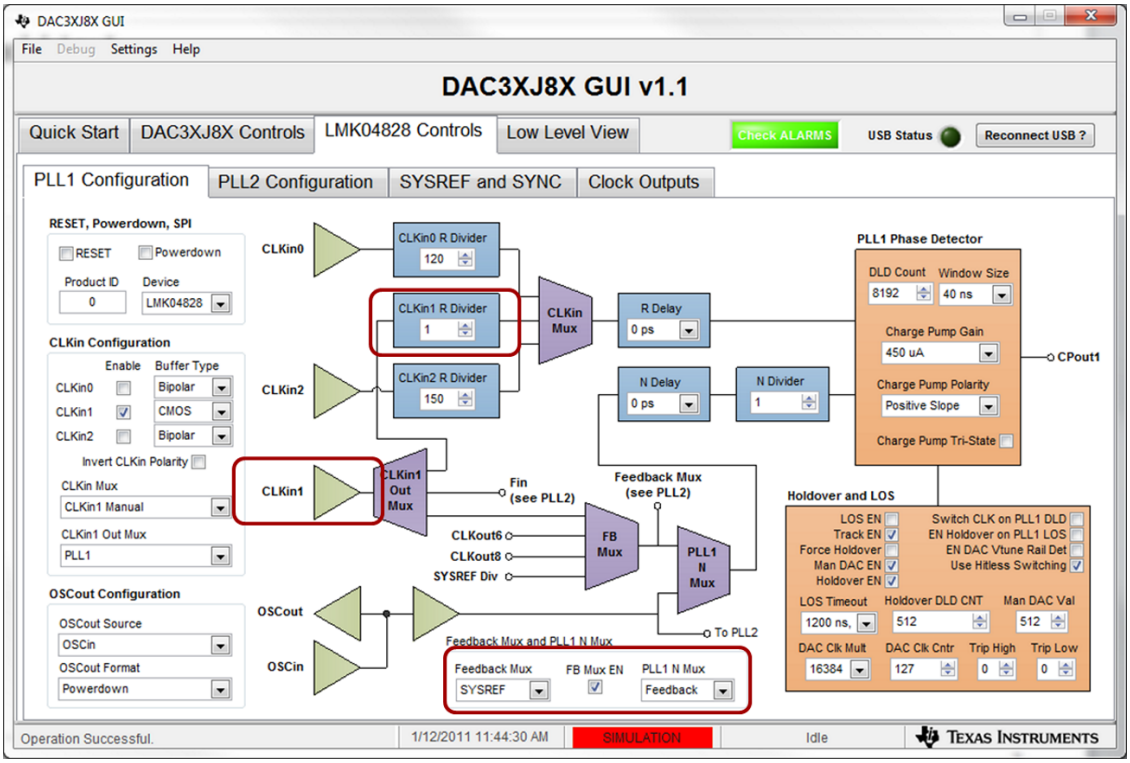


Figure 16. PLL1 Settings

5. Configure the PLL2 stage of the LMK04828 in nested 0-delay dual loop mode (see Figure 17).

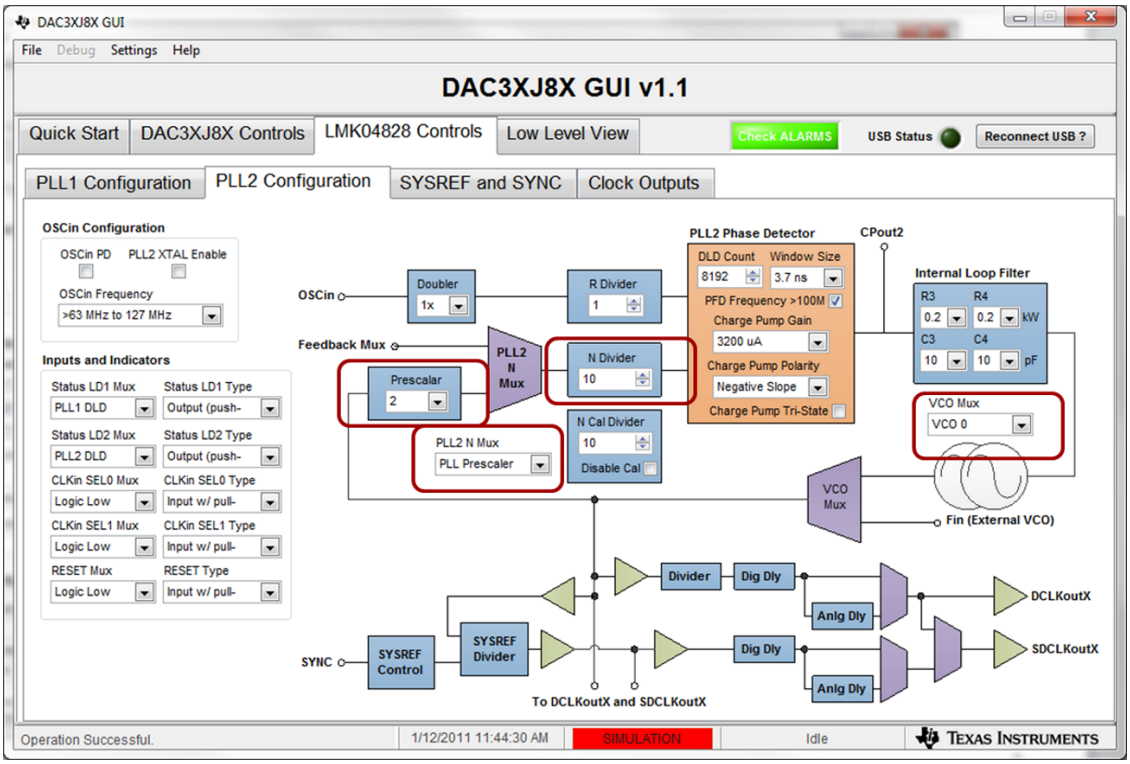


Figure 17. PLL2 Settings

6. Configure the SYSREF divider of the LMK04828 in nested 0-delay dual loop mode (see Figure 18).

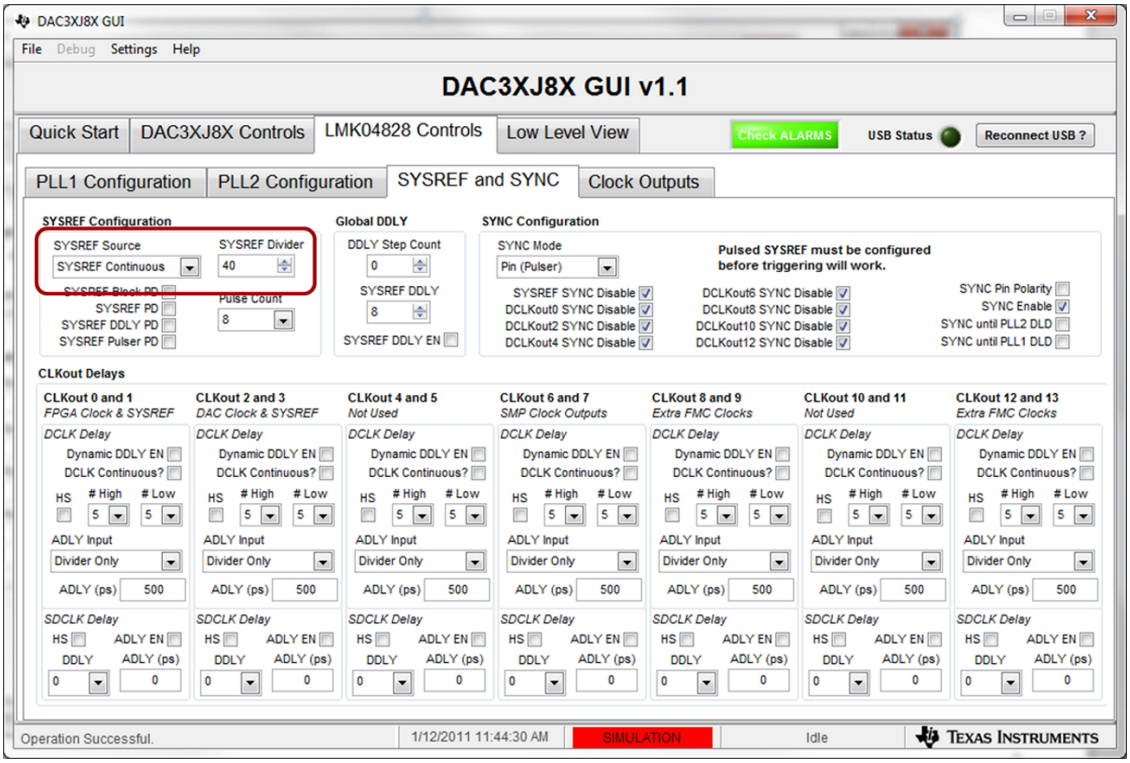


Figure 18. SYSREF Setting

7. Observe a general overview of the LMK04828 clock outputs (see Figure 19).

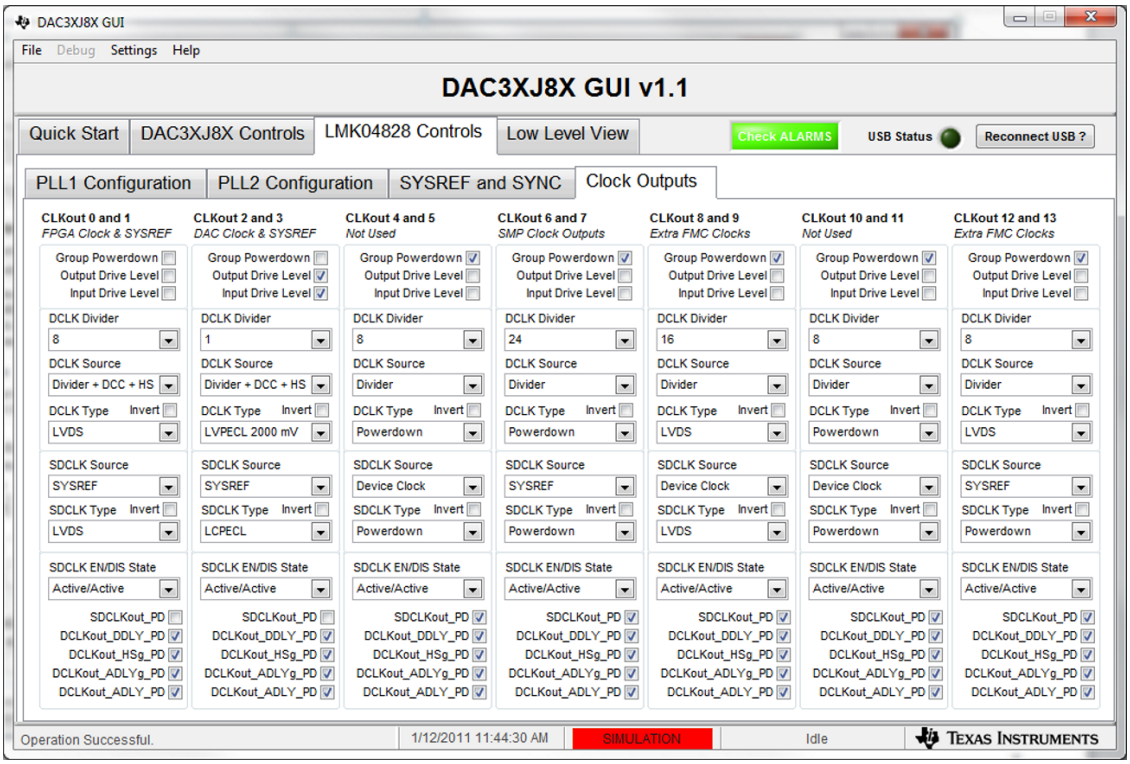


Figure 19. DCLK and SDCLK Setting

6.3 HSDC-PRO Software

The HSDC-PRO software suite includes support for the TSW14J56EVM to DAC3xJ8xEVM data transfer through a JESD204B link. The software can load existing data waveforms to play back on the DAC3xJ8x output. For further details, refer to the TSW14J56EVM user's guide (SLWU086) and the HSDC-PRO software user's guide (DATACONVERTERPRO-SW).

7 Test Setup

1. Connect J16 of DAC3xJ8x EVM0 to J4 of TSW14J56 EVM0. Then connect J16 of DAC3xJ8x EVM1 to J4 of TSW14J56 EVM1. The connection is based on a VITA 57 specified FMC connector. J16 of the DAC3xJ8x EVM is the male FMC connector while J4 of the TSW14J56 is the female FMC connector.
2. Apply 5 V of power to the J11 connector of both TSW14J56 EVM0 and EVM1. Connect the USB 3.0 cable from the PC to J9 connector of both TSW14J56 EVM0 and EVM1. Do not power up the TSW14J56 EVMs at this point.
3. Apply 5 V of power to the J23 connector of both DAC3xJ8x EVM0 and EVM1. Connect a USB 2.0 type B cable from the PC to only J14 of DAC3xJ8x EVM0 during this step. Do not connect the PC to the DAC3xJ8x EVM1 at this time.
4. Enable both the TSW14J56 EVM0 and EVM1 at this time by sliding SW6 to the ON position.
5. Connect the 61.44-MHz reference to a power splitter to split into two SMA connections. Make sure the 61.44-MHz reference is disabled for now. Connect one source to the J17 SMA connector of the DAC3xJ8x EVM0 and connect another source to the J17 SMA connector DAC3xJ8x EVM1. Be sure to use matched-length SMA cables and calibrate the delay of the two split 61.44-MHz signals to ensure a matched SYSREF output at the LMK04828 outputs. Enable the 61.44-MHz reference signal after the connection.
6. Start the DAC3xJ8x EVM GUI. Click on the Reconnect USB ? button to establish a USB-to-PC link of the DAC3xJ8x EVM0. The USB status LED on the GUI lights up green at this point.
7. Navigate to the *Low Level View* page of the DAC3xJ8x EVM GUI (Figure 20), click on the Load Config button and select the file *DAC38J84_4xint_Fdata614p4MHz_0_delay442.cfg*. This *.cfg* file is available for download in the TIDA-00996 design files. Section 6.2 describes the DAC38J84 EVM configuration in further detail. After the DAC3xJ8x EVM GUI finishes loading, the DAC3xJ8x EVM configuration has completed.

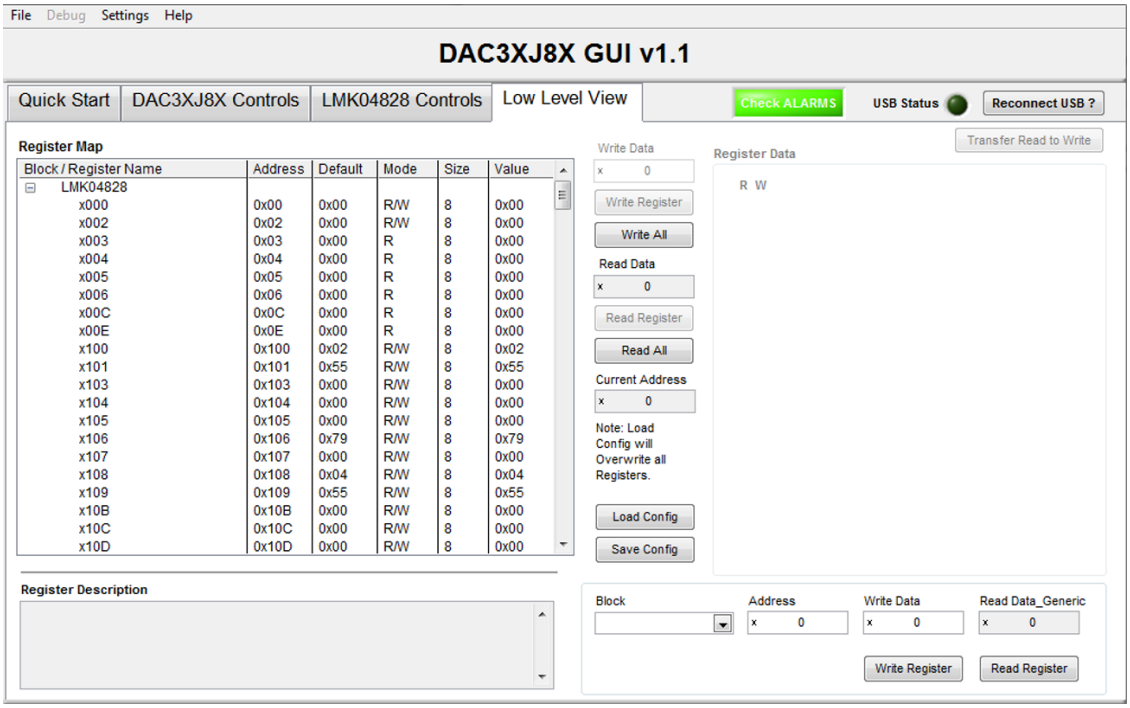


Figure 20. DAC3xJ8x EVM GUI—Low Level View

8. Disconnect the USB type B cable from DAC3xJ8x EVM0 and connect it to DAC3xJ8x EVM1. Repeat the loading procedure for the DAC3xJ8x EVM GUI described in the previous steps.
9. Start the HSDC PRO GUI software. Connect to the TSW14J56 EVM1 slave board first when the *Select Board* prompt appears (Figure 21). Note the serial number label on the TSW14J56 EVM1 and select the associated serial number of the board on the *Select Board* prompt.

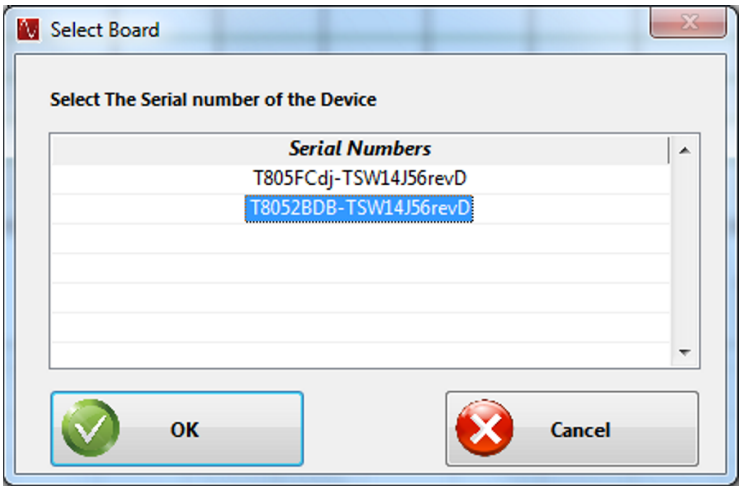
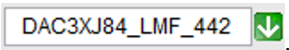
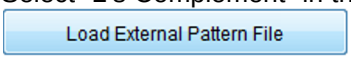


Figure 21. Select TSW14J56 EVM1 Slave Board

10. Select the DAC3xJ8x_LMF_442 mode from the drop-down menu 

. Type in "614.4M" in the field for *Data Rate (SPS)*. Select "2's Complement" in the drop-down menu of the *DAC Option* field (Figure 22). Click on the 

button and select the *rise.csv* file for a 64-samples-wide pulse pattern for the pattern file.

Figure 22. HSDC PRO GUI DAC Settings and Pattern File Loading

11. In the *File Menu*, navigate to *Data Capture Option* and then select *Trigger Option*. Inside the *Trigger Option* menu box, check the *Trigger mode enable* box (Figure 23). This action programs the TSW14J56 EVM1 into slave mode to accept an external trigger signal.

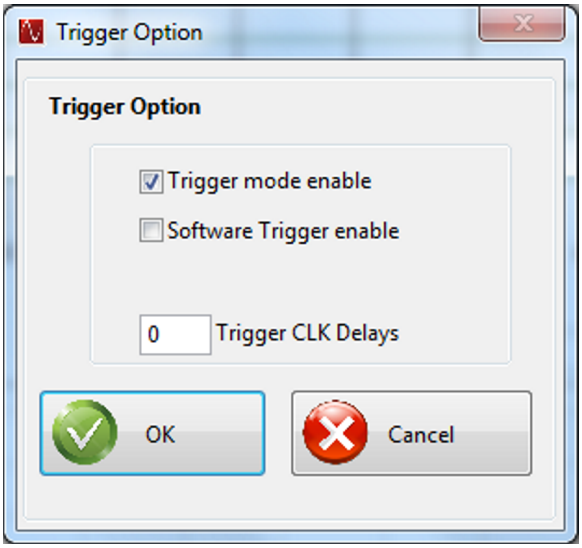
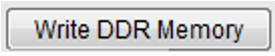


Figure 23. Enabling Slave Mode for TSW14J56 EVM1

12. Click the 

button on the HSDC PRO GUI main menu. This action arms the TSW14J56 EVM1 into slave mode and loads the pulse waveform into the memory. Any trigger signal to the J13 “Trigger In” port starts the waveform playback.
13. In the *File Menu*, navigate to *Instrument Options* and click on *Disconnect from the Board*. Then navigate to *Instrument Options* again and click on *Connect to the Board*. Connect to the TSW14J56 EVM0 master board during the *Select Board* prompt (Figure 24). Note the serial number label on the TSW14J56 EVM0 and select the associated serial number of the board on the *Select Board* prompt.

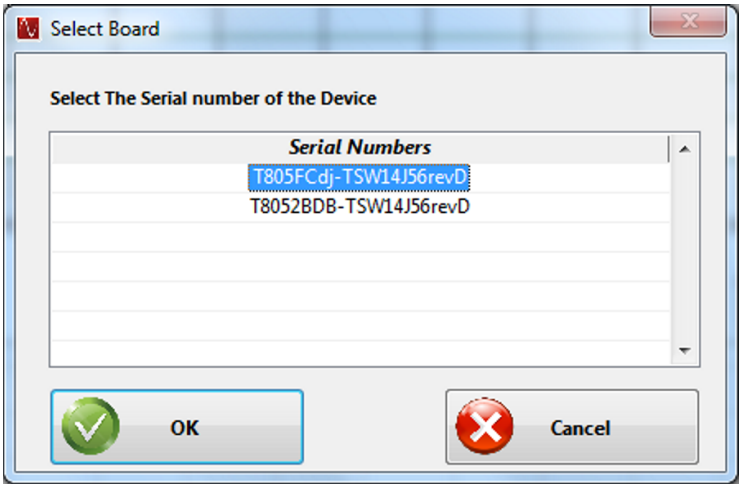


Figure 24. Select TSW14J56 EVM0 Master Board

14. Enter the DAC settings per the previous *Step 10* and load the pulse pattern.

15. In the *File Menu*, navigate to *Data Capture Options* and click *Trigger Option*. Inside the *Trigger Option* menu, check the boxes for both *Trigger mode enable* and *Software Trigger enable* (Figure 25). This action arms the TSW14J56 triggering input port and enables self-triggering mode.

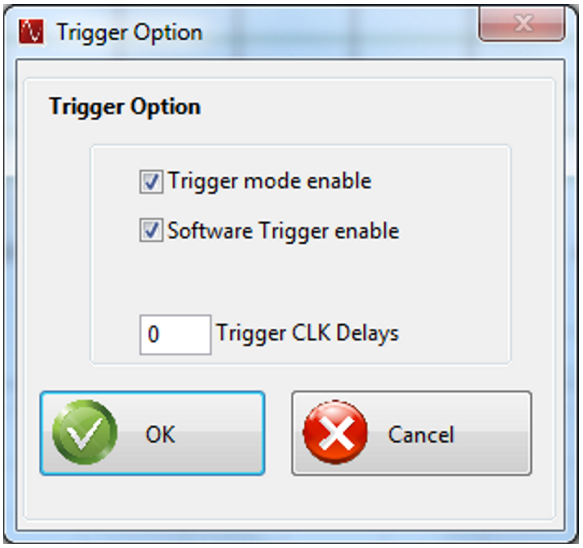


Figure 25. Enable Master Mode and Self-Triggering for TSW14J56 EVM0

16. Click the Generate Trigger button on the HSDC PRO main menu. This action programs the TSW14J56 EVM0 into master mode, loads the pulse waveform into the memory, and generates the triggering signal to itself and the TSW14J56 EVM1.
17. Both the DAC3xJ8x EVM0 and EVM1 must have a rising edge output at any of the ports. Measure the waveforms on the scope and the DAC outputs to ensure that these have been aligned. Be sure to calibrate out any probe delays.

8 Test Data

The setup provides good delay and phase matching of the DAC38J84 outputs on two separate transmitter EVM platforms. Additional baseband processing of the signal on either the FPGA or DAC3xJ8x signal processing side can be applied to match the system requirement. The setting for the LMK04828 nested 0-delay dual loop allows a phase-matched SYSREF, which has been applied globally to the system, to facilitate synchronization. If additional radio frequency (RF) modulation is required for over-the-air distribution, refer to the TSW38J8x EVM platforms. The setup is similar and includes a pair of analog quadrature modulators for baseband-to-RF modulation.

8.1 SYSREF Alignment Result on DAC3xJ8x EVMs

The configuration of the LMK04828 in nested 0-delay dual loop mode yields identical pairs of a SYSREF signal on both DAC3xJ8x EVMs. Figure 26 shows the test result measured on the oscilloscope for the SYSREF signal on DAC3xJ8x device 0 and the SYSREF signal on DAC3xJ8x device 1. Both SYSREF signals have the same delay. The blue signal is the SYSREF0 for DAC device 0 and the light green signal is the SYSREF1 for DAC device 1.

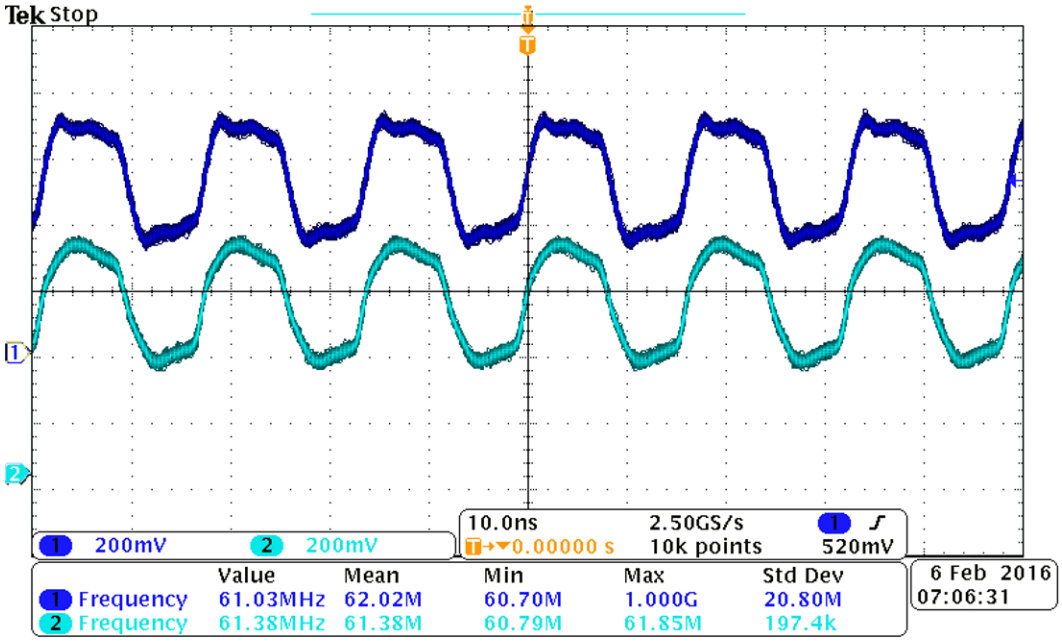


Figure 26. SYSREF Signal Probed at Two Different DAC3xJ8x EVM With LMK04828 in Nested 0-Delay Dual Loop Mode

8.2 DAC Output Alignments on Multiple DAC3xJ8x EVMs

The configurations of the TSW14J56 master and slave mode triggering for the data alignment and the JESD204B subclass 1 DAC3xJ8x device synchronization are responsible for yielding DAC outputs with the same output delay. Figure 27 shows the test result. The blue signal is channel A of DAC device 0 and the light green signal is channel B of DAC device 0. The pink signal is channel A of DAC device 1 and the green signal is channel B of DAC device 1.

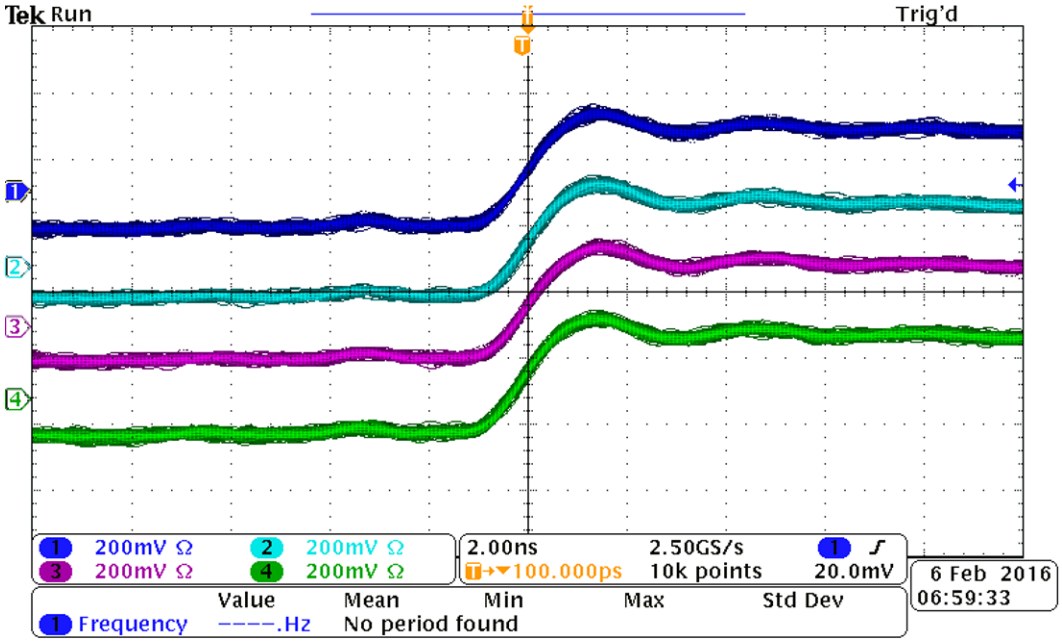


Figure 27. DAC3xJ8x Channel A and Channel B Outputs at Two Different DAC3xJ8x EVMs

9 Design Files

9.1 Schematics

To download the schematics, see the design files in the tool folder of the DAC38J84 Evaluation Module http://www.ti.com/tool/dac38j84evm.

9.2 Bill of Materials

To download the bill of materials (BOM), see the design files in the tool folder of the DAC38J84 Evaluation Module http://www.ti.com/tool/dac38j84evm.

9.3 Layer Plots

To download the layer plots, see the design files in the tool folder of the DAC38J84 Evaluation Module http://www.ti.com/tool/dac38j84evm.

9.4 Layout Guidelines

To view the layout guidelines, see the design files in the tool folder of the DAC38J84 Evaluation Module http://www.ti.com/tool/dac38j84evm.

10 Software Files

Download the software files for the DAC3xJ8x EVM at www.ti.com/lit/zip/slac644.

Download the software files for the High Speed Data Converter (HSDC) Pro Software at www.ti.com/tool/dataconverterpro-sw .

11 References

1. Texas Instruments, *JESD204B multi-device synchronization: Breaking down the requirements*, 2Q 2015 Analog Applications Journal (SLYT628)
2. Texas Instruments, *DAC3xJ8x SYSREF Configuration*, DAC3xJ8x Application Report (SLAA696)

12 Terminology

DAC3xJ8x— Family of JESD204B subclass 1 DAC products from TI

Frame (F) —Number of octets in a frame in JESD204B specification

JESD204B RX (JESD204B transmitter)—In a JESD204B system of FPGA/ASIC and the DAC3xJ8x device, this is referred to as the FPGA/ASIC

JESD204B TX (JESD204B receiver)—In a JESD204B system of FPGA/ASIC and the DAC3xJ8x device, this is referred to as the DAC3xJ8x

LMFC— Local multi-frame clock; this is a JESD204B sub-clock indicating the boundary of multi-frame

Multi-frame (K)—Number of frames in the multi-frame in JESD204B specification

P2S— Parallel-to-serial conversion; this refers to the data packing on the JESD204B TX

S2P— Serial-to-parallel conversion; this refers to the data packing on the JESD204B RX

SYSREF— System reference clock; this refers to the reference required in JESD204B subclass 1 system where the reference clock is used to align the LMFC

13 About the Author

KANG HSIA is an Applications Engineer in the High Speed Data Converters group at Texas Instruments (TI). He primarily provides customer support for TI's high-speed ADCs and DACs. Prior to joining TI in 2007, Kang earned his BSEE from California Polytechnic State University (Cal Poly) in San Luis Obispo, California and obtained his MSEE from the University of Texas at Dallas in 2015. Kang is an active member of the TI E2E™ Community and can be reached through e2e.ti.com for support.

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