TI Designs

Two-Port 40- and 100-GbE QSFP28 Signal Conditioner Reference Design

Design Overview

This verified reference design is a signal-conditioning solution for the front-port QSFP28, which supports two 100-Gigabit Ethernet (GbE) ports compatible with 100G-CR4/SR4/LR4, 40G-CR4/SR4/LR4, and 10G SFF-8431 requirements. The design is applicable to optical and passive or active copper cables. The design also allows for reach extension between the switch ASIC and the front-port QSFP28, which is often required for the outermost ports of a top-of-rack (ToR) switch or for add-in mezzanine implementations of QSFP28 line cards. This reference design offers the flexibility for users to upgrade from a DS280BR810 repeater to the pin-compatible DS250DF810 retimer.

Design Resources

TIDA-00427	Tool Folder Containing Design Files
DS280BR810	Product Folder
MSP430F5529	Overview Page
TPD4E004	Product Folder
TPS735	Product Folder
TPS75725	Product Folder

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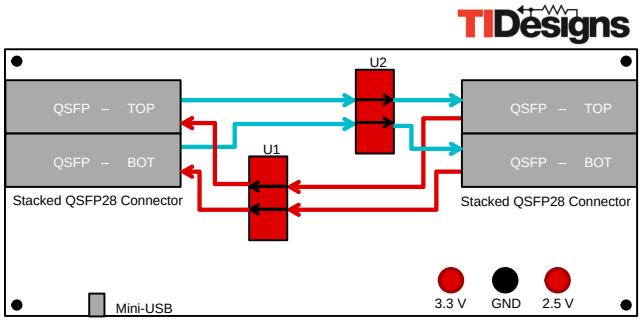
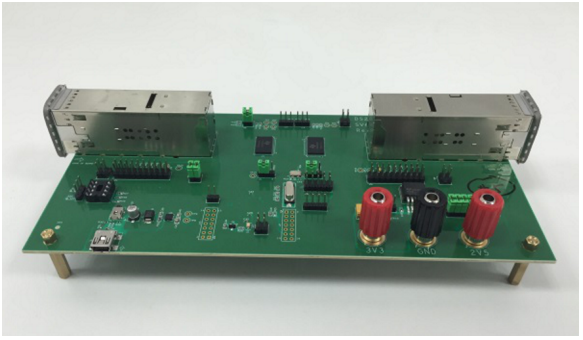
Design Features

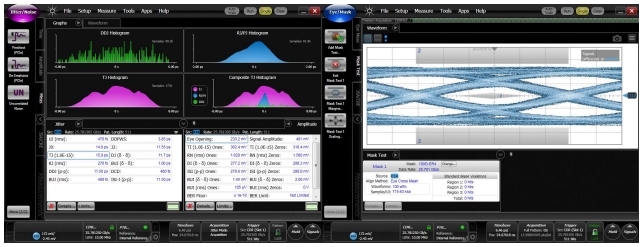
- Front-Port Stacked QSFP28 Implementation With Signal Conditioning to Support 10-, 40-, and 100-GbE Optical and Passive Copper
- Extends Reach Between Switch and Front-Port up to Three Times Beyond CAUI-4 Host Channel Loss Limit
- Low-Power and Low-Cost Solution for Front-Port Signal Conditioning
- Applicable to Top-of-Rack (ToR) Switch and Line Card Systems
- Single Power Supply—Does Not Require Firmware, Heatsink, or Reference Clock
- Lab-Tested HW Example Including 10-, 40-, and 100-GbE Specific Test Data

Featured Applications

- Ethernet Switch
- Optical Networking
- Server NIC Card







1 Introduction

This TIDA-00427 design guide summarizes the results of 100G CAUI-4 testing using the DS280BR810 low-power, 28-Gpbs, 8-channel linear repeater from Texas Instruments (TI). This guide also provides test results against the specifications of 40-GbE nPPI and SFF8431. The DS280BR810 has been tested in an egress signal-conditioning configuration against the jitter and eye mask requirement for CAUI-4 using a 2×1 stacked QSFP28 connector and host compliance board (HCB). These tests demonstrate the excellent signal conditioning capabilities of the DS280BR810 linear repeater and show that the DS280BR810 can extend the reach between the host application-specific integrated circuit (ASIC) and front-port cage by more than three times beyond the CAUI-4 host PCB channel limits.

The DS280BR810 is available in a small 8- × 13-mm leadless BGA package, which fits easily behind a standard 2x1 stacked QSFP28 connector, such as the TE Connectivity QSFP28 connector (2198373-1) used in these tests.

2 Block Diagram

Figure 1 shows the typical front-port applications of the DS280BR810 device.

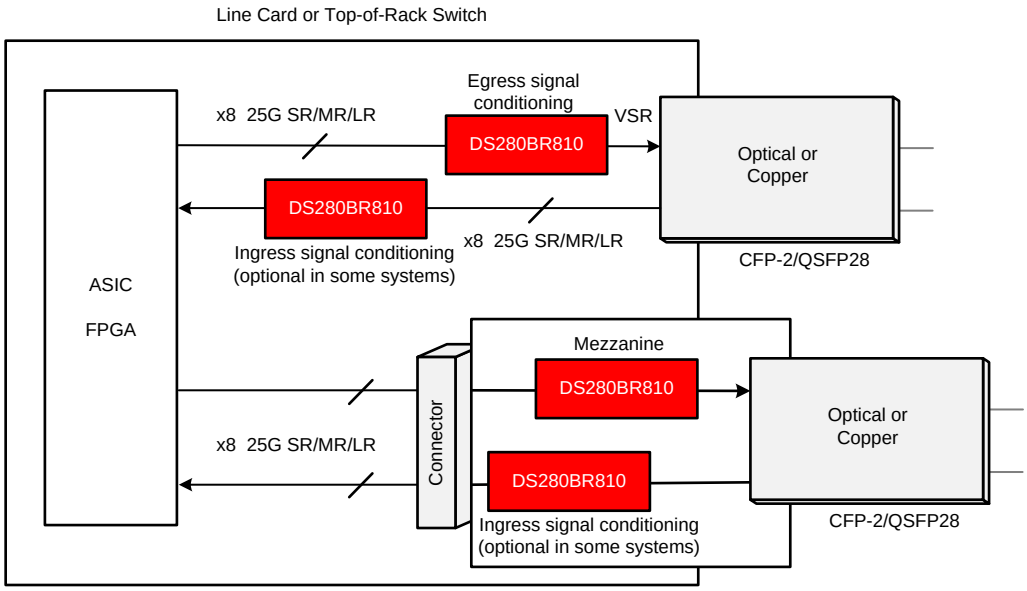


Figure 1. Typical Front-Port Applications of DS280BR810

3 System Description

Using the DS280BR810 linear repeater for 100-GbE front-port applications provides several advantages over a traditional PHY. Table 1 lists the key advantages for a generic 36-port switch card application.

Table 1. System-Level Benefits Breakdown for Generic 36-Port 100-GbE Switch Card

CRITERIA	TI DS280BR810 IMPLEMENTATION	TRADITIONAL CR4 PHY IMPLEMENTATION	BENEFIT OF TI
No. of devices	18 (Egress signal conditioning only) 36 (Egress + ingress signal conditioning)	18 (Egress + ingress signal conditioning)	Flexible
Total device PCB area consumed	18 × 104 mm2 = 1872 mm2 (Egress only) 36 × 104 mm2 = 3744 mm2 (Egress + ingress)	Approx. 18 × 361 mm2 =6498 mm2	Less than half the PCB area
No of power rails	One only (2.5 V)	Three or more	Simpler power supply design
Input-to-output latency	< 100 ps	Up to several hundred ns	Smaller latency
Reference clock required	No reference clock required	Low-jitter reference clock fan-out to all PHYs	No reference clock
PCB design flexibility	Uni-directional configuration allows for flexibility in device placement → more optimized for compact PCB design	Limited flexibility; lane swapping is complicated and limited	More flexibility in routing
User experience	Simple-to-use one-time configuration over I^2C or EEPROM; all devices can share one EEPROM.	Firmware load required	Faster initialization
Implementation cost	Minimal external passive components (that is, decoupling capacitors), no requirement for supply filtering or reference clock distribution	Numerous passive components typically used (power supply filters, low-jitter reference clock fan-out, and so forth)	Lower overall BOM cost

4 System Design Theory

4.1 100-GbE CAUI-4 Egress Testing

100-GbE CAUI-4 is a parallel physical interface that allows for the construction of compact optical transceiver modules for 100GBASE-SR4/LR4 with clock and data recovery circuits inside. As a result, the IEEE 802.3bm standard, which governs the CAUI-4 interface, has defined the electrical requirements at the host board output to ensure the proper functioning of the attached optical modules. This user's guide also shows test results for the specifications of 40-GbE nPPI and SFF8431.

The experiments in this report demonstrate the ability of the DS280R810 to provide excellent signal conditioning for the purposes of meeting CAUI-4 transmit electrical specifications.

4.1.1 CAUI-4 Specifications

CAUI-4 specifies jitter limits at a test point, which is equivalent to the output of the host compliance board (HCB). Figure 2 shows this test point, which is known as compliance point TP1a.

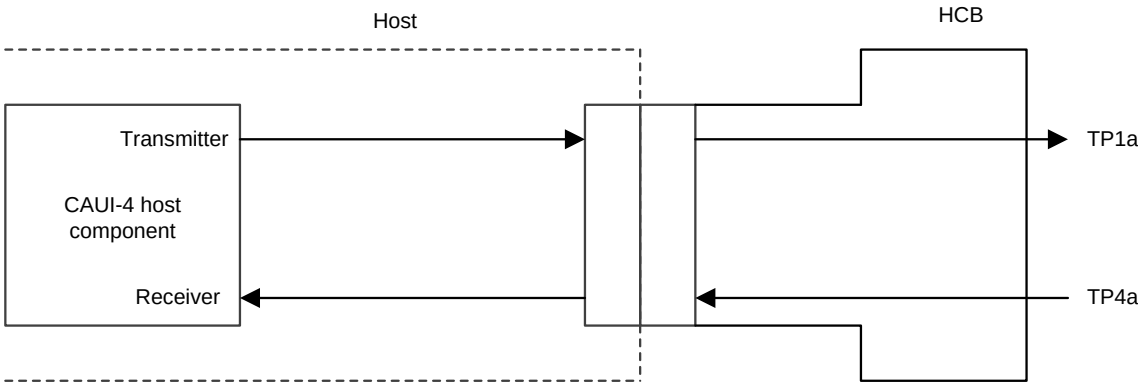


Figure 2. Host CAUI-4 Compliance Point

Table 2 lists the key specifications for CAUI-4 at the host output compliance point.

Table 2. CAUI Host Output Specifications

INTERFACE SPECIFICATION	EYE HEIGHT (MIN)	PEAK-PEAK OUTPUT VOLTAGE (MAX)	EYE WIDTH (MIN)	COMMENT
CAUI-4	95 mV	900 mV	0.46 UI1 (1)	IEEE 802.3bm, Table 83E-1

(1) Based on the 802.3bm 83E.4.2 specification, which is defined at 1E-15 BER

4.1.2 Setup—Hardware

The hardware setup for these tests consists of:

- Centellax BERT (SSB-16000J and PG32)
- Evaluation kit (EVK) of 25-Gbps Retimer DS250DF810 from TI
- Variable ISI channel, CLE1000
- Molex zQSFP+TM Host Compliance Boards (HCB)
- Agilent DCAx sampling scope with 86108B precision time base (PTB) module
- SMA cables, 1x8 MXP Huber-Suhner cables

Figure 3 shows the test setup. In this scenario, the Centellax transmitter PG32 transmits a PRBS9 data pattern at 25.78125 Gbps, which is required by CAUI-4 for transmitter testing. The output of the PG32 connects with the input of the DS250DF810 device on the DS250DF810EVK through a 1x8 MXP Huber-Suhner cable. The DS250DF810 device locks to the data and retransmits the signal to its output. This data passes through a variable ISI channel CLE1000 into the HCB and then into the input of the QSFP28 board (red). The DS280BR810 linear repeater on the QSFP28 board equalizes and redrives the signal towards the QSFP28 connector. The Agilent DCAx scope measures the equalized eye at the output of the HCB and checks the eye height and eye width against the CAUI-4 specifications.

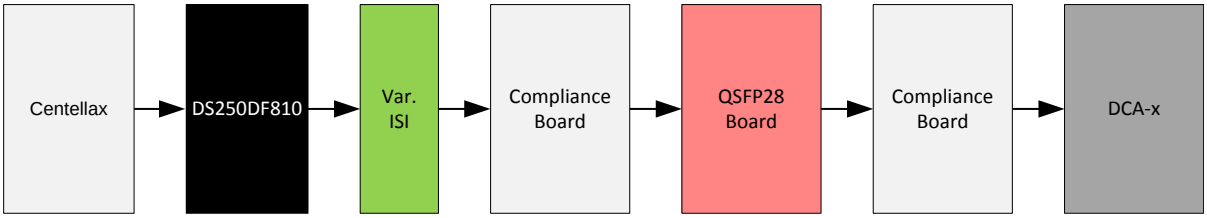


Figure 3. CAUI-4 Test Setup Diagram

The intention of this test fixture is to mimic a line card or rack-mounted switch card design, similar to what Figure 4 shows.

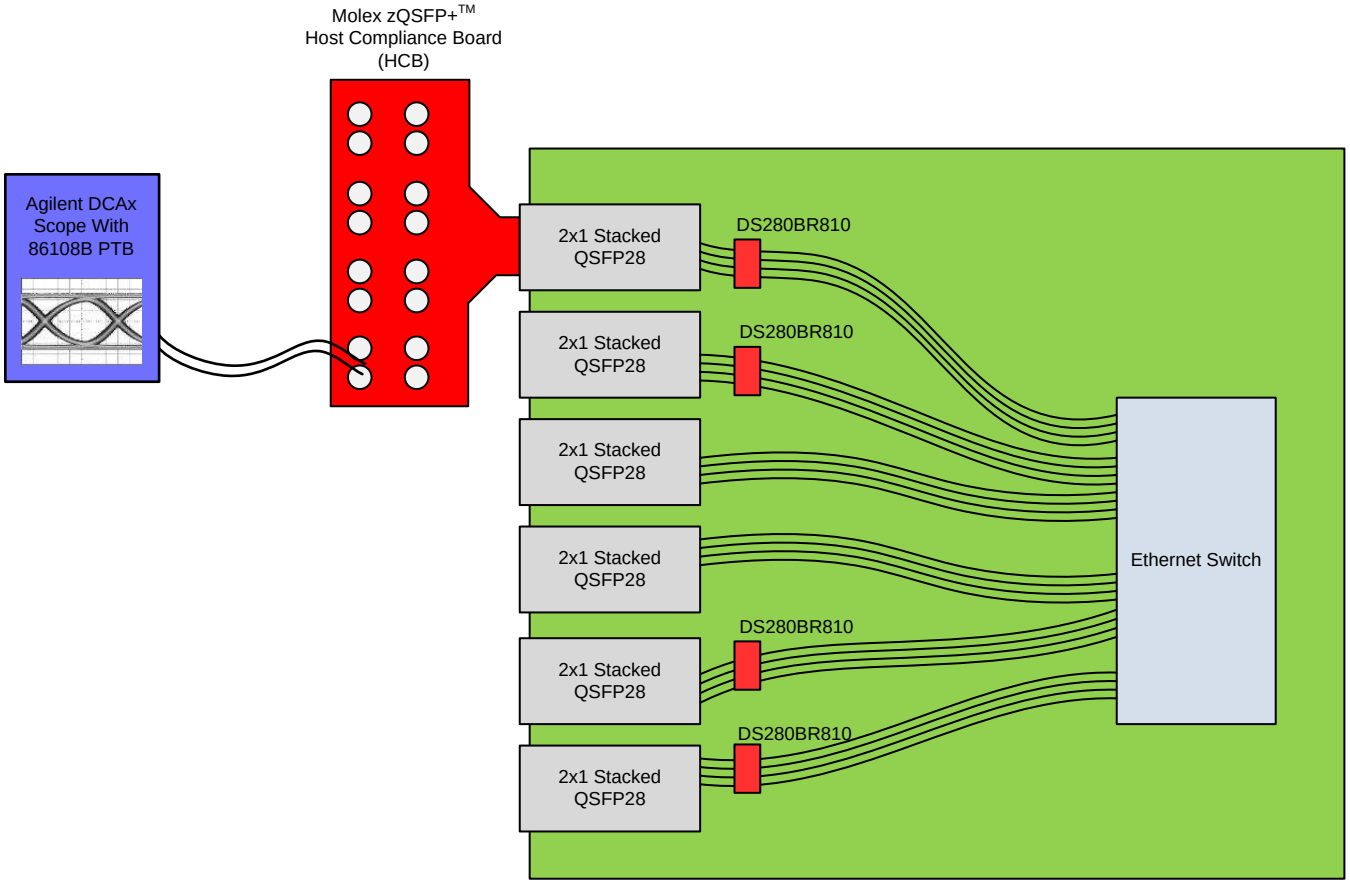


Figure 4. Front-Port Design Diagram Using DS280BR810 Linear Repeaters

Figure 5 shows the DS280BR810 QSFP28 reference design board. The test board has two 100G QSFP28 ports arranged in a stacked 2x1 configuration on each side.

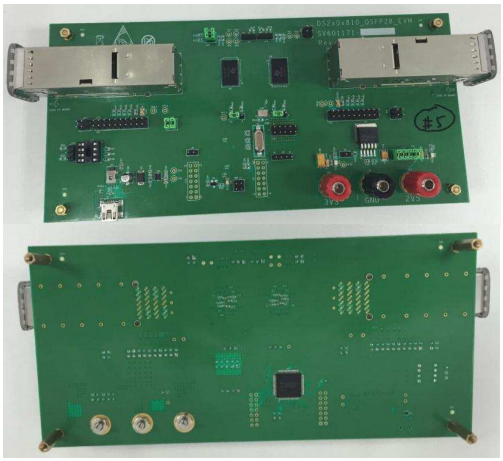


Figure 5. DS280BR810 QSFP28 Reference Design Board (Top and Bottom)

On the top side of the board, one HOST silk mark is labeled on the left side and one CABLE silk mark is labeled on the right side. These labels simplify the description of one specific QSFP 28 connector. Reference the top image in the preceding Figure 5.

On the schematic or PCB design of this board, the top QSFP port on the HOST side connects with the top QSFP port on the CABLE side. The bottom QSFP port on the HOST side connects with the bottom QSFP port on the CABLE side. Refer to the *TIDA-00427 DS280BR810 100G QSFP28 Test Setup* for the setup of this reference design board (TIDUBF8).

4.1.3 Results

The host transmitter output of eye height, peak-peak of the signal, and eye width have been measured for various combinations of losses. Table 3 summarizes the results.

Table 3. Host Transmit Output Eye Height and Eye Width Results for CAUI-4

					DS250DF810 TRANSMITTER[1]			DS280BR810 SETTING[2]				100-GbE CAUI-4		
												DIFFERENTIAL INNER EYE HEIGHT AT 1E-15 PROBABILITY (mV pk-pk)	DIFFERENTIAL OUTER EYE HEIGHT AT 1E-15 PROBABILITY (mV pk-pk)	EYE WIDTH AT 1E-15 PROBABILITY (UI pk-pk)
ISI SETTING	INPUT LOSS	OUTPUT LOSS	TOTAL LOSS	PORT	PRE	MAIN	PST	BW	BST1	BST2	VOD	≥ 95	≤ 900	≥ 0.46
None	10.1	6.4	16.5	BOT	–3	17	0	3	3	0	2	233	837	0.59
				TOP	–3	17	0	3	3	0	2	232	819	0.60
2	13.5	6.4	19.9	BOT	–3	13	0	3	3	0	2	147	711	0.53
				TOP	–3	13	0	3	3	0	2	153	682	0.53
7	15	6.4	21.4	BOT	–5	15	0	3	5	0	2	199	751	0.54
				TOP	–5	15	0	3	5	0	2	189	740	0.52
12	17.2	6.4	23.6	BOT	–3	17	0	3	5	0	2	149	818	0.54
				TOP	–3	17	0	3	5	0	2	137	805	0.52
18	19	6.4	25.4	BOT	–3	15	2	3	5	2	2	129	809	0.55
				TOP	–3	15	2	3	5	2	2	134	792	0.55
23	20.4	6.4	26.8	BOT	–4	16	0	3	5	2	2	120	749	0.53
				TOP	–4	16	0	3	5	2	2	119	740	0.55
29	22.4	6.4	28.8	BOT	–6	14	0	3	5	3	3	127	766	0.49
				TOP	–6	14	0	3	5	3	3	124	754	0.52

(1) The pre, main, and post cursor setting of DS250DF810 determines the output amplitude and dB of de-emphasis. Reference the datasheet of DS250DF810 for further details.

(2) DS280BR810 is configured as eq_high_gain=1 and linear mode when performing the CAUI-4 tests.

In Table 3, the ISI setting is *None* for situations where the variable ISI channel CLE1000 has been bypassed. Consequently, at the input of the DS280BR810 linear repeater, the following components mainly contribute to the channel loss:

- Trace on the DS250DF810EVK and 1x8 MXP Huber-Suhner cable, which totals 3.9 dB
- HCB board, 3.5 dB
- QSFP28 connector, 1 dB
- Trace on the QSFP28 board, 1.7 dB

At the output of the DS280BR810 linear repeater, the following components mainly contribute to the channel loss:

- Trace on the QSFP28 board, 1.2 dB
- QSFP28 connector, 1 dB
- HCB board, 3.5 dB
- SMA cable, 0.7 dB

As Table 3 shows, by adding the CLE1000 in the middle of the test channel and varying its setting from 2 to 29, the channel loss at the input of the DS280BR810 linear repeater varies from 13.1 dB up to 22.4 dB at 12.9 GHz. The loss at the output of the DS280BR810 linear repeater is always fixed as 6.4 dB at 12.9 GHz.

All test results have met the CAUI-4 specifications and have margins that can be observed in the last three columns of Table 3.

In some applications, the output of the DS280BR810 linear repeater must also support 40-GbE nPPI and 10-GbE SFF8431 specifications. The table in Figure 6 shows the results of the tests performed with the same channel configuration of the 25-Gbps CAUI-4 tests using the same ASIC (DS250DF810) transmitter setting. The settings of the DS280BR810 linear repeater are almost the same except that eq_high_gain has been set to 0 to avoid violating the ≤ 700-mV peak-peak specification of the nPPI and SFF8431. In the real application, the boost and VOD settings of the DS280BR810 device occasionally require fine tuning to meet all the specifications and achieve greater margins of the nPPI and SFF8431 specifications.

													40GbE nPPI					10GbE SFF-8431 (Table 12)					
													Differential Inner Eye Height @ 1E-15 Probability	Differential Outer Eye Height @ 1E-15 Probability	J9	J2	Data Dependant Pulse Width Shrinkage (DDPWS)	Differential Inner Eye Height @ 1E-15 Probability	Differential Outer Eye Height @ 1E-15 Probability	Total Jitter (TJ)	Data Dependant Jitter (DDJ)	Data Dependant Pulse Width Shrinkage (DDPWS)	Uncorrelated Jitter (UJ)
					DS250DF810 Transmitter			DS280BR810 Setting					mV pk-pk	mV pk-pk	UI pk-pk	UI pk-pk	UI pk-pk	mV pk-pk	mV pk-pk	UI pk-pk	UI pk-pk	UI pk-pk	UI RMS
ISI setting	Input loss	Output loss	Total loss	Port	PRE	MAIN	PST	BW	BST1	BST2	VOD		≥ 190	≤ 700	≤ 0.23	≤ 0.17	≤ 0.070	≥ 190	≤ 700	≤ 0.28	≤ 0.10	≤ 0.065	≤ 0.023
None	10.1	6.4	16.5	BOT	-3	17	0	3	3	0	2		459	669	0.12	0.07	0.045	459	669	0.14	0.07	0.045	0.006
				TOP	-3	17	0	3	3	0	2		447	647	0.12	0.07	0.054	447	647	0.14	0.07	0.054	0.005
2	13.5	6.4	19.9	BOT	-3	13	0	3	3	0	2		331	545	0.12	0.08	0.065	331	545	0.13	0.08	0.065	0.004
29	22.4	6.4	28.8	BOT	-6	14	0	3	5	3	3		308	634	0.13	0.09	0.063	308	634	0.15	0.08	0.063	0.006

Figure 6. Host Transmit Output—Eye Height and Eye Width Results for nPPI and SFF8431 (1)

(1) DS280BR810 is configured as eq_high_gain=0 and is in linear mode when performing the nPPI and SFF8431 tests.

5 Detailed Results

5.1 100-GbE CAUI-4

The following figures show the jitter and eye mask measurements for different loss configurations between the host transmitter and the DS280BR810 input on a 100-GbE front-port application.

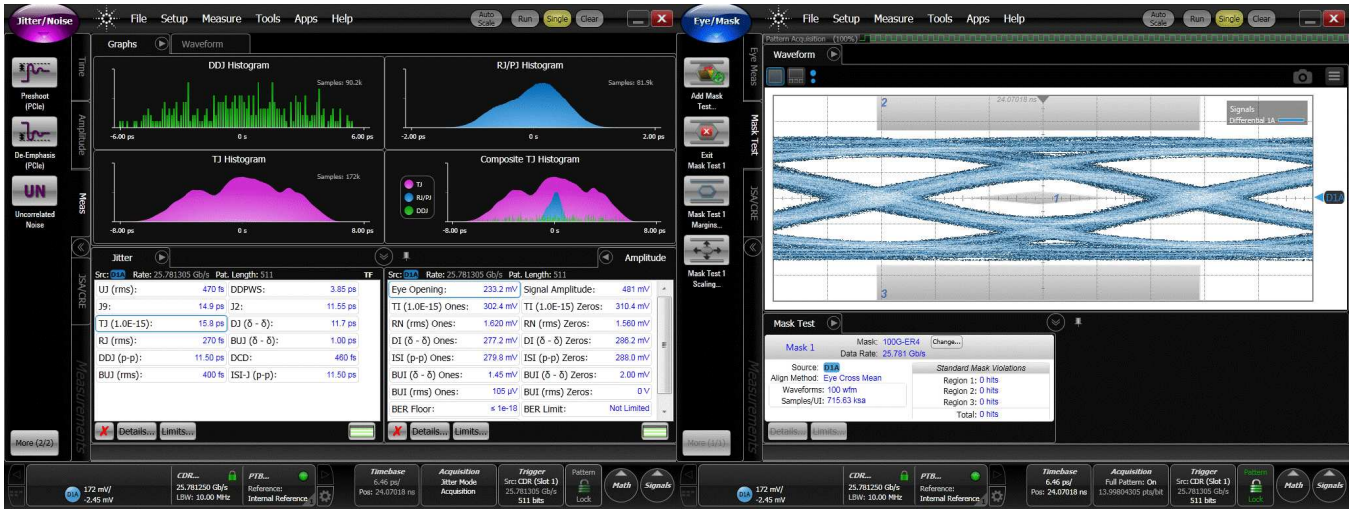


Figure 7. ISI Setting *None*—Bottom

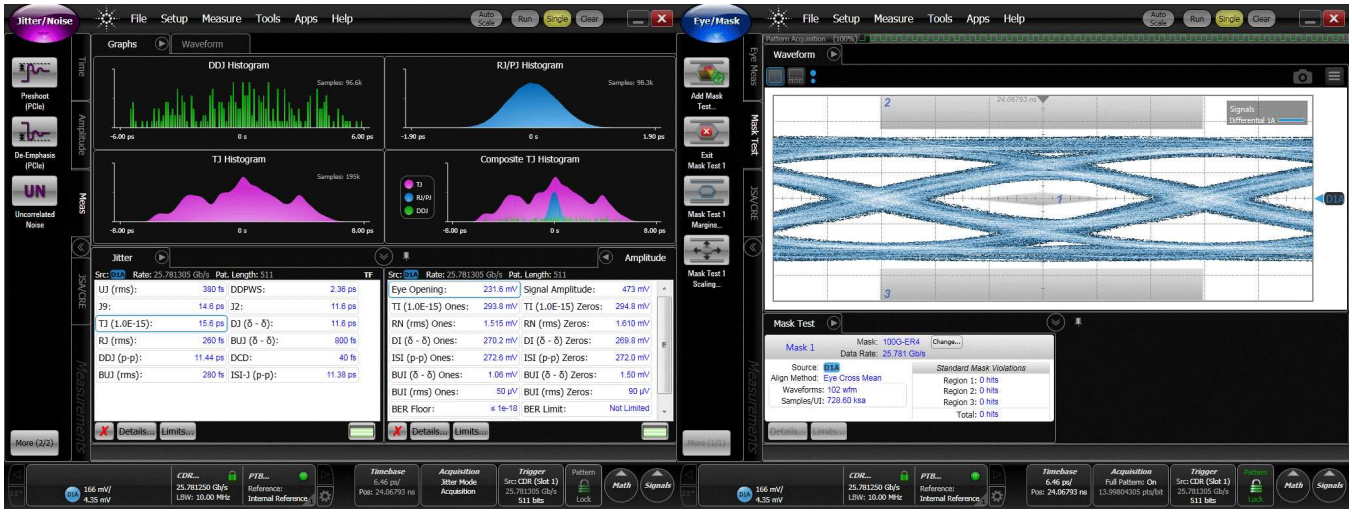


Figure 8. ISI Setting *None*—Top

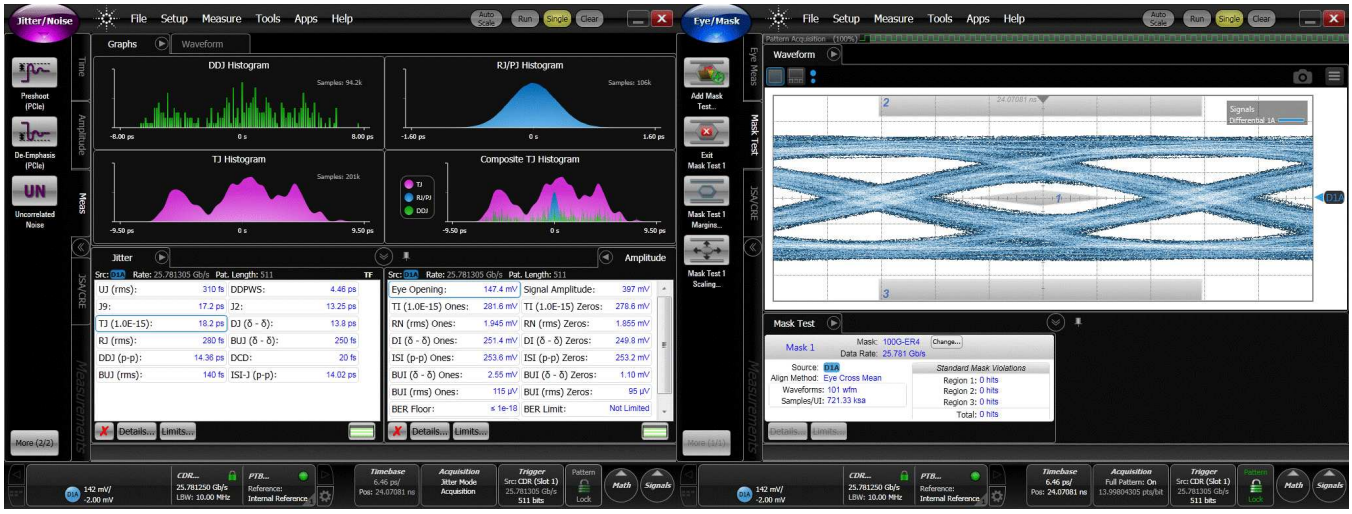


Figure 9. ISI Setting 2—Bottom

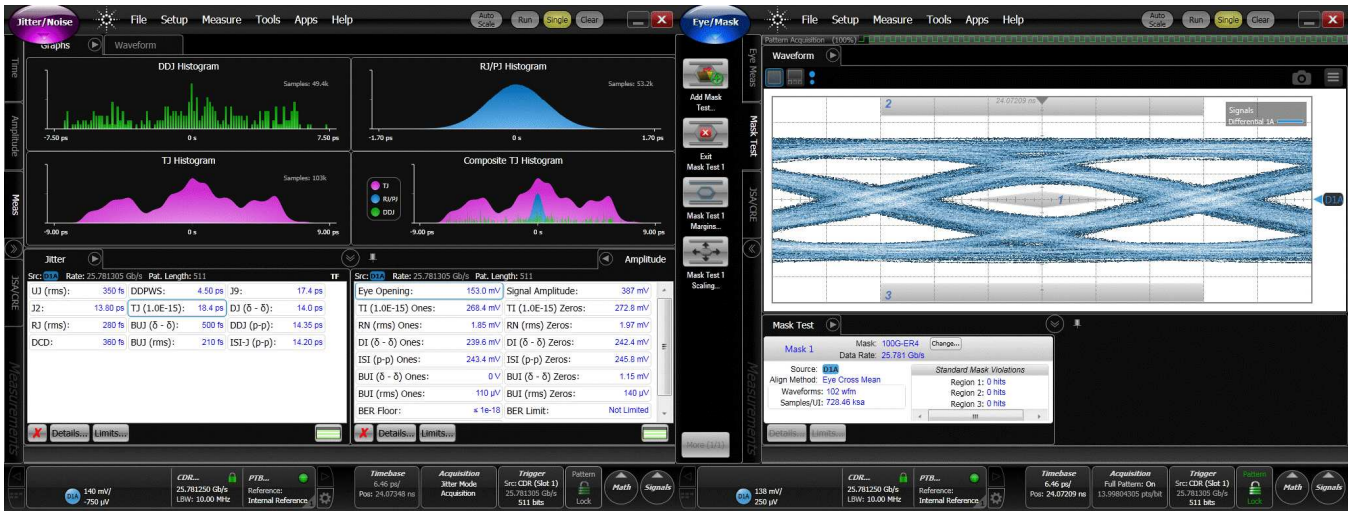


Figure 10. ISI Setting 2—Top

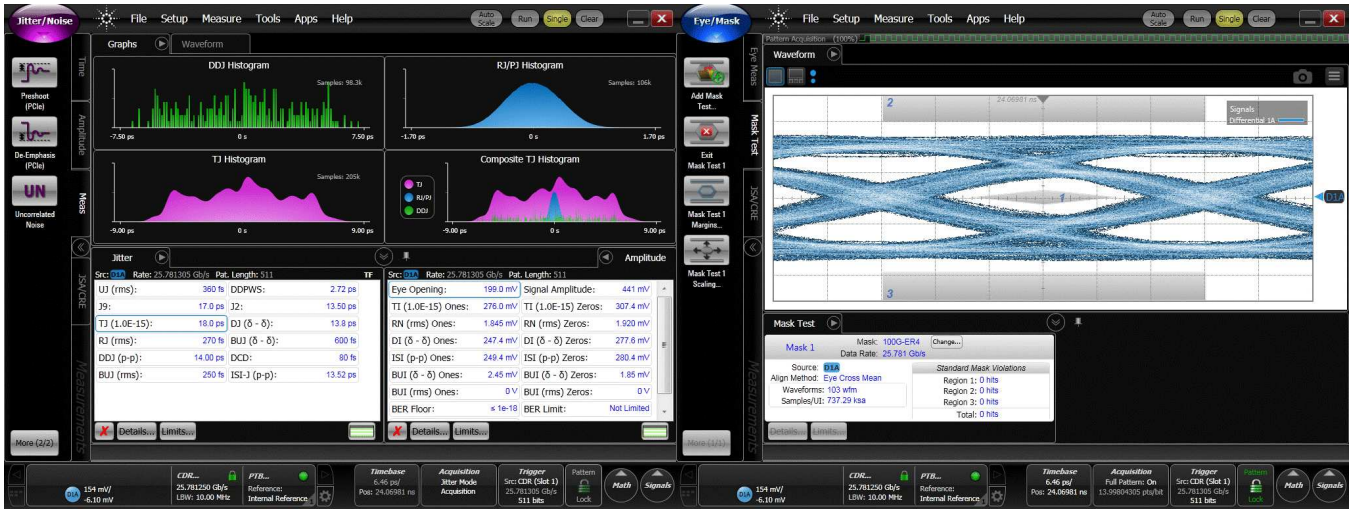


Figure 11. ISI Setting 7—Bottom

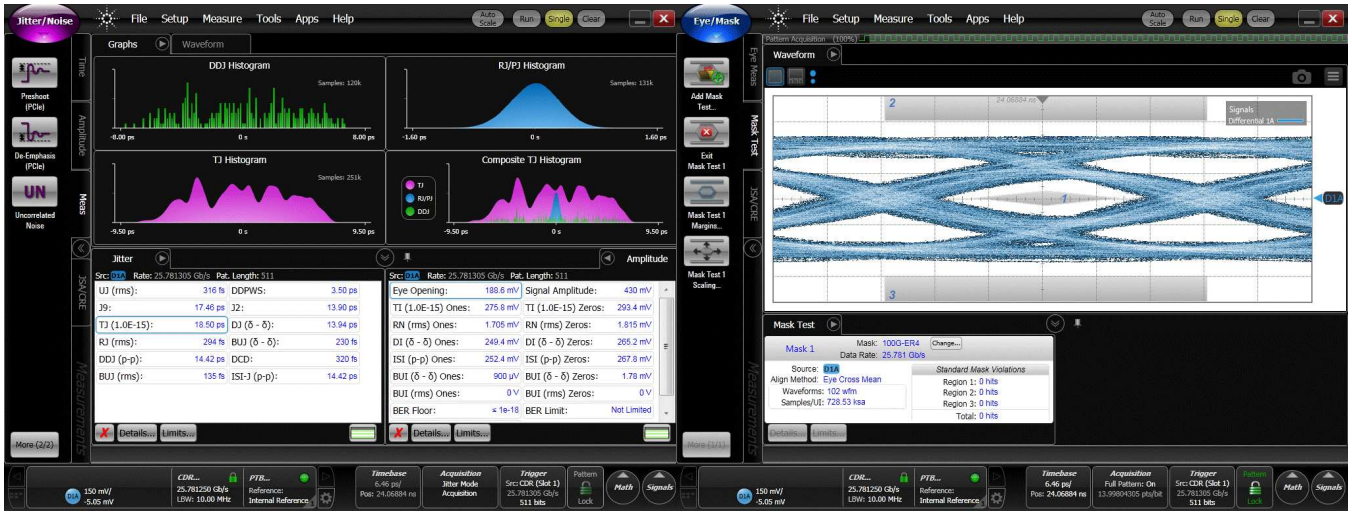


Figure 12. ISI Setting 7—Top

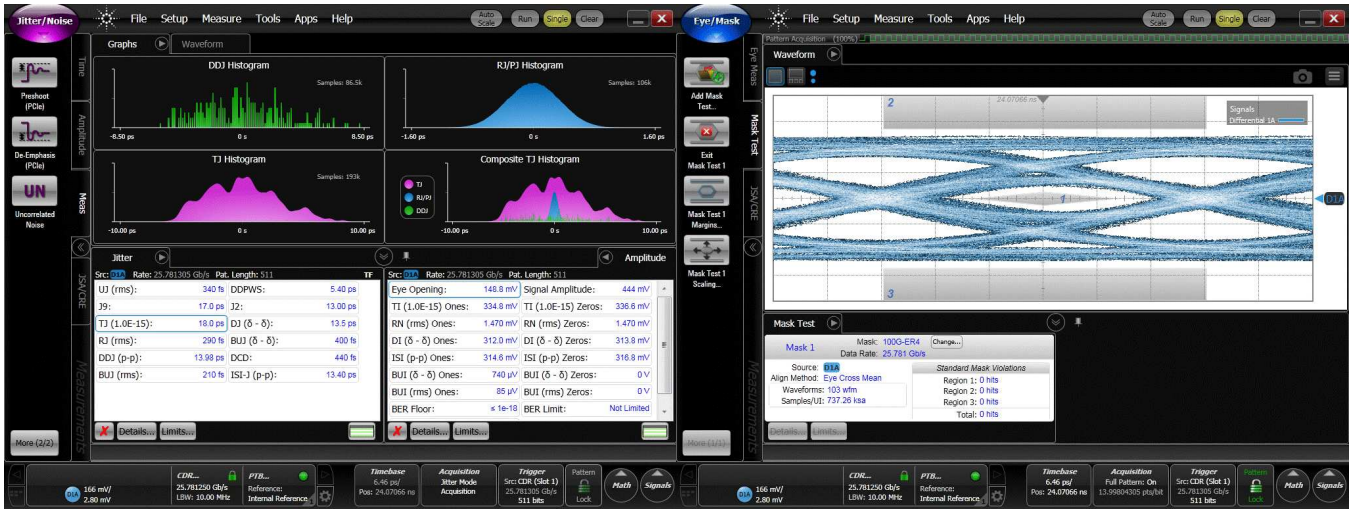


Figure 13. ISI Setting 12—Bottom

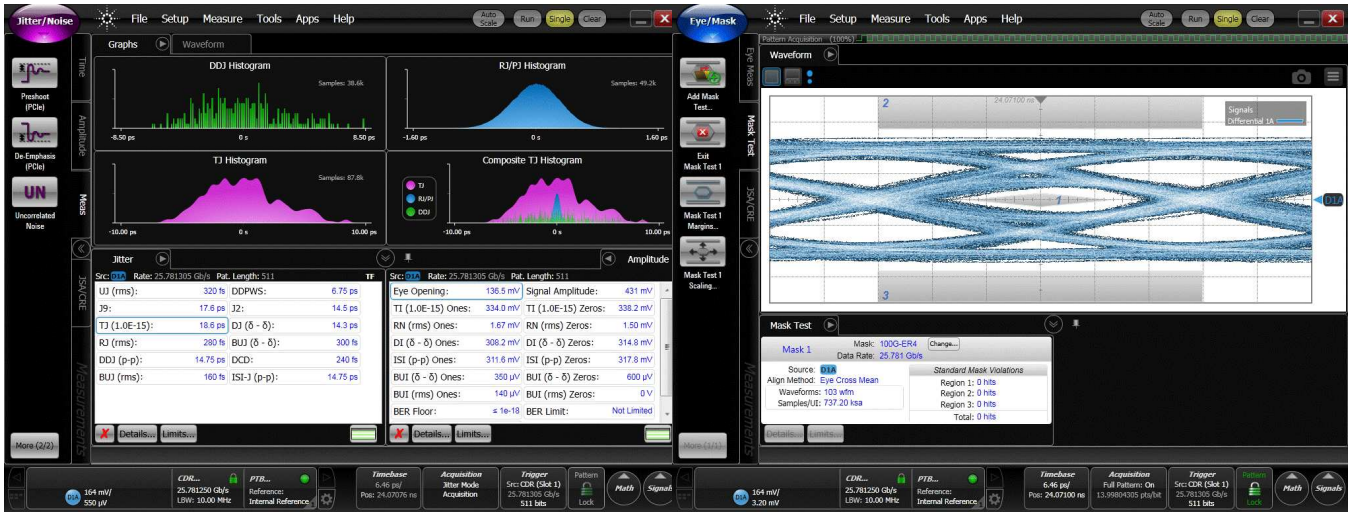


Figure 14. ISI Setting 12—Top

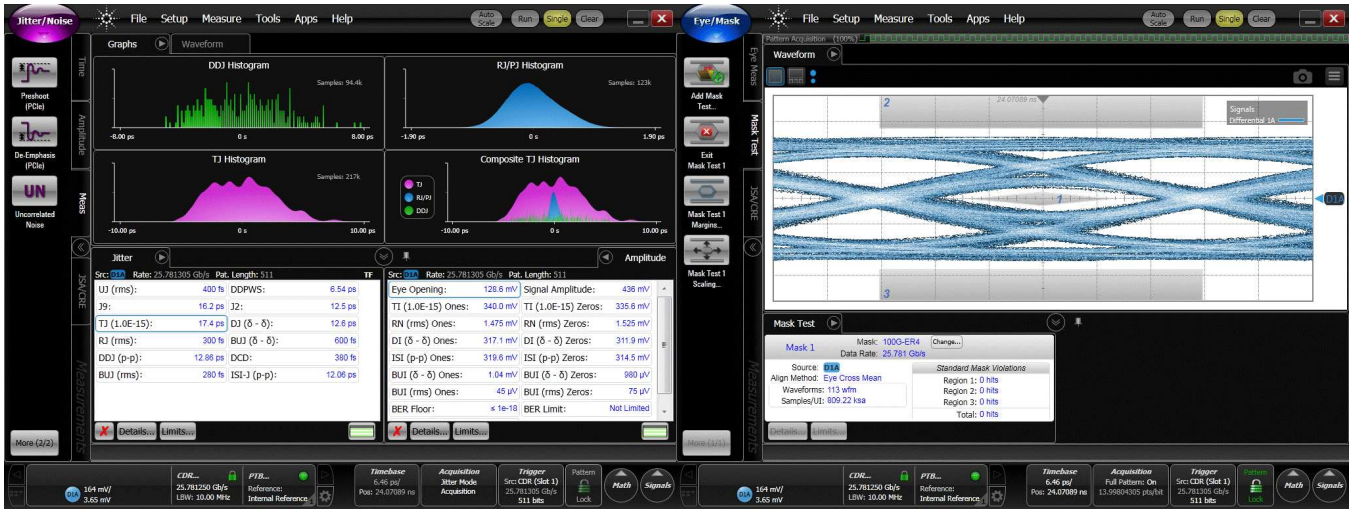


Figure 15. ISI Setting 18—Bottom

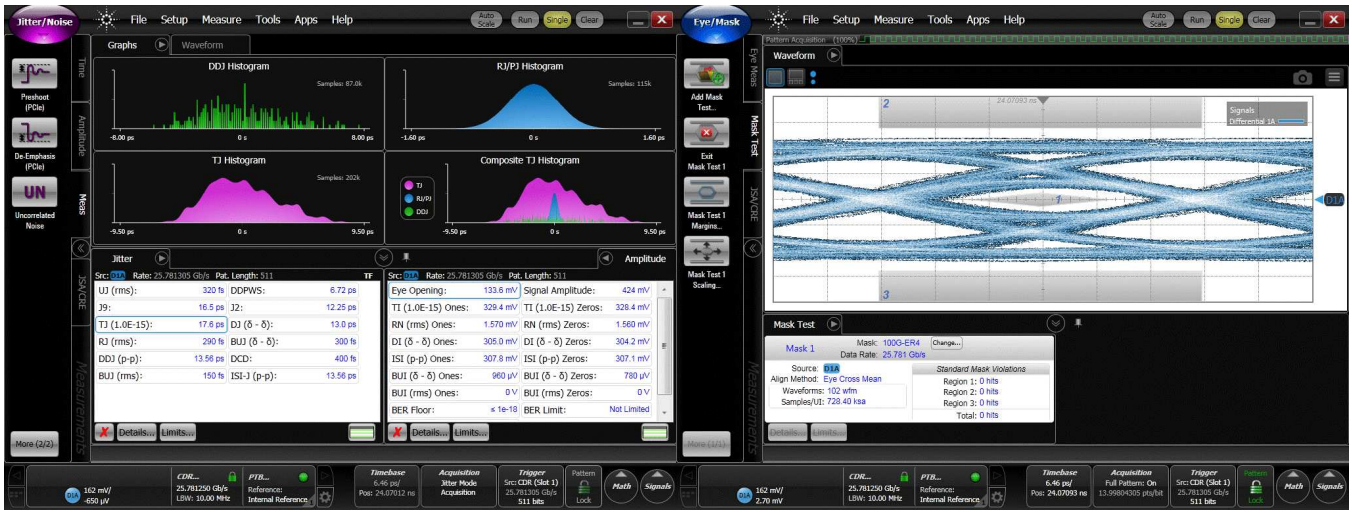


Figure 16. ISI Setting 18—Top

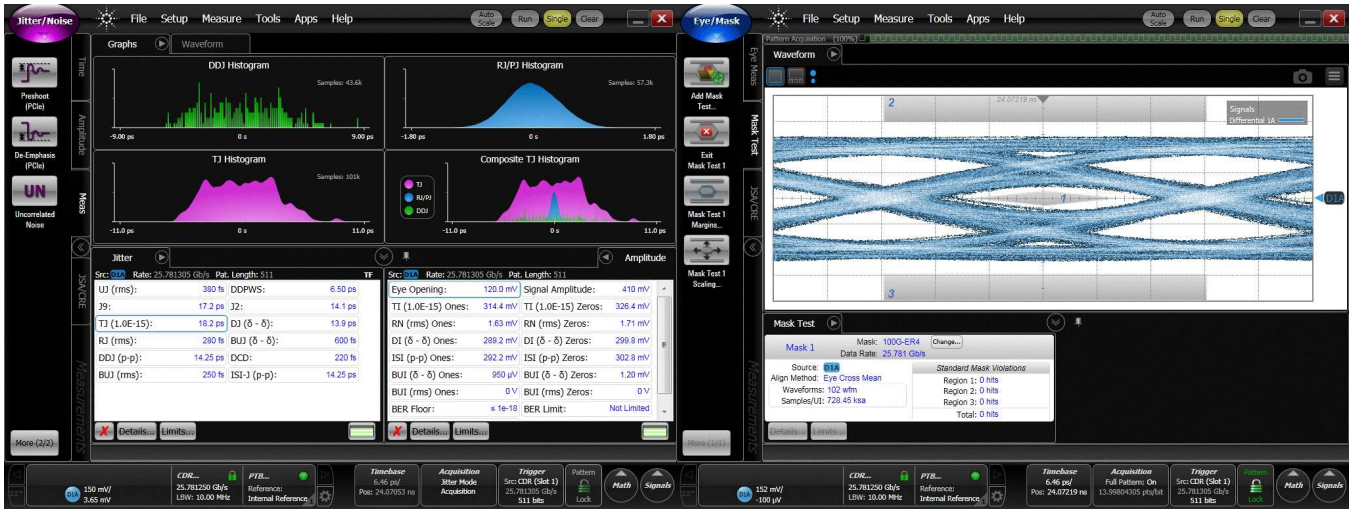


Figure 17. ISI Setting 23—Bottom

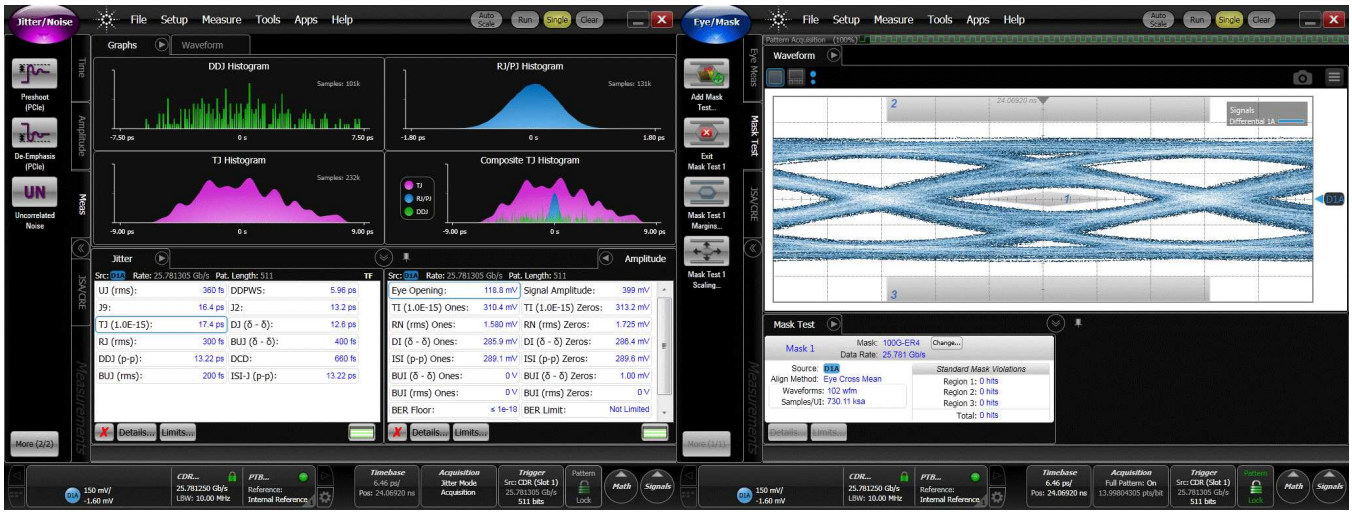


Figure 18. ISI Setting 23—Top

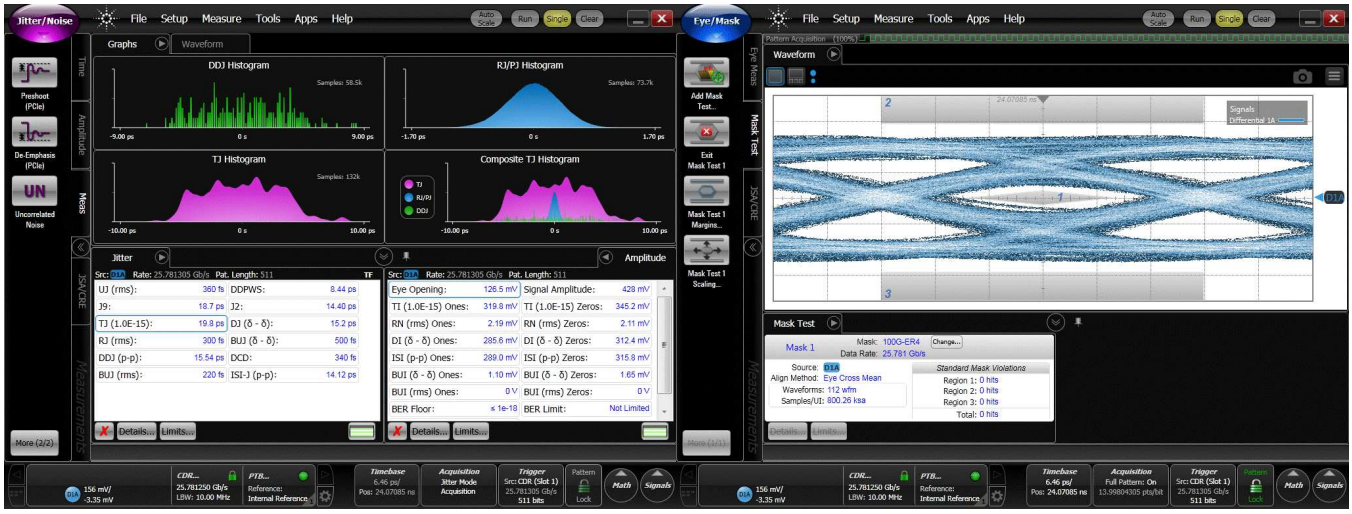


Figure 19. ISI Setting 29—Bottom

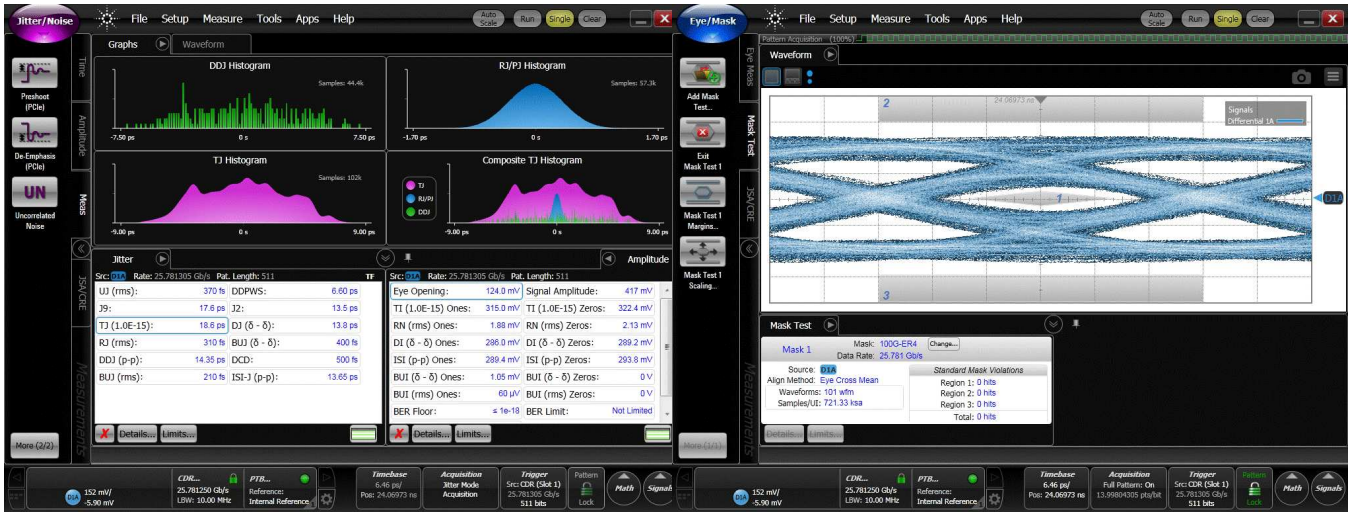


Figure 20. ISI Setting 29—Top

5.2 40-GbE nPPI and SFF8431

The following figures show the jitter and eye mask measurements for different lengths of PCB media between the host transmitter and the DS280BR810 input in a 40-GbE nPPI and 10-GbE SFF8431 front-port application.

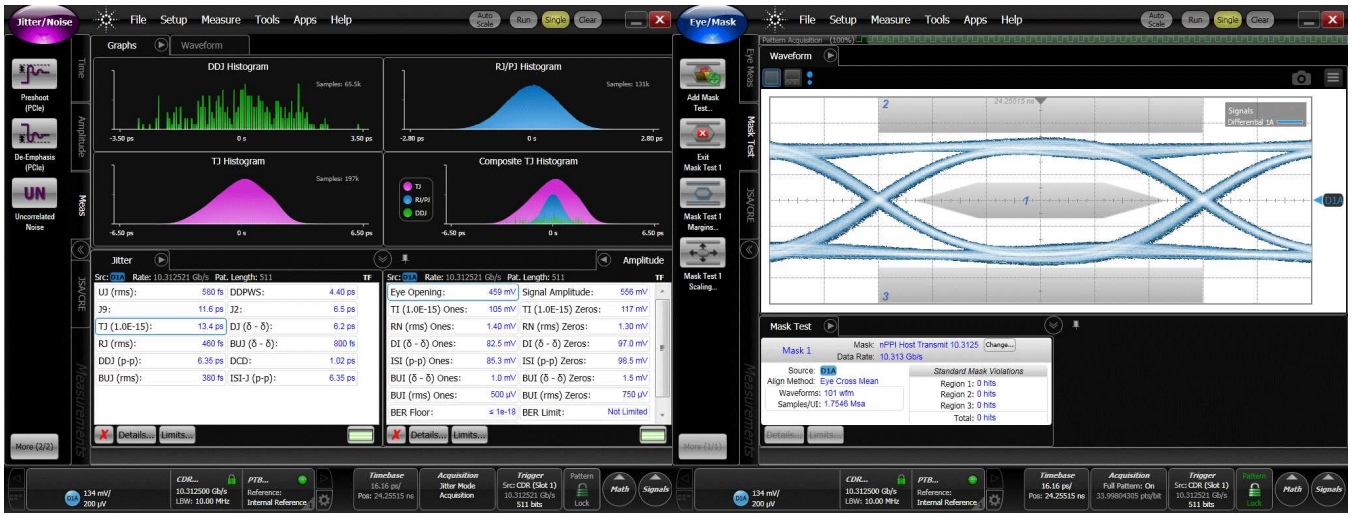


Figure 21. ISI Setting *None*—Bottom

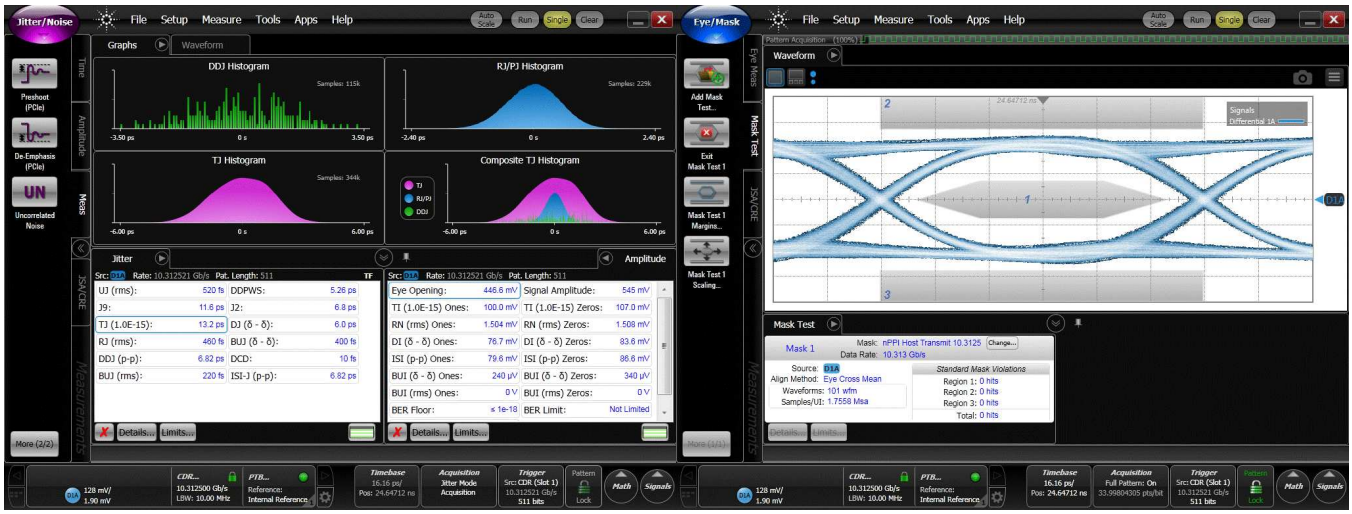


Figure 22. ISI Setting *None*—Top

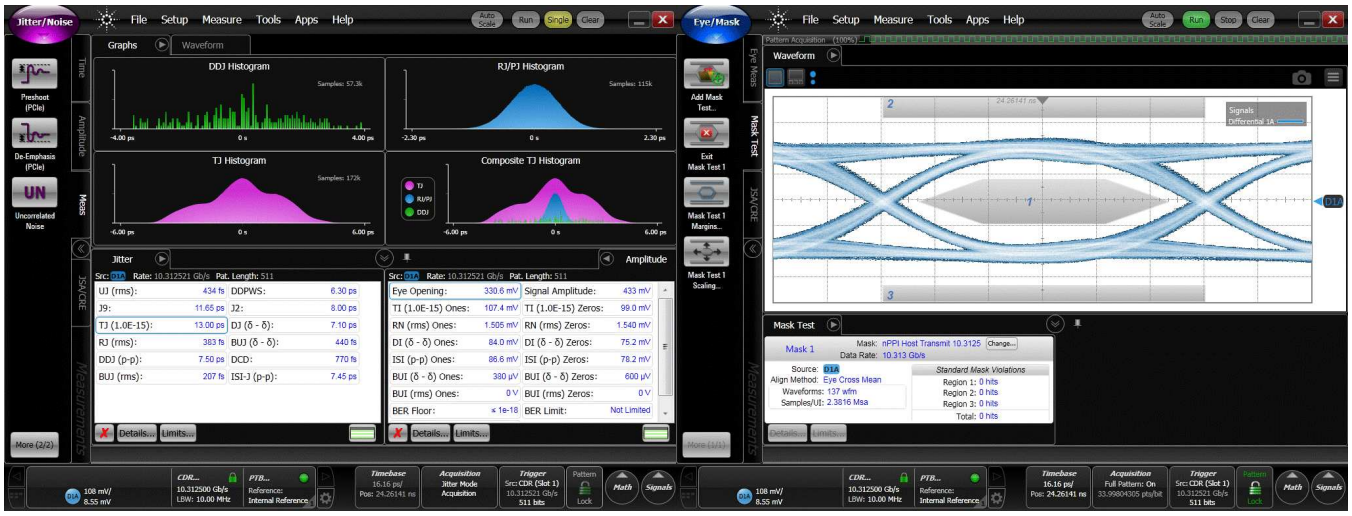


Figure 23. ISI Setting 2—Bottom

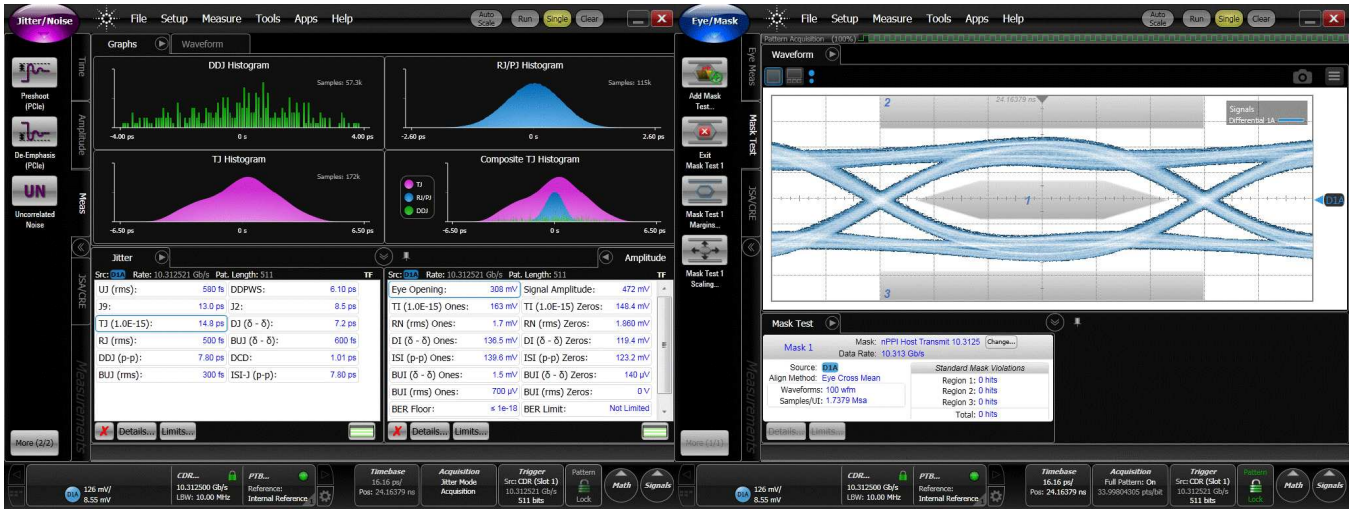


Figure 24. ISI Setting 29—Top

5.3 Layout Considerations

Stacked QSFP28 cages are commonly used in 100-GbE switch applications. The 8-channel DS280BR810 linear repeater easily fits behind a standard 2x1 stacked QSFP28 cage to service all eight egress channels or all eight ingress channels. The fact that the DS280BR810 is unidirectional allows for optimal placement of the signal conditioner: close to the cage for egress applications and close to the switch ASIC for ingress applications.

Figure 25 shows an example layout for the high-speed egress channels between two DS280BR810 devices (placed on the top of the PCB) and a stacked QSFP+ cage (placed on the top of the PCB). The DS280BR810 does not require a heat sink or airflow because the power consumption is 100 mW/channel.

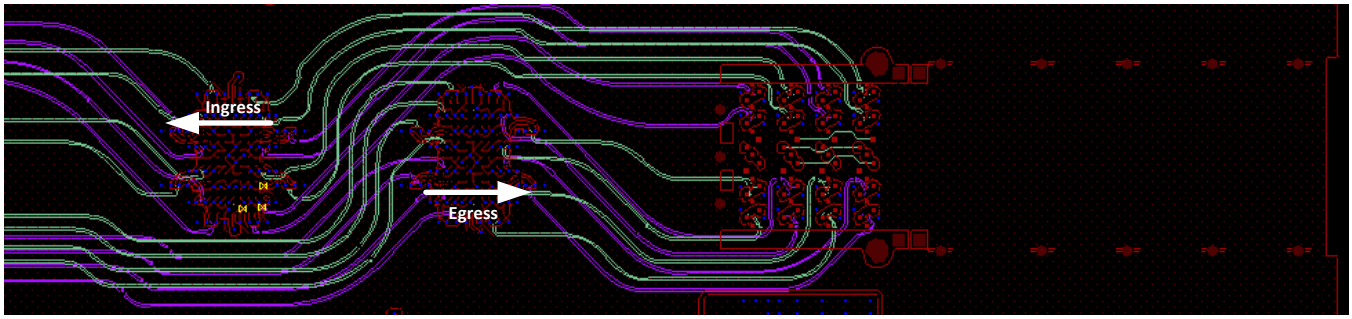


Figure 25. Example Layout for Egress and Ingress Repeaters Alongside Stacked QSFP28 Cage

6 Conclusion

The DS280BR810 linear repeater can enable CAUI-4 TX compliance for channels with up to 22 dB of insertion loss between the Host TX and the DS280BR810 input. The CAUI-4 specification normally limits the insertion loss between the host transmitter and the front-port cage to 7.3 dB. The tests in this report demonstrate that the DS280BR810 linear repeater enables host PCB loss three times greater than the CAUI-4 specifications, extending the channel from 7.3 dB to approximately 22 dB.

7 Design Files

7.1 Schematics

To download the schematics, see the design files at TIDA-00427.

7.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00427.

7.3 Layer Plots

To download the layer plots, see the design files at TIDA-00427.

7.4 CAD Project

To download the CAD project files, see the design files at TIDA-00427.

7.5 Gerber Files

To download the Gerber files, see the design files at TIDA-00427.

7.6 Software Files

To download the software files, see the design files at TIDA-00427.

8 References

1. Texas Instruments, *DS250DF810 25 Gbps Multi-Rate 8-Channel Retimer*, DS250DF810 Data Sheet (SNLS495)
2. IEEE.org, *802.3bm-2015 - IEEE Standard for Ethernet - Amendment 3: Physical Layer Specifications and Management Parameters for 40 Gb/s and 100 Gb/s Operation over Fiber Optic Cables*, IEEE 802.3bm-2015 Standard (https://standards.ieee.org/findstds/standard/802.3bm-2015.html)
3. IEEE.org, *802.3ba-2010 - IEEE Standard for Information technology-- Local and metropolitan area networks-- Specific requirements-- Part 3: CSMA/CD Access Method and Physical Layer Specifications Amendment 4: Media Access Control Parameters, Physical Layers, and Management Parameters for 40 Gb/s and 100 Gb/s Operation*, IEEE 802.3ba Standard (https://standards.ieee.org/findstds/standard/802.3ba-2010.html)
4. SFF Committee, *SFF-8431 Rev 4.1 + Addendum*, (ftp://ftp.seagate.com/sff/SFF-8431.PDF)

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