

Shunt-Based 200-A Peak Current Measurement Reference Design Using Isolation Amplifier



TI Designs

This TI Design provides a reference solution for isolated current measurement using shunt and isolated amplifiers. By limiting the shunt voltage to 25 mV, this design is able to reduce power dissipation in the shunt and achieves a high current measurement range of up to 200 A. Shunt voltage is further amplified by precision op amps in instrumentation amplifier-based configuration with a gain of 10 to match the input range of isolation amplifier. The output of isolation amplifier is level shifted and scaled to utilize the complete input range of 3.3-V ADC. This design uses free running transformer driver for generating isolated supply voltage for the high voltage side of the circuit. Small form factor for the power supply is achieved by the operation of driver at 400 kHz.

Design Resources

TIDA-00445	Design Folder
AMC1200	Product Folder
OPA2376	Product Folder
OPA376	Product Folder
REF2033	Product Folder
SN6501	Product Folder
LM4040	Product Folder

Design Features

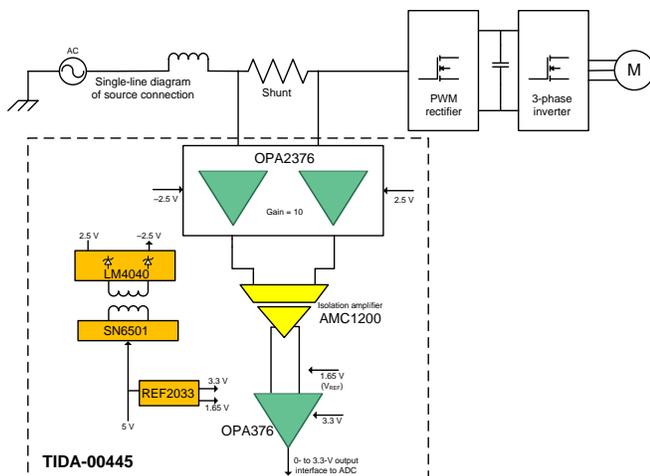
- Shunt-Based Isolated 200-A_{PK} Current Measurement Solution
- Limiting Shunt Voltage to 25 mV Lessens Power Dissipation
- High-Side Current Sense Circuit With High Common-Mode Voltage of 1200-V_{PEAK}, supporting up to 690-V AC Mains Powered Drives
- Calibrated AC Accuracy of < 1% Across Temperatures -25°C to 85°C
- Can Interface Directly With Differential or Single-Ended ADC
- Small Form Factor Push Pull-Based Isolated Power Supply to Power High-Side Circuit
- Built-in 1.65-V_{REF} to Level Shift Output

Featured Applications

- Active Front-End Converters
- UPS
- Variable Speed Drives



[ASK Our E2E Experts](#)



All trademarks are the property of their respective owners.



An IMPORTANT NOTICE at the end of this TI reference design addresses authorized use, intellectual property matters and other important disclaimers and information.

1 System Description

Current measurement is an inherent part of any inverter-driven application such as motor control, UPS, active front-end (AFE) converters, and so on. Motor control algorithms like vector control and direct torque control require current sensing for control purposes. Active front-end converters also measure grid current to ensure they are in phase with voltage. Current measurement in UPS is used to control the battery charging current as well as inverter operation and overload protection.

AFE converters are often used in high-performance adjustable speed drives (ASDs) where frequent acceleration and de-acceleration is required. AFE converters have many advantages like constant DC voltage, fast dynamic response, unity power factor, low harmonic distortion, and bidirectional power flow. Generally, two control methods have been proposed for PWM rectifiers: Voltage-oriented control (VOC) and direct power control (DPC). The main goal of these control techniques is to reduce the current harmonic and to regulate the DC bus voltage.

For normal operation, AFE requires three kinds of sensors to detect AC voltages, AC currents, and DC voltage. A DC voltage sensor is demanded for the DC voltage feedback control and excessive voltage protection. The two AC voltage sensors are needed to detect the phase angle of the source voltage, which is taken as a reference frame of the controller, and thus to perform input power factor control. The two line current sensors are required for the input current control for boosting action and excessive current protection. Alternatively, the single current sensor technique of PWM inverters can be applied to the AFE, where the phase currents are reconstructed using the measured DC link currents and the switching states of the PWM inverter. Current sensor locations in the AFE are depicted in [Figure 1](#).

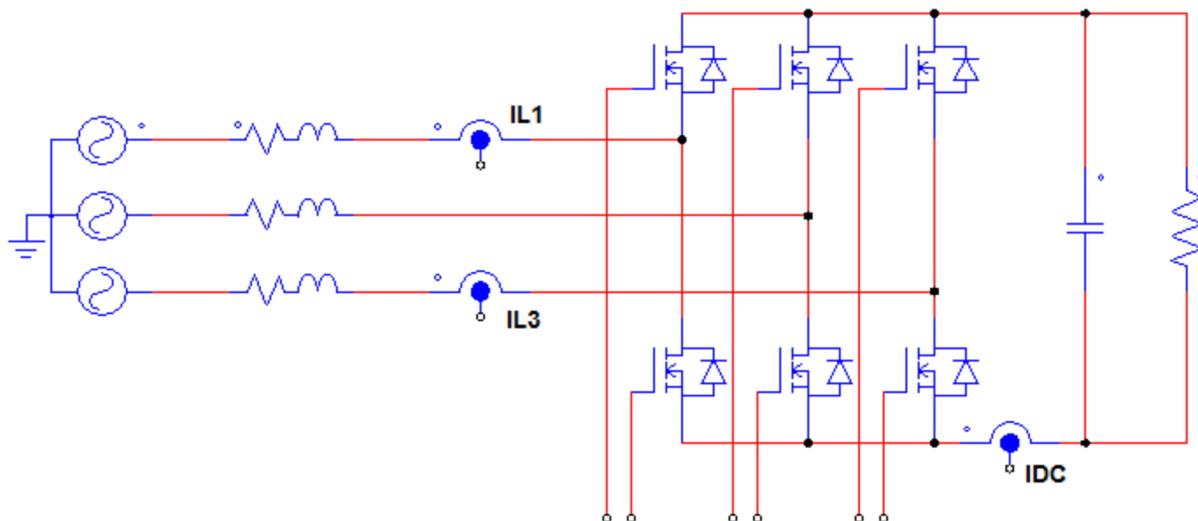


Figure 1. Current Sensor Locations in AFE

Multiple solutions exist today to measure current like Hall, flux gate sensors, current transformers, and shunt. Magnetic-based solutions inherently offer isolation benefits and have the capability to measure higher currents. However, magnetic-based solutions can be expensive. The shunts are usually limited to measure currents less than 50 A owing to higher power dissipation. This TI Design provides a low-cost solution to enhance current measurement range using a 125- $\mu\Omega$ shunt up to 200 A_{PK} with isolation amplifier and signal conditioning circuit. The voltage across the shunt is limited to 25 mV, which is subsequently amplified to 250 mV by a gain stage before fed to the isolation amplifier. The complete circuit design with simulation and test results are covered in this design guide. The current measurement range can be further enhanced by reducing the value of the shunt.

2 Key System Specifications

Table 1. Key System Specifications

PARAMETER	SPECIFICATION
Maximum current	200 A _{PK}
Current type	AC and DC
Common-mode voltage	1200 V _{PK}
Calibrated accuracy	< 1%
Common-mode transient immunity	15 kV/μs
Output	150 mV to 3.15 V
Operating ambient temperature	–25°C to 85°C
Features	Isolated current sense outputs designed to be interfaced to 3.3-V built-in ADCs of MCUs

3 Block Diagram

The block diagram for current measurement using shunt is shown in Figure 2. The main parts of this design consists of gain stage succeeding shunt using a precision op amp (OPA2376), an isolation amplifier (AMC1200), and a differential to single-ended conversion using the OPA376.

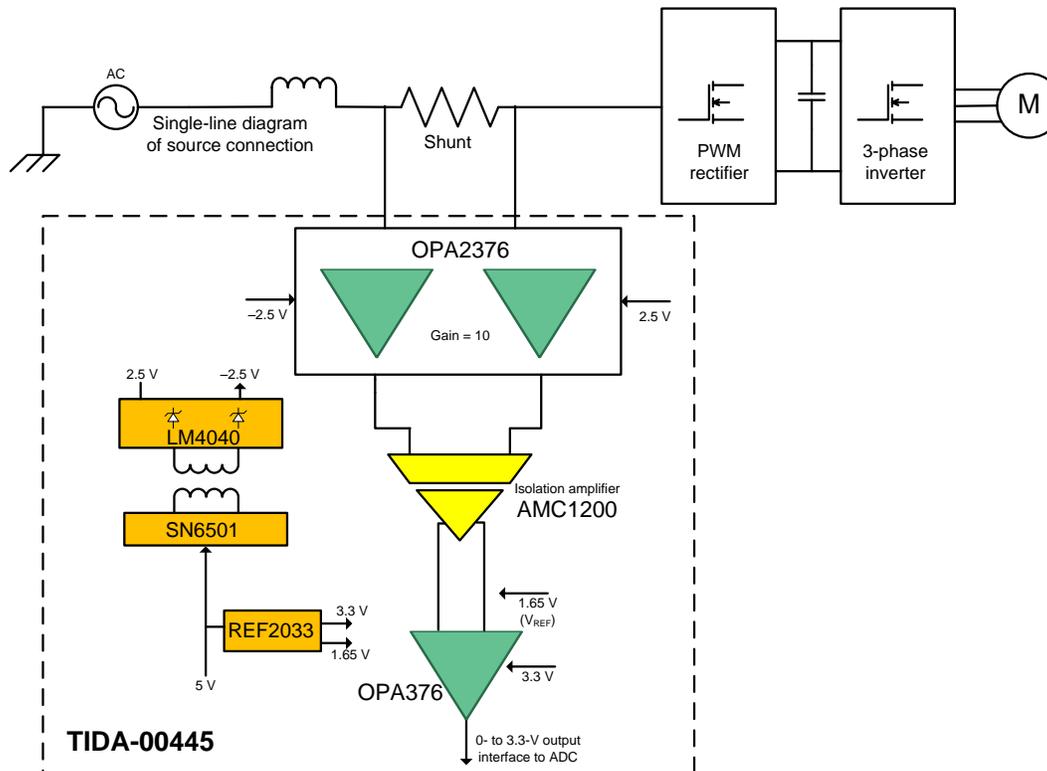


Figure 2. Block Diagram for Current Measurement Using Shunt

The front-end gain stage is designed using the OPA2376 in instrumentation amplifier topology enabling it to accept differential input and have differential output. The overall gain of this stage is set to 10 for amplifying the ± 25 mV across the shunt to ± 250 mV to fit the input range of the isolation amplifier. The OPA2376 is supplied with ± 2.5 V.

The next stage involves the AMC1200, which provides galvanic isolation of up to $4000 V_{PEAK}$ between the high-voltage and low-voltage circuit. It has a fixed internal gain of 8 and accepts a maximum input of ± 250 mV to operate in a linear region. It is powered on the high-voltage side by ± 2.5 V and on the low-voltage side by 3.3 V, thus giving a differential output at a common-mode voltage of 1.29 V. This common-mode voltage can either be given directly to differential ADC or to next level shifter stage.

The output of isolation amplifier is fed to level shifter circuit. This circuit converts the differential output from the AMC1200 to a single-ended signal along with level shift to match the input range of the single-ended ADC. This is achieved using the precision op amp OPA376, and the final output is mapped on to 0 to 3.3 V. This op amp is powered using 3.3 V with a reference voltage of 1.65 V for level shifting.

The power supply circuit consists of the REF2033 and the SN6501.

The REF2033 derives 3.3 and 1.65 V from a 5-V supply. 3.3 V is used to power the OPA376 and the low-voltage side of the AMC1200. 1.65 V is used for as a reference voltage for the OPA376 to map output of isolation amplifier to 0 to 3.3 V.

The SN6501 drives the transformer to generate an isolated power supply for powering the high-voltage side of the circuit consisting of the front-end gain stage and the high side of the AMC1200. It is powered from the 5-V input supply.

3.1 Highlighted Products

This TIDA-00445 reference design features the following devices, which were selected based on their specifications. The key features of the highlighted products are mentioned as follows. For more information on each of these devices, see their respective product folders at <http://www.ti.com> or click on the links for the product folders on the first page of this reference design.

3.1.1 OPA376, OPA2376

The OPA376 family represent a new generation of low-noise operational amplifiers with e-trim, offering outstanding AC precision and AC performance. Rail-to-rail input and output, low offset (25 μ V max), low noise (7.5 nV/ \sqrt Hz), quiescent current (950 μ A max), and a 5.5-MHz bandwidth make this part very attractive for a variety of precision and portable applications.

In this design, the OPA2376 works as an instrumentation amplifier for the front-end gain stage and in level shifter circuit.

This op amp was chosen for this design for its extremely low voltage offset, low temperature drift, rail-to-rail output, low noise, and low cost.

3.1.2 AMC1200

The AMC1200 is a precision isolation amplifier with an output separated from the input circuitry by a silicon dioxide (SiO₂) barrier that is highly resistant to magnetic interference. This barrier has been certified to provide galvanic isolation of up to 4000 V_{PEAK} according to VDE-V 0884-10 and UL1577. Used in conjunction with isolated power supplies, this device prevents noise currents on a high common-mode voltage line from entering the local ground and interfering with or damaging sensitive circuitry.

The excellent performance of this device supports accurate current control resulting in system level power saving and especially in motor control applications, lower torque ripple.

The AMC1200 is used in this design to provide galvanic isolation between the high and low voltage sides. It was selected mainly because of its very high transient immunity (10 kV/ μ s min), very low non-linearity (0.075 % max), and very low offset error.

3.1.3 REF2033

Applications with only a positive supply voltage often require additional stable voltage in the middle of the ADC input range to bias input bipolar signals. The REF2033 provides a reference voltage for the ADC and a second highly accurate voltage that can be used to bias the input bipolar signals.

The REF2033 offers excellent temperature drift (8 ppm/ $^{\circ}$ C, max) and initial accuracy (0.05%) on both the V_{REF} and V_{BIAS} outputs while operating at a quiescent current less than 430 μ A. In addition, the V_{REF} and V_{BIAS} outputs track each other with a precision of 6 ppm/ $^{\circ}$ C (max) across the temperature range of -40° C to 85° C. All these features increase the precision of the signal chain and decrease board space, while reducing the cost of the system as compared to a discrete solution. Both the V_{REF} and V_{BIAS} have the same excellent specifications and can sink and source current equally well. Very long-term stability and low-noise levels make these devices ideally suited for high-precision industrial applications.

The REF2033 is used for its dual outputs in very small package, very low drift in output with temperature, and for its V_{REF} and V_{BIAS} tracking for higher accuracy.

3.1.4 SN6501

The SN6501 is a monolithic oscillator and power driver, specifically designed for small form factor, isolated power supplies in isolated interface applications. The device drives a low-profile, center-tapped transformer primary from a 3.3- or 5-V DC power supply. The secondary can be wound to provide any isolated voltage based on transformer turns ratio.

This device includes an oscillator that feeds a gate-drive circuit. The gate-drive, comprised of a frequency divider and a break-before-make (BBM) logic, provides two complementary output signals that alternately turn the two output transistors on and off with a duty cycle of 50%.

The SN6501 is used in this design for its isolated power supply to power the AMC1200 high-voltage side and first gain stage.

4 System Design Theory

This section details the design procedure for each circuit section.

4.1 Selection of Shunt Resistor

The value of the shunt resistor is chosen to have a 25-mV drop across it while the 200-A current is flowing through it, leading to $125\ \mu\Omega$. The minimum power handling capability of the shunt must be 5 W. For testing purpose, two $250\text{-}\mu\Omega$ resistors (CSS2725FTL250CT from Stack pole Electronics) were connected in parallel with each having a 125-A current capability and 4-W dissipation. Other important parameters include the resistance tolerance, the temperature coefficient of resistance, low thermal EMF, and low inductance.

4.2 Front-End Gain Stage With Isolation Amplifier

4.2.1 Gain Stage Using OPA2376

This design is aimed to measure current as high as 200-A DC or 200-A peak-to-peak AC with a maximum drop of 25 mV across the shunt. The major requirement of this particular stage is to provide an amplified differential output to match the input (250 mV) of the isolation amplifier.

The individual op amp gains are set to 5, leading to a total gain of 10. Because the outputs are differential, each op amp provides an output of $\pm 125\ \text{mV}$ out of phase with each other by 180° . This is achieved by the configuration shown in Figure 3, which resembles instrumentation amplifier configuration:

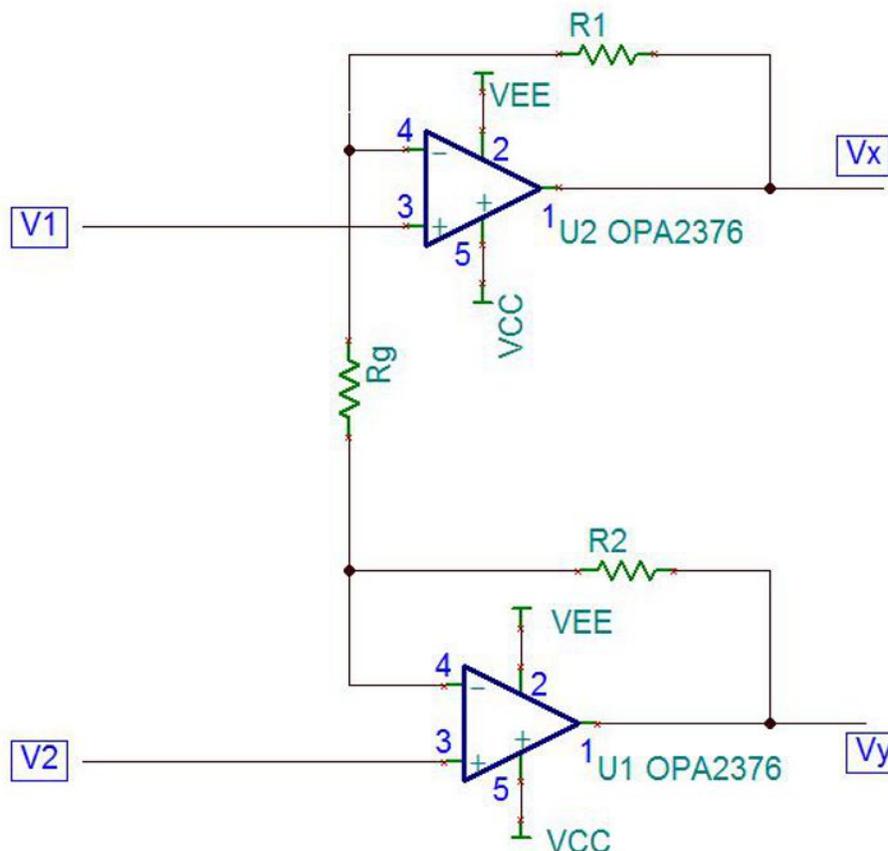


Figure 3. Configuration to Get Differential Output

The voltage drop across the shunt is given to positive terminals of both op amps shown in [Figure 3](#).

Applying KVL to the loop $V_X - R_1 - R_G - R_2 - V_Y$:

$$V_X - IR_1 - IR_G - IR_2 - V_Y = 0$$

$$V_X - V_Y = I(R_1 + R_G + R_2) \quad (1)$$

Here, I is given as $I = \frac{V_1 - V_2}{R_G}$ [Equation 1](#) now becomes:

$$V_X - V_Y = \frac{V_1 - V_2}{R_G} (R_1 + R_G + R_2)$$

$$V_X - V_Y = (V_1 - V_2) \left(1 + \frac{R_1 + R_2}{R_G} \right) \quad (2)$$

In this design, V_2 is grounded with the high-voltage side ground of the board. Thus, considering V_2 to be at ground potential with respect to V_1 :

$$V_X - V_Y = V_1 \left(1 + \frac{R_1 + R_2}{R_G} \right)$$

Since the design needs a differential output that can directly be given to isolation amplifier, V_X and V_Y must be equal and opposite of each other:

$$V_X = -V_Y \quad (3)$$

Again referring to [Figure 3](#), if V_2 is considered at ground potential, V_X and V_Y now become

$$V_X = I(R_1 + R_G)$$

$$V_Y = -IR_2$$

According to [Equation 3](#):

$$I(R_1 + R_G) = -(-IR_2)$$

$$R_1 + R_G = R_2 \quad (4)$$

[Equation 4](#) shows one of the constraints for choosing the values of resistors. To provide an overall gain of 10, each individual op amp has to provide a gain of 5 so that both the inputs to isolation amplifier are equal and opposite.

Again looking at [Figure 3](#), considering V_2 to be at ground potential, U_2 is behaving like a non-inverting amplifier having transfer function:

$$V_X = V_1 \left(1 + \frac{R_1}{R_G} \right)$$

To have a gain of 5:

$$\frac{R_1}{R_G} = 4 \rightarrow R_1 = 4R_G \quad (5)$$

From [Equation 4](#) and [Equation 5](#), $R_2 = 5R_G$.

In order to limit the gain error, 0.1% accurate resistors are chosen. The choices of feedback resistors are restricted to less than 10 k Ω to reduce the impact of noise voltages. Based on availability and accuracy needed, the values chosen for this design are $R_G = 1.27$ k Ω , $R_1 = 5.1$ k Ω , and $R_2 = 6.34$ k Ω .

The simulation results using TINA-TI for this particular section are shown in [Figure 4](#). All TINA-TI models can be found on the respective device product folders.

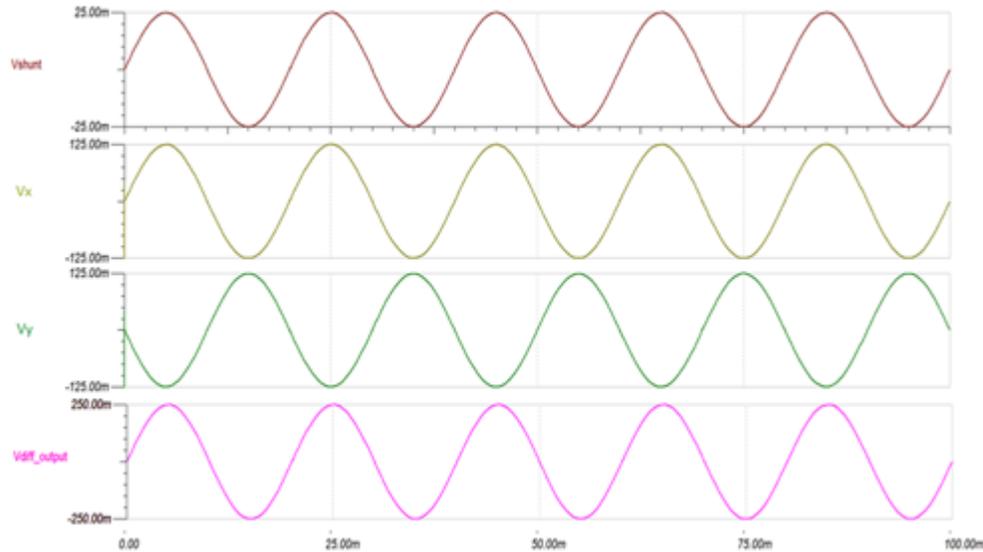


Figure 4. Simulation Result of Gain Stage

- V_{SHUNT} is the voltage across shunt
- V_x is the output of upper op amp in the schematic
- V_y is the output of lower op amp in the schematic
- V_{DIFF_OUTPUT} is the output of this gain stage.

An RC filter of 20-kHz cut-off frequency is added before the gain stage to avoid entry of any high frequency noise into the circuit. This filter can be changed according to the requirements of bandwidth versus noise immunity. The schematic for this stage is shown in [Figure 5](#).

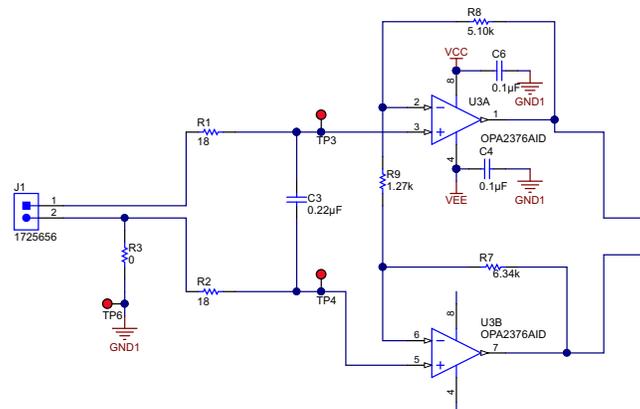


Figure 5. First Gain Stage

Connector J1 is used to connect the front-end stage with the shunt. The output of this gain stage is fed to isolation amplifier through the RC filter.

4.2.2 Isolation Amplifier

This design uses the AMC1200 to provide galvanic isolation between the high- and low-voltage sides. The AMC1200 provides a fixed gain of 8 along with level shifting the output. The high-voltage side is to be powered by 5 V while the low-voltage side can be powered either by 5 V or 3.3 V depending on the level shift of the output required.

This design uses ± 2.5 V to power the high-voltage side and 3.3 V to power the low-voltage side. A TINA simulation model for the isolation amplifier along with gain stage is shown in Figure 6. Here, $V_{DIFF_OUTPUT} = \pm 250$ mV, where V_{DIFF_OUTPUT} is the output of gain stage which is given to isolation amplifier, and $V_{ISO_OUT} = \pm 250$ mV $\times 8 = \pm 2$ V, where V_{ISO_OUT} is the output of isolation amplifier.

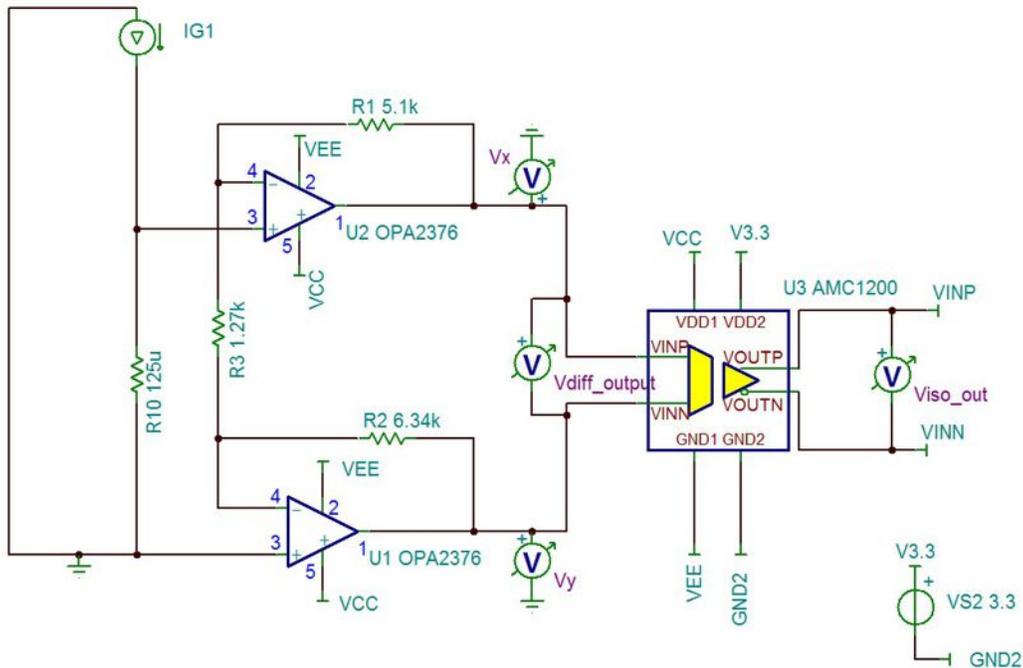


Figure 6. TINA Model of Isolation Amplifier and First Gain Stage

In Figure 6, a current of 200 A is passed through a resistor of 125 $\mu\Omega$, resulting in a voltage drop of 25 mV, which is amplified 10 times and given to the isolation amplifier. The output of both stages are shown as simulation results in Figure 7.

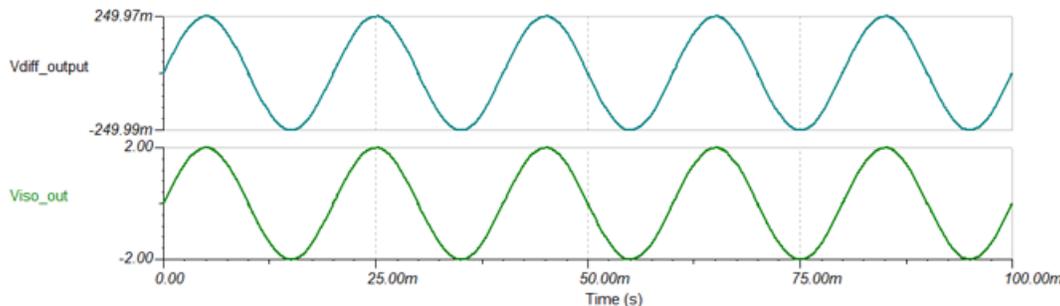


Figure 7. Simulation Result of Isolation Amplifier

The schematic for this circuit is shown in Figure 8.

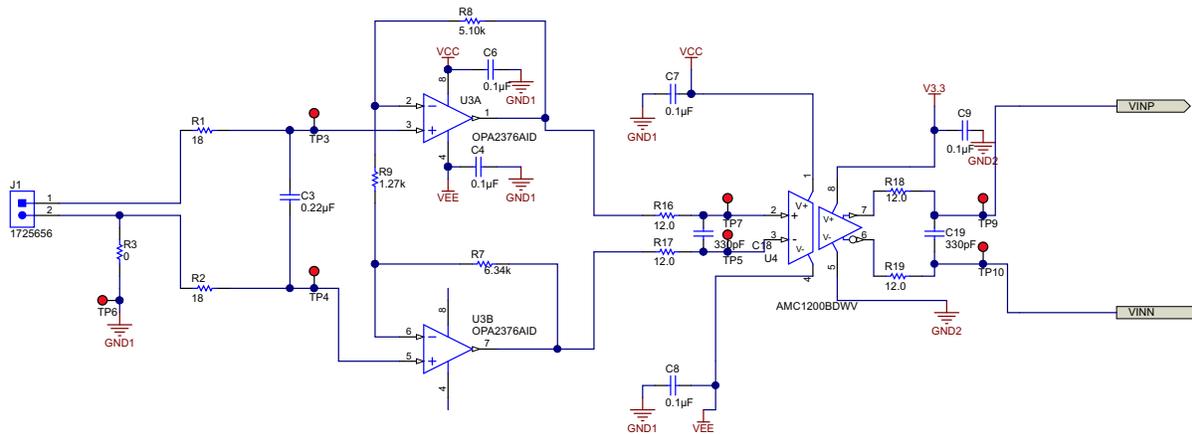


Figure 8. Isolation Amplifier Along With Front-End Amplifier

4.3 Differential to Single-Ended Conversion

In order to use the complete 3.3-V dynamic input range of the ADCs, the ± 2 -V output swing is mapped onto approximately 0 to 3.3 V. This is accomplished by the differential amplifier stage shown in Figure 9. The OPA376 was chosen for this stage mainly because of its low offset and high CMRR.

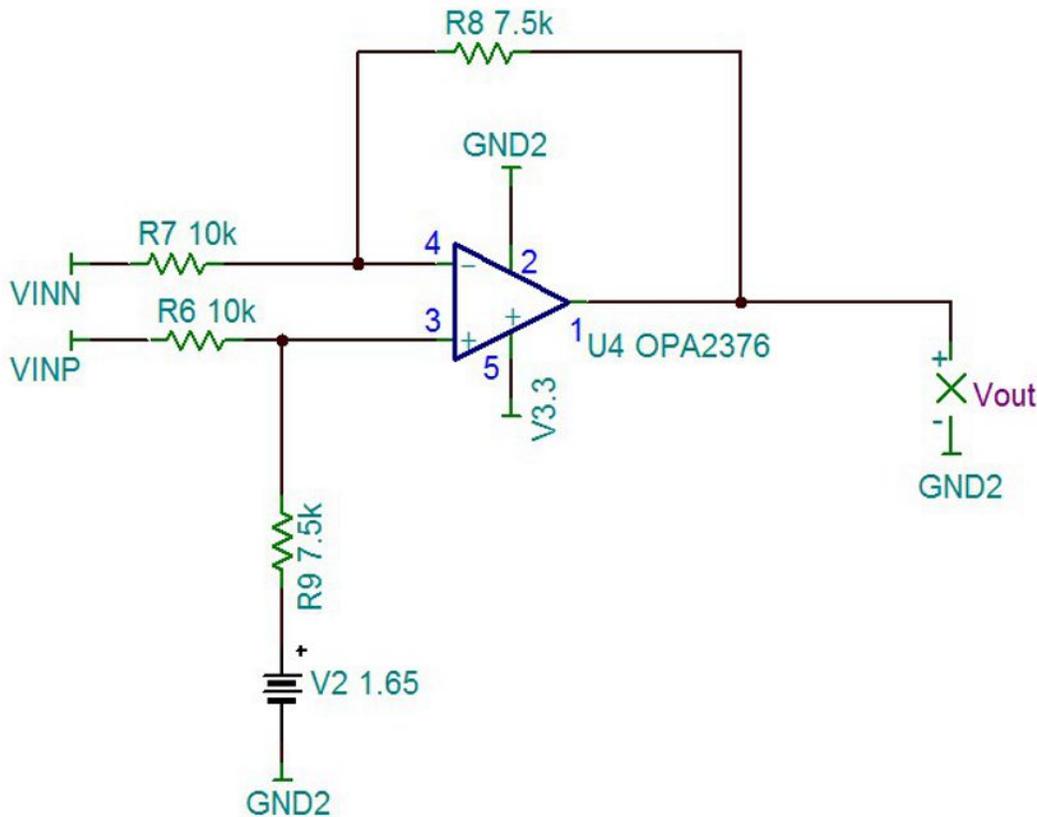


Figure 9. TINA Model for Differential to Single-Ended Conversion

The transfer function for this circuit can be derived easily considering $R_{13} = R_{12}$ and $R_{11} = R_{10}$ (see [Figure 11](#)) and using only two variables for them. The transfer function turns out to be:

$$V_{OUT} = (V_{INP} - V_{INN}) \left(\frac{R_{13}}{R_{11}} \right) + V_{REF} \tag{6}$$

Here, V_{REF} is 1.65 V.

The OPA376 output voltage swing is limited up to 10 mV from the rails typically and 20 mV over temperature. Considering the mismatch in resistor values, the output voltage is designed to be limited to a little over 100 mV from the rails.

The ± 2 -V input to the differential amplifier is to be mapped onto nearly 0 to 3.3 V with 1.65 V_{REF} . Providing a window of 150 mV from the rails, the maximum swing of output becomes 0.15 to 3.15 V. As a result, the positive and negative swing that is allowed is $3.15 \text{ V} - 1.65 \text{ V} = 1.5 \text{ V}$ riding over 1.65 V_{REF} .

Thus, the ratio of resistors needed to achieve this shift is calculated as given:

$$\text{Max swing allowed} = \frac{R_{13}}{R_{11}} (V_{INP} - V_{INN}) \tag{7}$$

$$1.5 = \left(\frac{R_{13}}{R_{11}} \right) (2)$$

$$\frac{R_{13}}{R_{11}} = 0.75$$

To have a margin of 150 mV from the rails, chosen values are $R_{13} = 7.5 \text{ k}\Omega$ and $R_{11} = 10 \text{ k}\Omega$; The simulation result with the output of this differential amplifier is shown in [Figure 10](#).

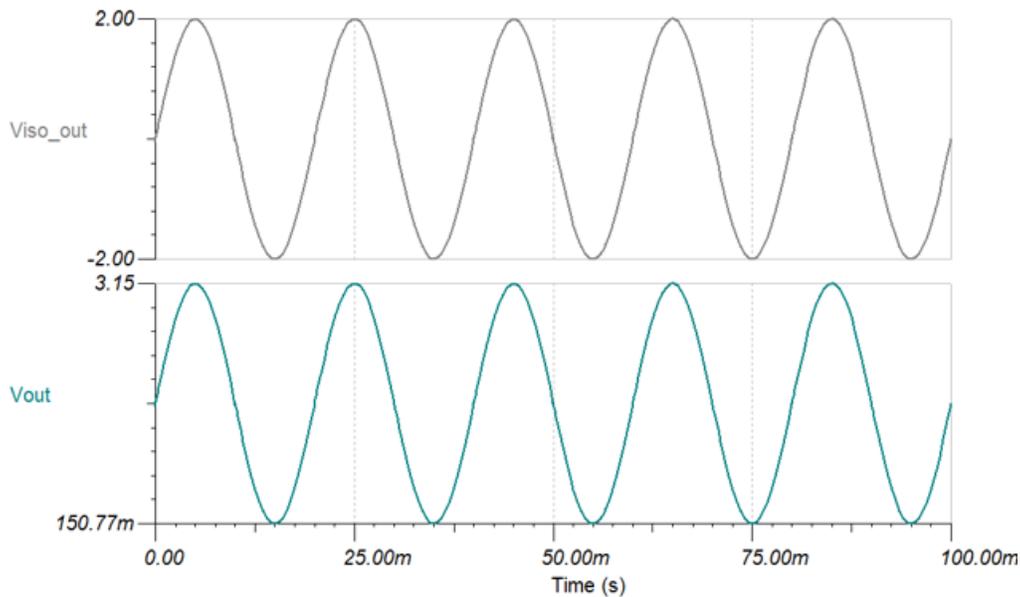


Figure 10. Simulation Result for Differential to Single-Ended Converter

Here, V_{ISO_OUT} is the output of the AMC1200 as depicted in [Figure 10](#), and V_{OUT} is the final output of level shifter. The schematic of the level shifter is shown in [Figure 11](#).

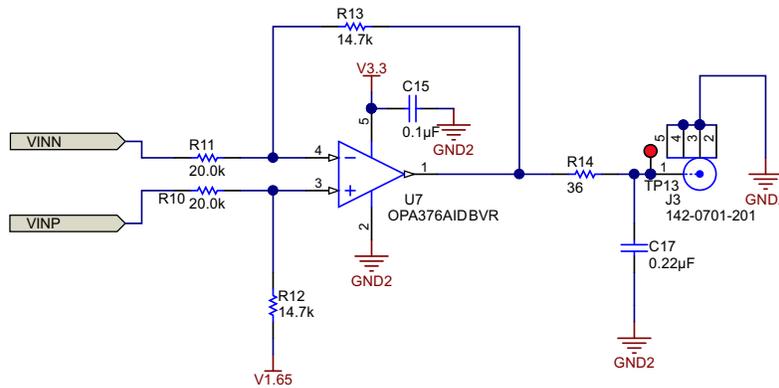


Figure 11. Differential Amplifier Stage

To compare the overall performance and linearity of the circuit, the transfer function is plotted for input current versus output of every stage separately as shown in Figure 12.

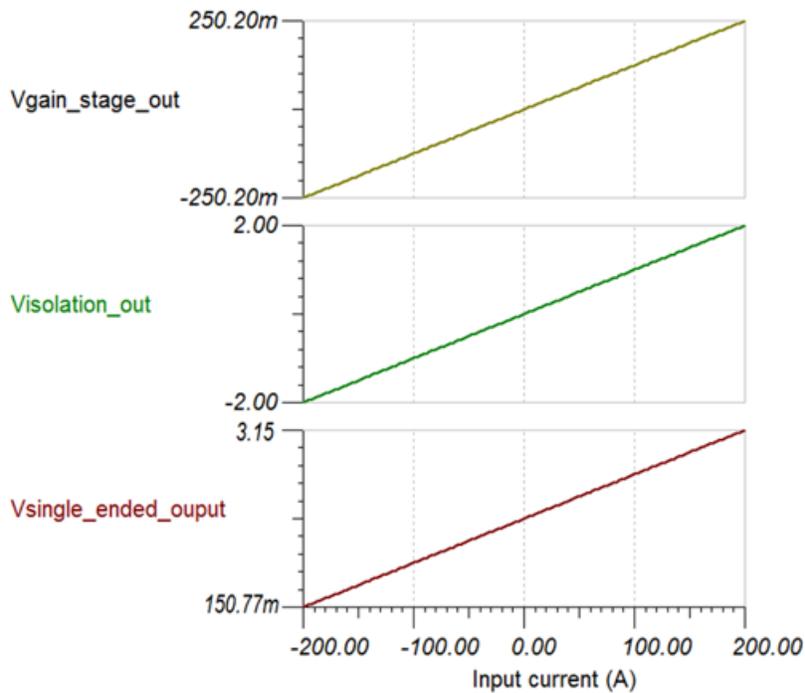


Figure 12. Transfer Function Plotted Using TINA

4.4 Power Supply and Reference Solution

4.4.1 Isolated Power Supply

The AMC1200 requires an isolated power supply for powering its input section. The SN6501 is used as a switching device to generate a 5-V isolated output and drives transformer.

The SN6501 is a monolithic oscillator and power-driver, specifically designed for isolated power supplies in isolated interface applications with a small form factor. It drives a low-profile, center-tapped transformer primary from a 3.3- or 5-V DC power supply. The SN6501 consists of an oscillator followed by a gate drive circuit that provides the complementary output signals to drive the ground referenced N-channel power switches. The internal logic ensures break-before-make action between the two switches.

The SN6501 features:

- Push-pull driver for small transformers
- Single 3.3- or 5-V supply

While selecting the transformer, it is important to prevent transformer from saturation. To achieve this, the transformer's V-t product must be greater than the maximum V-t product applied by the SN6501. The maximum voltage delivered by the SN6501 is the nominal converter input plus 10%. The maximum time this voltage is applied to the primary is half the period of the lowest frequency at the specified input voltage. Therefore, the transformer's minimum V-t product is determined through:

$$V_{T(\min)} \geq V_{IN(\max)} \times \frac{T(\max)}{2} = \frac{V_{IN(\max)}}{2 \times f(\min)} \quad (8)$$

$$V_{T(\min)} \geq \frac{5.5 \text{ V}}{2 \times 300 \text{ kHz}} = 9.1 \text{ V}\mu\text{s}$$

Common V-t values for low-power center-tapped transformers range from 22 to 150 Vμs with typical footprints of 10 × 12 mm.

This design needs to sense bipolar signal using a unipolar power supply. The front-end amplifier should be able to take negative as well as positive inputs. Thus it is necessary to power it using a dual supply. Therefore, after rectifying the output of the transformer, we have to split it to get ±2.5 V. This is achieved using zener diodes as seen in Figure 13.

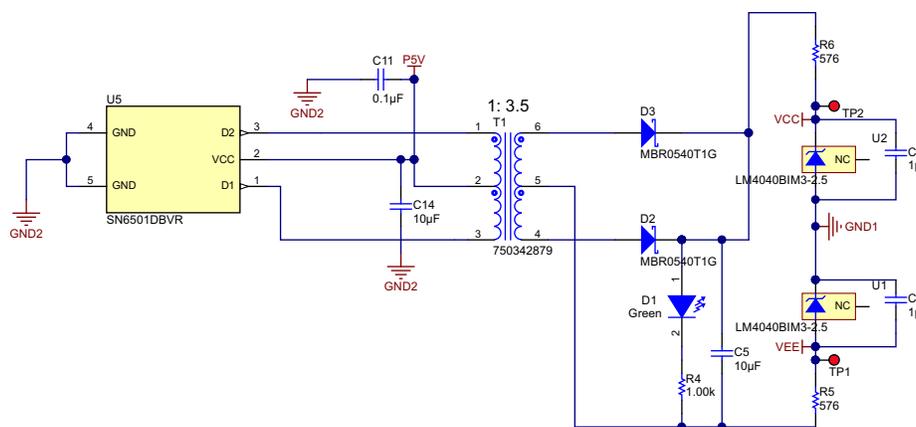


Figure 13. Isolated Power Supply

V_{CC} and V_{EE} as shown in Figure 13 are used to power the first gain stage as well as the high-voltage side of isolation amplifier. The turn's ratio of chosen transformer is 1:3.5. Thus, for a 5-V primary input voltage, the secondary voltage is 17.5 V. After accounting for the forward voltage drop of the diodes, the voltage available after rectification is around 16.5 V.

The maximum output current required from this supply is less than 10 mA, and the minimum current required by the Zener to stay in regulation is only 45 μ A. Voltage across the resistor in series with Zener is:

$$V_{\text{RES}} = \frac{16.5}{2} - 2.5 = 5.75 \text{ V} \quad (9)$$

For a current of 10 mA, the required resistor value is $R = \frac{5.75 \text{ V}}{10 \text{ mA}} = 575 \Omega$

4.4.2 Reference Solution

In this application, a bipolar signal has to be sensed using a unipolar power supply. To achieve this, it is required to level shift the output of the signal conditioning stage to the midpoint of the power supply rail. A voltage reference is required to bias the signal conditioning stage output to the middle of the ADC dynamic range. The REF2033 IC provides both the 3.3-V supply to the OPA317 as well as the 1.65-V reference voltage for biasing the signal to the middle of the ADC range. Both the outputs of the REF2033 IC can sink or source 20 mA. Also, there is excellent tracking between the 3.3-V and 1.65-V supplies, and both the supplies are available in a single, extremely small SOT23-5 package, thus reducing BOM count and board size. This power supply section is shown in Figure 14.

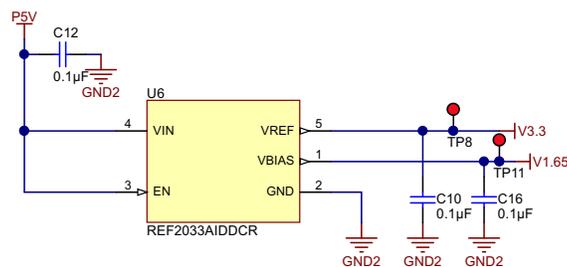


Figure 14. Power Supply and Reference Circuit

The IC is supplied with a 5-V power supply. The outputs are 3.3 V and 1.65 V. Place 0.1- μ F noise decoupling capacitors close to the IC pins for clean power input and output rails.

5 Test Setup

Tests were conducted with DC input voltage, AC input voltage, and current input. The frequency of AC input used for conducting the tests was 50 Hz. The values of voltages were measured after every stage using a 6½ digit multimeter from Agilent with the aid of averaging functionality. The test setup for DC test is shown in [Figure 15](#).

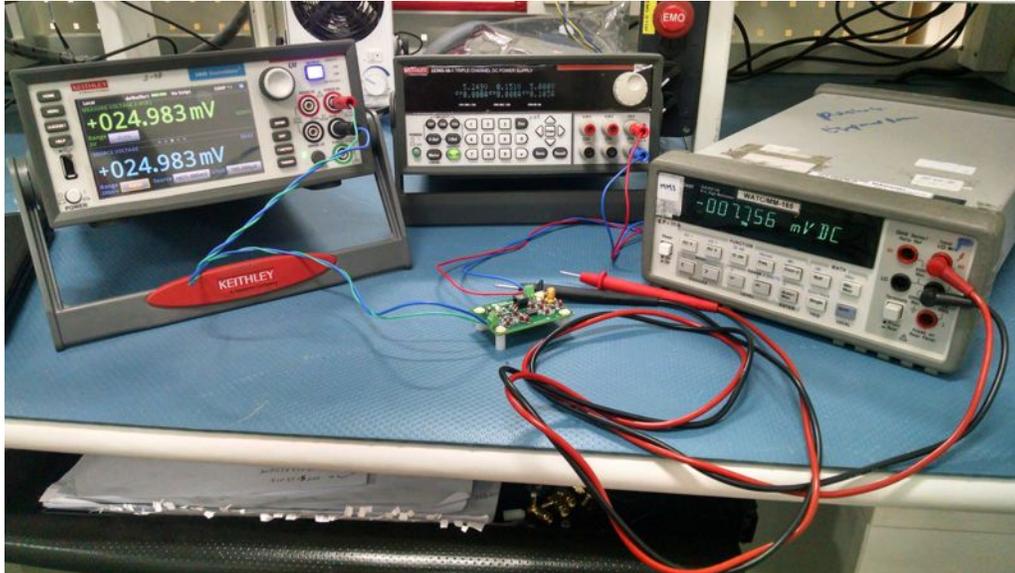


Figure 15. Test Setup for DC Input

The DC input voltage was supplied by a Keithley 2450 source meter. Accuracy of the design was calculated for every 1 mV in the input voltage over a range of -15 to 25 mV.

A similar test was conducted with AC input voltage and current wherein the design was tested for input ranging from 1 to 17 mV_{RMS} with 1-mV steps.

For testing the design over temperature range of -25°C to 85°C , the board was kept inside the temperature chamber and similar tests were conducted. [Figure 16](#) depicts the setup for testing across the temperature range of -25°C to 85°C .

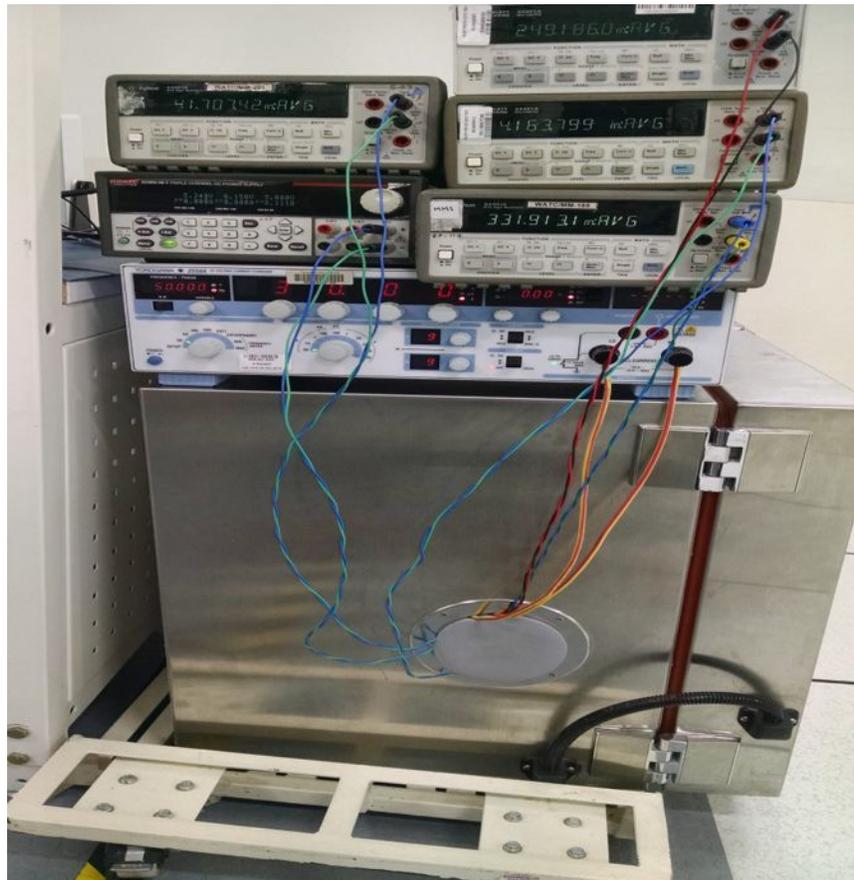


Figure 16. Test Setup for Testing Across Temperature Range

6 Test Data

The following test results are provided in following sections.

6.1 Power Supply

Figure 17 shows $\pm 2.5\text{-V}$ isolated power supplies generated on board to bias the front-end gain stage and high-voltage side of the AMC1200.

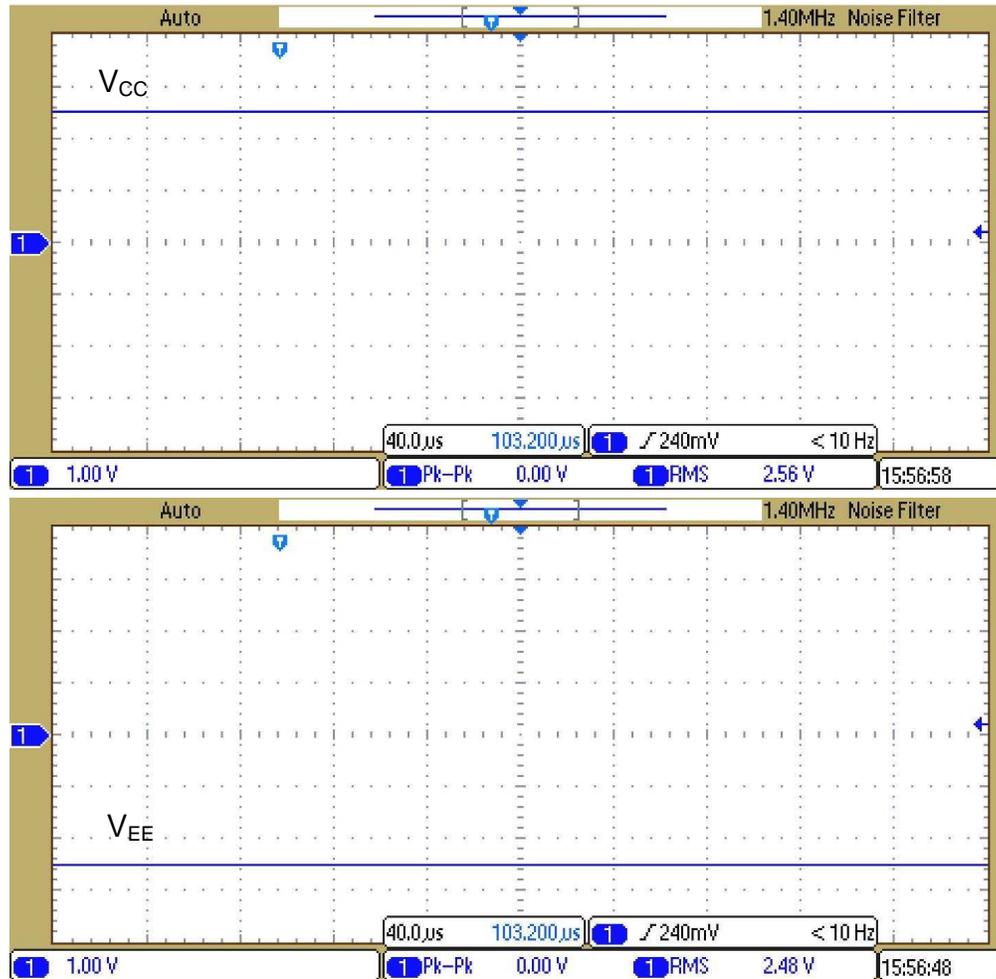


Figure 17. $\pm 2.5\text{-V}$ Supply

Figure 18 shows the 3.3-V supply powering the low-voltage side of the AMC1200 and level shifter and the 1.65-V built-in reference to level shift the output.

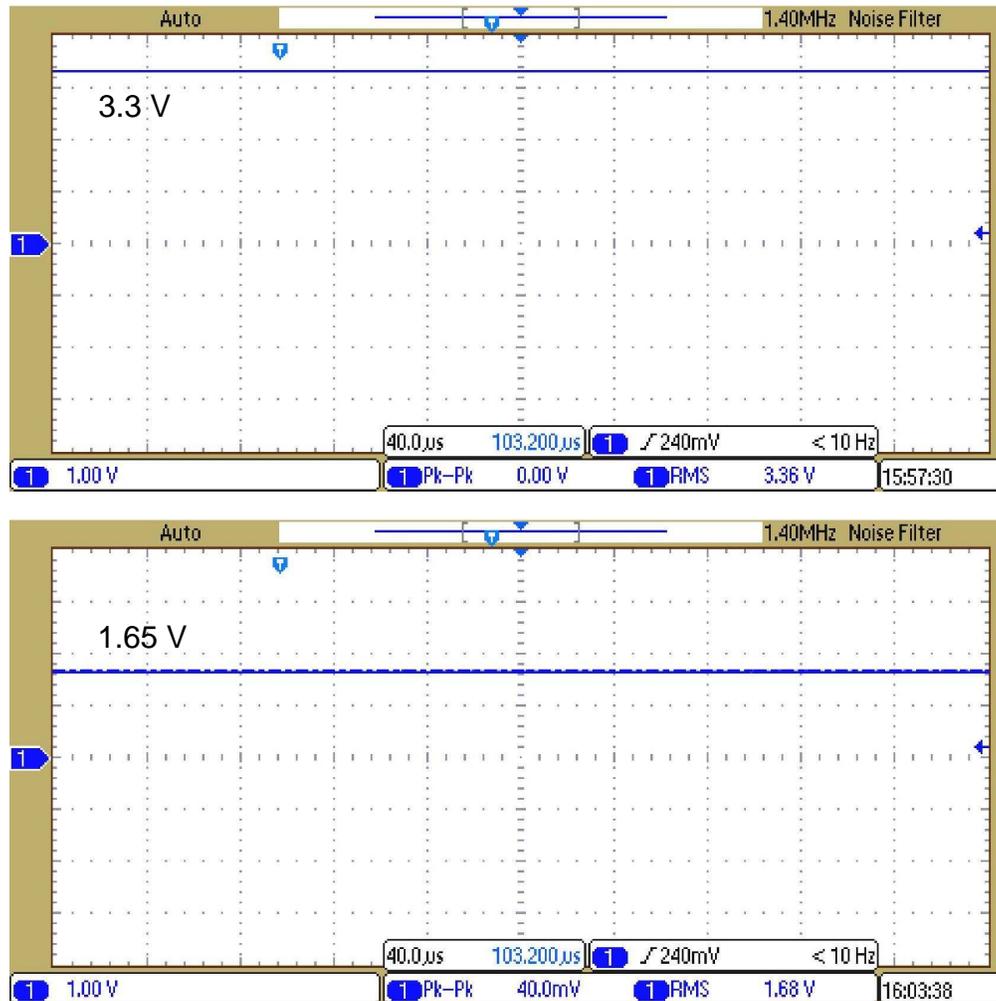


Figure 18. 3.3-V Supply and 1.65-V Reference Voltage

6.2 Accuracy Result

This section provides all the accuracy graphs obtained for this design.

Figure 19 shows the accuracy for DC input voltage to the board (simulating shunt voltage) across the temperature range. The 25-mV input corresponds to the 200-A DC current.

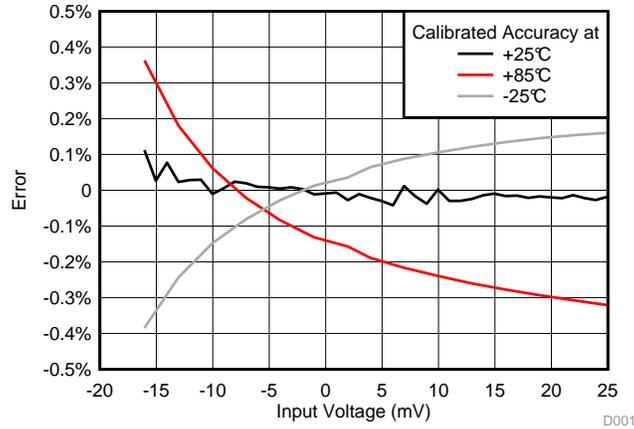


Figure 19. Accuracy of DC Input Voltage Across Temperature Range

Figure 20 shows the accuracy for AC voltage input voltage to the board across the temperature range where the frequency for the input is 50 Hz. The 17-mV input corresponds to the 136-A_{RMS} current.

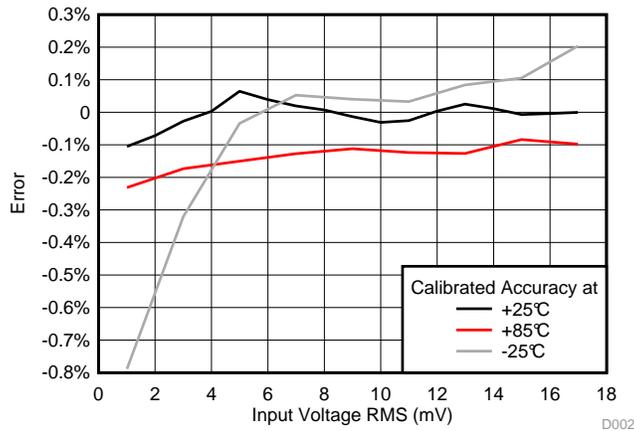


Figure 20. Accuracy of AC Input Voltage Across Temperature Range

Figure 21 shows the accuracy for AC current input wherein the current was passed through the shunt resistor of 125 $\mu\Omega$ and the voltage drop across shunt was fed to the board as an input voltage.

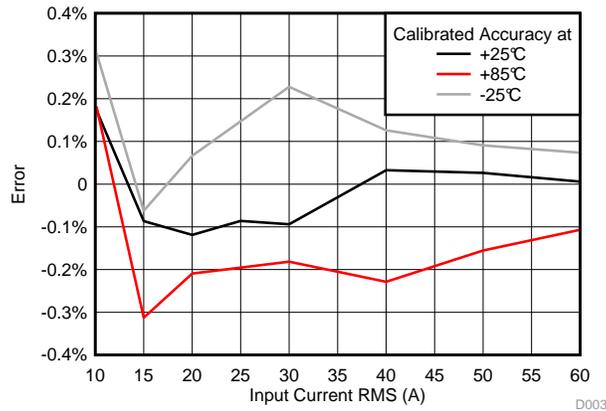


Figure 21. Accuracy of AC Current Input Across Temperature Range

The following figures provide a deeper analysis wherein the behavior of all the stages is shown separately for various tests conducted at 25°C. Figure 22 shows the behavior of the individual stages for the DC input voltage. Figure 23 and Figure 24 show the behavior for AC voltage input and AC current input flowing through the shunt, respectively.

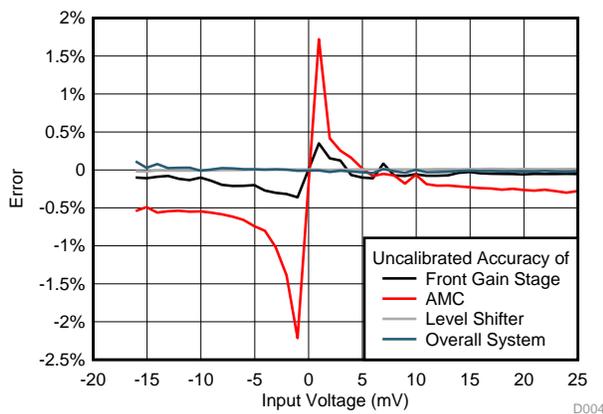


Figure 22. Accuracy of System at 25°C (DC Input Voltage)

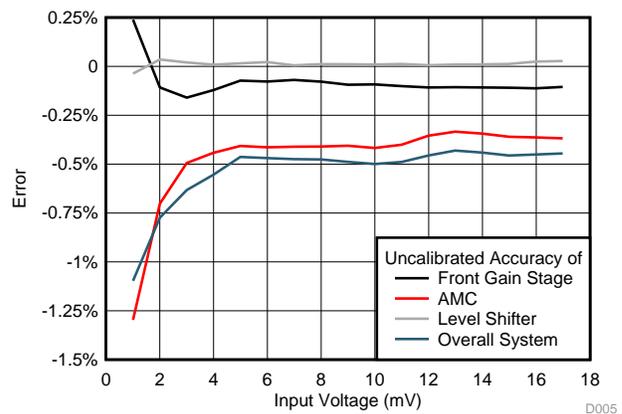


Figure 23. Accuracy of System at 25°C (AC_{RMS} Input Voltage)

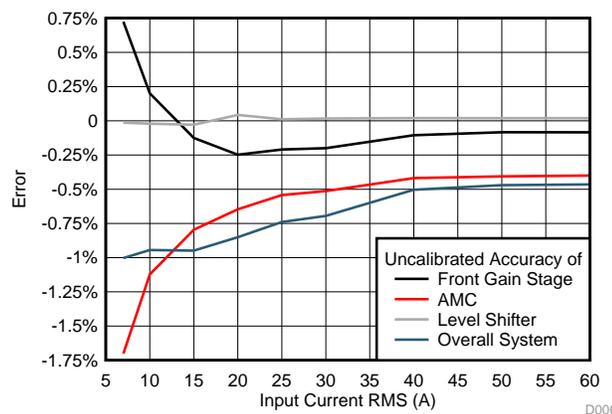


Figure 24. Accuracy of System at 25°C (AC Current Input)

6.3 Time Response

This section shows the response of the design to a step input of 25 mV. Figure 25 shows the total rise time of the input and corresponding rise time of the output.

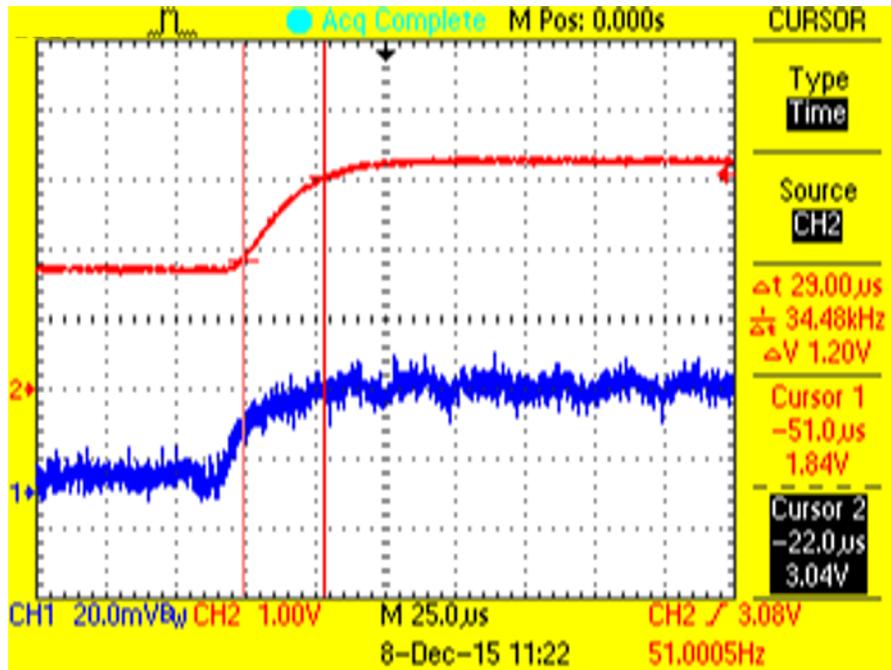


Figure 25. Rise Time of Input (CH1) and Output (CH2)

The measured rise time of the step input is 16.76 µs and the corresponding rise time of output is 29 µs. Figure 26 shows the rise time of only the AMC1200 when a step input of 250 mV is fed to it.

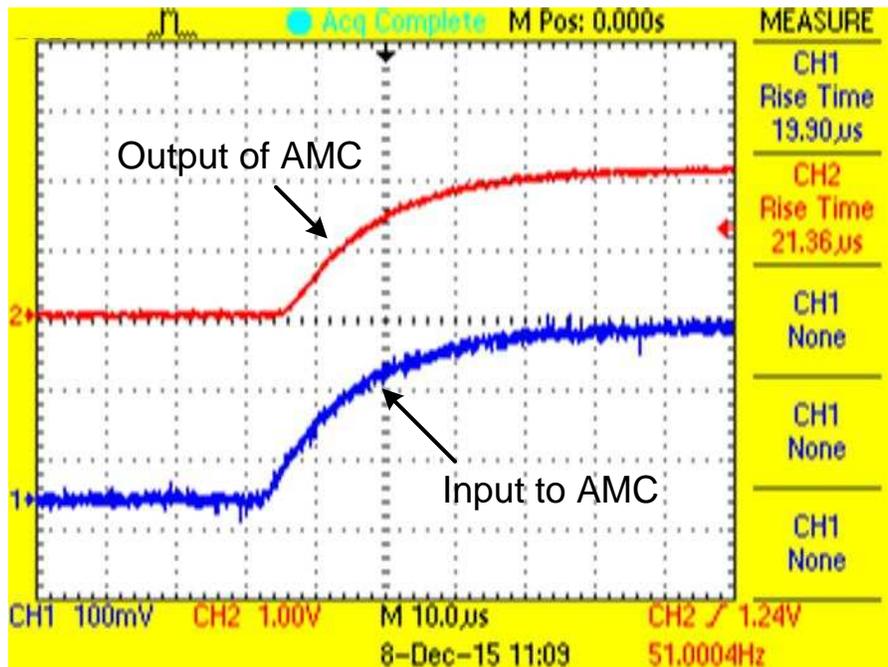


Figure 26. Rise Time of AMC1200

The rise time of the input to the AMC1200 is 19.90 μs , and the corresponding rise time of the AMC1200 is 21.36 μs . Figure 27 and Figure 28 show the propagation delay of the AMC1200 and the entire board, respectively.

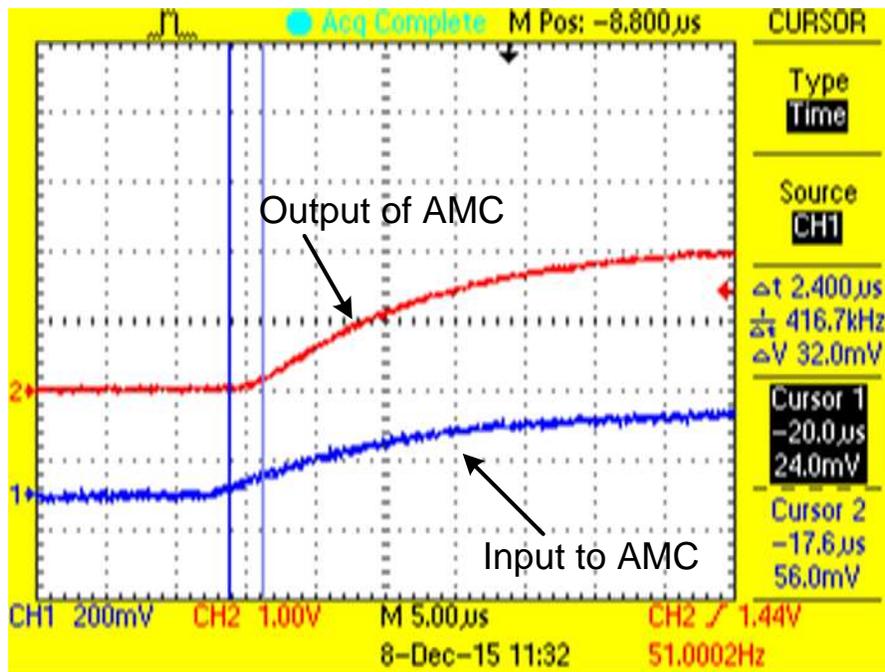


Figure 27. Propagation Delay of AMC1200

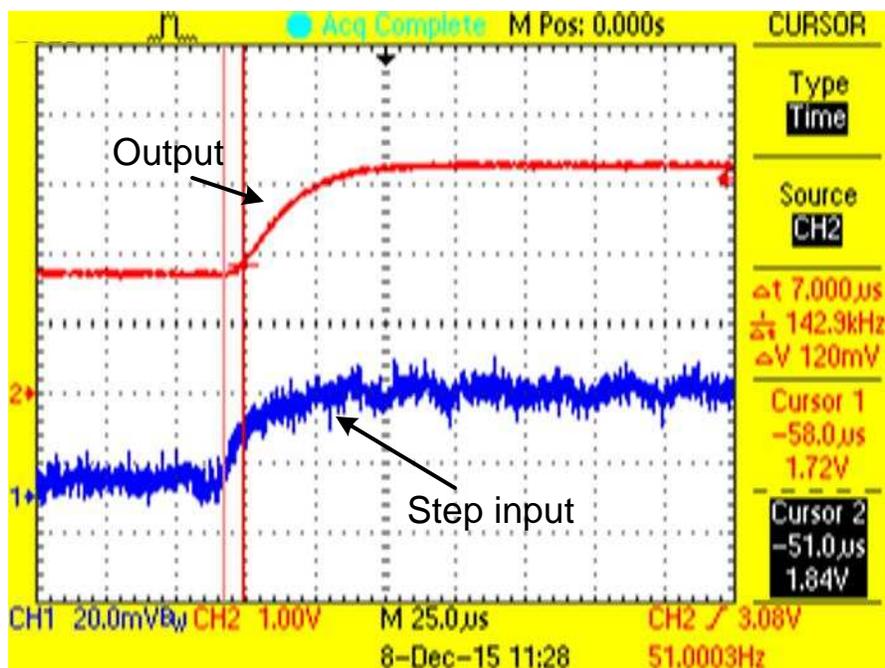


Figure 28. Propagation Delay of the Board

As seen in these waveforms, the measured propagation delay of the AMC1200 is 2.4 μs and the board is 7 μs .

7 Design Files

7.1 Schematics

To download the schematics, see the design files at [TIDA-00445](http://www.ti.com/.../TIDA-00445).

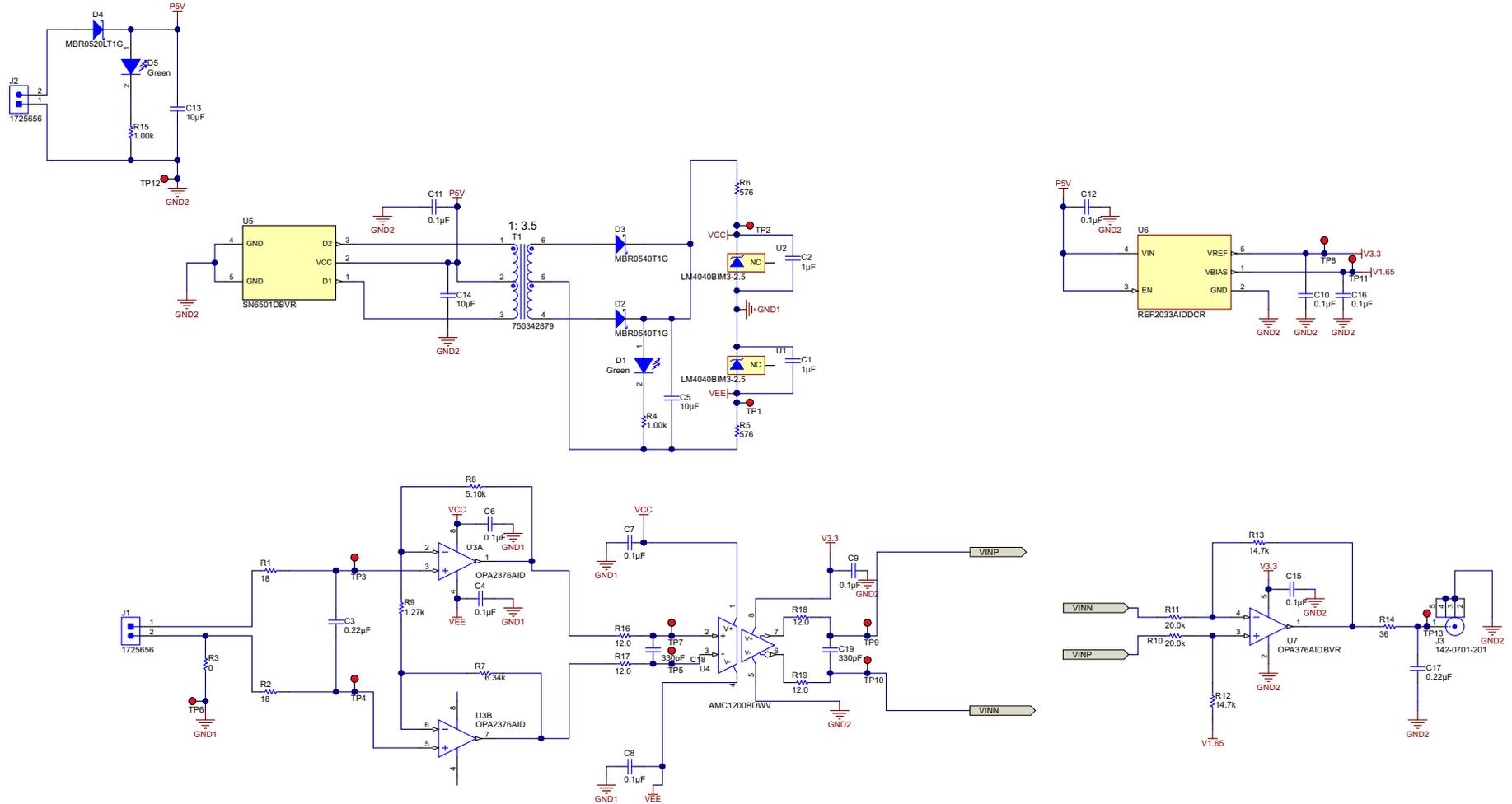


Figure 29. TIDA-00445 Schematic

7.2 Bill of Materials

To download the bill of materials (BOM), see the design files at [TIDA-00445](#).

7.3 PCB Layout Recommendations

- No copper between isolation with a minimum width of 9 mm (as represented by the arrows in [Figure 30](#)).

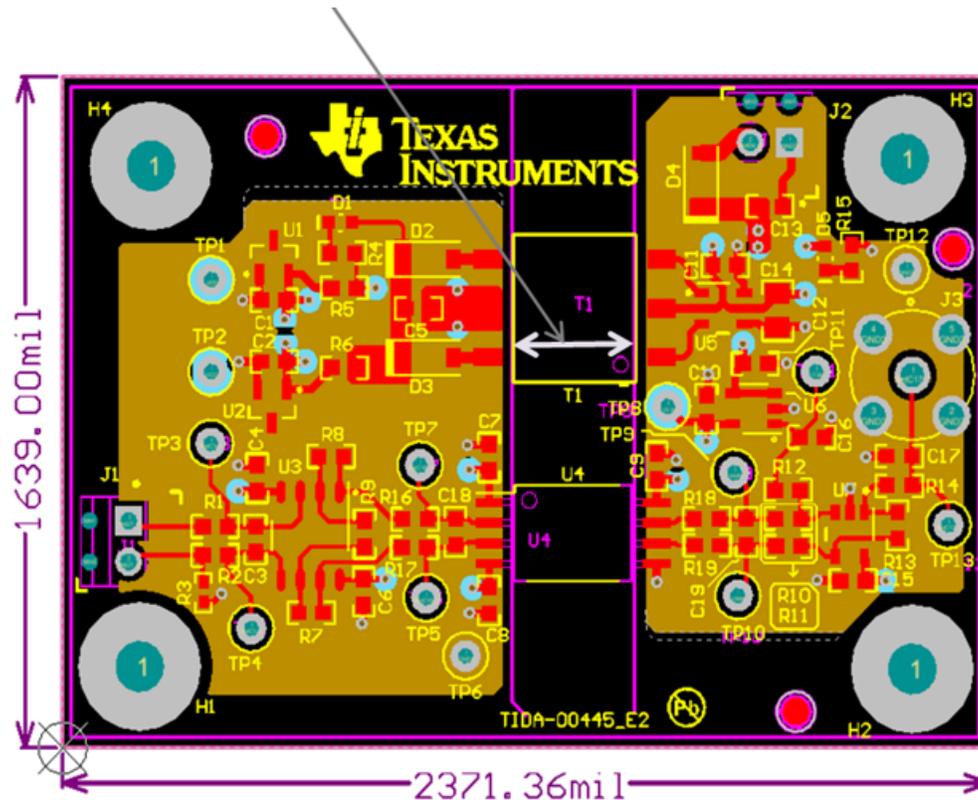


Figure 30. PCB Layout Showing Isolation Between High- and Low-Voltage Side of AMC1200

- Do not place any test points near the transformer to avoid noise pick up.
- Place decoupling capacitors very close to their corresponding pins with a low impedance path to the device GND.

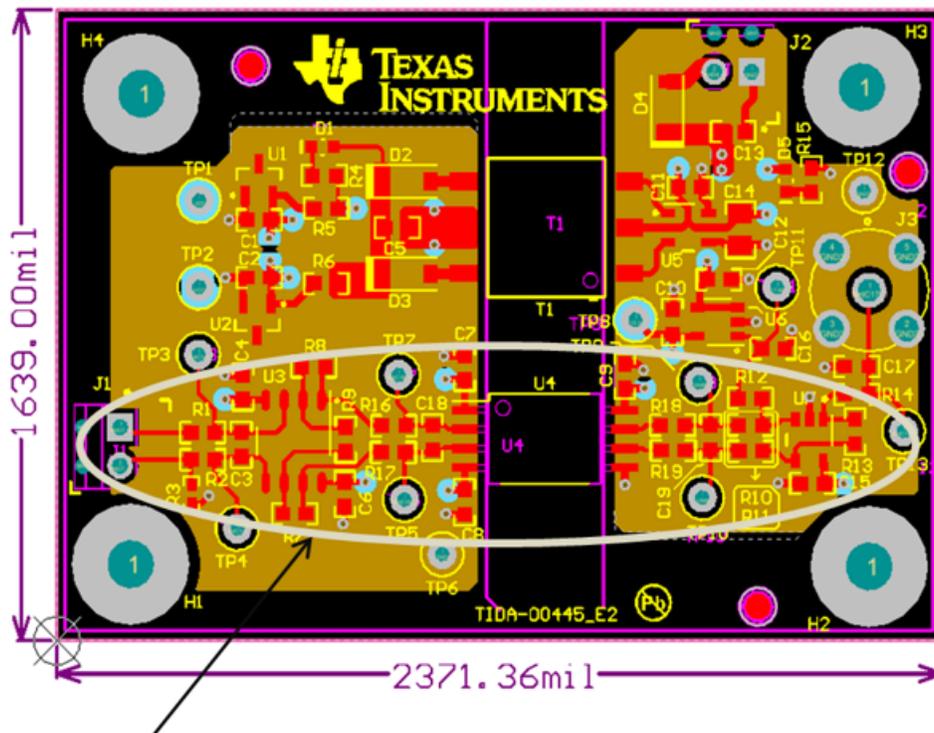


Figure 31. PCB Layout Representing Signal Chain

- Keep trace length from the input to signal chain equal and make sure the entire signal chain is in one straight line (as represented in [Figure 31](#)).
- Place input resistors very close to their corresponding pins. Traces for output resistors can be a little longer if required.
- Make sure to have non-plated mounting if any are between isolated regions.

7.3.1 Layout Prints

To download the layout prints, see the design files at [TIDA-00445](#).

7.4 Altium Project

To download the Altium project files, see the design files at [TIDA-00445](#).

7.5 Gerber Files

To download the Gerber files, see the design files at [TIDA-00445](#).

7.6 Assembly Drawings

To download the assembly drawings, see the design files at [TIDA-00445](#).

8 About the Authors

N. NAVANEETH KUMAR is a Systems Architect at Texas Instruments, where he is responsible for developing subsystem solutions for motor controls within Industrial Systems. N. Navaneeth brings to this role his extensive experience in power electronics, EMC, analog, and mixed signal designs. He has system-level product design experience in drives, solar inverters, UPS, and protection relays. N. Navaneeth earned his bachelor of electronics and communication engineering from Bharathiar University, India and his master of science in electronic product development from Bolton University, UK.

NEHA NAIN is a Systems Engineer at Texas Instruments, where she is responsible for developing subsystem reference design solutions for Industrial equipment. Neha earned her bachelor of electrical and electronics engineering from PES Institute of Technology (now PES University), Bangalore.

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (December 2015) to A Revision	Page
• Changed from preview page.....	1

IMPORTANT NOTICE FOR TI REFERENCE DESIGNS

Texas Instruments Incorporated ("TI") reference designs are solely intended to assist designers ("Buyers") who are developing systems that incorporate TI semiconductor products (also referred to herein as "components"). Buyer understands and agrees that Buyer remains responsible for using its independent analysis, evaluation and judgment in designing Buyer's systems and products.

TI reference designs have been created using standard laboratory conditions and engineering practices. **TI has not conducted any testing other than that specifically described in the published documentation for a particular reference design.** TI may make corrections, enhancements, improvements and other changes to its reference designs.

Buyers are authorized to use TI reference designs with the TI component(s) identified in each particular reference design and to modify the reference design in the development of their end products. HOWEVER, NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY THIRD PARTY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT, IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI REFERENCE DESIGNS ARE PROVIDED "AS IS". TI MAKES NO WARRANTIES OR REPRESENTATIONS WITH REGARD TO THE REFERENCE DESIGNS OR USE OF THE REFERENCE DESIGNS, EXPRESS, IMPLIED OR STATUTORY, INCLUDING ACCURACY OR COMPLETENESS. TI DISCLAIMS ANY WARRANTY OF TITLE AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, QUIET ENJOYMENT, QUIET POSSESSION, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS WITH REGARD TO TI REFERENCE DESIGNS OR USE THEREOF. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY BUYERS AGAINST ANY THIRD PARTY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON A COMBINATION OF COMPONENTS PROVIDED IN A TI REFERENCE DESIGN. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, SPECIAL, INCIDENTAL, CONSEQUENTIAL OR INDIRECT DAMAGES, HOWEVER CAUSED, ON ANY THEORY OF LIABILITY AND WHETHER OR NOT TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES, ARISING IN ANY WAY OUT OF TI REFERENCE DESIGNS OR BUYER'S USE OF TI REFERENCE DESIGNS.

TI reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques for TI components are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

Reproduction of significant portions of TI information in TI data books, data sheets or reference designs is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards that anticipate dangerous failures, monitor failures and their consequences, lessen the likelihood of dangerous failures and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in Buyer's safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed an agreement specifically governing such use.

Only those TI components that TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components that have **not** been so designated is solely at Buyer's risk, and Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.