

TI Designs

Optimized Radar System Design Using 66AK2L06 DSP+ARM[®] SoC and ADC14X250



TI Designs

TI Designs provide the foundation that you need including methodology, testing and design files to quickly evaluate and customize the system. TI Designs help *you* accelerate your time to market.

Design Resources

TIDEP0060	Tool Folder Containing Design Files
66AK2L06	Product Folder
ADC14X250	Product Folder
DAC38J84	Product Folder



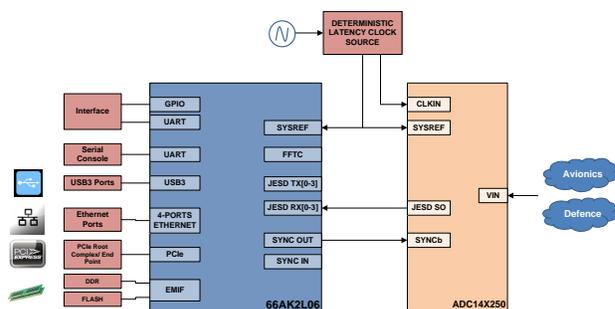
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Design Features

- Easy Integration of Signal Processor to Data Converters Over JESD204B
- DFE Processing for Filtering, Down-Sampling, or Up-Sampling
- FFT Hardware Accelerator for Low-Latency, High-Performance Radar System Design
- System Optimized for Avionics and Defense Applications
- JESD204B Attached Signal Processing Solution Including DSP, and ADC Boards, Demo Software, Configuration GUIs, and Getting Started Guide
- A Robust Demonstration and Development Platform Including Three EVMs, a Deterministic Latency Card, Schematic, BOM, User Guide, Benchmarks, Software, and Demos

Featured Applications

- Air-Borne and Space-Borne Synthetic Aperture Radar (SAR)



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 Linux is a registered trademark of Linus Torvalds.
 All other trademarks are the property of their respective owners.

1 General Texas Instruments High Voltage Evaluation (TI HV EVM) User Safety Guidelines



Figure 1. Warning

Always follow TI's setup and application instructions, including use of all interface components within their recommended electrical rated voltage and power limits. Always use electrical safety precautions to help ensure your personal safety and those working around you. Contact TI's Product Information Center at <http://www.ti.com/general/docs/dsnsuprt.tsp> for further information.

Save all warnings and instructions for future reference.

Failure to follow warnings and instructions may result in personal injury, property damage, or death due to electrical shock and burn hazards.

The term TI HV EVM refers to an electronic device typically provided as an open framed, unenclosed printed circuit board assembly. It is **intended strictly for use in development laboratory environments, solely for qualified professional users having training, expertise and knowledge of electrical safety risks in development and application of high voltage electrical circuits. Any other use or application are strictly prohibited by TI.** If you are not suitable qualified, you should immediately stop from further use of the HV EVM

1. Work Safety Area

- Keep work area clean and orderly.
- Qualified observer(s) must be present anytime circuits are energized.
- Effective barriers and signage must be present in the area where the TI HV EVM and its interface electronics are energized, indicating operation of accessible high voltages may be present, for the purpose of protecting inadvertent access.
- All interface circuits, power supplies, evaluation modules, instruments, meters, scopes and other related apparatus used in a development environment exceeding 50 Vrms/75 VDC must be electrically located within a protected Emergency Power Off EPO protected power strip.
- Use a stable and non-conductive workspace.
- Use adequately insulated clamps and wires to attach measurement probes and instruments. No freehand testing whenever possible.

2. Electrical Safety

As a precautionary measure, it is always a good engineering practice to assume that the entire EVM may have fully accessible and active high voltages.

- De-energize the TI HV EVM and all its inputs, outputs and electrical loads before performing any electrical or other diagnostic measurements. Re-validate that TI HV EVM power has been safely de-energized.
- With the EVM confirmed de-energized, proceed with required electrical circuit configurations, wiring, measurement equipment connection, and other application needs, while still assuming the EVM circuit and measuring instruments are electrically live.
- After EVM readiness is complete, energize the EVM as intended.

WARNING: While the EVM is energized, never touch the EVM or its electrical circuits as they may be at high voltages capable of causing an electrical shock hazard.

3. Personal Safety

- Wear personal protective equipment (for example, latex gloves or safety glasses with side shields) or protect the EVM in an adequate lucent plastic box with interlocks to protect from accidental touch.

Limited for safe use:

EVMs are not to be used as all or part of a production unit.

2 System Description

The *Optimized Radar System Design Using 66AK2L06 DSP+ARM® SoC and ADC14X250* demonstrates performance of the high-speed JESD204B connectivity between the 66AK2L06 System-on-Chip (SoC) with industry-leading high-speed data converters. This design also demonstrates the signal processing power of 66AK2L06 hardware co-processors, DSP CorePacs, and control processing power using ARM® CorePacs. A high-level hardware block diagram shown in [Figure 2](#) explains high-level connectivity of the 66AK2L06 device with the ADC14X250 for different applications. The analog input comes from an ADC that best matches the requirements of each industry application. The analog input is sampled, digitized, and sent to the 66AK2L06 device over a JESD204B interface. The 66AK2L06 processes the received data using its internal hardware co-processors and sends the data out through any of the available interfaces including JESD204B, Ethernet, or PCIe.

The *Optimized Radar System Design Using 66AK2L06 DSP+ARM SoC and ADC14X250* is well suited for applications such as:

- High-speed data acquisition and generation
- Electronic warfare and communications: Military radar, civilian radar, synthetic-aperture radar (SAR), signals Intelligence (SIGINT/ELINT), countermeasure
- Missiles and ground defense: Missile guidance and control systems, missile compute platforms, monitoring systems
- Military aircraft and general aviation: Unmanned systems, munitions, surveillance or mobility aircraft

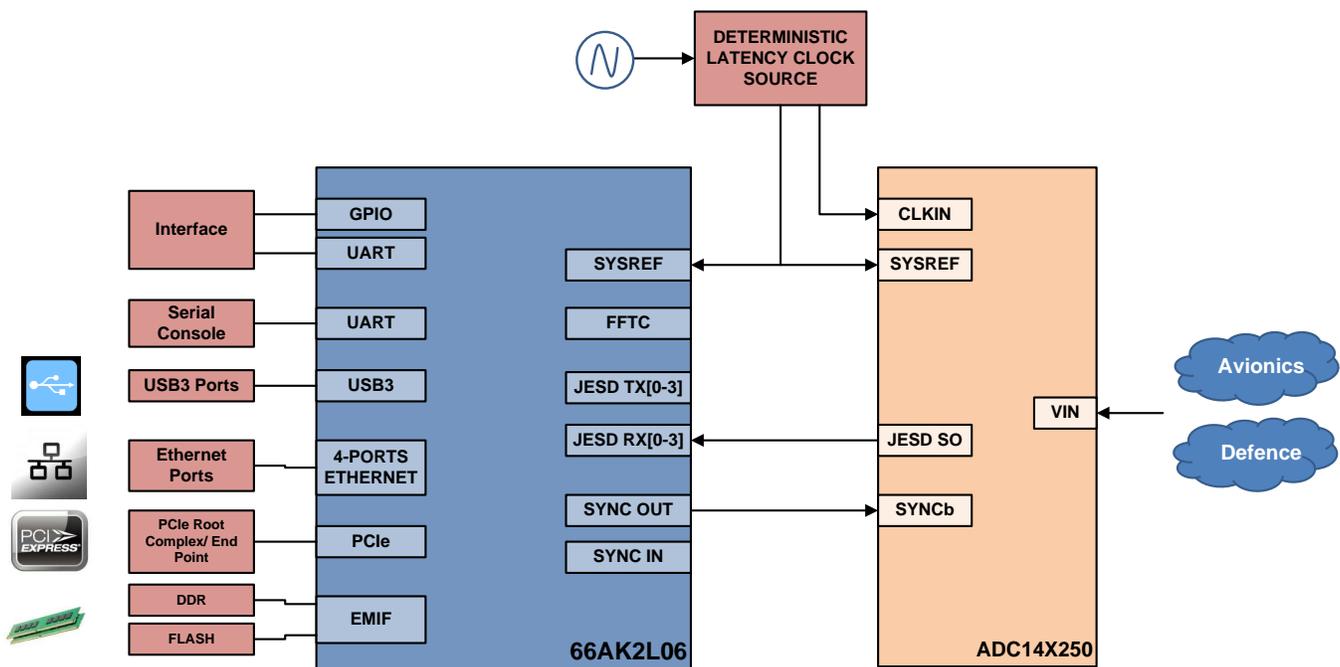


Figure 2. System Block Diagram

3 Highlighted Products

3.1 66AK2L06

The 66AK2L06 is a member of the C66x family based on TI's new Keystone™ II Multicore SoC architecture. The SoC is a lower power, smaller size, and lower-cost solution with eight integrated lanes of the JESD204B interface to meet the requirements of avionics and defense. The FFTC hardware accelerator allows compute-intensive 2D FFT operations to be offloaded. The device's ARM and DSP cores deliver exceptional processing power for platforms needing high signal and control processing. The Keystone II architecture provides a programmable platform integrating various subsystems (ARM CorePacs, C66x CorePacs, DFE, FFTC, 4-Port Ethernet Switch, and so on) and uses a queue-based

communication system that allows the SoC resources to operate efficiently and seamlessly. This unique SoC architecture also includes a TeraNet switch that enables a wide mix of system elements, from programmable cores to dedicated co-processors and high-speed I/O, to allow each of them to operate at maximum efficiency with no blocking and stalling. The 66AK2L06 SoC is part of TI's scalable multicore SoC architecture solution that provides developers with a range of software-compatible and hardware-compatible devices to minimize development time and maximize reuse across all applications.

Some key features that enable the 66AK2L06 SoC to be used in the avionics and defense applications such as synthetic aperture radar, phased array radar, weather radar, electronic warfare, surveillance and software defined radio.

- Seamless connectivity with JESD204B compliant data converters (ADCs/DACs).
- Four TX and four RX JESD204B lanes each supporting up to 7.37 Gbps.
- Integrated digital front end (DFE) for I/Q mapping, digital up/down conversion, FIR filtering and decimation.
- Two FFT coprocessors to accelerate the FFT and iFFT computations, meeting stringent latency requirements.
- Four C66x DSP cores to perform real-time signal processing tasks and two ARM Cortex A15 cores to perform housekeeping and management tasks.

See the 66AK2L06 product page for additional information on the 66AK2L06 family at 66AK2L06. For more information see [Figure 3](#), which shows the 66AK2L06 block diagram.

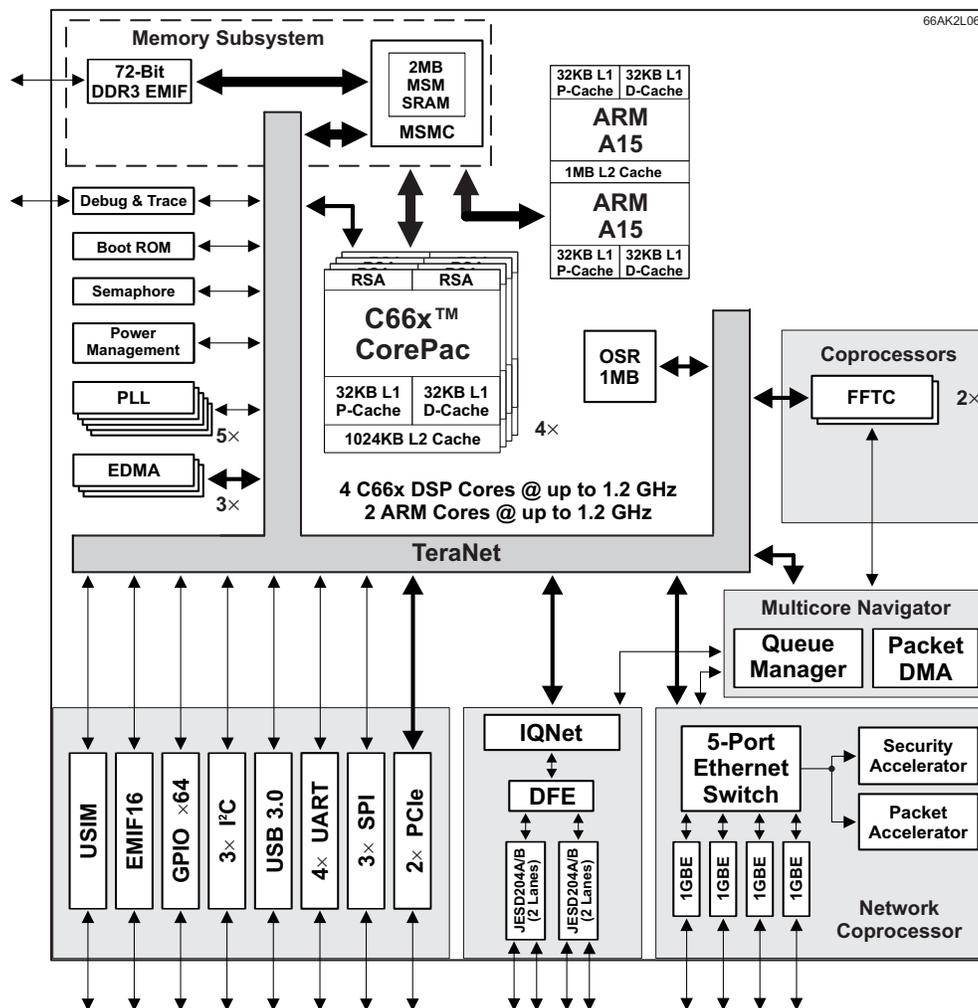


Figure 3. 66AK2L06 Block Diagram

3.2 **ADC14X250**

The ADC14X250 device is a monolithic single-channel high performance analog-to-digital converter, capable of converting analog input signals into 14-bit digital words with a sampling rate of 250 Msps. This converter uses a differential pipelined architecture with integrated input buffer to provide excellent dynamic performance while maintaining low power consumption. The device uses JESD204B subclass 1 interface for providing output digital data.

Refer to the [ADC14X250 product page](#) for additional information.

4 System Design Theory

A wideband demonstration of the *Optimized Radar System Design Using 66AK2L06 DSP+ARM SoC and ADC14X250* is available to evaluate the sampling of a single 100-MHz channel. The following sections provide details of the data flow and processing path.

4.1 Input Data Stream

The pre-defined input data stream is stored in the DDR memory. Two options of the pre-defined input data stream are available:

- A single dual-tone different amplitude data sampled at 122.88 Msps.
- 200 single tones spread across 100-MHz of bandwidth.

4.2 ADC14X250 Sending Data Over the JESD204B to the 66AK2L06

The ADC14X250 samples the analog input signal with sampling frequency (CLKIN) of 245.76 MHz. The sampled data is sent to JESD block inside the ADC which sends data out. The JESD module is configured as explained in [Section 4.3](#). The 66AK2L06 JESD module receives this data over Rx Lane 0. The 66AK2L06 JESD is configured for L=2 with Lane1 disabled so that the Q path is really zero. This parallel IQ data at 245.76Msps is sent to the Rx sub-block inside the DFE module. The Rx sub-block converts the real data to complex data. Later the data is filtered, frequency translated and then decimated by 2. The DDUC modules filters the incoming stream and provides output at 122.88 Msps to baseband module, which provides gain and transfers data to IQNet. The PktDMA stores the data in DDR memory. This data is picked up by FFTC co-processor to perform a 4096 point FFT, and the output data is stored to DDR memory. [Figure 4](#) shows the data flow–receive.

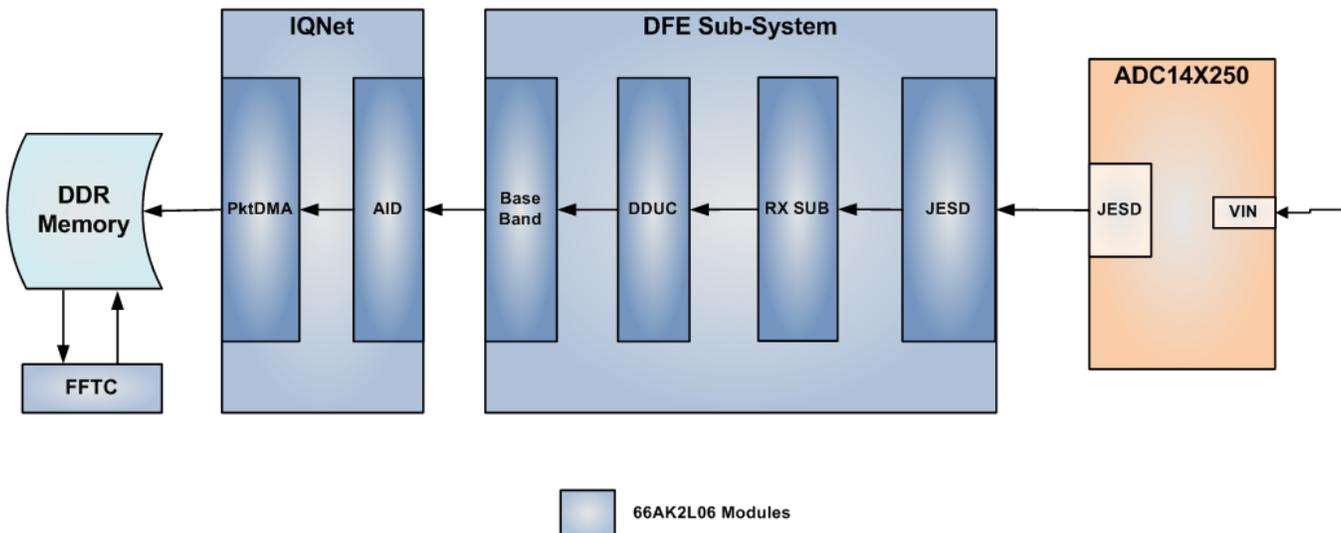


Figure 4. Data Flow–Receive

4.3 JESD204 B Capabilities and Configurations

The JESD204B module is capable of:

- Four transmit lanes with up to 7.37 Gbps each.
- Four receive lanes with up to 7.37 Gbps each.
- Alignment across multiple lanes within a single converter or multiple converters in the same device.
- Support for subclass 0 and 1.

In the demo application, the 66AK2L06 communicates with ADC14X250 over one lane operating at a link rate of 4.915 Gbps. ADC14X250 only supports JESD subclass 1. Data scrambling is supported on the 66AK2L06 as well as ADC14X250. For this application, scrambling is disabled. [Table 1](#) lists the JESD link parameters configuration.

Table 1. JESD Link Parameters

JESD PARAMETER	66AK2L06 CAPABILITY	PARAMETERS USED IN DEMONSTRATION
		ADC14X250 66AK2L06
M–(Number of converters per device)	Depends on the converter's capability. With a 4 Tx and 4 Rx lanes and bit rate requirement, a maximum of 4 converters may be supported in the Tx direction, and 4 converters in the Rx direction.	1
N–(Resolution of converters)	Depends on the converter's capability.	14
N'–(JESD word size)	Depends on the converter's capability.	16
L–(No. of lanes)	Total of 8 lanes, but maximum of 4 lanes in each direction.	1
F–(No. of octets per frame)	Calculated based on the other parameters.	2
K–(No. of multiframes)	Max 32	16
S–(Samples per converter per frame)	Depends on the converter's capability.	2

4.4 FFT Processing

The FFT co-processor (FFTC) modules in the 66AK2L06 provide the follow features:

- IFFT and FFT operations
- Maximum FFT size of 8192
- Processing up to 1200 Msps for a FFT size of 1024
- 77-dB SNR–dynamic and programmable scaling modes
- Support for FFT shift (switch left and right halves)
- Support for cyclic prefix addition or removal

5 Getting Started Hardware

The *Optimized Radar System Design Using 66AK2L06 DSP+ARM SoC and ADC14X250* Development Kit is an application development platform for evaluating the 66AK2L06 device's connectivity and performance with the leading-edge ADC14X250. As shown in [Figure 5](#), the 66AK2L06 EVM, and ADC14X250 EVM are connected through the K2L-HSP FMC adaptor board that provides signal routing across the FMC interface and supports Deterministic Latency. The DAC38J84 EVM is also shown in [Figure 5](#) as connected to the K2L-HSP FMC adaptor board, which is only used to provide a defined input reference signal on the VIN of the ADC14X250. The output of the DAC38J84 is the input reference signal for the demonstration application.

The purpose of the K2L-HSP FMC adaptor board is to generate sampling clocks for the ADC14X250 and the DAC38J84. The card uses SYSCLK provided by 66AK2L06 as an input reference clock for generating sampling clocks. The card also generates a common SYSREF clock for deterministic latency using the common input SYSCLK. The K2L-HSP FMC Adaptor board routes the JESD lanes and SYNC signals from one Lamarr FMC to 2 data converter FMC connectors, one for ADC and one for DAC. This process allows the 66AK2L06 EVM board to communicate with both ADC and DAC EVMs over the JESD204B interface.

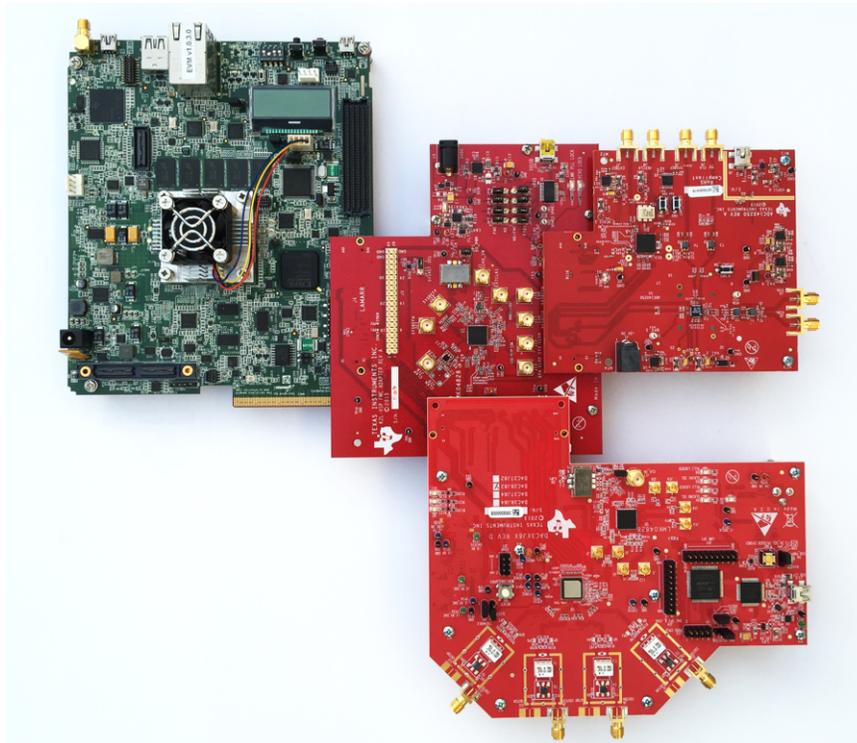


Figure 5. 66AK2L06 DSP+ARM Processor JESD204B Attach to ADC14X250 / DAC38J84 Design Development Kit

For additional information on the 66AK2L06 EVM, refer to <http://www.ti.com/tool/xevmk2lx>.

For additional information on the ADC14X250 EVM, refer to <http://www.ti.com/product/adc14X250evm>.

For additional information on the DAC38J84 EVM, refer to <http://www.ti.com/tool/dac38j84evm>.

6 Getting Started Software

The *Optimized Radar System Design Using 66AK2L06 DSP+ARM SoC and ADC14X250* provides a Linux® application developed using Software Development Kits available from TI.

6.1 Multicore Software Development Kit (MCSDK)

The MCSDK provides foundational software for TI KeyStone II devices. The MCSDK encapsulates a collection of software elements and tools intended to enable customer application development and migration. The foundational components include:

- TI-RTOS real-time embedded operating system on DSP cores.
- Linux high-level operating system running on the ARM A15 cluster (SMP mode).
- DSP chip support libraries, DSP and ARM drivers, and basic platform utilities.
- Interprocessor communication for communication across cores and devices.
- Bootloaders and boot utilities.
- Power-on-self test.

6.2 RF Software Development Kit (RFSDK)

The RFSDK is an integrated software solution that simplifies leveraging all the components of the 66AK2L06 Digital-Front-End (DFE) module. The RFSDK aims to provide an integrated environment to transmit, receive, process, and visualize signals.

- Provides an integrated solution requiring a minimal amount of software development to enable JESD data converters.
- Provides tools for evaluation and debug of the integrated solution with 66AK2L06 devices and data converters.

6.3 Design Linux Application

The *Optimized Radar System Design Using 66AK2L06 DSP+ARM SoC and ADC14X250* Linux application has the following features:

- The application configures the operation of IQN2 and DFE (and required infrastructure such as Navigator, Serdes, DDR, and others) for Tx and Rx according to a particular configuration.
- Users may load pre-defined distinct signal patterns in the Tx buffers (DDR memory) to continuously transmit known data patterns on both carriers. Data patterns are 10msec (one frame) IQ samples and are loaded into memory from where they are played out.
- Tx data may be looped back to Rx at multiple loop points (IQN2, JESD, or external). External Rx data can also be supplied to the receiver to capture external Rx signal (e.g. from a signal generator).
- When requested, playback may capture 10 msec worth of samples at a receiver-in-capture buffer in DDR.

7 Test Setup

Figure 6 shows the connectivity of the various boards. Find more information about the test setup, see the [Optimized Radar System Design Using 66AK2L06 DSP+ARM SoC and ADC14X250 Design Getting Started Guide](#). Figure 6 shows the hardware connectivity diagram.

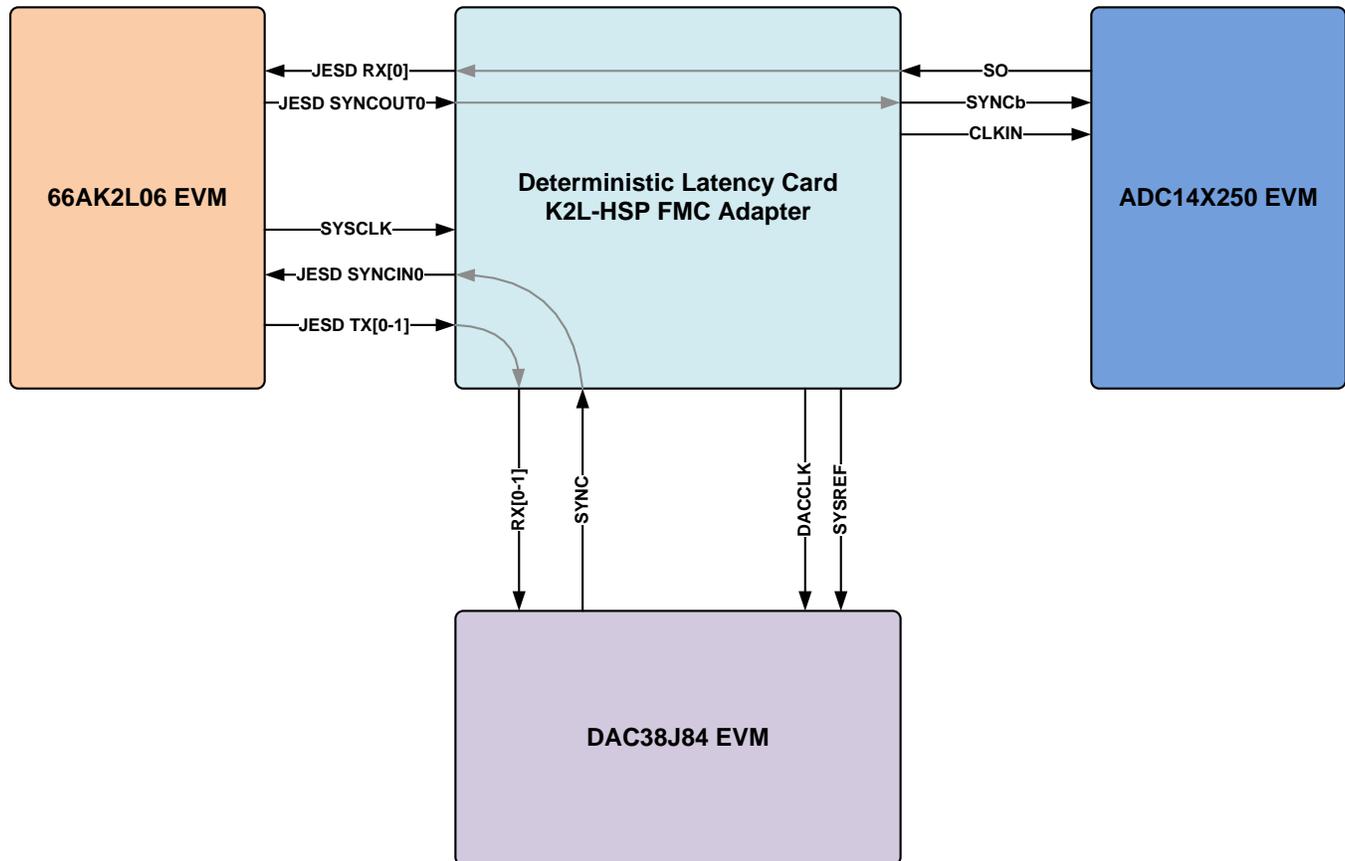


Figure 6. Hardware Connectivity Diagram

- JESD Tx [0-1]—Two 66AK2L06 JESD Transmit Lanes connecting with Rx[0-1] through DLC card.
- Rx[0-1]— Two DAC38J84 JESD Input Lanes.
- JESD Rx[0]— Single 66AK2L06 Receive Lane connecting with SO through DLC card.
- SO— ADC14X250 JESD Output Lane.
- JESD SYNCIN0— 66AK2L06 SYNC Input connected with DAC38J84 SYNC through DLC card.
- JESD SYNCOUT0— 66AK2L06 SYNC Output connected with ADC14X250 SYNCb through DLC card.
- SYSCLK— 122.88-MHz SYSCLK from 66AK2L06 routed through and back to DLC as clock input source for generating sampling clock and SYSREF clock for ADC and DAC.
- CLKIN— 245.76 MHz-Sampling Clock generated by DLC card for ADC14X250.
- DACCLK— 491.52-MHz Sampling Clock generated by DLC card for DAC38J84.
- SYSREF— 15.36-MHz Clock for Synchronization generated by DLC card for DAC38J84.

8 Test Data

8.1 Visualization of the Input, Tx, Rx Data

8.1.1 TX Data

Figure 7 shows the Tx data captured with the RFSDK visualization tools. This data is the raw base band data that will be processed by the 66AK2L06 DFE and converted by the DAC. The two available data files consist of a dual-tone example and a multi-tone example. The IQ data is sampled at 122.88 Msp/s (a dual tone or multi-tone signals). Figure 8 shows the Tx data—Multi-tone.

TX Signal Capture @ DSP (4k FFT, Hanning)

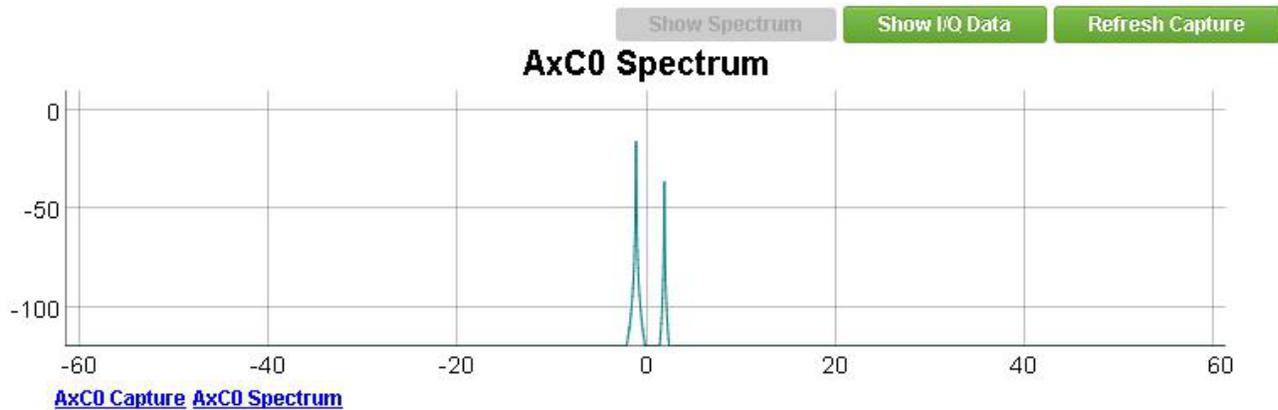


Figure 7. Tx Data— Dual Tone

TX Signal Capture @ DSP (4k FFT, Hanning)

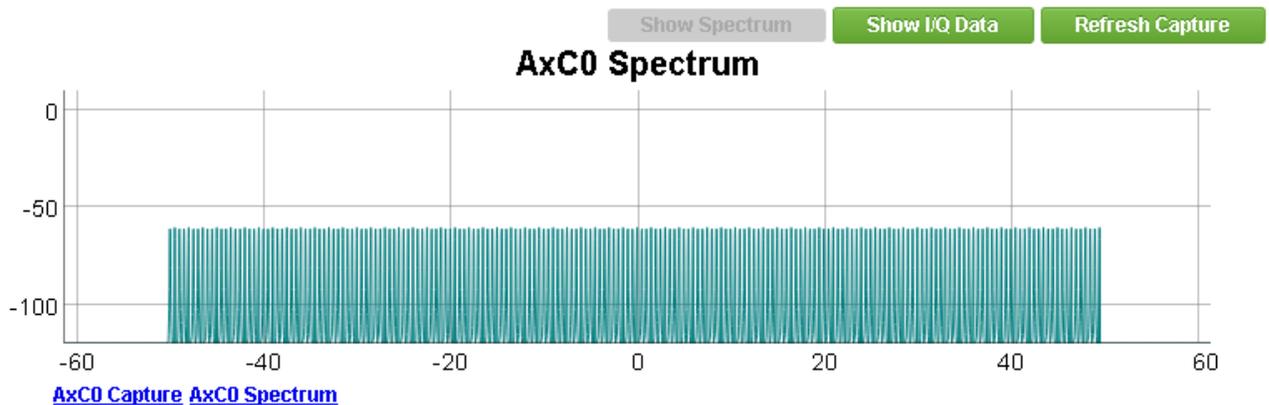


Figure 8. Tx Data— Multi-Tone

8.1.2 Analog Output Data

Figure 9 shows the TX data captured with a spectrum analyzer. This data has been processed by the Tx path of the 66AK2106 DFE and converted by the DAC. The data captured at the output of the DAC, as shown in Figure 10.

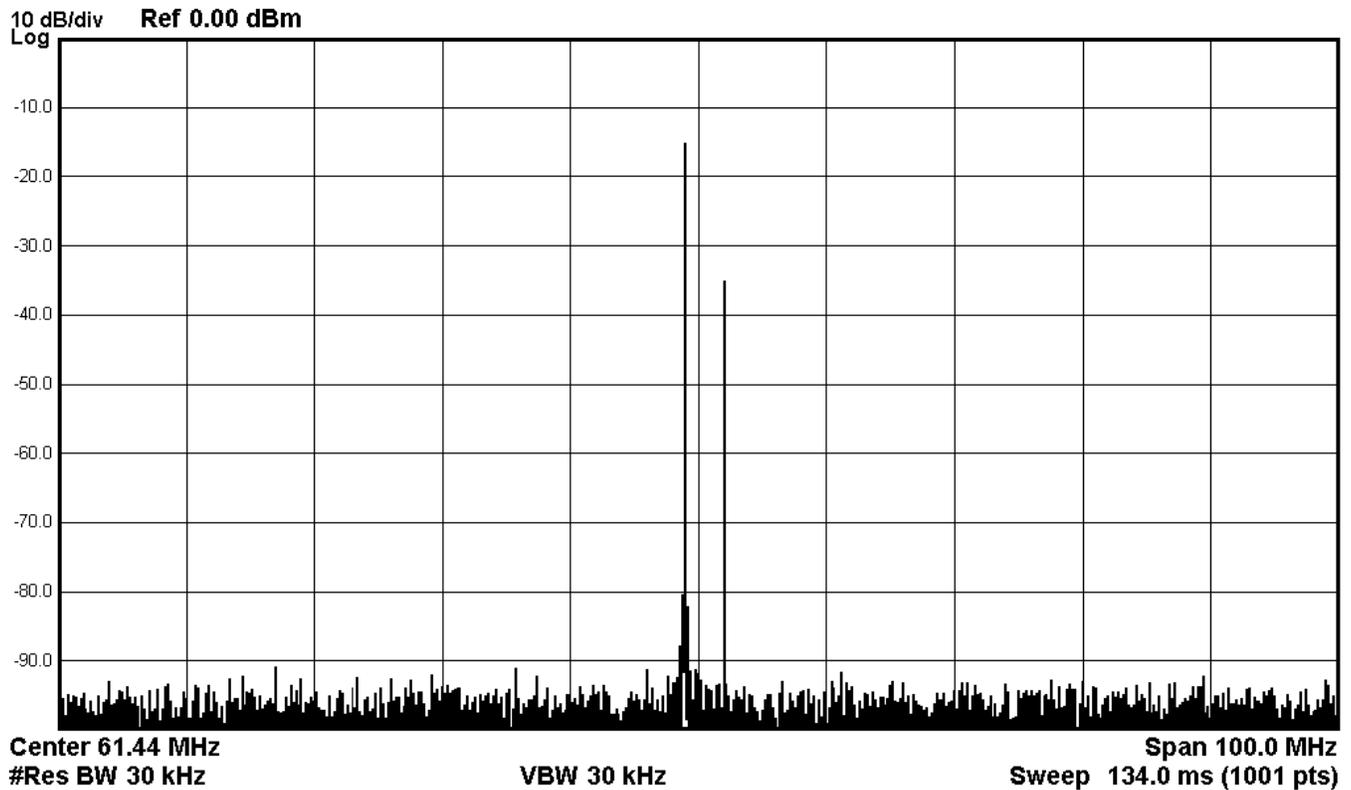


Figure 9. Analog Output Data– Dual Tone (1 MHz and 2 MHz Dual Tone, Centered at 0 IF)

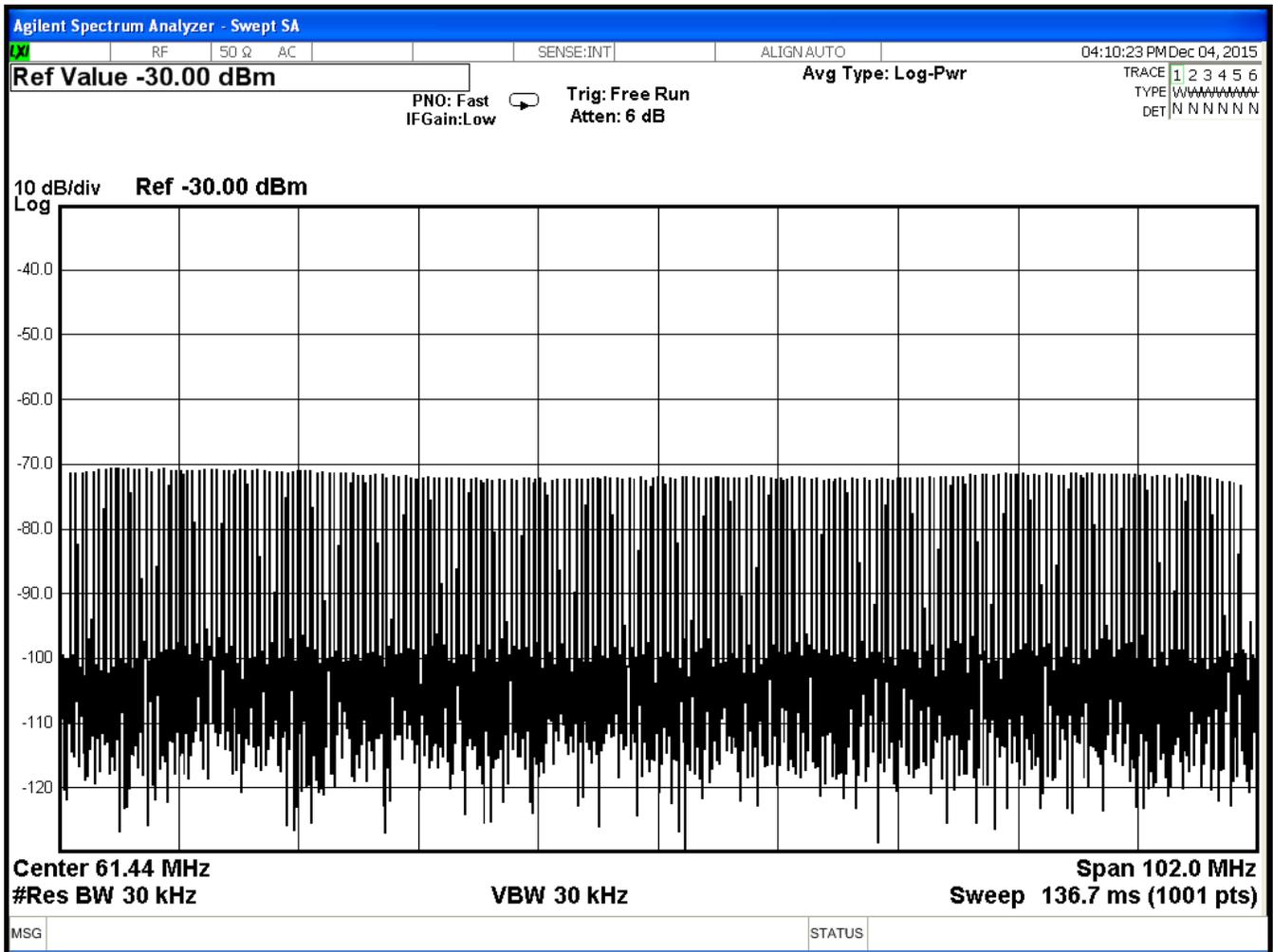


Figure 10. Analog Output Data– Multi Tone

8.1.3 Rx Data

Figure 11 shows the Rx data captured with the RFSDK visualization tools. This data is ADC input that has been converted digital format by the ADC, and processed by the Rx path of the 66AK2L06 DFE. The data is captured in the 66AK2L06 DDR memory. Figure 12 shows the Rx data–Multi-tone.

RX Signal Capture @ DSP (4k FFT, Hanning)

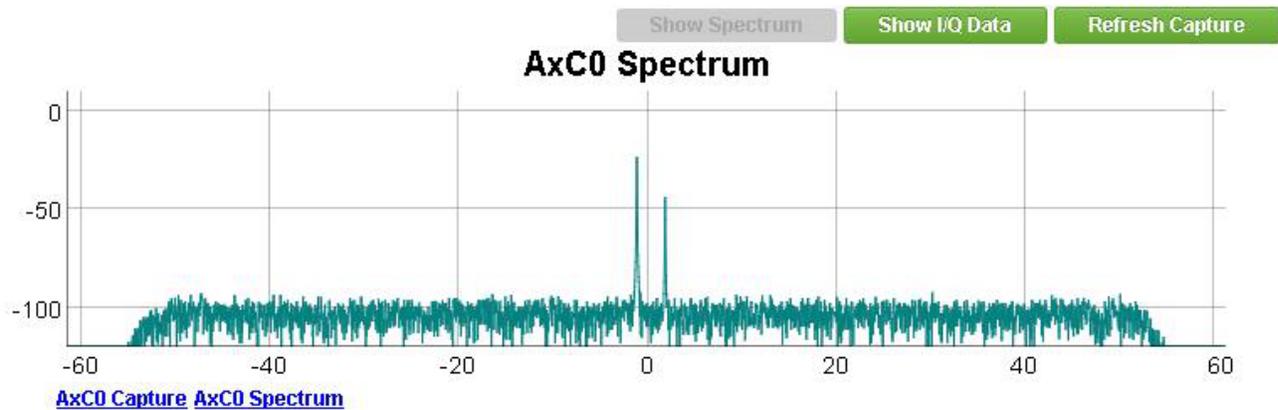


Figure 11. Rx Data– Dual Tone

RX Signal Capture @ DSP (4k FFT, Hanning)

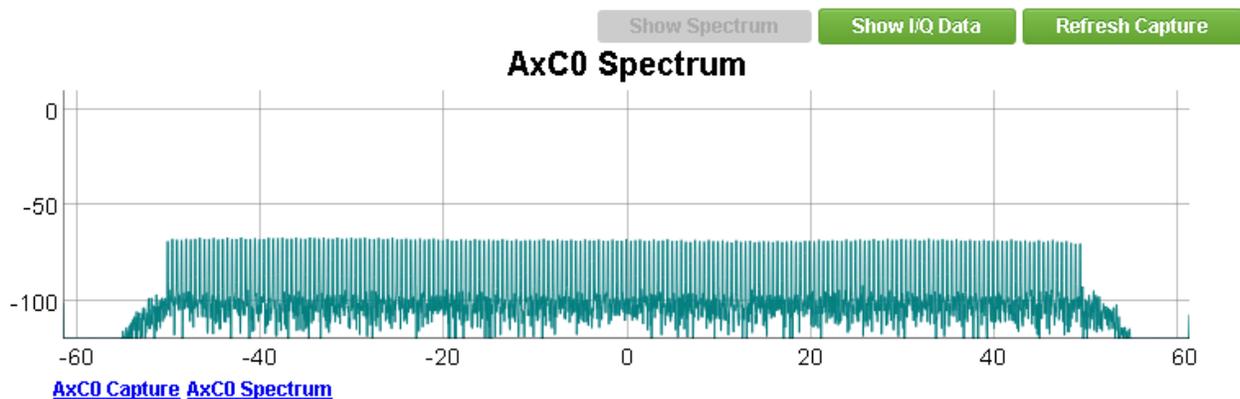


Figure 12. Rx Data– Multi-Tone

8.1.4 Stress Testing

TI ran the demo for 17 hours. The DFE JESD status registers reported no errors.

9 Design Files

9.1 Schematics

A reference schematic and bill of materials has been created which demonstrates a consolidated JESD204B interface and deterministic clocking solution between the 66AK2L06 and ADC14X250 devices. This reference design is based on the EVM environment described above. This design consolidates the integration to demonstrate the fundamental interfaces between these devices without the existing EVM architecture. Because of this, the necessary JESD204B, SPI, GPIO and clocking tree are simplified when compared to the EVM architecture.

Block diagrams are included with the schematic to provide an overall system context for the proposed consolidated design, however only the JESD204B and ADC control and deterministic JESD clocking components are actually implemented in the schematic itself. [Figure 13](#) shows the schematic diagram.

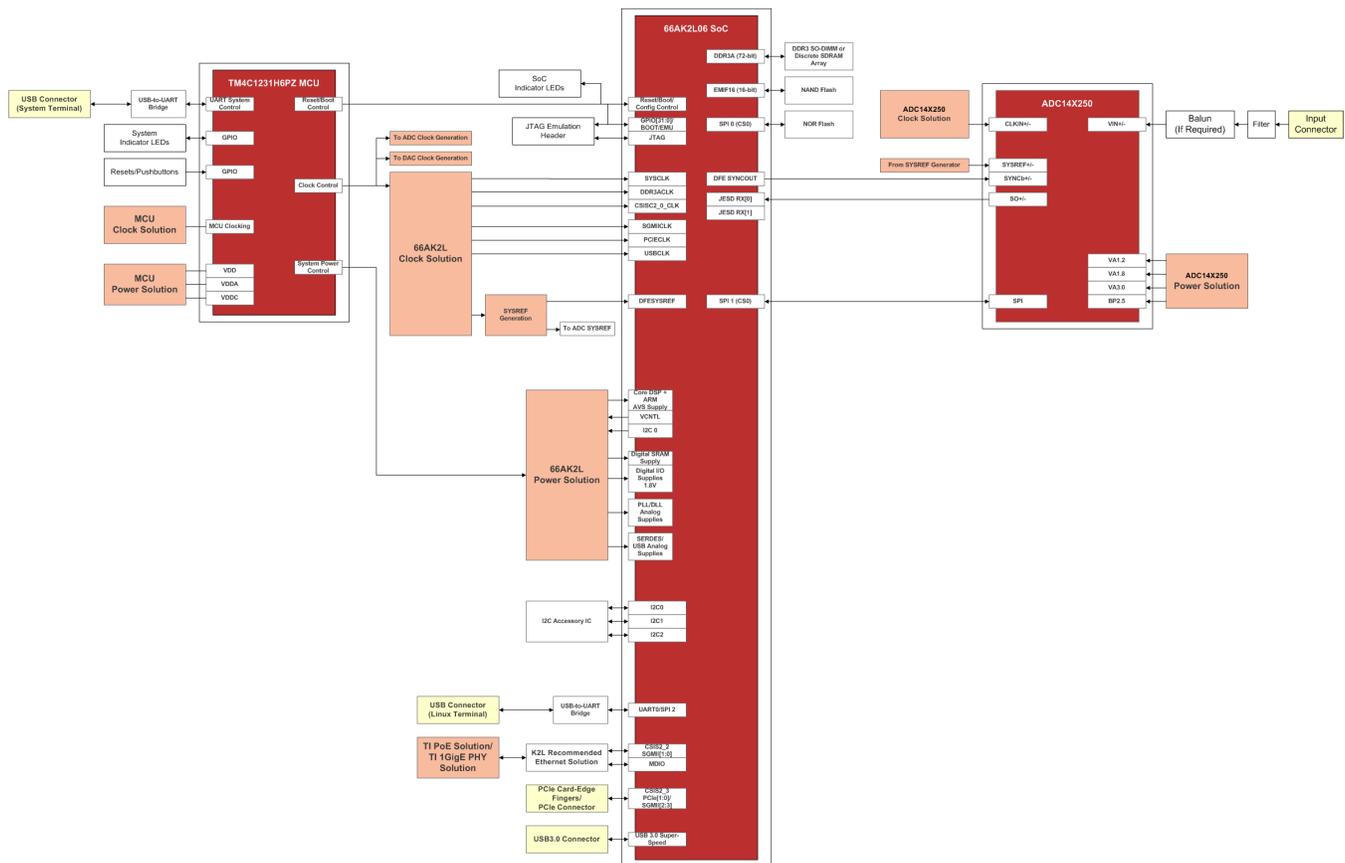


Figure 13. Schematic Diagram

Overall Proposed System

Figure 13 shows the basic structure of schematics. This system proposes a 66AK2L06 system which includes the following major components:

- TPS544 based AVS supply for the 66AK2L06 core digital supply.
- Dual TPS65400, quad-channel buck converters for providing all 66AK2L06, LMK04828m, and ADC14X250 power.
- LMK04828, dedicated, JESD synchronous clock solution.
- CDCM6208, low-jitter clock generator for the 66AK2L06.
- TM4C microcontroller to provide overall system control.
- Hypothetical, system use of non-JESD 66AK2L06 peripherals (SGMII, PCIe, DDR3, NAND flash, and more).

66AK2L06 to ADC14X250 JESD Integration

The 66AK2L06 SoC masters the ADC14X250 ADC through SPI port 0. TI recommends that the selected SPI port is dedicated to the task of supporting the attached ADC such that any commands to or feedback from the ADC may be serviced with the highest possible bandwidth. The ADC14X250 JESD SERDES transmit channel, SO±, is routed to the 66AK2L06 SERDES receiver channel JESDRX0P/N which is a subset of the 2-port SHARED_SERDES_0 block. The remainder JESD transmitter and receiver channels of the 66AK2L06 JESD interface are left unconnected in this use-case. The SERDES reference clock inputs of the SHARED_SERDES_1 block are properly left unconnected along with all of the unused transmitter and receiver differential pairs.

The LMK04828 JESD204B clock synthesizer is used to provide the device clock and periodic SYSREF pulses for the 66AK2L06 and ADC14X250 devices. The LMK04828 is also used to provide the SERDES reference clocks for the 66AK2L06. The LMK04828 dual PLL architecture and high output frequency limit provides a deterministic reference clock source. The reference clock source is used by all data acquisition and processing elements, SERDES transmitters, receivers, and baseband processing elements within the JESD204B system.

9.2 Bill of Materials

To download the BOM, see the design files at .

9.3 PCB Layout Recommendations

- Refer to the 66AK2L06 JESD204B specific section in the *KeyStone II Architecture Serializer/Deserializer (SerDes) User Guide (SPRUHO3)*.
- Refer to the 66AK2L06 JESD204B specific section in the *Hardware Design Guide for KeyStone II Devices (SPRABV0)*.
- Refer to the layout section of the LMK0482x *Ultra Low-Noise JESD204B Compliant Clock Jitter Cleaner with Dual Loop PLLs (SNAS605AQ)*.
- Refer to the layout section of the *ADC14X250 14-Bit 250 Msps ADC with Integrated DDC* at <http://www.ti.com/product/adcX250>.

9.4 Software Files

To download the software files for this design, see the design files at <http://www.ti.com/tool/TIDEP0060>.

- The MCSDK may be downloaded from [bioslinuxmcsdk](#)
- The RFSdk may be downloaded from [rfsdk](#)

10 References

1. KeyStone II Architecture Digital Radio Front End user's Guide ([SPRUHX8](#))
2. KeyStone II Architecture Serializer/Deserializer (SerDes) User Guide ([SPRUHO3](#))
3. Hardware Design Guide for KeyStone II Devices ([SPRABV0](#))

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