TI Designs

LDO Parallel Solution Reference Design With TPS7B4253-Q1

TI Designs

This TI Design uses a very low-tolerance, voltage-tracking LDO TPS7B4253-Q1 to demonstrate the implementation of LDO parallel solution for high output current and low quiescent current (IQ) requirements. In this design, TPS7B6750-Q1 regulates 5-V output voltage and two TPS7B4253-Q1 devices expand the output current and realize the current sharing of each channel.

Design Resources

TIDA-00863	Design Folder
TPS7B4253-Q1	Product Folder
TPS7B6750-Q1	Product Folder

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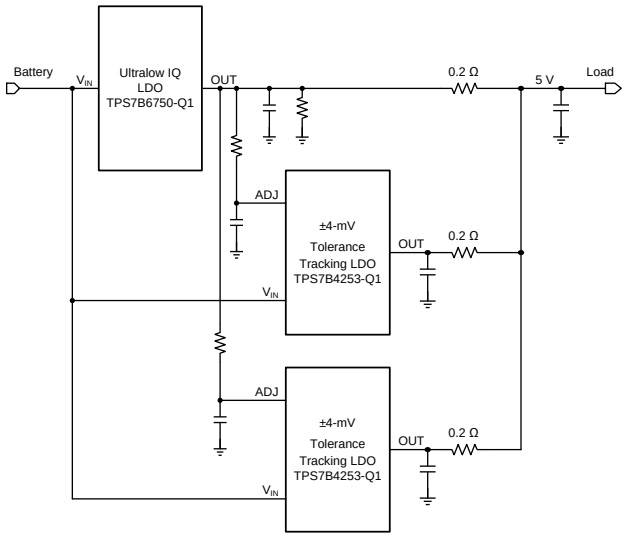
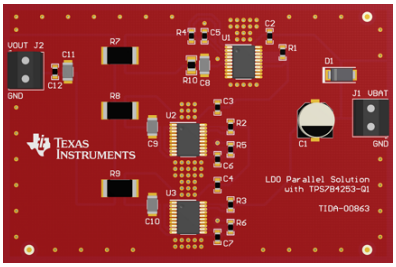
Design Features

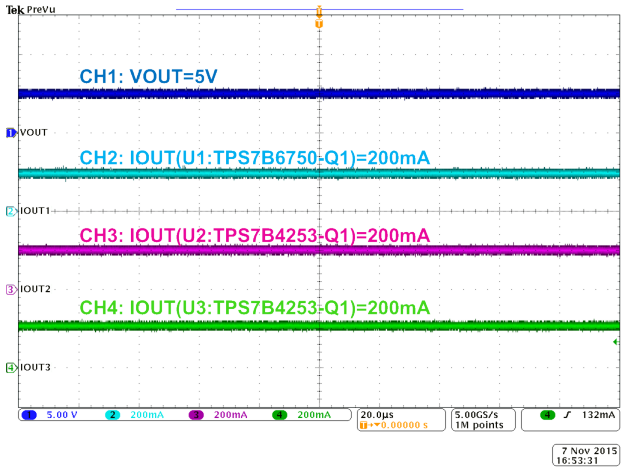
- Expanded Output Current, Up to 900 mA
- Good Thermal Performance Under Large Load Conditions
- 4- to 40-V Wide Input Voltage Range
- Wide Range of Output Capacitor Selection
  - Stable With 10- to 500-µF Ceramic Output Capacitor
  - ESR Range From 0.001 Ω to 20 Ω

Featured Applications

- Cluster
- HVAC
- Body Control Modules
- Shift-by-Wire







Current Sharing of Each Channel

1 Key System Specification

Table 1. Key System Specifications

PARAMETER	SPECIFICATION
Input voltage	6- to 40-V DC
Regulated output voltage	5 V
Output current range	900 mA maximum
Operating temperature	–40°C to 125°C

2 System Description

The TIDA-00863 reference design provides a linear regulator parallel solution for the large output current requirement of linear regulators. A first-stage power supply in automotive applications, where both large current and low-quiescent current (I_Q) are required, is one use of this design.

In this TIDA-00863 reference design, TPS7B6750-Q1 regulates 5-V output voltage and TPS7B4253-Q1 expands the output current and realizes the current sharing of each channel.

The TIDA-00863 reference design is primarily focused in the linear regulator parallel section and provides test data, schematic, and Gerber files.

3 Block Diagram

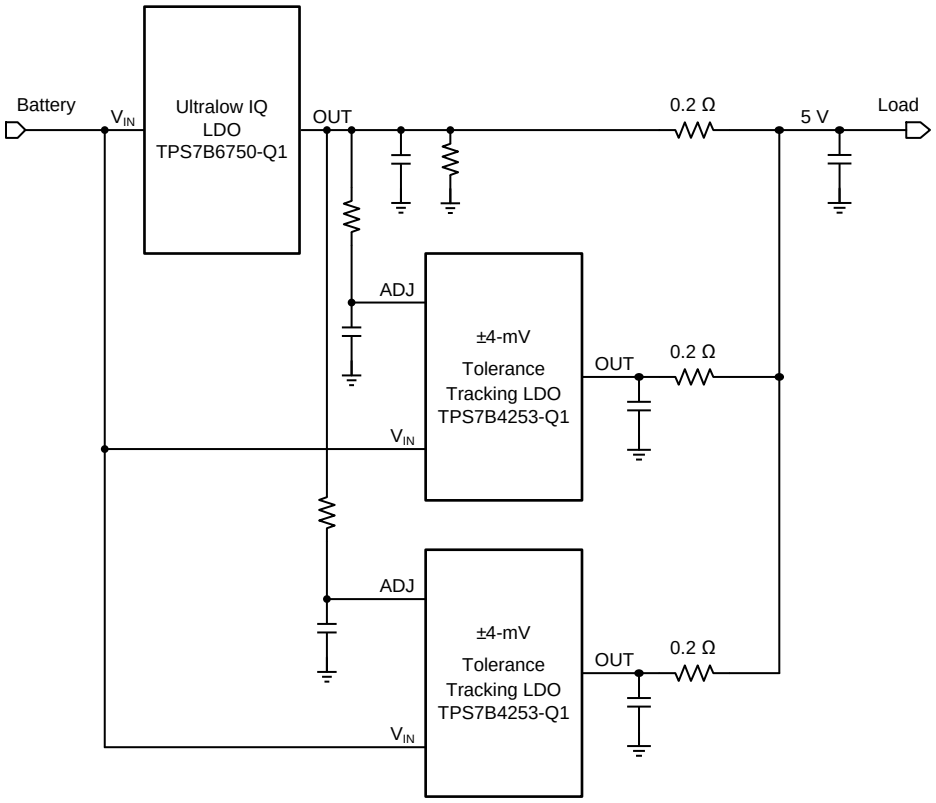


Figure 1. Block Diagram

3.1 Highlighted Products

The TIDA-00863 reference design features the following TI regulators:

- TPS7B6750-Q1: 450-mA high-voltage ultralow-I_Q, low-dropout regulator
- TPS7B4253-Q1: 300-mA low-dropout, voltage-tracking LDO

Key features for selecting the devices for this reference design are provided in the following sections. See the respective product folders at www.ti.com for complete details of these devices.

3.1.1 TPS7B6750-Q1

The TPS7B6750-Q1 device is one low-dropout linear regulator designed for up to 40-V VIN operations. With only 15-µA I_Q at a light load, this device increases the endurance time of automotive batteries.

The TPS7B6750-Q1 device drives loads up to 450 mA and is suitable for many automotive applications, especially when used as a power supply of an infotainment system, body control module, and always-on battery applications.

In the TIDA-00863 design, TPS7B6750-Q1 regulates 5-V voltage at the output. This 5-V voltage is the reference voltage (ADJ) for TPS7B4253-Q1.

3.1.2 TPS7B4253-Q1

The TPS7B4253-Q1 device is designed for automotive applications with a 45-V load dump. The device offers a 4-mV ultralow-tracking tolerance between the ADJ and FB pins across a temperature range of –40°C to 125°C. The reference voltage at the ADJ pin accurately regulates the output of the device.

The TPS7B4253-Q1 device can either be used as one tracking low-dropout regulator, or as a voltage tracker to build one closed-power loop for off-board sensors with an onboard mains supply. In the TIDA-00863 design, TPS7B4253-Q1 is used to expand the total output current up to 600 mA.

4 System Design Theory

The TIDA-00863 reference design uses the voltage-tracking LDO TPS7B453-Q1 and the I_Q LDO TPS7B6750-Q1 to demonstrate the LDO parallel solution for large output current and low I_Q demands.

The TPS7B6750-Q1 is a 5-V fixed version, low dropout regulator in the TPS7B67xx-Q1 family. When powered up with input voltage higher than 5.5 V, the TPS7B6750-Q1 regulator regulates a 5-V output voltage within ±2% accuracy. In this reference design, this 5-V voltage is directly the ADJ of the TPS7B4253-Q1 device. A voltage-tracking LDO with ultralow-tracking tolerance, the TPS7B4253-Q1 follows the reference voltage within ± 4 mV. The voltage difference between the three LDOs measures ±4 mV only (maximum).

The TPS7B6750-Q1 can output current up to 450 mA and the TPS7B4253-Q1 can output current up to 300 mA. Using one TPS7B6750-Q1 LDO with two TPS7B4253-Q1 LDOs in parallel can expand output current to 1050 mA. This large output current is theoretical; the maximum value is determined by the working conditions of this TI Design. The following sections discuss the design theory based on a test case from three aspects:

- Thermal design
- Current sharing
- Loop stability

4.1 Thermal Design Considerations

In the circuit design of linear regulators, thermal designs are important. Avoid device junction temperatures exceeding 150°C to ensure the stability of the three LDOs.

The following is a design example to illustrate this concept:

Table 2. Design Example

PARAMETER	DESIGN SPECIFICATION
Input voltage, V_{IN}	12 V
Output voltage, V_{OUT}	5 V
Ambient temperature, T_A	85°C
PCB parameters	four layer, 1 oz
θJA(TPS7B4253-Q1, HTSSOP-20)	45°C per W(1)
θJA(TPS7B6750-Q1, HTSSOP-20)	45°C per W(1)
Operating junction temperature range, T_J	–40°C to 150°C

(1) Thermal impedance data is measured on the PCB in this reference design

Calculate the maximum power dissipation of the devices with Equation 1 and Equation 2

$$P_{D\_MAX} = \frac{\Delta T}{\theta_{JA}} = \frac{T_J - T_A}{\theta_{JA}} = \frac{150°C - 85°C}{45°C / W} = 1.444\ W \quad (1)$$

Calculate the maximum current of the devices:

$$I_{MAX} = \frac{P_{D\_MAX}}{V_{IN} - V_{OUT}} = \frac{1.444\ W}{12\ V - 5\ V} = 0.206\ A \quad (2)$$

Maximum current of each device is approximately 200 mA, therefore the total maximum current is 600 mA.

4.2 Current Sharing Considerations

As the TPS7B4253-Q1 is a voltage-tracking LDO with ultralow-tracking tolerance, the maximum voltage difference between the outputs of three LDOs is small (±4 mV) across all conditions. This small voltage difference results in unbalanced current sharing if three outputs are connected directly (otherwise, system instability may occur).

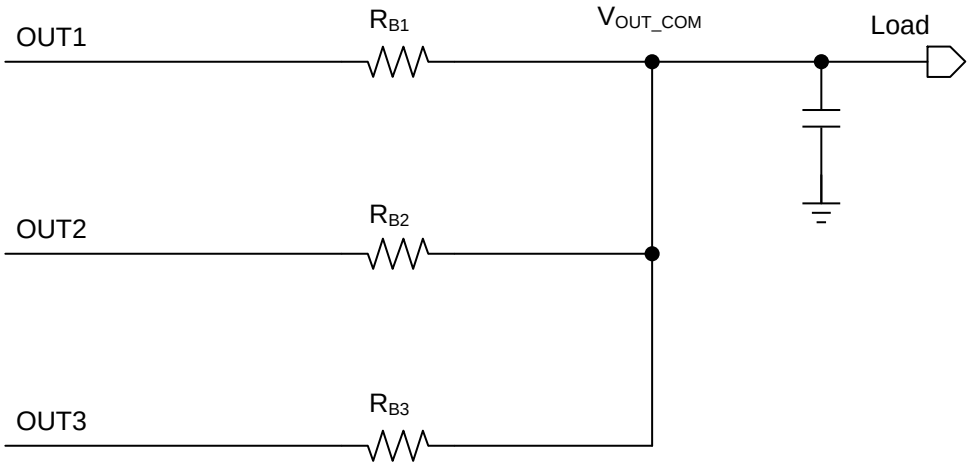


Figure 2. Current Balancing With Ballasting Resistor

Solve this problem by inserting the ballasting resistor R_B at each output of the three LDOs, as shown in Figure 2. Choose three identical resistors to ensure the current flow through the three channels are close under a heavy load.

In addition, compensate for the ± 4-mV voltage difference through the current difference between each channel. Equation 3 calculates the maximum current difference.

$$\Delta I_{MAX} = \frac{\Delta V_{MAX}}{R_B} = \frac{\pm 4\ mV}{R_B} \tag{3}$$

Under a heavy load, like 600 mA, the same current flows through each channel, and Equation 4 calculates this current value:

$$I_{OUTx} = \frac{I_{LOAD}}{3} \tag{4}$$

Equation 5 calculates the voltage drop across the ballasting resistor.

$$\Delta V_{DROP} = \frac{I_{LOAD}}{3} \times R_B = \frac{600\ mA}{3} \times R_B \tag{5}$$

The previous equations show a trade-off between the voltage drop and the current difference. A larger R_B produces a smaller current difference but a larger voltage drop. A smaller R_B produces a smaller voltage drop but a higher current difference. In this reference design, choose 0.2-Ω resistors.

See the previous equations and calculate the output voltage of this LDO parallel solution using Equation 6.

$$V_{OUT} = V_{OUT\_TPS7B6750\text{-}Q1} - \frac{I_{LOAD}}{3} \times R_S = 5\ V - \frac{600\ mA}{3} \times 0.2\ \Omega = 4.96\ V \tag{6}$$

4.3 Loop Stability Consideration

System instability occurs when the common node has no load, or either V_{OUT2} or V_{OUT3} measures 4 mV higher than V_{OUT1}. In this instance, the only current path travels from OUT2 or OUT3 to OUT1, causing system instability.

To maintain system stability, disable the other two TPS7B4253-Q1 LDOs by pulling EN down or connect a dummy load at OUT1 (as shown in Figure 3).

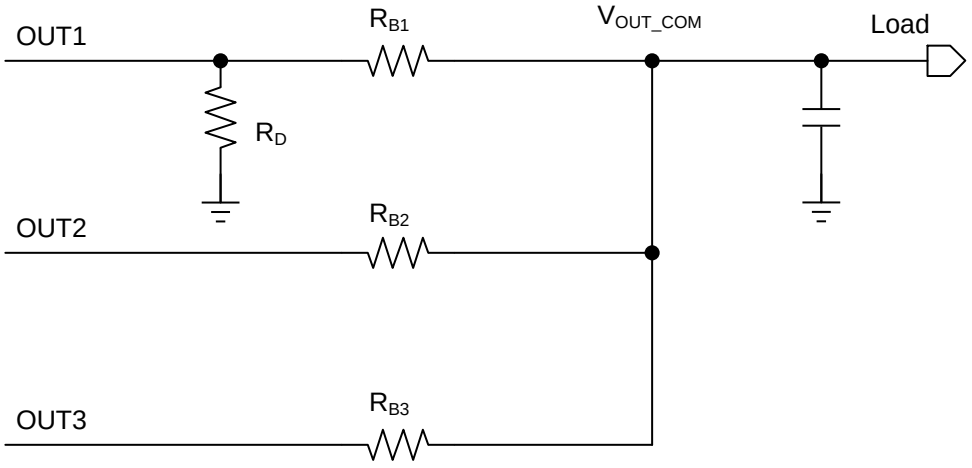


Figure 3. Dummy Load

Calculate the minimum dummy load with Equation 7.

$$I_{DUMMY} = \frac{4\ mV}{R_{B1} + \frac{R_{B2} \times R_{B3}}{R_{B2} + R_{B3}}} = \frac{4\ mV}{0.2\ \Omega + \frac{0.2\ \Omega \times 0.2\ \Omega}{0.2\ \Omega + 0.2\ \Omega}} = 13.3\ mA \quad (7)$$

Calculate the maximum resistor R_D with Equation 8.

$$R_D = \frac{V_{OUT1}}{I_{DUMMY}} = \frac{5\ V}{13.3\ mA} = 375\ \Omega \quad (8)$$

Select 365 Ω for this reference design.

5 Getting Started

Implement this design based on the previous LDO parallel specifications in this section.

5.1 Input Capacitor

The TIDA-00863 reference design requires an input bypass capacitor, the value of which depends on the application. The typical recommended value for the bypass capacitor is 22 µF. The voltage rating must be greater than the maximum input voltage.

5.2 Output Capacitor

To ensure the stability and proper loop operation of device TPS7B4253-Q1 and device TPS7B6750-Q1, this design requires an output capacitor with a value between 10 µF to 500 µF and an ESR range from 0.001 Ω to 20 Ω at the output of each device and at the common node.

TI recommends the X7R ceramic capacitor with low ESR to improve the load transient response.

When multiple capacitors (two or more) are connected in parallel at the OUT pin, the ESR range of each output capacitor must be from 0.001 Ω to 3 Ω for loop stability.

6 Test Data

The test data in this section applies to the parameters mentioned in this TI Design. For alternative configurations, see the respective data sheets of the devices.

NOTE: All of the measurements in this section were measured with calibrated lab equipment.

6.1 Test Equipment

The following Table 3 shows the test equipment used in these sections.

Table 3. Test Equipment

TEST EQUIPMENT	MODEL
Power supply	Agilent E3634A
Oscilloscope	Tektronix DPO4104
Multimeter	Agilent E34401A
Loads	Power resistors

6.2 Line Regulation

Figure 4 shows the line regulation with different supply voltages.

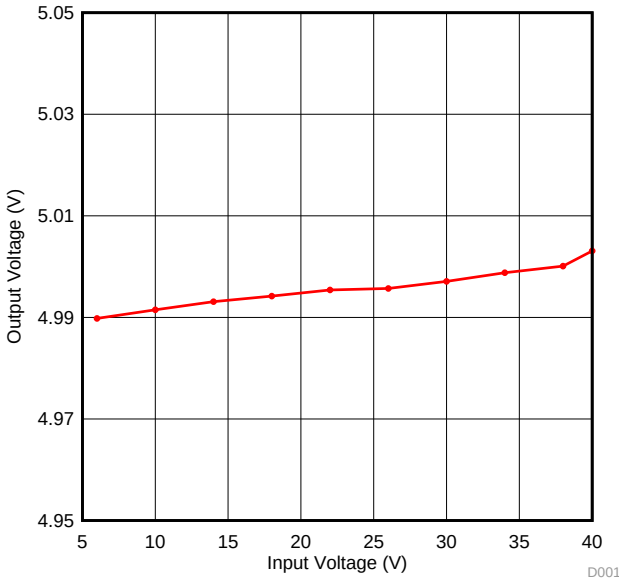


Figure 4. Line Regulation (Load = 300 mA)

6.3 Load Regulation

Figure 5 shows the device line transient response under different load conditions.

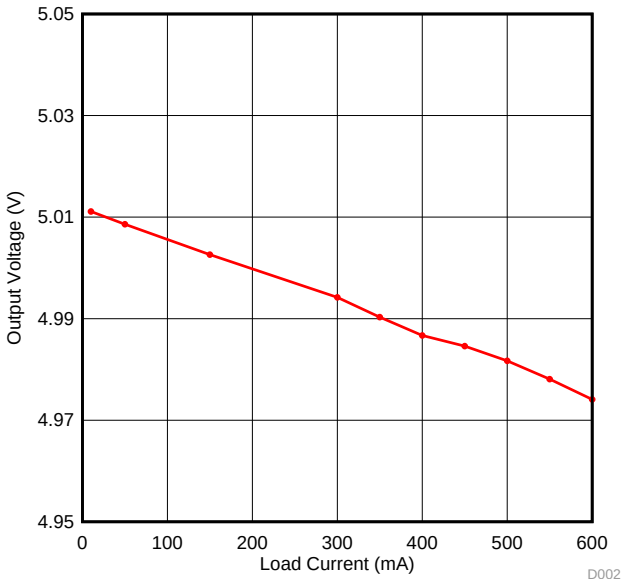


Figure 5. Load Regulation (V_{IN} = 14 V)

6.4 Line Transient

Figure 6 and Figure 7 show the device line transient response under different load conditions.

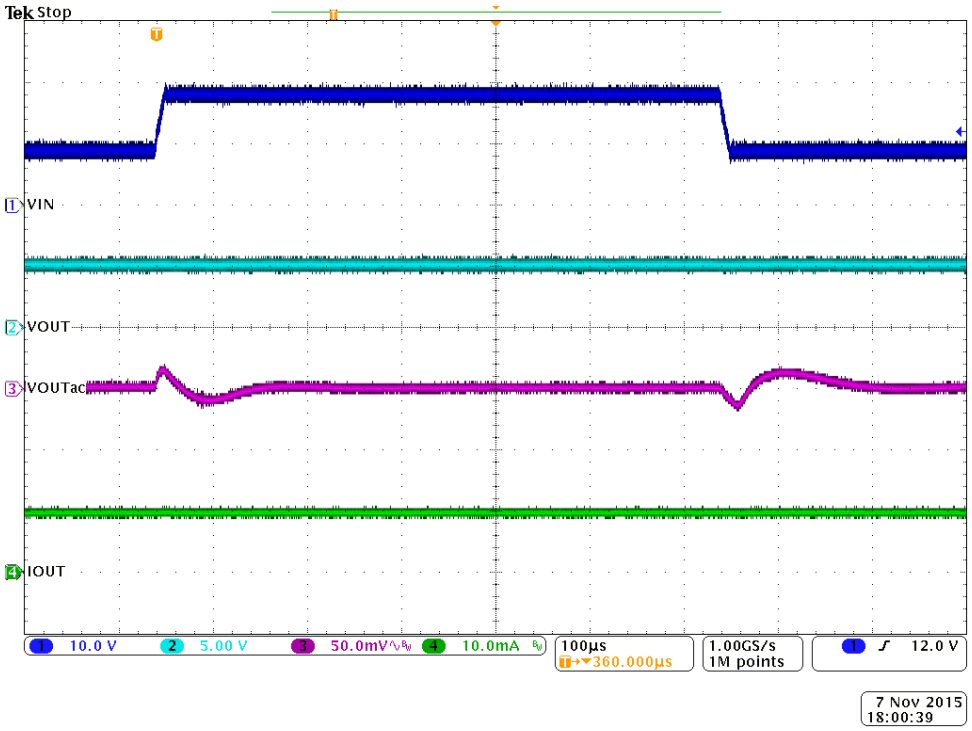


Figure 6. Line Transient From 9 V to 18 V (1 V/µs) With 10-mA Load

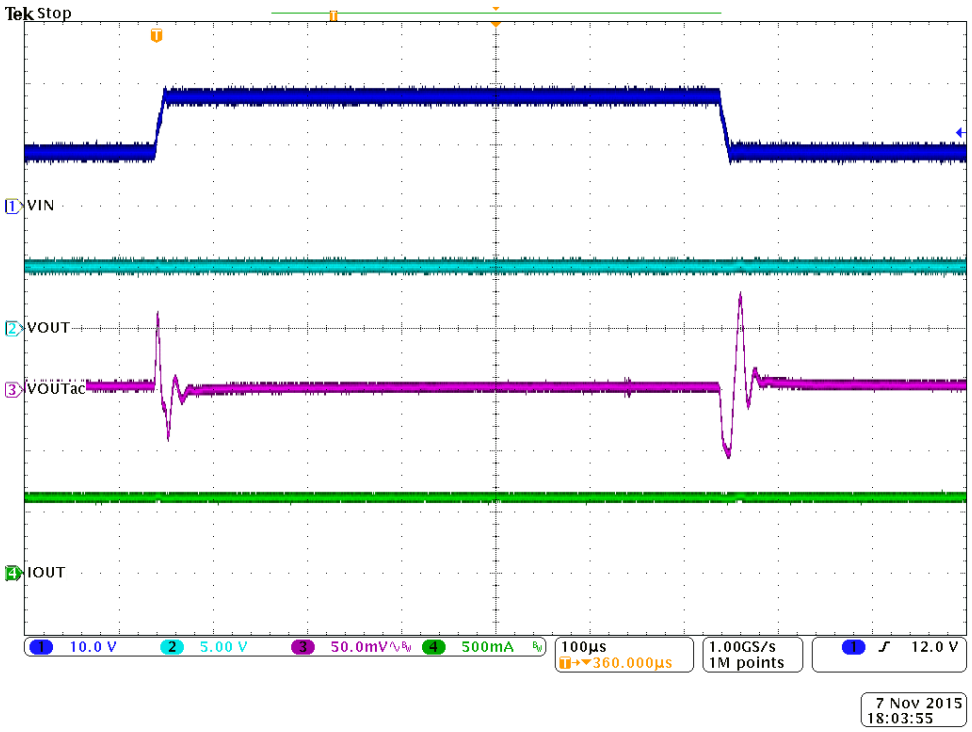


Figure 7. Line Transient From 9 V to 18 V (1 V/µs) With 600-mA Load

6.5 Load Transient

Figure 8 shows the device load transient response with a 14-V input voltage.

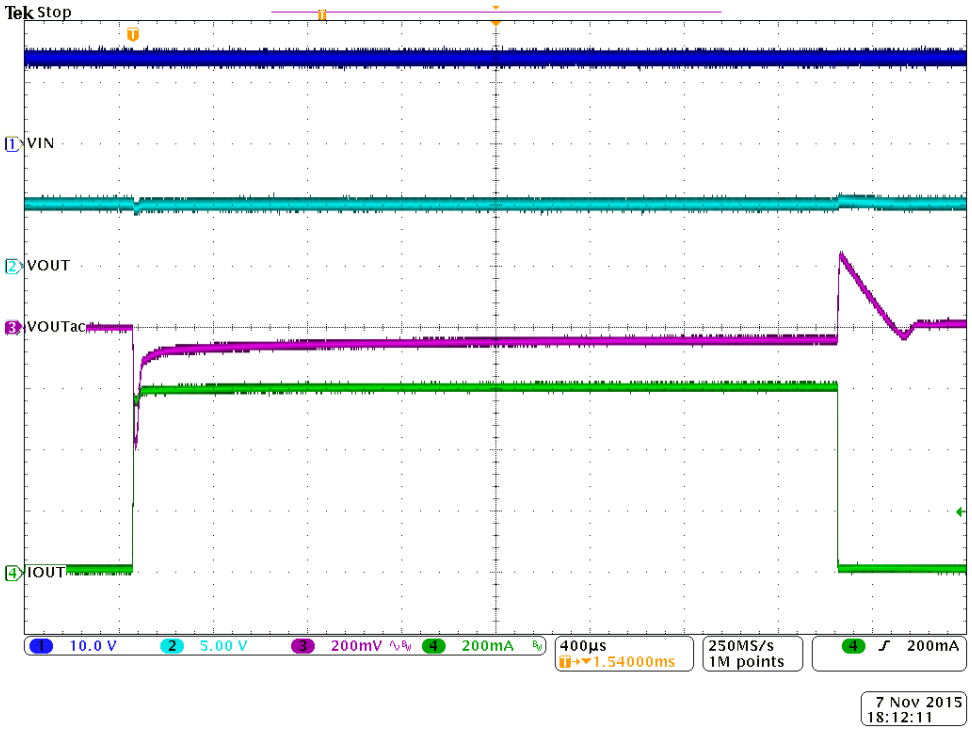


Figure 8. Load Transient From 10 mA to 600 mA

6.6 Power Up

Figure 9 and Figure 10 show the device output response during power up under different load conditions.

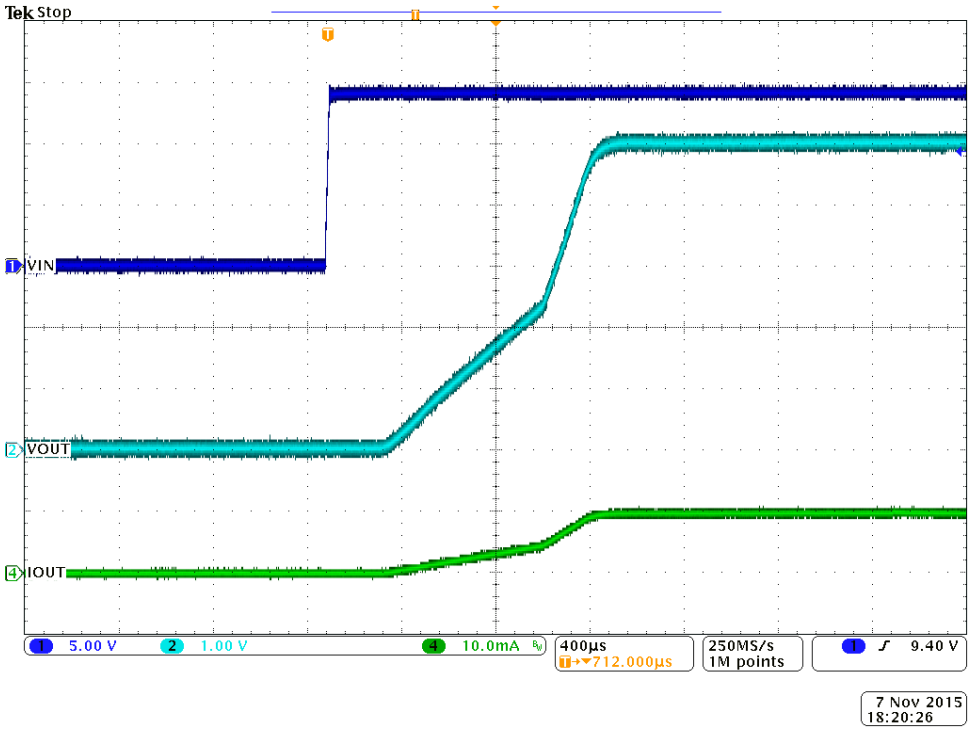


Figure 9. Power-up From 0 V to 14 V With 10-mA Load

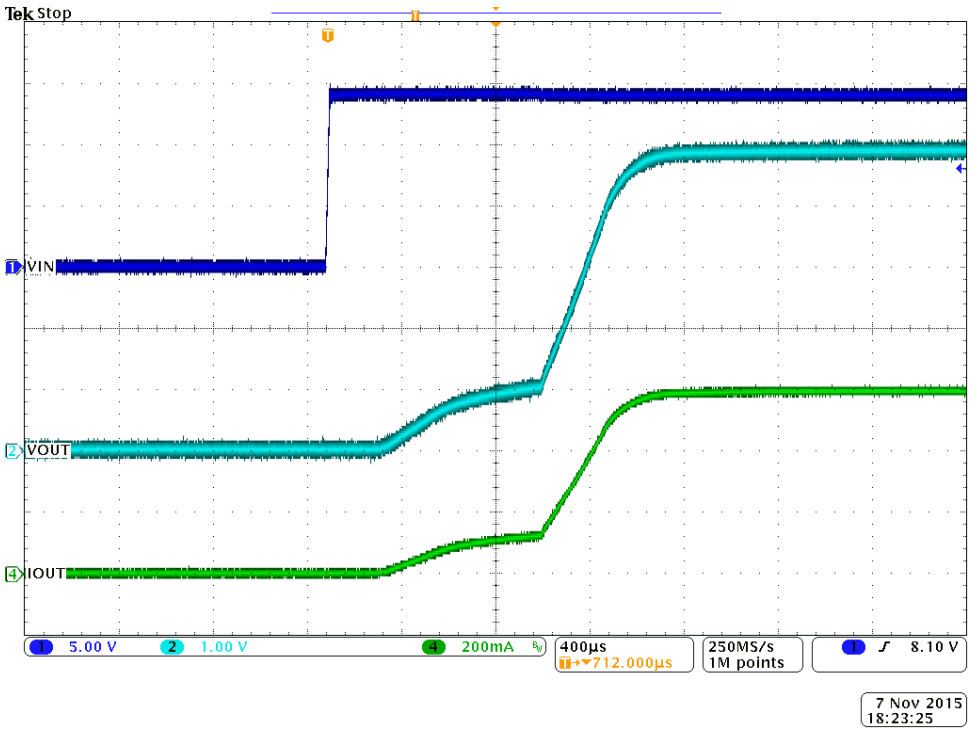


Figure 10. Power-up From 0 V to 14 V With 600-mA Load

6.7 Load Transient Improvement

In the default setup, the output capacitors are 10-µF ceramic capacitors. To improve load transient response, use larger output capacitors.

Figure 11 shows the device load transient response by increasing output capacitors to 22 µF with the same test conditions and 100 mV of lower undershot (for which overshot voltage is achieved).

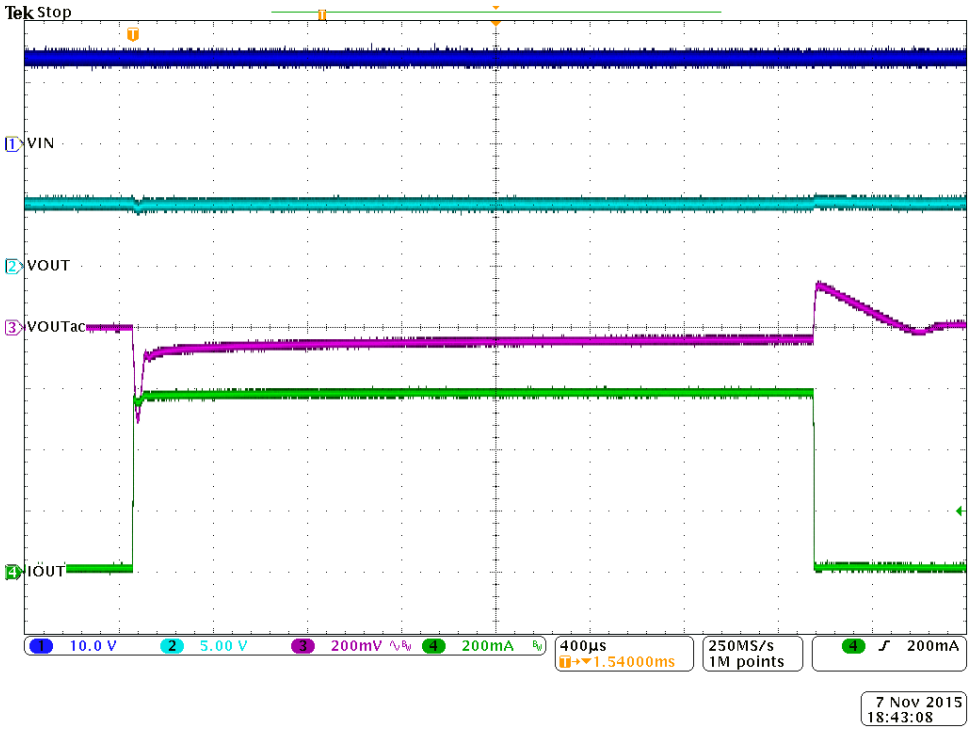


Figure 11. Improved Load Transient From 10 mA to 600 mA

6.8 Thermal Performance

Figure 12 shows the device thermal performance with the condition of V_{IN} = 12 V and load = 600 mA under room temperature (T_A = 25°C).

The highest temperature in the figure is 89.5°C, concentrated on the three LDO devices and the temperature rise is consistent with calculations Equation 1 and Equation 2 in Section 4.1. When the ambient temperature reaches 85°C, the device temperature remains lower than 150°C to prevent the device from thermal shutdown.

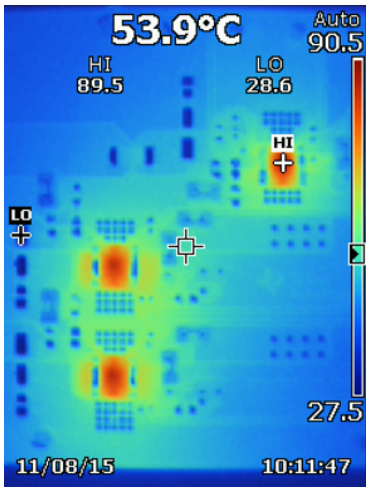


Figure 12. Thermal Performance at V_{IN} = 12 V; Load = 600 mA; 25°C

7 Design Files

7.1 Schematics

To download the schematics for each board, see the design files at TIDA-00863

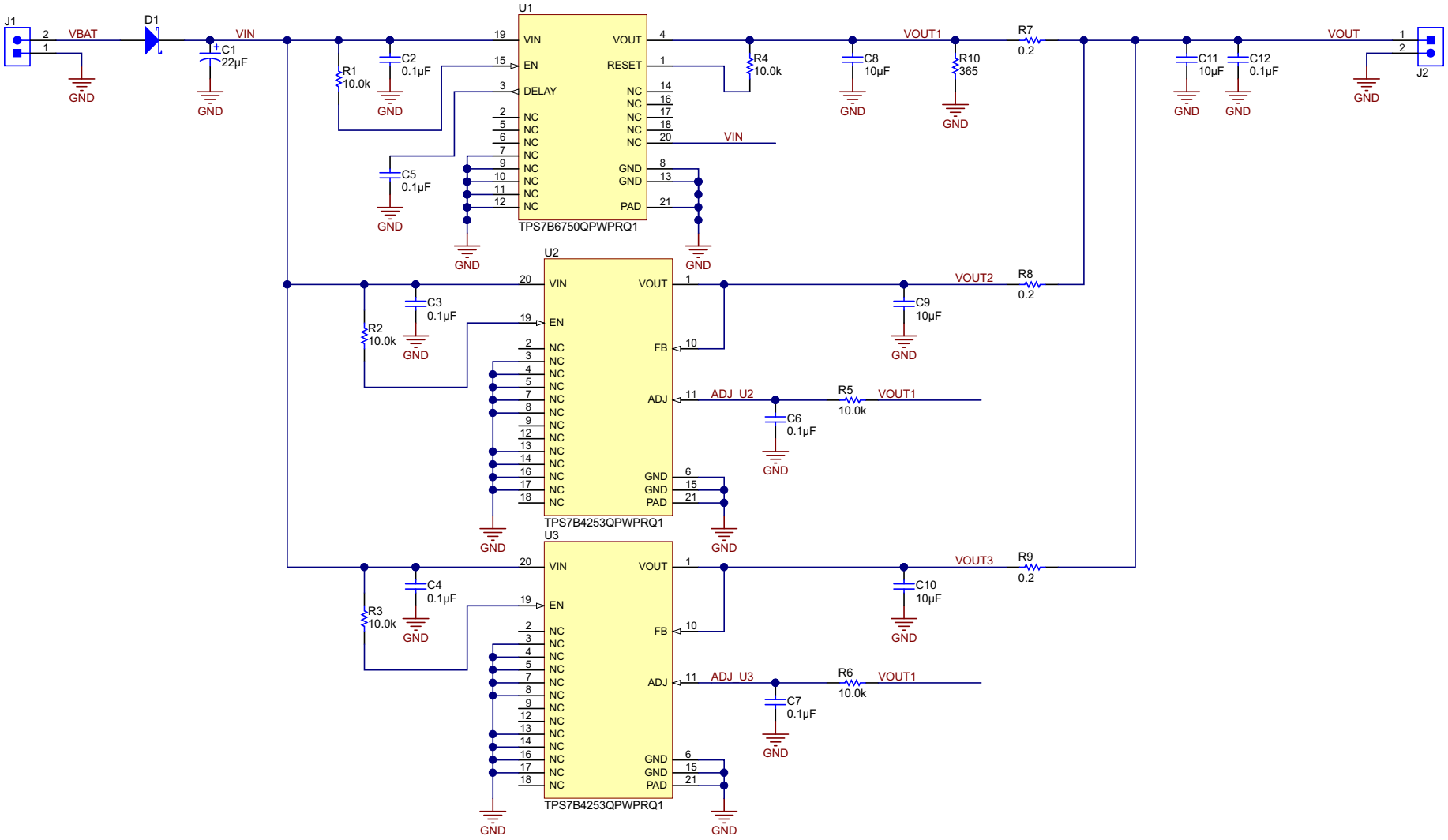


Figure 13. Schematic of LDO Parallel Solution

7.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00863.

Table 4. Bill of Materials

DESIGNATOR	QUANTITY	VALUE	DESCRIPTION	PACKAGE REFERENCE	PART NUMBER	MANUFACTURER
!PCB1	1		Printed Circuit Board		TPS7B4253	Any
C1	1	22 µF	CAP, AL, 22 µF, 50 V, ±20%, 0.88 Ω, SMD	SMT Radial D	EEE-FK1H220P	Panasonic
C2, C3, C4, C5, C6, C7, C12	7	0.1 µF	CAP, CERM, 0.1 µF, 50 V, ±10%, X7R, 0603	603	GCM188R71H104KA57D	MuRata
C8, C9, C10, C11	4	10 µF	CAP, CERM, 10 µF, 16 V, ±10%, X7R, AEC-Q200 Grade 1, 1206_190	1206_190	GCM31CR71C106KA64L	MuRata
D1	1	60 V	Diode, Schottky, 60 V, 2 A, SMA	SMA	B260A-13-F	Diodes Inc.
FID1, FID2, FID3	3		Fiducial mark. There is nothing to buy or mount.	Fiducial	N/A	N/A
J1, J2	2		Terminal Block, 6A, 3.5-mm Pitch, 2-Pos, TH	7.0 × 8.2 × 6.5 mm	ED555/2DS	On-Shore Technology
R1, R2, R3, R4, R5, R6	6	10.0k	RES, 10.0k, 1%, 0.1 W, 0603	603	CRCW060310K0FKEA	Vishay-Dale
R7, R8, R9	3	0.2	RES, 0.2, 1%, 1 W, 2512	2512	WSL2512R2000FEA	Vishay-Dale
R10	1	365	RES, 365, 1%, 0.125 W, 0805	805	CRCW0805365RFKEA	Vishay-Dale
U1	1		450-mA High-Voltage, Ultralow-IQ, Low-Dropout Regulator, PWP0020D	PWP0020D	TPS7B6750QPWPRQ1	TI
U2, U3	2		300mA Low-Dropout Voltage Tracking LDO, PWP0020D	PWP0020D	TPS7B4253QPWPRQ1	TI

7.3 PCB Layout Recommendations

For the LDO-power supply, especially high voltage and large current ones, layout is important. If not carefully designed, the regulator cannot deliver enough output current because of thermal limitations.

To improve the thermal performance of the device and maximize the current output at high-ambient temperature, use four-layer planes in PCB design, spread the thermal pad as wide as possible, and use plenty of thermal vias on and around the thermal pad.

7.3.1 Layer Prints

To download the layer plots, see the design files at TIDA-00863.

7.4 Altium Project

To download the Altium project files, see the design files at TIDA-00863.

7.5 Gerber Files

To download the Gerber files, see the design files at TIDA-00863

7.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-00863

8 References

1. *TPS7B4253-Q1 300-mA 40-V Low-Dropout Voltage-Tracking LDO With 4-mV Tracking Tolerance* (SLVSCP3)
2. *TPS7B6750-Q1 450-mA High-Voltage Ultra-Low IQ Low-Dropout Regulator* (SLVSCB2)

9 About the Author

JASON LIU is the applications engineer at TI, where he manages the linear regulators applications support in the AVL product line of mixed signal automotive (MSA).

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Revision History A

Changes from Original (November 2015) to A Revision	Page
• Changed block diagram to an updated figure	4

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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