Collin Wells, Jared Becker

TI Designs — Precision: Verified Design

Low-Cost Digital Programmable Gain Amplifier Reference Design

TEXAS INSTRUMENTS

TI Designs — Precision

TI Designs — Precision are analog solutions created by TI's analog experts. Verified Designs offer the theory, component selection, simulation, complete PCB schematic & layout, bill of materials, and measured performance results of useful circuits. Circuit modifications that help to meet alternate design goals are also discussed.

Design Resources

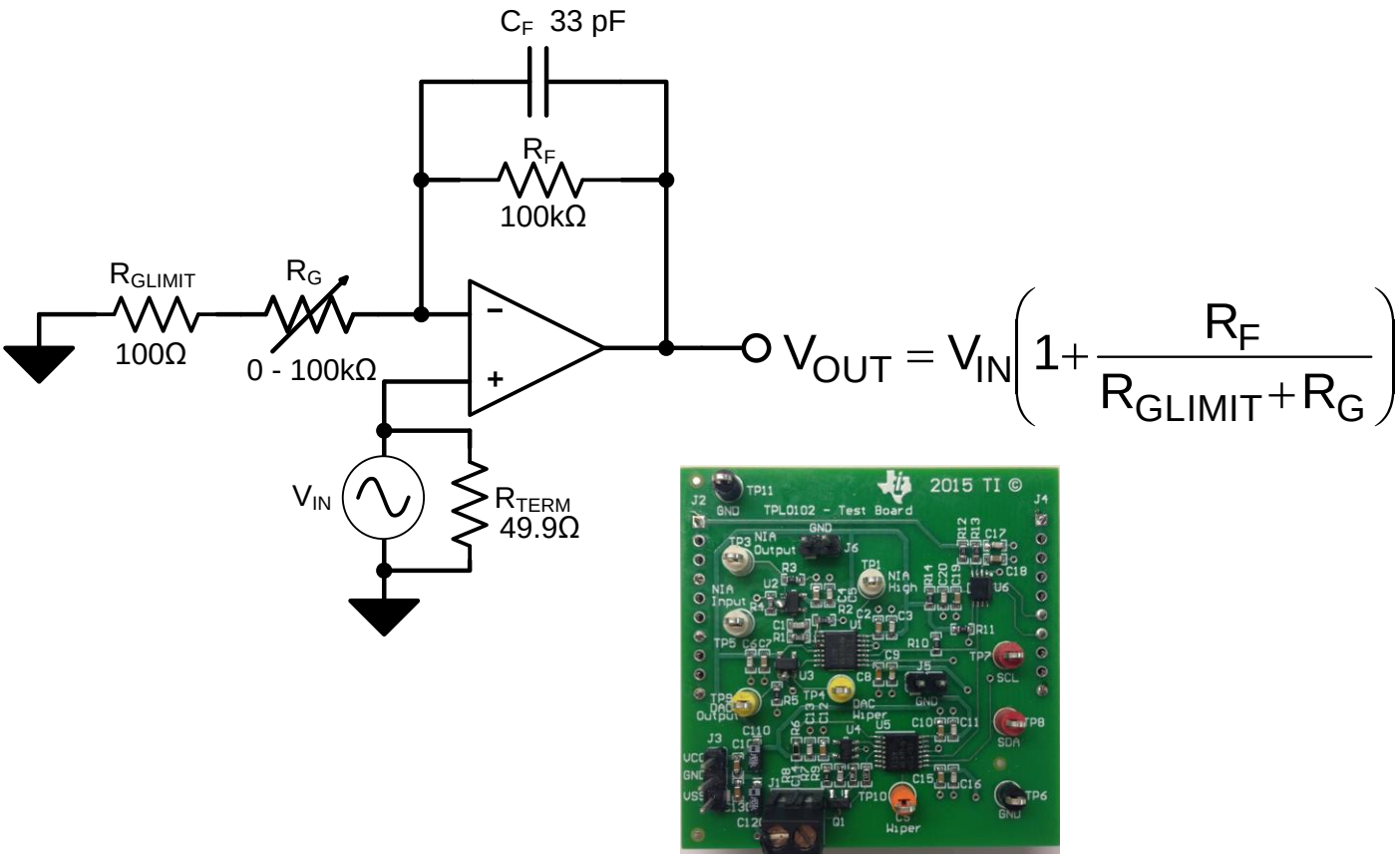
TIPD204	All Design files
OPA316	Product Folder
TPL0102	Product Folder

Circuit Description

This simple and low-cost programmable gain amplifier design creates non-inverting gains ranging from 6dB (2V/V) to 60dB (1000V/V). The design is based on a general purpose op amp and a digital potentiometer as one of the gain-setting elements. The digital potentiometer is controlled with a standard I2C digital interface.

TI E2E™ Community

Ask The Analog Experts
WEBENCH® Design Center
TI Designs - Precision Library



1 Design Summary

The design requirements are as follows:

- Supply Voltage: ±1.3 V to ±2.5 V
- Gain Control: I2C Digital Communication
- Gain Range: 6dB – 60dB (2V/V – 1000V/V)

The design goals and performance for this low-cost digital programmable gain amplifier are summarized in Table 1. Figure 1 depicts the results for the design.

Table 1: Comparison of Design Goals, Calculated, and Measured Performance

Specification	Goals	Calculated	Measured
Gain Range	6dB – 60dB	6dB – 55.9dB	6dB – 55.6dB

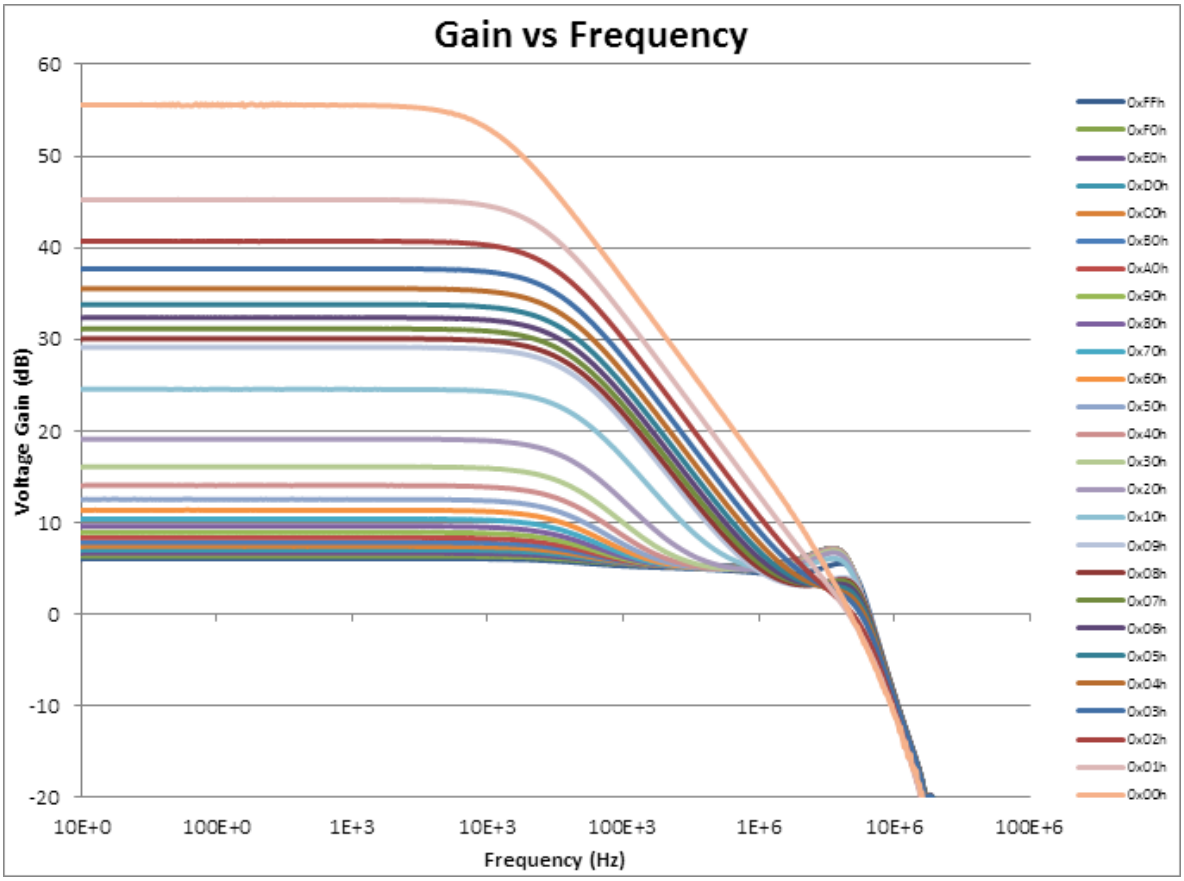


Figure 1: Measured Transfer Function over the Full Range of Input Codes

2 Theory of Operation

A standard non-inverting amplifier is created from an op amp, a feedback resistor, R_F, and an input, or gain-setting resistor, R_G, as shown in Figure 2. The transfer function for this standard op amp building block is shown in Equation 1.

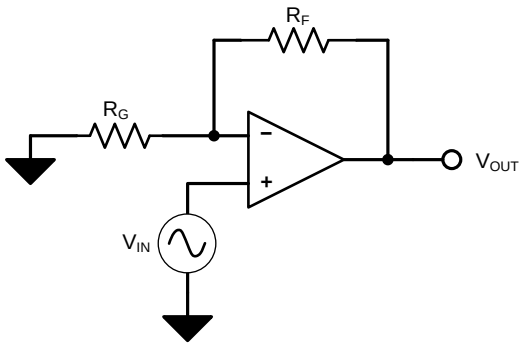


Figure 2: Non-Inverting Amplifier Circuit

$$V_{OUT} = V_{IN} * \left(1 + \frac{R_F}{R_G}\right) \quad (1)$$

To turn the non-inverting amplifier into a digitally controlled programmable gain amplifier, either the R_F or R_G resistance must be variable based on a digital control signal. Figure 3 and Equation 2 display the circuit and transfer function displayed in this design. R_{GLIMIT} is included in the circuit to set the maximum gain in the circuit, preventing an unbounded gain condition as the variable R_G resistance approaches 0 Ω.

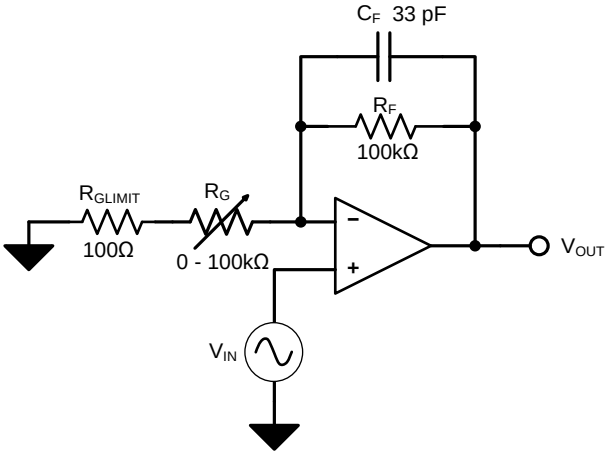


Figure 3: Non-Inverting Programmable Amplifier Circuit Topology

$$V_{OUT} = V_{IN} * \left(1 + \frac{R_F}{R_{GLIMIT} + R_G}\right) \quad (2)$$

For the non-inverting topology it is advantageous to control the R_G resistance for two reasons. First, with a fixed R_F resistance the feedback network resistance remains constant. Therefore, the output current delivered to the feedback network doesn't change with gain and R_F can be configured based on the circuit's current consumption and noise requirements. Second, if a bandwidth limiting capacitor, C_F, is placed into the circuit to limit the bandwidth, the cutoff frequency, $f_{(-3dB)}$, won't vary as the gain changes. The cutoff frequency equation is shown in Equation 3.

$$f_{(-3dB)} = \frac{1}{2\pi R_F C_F} \tag{3}$$

It is important to note that because of the non-inverting topology, the filtering effect will reduce the gain of the circuit down to 1V/V, but will not create a true single-pole filtering effect as created with a feedback capacitor in the inverting topology. This is because at high frequencies the C_F capacitor will short out the R_F resistance resulting in a feedback impedance, Z_F, near 0 Ω. However, based on the transfer function for a non-inverting amplifier the gain will never decrease below 1V/V. This is shown in Equation 4.

$$\text{Gain} = \frac{V_{OUT}}{V_{IN}} = \left(1 + \frac{R_F}{R_{GLIMIT} + R_G}\right) = \left(1 + \frac{0}{R_{GLIMIT} + R_G}\right) = 1V/V \tag{4}$$

3 Component Selection

3.1 TPL0102 Digital Potentiometer

The TPL0102 features two linear-taper potentiometers that are digitally controlled with a standard two-wire I2C communication protocol. The TPL0102 features a resistance range from roughly 0 Ω to 100 kΩ with 256 steps (8-bits). The TPL0102 can be configured as a two-terminal rheostat as used in this application or as a three-terminal potentiometer. A non-volatile memory (EEPROM) is used to store the wiper position between power cycles, returning the wiper to the previously programmed position once power is returned. The device features performance specifications of ≤±0.5 LSBs of integral non-linearity (INL), ≤±0.25 LSBs of differential non-linearity (DNL), and <2LSBs of zero-scale and full-scale errors.

3.2 OPA316 Op Amp

The OPA316 is a low-cost, low-voltage rail-to-rail input/output CMOS op amp. It features a power supply range from 1.8 V to 5.5 V, a unity gain bandwidth of 10 MHz, quiescent current of 400 µA and input noise of 11 nV/√Hz. The input offset voltage is 0.5 mV and input bias current is ±5 pA.

3.3 Passive Component Selection

To achieve the desired gain range from 6dB (2 V/V) to 60dB (1000 V/V) the R_F and R_G are selected based on the resistance range of the TPL0102 digital potentiometer, which is 0 Ω – 100 kΩ. To achieve the low-end gain of 6 dB (2 V/V) the R_F resistor will be selected to be 100 kΩ as shown in Equation 5. The R_{GLIMIT} resistance is assumed to be significantly smaller than the maximum resistance of the TPL0102 (R_{G_MAX}) so it falls out of the equation.

$$\begin{aligned} &\text{Gain} = \frac{V_{OUT}}{V_{IN}} = \left(1 + \frac{R_F}{R_{GLIMIT} + R_{G\_MAX}}\right) = 2V/V \\ &\Rightarrow R_F = \frac{2V/V - 1V/V}{100k\Omega} = 100k\Omega \end{aligned} \tag{5}$$

The R_{GLIMIT} resistance will be set based on the maximum gain goal of 60 dB (1000 V/V) as shown in Equation 6. The R_{G_MIN} resistance of the TPL0102 is ideally 0 Ω.

$$\text{Gain} = \frac{V_{OUT}}{V_{IN}} = \left(1 + \frac{R_F}{R_{GLIMIT} + R_{G\_MIN}}\right) = 1000V/V$$
$$\Rightarrow R_{GLIMIT} = \frac{100k\Omega}{1000V/V - 1V/V} = 99.9\Omega \quad (6)$$

R_{GLIMIT} was selected to be a 100 Ω resistor because it's the closest standard value.

The complete circuit for this design including the selected passive components and the TPL0102 parasitic capacitances is shown in Figure 4.

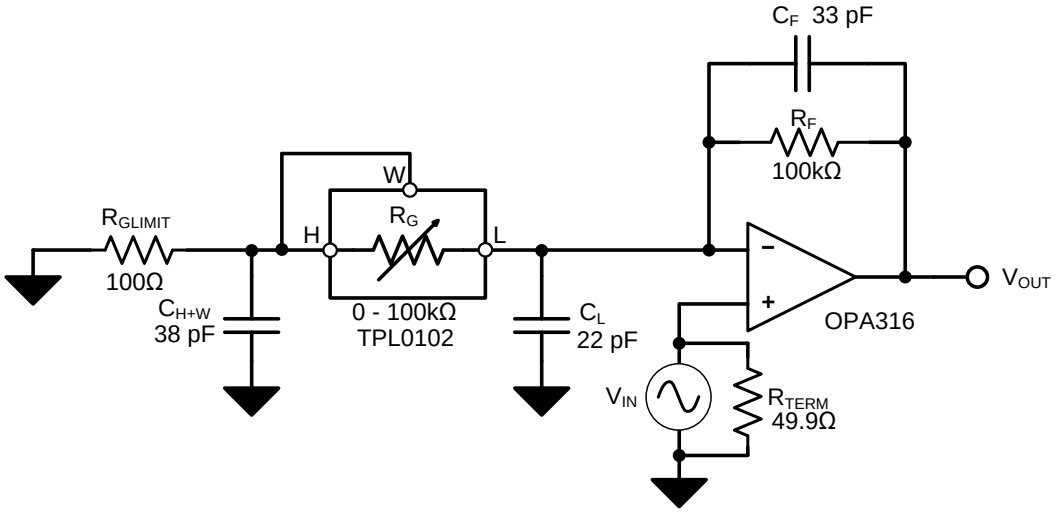


Figure 4: Detailed Programmable Gain Amplifier Circuit Schematic

As shown, the parasitic capacitance of the "L" pin of the TPL0102 is presented directly at the inverting input of the op amp requiring a feedback capacitor to prevent oscillations and other stability issues. As explained in Section 2 and Equation 3, the C_F capacitor also limits the gain-bandwidth of the circuit. The bandwidth limit for this circuit will be set to 50kHz. Therefore, the C_F capacitor was set to 33pF based on the closest standard value to the of the results shown in Equation 7.

$$f_{(-3dB)} = 50kHz = \frac{1}{2\pi R_F C_F}$$
$$\Rightarrow C_F = \frac{1}{2\pi * 100k\Omega * 50kHz} = 31.8pF \quad (7)$$

The R_F and R_{GLIMIT} resistors are selected for 1% tolerance to match the ±2LSB (out of 256) gain accuracy of the TPL0102.

4 Circuit Performance Calculations

The gain accuracy of this design is based on the specifications of the TPL0102 and the accuracy of the passive components selected in Section 3.

The TPL0102 also has some limitations on the range of resistances it produces which will limit the final gain range. The wiper-to-low resistance has a maximum value of 99.61kΩ which sets the minimum gain to a little above 2V/V, as shown in Equation 8.

$$\text{Gain}_{MIN} = \frac{V_{OUT}}{V_{IN}} = \left(1 + \frac{R_F}{R_{GLIMIT} + R_{G\_MAX}}\right) = \left(1 + \frac{100k\Omega}{100\Omega + 99.61k\Omega}\right) = 2.003V/V \quad (8)$$

While the minimum wiper-to-low resistance of the TPL0102 is ideally 0 Ω, the typical terminal resistance is 60 Ω with a maximum value of 200 Ω. This limits the typical R_{G_MIN} resistance to 60 Ω, which limits the maximum gain to 626 V/V or roughly 56 dB as shown in Equation 9.

$$Gain_{MIN} = \frac{V_{OUT}}{V_{IN}} = \left(1 + \frac{R_F}{R_{GLIMIT} + R_{G\_MIN}}\right) = \left(1 + \frac{100k\Omega}{100\Omega + 60\Omega}\right) = 626V/V = 55.9dB \quad (9)$$

5 PCB Design

The PCB schematic and bill of materials can be found in Appendix A.

5.1 PCB Layout

For optimal performance of this design follow standard precision PCB layout guidelines, including proper decoupling close to all mixed signal integrated circuits and providing adequate power and GND connections with large copper pours.

The layout for the TIPD204 design is shown in Figure 5.

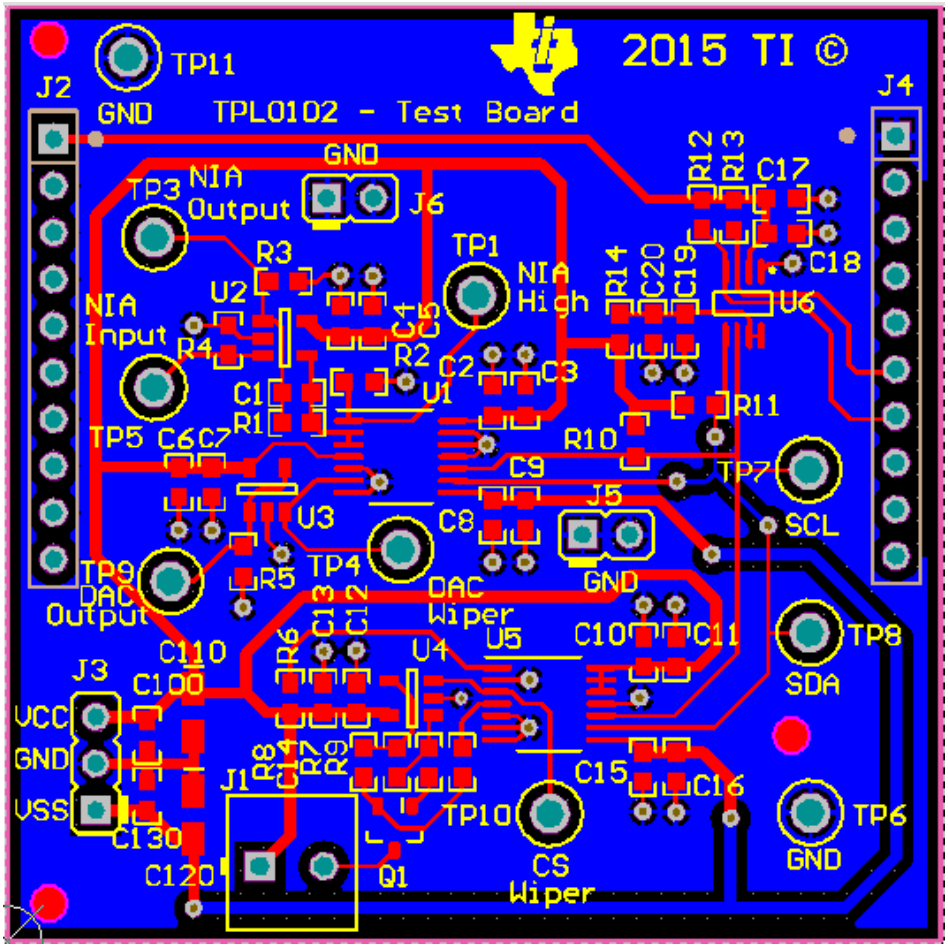


Figure 5: Altium PCB Layout

Note that this PCB is also used for TIPD205 and TIPD206 which is why there are some extra components not described in this document. Refer to the Bill of Materials to understand which components are used in TIPD204.

6 Verification and Measured Performance

The measured transfer function over the full range of input code values is shown in Figure 6. The minimum gain is 6dB and the maximum gain is 55.6dB as expected based on the calculations in Section 4.

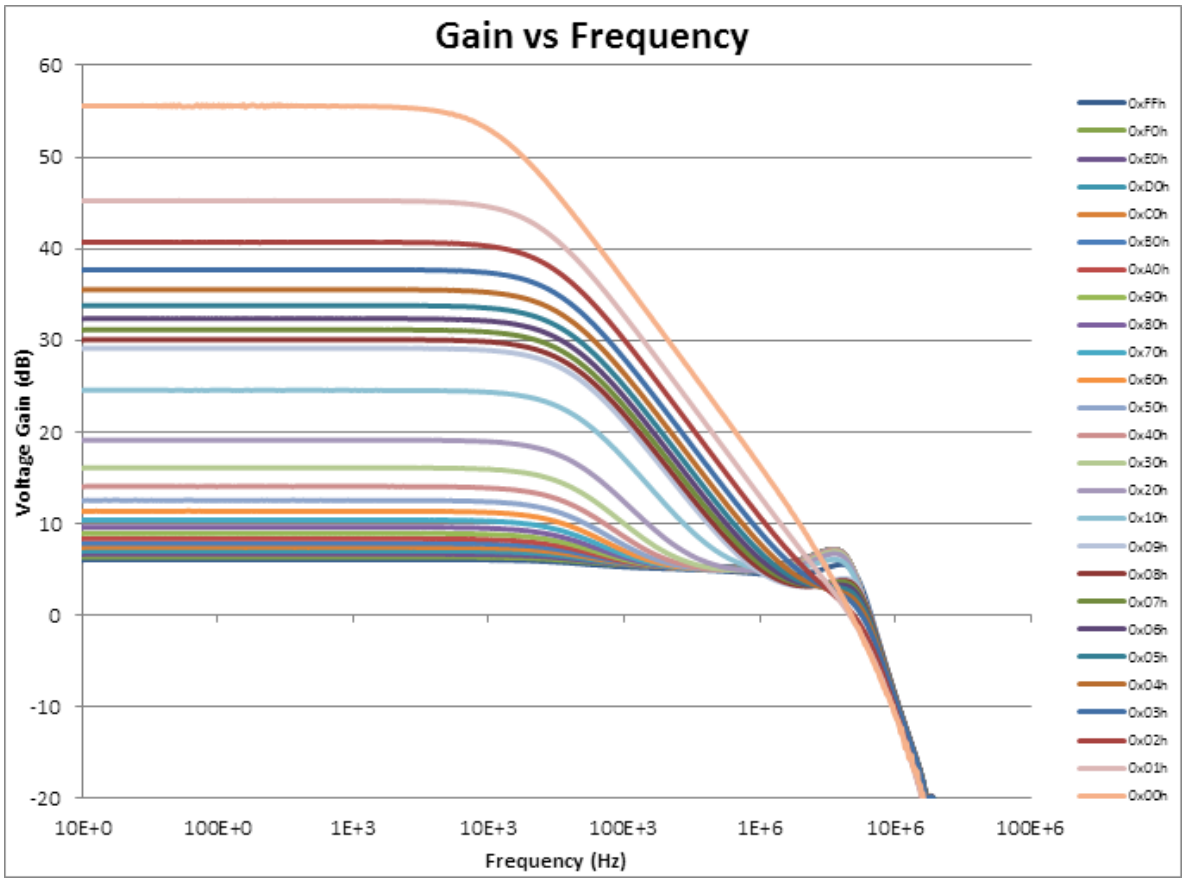


Figure 6: Calibrated Output Current Error vs. RTD Temperature

6.1 Measured Result Summary

The measured performance is summarized and compared with the goals and calculated values in Table 2.

Table 2: Comparison of Design Goals, Simulated, and Measured Performance

Specification	Goals	Calculated	Measured
Gain Range	6dB – 60dB	6dB – 55.9dB	6dB – 55.6dB

7 Modifications

There are a few additional digital potentiometers that could be used to achieve similar designs to the one featured in TIPD204. They are listed in Table 3.

Table 3: Alternative Digital Potentiometers

Part Number	Resolution	Resistance Range	Channels	Smallest Package
TPL0102	8 bits	0 – 100kΩ	2	QFN-14
TPL022	8 bits	0 – 10kΩ	2	WQFN-16
TPL0501	8 bits	0 – 100kΩ	1	8SOT-23

Since this design is for a basic circuit building block, there are many other op amp options that would be good candidates for this design depending on the design goals. Designs requiring higher levels of DC accuracy would benefit from the lower offset voltages and drifts featured in zero-drift (chopper) devices. A few other options are listed in Table 4.

Table 4: Alternative Op Amps

Part Number	Bandwidth	Offset Voltage	Noise	Quiescent Current	Smallest Package
OPA316	10 MHz	500 µV	11nV/√Hz	400 µA	SC70-5
OPA317	0.3 MHz	90 µV	55nV/√Hz	21 µA	SC70-5
OPA313	1 MHz	2500 µV	25nV/√Hz	50 µA	SC70-5
OPA314	3 MHz	2500 µV	14nV/√Hz	150 µA	SC70-5

8 About the Authors

Collin Wells is an applications engineer in the Precision Linear group at Texas Instruments where he supports industrial products and applications. Collin received his BSEE from the University of Texas, Dallas.

Jared Becker is in the Applications Rotation Program at Texas Instruments where he supports System Connectivity products and the Centralized Application Team. Jared received his BSEE from Arizona State University.

Appendix A.

A.1 Electrical Schematic

The Altium electrical schematic for this design can be seen in Figure 7.

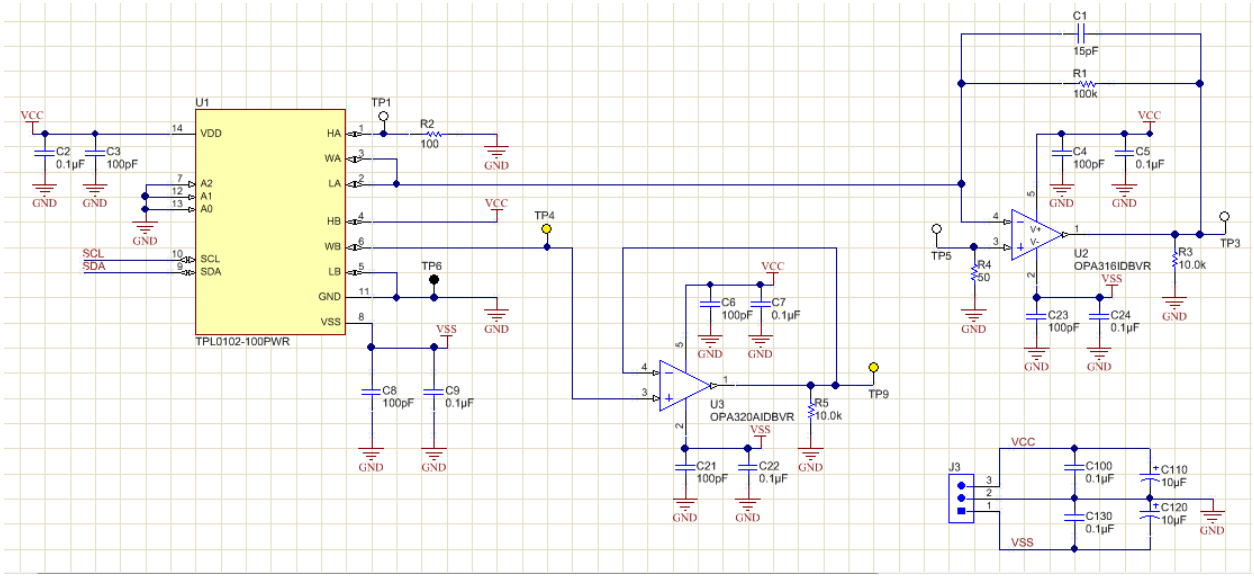


Figure 7: Altium Schematic

A.2 Bill of Materials

The bill of materials for this circuit can be seen in Figure 8.

Texas Instruments

Bill of Materials

TI DESIGNS
TIPD204 - TPL0102 Applications

Item #	Quantity	Designator	Value	Description	Manufacturer	Part Number
1	1	C1	33pF	CAP CER 33PF 50V NP0 0603	MuRata	GRM1885C1H330JA01D
2	9	C2, C5, C7, C9, C17, C19, C24, C100, C130	0.1uF	CAP, CERM, 0.1 µF, 25 V, +/- 5%, X7R, 0603	Kemet	C0603C104J3RAC
3	7	C3, C4, C6, C8, C18, C20, C23	100pF	CAP, CERM, 100 pF, 25 V, +/- 10%, X7R, 0603	AVX	06033C101KAT2A
4	2	C110, C120	10uF	CAP, TA, 10 µF, 6.3 V, +/- 10%, 3.4 ohm, SMD	Vishay-Sprague	293D106X96R3A2TE3
5	2	J2, J4		Receptacle, 100mil, 10x1, Tin, TH	Sullins Connector Solutions	PPTC101LFBN-RC
6	1	J3		Header, 2.54 mm, 3x1, Gold, TH	Sullins Connector Solutions	GBC03SAAN
7	2	J5, J6		Header, 2.54 mm, 2x1, Gold, TH	Sullins Connector Solutions	GBC02SAAN
8	1	R1	100k	RES, 100 k, 1%, 0.1 W, 0603	Yageo America	RC0603FR-07100KL
9	1	R2	100	RES, 100, 1%, 0.1 W, 0603	Yageo America	RC0603FR-07100RL
10	2	R3, R5	10.0k	RES, 10.0 k, 1%, 0.1 W, 0603	Vishay-Dale	CRCW060310K0FKEA
11	1	R4	49.9	RES SMD 49.9 OHM 1% 1/10W 0603	Yageo America	RC0603FR-0749R9L
12	2	R10, R11	1.54k	RES, 1.54 k, 1%, 0.1 W, 0603	Vishay-Dale	CRCW06031K54FKEA
13	2	R12, R13	1.02k	RES, 1.02 k, 1%, 0.1 W, 0603	Vishay-Dale	CRCW06031K02FKEA
14	1	R14	200k	RES, 200 k, 1%, 0.1 W, 0603	Vishay-Dale	CRCW0603200KFKEA
15	3	TP1, TP3, TP5		Test Point, Compact, White, TH	Keystone	5007
16	2	TP4, TP9		Test Point, Compact, Yellow, TH	Keystone	5009
17	1	TP6		Test Point, Compact, Black, TH	Keystone	5006
18	2	TP7, TP8		Test Point, Compact, Red, TH	Keystone	5005
19	1	U1		IC DGTL POT 256POS 100K 14TSSOP	Texas Instruments	TPL0102-100PWR
20	1	U2		IC OPAMP GP 10MHZ RRO SOT23-5	Texas Instruments	OPA316IDBVR
22	1	U6		Dual Bi-Directional I2C-Bus and SMBus Voltage Level-Translator, 0 to 5.5 V, -40 to 85 degC, 8	Texas Instruments	PCA9306DCTR

Figure 8: Bill of Materials

IMPORTANT NOTICE FOR TI REFERENCE DESIGNS

Texas Instruments Incorporated ("TI") reference designs are solely intended to assist designers (“Buyers”) who are developing systems that incorporate TI semiconductor products (also referred to herein as “components”). Buyer understands and agrees that Buyer remains responsible for using its independent analysis, evaluation and judgment in designing Buyer’s systems and products.

TI reference designs have been created using standard laboratory conditions and engineering practices. **TI has not conducted any testing other than that specifically described in the published documentation for a particular reference design.** TI may make corrections, enhancements, improvements and other changes to its reference designs.

Buyers are authorized to use TI reference designs with the TI component(s) identified in each particular reference design and to modify the reference design in the development of their end products. HOWEVER, NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY THIRD PARTY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT, IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI REFERENCE DESIGNS ARE PROVIDED "AS IS". TI MAKES NO WARRANTIES OR REPRESENTATIONS WITH REGARD TO THE REFERENCE DESIGNS OR USE OF THE REFERENCE DESIGNS, EXPRESS, IMPLIED OR STATUTORY, INCLUDING ACCURACY OR COMPLETENESS. TI DISCLAIMS ANY WARRANTY OF TITLE AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, QUIET ENJOYMENT, QUIET POSSESSION, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS WITH REGARD TO TI REFERENCE DESIGNS OR USE THEREOF. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY BUYERS AGAINST ANY THIRD PARTY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON A COMBINATION OF COMPONENTS PROVIDED IN A TI REFERENCE DESIGN. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, SPECIAL, INCIDENTAL, CONSEQUENTIAL OR INDIRECT DAMAGES, HOWEVER CAUSED, ON ANY THEORY OF LIABILITY AND WHETHER OR NOT TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES, ARISING IN ANY WAY OUT OF TI REFERENCE DESIGNS OR BUYER’S USE OF TI REFERENCE DESIGNS.

TI reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques for TI components are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

Reproduction of significant portions of TI information in TI data books, data sheets or reference designs is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards that anticipate dangerous failures, monitor failures and their consequences, lessen the likelihood of dangerous failures and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in Buyer’s safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed an agreement specifically governing such use.

Only those TI components that TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components that have ***not*** been so designated is solely at Buyer's risk, and Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265