TI Designs
70V WLED Drive with Dimming Control and Thermal Scale-back

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OPA4374	Product Folder
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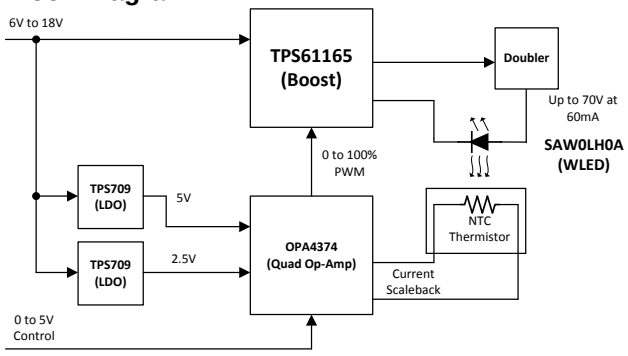
Block Diagram



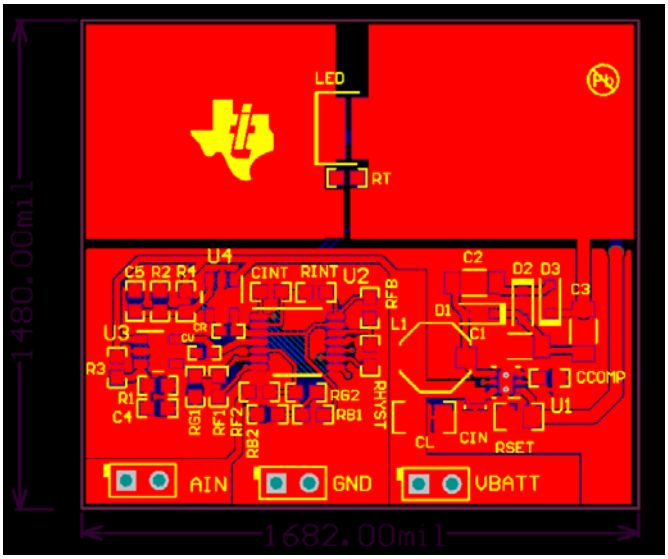
Design Features

- 6V to 18V DC Input Voltage Range
- 60mA max LED current at 70V
- 440 Lumens Light Output
- >90% Efficient
- Automatic Current Scale Back For High Temperatures
- Voltage Controlled Dimming for interfacing with Potentiometers or DAC's
- Operating Temperature Range -40C to 85C
- Noise Free Dimming Control

Featured Applications

- Landscape Lighting
- Flashlights
- Automotive Lighting
- Industrial Lighting

Board Image



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1 Introduction

Inductive boost white LED drivers are the standard method for driving LEDs. For simple single string LED drivers, the LED current is regulated by the inductive boost's feedback loop. This feedback loop regulates a voltage across an external low side resistor (LED cathode to GND), thus developing a current (VFB/R). The maximum LED voltage is limited by the LED drivers over voltage threshold (OVT). The maximum LED current is limited by the LED driver's peak current rating, and/or the VIN to VOUT ratio. The LED current is typically changed by a varying duty cycle (PWM control).

Typical boost converters for driving LEDs are often limited to output voltages of <40V due to the voltage limitations of their integrated MOSFET. An internal protection circuitry is added to the LED driver to keep the output voltage below the absolute maximum rating of the switch (Over Voltage Protection, or OVP). This OVP circuitry prevents driving LED's (or series string of LEDs) that are higher than the OVP threshold. To overcome this limitation, an external voltage doubler can be added to the boost output. By adding this voltage doubler, the maximum output voltage that the boost can attain is essentially doubled (to OVPx2). This enables the driving of much higher voltage LEDs which can offer the ability to power LEDs with more lumens per die area.

The objective of this reference design is to demonstrate a boost + voltage doubler that drives a 70V white LED for general lighting applications with currents up to 60mA. The design also shows the implementation of a quad operational amplifier which generates a 2.5% to 100% PWM waveform from an analog input (0 to 4.55V). This PWM waveform is then used to provide the dimming signal into the LED drivers dimming input. The operational amplifier also takes feedback from a thermistor which is then used to provide current scale back to prevent over heating in the LED.

2 Key System Specifications

Table 1. Key System Specifications

Parameter	Specification and Features
LED Current Range	1.5mA to 60mA
VIN Range	6V to 18V
VOUT Range	12V to 73.5V
Input Current Requirements	<1A
Operating Temperature Range	-40C to 85C
Generated PWM Frequency	10kHz
PWM Input Duty Cycle Resolution	>8 Bits
Generated PWM Duty Cycle Range	2.6% to 100%
Analog Dimming Input Voltage Range	0 to 5V
Analog Input Resolution	<20mV
Maximum Fold Back Current	30mA
Boost Switching Frequency	1.2MHz
Form Factor (L x W x H)	1.48mm x 1.68mm

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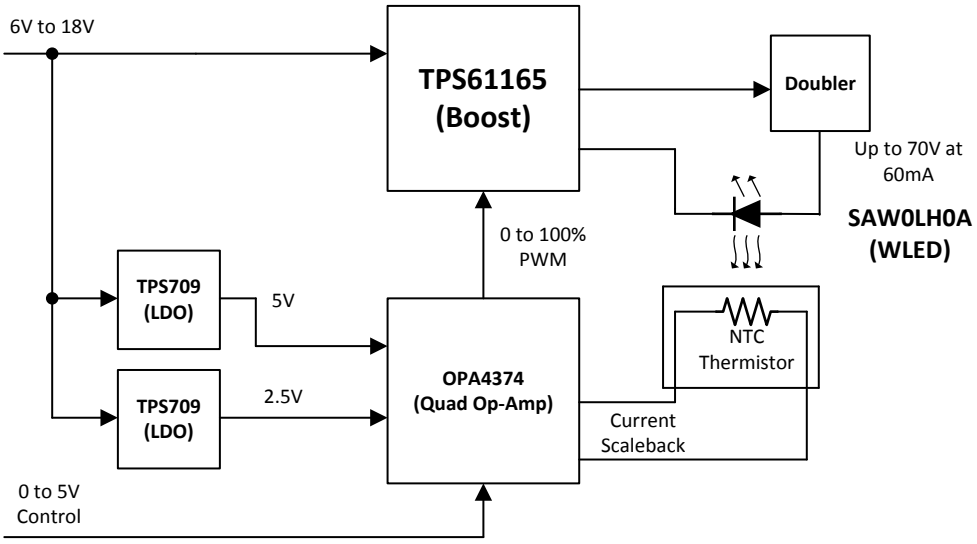

Figure 1. Block Diagram

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3 System Description

3.1 TI Device 1 (TPS61165 WLED Driver)

The boost LED driver + voltage doubler is the main component in the design. The boost used is the TPS61165 white LED driver while the voltage doubler is composed of Schottky diodes D2 and D3 and capacitors C2 an dC3. The schematic is shown in figure 2.

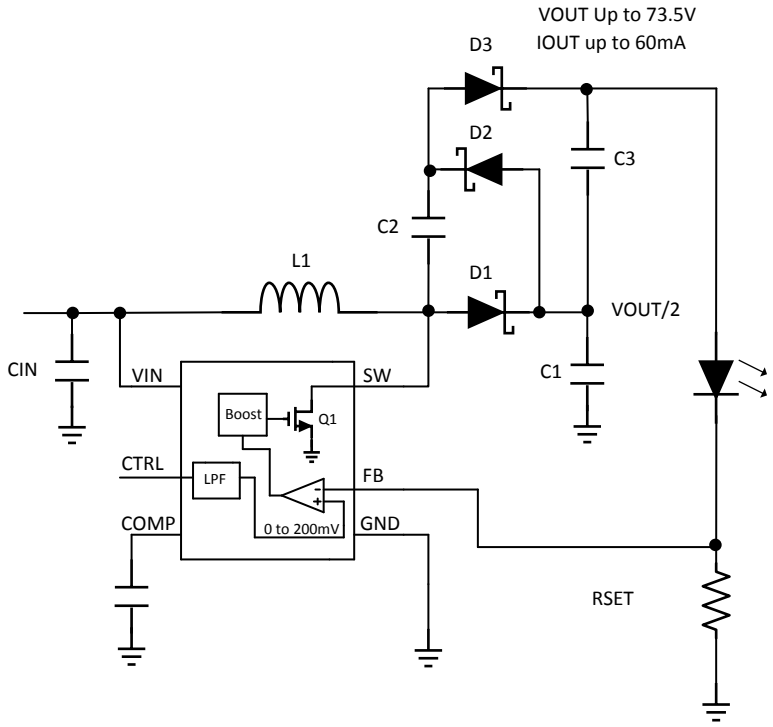

Figure 1: Boost + Voltage Doubler

The operation of the boost + doubler is shown in figure 3 and described in 1 through 5 below:

1. The boost drives the voltage across C3 so that the current through RSET makes FB regulate to the control voltage of 200mV.
2. During the Q1 on time SW pulls to GND causing C2 to charge up to VC1 through D2.
3. When Q1 turns off the inductor causes the SW voltage to raise up until D1 is turned on. This brings SW up to VC1 causing D3 to turn on and forcing VC3 to VC1 + VC2 = 2×VC1. The output of the circuit (voltage across C3) is always 2X the voltage across C1.
4. The average peak current through D1 and D3 are equal and are both ILED/(1-D).
5. The average peak current through D2 is ILED/D.
6. The input current is 2X the average peak current through either D1 or D3 (2xILED/(1-D)).

This circuit duty cycle is lower than with a standard boost operating at the same voltages. In a standard boost the duty cycle is D1 = (VOUT – VIN×e)/VOUT. In the boost + doubler the conversion ratio is D2 = (VOUT – 2×VIN×e)/VOUT. The doubler provides for a cuts the conversion ratio in half compared to a boost without doubler at the same output voltage. This doubler cuts the duty cycle by a factor of $G = \frac{(VOUT - VIN \times eff)}{(VOUT - 2 \times VIN \times eff)}$.

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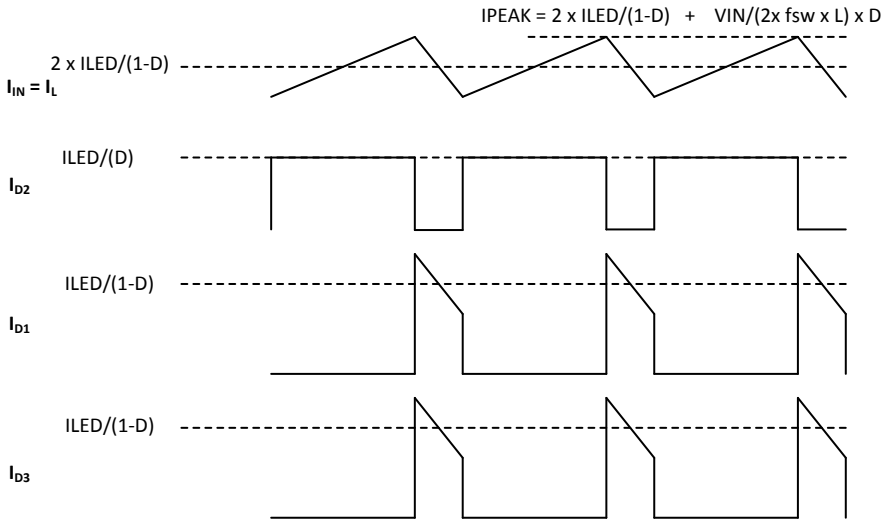
The boost + doubler has three main advantages. First, it enables higher boost converter ratios (VOUT/VIN) that would normally not be allowed due to max duty cycle limitations in a boost. Second, it allows for higher output voltages that would not be allowed due to OVP limitations of a typical boost. Third, the boost + doubler provides for a higher efficient solution since the switch voltage is cut by a factor of 2, which results in the switching power losses that are dependent on $VOUT^2$ to be cut by a factor of 4X.



VIN x IIN x efficiency = VOUT x ILED

VIN x [2 x ILED/(1-D)] x efficiency = VOUT x ILED

D = (VOUT – 2 x VIN x efficiency)/VOUT

Figure 3: Boost + Doubler Waveforms

Boost + Doubler Maximum Output Power

The maximum output power is dependent on two factors:

1. The max output voltage capability of the TPS61165 + Doubler
2. The peak current limit of the TPS61165

Maximum Output Voltage

The maximum output voltage supported by the TPS61165 + doubler circuit is given by:

$$V_{OUTMAX} = V_{OVPMIN} \times 2 - V_{D3}$$

V_{OVPMIN} is 37V and V_{D3} is around 0.5V. This gives a max working output voltage of 73.5V.

In the design, the LED (SAW0LH0A from Seoul Semiconductor) has a specified tolerance in VLED at 20mA of (60V min, 63V typ, and 68V max) at 25C. This is (-5% and +7.9%) and we will assume this same tolerance applies to VLED at any LED current.

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Since the highest output voltage we can regulate is 73.5V (due to OVP limitations) the typical VLED for a max of 73.5V is then (73.5V – 7.9% = 68V). Using bench data of typical VLED vs current (figure 7), we get an ILED of 42.4mA with VLED at 68V. This is the max ILED we can specify based on OVP limitations.

Current Limit

The TPS61165's current limit has a minimum specification of 0.96A. This sets the peak operating inductor current. For the boost + doubler the peak operating inductor current is given by:

$$I_{PEAK} = 2 \times I_{OUT\_MAX} \times \frac{\frac{VOUT}{2}}{VIN \times e} + \frac{VIN}{2 \times fsw \times L} \times \frac{\frac{VOUT}{2} - VIN \times e}{\frac{VOUT}{2}}$$

Based on OVP limitations the max possible voltage is 73.5V at 42.4mA. Allowing for min/max tolerances we get the following:

1. VIN_MIN = 6V
2. VOUT_MAX = 73.5V
3. ILED_MAX = 42.4mA
4. fsw_min = 1MHz (1.2MHz +/-20%)
5. L_min = 8uH (10uH +/-20% from inductor datasheet)
6. e = 83% (estimate using bench data and some margin)

Based on these tolerances the peak operating inductor current is IPEAK = 0.95A. This is just below the peak current limit of the TPS61165.

Inductor Selection

The inductor must have a peak current rating that satisfies the peak operating current of the application (see previous section). The inductor recommended in the parts table (LTF5022T-100M1R4-LC) has a peak current rating of 1.4A min. This is sufficient for the application. This inductor also has a low DC resistance which allows for maximum possible efficiency for the application.

Output Capacitance

The output capacitance required by the application is provided by capacitors C1, C2 and C3. These are all nominal 4.7uF (50V). C1 and C3 are connected in series and give a total output (nominal) capacitance of 2.35uF at OUT. The two main concerns with the output capacitors are:

1. Having a capacitor voltage rating that is high enough for the application
2. Having a total capacitance that is high enough for stable operation

For the application, the maximum voltage C1, C2, or C3 will see is 73.5V/2 = 36.75V. A 50V ceramic is chosen because of this. For stability, the total output capacitance for C1 must be > than 0.5uF, this must account for tolerance, temperature coefficient, and DC bias degradation. The Chosen capacitor for C1, C2, and C3 is the C3216X5R1H475K (TDK). This has a tolerance of +/-10%, a temperature coefficient of +/-15%, and a DC bias degradation of -70% at 35V. Due to all these factors, the min capacitance for C1 could be as low as:

4.7uF × (1 - 0.1) × (1 - 0.15) × (1 – 0.7) = 1.07uF.

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This gives a total output capacitance (min) of 1.07uF/2 = 0.539uF, which is sufficient for stability.

Schottky Diodes
Diodes D1, D2, and D3 must all be Schottky diodes. This is due to their fast recovery time. Non-Schottky diodes are typically too slow and can lead to efficiency loss. The chosen diode for the application is the B0540WS-7 from Diodes Inc. This diode has 40V max reverse voltage and low forward voltage drop of typically 340mV at 60mA.

The 40V reverse voltage blocking requirement is the most important parameter since each diode will need to block a potential max voltage of 39V (max OVP spec of the TPS61165).

PWM Dimming
The TPS61165's CTRL input is used for PWM dimming. The PWM input frequency range is from 5kHz to 50kHz. The TPS61165 incorporates an internal level shifter and low pass filter which filters the logic level PWM input waveform to a DC voltage and applies this filtered DC to the control loop of the TPS6115's boost. The average value of the level shifted and filtered PWM input becomes the target reference voltage for feedback. The boost will then regulate VOUT such that the target FB voltage is the same as the rference voltage. Having the external resistor (RSET) from FB to GND sets the LED current at VFB/RSET.

The maximum LED current is set by the TPS61165's maximum FB voltage (200mV) divided by RSET. For this application RSET is a 3.3 Ohm (1%) resistor. This gives a maximum current of 60.6mA with the CTRL pin at a logic high (100% duty cycle). As the CTRL input duty cycle is lowered, the FB voltage is lowered linearly. The internal PWM filter has a corner frequency of around 2kHz. To ensure there is enough attenuation of the PWM signal the PWM frequency is chosen around 10kHz. This provides for enough attenuation at FB such that the peak to peak ripple at the boost + doubler output is < 60mV. This eliminates any audible noise due to the piezoelectric effect of the ceramic output capacitor.

3.2 TI Device 2 (OPA4374 Quad Op-Amp)

The OPA4374 quad operational amplifier is used to convert an analog control voltage (0 to 4.55V) to a PWM control dimming waveform. The analog control voltage is multiplied with a thermistor (temperature) feedback which provides for automatic current reduction during high LED temperature conditions. Figure 4 shows the schematic for the quad op-amp.

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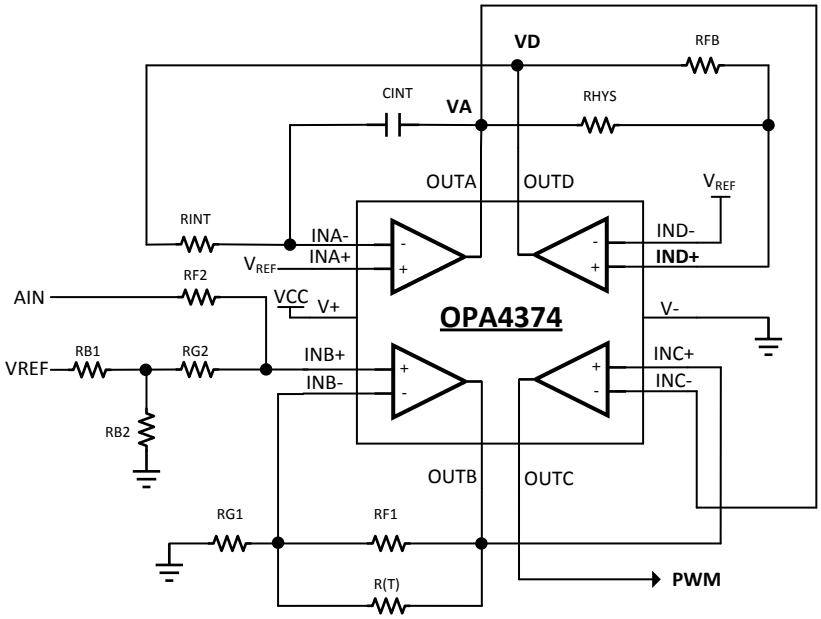

Figure 4. A2PWM Schematic

OP-Amp A and Op-Amp D

Amplifier A and D build a triangle waveform. A is configured as an integrator while D is configured as a Schmitt trigger.

Referring to figure 4 and 5, if OUTD voltage starts out low, OUTA voltage will ramp linearly towards VCC until the voltage at IND+ reaches VREF. When IND+ reaches VREF, OUTD and IND+ step up to VCC. This causes VA to turn around and start to ramp down to zero. When INA- reaches VREF, OUTD and IND+ both step down to GND. This creates the triangle waveform output at OUTA. The voltage excursion of OUTA is controlled by the hysteresis of the Schmitt trigger (VHYS = OUTD × RHYS/RFB), where OUTD swings between close to 0 and VCC due to the rail to rail outputs of the amplifier.

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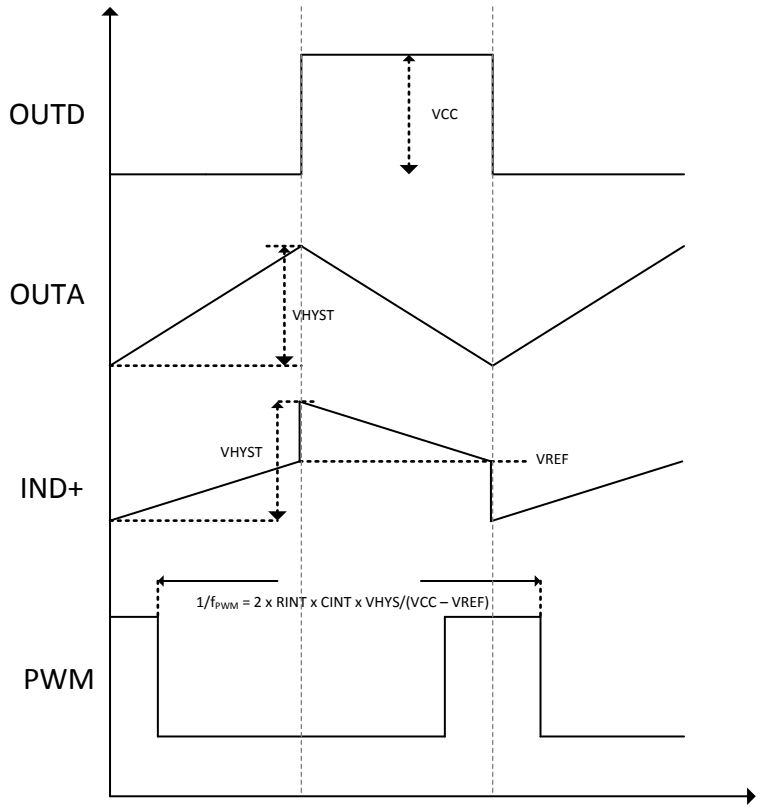

Figure 5. A2PWM Voltage Waveforms

The linear slope of OUTA is controlled by both the hysteresis of the Schmitt trigger, and RINT, CINT. Since the voltage at INA+ is fixed at VREF, the charging current into CINT is given as (OUTD – VREF)/RINT = CINT × ΔV/Δt. ΔV is the hysteresis of the Schmitt trigger and Δt is ½ the PWM period. This gives a PWM frequency of:

$$\frac{1}{f_{PWM}} = 2 \times RINT \times CINT \times \frac{VHYS}{VCC - VREF}$$

In the design, VCC is fixed at 5V and VREF is 2.5V. RHYST is 9.1kΩ and RFB is 10kΩ, thus giving a hysteresis of 4.55V. RINT is 10kΩ and CINT is 2700pF. This gives a PWM frequency of around 10kHz. The slew rate of the Op-amp output (5V/µs) has a slight effect on the linearity of the duty cycle vs AIN voltage at low duty cycles. This is mitigated by adding an offset to the input stage amplifier Op-Amp B (see next section).

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Op-Amp B

Input Stage

Amplifier B is configured as a non-inverting gain amplifier. Its gain is set by the following:

$$(VINB^{+}) \times (1 + \frac{RF1//R(T)}{RG1})$$

The Voltage at VINB+ is a divided down and offset version of the analog input control voltage (AIN). Resistors RF2 (200kΩ) and RG2 (200kΩ) divide down the AIN control voltage and compensate for the gain of 2 provided by Amplifier B.

The resistors RB1 and RB2 divide down VREF and provide an offset to amplifier B's output of around 300mV when AIN is 0 (RB1 = 10kΩ and RB2 = 1.37kΩ). This forces the output of Op-Amp C to have an approximate 2.6% duty cycle PWM duty cycle with AIN set to 0. Adding this offset eliminates issues with the TPS61165's single wire interface (1-Wire, which shares the same input as the PWM). This 1-Wire interface can get triggered and turned on if the PWM waveform is toggling between a logic high and low voltage. This can happen at very low duty cycles due to the slew rate of the op-amp and any movement on the AIN voltage. This could force the LED current to glitch between 0 and full scale due to the 1-Wire interface turning on. Adding the offset duty cycle forces the TPS61165 to always turn on in a fixed state which forces the CTRL input into a definate logic state and prevents the 1-Wire from taking over brightness control.

The offset is done via dividing down VREF through RB1 and RB2. Since RB2 is << (RF2 + RG2), it has minimal effect of the resistive divider for AIN (RF2 and RG2). The total gain from AIN to OUTB is then approximately:

$$\left(\frac{AIN}{2} + 0.15V\right) \times (1 + \frac{5k//R(T)}{5k})$$

Thermistor Feedback

The non-inverting amplifier configuration allows for adding a thermistor (R(T)) in the feedback path such that the PWM output duty cycle has a roll off at higher temperature. This is intended to keep the LED operating within its maximum die temperature range (125°C). The NTC thermistor (Negative Temperature Coefficient) was chosen since it can be made to have a nice roll off at a predetermined temperature.

NTC thermistors by themselves have a decreasing resistance vs temperature that is approximated by the equation:

$$R(T) = R0 \times e^{\left(\beta \times \left(\frac{1}{T} + \frac{1}{T0}\right)\right)}$$

R0 is the nominal NTC resistance (usually at 25C)
β is the thermistor constant
T is the thermistor temperature in Kelvin
T0 is the thermistor temperature at resistance R0 in Kelvin (298K)

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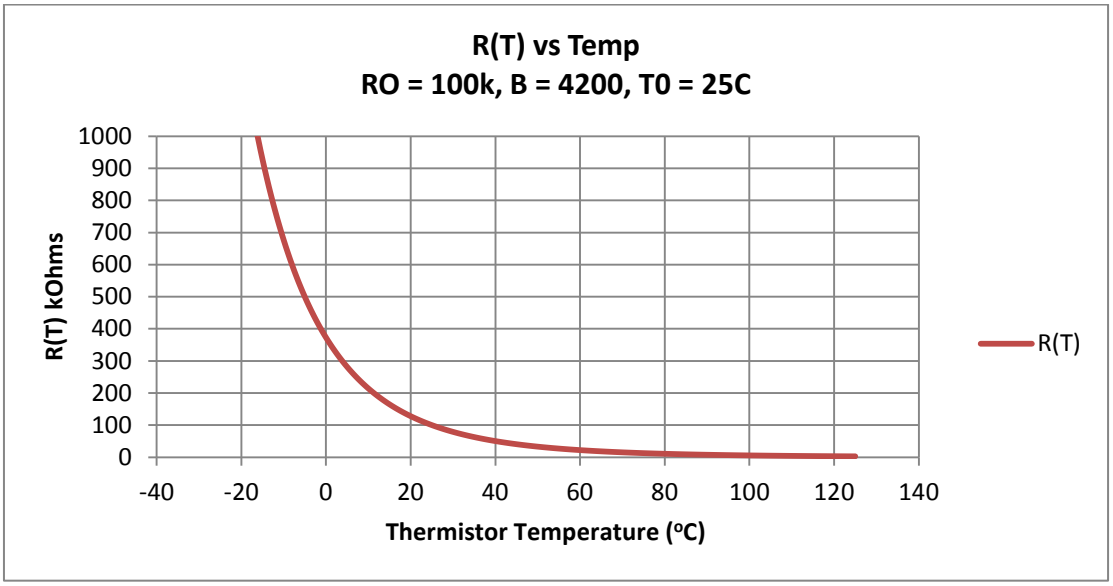

Figure 6. NTC Thermistor Resistance vs Temperature

The typical non-linearity of a thermistor gives the response vs temperature shown in figure 6. This is not by itself very useful since R(T) vs temperature is very non-linear and usually does not occur near the temperature of interest (125C). Adding a parallel fixed resistor (RF1) modifies the response such that it is more useful in the application. This results in a equivalent resistance RP shown in figure 7.

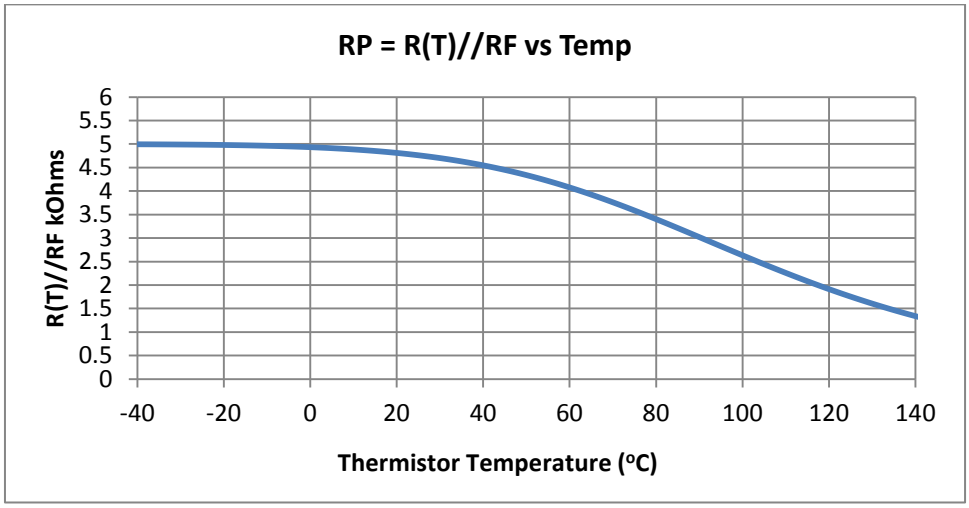

Figure 7. Modified Thermistor Response

For the non-inverting amplifier feedback of Op-Amp B the response of RP is made to give a very high resistance for temperatures below the knee of the modified roll off. and a relatively sharp roll-off above a predetermined temperature. This allows for a relatively constant resistance (and gain) up until the fold back in current must start taking effect.

In the design, a 100kΩ nominal thermistor with an RF1 of 5kΩ gives a parallel equivalent RP of 4.76kΩ. This has little effect on the gain (and thus duty cycle) for T below around 40C. As the temperature starts increasing in the thermistor above 40C, the roll off in RP reduces the gain of op-amp B, and thus the duty cycle at op-amp C's output. The maximum slope occurs at the point where

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R(T) = RF1. Choosing RF1 = R(T = 100C) can be a good design criteria since this ensures that the maximum slope happens before the max allowable LED junction temp (125C).

Current Fold-Back Operation

Measuring the PWM output duty cycle vs increasing ambient temperature gives the plot of figure 8. This plot was taken with D set at 95% (at TA = 25C), and Op Amp C's output disconnected from the TPS61165. The plot shows a flat duty cycle from -40C up to around 40°C. Above 40°C the duty cycle begins to scale back increasingly faster until 60°C. At 60°C the decrease in duty cycle vs temp has a slope of approximately 0.4125%/°C. In terms of LED current, this equates to a reduction in LED current with temperature of approximately 0.248 mA/°C.

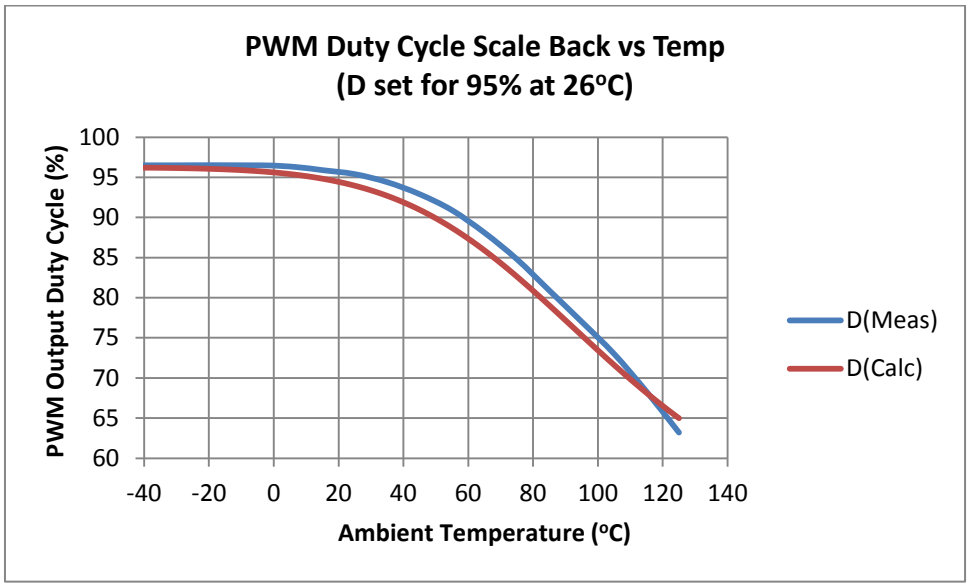

Figure 8. PWM Duty Cycle Scale-Back vs Temp

Error due to Temperature Gradients

Since the thermistor does not share the same die as the LED the thermistor temperature will always be less due to thermal gradients between the two devices. In the design, this gradient was measured by first characterizing the LED's temperature to voltage coefficient in a non-self-heating condition (see Figure 9). The change in VLED from TA = 25°C to TA = 125°C showed the following temperature coefficient:

(75V – 69.6V)/(24.5C – 127.5C) = -52.2mV/C

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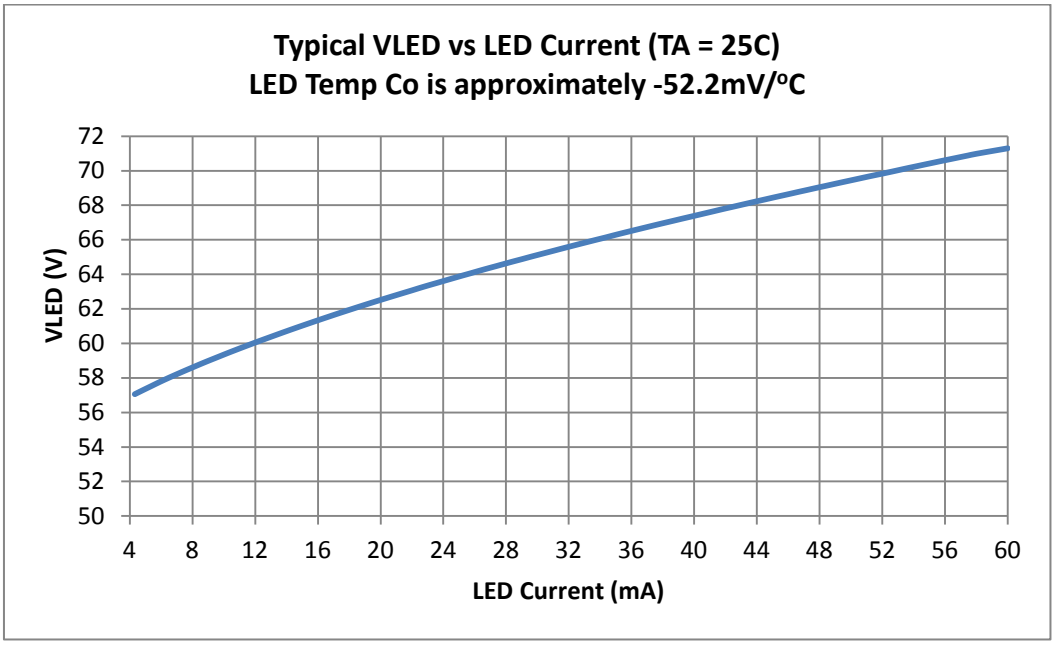

Figure 9. Typical VLED vs Current (SAW0LH0A from Seoul Semiconductor)

The coupling between the LED and the thermistor was then measured (at TA = 25°C with ILED set to 57.4mA, D = 95.6%) As the LED heated up the thermal scaleback forced the duty cycle lower. After a steady state LED temperature was reached, the duty cycle had been reduced from 95.6% initially at T(thermistor = 25C) to 83.9% at T(thermistor_final). During this time, the LED voltage had dropped from 75V (at TLED = 25C) to 70.1V (at TLED = T(thermistor_final). Based on the data in figure 9 the change in VLED indicated a final LED temperature of 119°C, (25°C+ 4.9V/52.2mV/°C = 118.9°C). Using the measured duty cycle vs temperature curve from figure 8, this indicated that the thermistor was reading a temp of 77°C. The delta from LED to thermistor was then estimated at 42°C.

This test also estimated the thermal resistance of the LED pad as:

ΔT(LED)/LED Power = Theta j-a. Or 93.9°C/(70.1V $\times$ 60mA) = 22.3°C/W.

With this Theta j-a, the LED could operate at maximum current for TA up 31.1 °C assuming ILED = 60mA and VLED = 70.1V (without thermal scaleback). Above this ambient temp, the LED temperature would be forced above its maximum die temperature. However, with the current scaleback the LED current will automatically decrease to help limit the LED temperature. Based on the calculations and measurements taken, the thermistor fold back circuit will be reducing the LED current at around 248uA/°C when the LED temperature reaches 102°C (60°C for thermistor + 42°C gradient).

As an example, assume the conditions of ILED = 50mA, TA = 60°C, VLED = 68.1. The LED power is 3.405W and the estimated LED temperature is 60°C + 3.405W × 22.3°C/W = 136°C (without thermal fold-back). With the thermal fold-back at the same conditions, the circuit duty cycle is forced back to 66% (ILED = 40mA) with VLED = 65.4V. This ends up reducing the LED temp to an estimated 118°C.

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Op-Amp C

The last stage in the voltage to PWM converter is Amplifier C. This is configured as a comparator which takes the generated triangle waveform from amplifier A and D and compares it against the gained up and temperature reduced input (AIN). Due to the hysteresis the triangle waveform ranges from 0 to 4.55V. The output of amplifier B is compared against this triangle waveform to produce the duty cycle information at OUTC. OUTC drives the dimming input of the TPS61165 (CTRL).

Figure 10 shows the PWM duty cycle vs analog control input voltage AIN. The low end is limited to around 2.6% due to the forced offset. AIN > 4.55V forces 100% duty cycle.

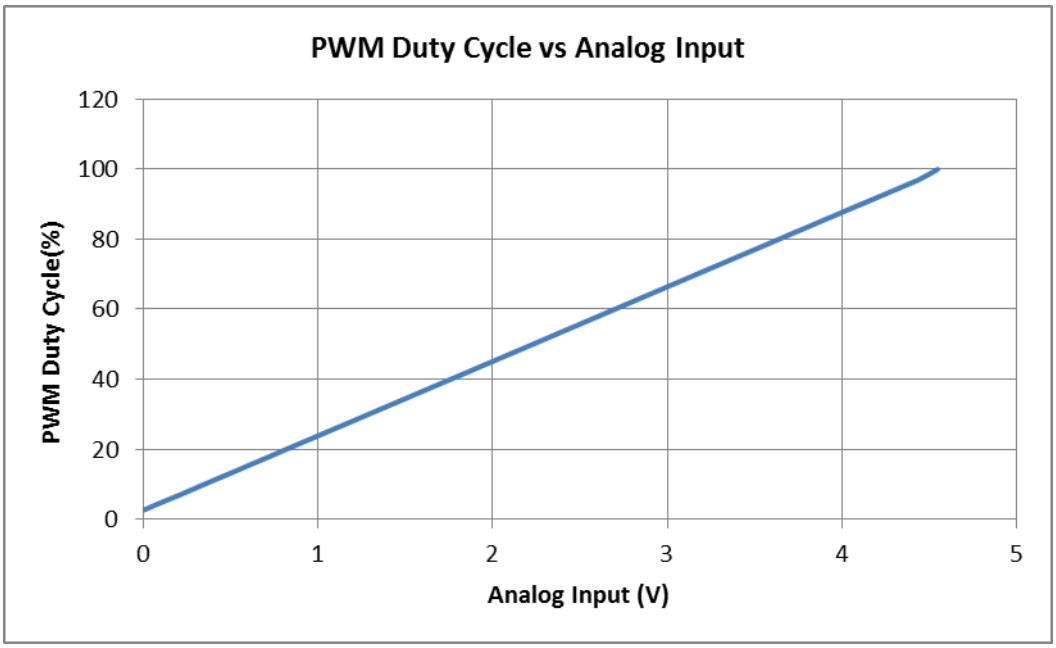

Figure 10. PWM Duty Cycle vs AIN

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3.3 TI Device 3 (TPS709 Linear Regulators)

The two TPS709 linear regulators provide the 5V VCC and 2.5V VREF for the quad op-amp voltage to PWM circuit. The TPS709 has a voltage range of 2.7V to 30V and a max output current of 200mA. The wide input range of the TPS709 allows it to be tied to the same 6V to 18V range as the TPS61165. The TPS709 was also chosen because it provides an enable input which can be used for delaying the turn on of VCC and VREF relative to the input supply. This prevents theTPS61165 turning on with a voltage at its CTRL input which could cause flicker during power on.

Figure 11 shows the typical schematic of the TPS709 in the circuit. Resistors R3, R1 and capacitor C4 are used to create a divided down and slow ramped logic voltage at the devices enable input. When VIN is applied, C4 charges up to VIN × (R4/(R3+R4)). The divider (R4 = 62kΩ and R3 = 200kΩ) ensures that the EN input doesn't go over 7V (absolute max voltage) when VIN is 18V and ensures EN is at a logic high voltage for VIN = 6V. The delay from VIN going high until EN hits a logic high is set by the time constant of R3 and C4 (200kΩ and 10uH). Typical logic high voltages on the TPS709's EN input are around 0.52V. Figure 12 shows the typical delay from VIN to VCC and VREF after power is applied.

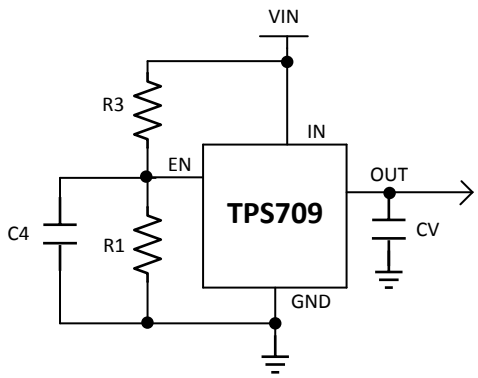

Figure 11 VCC, VREF Generation Using the TPS709

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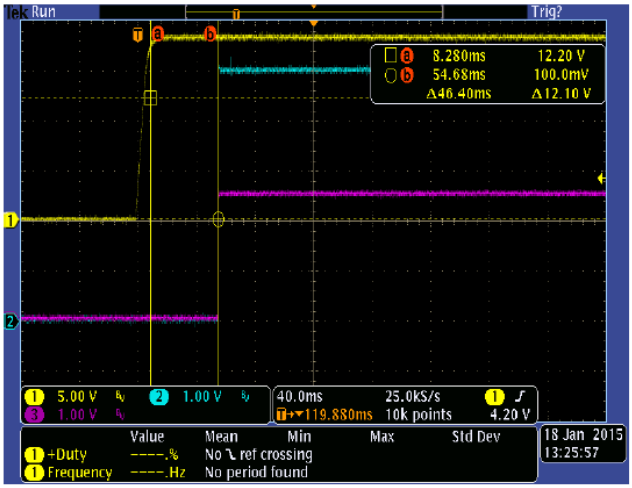
VIN = 18V



VIN = 6V

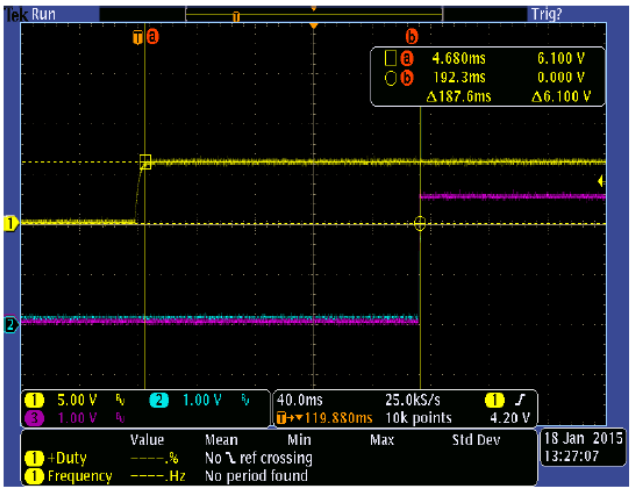


Figure 12. t_{DELAY} between VIN (Ch1) and VCC (Ch2), VREF (Ch3)

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4 Getting Started Hardware

Figure 13 shows a 3d representation of the board layout. The VBATT header connects to a 6V to 18V power source with at least 1A current capability. AIN connects to the DC control voltage (0 to 5V). The AIN current requirement is < 1mA.

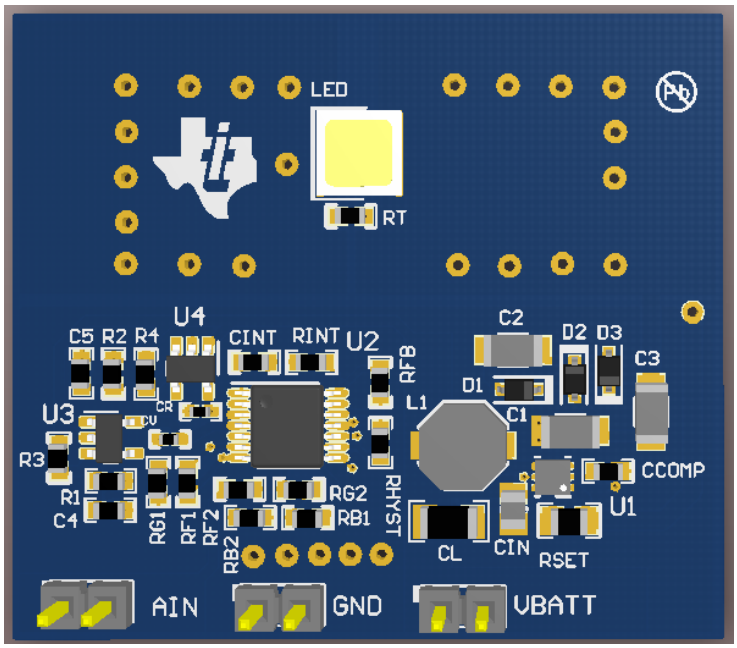

Figure 13. 3D View of PCB

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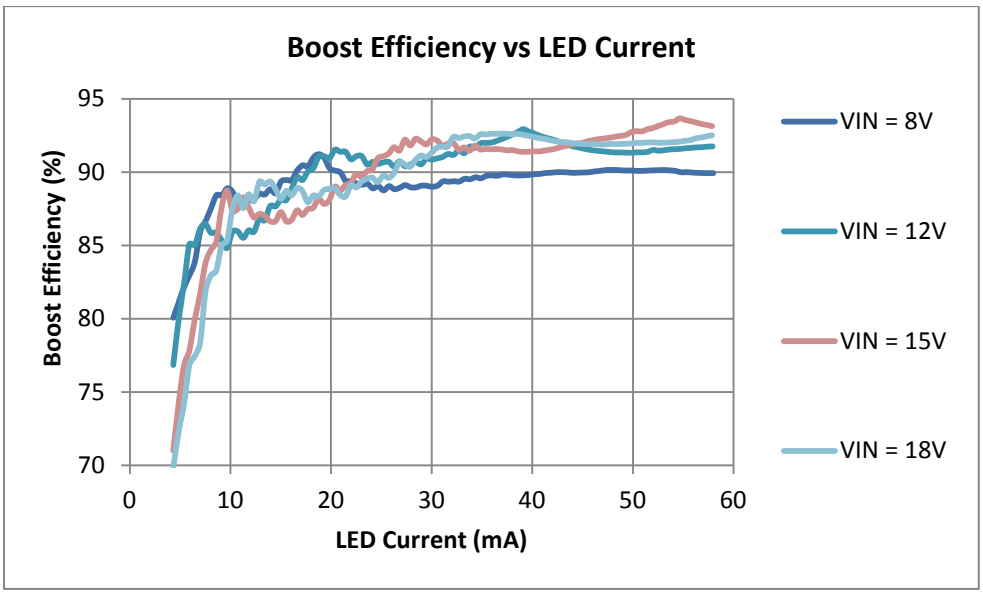
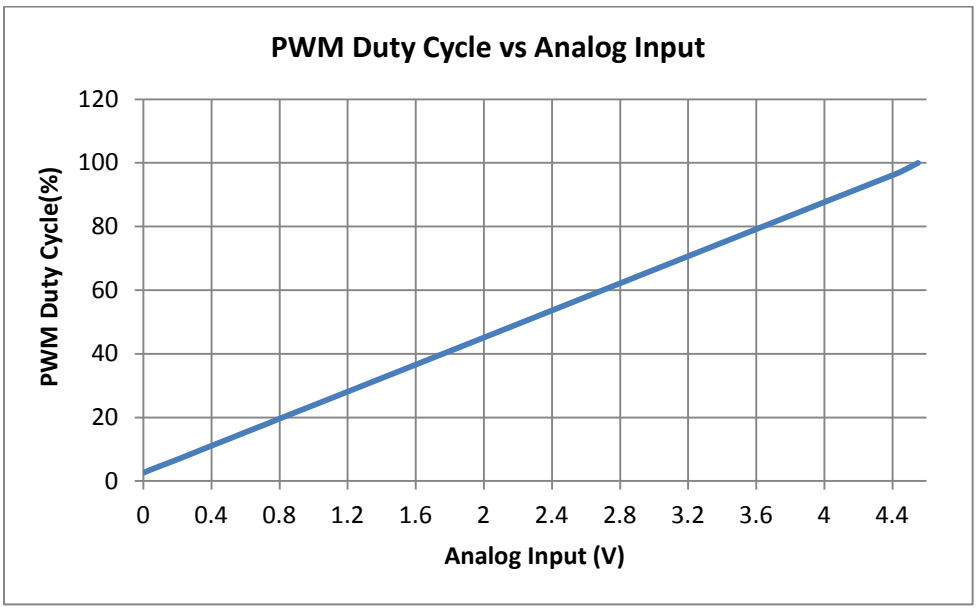
5 Test Data

The following plots show the typical performance of the

5.1 Efficiency vs VIN and ILED



5.2 Generated PWM Duty Cycle vs Analog Input Voltage



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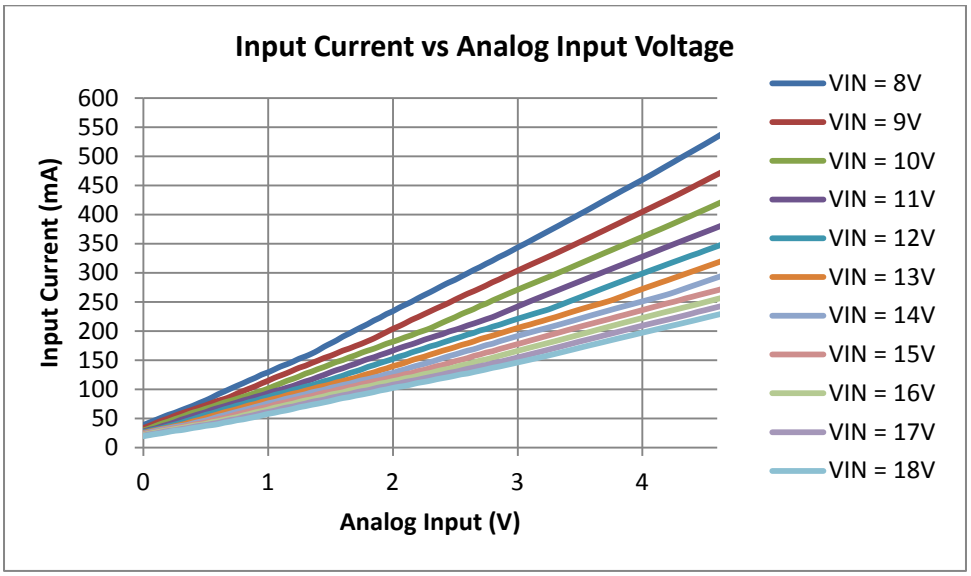
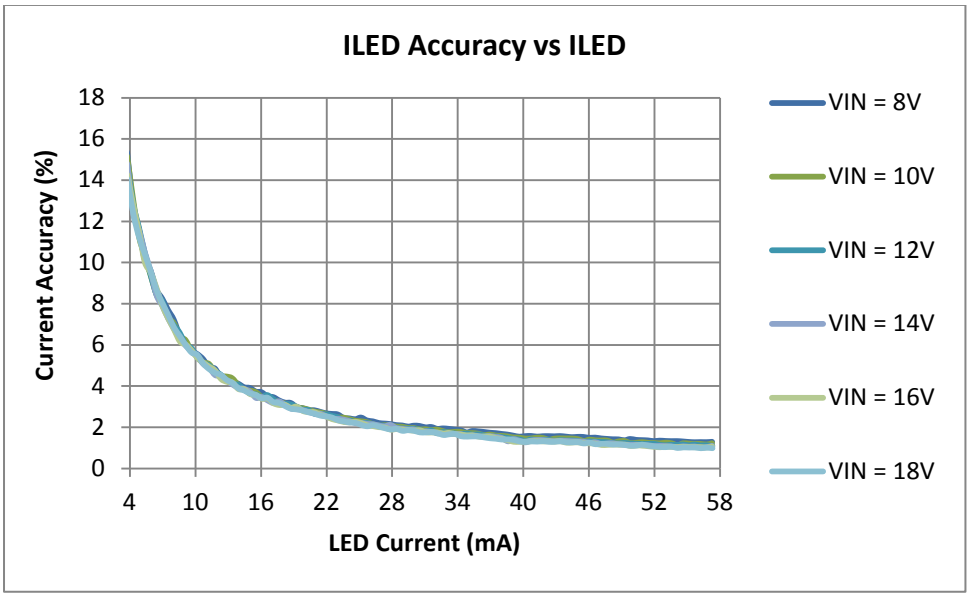
5.3 Input Current (IBATT) vs VIN, ILED



5.4 ILED Accuracy vs LED Current



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6 Design Files

6.1 Schematics

To download the Schematics for each board, see the design files at
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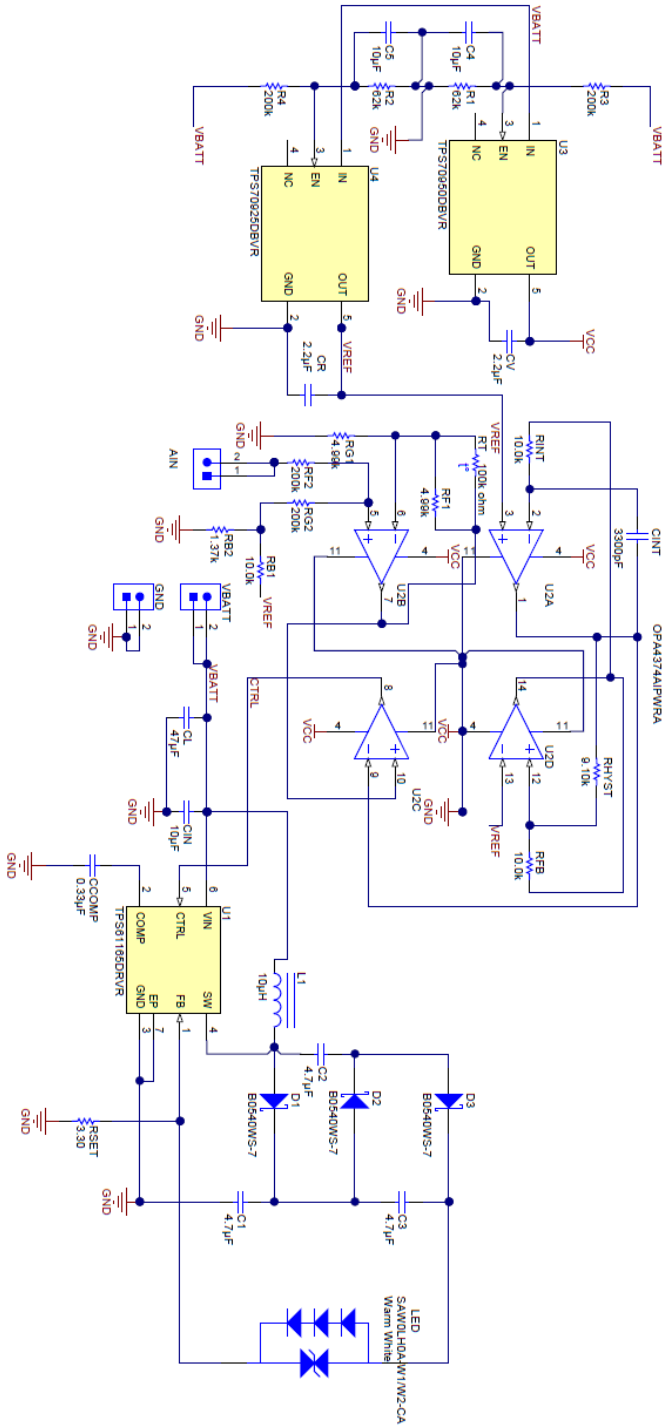

Figure 14: Board Schematic

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6.2 Bill of Materials

To download the Bill of Materials for each board, see the design files at http://www.ti.com/tool/TIDA-00660

Texas Instruments

Bill of Material

TI DESIGNS

TIDA-00660

Item	Qty	Reference	Value	Part Description	Manufacturer	Manufacturer Part Number
1	1	PCB	N/A	Printed Circuit Board	Any	TIDA-00660
2	3	AIN, GND, VBATT	N/A	Header, 100mil, 2x1, Gold, TH	Samtec	HMTSW-102-07-G-S-240
3	3	C1, C2, C3	4.7uF	CAP, CERM, 4.7 µF, 50 V, +/- 20%, X7R, 1206_190	TDK	C3216X7R1H475M160AC
4	2	C4, C5	10uF	CAP, CERM, 10 µF, 25 V, +/- 20%, X5R, 0603	TDK	C1608X5R1E106M080AC
5	1	CCOMP	0.33uF	CAP, CERM, 0.33 µF, 6.3 V, +/- 10%, X7R, 0603	Kemet	C0603C334K9RACTU
6	1	CIN	10uF	CAP, CERM, 10 µF, 25 V, +/- 20%, X5R, 0805_140	Taiyo Yuden	TMK212BBJ106MG-T
7	1	CINT	2700pF	CAP, CERM, 2800 pF, 50 V, +/- 5%, C0G/NP0, 0603	TDK	C1608C0G1H282J
8	1	CL	47uF	CAP, CERM, 47 µF, 25 V, +/- 20%, X5R, 1206	TDK	C3216X5R1E476M160AC
9	2	CR, CV	2.2uF	CAP, CERM, 2.2 µF, 10 V, +/- 20%, X5R, 0402	Wurth Elektronik	885012105013
10	3	D1, D2, D3	N/A	Diode, Schottky, 40 V, 0.5 A, SOD-323	Diodes Inc.	B0540WS-7
11	1	L1	10uH	Inductor, Shielded, Ferrite, 10 µH, 1.4 A, 0.16 ohm, SMD	TDK	LTF5022T-100M1R4-LC
12	1	LED	N/A	LED, Warm White, SMD	Seoul Semiconductor	SAW0LH0A-W1/W2-CA
13	2	R1, R2	63kOhm	RES, 62 k, 5%, 0.1 W, 0603	Vishay-Dale	CRCW060362K0JNEA
14	2	R3, R4	200kOhm	RES, 200 k, 5%, 0.1 W, 0603	Vishay-Dale	CRCW0603200KJNEA
15	3	RB1, RFB, RINT	10kOhm	RES, 10.0 k, 1%, 0.1 W, 0603	Vishay-Dale	CRCW060310K0FKEA
16	1	RB2	1.37kOhm	RES, 1.37 k, 1%, 0.1 W, 0603	Vishay-Dale	CRCW06031K37FKEA
17	2	RF1, RG1	4.99kOhm	RES, 4.99 k, 1%, 0.1 W, 0603	Vishay-Dale	CRCW06034K99FKEA
18	2	RF2, RG2	200kOhm	RES, 200 k, 1%, 0.1 W, 0603	Yageo America	RC0603FR-07200KL
19	1	RHYST	9.1kOhm	RES, 9.10 k, 1%, 0.1 W, 0603	Yageo America	RC0603FR-079K1L
20	1	RSET	3.3Ohm	RES, 3.30, 1%, 0.125 W, 0805	Panasonic	ERJ-6RQF3R3V
21	1	RT	100kOhm	Thermistor NTC, 100k ohm, 1%, 0603	MuRata	NCP18WF104F12RB
22	1	U1	N/A	High Brightness White LED Driver, 3 to 18 V, -40 to 85 degC, 6-pin SON (DRV6), Green (RoHS & no Sb/Br)	Texas Instruments	TPS61165DRVR
23	1	U2	N/A	Quad 6.5 MHz, 585 uA, Rail-to-Rail I/O CMOS Operational Amplifier, 2.3 to 5.5 V, -40 to 125 degC, 14-pin SOP (PW0014A), Green (RoHS & no Sb/Br)	Texas Instruments	OPA4374AIPWRA
24	1	U3	N/A	150-mA, 30-V, 1-uA IQ Voltage Regulators with Enable, DBV0005A	Texas Instruments	TPS70950DBVR
25	1	U4	N/A	150-mA, 30-V, 1-uA IQ Voltage Regulators with Enable, DBV0005A	Texas Instruments	TPS70925DBVR

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6.2.1 Layout Prints

To download the Layout Prints for each board, see the design files at
http://www.ti.com/tool/TIDA-00660

Top Layer

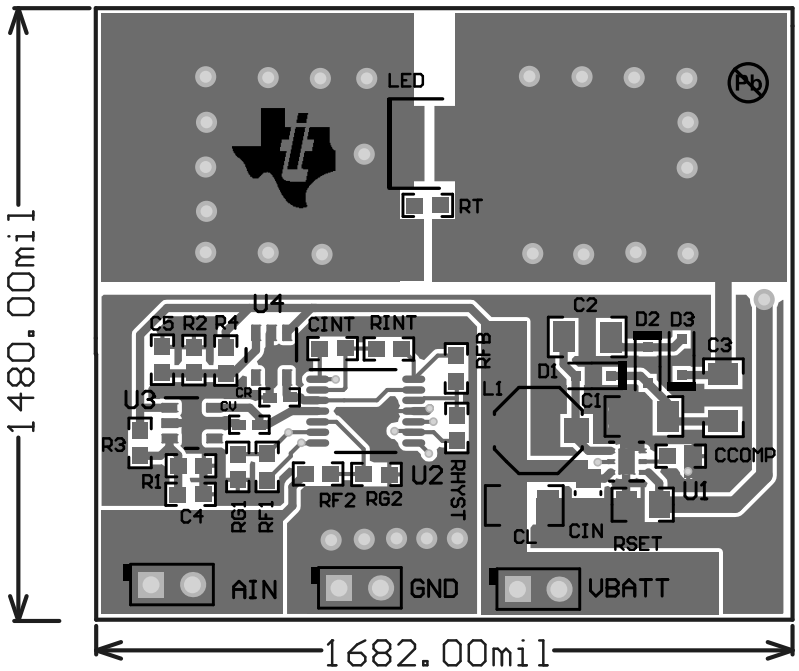

Figure 15: To insert a caption, right click picture > Insert Caption

Bottom Layer

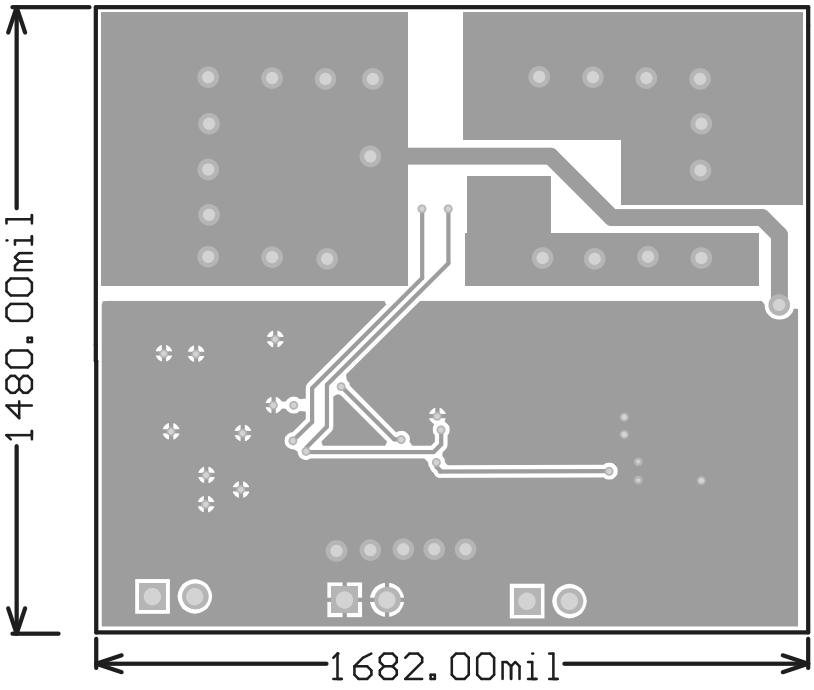

Figure 12: To insert a caption, right click picture > Insert Caption

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6.3 Layout Guidelines

The guidelines for the board layout are as follows:

1. The TPS61165 and all its power components (L1, C1, C2, C3, D1, D2, and D3) should be on the same layer. This ensures that no vias are used for routing the high di/dt switched currents. Using vias with these components will add excessive inductance that will increases noise and can possibly reduce the operating range and decrease efficiency.

The most important goal in laying out the PCB with regards to the TPS61165 is to keep the PCB trace inductance to a minimum. Steps 2 through 7 should be used as the placement order when routing the PCB.

2. C1- should be placed as close as possible to the TPS61165's GND pin and C1+ should be connected as close as possible to D2's cathode and D1's anode.
3. L1 and D1's cathode should be placed as close as possible to the SW pin of the TPS61165.
4. C2- should be placed as close as possible to D1's cathode. C2+ should be placed as close as possible to D2's anode
5. D3's cathode should be placed as close as possible to D2's anode.
6. D3's anode should be placed as close as possible to C3+.
7. C3- should be placed as close as possible to C1+.

8. RSET should be placed close to the FB input of the TPS61165. This limits the trace area from RSET back to FB and limits any noise from coupling into FB.
9. The OPA4374 and its components are not as critical as the TPS61165's power components, but the layout for this circuit should kept away from the power components of the TPS61165. This prevents any noise from coupling into the high impedance nodes of the OPA4374.

10. The PCB footprint for the LED must be sized as large as possible. The power generated by the LED can be over 4W. The larger the LED footprint, the lower the thermal resistance, and the lower the operating temperature of the LED. The suggested PCB layout uses the top and bottom layer of the two layer board for a thermal pad. The bottom layer is thermally coupled to the top layer by using 10 to 12, 28mil vias on both the anode and cathode of the LED to help conduct the heat.

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6.4 Gerber files

To download the Gerber files for each board, see the design files at http://www.ti.com/tool/TIDA-00660

6.5 Assembly Drawings

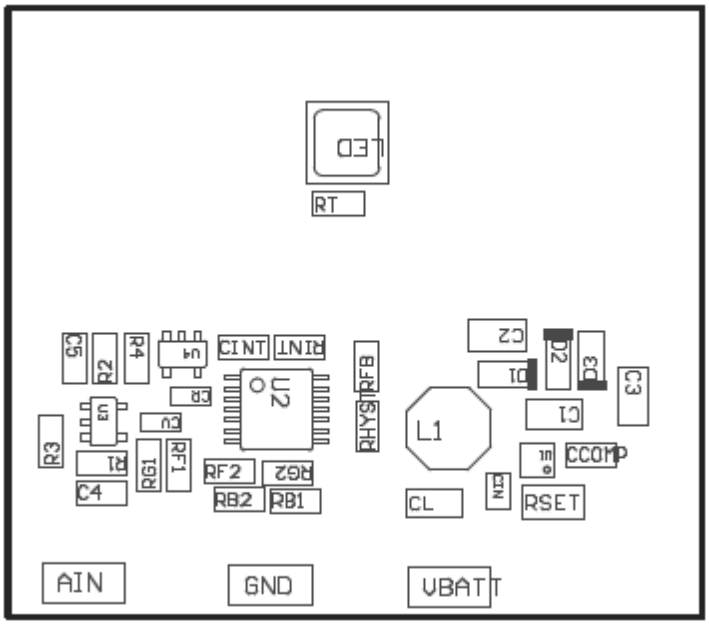

Figure 17. Assembly Drawing (Top Layer)

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7 Software Files

None

8 References

1. Planet Analog, Signal Chain Basics #76: Design a Low Cost PWM Circuit for Single IGBT drive applications, Thomas Kuglestadt, Systems Engineer, Texas Instruments

   http://www.planetanalog.com/author.asp?section_id=483&doc_id=559556&print=yes

2. TPS61165 Datasheet
   http://www.ti.com/lit/ds/symlink/tps61165.pdf

3. OPA4374 Datasheet
   http://www.ti.com/lit/ds/symlink/opa4374.pdf

4. TPS709 Datasheet
   http://www.ti.com/lit/ds/symlink/tps709.pdf

9 About the Author

Travis Eichhorn is a Systems Engineer at Texas Instruments Grass Valley Design Center. He works with LED drivers and mobile power.

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