PMP10081RevC Test Results

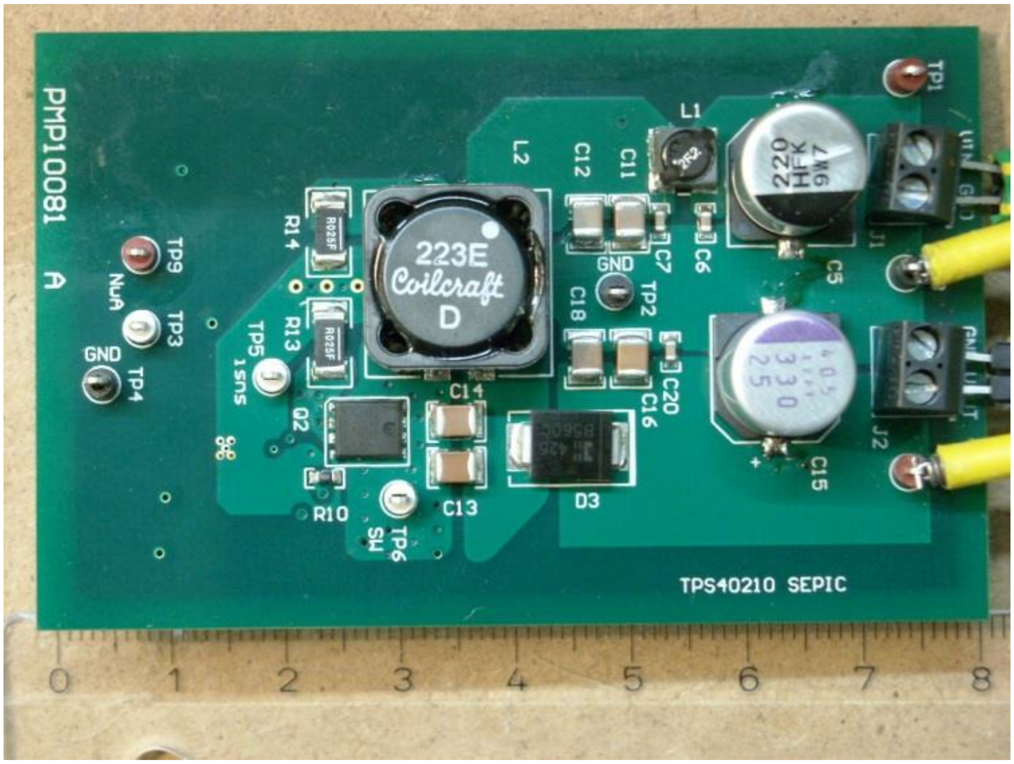
Topology: SEPIC, added CC charging by additional current ctr (via TLC272)
Device: TPS40210 and CSD18563Q5A

Unless otherwise indicated, resistive load was applied, load current was set to 1.5A;
For charger verification battery YUASA NP 5-12 (= 12V, 5Ah, AGM) was used;
here load current has been set to 1.0A (5Ah @ 20%).

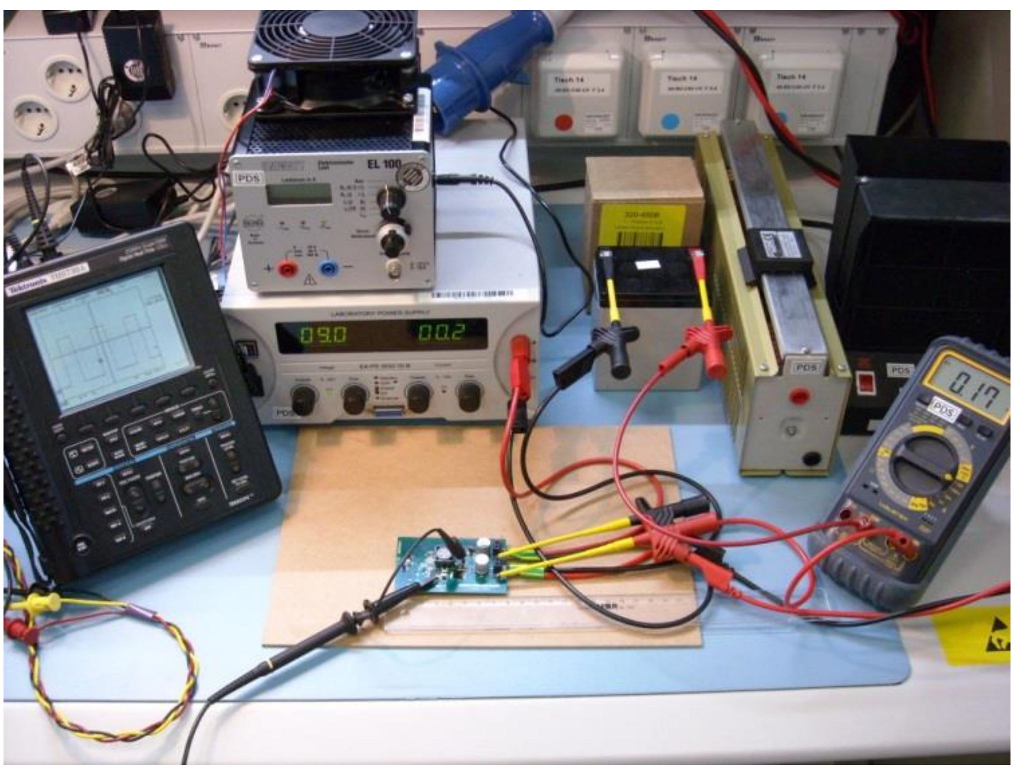
Static measurements:

Fsw	302kHz	OK
ON	8.8V	OK
OFF	7.6V	OK

Picture A shows the 20W SEPIC power stage controlled by TPS40210 and driven by CSD18563:

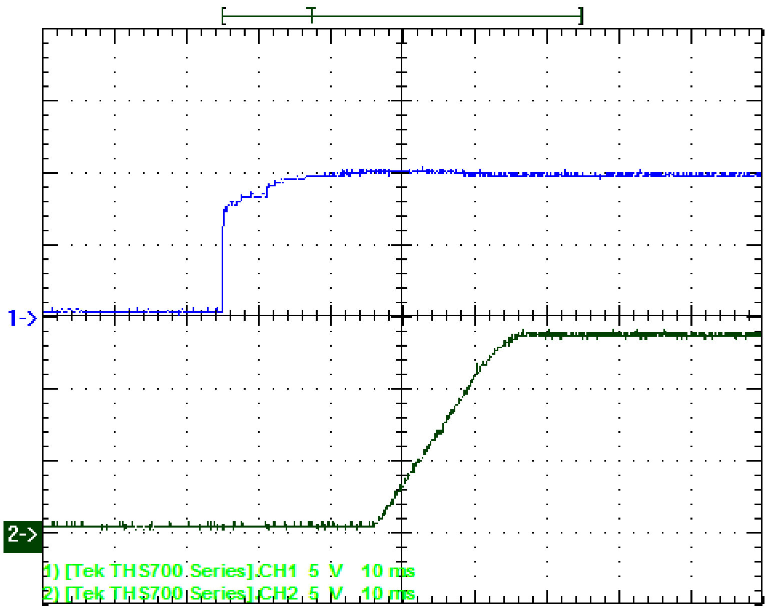


Picture B shows the test setup electronic load, resistive load and – here - lead acid battery 5Ah:



1 Startup

The CV startup waveform is shown in the Figure 1. The input voltage was set to 9V, Css 220nF.



Ch1=> input voltage 5V/div

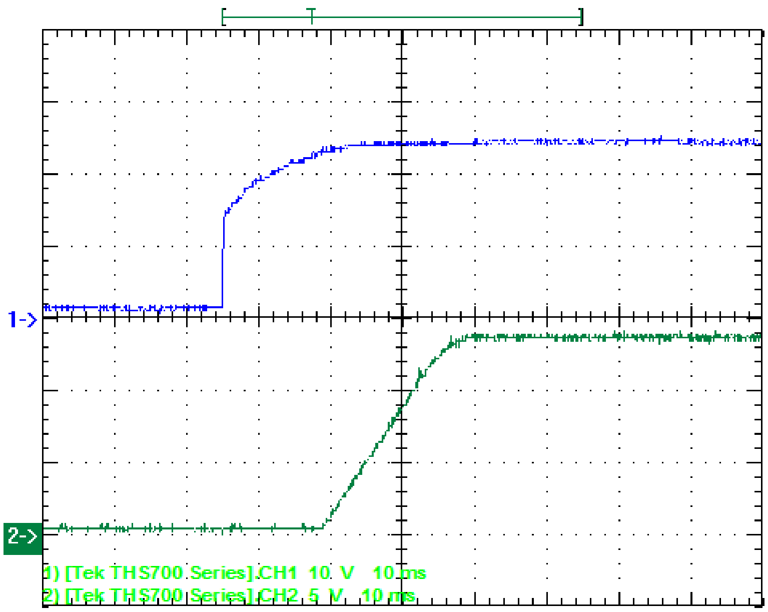
Ch2=> output voltage 5V/div

10ms/div

20MHz bw

Figure 1

The CV startup waveform is shown in the Figure 2. The input voltage was set to 24V.



Ch1=> input voltage 10V/div

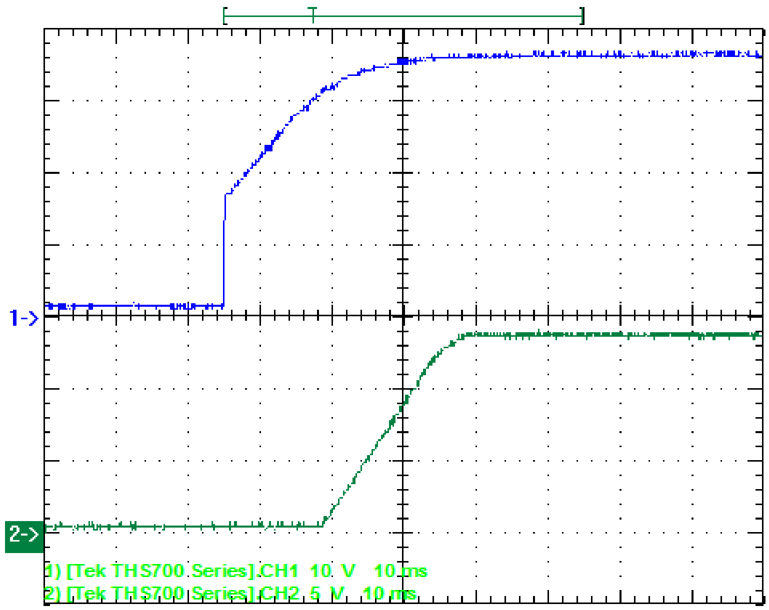
Ch2=> output voltage 5V/div

10ms/div

20MHz bw

Figure 2

The CV startup waveform is shown in the Figure 3. The input voltage was set to 36V.



Ch1=> input voltage 10V/div

Ch2=> output voltage 5V/div

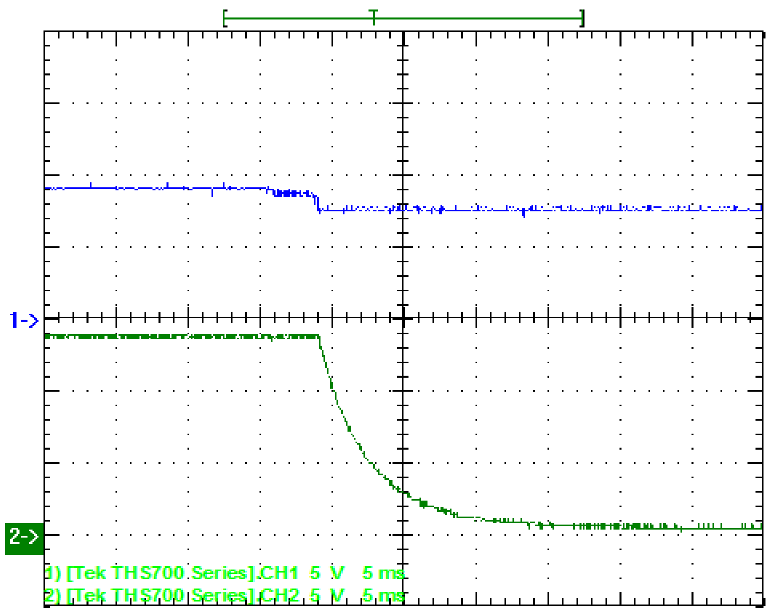
10ms/div

20MHz bw

Figure 3

2 Shutdown

The CV shutdown waveform is shown in the Figure 4. The input voltage was set to 9V. The power supply was disconnected.



Ch1=> input voltage 5V/div

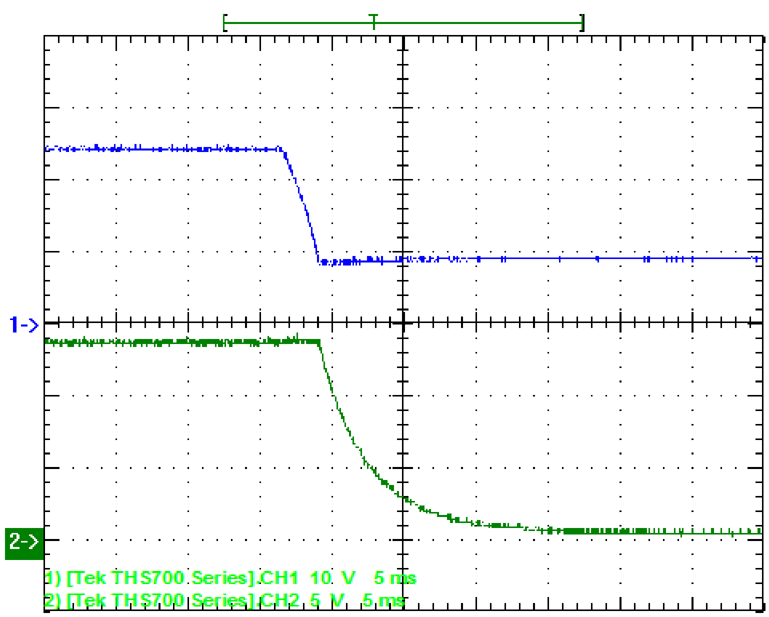
Ch2=> output voltage 5V/div

5ms/div

20MHz bw

Figure 4

The CV shutdown waveform is shown in the Figure 5. The input voltage was set to 24V. The power supply was disconnected.



Ch1=> input voltage 10V/div

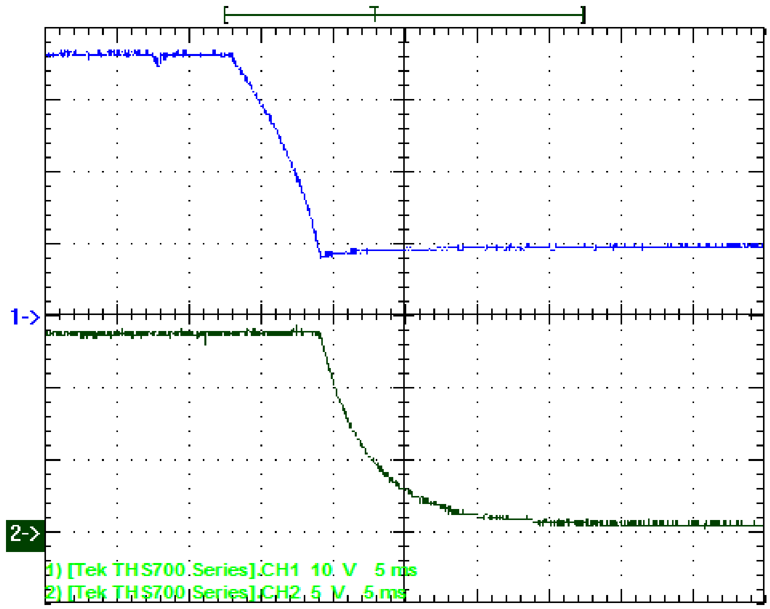
Ch2=> output voltage 5V/div

5ms/div

20MHz bw

Figure 5

The CV shutdown waveform is shown in the Figure 6. The input voltage was set to 36V. The power supply was disconnected.



Ch1=> input voltage 10V/div

Ch2=> output voltage 5V/div

5ms/div

20MHz bw

Figure 6

3 Efficiency

The CV efficiency is shown in the Figure 7 below. The input voltage was set to 9V, 24V and 36V (resistive load).

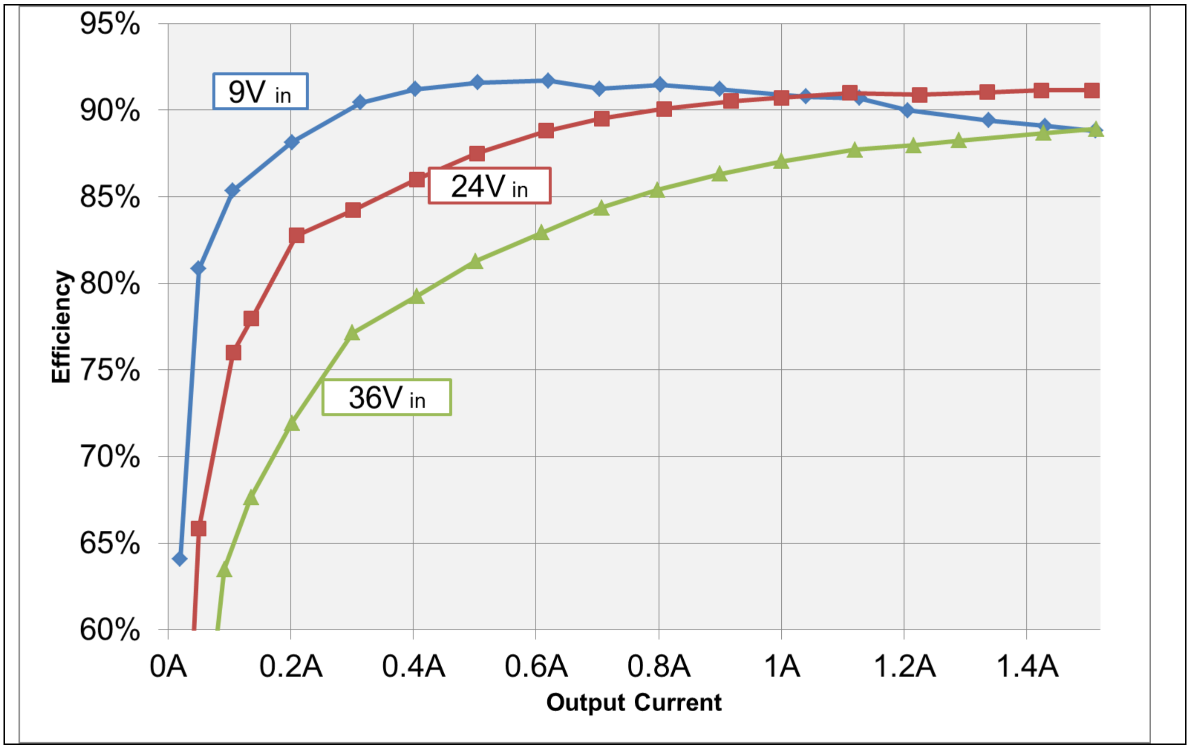


Figure 7

4 Load Regulation

The CV load regulation of the output is shown in the Figure 8 below. The input voltage was set to 9V, 24V and 36V (resistive load).

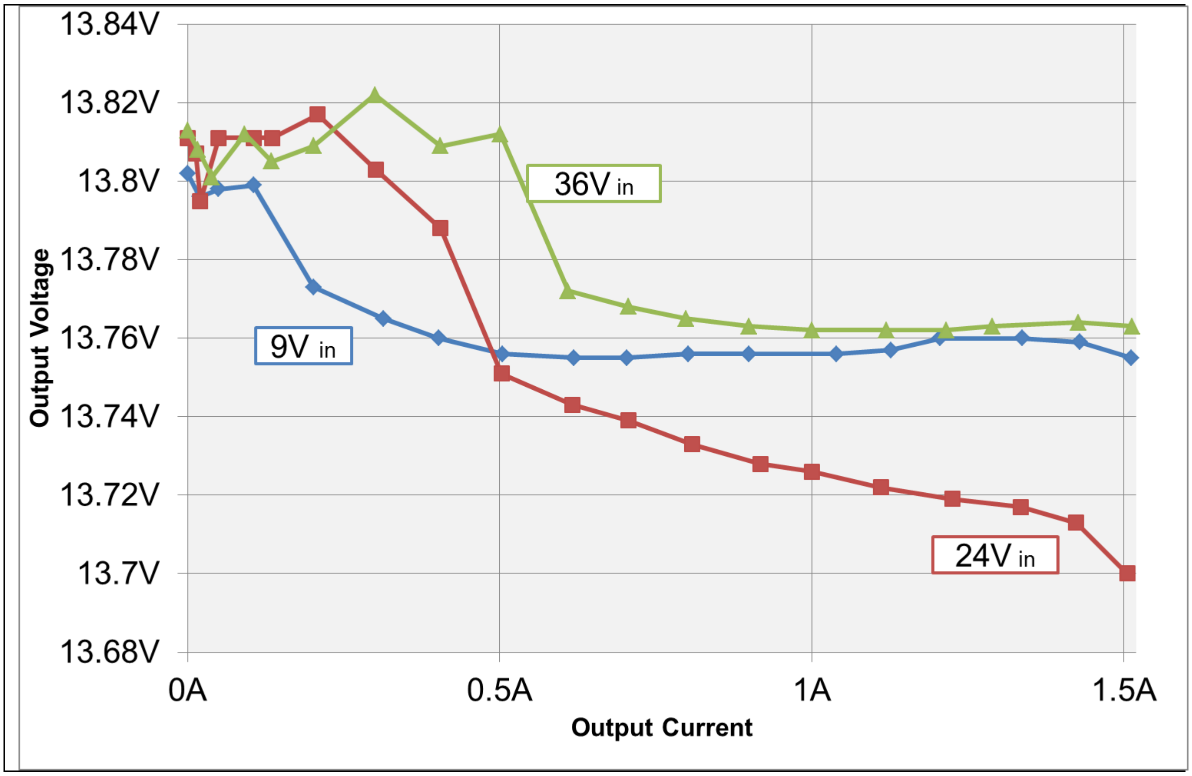


Figure 8

5 Line Regulation

The CV line regulation is shown in Figure 9. The output current was set about 1.5A.

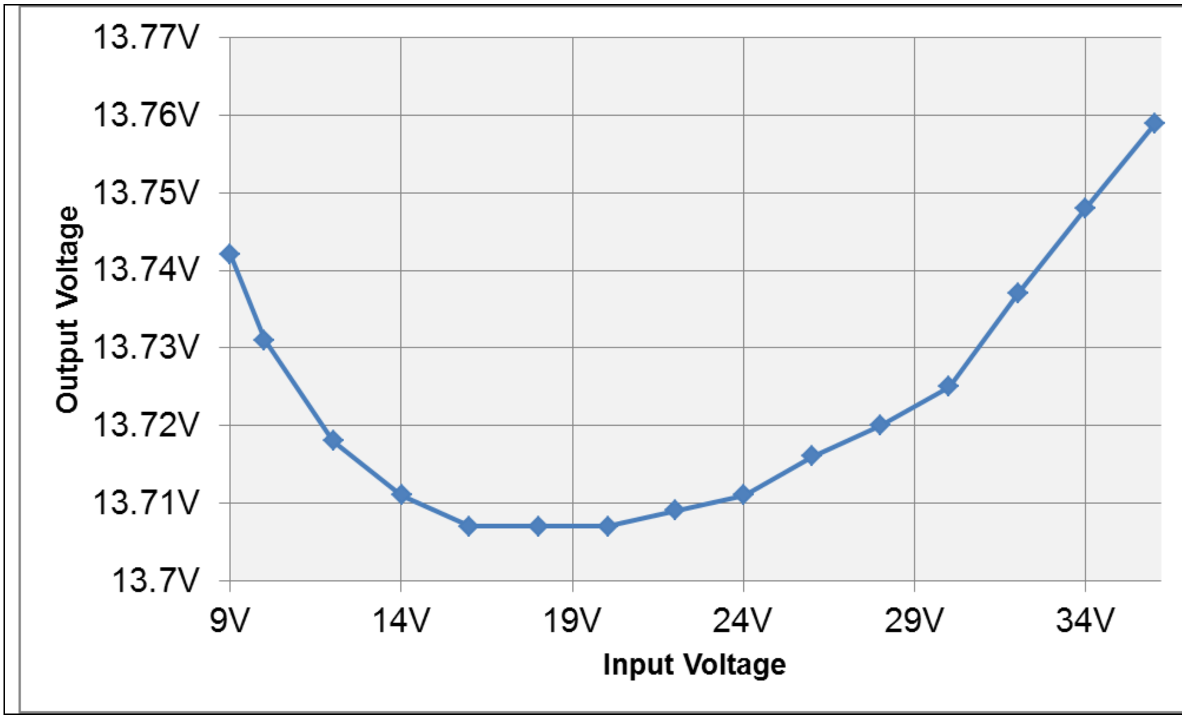


Figure 9

With the same setup efficiencies were calculated. This is shown in Figure 10

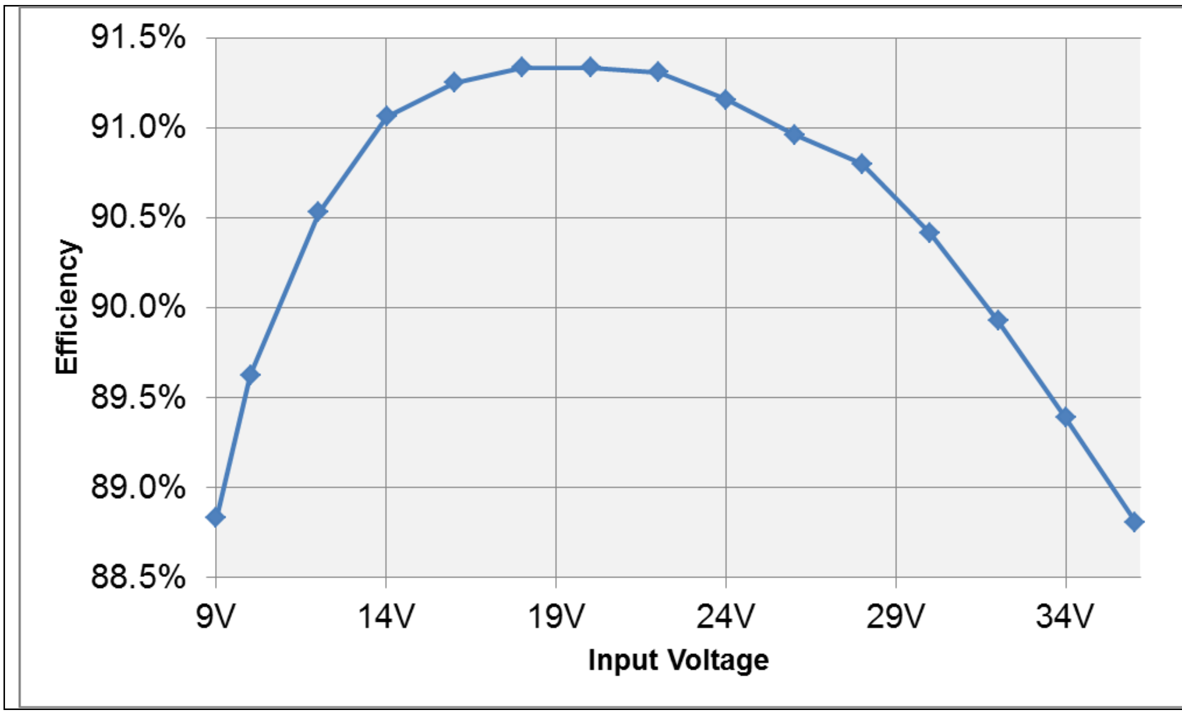
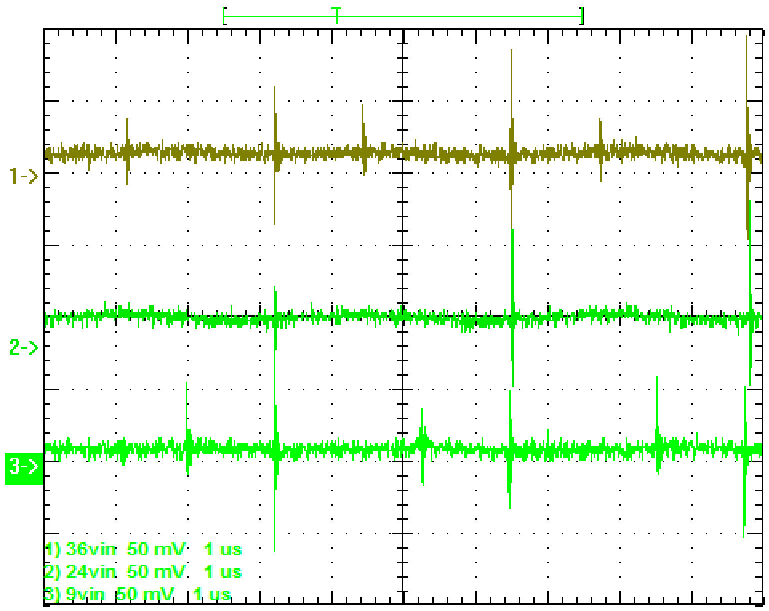


Figure 10

6 Output Ripple Voltage

The CV output ripple voltage at full load 1.5A is shown in Figure 11.



Ch1 => output ripple with 36V Vin

Ch2 => output ripple with 24V Vin

Ch3 => output ripple with 9V Vin

50mV/div

AC coupled

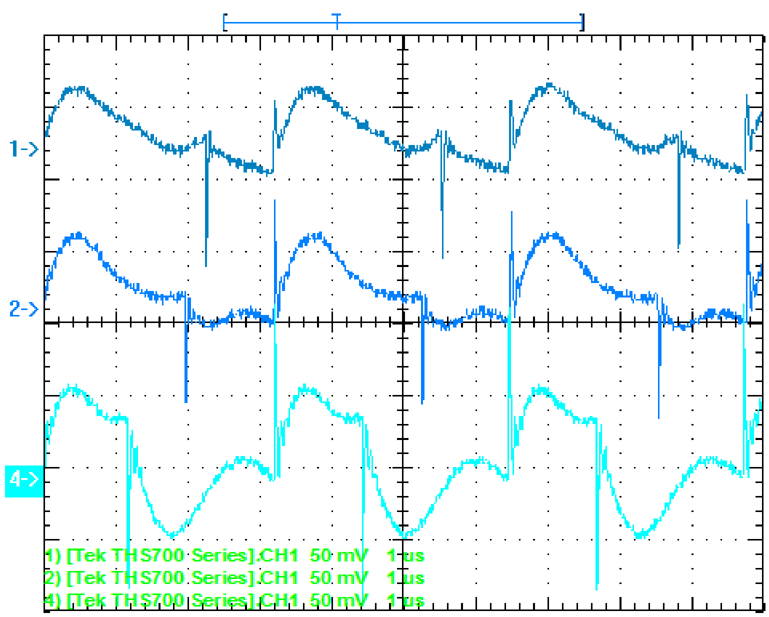
full bw

1µs/div

Figure 11

7 Input Ripple Voltage

The input ripple voltage is shown in Figure 12.



Ch1 => input ripple with 36V Vin

Ch2 => input ripple with 24V Vin

Ch3 => input ripple with 9V Vin

50mV/div

AC coupled

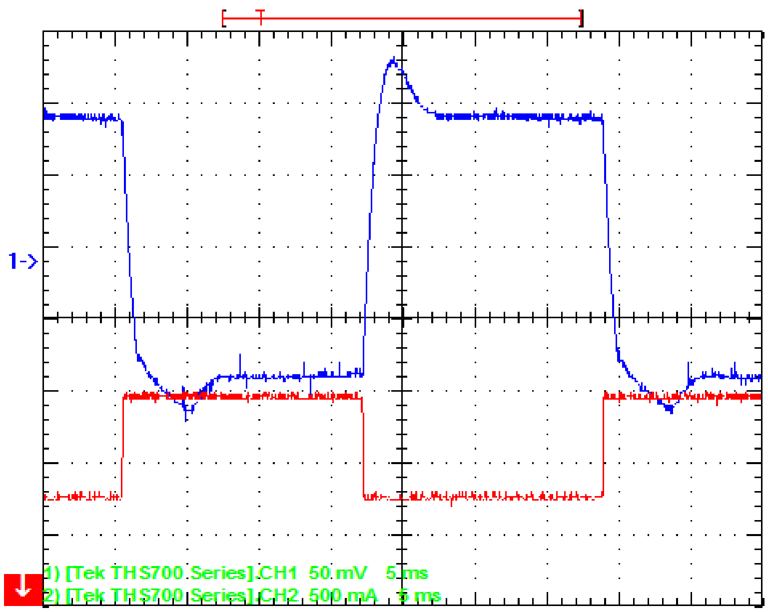
20MHz bw

1µs/div

Figure 12

8 Load Transients

The Figure 13 shows the response to load transients with 9V input voltage. The load is switching from 0.75A to 1.5A with 30Hz. N3305 load was used.



Ch1 => output voltage 50mA/div AC coupling

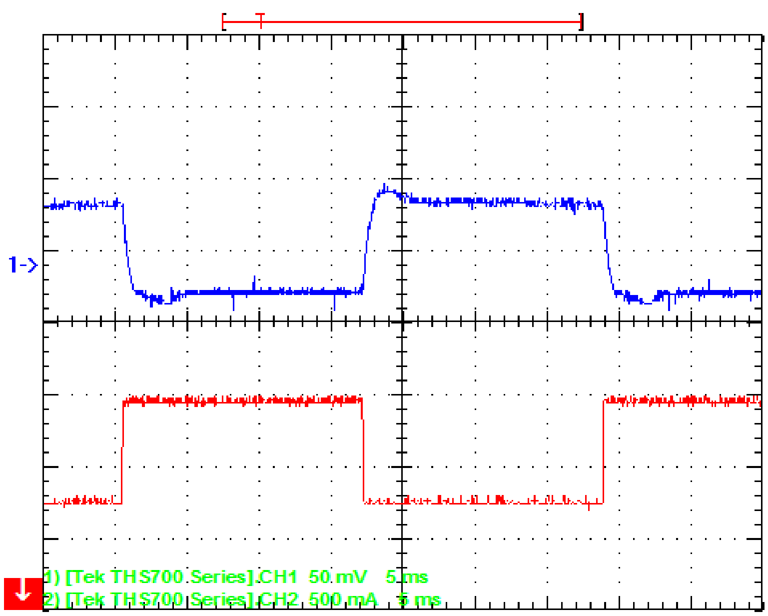
Ch2 => output current 500mA/div

20MHz bw

5ms/div

Figure 13

The Figure 14 shows the response to load transients with 24V input voltage. The load is switching from 0.75A to 1.5A with a frequency of 30Hz (load N3305A).



Ch1 => output voltage 50mV/div AC coupled

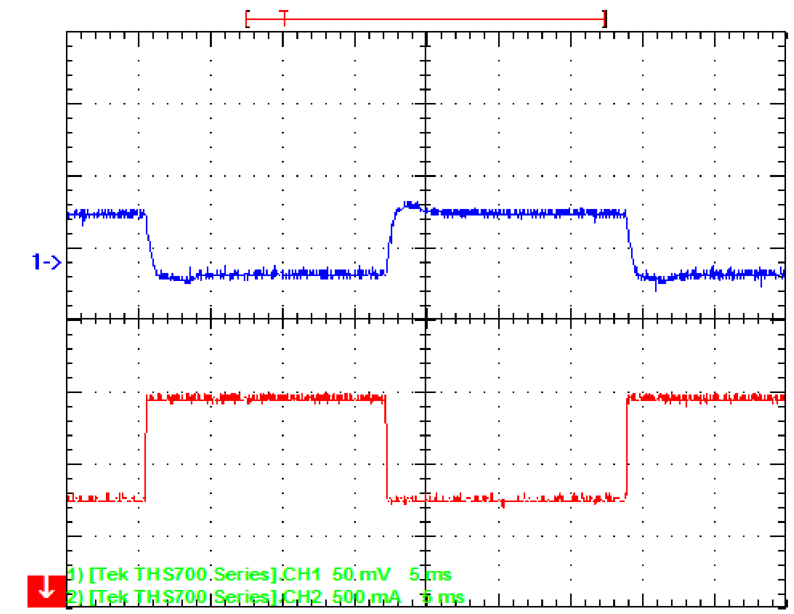
Ch2 => output current 500mA/div

20MHz bw

5ms/div

Figure 14

The Figure 15 shows the response to load transients with 36V input voltage. The load is switching from 0.75A to 1.5A with a frequency of 30Hz. (N3305 load)



Ch1 => output voltage 50mV/div AC coupled

Ch2 => output current 500mA/div

20MHz bw

5ms/div

Figure 15

9 Control Loop Frequency Response

Input voltage was set worst case to 9V input, so at maximum duty cycle RHPZ is lowest.

9.1 Resistive Load

Figure 16 shows the closed loop **voltage controlled** = CV at a load current of 500mA.

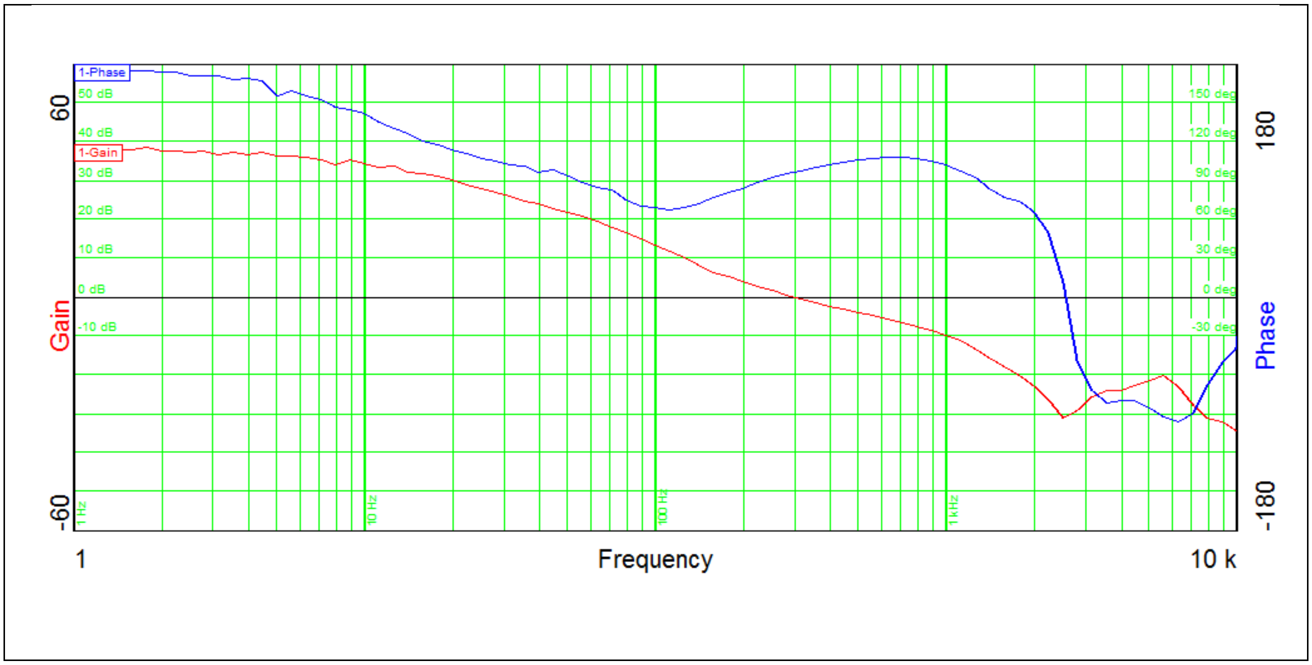


Figure 16

Figure 17 shows the closed loop **current controlled** = CC at a load current of 1A.

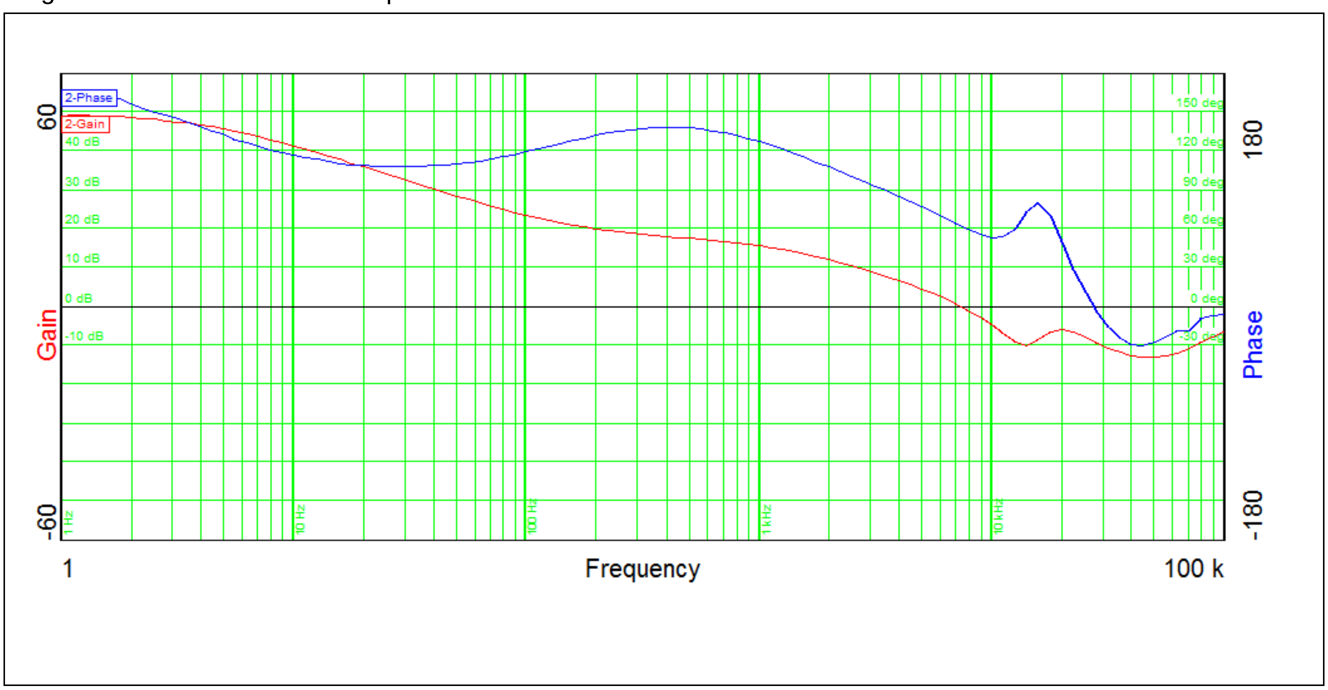


Figure 17

9.2 True C/V Battery Loading @ 12V 5Ah

Figure 18, first - **current controlled** loading at 1A constant current, voltage rises:

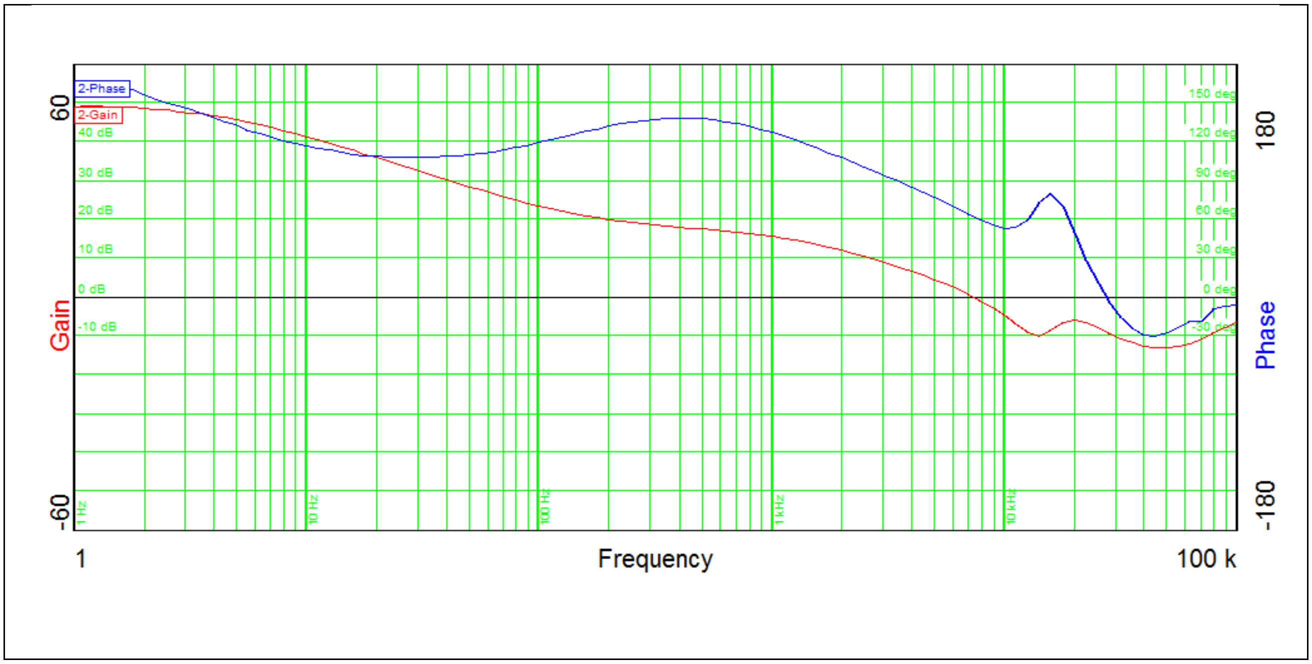


Figure 18

Figure 19, second – transfer current control to **voltage control**, loading now at 13.8V/700mA

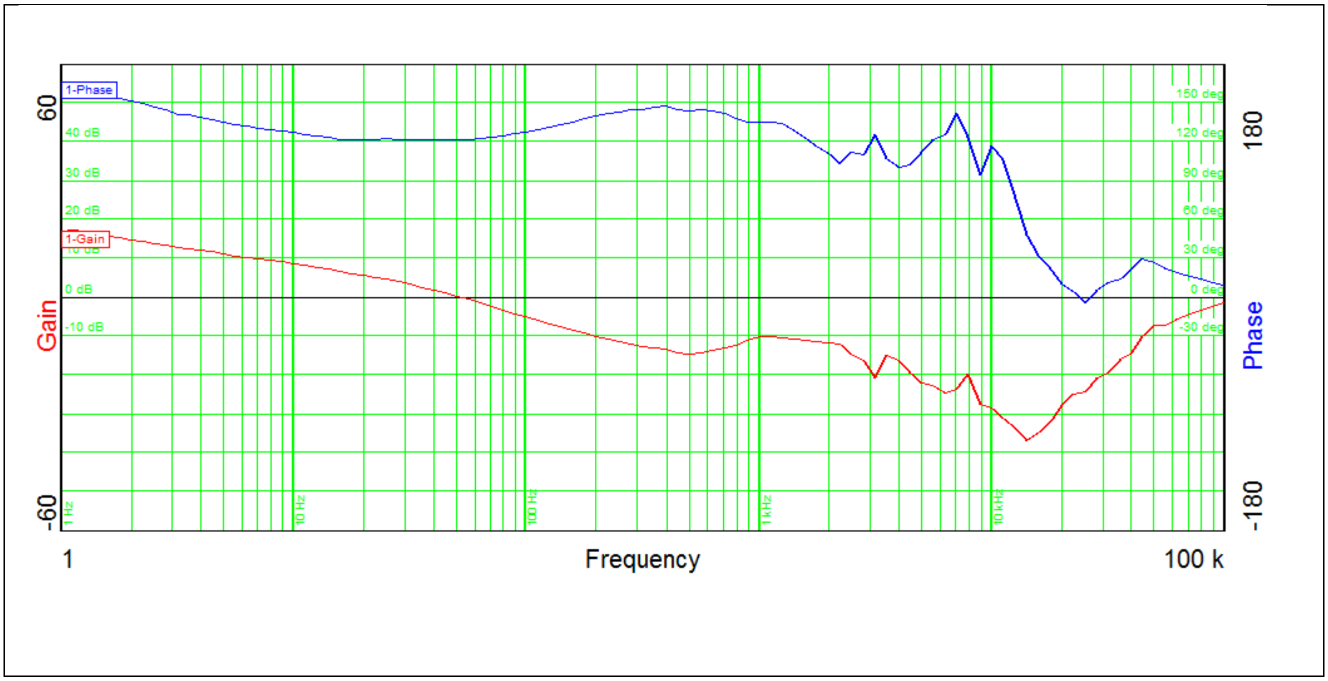


Figure 19

Figure 20, further **voltage control**, charging current drops, shown 700mA – 200mA – 70mA

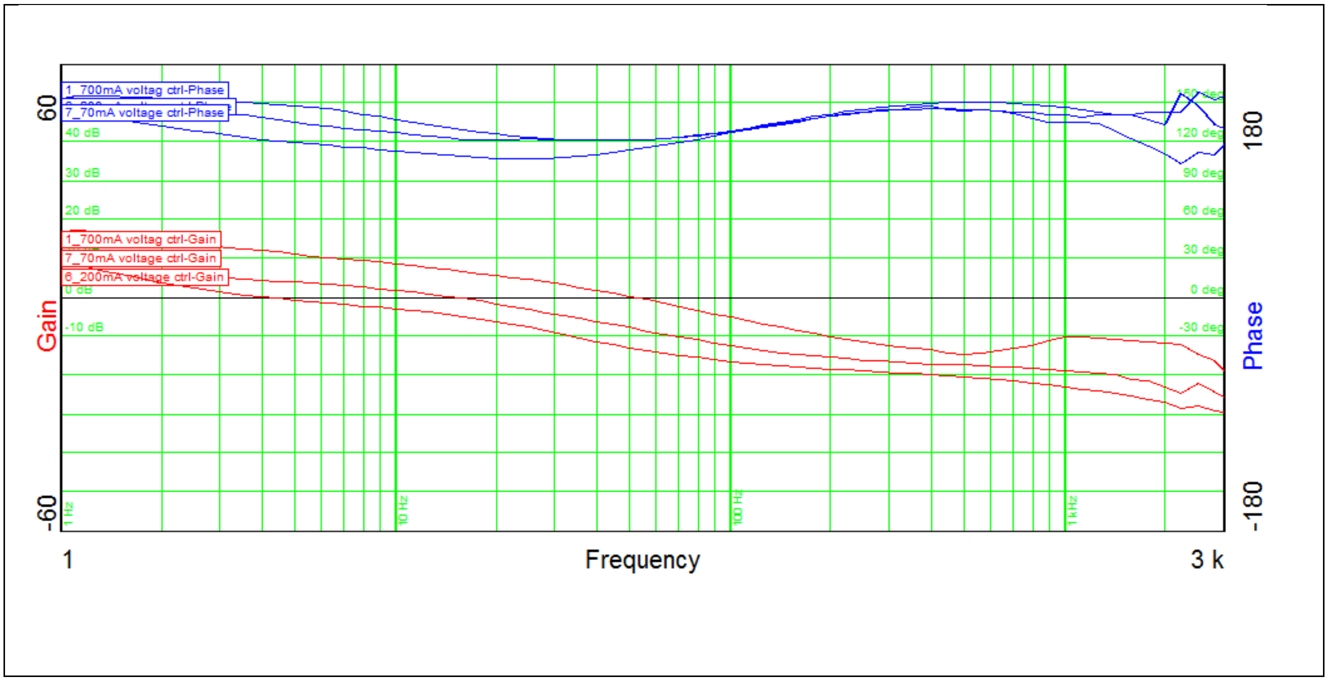


Figure 20

Figure 21 shows comparison voltage control (ye/or) and current control 900mA (rd/bl)

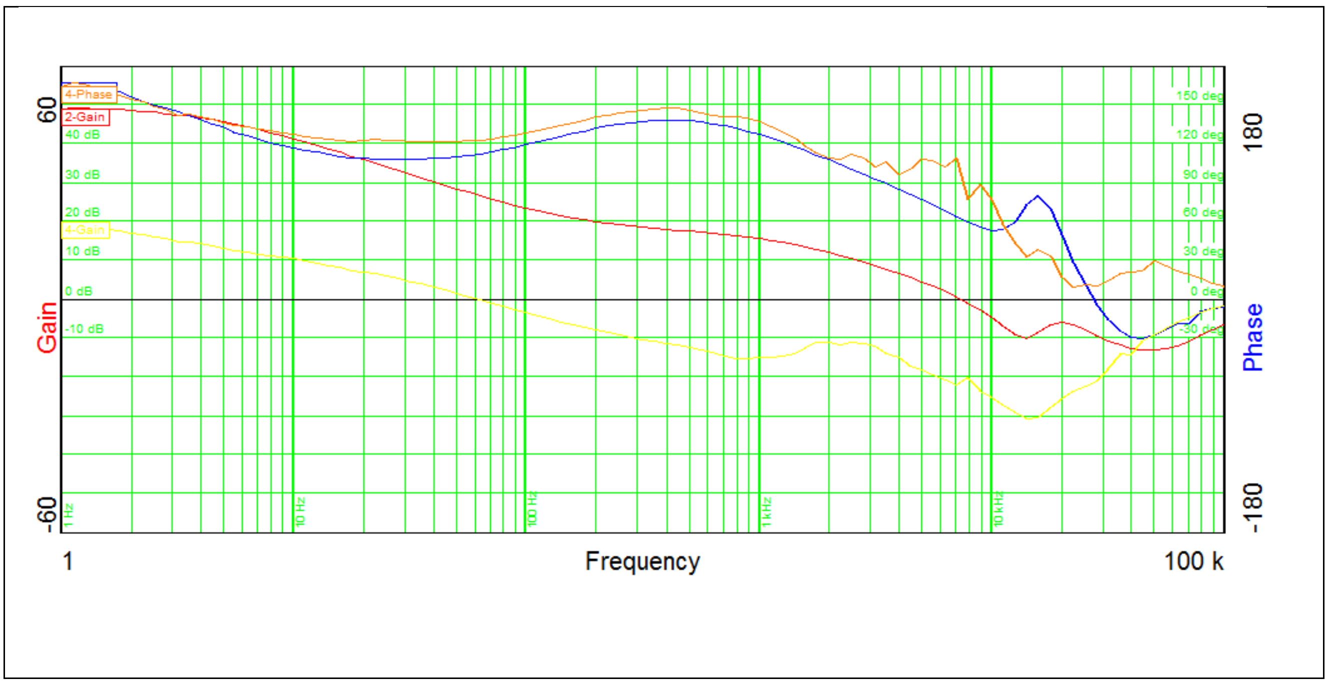


Figure 21

Table 1 + 2 summarizes the results of the Bode measurements:

	R Load		5Ah Battery		
Vin	V ctrl	I ctr	I ctr	Vctrl	V ctr
Bandwidth (Hz)	296.8	7306	7306	60.86	52.06
Phase margin	95.78°	62.54°	62.54°	122.5°	121.2°
slope (20dB/decade)	-0.955	-1.57	-1.57	-0.860	-0.853
			(1000mA)	(900mA)	(700mA)
gain margin (dB)	-30.76	-9.078	-9.078		
slope (20dB/decade)	-1.93	-1.42	-1.42		
freq (Hz)	2565	27230	27230		

Table 1

	5Ah Battery		
Vin	V ctrl 700mA	Vctr 200mA	V ctr 70mA
Bandwidth (Hz)	52	14.7	3.9
Phase margin	121°	130°	122°
slope (20dB/decade)	-0.85	-0.59	-0.41

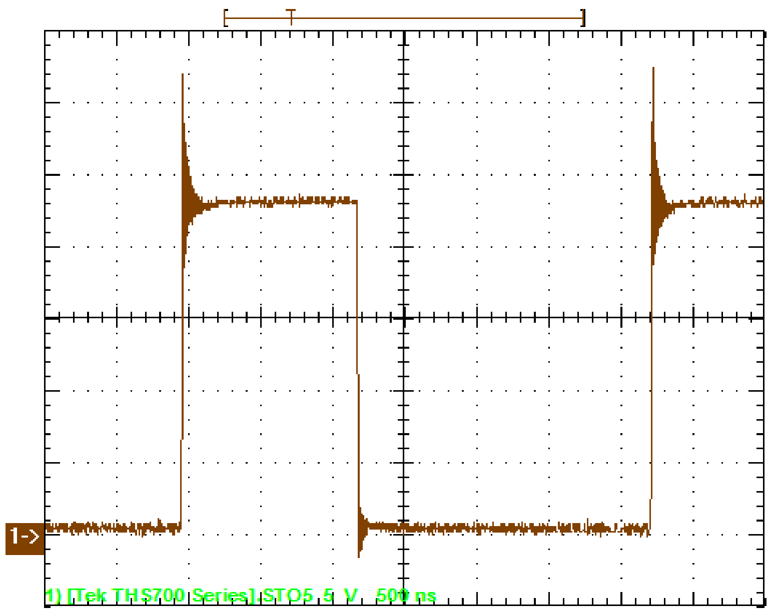
Table 2

CC/CV loading has been verified at true battery; current control charges battery with **constant current** set point 1000mA and voltage at battery increases = CC loading. Touching the voltage set point at 13.8V voltage control takes over and charges the battery further at **constant voltage** 13.8V while current drops continuously = CV loading. Continuously load current decreases to 5mA holdup current.

10 Miscellaneous Waveforms

10.1 Switchnode (drain-source)

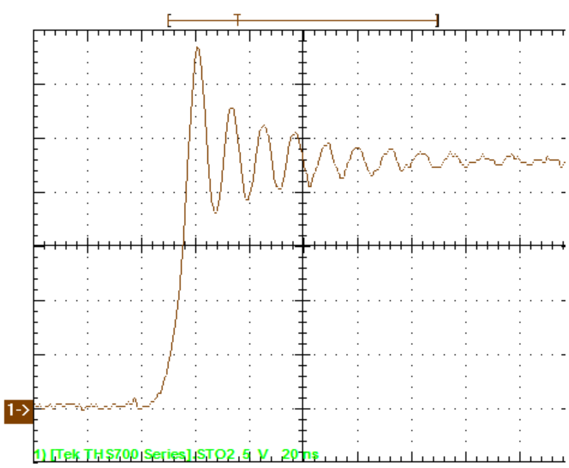
The waveform of the voltage on switchnode (drain to source) is shown in Figure 22. Input voltage was set to 9V.

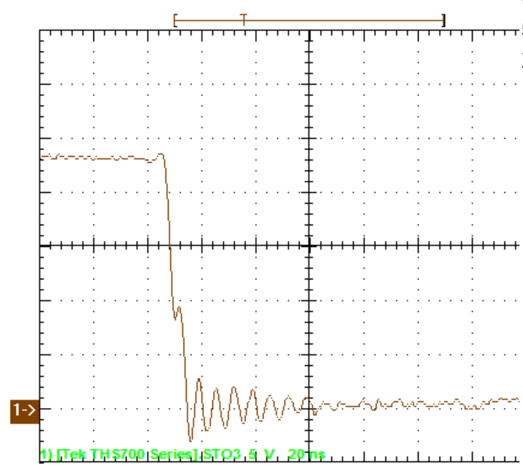


Ch1 =>
5V/div

500ns/div

full bandwidth





Ch1 =>
5V/div
20ns/div

Figure 22

The waveform of the voltage on switchnode (drain to source) is shown in Figure 23. Input voltage was set to 24V.

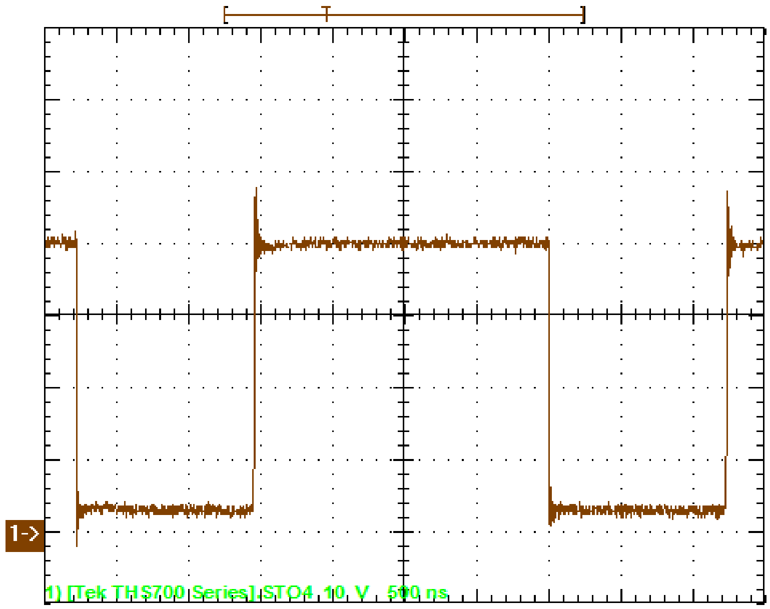
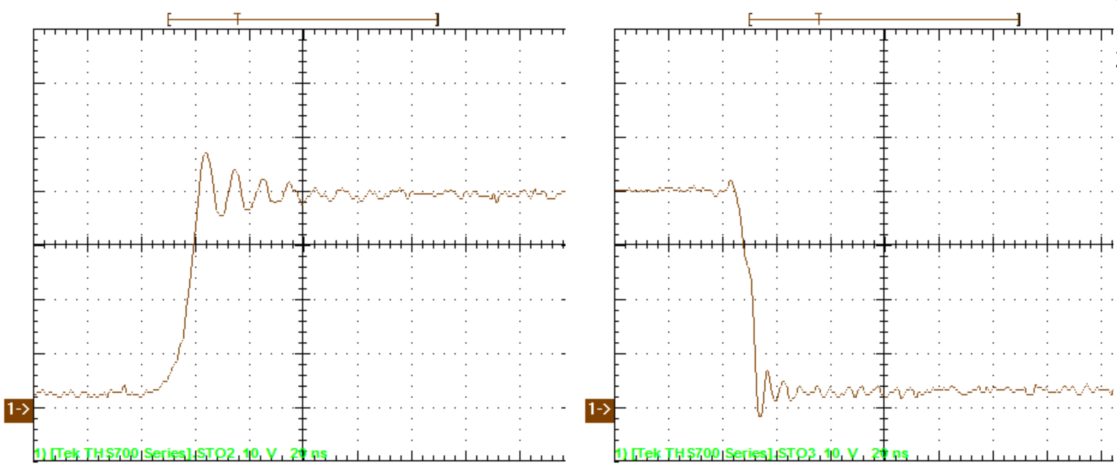
	Ch1 => 10V/div 500ns/div full bandwidth
	Ch1 => 10V/div 20ns/div

Figure 23

The waveform of the voltage on switchnode (drain to source) is shown in Figure 24. Input voltage was set to 36V.

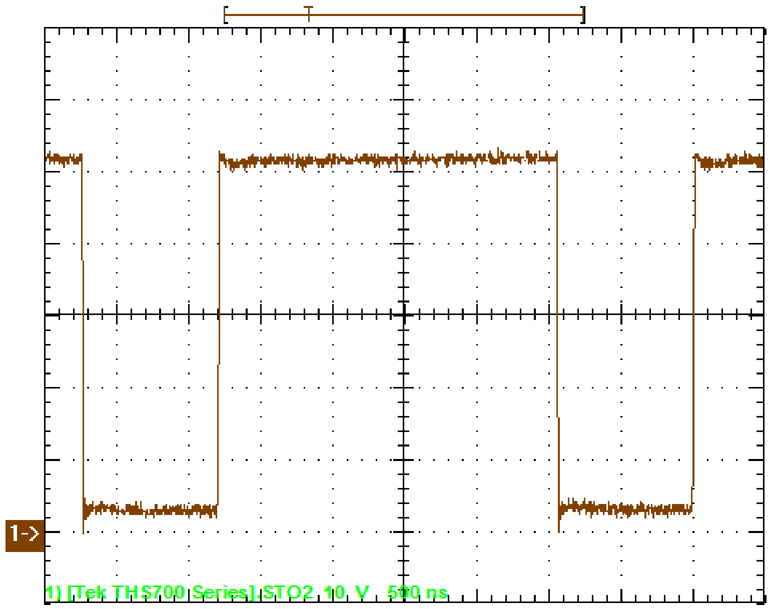
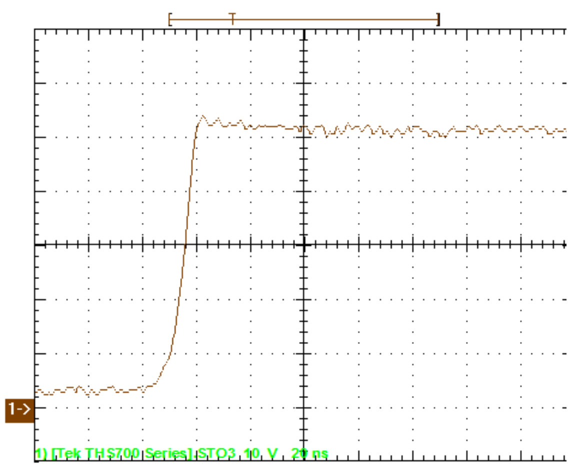
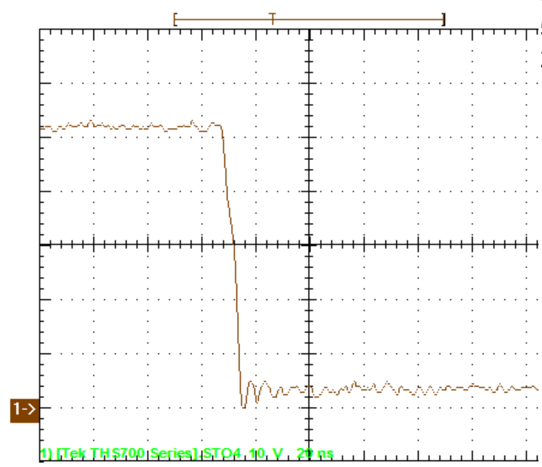
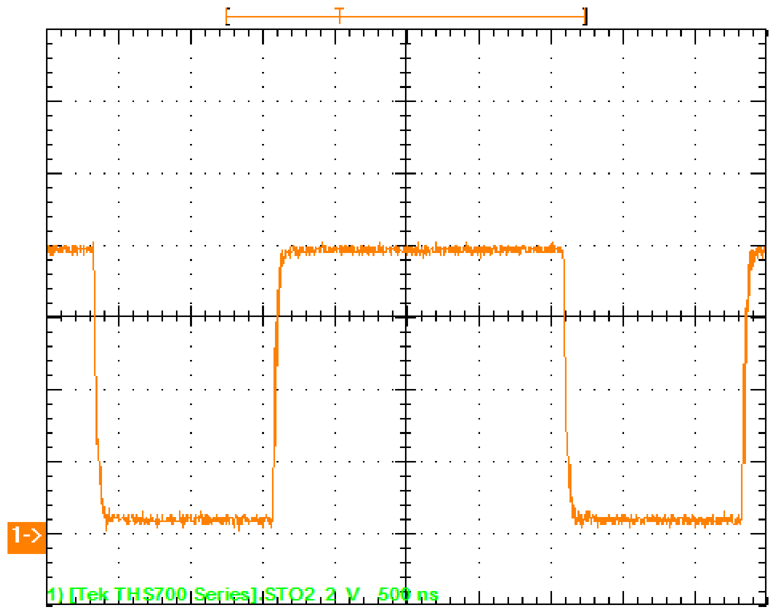
	Ch1 => 5V/div 500ns/div full bandwidth
 	Ch1 => 5V/div 20ns/div

Figure 24

10.2 Gate to Source

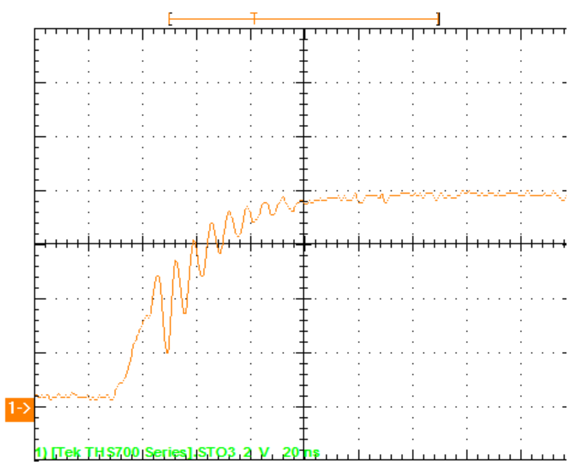
The waveform of the voltage on the gate to source is shown in Fig. 25. Input voltage was set to 9V.

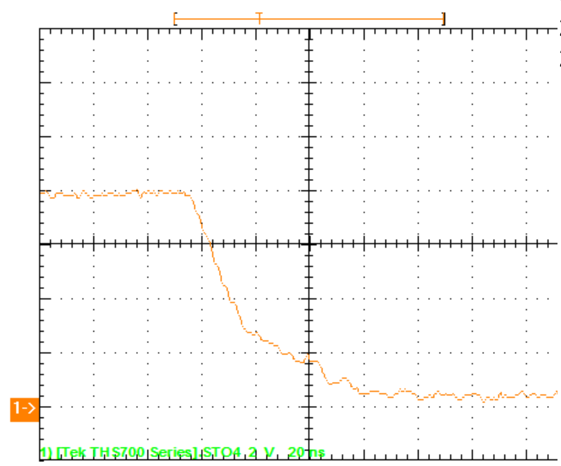


Ch1 => 2V/div

500ns/div

full bandwidth

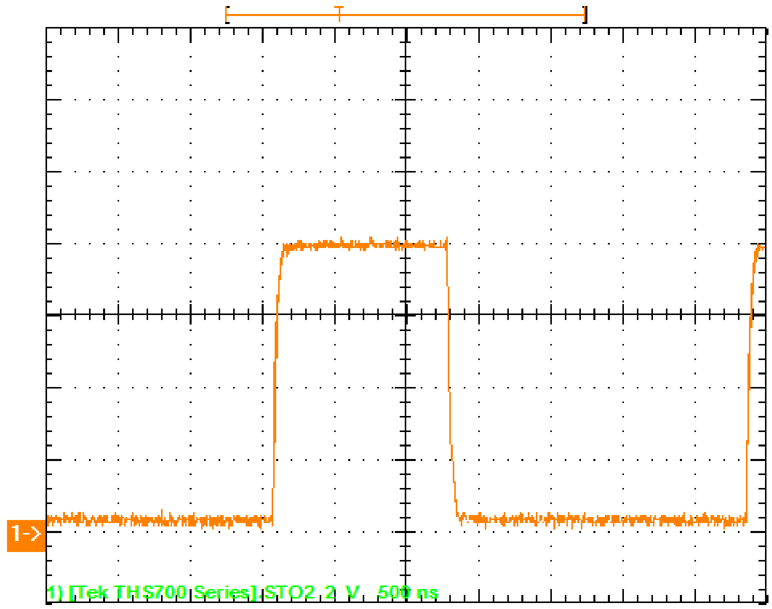




Ch1 => 2V/div
20ns/div

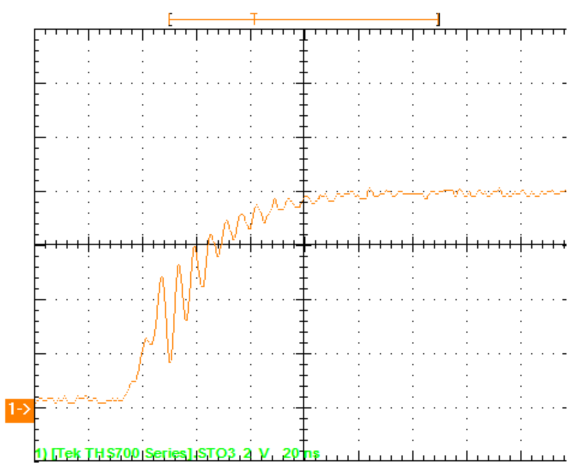
Figure 25

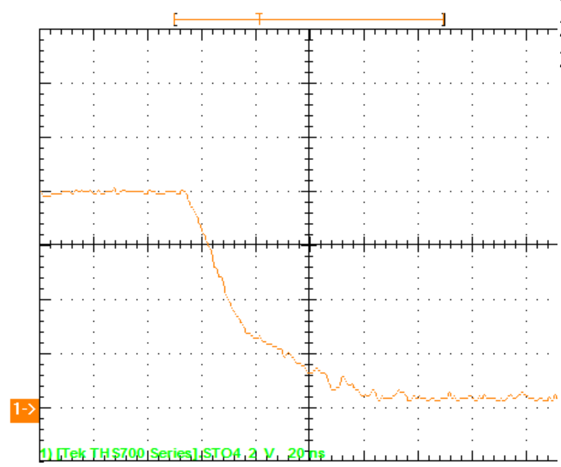
The waveform of the voltage on gate to source is shown in Figure 26. Input voltage was set to 24V.

<table>
<tr>
<td>


</td>
<td>Ch1 =>
2V/div

500ns/div

full bandwidth</td>
</tr>
<tr>
<td>




</td>
<td>Ch1 =>
2V/div
20ns/div</td>
</tr>
</table>

Figure 26

The waveform of the voltage on gate to source is shown in Figure 27. Input voltage was set to 36V.

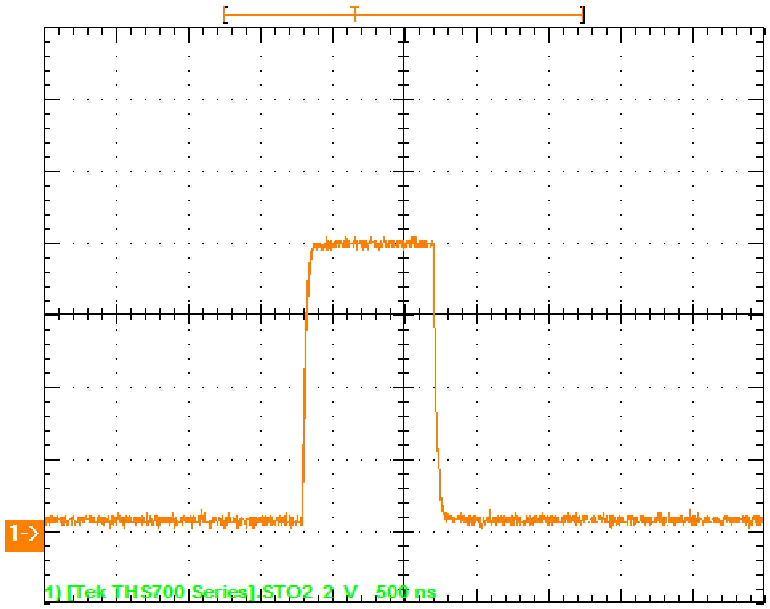
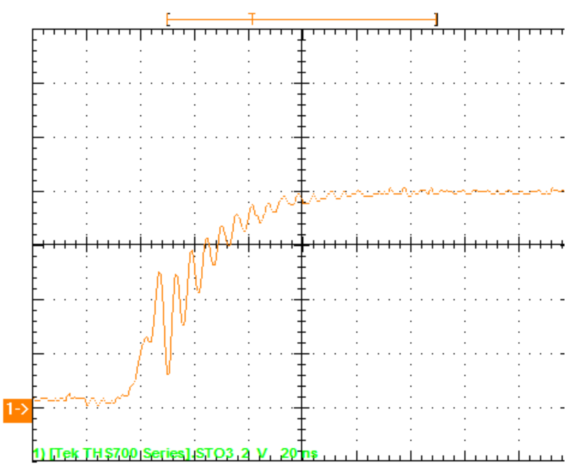
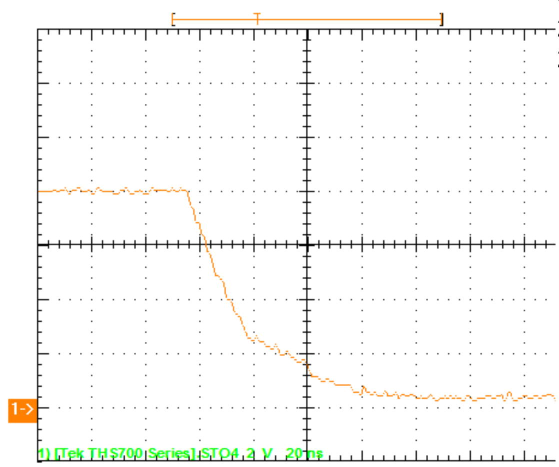
	Ch1 => 2V/div 500ns/div full bandwidth
 	Ch1 => 2V/div 20ns/div

Figure 27

10.3 Voltage D3 (referenced to VOUT)

The waveform of the voltage is shown in Figure 28. Input voltage was set to 9V.

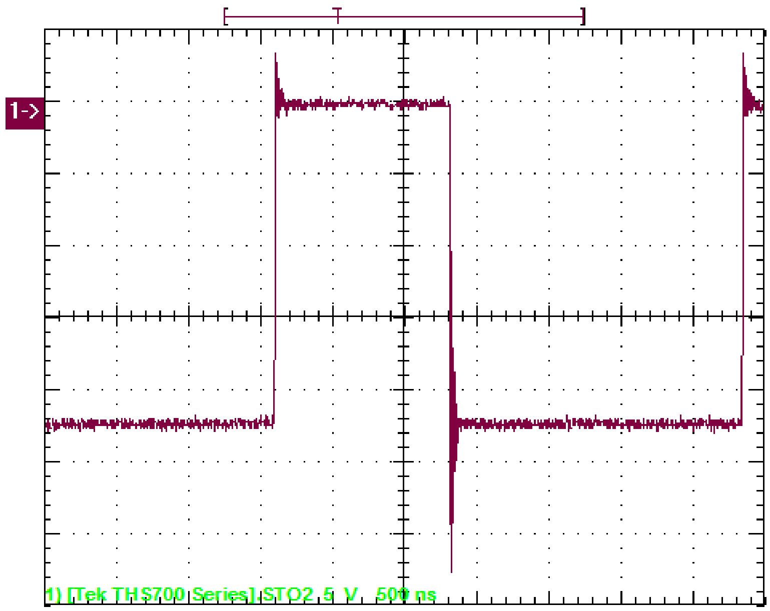
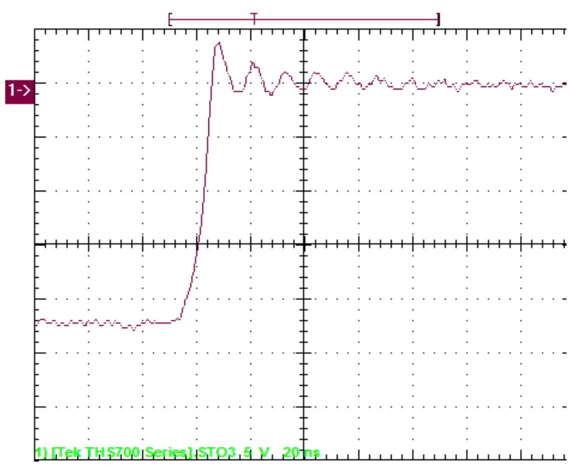
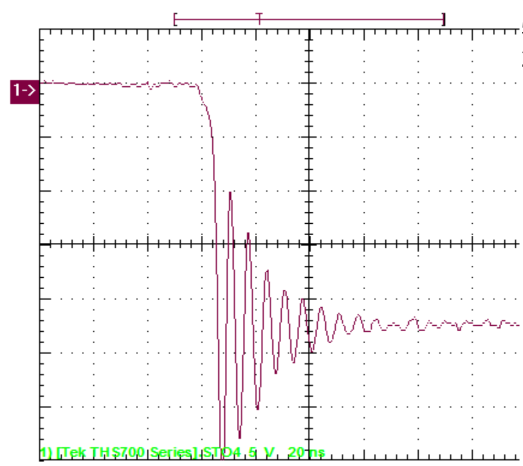
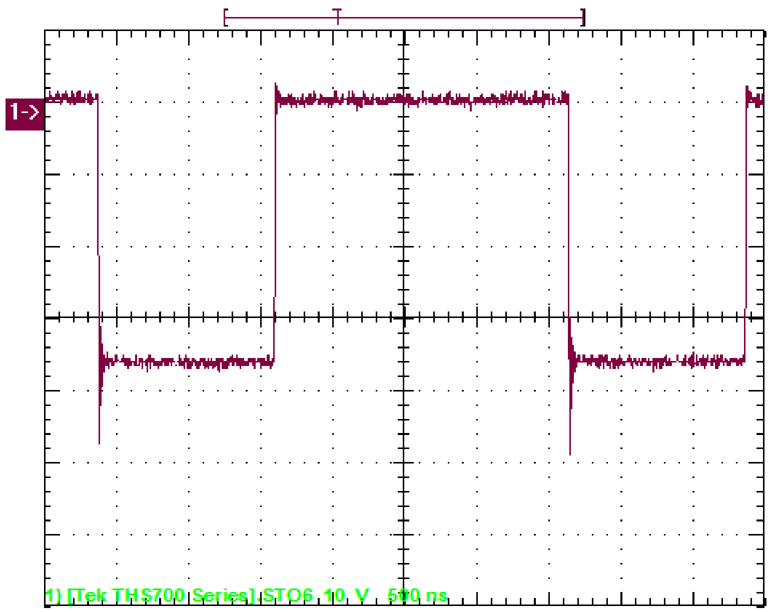
	Ch1 => 5V/div 500ns/div full bandwidth
 	Ch1 => 5V/div 20ns/div

Figure 28

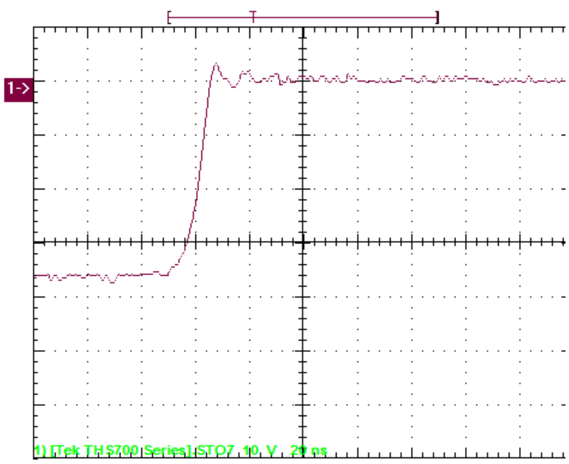
The waveform of the voltage is shown in Figure 29. Input voltage was set to 24V.

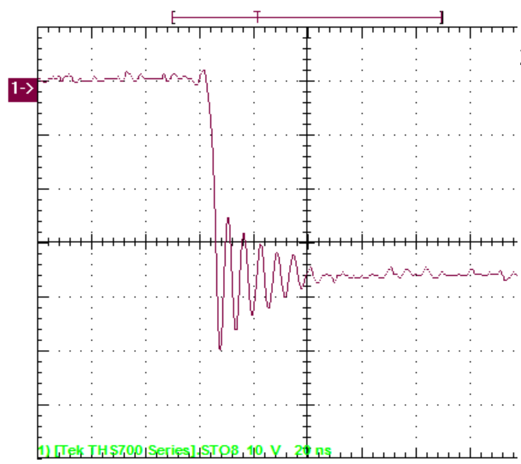


Ch1 =>
10V/div

500ns/div

full bandwidth





Ch1 =>
10V/div
20ns/div

Figure 29

The waveform of the voltage is shown in Figure 30. Input voltage was set to 36V.

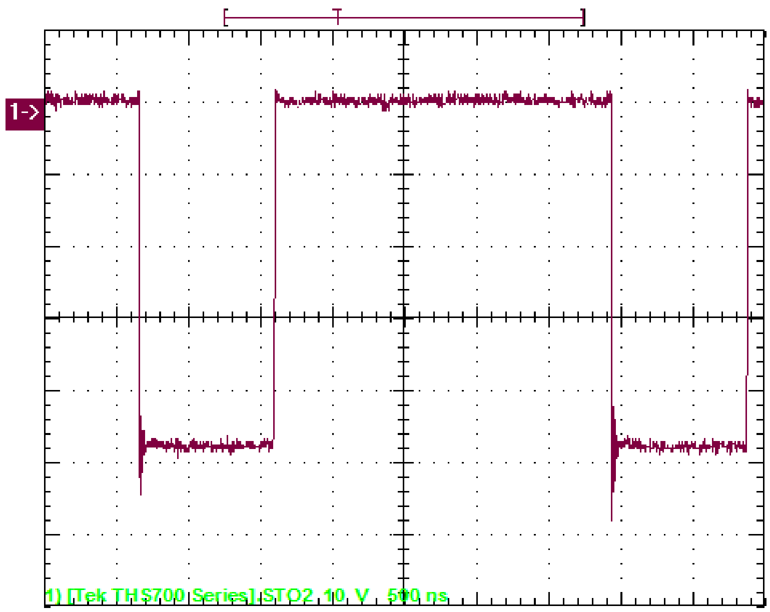
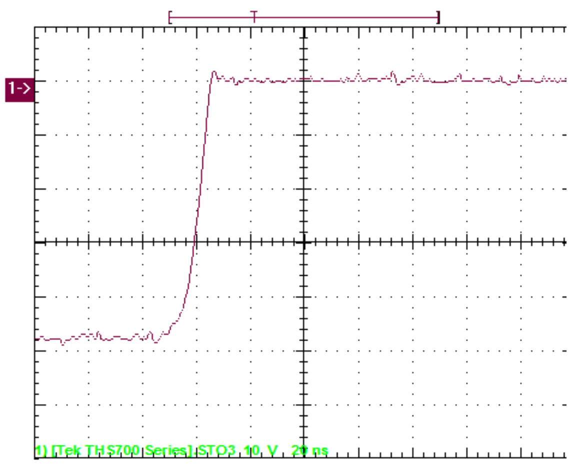
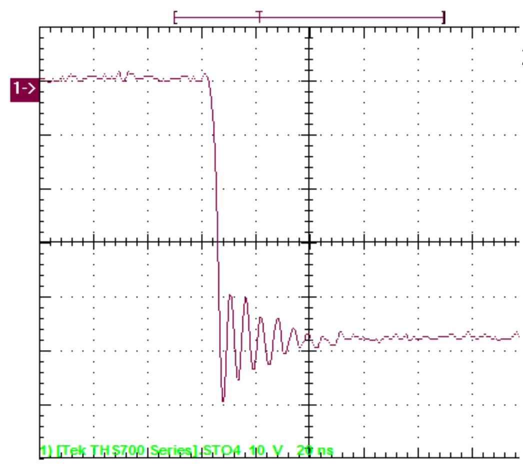
	Ch1 => 10V/div 500ns/div full bandwidth
 	Ch1 => 10V/div 20ns/div

Figure 30

11 Thermal Image

Figure 31 shows the thermal image at 24V input voltage and full load 1.5A for >1hr.

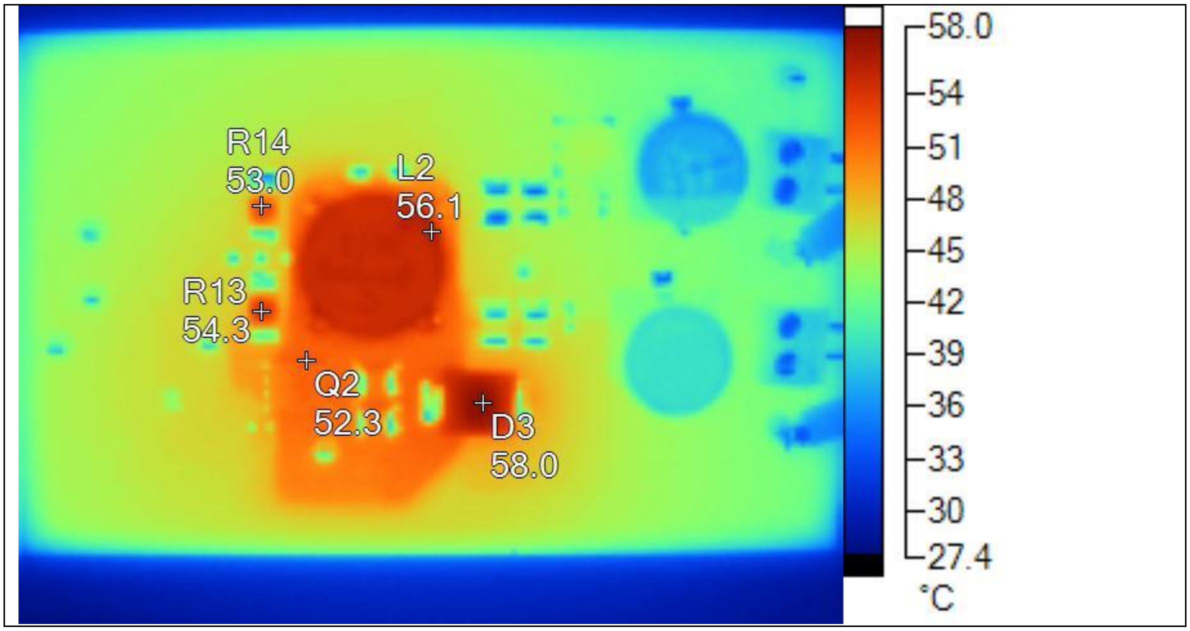


Figure 31

Name	Temperature
D3	58.0°C
L2	56.1°C
R14	53.0°C
R13	54.3°C
Q2	52.3°C