

Test Data For TIDA-00558 09/18/2015





Table of Contents

1.	De	sign Specifications	2
Вι	ıck M	ode	2
В	oost N	Лоde	3
2.	De	sign Description	3
Sy	/stem	Overview:	4
ΤI	DA-00	0558 Design and Debug Flow	4
3.	TIE	DA-00558 Board Photos	5
	3.1	Buck Mode Board Setup	6
	3.2	Boost Mode Board Setup	6
4	Ca	libration Results	7
5	Ро	st Calibration Readings	10
6	Th	ermal Data	11
7	Eff	iciency	12
	7. 1.	Efficiency of Phase 1 & 2 Buck Mode	12
	7.1	Efficiency of Phase 1 & 2 Boost Mode	12
8	PW	VM Waveforms	13
	8.1	Inductor Current and PWM Waveform – BUCK Mode at 56A Load	13
	Q D	Inductor Current and DWM Waveform - Roost Mode at 564 Load	1 /

1. Design Specifications

Buck Mode

Vin Minimum	36V
Vin Maximum	56V
Vin Nominal	48V
Vout	12VDC
lout	56A CV Mode Load set at 48V
Switching Frequency(SMPS)	150KHz
Total Power	672W
Number of Phases	2
Load Distribution Per Phase	28A



Boost Mode

Vin Minimum	9V
Vin Maximum	16V
Vin Nominal	12V
Vout	48VDC
lout	56A CV Mode Load set at 12V
Switching Frequency(SMPS)	150KHz
Total Power	672W
Number of Phases	2
Load Distribution Per Phase	28A

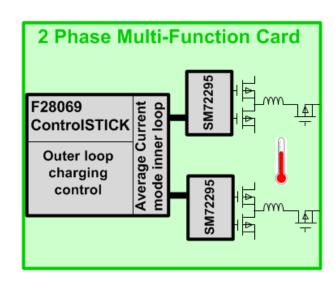
2. Design Description

To address ever tightening fuel economy demands the automotive industry is adopting two battery power systems to facilitate Stop-Start operation in which the internal combustion engine shuts down when stopped or coasting, and automatically restarts when power is applied. Typically a 12V lead acid battery will be used to power many of the car's traditional systems, but a 48V Lithium battery will be used to operate the starter. That same 48V battery will provide a storage reservoir to capture regenerative braking or coast down energy. This creates a need to move power bi-directionally between the two batteries depending on overall system needs.

This application note will address deploying the SM72295 in a 48:12 bidirectional charger.

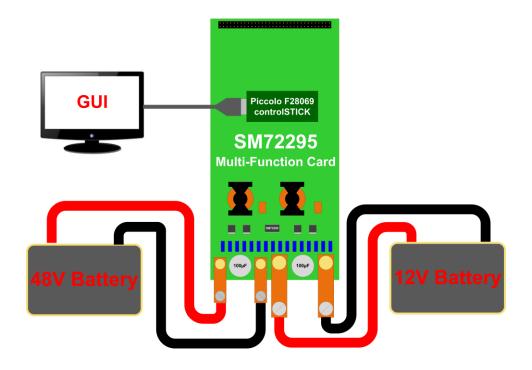
The main features of 48-12 Bi-Directional Power Converter TIDA-00558 are as followed:

- Nominal 48V-to-12V bidirectional
- 28A per phase
- 150kHz operation
- 2 Phases per card
- One SM72295 per phase
- One C2000 control stick per card
- Average current mode control inner loop
- Voltage mode outer loop
- Firmware OCP & OVP
- GUI monitoring & control of power transfer

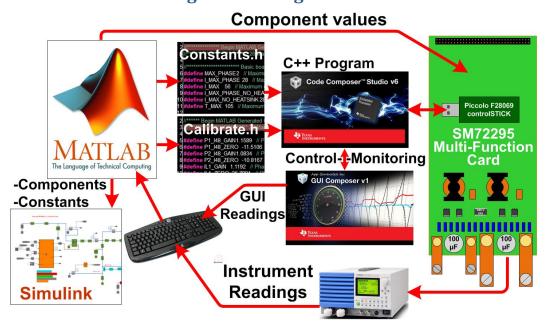




System Overview:



TIDA-00558 Design and Debug Flow:





3. TIDA-00558 Board Photos

Board Dimensions: 8660mil *6340mil



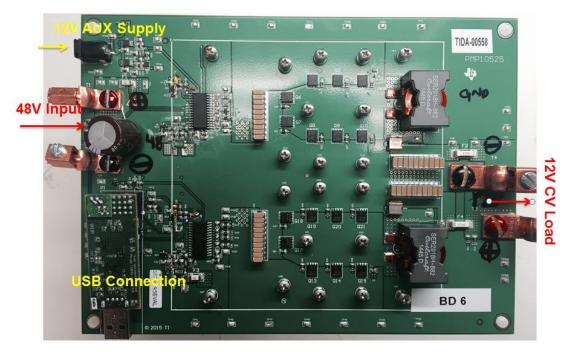
Board Photo (Top)



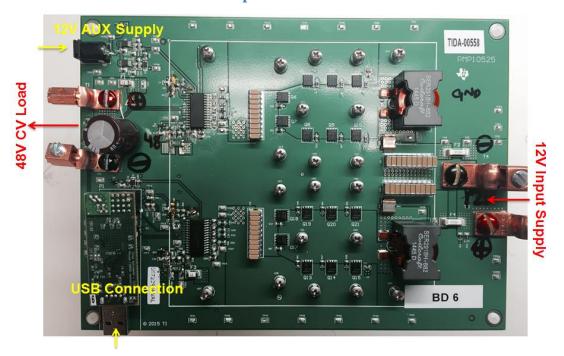
Board Photo (Side View)



3.1 Buck Mode Board Setup



3.2 Boost Mode Board Setup





4 Calibration Results

<mark>Load</mark>		resures		
SetPoin t	P1 I48 Raw	P1 I48 Standard	P1_I48_Calculated	P1 I48 Error
-28	3.87	-6.666	-6.719	0.795149
	5.5	-4.942	-4.96424	0.450006
-15	6.56	-3.818	-3.8231	0.133671
-10	7.64	-2.674	-2.66044	-0.50722
-5	8.75	-1.526	-1.46547	-3.96632
5	11.15	0.945	1.11823	18.33117
10	12.06	2.2	2.097884	-4.64164
15	13.3	3.5	3.432797	-1.92007
20	14.69	4.868	4.929192	1.257033
28	16.61	7.055	6.996155	-0.83409
<mark>LoadSet</mark>				
<mark>Point</mark>	P2_I48_Raw	P2_I48_Standard	P2_I48_Calculated	P2_I48_Error
-28	3.96	-6.52	-6.52523	0.080165
-20	5.59	-4.812	-4.8153	0.068551
-15	6.66	-3.686	-3.69283	0.18531
-10	7.75	-2.552	-2.54938	-0.1026
-5	8.87	-1.392	-1.37446	-1.25993
5	11.17	1.024	1.03832	1.398458
10	12.34	2.278	2.265692	-0.5403



15	13.55	3.547	3.535025	-0.33761
20	14.81	4.845	4.85681	0.243756
28	16.84	6.993	6.986352	-0.09506
<mark>Load</mark> SetPoin				
t	IL1_Raw	IL1_Standard	IL1_Calculated	IL1_Error
-28	6.8	-29.026	-28.7875	-0.82174
-20	13.76	-21.056	-21.1555	0.472521
-15	18.29	-16.062	-16.1881	0.785226
-10	22.74	-11.151	-11.3085	1.412215
-5	27.29	-6.38	-6.31917	-0.95338
5	36.35	3.61	3.615568	0.154226
10	40.9	8.592	8.604869	0.149784
15	45.43	13.542	13.57224	0.223308
20	49.97	18.532	18.55058	0.100241
28	57.24	26.506	26.52249	0.062228
<mark>Load</mark> SetPoin				
t	IL2_Raw	IL2_Standard	IL2_Calculated	IL2_Error
-28	6.61	-28.242	-28.0766	-0.58579
-20	13.69	-20.395	-20.4758	0.396007
-15	18.25	-15.451	-15.5803	0.837083
-10	22.8	-10.844	-10.6956	-1.36808
-5	27.33	-5.705	-5.83242	2.233557
5	36.39	3.938	3.894018	-1.11687



10	40.92	8.8	8.757239	-0.48592
15	45.48	13.632	13.65267	0.151603
20	50.01	18.48	18.51589	0.194197
28	57.27	26.256	26.30992	0.205378
V12_Set				
<mark>Point</mark>	V12_Raw	V12_Standard	V12_Calculated	V12_Error
9	9	9.1999	9.20938	0.10305
10	9.97	10.2009	10.20164	0.00722
11	10.94	11.1997	11.19389	-0.05185
12	11.9	12.201	12.17592	-0.20556
13	12.92	13.201	13.21932	0.138795
14	13.88	14.199	14.20135	0.016543
V48_Set				
V48_Set Point	<mark>V48_Raw</mark>	V48_Standard	V48_Calculated	V48_Error
		V48_Standard 36.67	V48_Calculated 36.67442	V48_Error 0.012045
Point Point	V48_Raw			
Point 36	V48_Raw 35.92	36.67	36.67442	0.012045
Point 36 40	V48_Raw 35.92 39.87	36.67 40.76	36.67442 40.76281	0.012045 0.006895
Point 36 40 44	V48_Raw 35.92 39.87 43.81	36.67 40.76 44.847	36.67442 40.76281 44.84085	0.012045 0.006895 -0.01371
Point 36 40 44 48	V48_Raw 35.92 39.87 43.81 47.76	36.67 40.76 44.847 48.936	36.67442 40.76281 44.84085 48.92925	0.012045 0.006895 -0.01371 -0.0138
Point 36 40 44 48 52	V48_Raw 35.92 39.87 43.81 47.76 51.71	36.67 40.76 44.847 48.936 53.019	36.67442 40.76281 44.84085 48.92925 53.01764	0.012045 0.006895 -0.01371 -0.0138 -0.00257
Point 36 40 44 48 52	V48_Raw 35.92 39.87 43.81 47.76 51.71 55.66	36.67 40.76 44.847 48.936 53.019	36.67442 40.76281 44.84085 48.92925 53.01764	0.012045 0.006895 -0.01371 -0.0138 -0.00257
Point 36 40 44 48 52 56 Param	V48_Raw 35.92 39.87 43.81 47.76 51.71 55.66 STDEV	36.67 40.76 44.847 48.936 53.019	36.67442 40.76281 44.84085 48.92925 53.01764	0.012045 0.006895 -0.01371 -0.0138 -0.00257



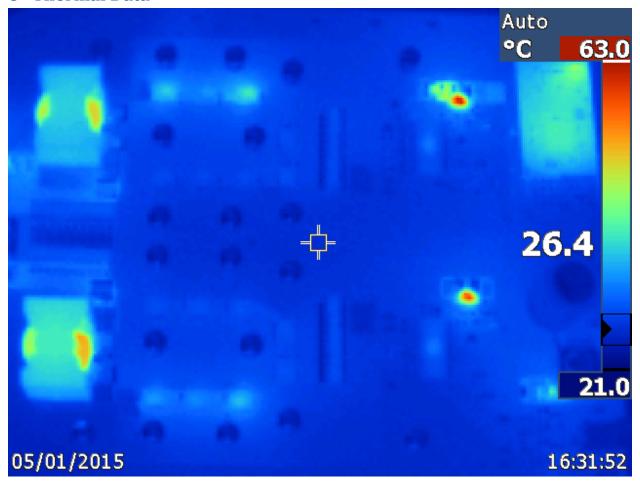
IL2	1.034205
V12	0.122592
V48	0.012075

5 Post Calibration Readings

Phase1 BUCK	Load Set Point (A)	GUI Reading	STND value	% Error	Phase2 Boost	Load Set PT	GUI Reading	Standered Reading Metter	%error
	5	4.99	4.978	0.24048		5	4.99	5.06	-1.40281
	10	9.98	9.972	0.08016		10			
	15	14.97	14.934	0.24048		15	14.97	14.851	0.794923
	20	19.96	19.95	0.0501		20			
	28	27.97	27.928	0.15016		28	27.43	27.52	-0.32811
	56	55.96	55.582	0.67548		56	55.73	55.58	0.269155
V-12	10	12.24		0.16339	V-48	10	47.96	48.14	-0.37531
V-48	10	48.92		-0.01635	V-12	10	12.08	12.035	0.372517
Phase1 BUCK	Load Set Point (A)	GUI Reading	STD value	%error	Phase2 Boost	Load Set Point (A)		Standered Reading Meter	%error
	5	5.03	5.088	-1.15308		5	4.94	4.88	1.214575
	10					10			
	15	14.99	14.98	0.066711		15	14.96	14.82	0.935829
	20	20	20.024	-0.12		20			
	28	28.02	28.01	0.035689		28	27.84	28.04	-0.71839



6 Thermal Data



IR thermal image taken at steady state with 48Vin and 12Vout@ 56A load (no airflow)-Buck only



7 Efficiency

7. 1. Efficiency of Phase 1 & 2 Buck Mode

Load Set Point (A)	Power In (W)	Power Out (W)	Efficiency %
Phase 1 - 28A	338.5	324.7	96.42
Phase 2 – 28A	336.1	319.27	95
Phase 1&2 – 56A	672.4	639.25	95.08

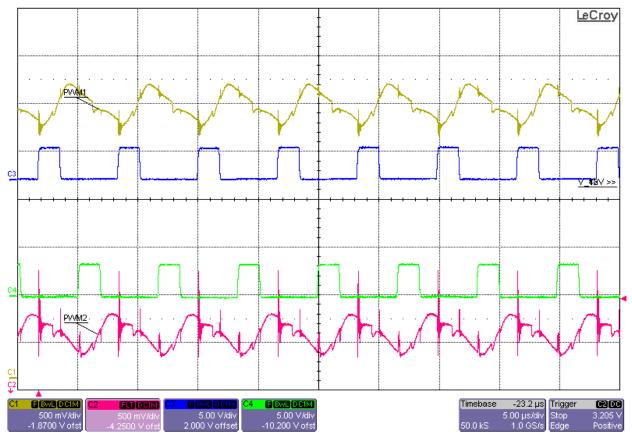
7.1 Efficiency of Phase 1 & 2 Boost Mode

Load Set Point (A)	Power In (W)	Power Out (W)	Efficiency
Phase 1 - 28A	357.50	346.07	96.80%
Phase 2 – 28A	359.42	347.39	96.60%
Phase 1&2 – 56A	733.3	707.54	96.52%



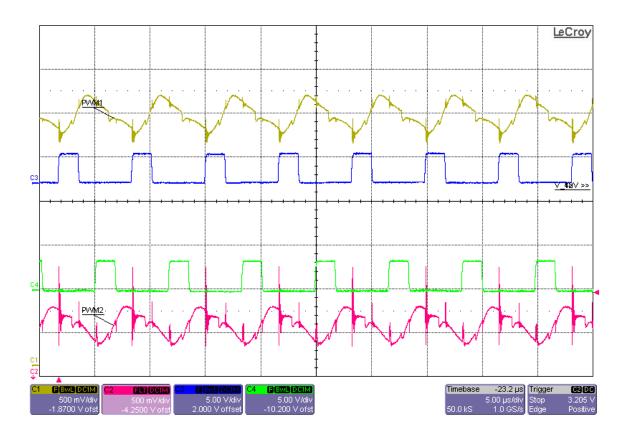
8 PWM Waveforms

8.1 Inductor Current and PWM Waveform – BUCK Mode at 56A Load





8.2 Inductor Current and PWM Waveform – Boost Mode at 56A Load



IMPORTANT NOTICE FOR TI REFERENCE DESIGNS

Texas Instruments Incorporated ("TI") reference designs are solely intended to assist designers ("Buyers") who are developing systems that incorporate TI semiconductor products (also referred to herein as "components"). Buyer understands and agrees that Buyer remains responsible for using its independent analysis, evaluation and judgment in designing Buyer's systems and products.

TI reference designs have been created using standard laboratory conditions and engineering practices. TI has not conducted any testing other than that specifically described in the published documentation for a particular reference design. TI may make corrections, enhancements, improvements and other changes to its reference designs.

Buyers are authorized to use TI reference designs with the TI component(s) identified in each particular reference design and to modify the reference design in the development of their end products. HOWEVER, NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY THIRD PARTY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT, IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI REFERENCE DESIGNS ARE PROVIDED "AS IS". TI MAKES NO WARRANTIES OR REPRESENTATIONS WITH REGARD TO THE REFERENCE DESIGNS OR USE OF THE REFERENCE DESIGNS, EXPRESS, IMPLIED OR STATUTORY, INCLUDING ACCURACY OR COMPLETENESS. TI DISCLAIMS ANY WARRANTY OF TITLE AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, QUIET ENJOYMENT, QUIET POSSESSION, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS WITH REGARD TO TI REFERENCE DESIGNS OR USE THEREOF. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY BUYERS AGAINST ANY THIRD PARTY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON A COMBINATION OF COMPONENTS PROVIDED IN A TI REFERENCE DESIGN. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, SPECIAL, INCIDENTAL, CONSEQUENTIAL OR INDIRECT DAMAGES, HOWEVER CAUSED, ON ANY THEORY OF LIABILITY AND WHETHER OR NOT TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES, ARISING IN ANY WAY OUT OF TI REFERENCE DESIGNS OR BUYER'S USE OF TI REFERENCE DESIGNS.

TI reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques for TI components are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

Reproduction of significant portions of TI information in TI data books, data sheets or reference designs is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards that anticipate dangerous failures, monitor failures and their consequences, lessen the likelihood of dangerous failures and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in Buyer's safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed an agreement specifically governing such use.

Only those TI components that TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components that have *not* been so designated is solely at Buyer's risk, and Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.