TI Designs

Universal Digital Interface to Absolute Position Encoders

TI Designs

The TIDA-00179 reference design is an EMC-compliant universal digital interface to connect to absolute position encoders like EnDat 2.2, BiSS®, SSI, or HIPERFACE DSL®. The design supports a wide input voltage range from 15 to 60 V (24 V nom). A connector with 3.3-V logic I/O signals allows for direct interface to the host processor to run the master protocol. The design allows the host processor to select between a 4-wire encoder interface like EnDat 2.2 and BiSS or a 2-wire interface with power over RS-485 like HIPERFACE DSL. To meet the selected encoder's supply range, the design offers a programmable output voltage with either 5.25 or 11 V. This design's power supply offers protection against overvoltage and short circuit according to the selected encoder's voltage range to prevent damage during a cable short. The TIDA-00179 has been tested up to 100-m cable length with EnDat 2.2 and 2-wire HIPERFACE DSL encoders.

Design Resources

TIDA-00179	Design Folder
SN65HVD78	Product Folder
TPS54060A	Product Folder
TPS24750	Product Folder
LM2903	Product Folder
SN74CBTLV3257	Product Folder
CSD25402Q3A	Product Folder

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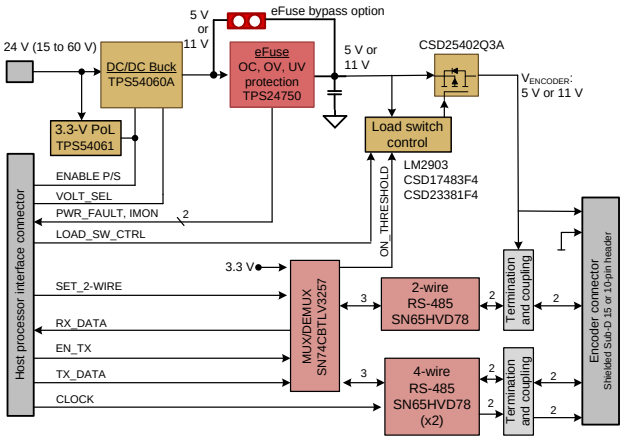
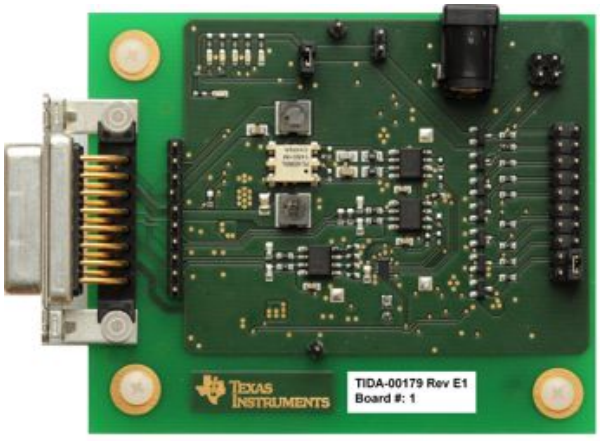
Design Features

- Universal Hardware to Interface With EnDat 2.2, BiSS, SSI, and 4-Wire or 2-Wire HIPERFACE DSL Encoders. Supports All Corresponding Standard Data Rates up to at Least 100-m Cable Length
- 3.3-V Supply Half-Duplex RS-485 Transceiver SN65HVD78 With 12-kV IEC-ESD and 4-kV EFT Eliminates Cost for External ESD Components
- Encoder P/S With Wide Input Range (15 to 60 V) Offers Programmable Output Voltage 5.25 or 11 V, Compliant to EnDat 2.2, BiSS, or HIPERFACE DSL Encoders
- OV, UV, OC, and SC Protections With Precise Current Limit Leveraging TI eFuse Technology With Current Monitor and Fault Indicator
- Logic Interface (3.3-V I/O) to Host Processors Like Sitara™ AM437x or C2000™ MCU to Run EnDat 2.2, BiSS, SSI, or HIPERFACE DSL Master
- Design Exceeds EMC Immunity for ESD, Fast Transient Burst, Surge, and Conducted RF With Levels According to IEC61800-3

Featured Applications

- Servo Drives
- Industrial Drives
- Factory Automation and Control





1 System Description

1.1 TI Design Overview

This TI Design implements an EMC-compliant universal digital interface to absolute position encoders like EnDat 2.2, BiSS, or HIPERFACE DSL.

The major building blocks of this TI hardware design are the bidirectional 4-wire RS-485 interface and the 2-wire bidirectional RS-485 interface with power of RS-485 along with a multiplexer or de-multiplexer to select the active encoder interface, the encoder power supply with programmable output voltage and overvoltage, overcurrent, and short-circuit protection as well as a 3.3-V digital interface to a host processor to run the corresponding encoder standard protocol. The host processor that runs the corresponding encoder master protocol is not part of this design.

Figure 1 shows a simplified system block of a universal digital interface module as a subsystem of an industrial drive to connect to absolute, with the TI Design represented by the box in light green.

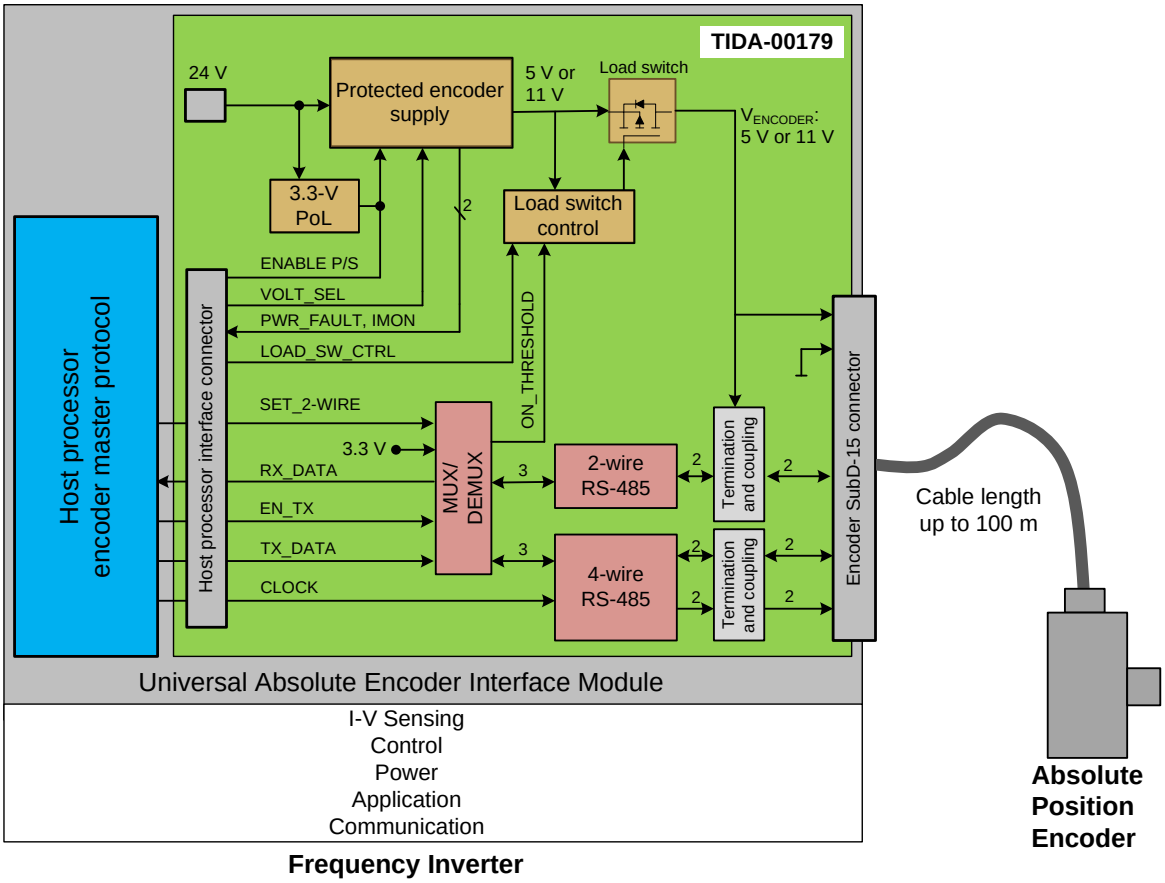


Figure 1. Industrial Drive With Universal Digital Interface to Absolute Position Encoders

The design is powered through industry standard 24 V and features a wide input voltage range from 15 to 60 V. A connector with 3.3-V logic I/O signals allows for a direct interface to the host processor like Sitara AM437x or C2000 MCU to run the corresponding encoder's master protocol. The design allows the host processor to activate either the 4-wire RS-485 physical interface to connect to an EnDat 2.2, BiSS, or SSI encoder, or the 2-wire RS-485 interface with power over RS-485 to connect to a HIPERFACE DSL encoder. To meet the selected encoder's supply ranges and specifications, the protected encoder power supply features a programmable output voltage of either 5.25 or 11 V. The voltage along with the voltage ripple and output current was chosen to ensure it is compliant to the overall supply specification for the encoder standards EnDat 2.2, BiSS, SSI, and HIPERFACE DSL. The encoder supply is also protected against short circuit, and the overvoltage threshold is matched to the selected output voltage with fault feedback.

The absolute position encoder can be connected to the reference design either through a SubD-15 connector or a 10-pin header. The connector has dedicated pins for connecting a 2-wire HIPERFACE DSL encoder, which includes power over RS-485 and shared pins for EnDat 2.2, BiSS, and SSI position encoders. This design supports cable lengths of up to at least 100 m. For cable specifications, refer to the recommendations of the corresponding encoder vendor.

The design has been tested for EMC immunity against electrostatic discharge (ESD), fast transient burst (EFT), surge, and conducted RF with levels specified per IEC61800-3.

The following sections provide an overview on common encoder standards with focus on the physical layer interface.

1.2 Absolute Position Encoder Interface Standards Overview

There are multiple absolute position encoder standards that use RS-485 or RS-422 based serial digital interfaces with, like EnDat 2.2, BiSS, or HIPERFACE DSL. Further interface standards include PROFIBUS® DP and PROFIBUS IO as well as CAN or Ethernet-based interfaces. Additional standards include proprietary, drive vendor-specific standards, like DRIVE-CLiQ from Siemens™, Fanuc Serial Interface, Mitsubishi® High-Speed Serial Interface, and more.

This TI Design supports the most common industrial serial interfaces such as EnDat 2.2, BiSS, SSI, and HIPERFACE DSL. A brief overview on each of the standards is provided in the following subsections.

1.2.1 EnDat 2.2

The EnDat 2.2 interface from HEIDENHAIN is a purely digital, bidirectional serial interface standard for linear or rotary position feedback encoders. The EnDat 2.2 master sends the type of data transmitted, like absolute position, parameters, and diagnostics, through mode commands to the encoder. The EnDat 2.2 interface is also suited for safety-related applications up to SIL 3.

Figure 2 shows the corresponding example for an EnDat 2.2 position encoder interface to an industrial drive (for example, a servo drive). The position encoder with EnDat 2.2 is connected to the subsequent electronics in the servo drive through a single, 8-wire shielded cable.

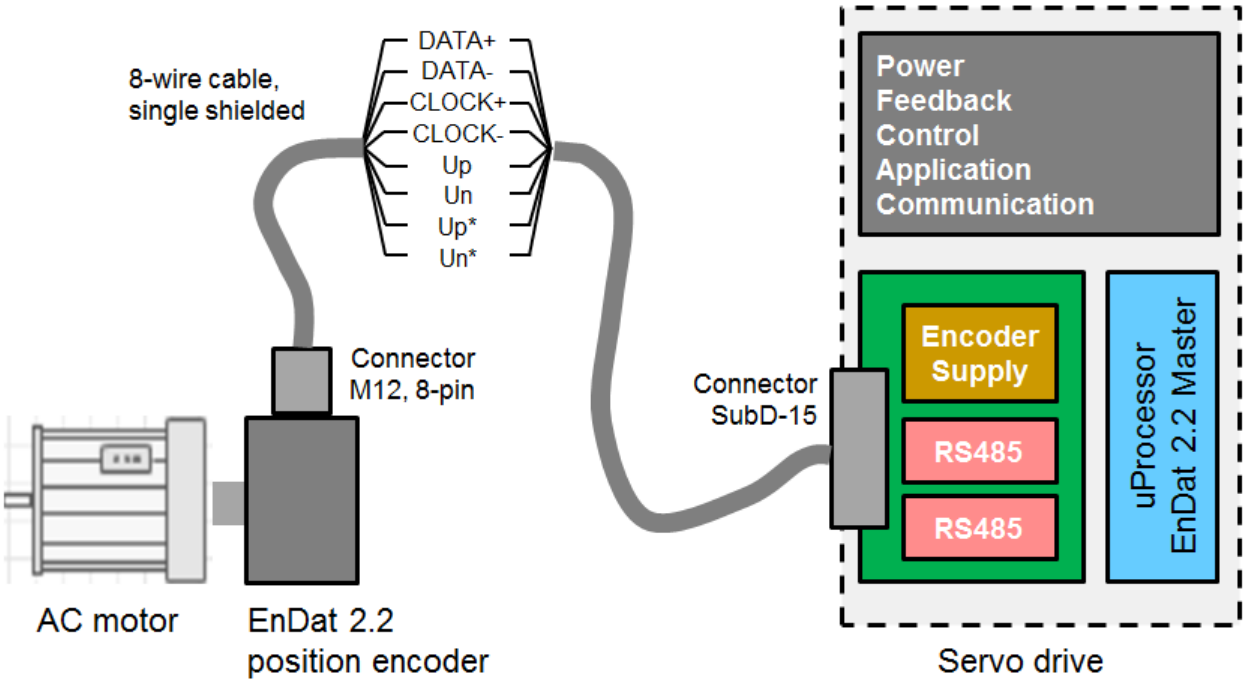


Figure 2. Industrial Drive With EnDat 2.2 Position Encoder Interface

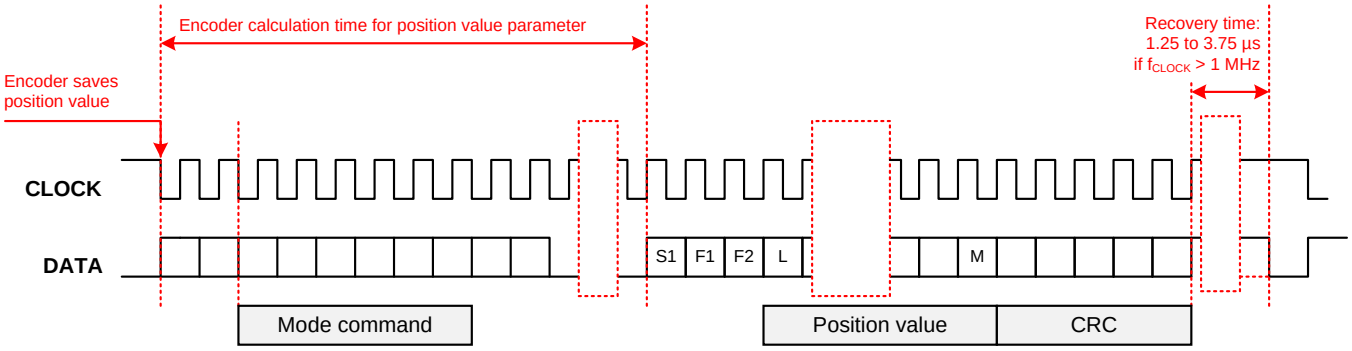
The communication only requires four signal wires. Two wires are for the bidirectional differential data (DATA+ and DATA–) and are transmitted in half-duplex mode. The other two wires are for the differential clock signal (CLOCK+ and CLOCK–). From the remaining wires, two wires are used for the encoder power supply. The other two wires are used for battery buffering or for parallel power supply lines to reduce the cable's losses.

1.2.1.1 EnDat 2.2 Physical Layer

EnDat 2.2 specifies a differential line transmitter and receiver according to EIA standard RS-485 for the differential signals CLOCK+, CLOCK–, DATA+, and DATA–. The differential DATA+ and DATA– signals are bidirectional half-duplex, and the RS-485 transceiver is configured in directional mode with DE and /RE tight together. The differential CLOCK+ and CLOCK– signals are unidirectional and are an output of the subsequent electronics. The data is transmitted and received synchronous to the clock signal, which is generated by the EnDat 2.2 master. On the EnDat 2.2 master, the transmit data changes on the falling edge clock edge. Without delay compensation on the master, the receive data is latched on the rising clock edge. The clock remains high when there is neither data transmitted nor data received.

The clock frequency is variable. The maximum clock frequency depends on the cable length. With propagation-delay compensation in the EnDat 2.2 master, the clock frequency can be from 100 kHz up to 16 MHz, and up to 100-m cable length with 8 MHz. Use of HEIDENHAIN cables is required.

Figure 3 shows a position-value packet-transfer example. After two clock pulses, the EnDat 2.2 master transmits a mode command (encoder transmit position), and the slave encoder replies with the position value, start and error bits, and a 5-bit cyclic redundancy check (CRC).



S = start, **F1** = error 1, **F2** = error 2, **L** = LSB, **M** = MS
Diagram does not include the propagation delay compensation

Figure 3. Position-Value Packet Transfer With EnDat 2.2

Although Figure 3 does not depict propagation delay compensation, the delay compensation is an important function because the delay through a typical encoder cable is around 5 ns/m. With a 10-m cable, the round-trip delay is 100 ns. With a 16-MHz EnDat 2.2 clock, this equals a phase shift of 1.6 clock periods. Therefore, proper delay compensation is a major function of the EnDat 2.2 master.

1.2.1.2 EnDat 2.2 Power Supply

EnDat 2.2 specifies the power supply range from 3.6 to 14 V. The low-frequency output voltage ripple must be less than 100 mV_{PP}. The high frequency interference on the output voltage must be less than 250 mV_{PP} for transients with dU/dt > 5 V/us.

For more details on the EnDat 2.2 specification, please refer to *EnDat 2.2—Bidirectional Interface for Position Encoders* [1].

For details on a TI design for an EMC-compliant interface to EnDat 2.2 encoders, see the TIDA-00172 design guide [11]. For an EnDat 2.2 master implementation on the Sitara AM437x, see the TIDEP0025 design guide [10].

1.2.2 BiSS Interface

The BiSS interface is an open source protocol introduced by iC-Haus GmbH. BiSS defines a digital bidirectional serial interface for actuators and sensors, such as rotary or position encoders. BiSS details can be found at BiSS Interface [7]. BiSS allows serial-synchronous data communication in unidirectional mode or bidirectional mode (BiSS-C continuous mode). The BiSS interface is hardware-compatible to the SSI. The BiSS protocol defines each subscriber into the following data sections: sensor data, actuator data, and register data. Each section can have various setups according to access and transmission performance, depending on the different sensor application. This protocol is referred to as the BiSS master that sends and receives data from the position encoder.

With BiSS linear or rotary position encoders, the BiSS point-to-point configuration is often used as shown in Figure 4. In the point-to-point configuration, only one device with one or more sensors is operated on the master. The MO line is eliminated, and the SL line is routed back directly from the slave.

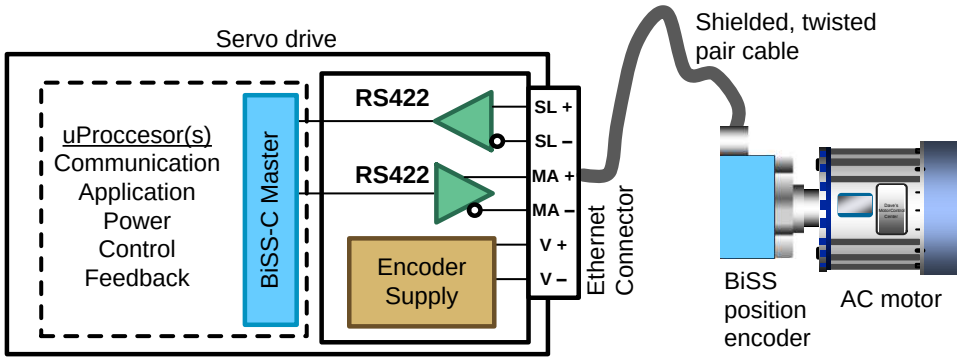


Figure 4. Industrial Drive With BiSS Position Encoder Interface

The point-to-point structure is based on two signals only: MA and SL. Respectively, there are four differential signals, MA+, MA– and SL+, SL–, in unidirectional full-duplex mode. Two additional wires are for the encoder power supply, V+ and V–, where V– is typically the GND.

1.2.2.1 BiSS Physical Layer

The BiSS interface has two PHY options. One option is based on the TIA/EIA-422 standard, and the other option uses the LVDS TIA/EIA-644 standard. BiSS specifies a differential line transmitter and receiver according to EIA standard RS-422 for the differential signals MA+, MA–, SL+, and SL–. Two lines are for the unidirectional differential data receive (SL+ and SL–) and are transmitted in full-duplex mode. Two lines are for the differential clock and data transmit signal (MA+ and MA–). The BiSS master starts the transmission frame with the clock MA. The first rising edge at MA synchs the slaves. With the second rising edge of MA, the slaves set the SLO line to "0" and generate an acknowledge signal (Ack). In the point-to-point configuration, the start bit is generated by the last slave. The start bit is then passed on synchronously with the clock MA from each slave delayed by one clock pulse, while the CDS bit is either passed on by the slave or is set according to the rules of the control. The output of the slave device (SLO) is directly connected to the SL input of the master in this case.

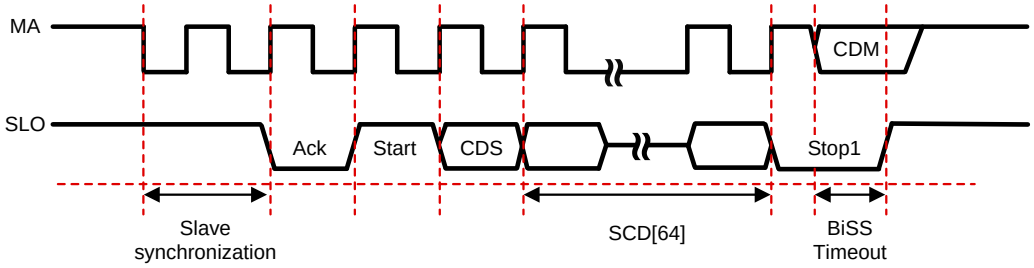


Figure 5. BiSS-C Data Frame Example for a Point-to-Point Setup

Figure 5 does not include the line delay. To determine the line delay, the BiSS master measures the delay from the second rising MA edge to the received falling edge of the Ack bit of the slave response (SL: Ack). The line delay is carried out again with each BiSS frame. Therefore, the line delay also takes aging and temperature-dependent drift effects into account.

The MA-clock frequency varies. The recommended MA-clock frequency depends on the cable length as outlined in Table 1, which was generated using Table 1 in the document *AN15: BiSS C MASTER OPERATION DETAILS (preliminary)* from BiSS Interface [8].

Table 1. Recommended BiSS MA-Clock Frequencies versus Cable

CABLE LENGTH	BiSS MA FREQUENCY
Up to 10 m	10 MHz
Up to 25 m	5 MHz
Up to 60 m	2 MHz
Up to 100 m	1 MHz
Up to 200 m	500 kHz
Up to 500 m	200 kHz
Up to 1000 m	100 kHz

This line delay is specified to be 40 µs maximum. The line delay compensation enables accelerated communication with high data rates of typically 10 Mb/s. Table 2 outlines an extract of timing requirements with respect to the signal MA.

Table 2. Timing Requirements for BiSS-C Interface

NO.	SYMBOL	PARAMETER	CONDITION	MIN	MAX	UNIT
1	$1/T_{MA}$	Clock frequency	Signal MA	80	10,000 (with RS-422)	kHz
8	$t_{LineDelay}$	Propagation delay MA → SL	Measured from the second rising MA edge to the first falling SL edge	0	40	µs
9	$t_{LineJitter}$	Delay jitter MA → SL	Within a BiSS frames	–25	25	$\%T_{MA}$

1.2.2.2 BiSS Encoder Power Supply

BiSS encoders are available from multiple vendors and typically require either a 5-V or 10-V to 30-V supply. The supply voltage specification is vendor specific including input voltage tolerance and supply current.

For more details on the BiSS specification, refer to BiSS Interface [7].

For details on a TI design for an EMC compliant interface to BiSS encoders, see the TIDA-00175 design guide [12]. For the master implementation, see the TIDEP0022 design guide [9].

1.2.3 HIPERFACE DSL

HIPERFACE DSL is a digital protocol specified and owned by Sick. HIPERFACE DSL is derived from HIgh PERformance InterFACE Digital Servo Link. The robustness of the protocol enables the connection to the motor feedback system through the motor connection cable and simplifies the installation of an encoder system in the drive.

Key features of HIPERFACE DSL 2-wire physical interface are:

- Digital interface compliant to RS-485 standard with a transfer rate of 9.375 MBaud
- Half-duplex communication with the encoder through dual wires
- Power supply and communication with the encoder carried out using the same dual wires. The connection cables to the encoder are routed as a shielded, twisted pair cable in the power supply cable to the motor. Therefore, no separate cable for the encoder plug connector is required
- Cable length between the frequency inverter and the encoder up to 100 m, without degradation of the operating performance

HIPERFACE DSL can be used in two different interface circuit configurations. Each configuration requires a different kind of connection cable. When using a separate encoder cable, the 4-wire interface is used. To use a 2-wire cable integrated in the motor cable (as shown in Figure 6), a transformer is required to increase common mode rejection ratio. The supply voltage and GND are coupled onto the RS-485 differential signals through inductors L1 and L2, and DC is decoupled to the transformer through capacitors C3 and C4, respectively. The differential RS-485 signals after the transformer are AC coupled into the two wires through wires. The corresponding values of the passive components for line termination are provided in the HIPERFACE DSL specification. R1 = R2 = 56 Ω, C1 = 100 ns, C2 = 2.2 µF/16 V, C3 = C4 = 470 nF/50 V. L1 = L2 = 100 µH.

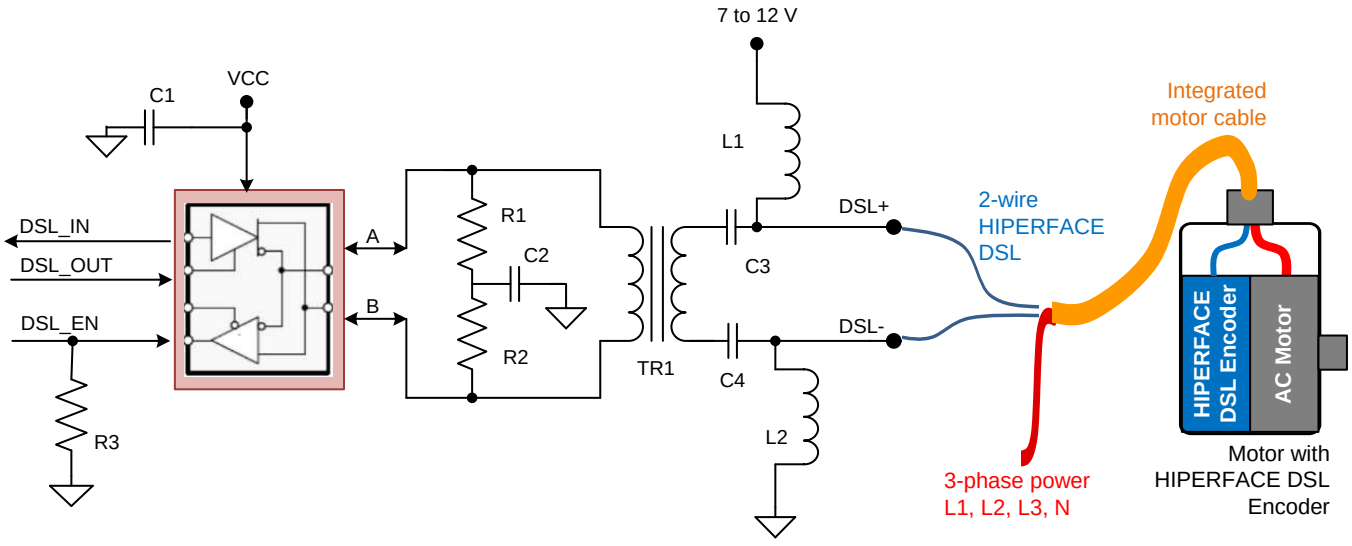


Figure 6. 2-Wire HIPERFACE DSL Interface With Integrated Motor Cable

1.2.3.1 HIPERFACE DSL Physical Layer

As a physical layer, HIPERFACE DSL uses a transfer in accordance with EIA-485 (RS-485). Valid RS-485 interface drivers must comply with the conditions in Table 3.

Table 3. RS-485 Transceiver Specifications

CHARACTERISTIC	VALUE
Transfer rate	≥ 20 MBaud
Permitted common mode voltage	–7 to 12 V
Minimum differential input voltage detected	< 200 mV
Minimum load resistance	< 55 Ω
Receiver propagation delay	< 60 ns
Transmitter propagation delay	< 60 ns
Transmitter power-up delay	< 80 ns
Transmitter power-down delay	< 80 ns
Transmitter rise time	< 10 ns
Transmitter fall time	< 10 ns

1.2.3.2 HIPERFACE DSL Power Supply

Motor feedback systems with HIPERFACE DSL have been developed to operate with a supply voltage of 7 to 12 V. The voltage supply is measured at the encoder plug connector. The specification for the HIPERFACE DSL power supply is listed in Table 4.

Table 4. HIPERFACE DSL Power Supply Specification

PARAMETER	VALUE
Operating supply voltage	7 to 12 V
Supply voltage power-up ramp time (0 to 7 V)	< 180 ms
Inrush current (0 to 100 µs)	≤ 3.5 A
Inrush current (100 to 400 µs)	≤ 1 A
Operating current (> 400 µs)	≤ 250 mA at 7 V

For details on the HIPERFACE DSL protocol, see the *HIPERFACE DSL Implementation Manual* [3].

For details on a TI design for a 2-wire interface to a HIPERFACE DSL encoder, see the TIDA-00177 design guide [13].

1.2.4 SSI

SSI is a unidirectional serial protocol over RS-422. The unidirectional clock is generated by the master and is specified from 80 kHz to 2 MHz. The receive data is unidirectional too with the MSB transmitted first. SSI does not support propagation delay compensation. Multiple encoder vendors manufacture absolute position encoders with SSI.

The clock is high when inactive. To initiate a data transfer, the clock goes low and the position is stored. On the first rising edge of the clock signal, the MSB is shifted out at the SSI encoder. On the second rising edge, the MSB-1 is shifted out, and so on, until the last bit (LSB) is shifted out. After another clock cycle, the clock remains high until the next data transfer is started. Depending on the time-out, the current latched position or a new position value are transmitted on the next transfer. For details, refer to the datasheet of the corresponding SSI encoder.

1.2.5 Common Requirements for an Absolute Position Encoder Interface

1.2.5.1 Comparison of Physical Layer and Power Supply Requirements

Table 5 shows a comparison of four standards (EnDat 2.2, HIPERFACE DSL, BiSS, and SSI) with regards to physical layer and supply voltage. Figure 7 shows an overview in the maximum clock versus cable length.

Table 5. EnDat 2.2, BiSS, SSI, and HIPERFACE DSL Interface

PROTOCOL	ENDAT 2.2	BiSS	HIPERFACE DSL	SSI
Owner	HEIDENHAIN	iC-Haus	Sick	Sick (Max Stegmann)
Serial bit rate(1)	100 kbps to 16 Mbps	80 kbps to 10 Mbps	9.375 Mbps	80 kHz to 2 MHz(2)
Cable length(1)	0 to 100 m (300 m)	0 to 100 m (1000 m)	0 to 100 m	NA(2)
Propagation delay compensation	Yes	Yes	Yes	No
Cable wires for Communication + Power (min)	4+2	4+2	2 (or 2+2)	4+2
PHY	RS-485	RS-422	RS-485	RS-422
PHY data	Half-duplex (bidirectional)	Full-duplex (unidirectional)	Half-duplex, Manchester encoded (bidirectional)	Unidirectional
PHY clock	Unidirectional (master)	Unidirectional (master)	N/A (SYNC through master)	Unidirectional (master)
Power supply	3.6 to 14 V	5 V or 10 to 30 V(2)	7 to 12 V, 250 mA(3)	NA(2)

(1) See Figure 7 for maximum clock frequency versus cable length
(2) Encoder vendor specific
(3) 250 mA is the max consumption in steady state. At startup, the current profile is 3.5 A (100 us) and 1 A (400 µs).

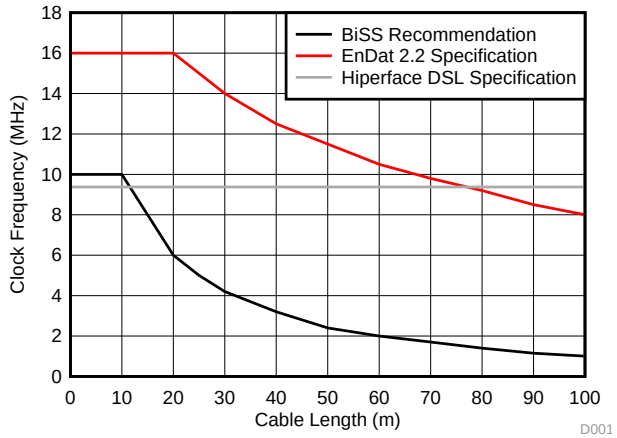


Figure 7. Maximum Clock Frequency versus Cable Length Specifications from 0 to 100 m

1.2.5.2 RS-422/RS-485 Transceiver Specification

Table 6 lists the basic specification for an RS-422/RS-485 transceiver applicable to all four standards.

Table 6. Transceiver Requirements

PARAMETER	VALUE
Standard	RS-485
Configuration	Half-duplex
Baud rate	≥ 32 Mbps
Max receive and transmit propagation delay	< 60 ns
Transmitter rise and fall time	< 10 ns

1.2.5.3 Encoder Power Supply Specification

Table 7 lists the basic specification for universal power supply applicable to all four standards.

Table 7. Encoder Power Supply Requirements

PARAMETER	VALUE
Output voltage[(1)]	Programmable: 5 V and any voltage from 7 to 12 V (For example, 11 V)
Output voltage ripple (transient)	<100 mV_{PP}, <250 mV at dV/dt >5 V/us
Output current (continuous/peak)	250 mA (continuous), 3.5-A/1-A (peak 100 µs/400 µs)

(1) Need to consider enough voltage margin because the supply voltage is specific at the encoder input

2 Design Features

This TI Design implements an industrial temperature and EMC-compliant universal digital interface to absolute position encoders like EnDat 2.2, BiSS, SSI, or HIPERFACE DSL.

The major building blocks of this TI Design's hardware are: the 4-wire and the 2-wire bidirectional RS-485 interfaces along with a multiplexer/de-multiplexer to select the active encoder interface; the encoder power supply with programmable output voltage and overvoltage, overcurrent, and short-circuit protection; and a 3.3-V digital interface to a host processor to run the corresponding encoder standard protocol. The host processor to run the corresponding encoder master protocol is not part of this design.

The main features of this design are:

- Universal hardware to interface to EnDat 2.2, BiSS, SSI, and HIPERFACE DSL encoders, supports all corresponding standard data rates up to at least 100-m cable length
- Industry standard 24-V DC supply input with wide input voltage range from 15 to 60 V. The input is protected against reverse polarity. Onboard DC/DC to generated 3.3-V point-of-load
- 3.3-V supply half-duplex RS-485 transceiver SN65HVD78 with 12-kV IEC-ESD and 4-kV EFT eliminates cost for external ESD components.
- Encoder P/S with wide input range (15 to 60 V) and programmable output voltage 5.25 V or 11 V, compliant to EnDat 2.2, BiSS, or HIPERFACE DSL encoders
- OV, UV, and precise overcurrent limit with short-circuit protection leveraging TI eFuse technology with current monitor (IMON) and fault Indicator. Option to bypass eFuse if protection features not required
- Host processor interface (3.3-V I/O) to processors like Sitara AM437x or C2000 MCU to run the EnDat 2.2, BiSS, or HIPERFACE DSL master.
- LEDs for status indication
- Meets EMC immunity for ESD, EFT, surge, and conducted RF with levels according to IEC61800-3

2.1 Input Supply Voltage With Reverse Polarity Protection

This design features a 24-V DC input with a wide input voltage range from 15 to 60 V. The input is protected against reverse polarity. An EMI input filter is added to minimize conducted emissions. Two wide input voltage onboard DC/DC power supplies are available to generate the corresponding supply voltage for the encoder as well as a 3.3-V point-of-load.

Table 8. Input Power Supply Specification

CHARACTERISTICS	VALUE
Input voltage	15 to 60 V, 24 V (nominal)
Max. input current	500 mA
Reverse polarity protection	Yes
Input EMI filter	Yes
Connector	DC jack (3.5 mm)

2.2 Absolute Encoder Interface

The design offers a shielded SubD-15 female or 10-pin male standard header to connect an absolute encoder. The additional 10-pin header is made available for further flexibility and use with a custom specified shielded connector.

Table 9. Encoder Connector Assignment (SubD-15 Female)

PIN	NAME	DESCRIPTION	LEVEL	ENCODER STANDARD
1	DSL4–	DATA–	RS-485	HIPERFACE DSL (4-wire)
2	GND	Encoder Supply Return	GND	All(1)
3	DSL4+	DATA+	RS-485	HIPERFACE DSL (4-wire)
4	VENCODER	Encoder Supply Voltage	5.25 V or 11 V	All(1)
5	DATA+	DATA+ (EnDat 2.2) or SL+ (BiSS)	RS-485	EnDat 2.2, BiSS, SSI
6	DSL2+	DSL+	RS-485+Power (11 V)	HIPERFACE DSL (2-wire)
7	DSL2–	DSL–	RS-485+Power (GND)	HIPERFACE DSL (2-wire)
8	CLOCK+	CLOCK+ (EnDat 2.2) or MA+ (BiSS)	RS-485	EnDat 2.2, BiSS, SSI
9	—	—	—	—
10	Un* (0 V)	Remote Sense Supply Voltage Return	GND	EnDat 2.2
11	—	—	—	—
12	Up*	Remote Sense Supply Voltage	5.25 V or 11 V	EnDat 2.2
13	DATA–	DATA– (EnDat 2.2) or SL+ (BiSS)	RS-485	EnDat 2.2, BiSS, SSI
14	—	—	—	—
15	CLOCK–	CLOCK– (EnDat 2.2) or MA+ (BiSS)	RS-485	EnDat 2.2, BiSS, SSI

(1) Not required for HIPERFACE DSL 2-wire interface

2.2.1 2-Wire and 4-Wire RS-485 Interface

To be compatible with the recommended physical layer and line termination for HIPERFACE DSL, EnDat 2.2, BiSS, and SSI, the RS-485 transceiver section is split in two subsystems:

- The 4-wire RS-485 interface to support standards like EnDat 2.2, BiSS, or SSI
- The 2-wires RS-485 interface to support HIPERFACE DSL

The 2-wire and 4-wire encoder RS-485 differential signals are assigned to separate pins on the encoder connector. Only one interface type is active at a time—either the 2-wire or 4-wire. The active interface can be selected by the host processor as well as the encoder voltage (5.25 V or 11 V). Refer to Section 2.4 for more details.

Table 10. 4-Wire and 2-Wire Interface

INTERFACE	SIGNALS	LINE TERMINATION	COMMENT
2-wire	DSL–	Compliant to HIPERFACE DSL 2-wire motor integrated cable with 11 V	See Figure 6
	DSL+		
4-wire	DATA+	120 Ω differential, 330 pF to GND	Default status receive
	DATA–		
	CLOCK+	330 pF to GND	Default transmit, high
	CLOCK–		

The RS-485 interface features the SN65HVD78 half-duplex transceiver with a 3.3-V supply and IEC-ESD with key parameters listed in Table 11.

Table 11. RS-485 Transceiver Specifications

PARAMETER	VALUE
Standard	RS-485
Configuration	Half-duplex
Baud rate	50 Mbps
Receiver and driver propagation delay (max)	≤ 35-ns receive, ≤ 15-ns transmit
Receiver and driver differential rise/fall time (max)	≤ 6 ns
Bus I/O protection	>±12 kV IEC 61000-4-2 Contact Discharge >±4 kV IEC 61000-4-4 EFT

2.2.2 Protected Encoder Power Supply

The protected encoder power supply is split into two functional blocks. The DC/DC buck converter provides either a 5.25-V or 11-V output. The eFuse provides protection for OV, UV, and OC. The specifications are listed in Table 12 and Table 13.

Table 12. Encoder Power Supply Generic Specification

PARAMETER	VALUE
Input voltage, nominal (range)	24-V DC nominal, 15 to 60-V range
Output voltage (selectable through GPIO or jumper)	11-V DC or 5.25-V DC (programmable with GPIO)
Output voltage accuracy	≤ ±5%
Output voltage ripple	< 30 mV_{PP}
Output current (nominal)	250 mA
Output current (nominal/inrush) (HIPERFACE DSL)	250 mA, 3.5 A (100 µs), 1 A (400 µs)
Output voltage start-up time (0 V → 5.25 V or 11 V)	< 30 ms
Full system efficiency	>80% at nominal load
DC/DC switching frequency	500 kHz

Table 13. Protection Features of Encoder Supply Output

CHARACTERISTICS	VALUE FOR 5.25-V OUTPUT	VALUE FOR 11-V OUTPUT
Overvoltage	6 V	12 V
Undervoltage	4 V	4 V
Overcurrent (continuous)	< 300 mA (±10%)	
Short-circuit protection	Yes	
Short-circuit shutdown (output voltage off)	30 ms (eFuse)	
OC, OV, UV fault flag	Yes	
Bypass option for eFuse (if desired)	Yes	

2.2.3 3.3-V Point-of-Load

An additional onboard DC/DC converter provides a 3.3-V point-of-load with up to a 200-mA output current to supply the onboard logic and RS-485 transceivers.

2.3 Host Processor Interface

The host processor interface provides the basic encoder's serial communication signals for clock, data receive and data transmit, the data direction configuration signals, and two signals to configure the output voltage and the active encoder interface, which is either 2-wire (HIPERFACE DSL) or 4-wire (EnDat 2.2 and BiSS).

Additional I/O signals configure and diagnose to realize additional and optional features.

Table 14. Host Processor Interface

SIGNAL	3.3 V (I/O)	DEFAULT STATE	DESCRIPTION
RX_DATA	(O)	NA(1)	Data receive signal (EnDat 2.2, HIPERFACE DSL, BiSS, SSI)
TX_EN	(I)	Low (PD)	Data communication direction (EnDat 2.2, HIPERFACE DSL)
TX_DATA	(I)	Low (PD)	Data transmit signal (EnDat 2.2, HIPERFACE DSL)
CLOCK	(I)	High (PU)	Clock signal (EnDat 2.2, BiSS, SSI)
HIPERFACE	(I)	Low (PD)	Set 2-wire (HIPERFACE DSL or 2-wire (EnDat 2.2, SSI, BiSS) interface
nPWR_FAULT	(O)	High	Encoder power supply fault indication (active low)
PWR_EN	(I)	High (PU)	Encoder power supply enable
HI_V_SEL	(I)	Low (PD)	Select the voltage rail (5 V or 11 V)
LOAD_SW_CTRL	(I)	Low (PD)	Disable the load switch that connect the supply to the encoder
PS_IMON	(O) Analog 0 to 0.675 V	NA(1)	Encoder power supply output current (analog signal)

(1) Pending operation conditions

2.4 Indicator LEDs

LEDs signal the board settings to the user (see Table 24). Refer to Section 5.3 for a detailed description.

2.5 EMC Immunity

The design meets ESD, EFT, surge, and conducted RF immunity requirements per IEC61000-4-2, 4-4, 4-5, and 4-6 with levels specified in the IEC61800-3 standard "EMC immunity requirements for adjustable speed, electrical-power drive systems". It is assumed only the SubD-15 connector to the position encoder can be accessed, and shielded encoder cables connect to the encoder.

Table 15. EMC Immunity

PORT	PHENOMENON	BASIC STANDARD	LEVEL	PERFORMANCE (ACCEPTANCE) CRITERION
Encoder interface connecter	ESD	IEC61000-4-2	±4-kV DC	B
	EFT	IEC61000-4-4	±2 kV/5 kHz	B
	Surge 1.2/50 µs, 8/20 µs	IEC61000-4-5	±1 kV	A
	Conducted RF	IEC61000-4-6	0.15 to 80 MHz, 10 V/m, 80% AM (1 kHz)	A

Test results are provided in Section 6.

3 Block Diagram

The major building blocks of this TI Design, as outlined in Figure 8, are the 4-wire and the 2-wire bidirectional RS-485 interfaces along with a multiplexer/de-multiplexer to select the active encoder interface; the encoder power supply with programmable output voltage and overvoltage, overcurrent protection, and short-circuit protection; and a 3.3-V digital interface to a host processor to run the corresponding encoder standard protocol. A SubD-15 female connector with shield is made available to connect to the absolute position encoder. An additional 10-pin header is made available for further flexibility and use with custom specified encoder connectors.

The host processor to run the corresponding encoder master protocol is not part of this design.

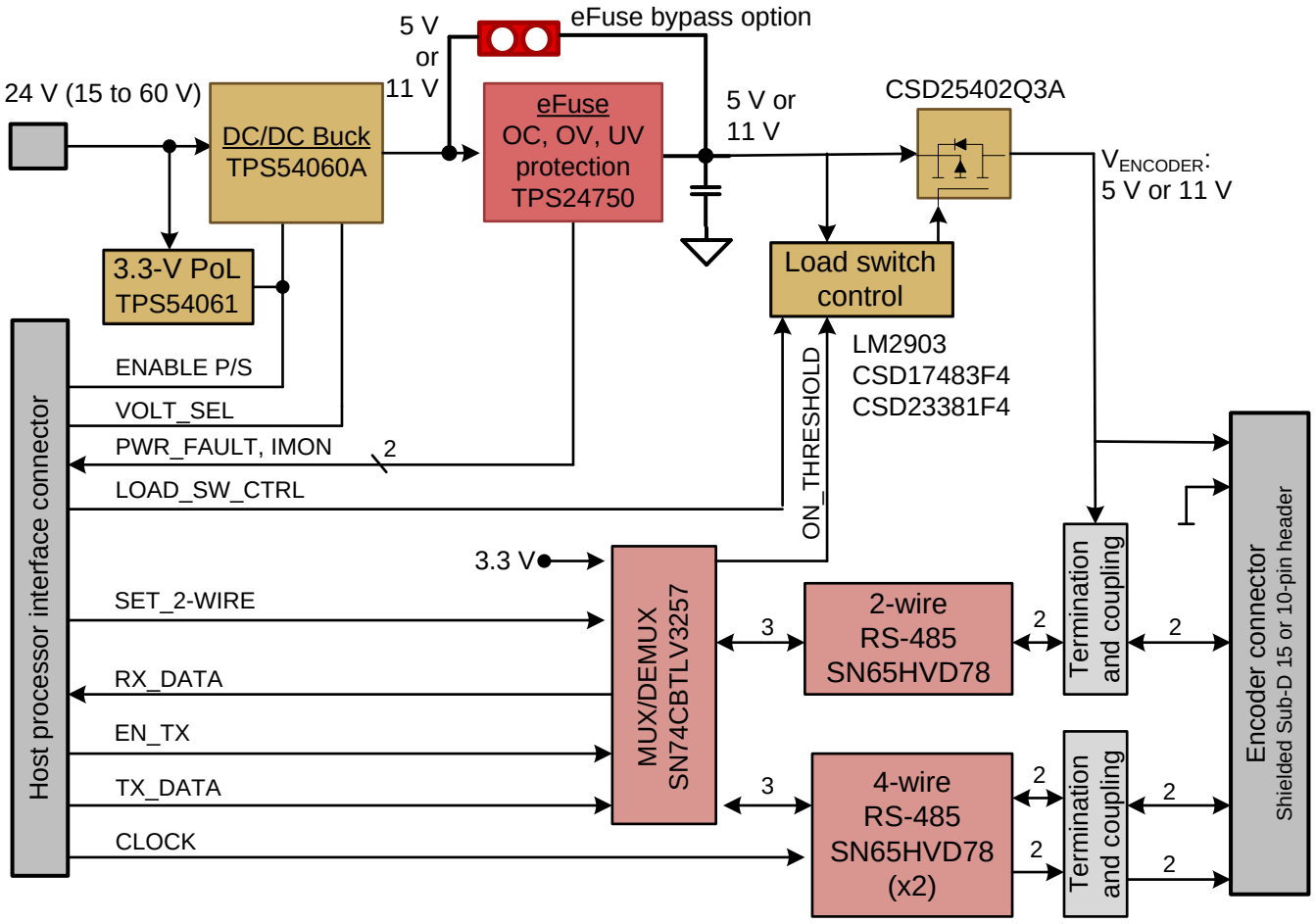


Figure 8. System Block Diagram of TIDA-00179

4 Circuit Design and Component Selection

4.1 4-Wire Interface

4.1.1 RS-485 Transceiver Circuits

When choosing the RS-485 device for EnDat 2.2, consider the relationship between baud rate and clock frequency. EnDat 2.2 is a synchronous communication with the data shifted out at the falling clock edge. Each clock period equals two bauds; the first half clock period equals a symbol as well as the second half period. Hence the baud rate should be at least twice the clock rate. Therefore, an EnDat 2.2 compliant RS-485 transceiver needs to be specified for a minimum baud rate of 32 Mbps.

When EnDat 2.2 is implemented without delay compensation at maximum clock of 2 MHz, the entire loop propagation delay (Master and Encoder) must not exceed 250 ns. Parameters with regards to RS-485 transceivers taken into consideration are listed in Table 16.

Table 16. RS-485 Parameters From Corresponding Datasheets (SLLS505, SLLSE11)

PARAMETER	SN65HVD78
Supply voltage (recommended)	3.3 V
Baud rate (maximum)	50 Mbps
Receiver propagation delay (maximum)	35 ns
Driver propagation delay (maximum)	15 ns
Receiver rise/fall time (maximum)	6 ns
Driver rise/fall time (maximum)	6 ns
Supply current (quiescent) driver and receiver enabled	0.95 mA (max)
IEC61000-4-2 ESD (absolute maximum ratings)	±12 kV (CD)
IEC61000-4-4 EFT (absolute maximum ratings)	±4 kV

With that information, the RS-485 device chosen was the SN65HVD78, with the option to verify performance versus SN65HVD10.

4.1.2 RS-485 Termination and Transient Protection

Instead of single 120-Ω/0.1-W resistors, two smaller resistors 0603 in series 0.1 W each have been chosen.

A pulse-proof resistor is added to the A and B bus lines if a transient voltage is higher than the specified maximum voltage of the transceiver bus terminals. These resistors limit the residual clamping current into the transceiver and prevent it from latching up. In data receive mode, due to the low input current of typical 240 µA, the voltage drop across the 10-Ω resistors is negligible. In the clock and data transmit direction, the voltage drop across both 10-Ω resistors is around 15%, which results in a slightly lower transmit differential voltage.

To further improve immunity against common mode noise and only for clock frequencies of up to 8 MHz, 330-pF bypass capacitors are added from each differential RS-485 outputs A and B to GND. See C28, C30, C33, and C35 in Figure 9; these caps need to be high quality caps (NP0/C0G).

The bus terminals of the SN65HVD7x transceiver family possess on-chip ESD protection against ±15-kV human body model (HBM) and ±12-kV IEC61000-4-2 contact discharge, meaning no further protection is required.

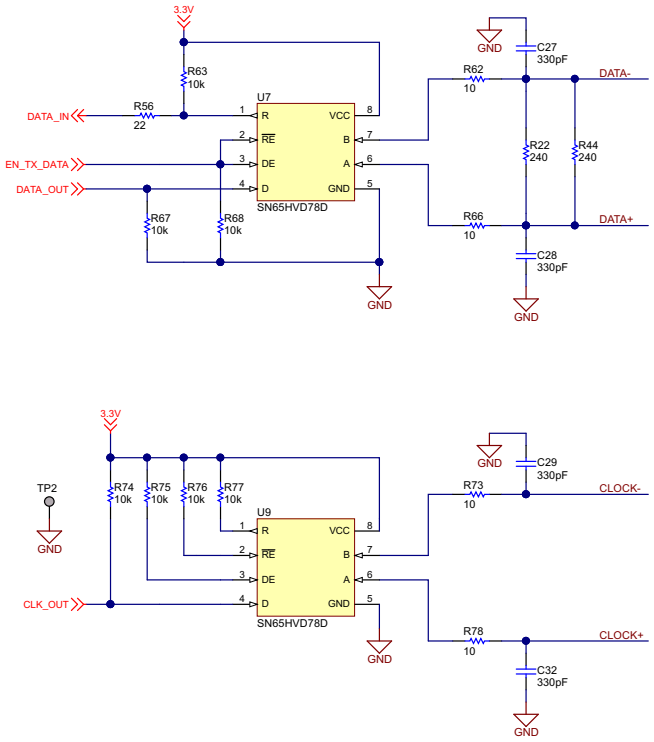


Figure 9. 4-Wire RS-485 Interface Schematic

4.2 2-Wire Interface

This section thoroughly describes the interface circuit and recommends components.

As a physical layer, HIPERFACE DSL uses a transfer in accordance with EIA-485 (RS-485). Valid RS-485 interface drivers must comply with the conditions in Table 17.

Table 17. RS-485 Driver Interface Specifications

CHARACTERISTIC	VALUE	SN65HVD78D
Transfer rate	>20 MBaud	Up to 50 MBaud
Permitted common mode voltage	–7 to 12 V	–7 to 12 V
Minimum differential input voltage detected	< 200 mV	80 mV typ
Load resistance	< 55 Ω	54 Ω
Receiver propagation delay	< 60 ns	< 35 ns
Transmitter propagation delay	< 60 ns	< 15 ns
Transmitter power-up delay	< 80 ns	< 30 ns
Transmitter power-down delay	< 80 ns	< 30 ns
Transmitter rise time	< 10 ns	< 6 ns
Transmitter fall time	< 10 ns	< 6 ns
ESD	N/A	12-kV CD
EFT	N/A	4 kV

4.2.1 RS-485 Termination and Transient Protection

To minimize voltage rails, a 3.3-V supply RS-485 transceiver with a 5-V tolerant I/O and low quiescence power has been selected. Due to the 3.3-V I/O, it can typically directly connect to a processor.

To connect through a 2-wire cable integrated in the motor cable, the data cables must be decoupled by a transformer to raise the common mode rejection ratio. To feed the supply voltage into the data cables, choke coils are also required.

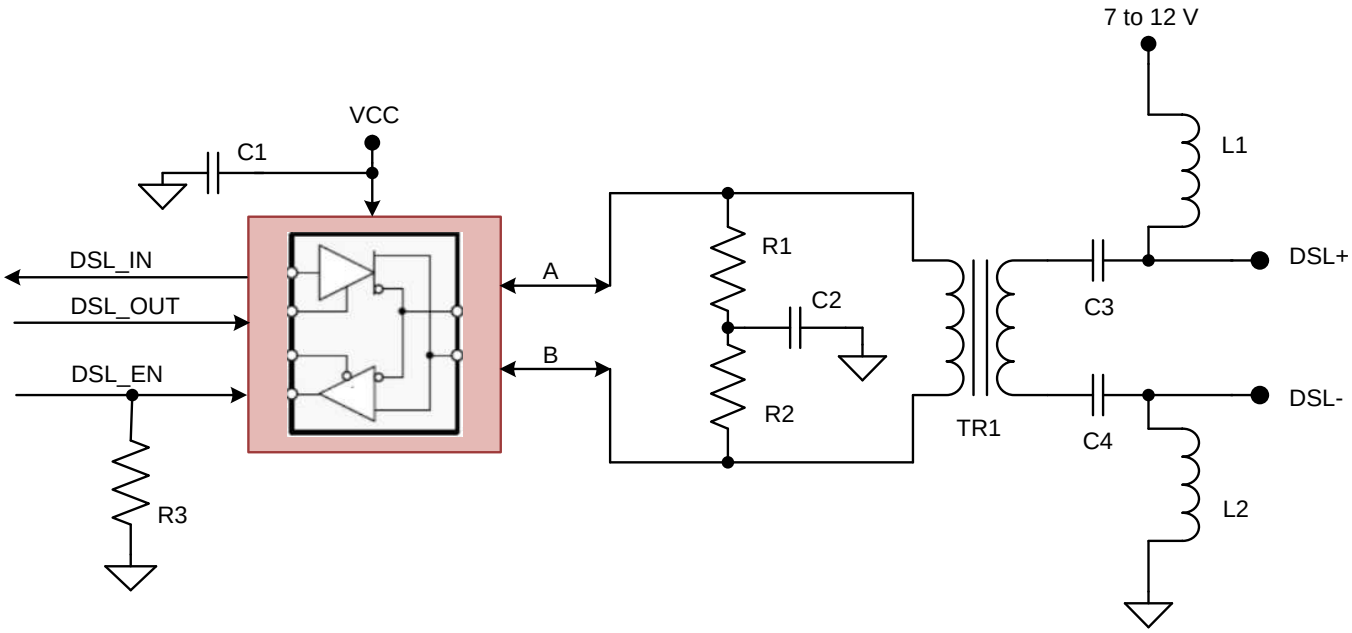


Figure 10. HIPERFACE DSL 2-Wire Interface Circuit With Integrated Motor Cable

With Figure 10, the following values are used:

Table 18. Interface Circuit With 2-Wire Cables (Integrated in Cable)

COMPONENT	DESCRIPTION	PART
C1	Ceramic capacitor	2.2 µF, 16 V
C2, C3	Ceramic capacitor	470 nF, 50 V
L1, L2	Inductors	Würth Elektronik 744043101, 100 µH or Panasonic ELL6SH101M, 100 µH
R1, R2	Resistors	56R
R3	Resistors	1k to 100k
U1	RS-485 transceiver	Texas Instruments SN65HVD78D
TR1	Transformer	Pulse Engineering PE-68386NL or Murata 78602/1C or Epcos B78304B1030A003

4.2.2 TIDA-00179 Interface Solution

To meet the previous requirement, the SN65HVD78D is selected to implement the RS-485 transceiver.

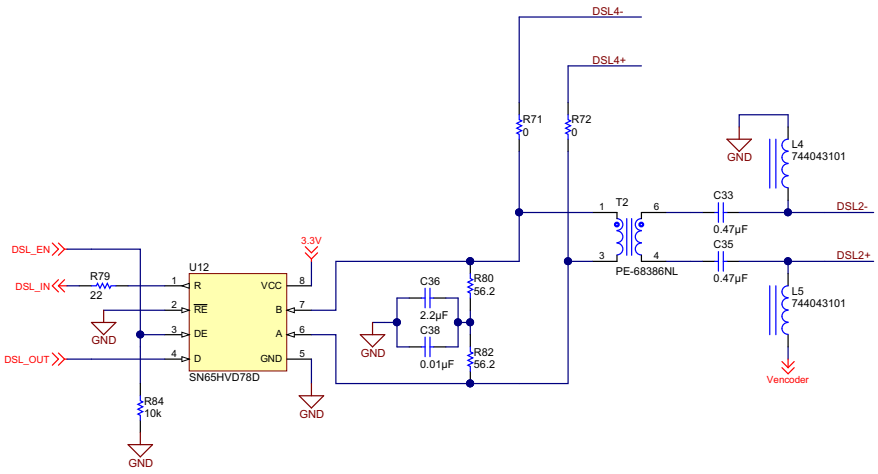


Figure 11. 2-Wire RS-485 Interface Schematic

The transceiver topology is a half-duplex with the receiver always active and the transmitter enabled from the MPU GPIO. Data are collected by the CPU across the R and D pins (RX and TX, respectively).

4.3 Host Processor Interface

To switch from one interface to the other, this design uses an analog MUX.

The analog MUX is selected instead of a pure digital one because the communication bus is bidirectional (the pure digital MUX is unidirectional).

Furthermore, to avoid any impact on the communication between the host processor (master) and the encoder, the propagation delay is a key parameter when selecting a proper MUX/DEMUX.

For a 3.3-V MUX/DEMUX with an ultra-small propagation delay, a small size or package, and limited cost, the Texas Instruments SN74CBTL3257 is chosen.

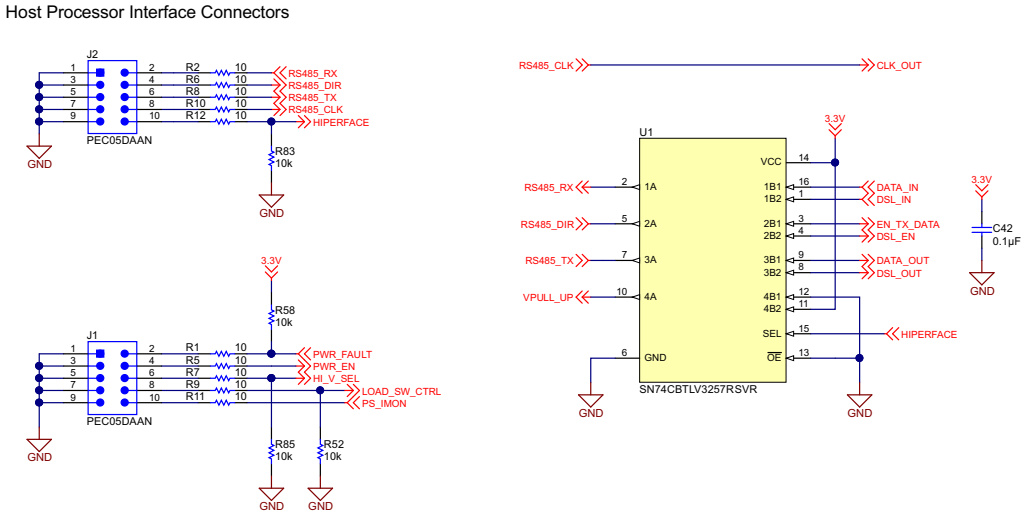


Figure 12. MUX for Protocol Selection

In addition to the MUX/DEMUX block, an ESD protection barrier is provided between the I/O connectors and the host processor since these two parts could be also connected among a long cable. This barrier specifically protects the inputs while all I/Os are provided with current pulse limiting resistors.

4.4 Protected Encoder Power Supply

With reference to the electrical specification for the various encoders (see Table 7), a voltage between 10 and 12 V is enough to cover all the possible encoder except the 5-V encoders.

For this purpose, a dual level programmable DC/DC converter is used, where the two levels are 5 V and 11 V, respectively. The current requirement is 250 mA max for all the encoders except the HIPERFACE DSL, which requires a 3.5-A inrush current at the start-up.

The encoder supply voltage also requires some safety features, like overcurrent protection (OCP), overvoltage protection (OVP), undervoltage protection (UVP), short-circuit protection (SCP), and over temperature protection (OTP). Those safety features will be handled by the eFuse.

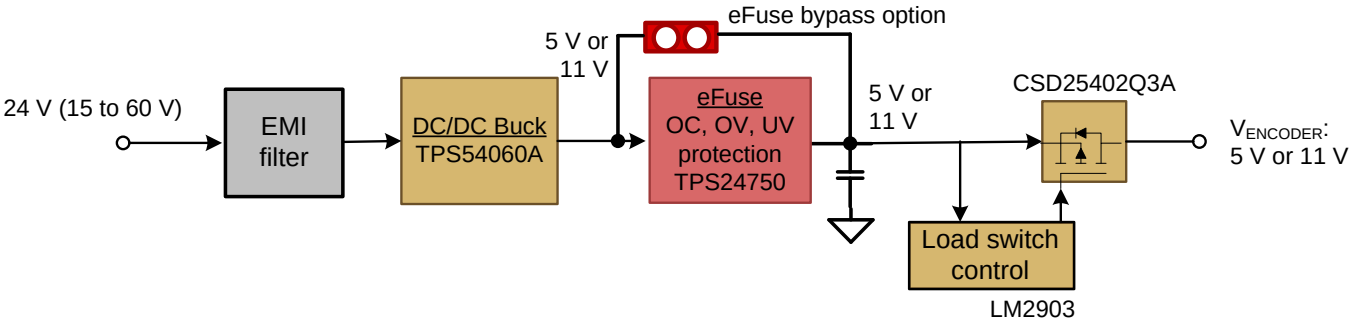


Figure 13. Protected Encoder Power Supply Block Diagram

4.4.1 Input Filter and Reverse Polarity Protection

Conducted EMI are generated by the normal operation of switching circuits. Large discontinuous currents are generated as the power switches turn on and off. In a buck topology, large discontinuous currents are present at the input. The voltage ripple created by those discontinuous currents can couple into the rest of the system and cause EMI issues. To prevent this, an input filter reduces the input voltage ripple accordingly. In this design's case, this input filter consists of a PI filter with the cutoff frequency around 1/10 of the switching frequency of the converters to have 40 dB of attenuation at the switching frequency.

Because the two switching converters used in the TIDA-00179 work at the same frequency (synchronized) of ≈ 380 KHz, the LC input filter can be calculated as

$$f_C = \frac{1}{2 \times \pi \times \sqrt{L \times C}} = \frac{F_{SW}}{10} \approx 38\ \text{KHz} \quad (1)$$

When L = 8.2 µH, then C ≈ 1.8 µF (2 × 1 µF solution is chosen for simplicity).
When L = 6.8 µH, then C ≈ 2.2 µF (2 × 1 µF solution is chosen for simplicity).

Assuming an efficiency of 60% minimum, the total input current could be calculated as

$$P_{IN} \times 0.6 = P_{OUT} \quad (2)$$

$$I_{IN} \times V_{IN} \times 0.6 = 11\ \text{V} \times 0.3\ \text{A} + 3.3\ \text{V} \times 0.2\ \text{A} \quad (3)$$

$$I_{IN} < \frac{6.6\ \text{W}}{V_{IN\_min}} \cong 370\ \text{mA} \quad (4)$$

These results mean that a coil with a saturation current of 0.5 A is more than enough for this purpose. The Würth 74438334xxx series of the Coilcraft LPS3314 series, which is almost pin-to-pin compatible, is an example of a good solution.

To achieve more attenuation, the pin-to-pin 10-µH part could be used as well.

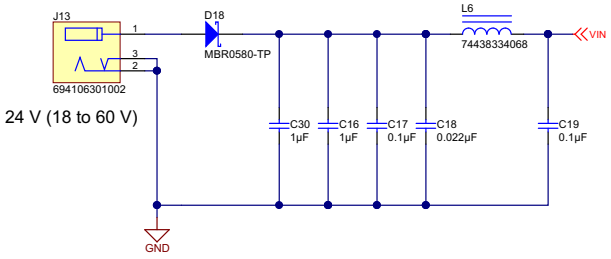


Figure 14. Input Filter Schematic

4.4.2 DC/DC Buck (TPS54060A)

The specifications for the encoder power supply are

- Input: 15 to 36 V, 24 V nominal, 60 V tolerant
- Output: 5.25 V or 11 V at 250 mA, programmable
- Switching frequency ≈ 400 kHz with synchronization capability
- Non-isolated
- Output voltage ripple: 30 mV max
- With Enable pin

Many TI parts meet the previous specifications, but the TPS54060A is pin-to-pin compatible with many other parts from the TPS54xxx product family.

This compatibility gives to the customers the ability to easily replace the TPS54060A with either a cheaper part or a more or less powerful one (based on the specific output current requirements).

For example, when the 60-V input rating is not a must, then the cheaper TPS5401 (42 V rated) could be used in place of the TPS54060A.

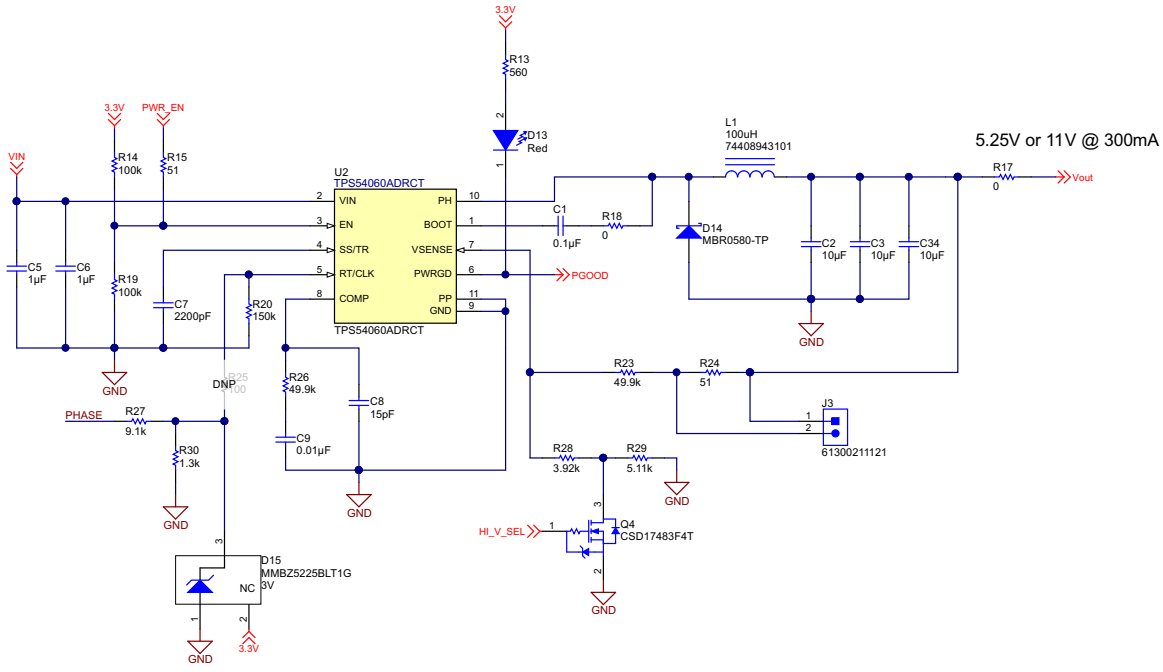


Figure 15. Protected Encoder Power Supply Schematic Based on TPS54060A DC/DC Converter

The converter is enabled when the 3.3-V rail is settled (>2.5 V typically, 2.7 V worst case) or by using an externally driven GPIO that could drive at least a 1.5-V logic level.

Because this converter starts up after the 3.3-V rail, the master clock for the frequency synchronization comes from the 3.3-V PoL, and in particular from the switching node through a voltage divider plus a clamping diode barrier to avoid potential damages to the RT/CLK pin.

Inductor current peak-to-peak ripple is calculated as 233 mA, meaning that the RMS current into the inductor is basically identical to the output DC current level.

$$\Delta I_L = V_{OUT} \times \frac{V_{IN\_max} - V_{OUT}}{V_{IN\_max} \times L \times F_{SW}} \quad (5)$$

The expected output voltage ripple is below 20 mV_{PP}. For the purpose, two ceramic caps are used in parallel to reduce the ESL effects on the ripple. A third one could be added to further reduce the output voltage ripple, according to Equation 6:

$$V_{OUT\_ripple} = \frac{\Delta I_L}{8 \times F_{SW} \times C_{OUT}} \quad (6)$$

Because this converter has to provide two different voltages, a shunt is provided on the feedback divider and could be driven by another GPIO. For lower ripple demand, a third cap could be added (not populated in original design).

This solution is preferred because changing the resistor of the divider to ground (R28+R29 in the schematic) does not affect the system stability.

Catch diode is selected to be at least I_{Lpeak} rated (≈ 0.4 A) in terms of current and V_{IN_max} rated in terms of voltage. So, the MBR0580-TP (80 V, 0.5 A, 0.4 W) has been selected for the purpose.

The power loss on the catch diode can be estimated by using Equation 7:

$$P_D = \frac{V_{IN\_max} - V_{OUT}}{V_{IN\_max}} \times I_{OUT} \times V_F + \frac{\left(V_{IN\_max} - V_F\right)^2}{2} \times C_J \times F_{SW} \quad (7)$$

Where C_J is the junction capacitance of the diode and V_F is its forward voltage.

Since the TPS54060A is supposed to work up to 300 mA (anything greater will be limited by the eFuse), the maximum power dissipation of the selected diode will be lower than 250 mW.

Regarding the device's datasheet and that the ESR of each ceramic used on the power stage is 3 mΩ, the components of the compensation network are calculated as shown in Table 19:

Table 19. Compensation Network Components

PARAMETER	CALCULATED VALUE (FOR V_{OUT} = 5.25 V)	CALCULATED VALUE (FOR V_{OUT} = 11 V)
F_{Pmod}	460 Hz	220 Hz
F_{Zmod}	5.31 MHz	5.31 MHz
F_{co}	9.35 KHz	6.47 KHz
R4	41.4 KΩ	59.5 KΩ
C7	8.36 nF	12.2 nF
C8	16 pF	16 pF

At this point, the middle value is considered, so R4 = 49.9 KΩ, C7 = 10 nF, and C8 = 15 pF.

4.4.3 eFuse Protection

The specifications for the eFuse are:

- Current limit during inrush: 300 mA
- Power limit: not needed
- OVP: 12 V or 6 V, depending on encoder voltage selected
- Undervoltage lockout (UVLO): 4 V
- Latching when a fault is detected
- Fault feedback (active low)
- Analog output current monitor (IMON)

The smallest and most complete eFuse that performs and meets all the previous specifications is the TPS24750, whose BOM has been designed according to Figure 16:

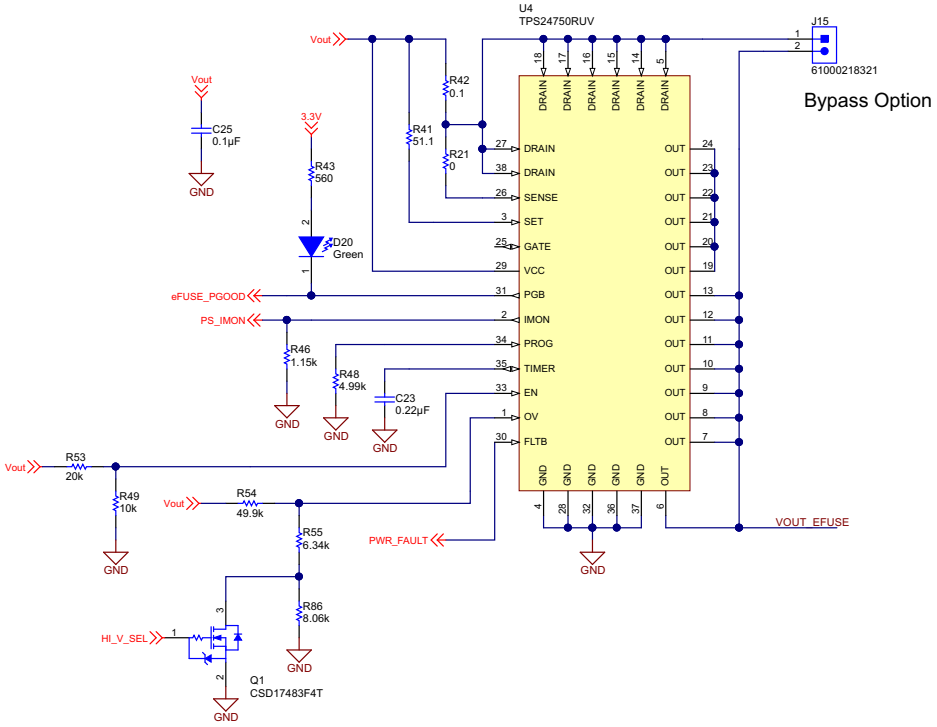


Figure 16. eFuse Protection Based on TPS24750

As in the TIDA-00177, the large bulk capacitor C22 (470 µF) placed at the output of the eFuse needs to be charged without triggering a false OCP. With the eFuse current limit of 300 mA, the time to charge the C22 to 11 V takes around 470 µF × 11 V / 0.3 A ~ 17.5 ms, so the timer capacitor C_{TIMER} is set to latch the OCP after around 30 ms, according to Equation 8:

$$t_{FAULT} = \frac{10\ \mu A}{1.35\ V \times C_{TIMER}} \quad (8)$$

The power limit feature is not necessary, so 4.99 KΩ is chosen to connect the PROG pin to GND. For the current limit settings,

$$I_{LIM} = \frac{675\ mV \times R_{SET}}{R_{IMON} \times R_{SENSE}} \quad (9)$$

where

- R_{SENSE} = 100 mΩ 1%
- R_{SET} = 51 Ω 1%
- R_{IMON} = 1.15 K 1%

These values lead to I_{LIM} = 300 mA.

OVP and UVP are set through a proper divider on the OV and EN pin, respectively. According to the device datasheet, UVP is triggered when EN pin voltage drops below 1.3 V; OVP is triggered when OV pin voltage crosses over 1.35 V.

By specification of TIDA-00179 the UV and OV levels change dynamically according to the output voltage selected (5.25 V or 11 V). Normally, a ±20% window is used, so the levels are 6 V and 12 V, respectively, while the UV is set the same for both rails at 4 V nominal.

This leads to the equations:

- R55 = 0.290 × R54 for the 6-V OVP
- R55 = 0.127 × R54 for the 12-V OVP
- R53 = 2 × R49 for the 4-V UVP

R54 is then chosen equal to 49.9 KΩ, so that

- R55 = 14.5 KΩ when the 5-V rail is selected
- R55 = 6.3 KΩ when the 10-V rails is selected

for which the commercial values of 8.06 KΩ and 6.34 KΩ at 1% are selected.

For UVP, the values are:

- R49 = 10 KΩ and R53 = 20 KΩ, for which the commercial at 5% are selected (no need for better accuracy here).
- When V_{IN} < 3.90 V, the UVP is triggered.
- When V_{IN} > 6.03 V, the OVP is triggered (if the 5.25-V output voltage is selected or enabled)
- When V_{IN} > 11.98 V, the OVP is triggered (if the 11-V output voltage is selected or enabled)

These conditions basically match the desired values.

4.4.4 Load Switch Control

Besides the eFuse protection level, to achieve the current inrush at the start-up demanded by the HIPERFACE DSL encoders, a load switch control scheme similar to the one used in TIDA-00177 has been implemented and improved here.

In particular, as a universal encoder interface, the load switch should work as in TIDA-00177 when a HIPERFACE encoder is used, and bypassed (always active) otherwise.

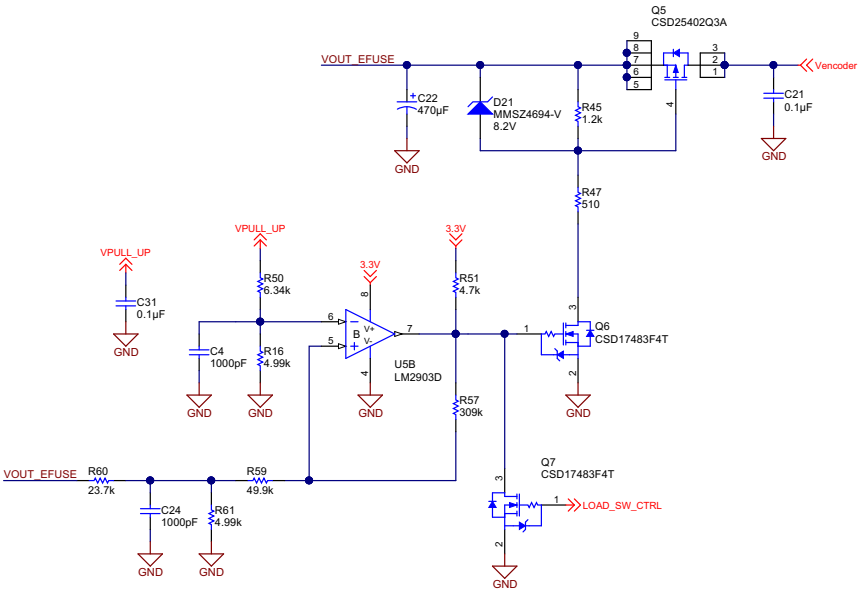


Figure 17. Load Switch Control Circuit

The comparator with hysteresis based on the LM2903D is the same as for TIDA-00177, where two extra controls have been added:

- LOAD_SW_CTRL signal bypass completely the comparator, and can ONLY disable the load switch
- HIPERFACE signal enable the hysteresis control (when high), while when low automatically enables the load switch as soon as the 3.3-V rail is settled

With this combination, the following features are achieved:

- Protection (through host CPU) is always possible to open the load switch in any condition as soon as LOAD_SW_CTRL is driven high.
- Automatic start-up occurs when HIPERFACE is disabled (low). Then the load switch is always on, meaning there is no current inrush at the start-up for the non HIPERFACE encoders.
- When HIPERFACE is high, then the load switch is controlled like TIDA-00177, with thresholds at 10 V (rising) and 7 V (falling).

To reduce the spreads from board to board due to components tolerances, a precise voltage reference like the TLV431 could be used in place of R16; this will strongly mitigate the dependency on the DC level of the 3.3-V rail. Furthermore, the ATL431 requires only a 10-µA current to guarantee a well-regulated reference.

Because the LM2903 is an open-drain output op-amp, the calculation is a bit more complex than usual.

A reference for the comparator is set to 1.453 V through Equation 10:

$$3.3\ V \times \frac{R16}{R50 + R16} = 1.453\ V \quad (10)$$

While the two thresholds for are set by Equation 11:

$$V_{OUT\_eFuse} \times K_1 \times K_2 = 1.453\ V \quad (11)$$

In which

- $K_1 = \frac{R61}{R60 + R61} = 0.174$
- $K_2 = \frac{R57}{R57 + R59} = 0.861$

This results in $V_{OUT\_eFuse} \approx 9.70$ V (the rising threshold), and

$$V_{OUT\_eFuse} \times K_1 + \left(3.3\ V - V_{OUT\_eFuse} \times K_1\right) \times K_3 = 1.453\ V \quad (12)$$

In which

- $K_3 = \frac{R59}{R51 + R57 + R59} = 0.137$

This results in $V_{OUT\_eFuse} \approx 6.67$ V (the falling threshold).

R57 + R59 >> R60 + R61

Note that because the falling threshold is less important than the rising threshold, the R51 (which only affects the falling threshold of the comparator) could be chosen as a cheaper 5% resistor, compared to the other resistors that should be at least 1% accurate.

Also note that both the thresholds could be shifted up or down just acting on the R16 / R50 divider.

4.5 3.3-V PoL

The voltage rail for the RS-485 is 3.3 V, coming from the 24-V bus. As this power supply does not need to be isolated, a buck (step-down) topology is optimal. The specifications for this power supply are:

- Input: 15 to 36 V, 24 V nominal, 60 V tolerant
- Output: 3.3 V at 200 mA
- Target switching frequency: ~400kHz
- Non-isolated
- Low ripple at light load

The TPS54061 has been chosen because the catch diode is embedded into the converter:

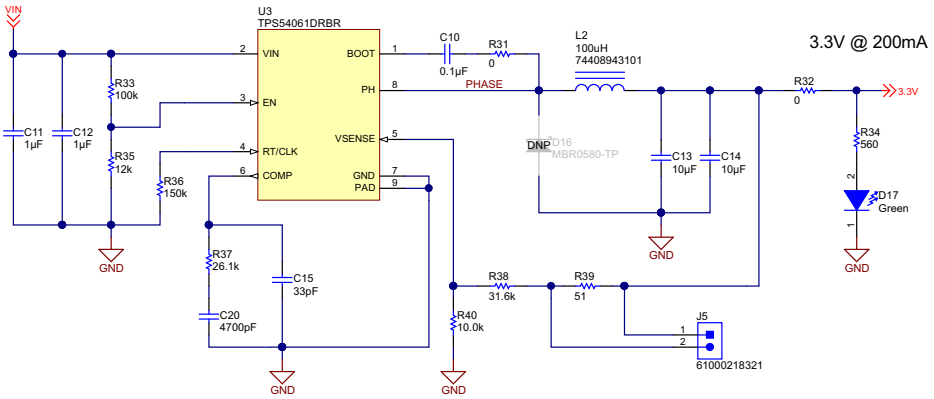


Figure 18. 3.3-V Logic Power Supply Schematic Based on TPS54061

The TPS54061EVM-142 was used as a reference for the PoL design because the specifications are identical to this design. See the device's datasheet (SLVSBB7) and EVM user's guide (SLVU721) for details.

The minimum input voltage to enable the 3.3-V PoL is set by Equation 13:

$$V_{EN} = V_{IN} \times \frac{R35}{R35 + R33} = 1.23\ V \tag{13}$$

meaning that the converter starts up when V_{IN} crosses over 11.5 V (13.1 V worst case). The output voltage is programmed by the divider R38 / R40 in according to Equation 14:

$$V_{REF} = V_{OUT} \times \frac{R40}{R38 + R40} = 0.8\ V \tag{14}$$

Note that this controller does not need a catch diode. The D16 in the schematic is minded in case of future upgrades, because the TPS54061 is, like the TPS54060A, pin-to-pin compatible with many other members of the TPS54xxx family.

5 Getting Started

5.1 PBC Overview

Figure 19 and Figure 20 show the top and bottom of the PCB, respectively. To minimize the PCB size, components are mounted on the top and bottom layer. All jumpers and connectors to external components are mounted on the top layer.

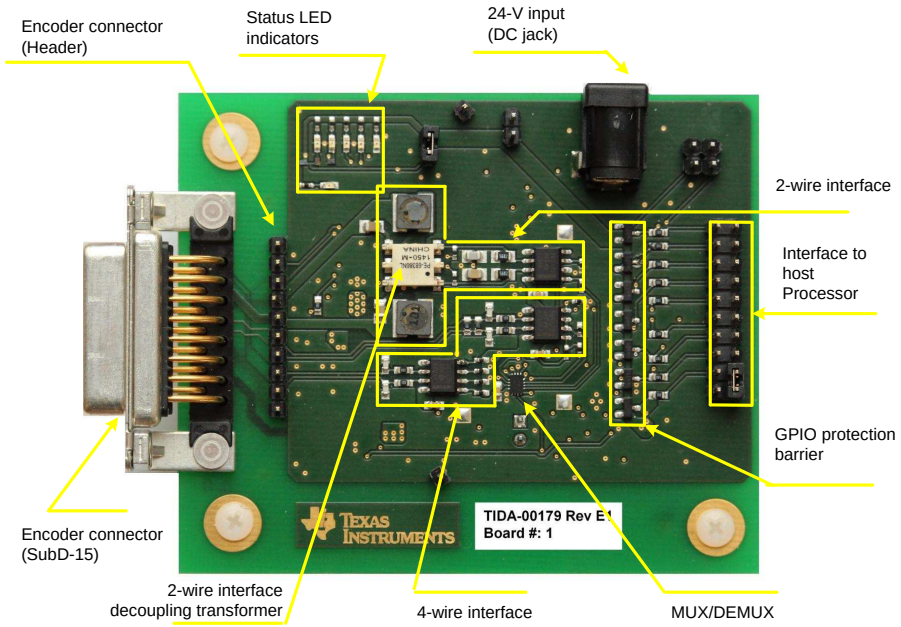


Figure 19. TIDA-00179 PCB Top View With Functional Blocks

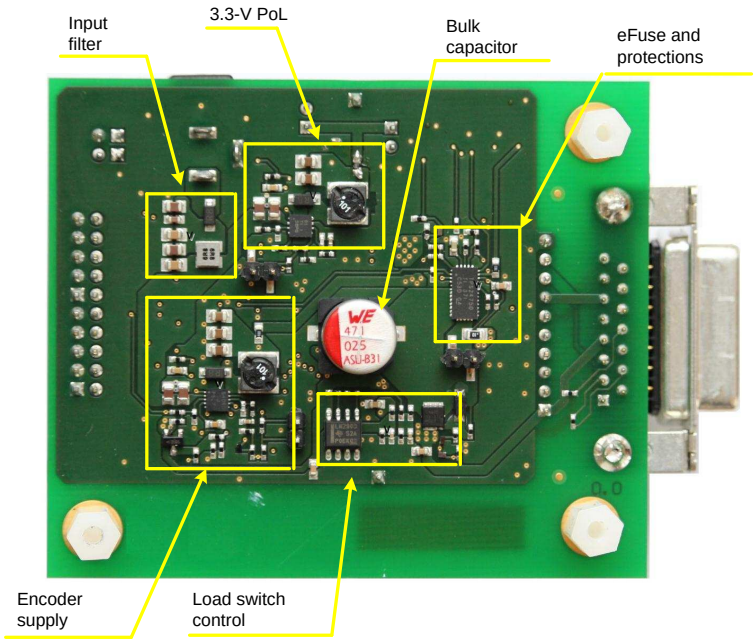


Figure 20. TIDA-00179 PCB Bottom View With Functional Blocks

5.2 Connectors and Jumper Settings

The connector assignments and jumper settings are outlined in Table 20 to Table 22.

Table 20. Host Interface Connectors

CONNECTOR	PIN	SIGNAL	PIN	SIGNAL	DESCRIPTION
J1	1	GND	2	RS485_RX (O)	Data receive signal
	3	GND	4	RS485_DIR (I)	Data communication direction (half-duplex)
	5	GND	6	RS485_TX (I)	Data transmit signal
	7	GND	8	RS485_CLK (I)	Clock signal (EnDat 2.2 and BiSS only)
	9	GND	10	HIPERFACE (I)	Enable HIPERFACE DSL 2-Wire Interface
J2	1	GND	2	nPWR_FAULT (O)	Encoder power supply fault indication (active LOW)
	3	GND	4	PWR_EN (I)	Encoder power supply enable
	5	GND	6	HI_V_SEL (I)	Select the voltage rail (5 V or 11 V)
	7	GND	8	LOAD_SW_CTRL (I)	Disable the load switch that connect the supply to the encoder
	9	GND	10	PS_IMON (O)	Encoder power supply output current (analog signal)

Table 21. Encoder SubD-15 Connector

CONNECTOR	PIN	NAME	DESCRIPTION
J6	1	DSL4–	DSL– with 4-wire HIPERFACE DSL
	2	GND	Encoder supply return
	3	DSL4+	DSL+ with 4-wire HIPERFACE DSL
	4	VENCODER	Encoder supply voltage
	5	DATA+	DATA+ (EnDat 2.2) or SL+ (BiSS)
	6	DSL2+	DSL+ with 2-wire HIPERFACE DSL interface (power over RS-485)
	7	DSL2–	DSL– with 2-wire HIPERFACE DSL interface (power over RS-485)
	8	CLOCK+	CLOCK+ (EnDat 2.2) or MA+ (BiSS)
	9	—	—
	10	Sensor Un* (0 V)	Remote sense supply voltage return
	11	—	—
	12	Sensor Up*	Remote sense supply voltage
	13	DATA–	DATA– (EnDat 2.2) or SL+ (BiSS)
	14	—	—
	15	CLOCK–	CLOCK– (EnDat 2.2) or MA+ (BiSS)

Table 22. Encoder 10-Pin Header Connector

CONNECTOR	PIN	NAME	DESCRIPTION
J7	1	VENCODER	Encoder supply voltage
	2	CLOCK–	CLOCK– (EnDat 2.2) or MA+ (BiSS)
	3	CLOCK+	CLOCK+ (EnDat 2.2) or MA+ (BiSS)
	4	DATA–	DATA– (EnDat 2.2) or SL+ (BiSS)
	5	DATA+	DATA+ (EnDat 2.2) or SL+ (BiSS)
	6	DSL2–	DSL– with 2-wire HIPERFACE DSL interface (power over RS-485)
	7	DSL2+	DSL+ with 2-wire HIPERFACE DSL interface (power over RS-485)
	8	DSL4–	DSL– with 4-wire HIPERFACE DSL
	9	DSL4+	DSL+ with 4-wire HIPERFACE DSL
	10	GND	Encoder supply return

The Encoder SubD-15 connector is compatible with the HEIDENHAIN SubD-15 (female) to M12 (male) adapter cable. The TIDA-00179 PCB default configuration is Up* and Un*, which are connected to Up and Un, respectively. If not desired, remove the 0-Ω resistors (R35 and R41) close to the SubD-15 connector on the bottom PCB.

Table 23. Jumper Settings

JUMPER	DESCRIPTION AND FUNCTION	SETTINGS
J8	Pulls down the PWR_EN signal Enable or disable the encoder supply voltage	Insert to keep the encoder PS disabled Leave open for normal operation (default)
J9	Pulls up the HI_V_SEL signal Select encoder supply voltage 5.25 or 11 V	Leave open to set $V_{ENCODER}$ = 5.25 V Insert to set $V_{ENCODER}$ = 11 V (default)
J10	Pulls up the HIPERFACE signal Select 2-wire or 4-wire interface	Leave open to select an EnDat 2.2 or BiSS encoder Insert to select a HIPERFACE DSL encoder
J11	Pulls up the LOAD_SW_CTRL signal Load switch control	Leave open for normal operation (default) Insert to disable the load switch
J3	Encoder power supply loop response test point	Insert to shunt the 50-Ω termination Leave open for normal operation (default)
J15	eFuse bypass option	Insert to bypass the eFuse Leave open for normal operation (default)
J5	3.3-V PoL power supply loop response test point	Insert to shunt the 50-Ω termination Leave open for normal operation (default)

5.3 LED Functionality Description

LEDs signal the board settings to the user (see Table 24).

Table 24. LED Status Indicator

DESIGNATOR AND LED COLOR	FUNCTIONALITY DESCRIPTION
D17, Green	3.3-V rail active or running: ON when the 3.3-V rail is activated (V_{IN} > 12 V)
D13, Red	Power good for the 5.25 to 11 V: ON when the encoder supply voltage is out of regulation
D20, Green	eFuse power good: ON when eFuse output to input voltage is below 200 mV, indicating the eFuse is working properly
D1, Green	11-V encoder supply enabled: ON when the output voltage is set to 11 V: applies to all encoders but the 5-V BiSS
D2, Yellow	5-V encoder supply enabled: ON when the output voltage is set to 5.25 V: applies only to the 5-V BiSS encoder
D19, Blue	HIPERFACE DSL enabled: ON when the HIPERFACE DSL PHY is selected

Table 25. LED Indicators for Enabled Protocol or Interface

D1	D2	D19	DESCRIPTION
OFF	OFF	OFF	System OFF or 3.3-V rail is not available
OFF	OFF	ON	Not expected—System error (software or hardware problem)
OFF	ON	OFF	5.25-V encoder supply selected
OFF	ON	ON	Not expected—System error (software or hardware problem)
ON	OFF	OFF	11-V encoder supply selected, EnDat or BiSS mode enabled
ON	OFF	ON	11-V encoder supply selected, HIPERFACE DSL mode enabled
ON	ON	OFF	Not expected—System error (software or hardware problem)
ON	ON	ON	Not expected—System error (software or hardware problem)

6 Test Results

Various tests have been conducted for the individual subsystems like the RS-485 communication interface and power supply, as well as an application tests with the various encoders. Test results are illustrated in the following sections. Test results are illustrated in the following sections.

NOTE: Whenever not differently stated, all the tests are assumed to be performed at a 24-V input and 25°C ambient temperature.

6.1 RS-485 Transceiver Performance

6.1.1 Test Setup

Figure 21 shows the setup of the RS-485 transceiver performance test and the test equipment used.

Figure 21. Picture of Test Setup for TIDA-00179 RS-485 Performance Tests

This test used the following equipment:

Table 26. Test Equipment for TIDA-00179

TEST EQUIPMENT	PART NUMBER
Programmable dual-channel signal generator with 16-bit resolution	Keysight (Agilent) 33600A
Low-speed oscilloscope (suitable for power management tests)	Tektronix TDS2024B
High-speed oscilloscope (suitable for analog signal tests)	Tektronix TDS784C
Adjustable SMPS	Knuerr-Heinzinger Polaris 125-5
24-V, 2.5-A SMPS (power brick)	V-infinity 3A-621DN24
True RMS multimeter	Fluke 179
Differential probes	Tektronix P6630
Single ended probes	Tektronix P6139A
Programmable electronic load module	Chroma 63103
Control module for electronic load module	Chroma 6314
Thermal camera	Fluke TI40
Control system loop analyzer	V_{ENABLE} 3120
HEIDENHAIN shielded cables, PUR (4 × 0.14 mm^2, 4 × 0.34 mm^2), 10 m, 20 m, 20 m, 50 m	368330-xx, xx = cable length
HEIDENHAIN M12/Sub-D15 male adapter cable (1 m)	524599-1
EnDat 2.2 encoders	ROQ 437, ROC 425, ROQ 1035
HIPERFACE DSL encoder	EKM36-0KF0A018A
HIPERFACE DSL integrated motor cable, 20 m, 50 m, 80 m, 100 m	TOPSERV Hybrid PUR 708545 LI9YC11Y 4G2, 5 +(2×1.0)C+(2x22AWG)C
HIPERFACE DSL Programming Tool and Analyzer PGT-09-S	PGT-09-S

6.1.2 RS-485 Clock Frequencies versus Cable Length

Figure 22 shows the maximum clock frequency versus cable length for all the interfaces covered by the TIDA-00179. The design's performance equals the synchronous data rate in half-duplex mode without any bit errors as specified previously. Data was shifted out on the master side on the falling clock edge.

On the master side, a dual-output signal generator provides both clock and data signals, internally synchronized by the instrument itself. The clock frequency is increased until the slave device starts to loose clock edges.

The data line is fed with a random data pattern.

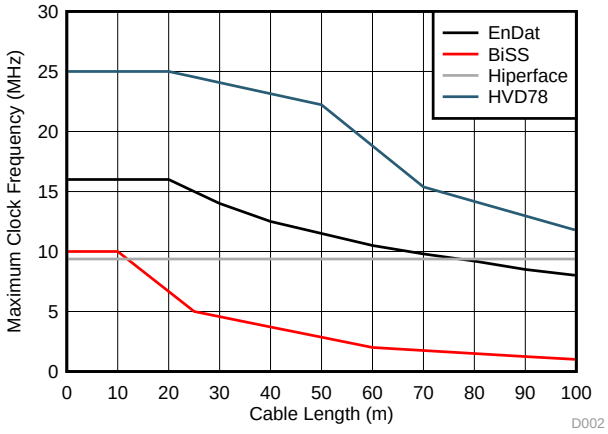


Figure 22. Maximum Clock Frequency Specifications versus TIDA-00179 Performances

Observe how the TIDA-00179 performances are far beyond the actual needs and specifications, even at the maximum cable length (100 m).

6.1.3 RS-485 Eye Diagrams versus Cable Length

Figure 23 to Figure 26 show the eye diagrams using random NRZ data measured differentially with 110-Ω or 120-Ω termination (depending on the interface that is tested) at the cable end (slave receive side) with a differential probe. The master transmitter clock rate was connected to channel 1 of the scope to trigger sampling of the differential data at the far cable end. The master clock was measured single ended at the input of the master RS-485 clock transmitter and is shown as reference on the scope plots too.

Only the worst case scenario was tested here: this means that, being the BISS a subset of the ENDAT 2.2 interface, only the ENDAT 2.2 results are shown. For more details on the eye diagram test results, see the design guides for the TIDA-00172 [11], TIDA-00175 [12], and TIDA-00177 [13] for ENDAT 2.2, BiSS, and HIPERFACE DSL interface, respectively.

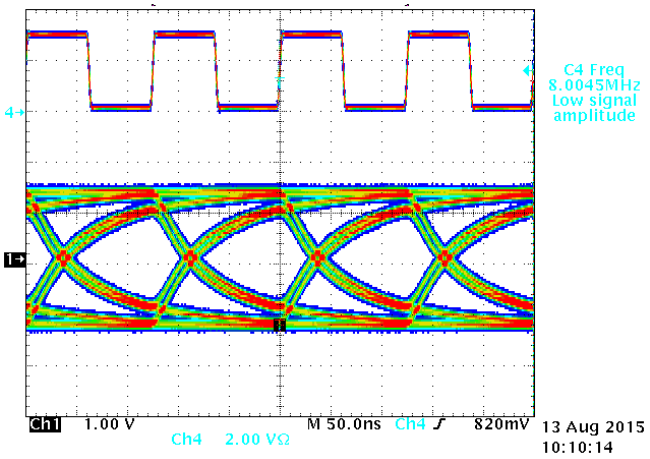


Figure 23. Eye Diagram for 4-Wire Interface, 100-m Cable, 8-MHz Data Rate

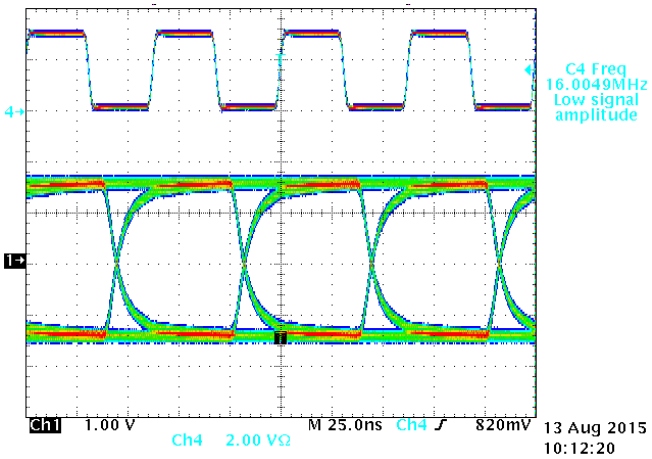


Figure 24. Eye Diagram for 4-Wire Interface, 20-m Cable, 16-MHz Data Rate

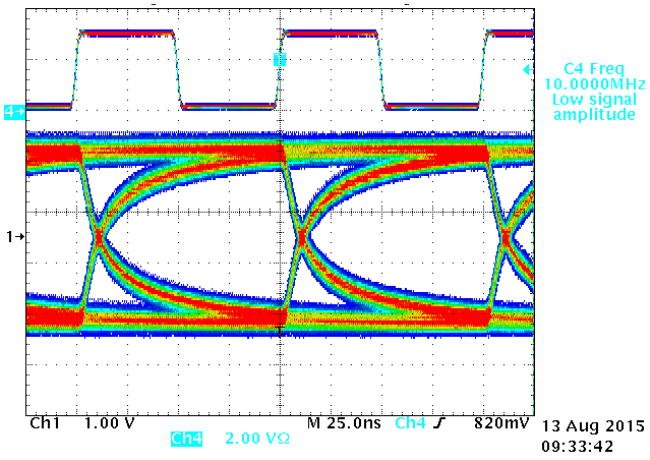


Figure 25. Eye Diagram for 4-Wire HIPERFACE DSL Interface, 100-m Cable, 9.375-MHz Data Rate

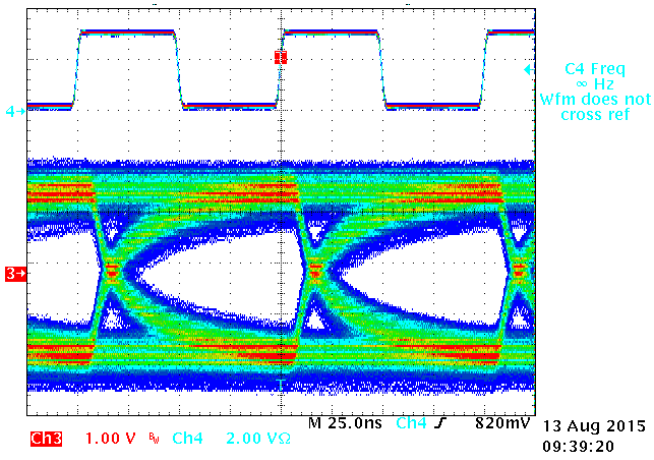


Figure 26. Eye Diagram for 2-Wire HIPERFACE DSL Interface, 100-m Cable, 9.375-MHz Data Rate

6.1.4 Current Consumption for RS-485 Transceivers

The worst case scenario has been analyzed to estimate the supply current on the 3.3-V rail consumed by the RS-485 transceivers.

In particular, the test consists of transmitting over a 0-m cable terminated on a 110-Ω or 120-Ω resistor (depending on the selected protocol) a random data stream for any encoder type at the highest possible frequency allowed for the selected protocol.

Also note that except for the HIPERFACE DSL protocol interface, both DATA and CLOCK lines have to be terminated.

Current over the resistor R32 is then measured. Results are shown in Table 27:

Table 27. Interface Power Consumption versus Protocol at 25°C

SELECTED RS-485 PHYs	CLOCK FREQUENCY	CONDITIONS	STATIC (INACTIVE DATA TRANSFER) CONSUMPTION(1)	DYNAMIC (ACTIVE DATA TRANSFER) CONSUMPTION(2)
4-wire interface	10 MHz	0-m cable, 120-Ω termination	55.6 mA	78.2 mA
4-wire interface	16 MHz	0-m cable, 120-Ω termination	55.6 mA	91.3 mA
2-wire interface	9.375 MHz	0-m cable, 110-Ω termination	112 mA(3)	50.8 mA

(1) Indicates the consumption when no communication occurs, but the lines are still terminated and active (CLOCK = HI, EN_TX = HI, TX_DATA = LO)

(2) Indicates the consumption when the communication occurs, with the lines terminated and active (CLOCK = Toggling, EN_TX = HI, TX_DATA = Random Pattern)

(3) The higher static consumption in the 2-wire is due to the fact that the decoupling transformer acts like a short circuit in DC.

6.2 Protected Encoder Power Supply Performance

6.2.1 Output Voltage Ripple

The voltage ripple is well below the EnDat 2.2 specification, even for the output voltage at full load. The results as shown in Table 28 and Table 29 are less than 20 mV_{PP} at 200 mA.

Table 28. 5-V Rail Voltage Ripple

INPUT VOLTAGE	OUTPUT CURRENT	OUTPUT VOLTAGE RIPPLE
15 V	0 mA	< 10 mV_{PP}
24 V	0 mA	< 10 mV_{PP}
36 V	0 mA	≈ 10 mV_{PP}
48 V	0 mA	≈ 10 mV_{PP}
60 V	0 mA	≈ 10 mV_{PP}
15 V	300 mA	≈ 10 mV_{PP}
24 V	300 mA	≈ 10 mV_{PP}
36 V	300 mA	< 20 mV_{PP}
48 V	300 mA	≈ 20 mV_{PP}
60 V	300 mA	≈ 30 mV_{PP}

Table 29. 11-V Rail Voltage Ripple

INPUT VOLTAGE	OUTPUT CURRENT	OUTPUT VOLTAGE RIPPLE
15 V	0 mA	< 10 mV_{PP}
24 V	0 mA	< 10 mV_{PP}
36 V	0 mA	< 10 mV_{PP}
48 V	0 mA	≈ 10 mV_{PP}
60 V	0 mA	< 20 mV_{PP}
15 V	300 mA	≈ 10 mV_{PP}
24 V	300 mA	≈ 10 mV_{PP}
36 V	300 mA	< 20 mV_{PP}
48 V	300 mA	< 20 mV_{PP}
60 V	300 mA	< 20 mV_{PP}

Note that better voltage ripple performances are achieved with the synchronization feature disabled. This because the high V_{IN} / V_{OUT} ratio for the master sync generator (3.3-V PoL) goes in deep skip mode (even at full load), causing the encoder output voltage ripple to increase above 100 mV_{PP} when the input voltage is above 36 to 48-V DC.

6.2.2 Load and Line Regulation

Performances for the load and line regulation exceeded expectations (measured in Figure 27 and Figure 28).

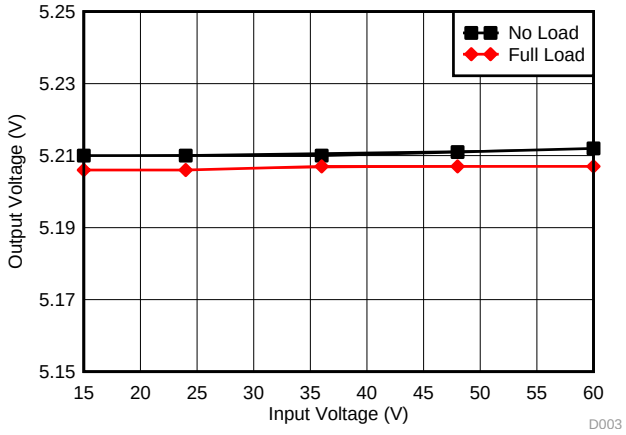


Figure 27. 5-V Encoders

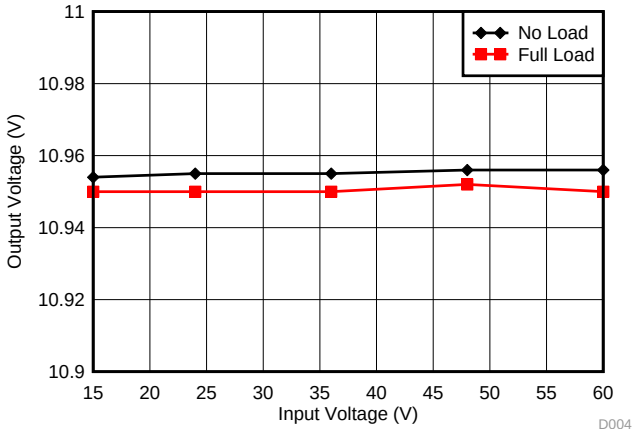


Figure 28. 11-V Encoders

6.2.3 Efficiency

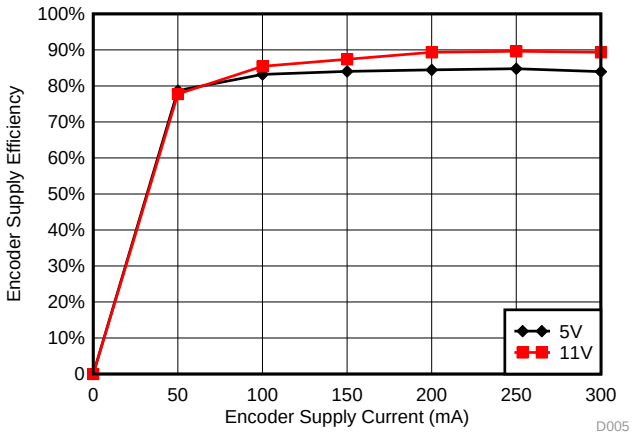


Figure 29. Encoder Supply Efficiency

6.2.4 Thermal Image

Many thermal pictures are done at room temperature (25°C) when the maximum load possible for both the outputs, changing the input voltage to catch the worst case working condition.

Three different points have been identified:

1. At minimum input voltage (15 V), the input current is at maximum, so the thermal stress occurs on the reverse polarity protection diode, which peaks around 65°C (see Figure 30)
2. At nominal input voltage (24 V), the hot spots are still the reverse polarity protection diode plus the catch diode of the TPS54060 that generates the encoder voltage supply. Here, the peak temperature detected is around 50°C (see Figure 31)
3. At maximum input voltage (60 V), the input current is also the minimum so all the stress is detected on the catch diode of the TPS54060 (66°C measured) (see Figure 32)

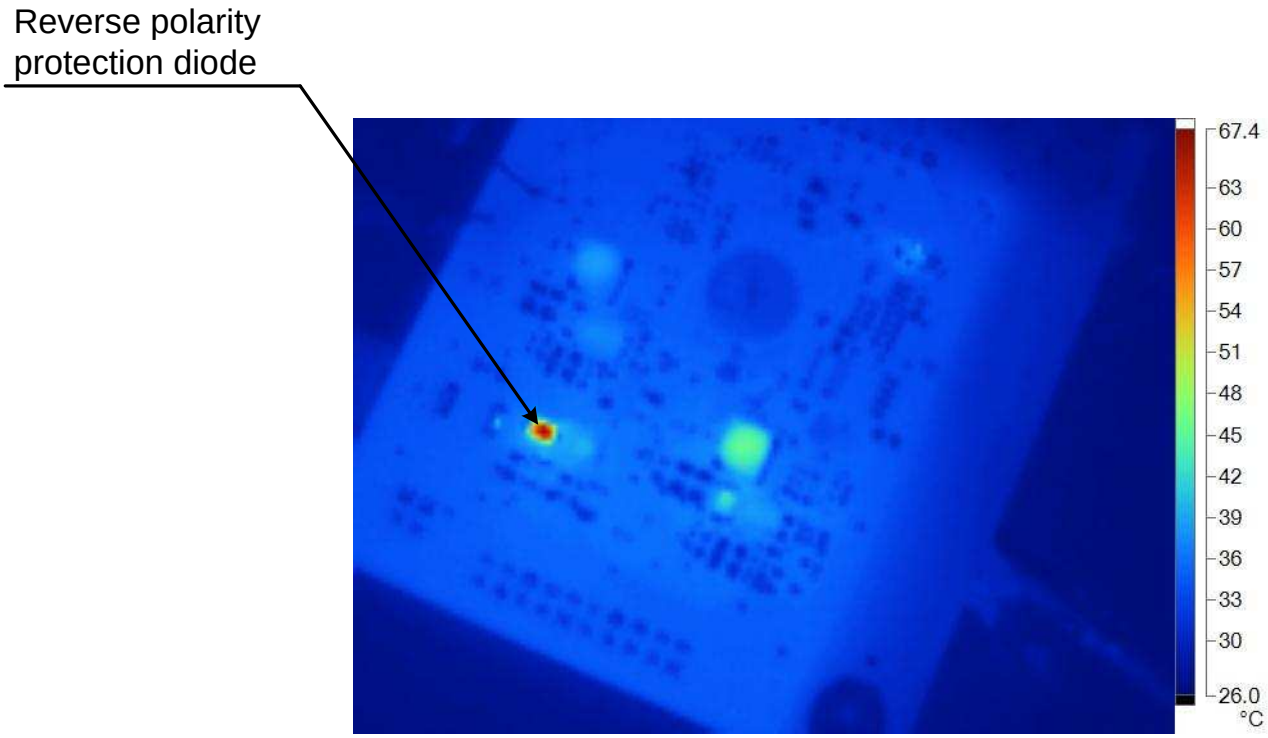


Figure 30. TIDA-00179 Thermal Picture at 15-V Input

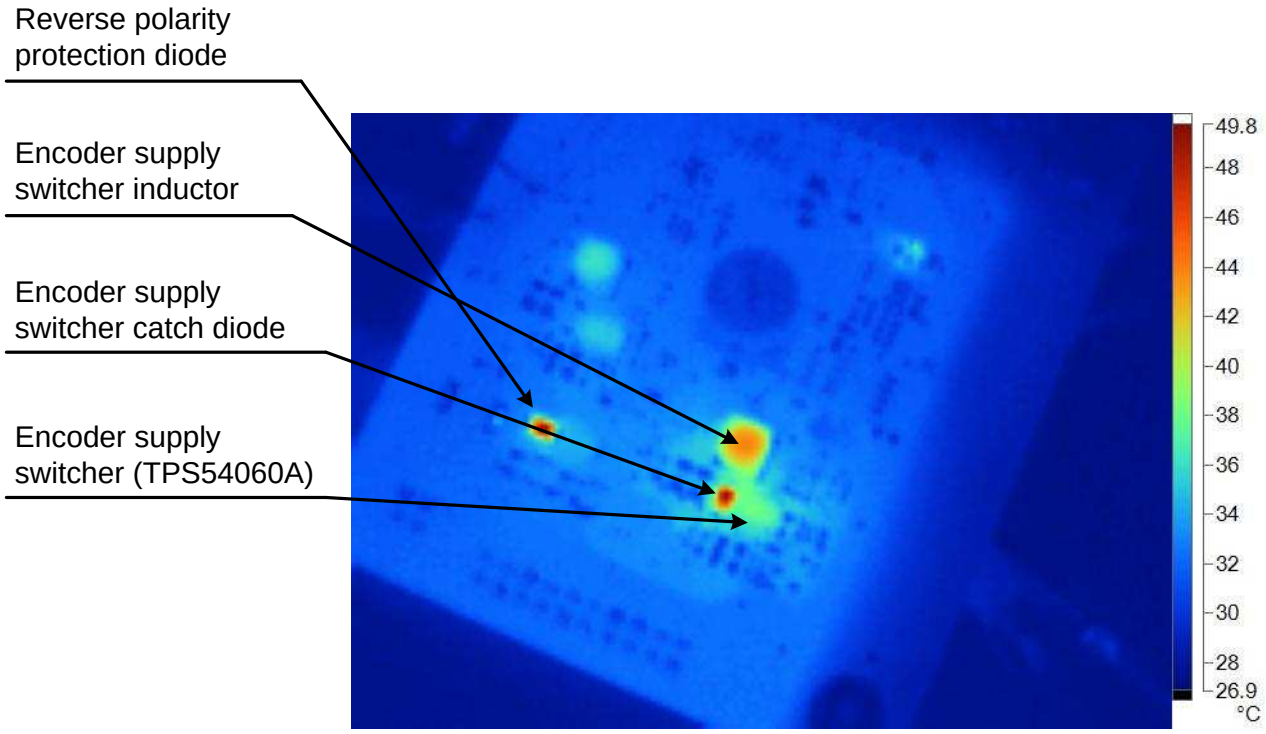


Figure 31. TIDA-00179 Thermal Picture at 24-V Input

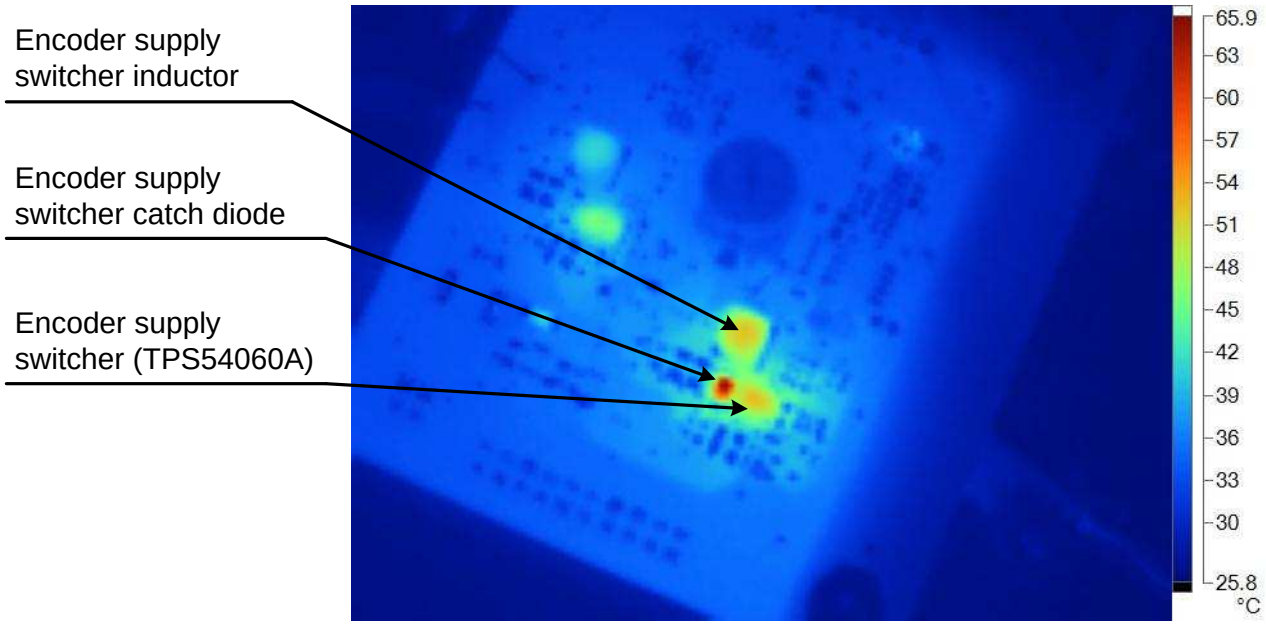


Figure 32. TIDA-00179 Thermal Picture at 60-V Input

6.2.5 Start-up

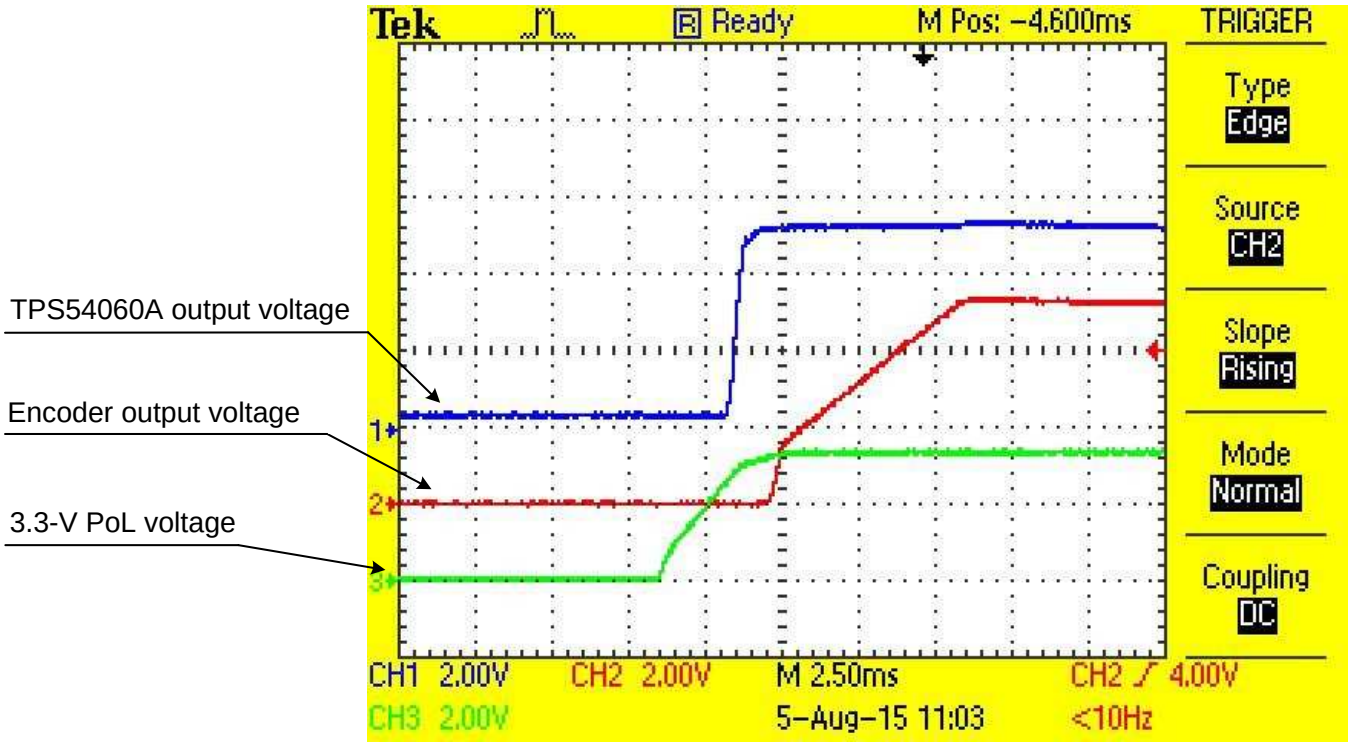


Figure 33. 5-V Encoder Power Supply Without Load Start-Up

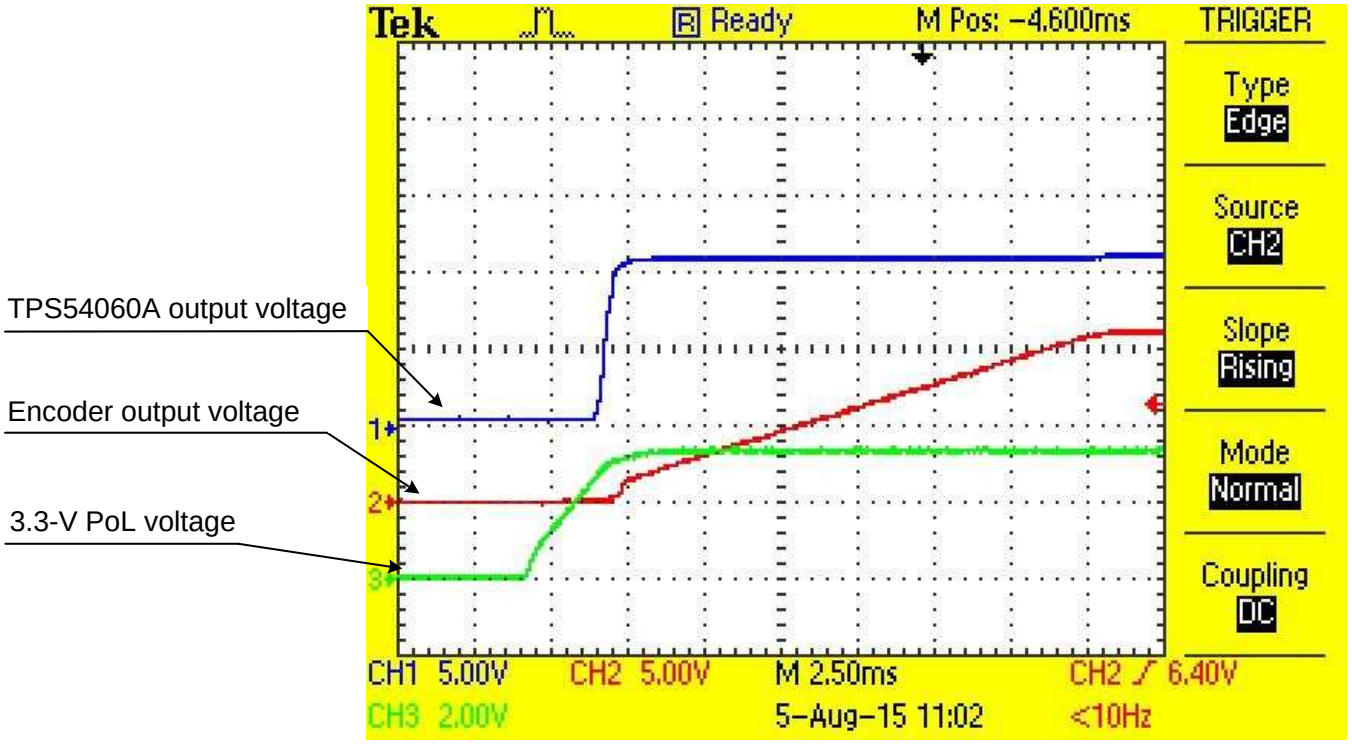


Figure 34. 11-V Encoder Power Supply Without Load Start-Up

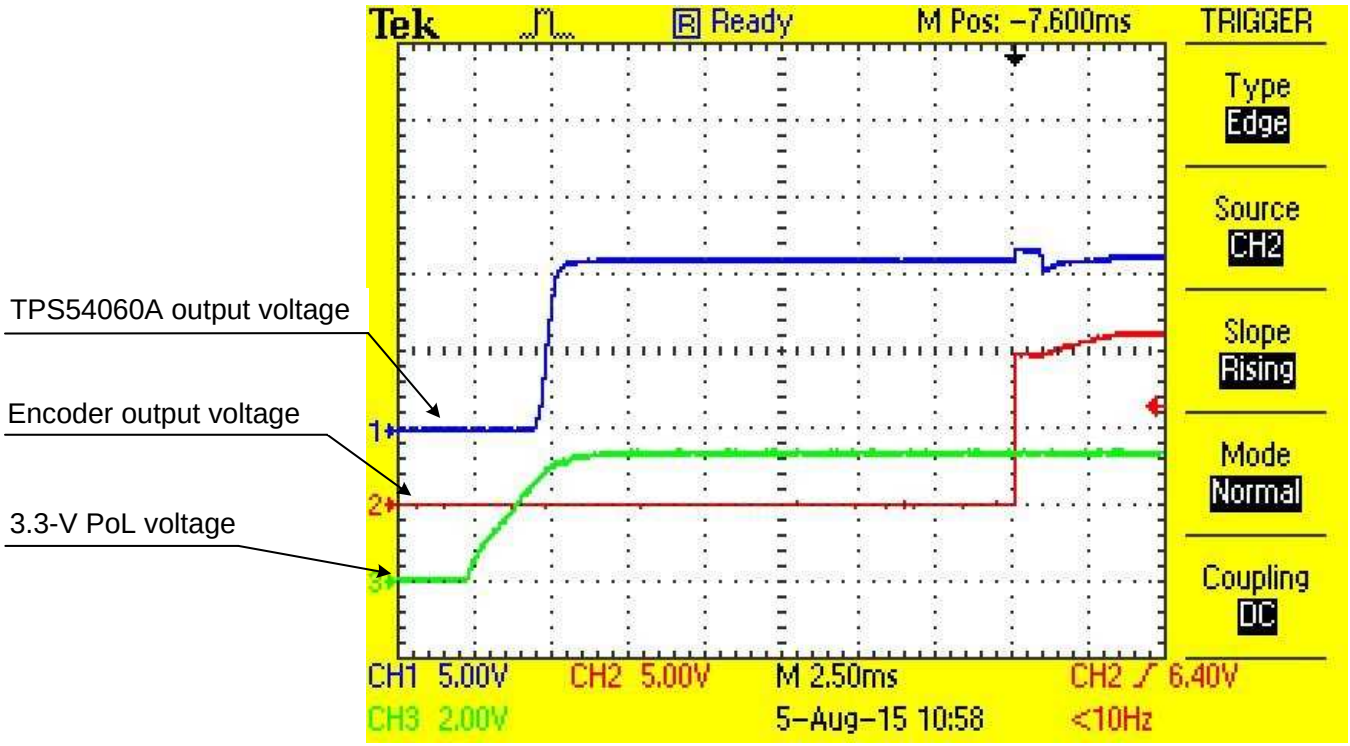


Figure 35. HIPERFACE DSL Encoder Power Supply Without Load Start-Up

6.2.6 Shutdown

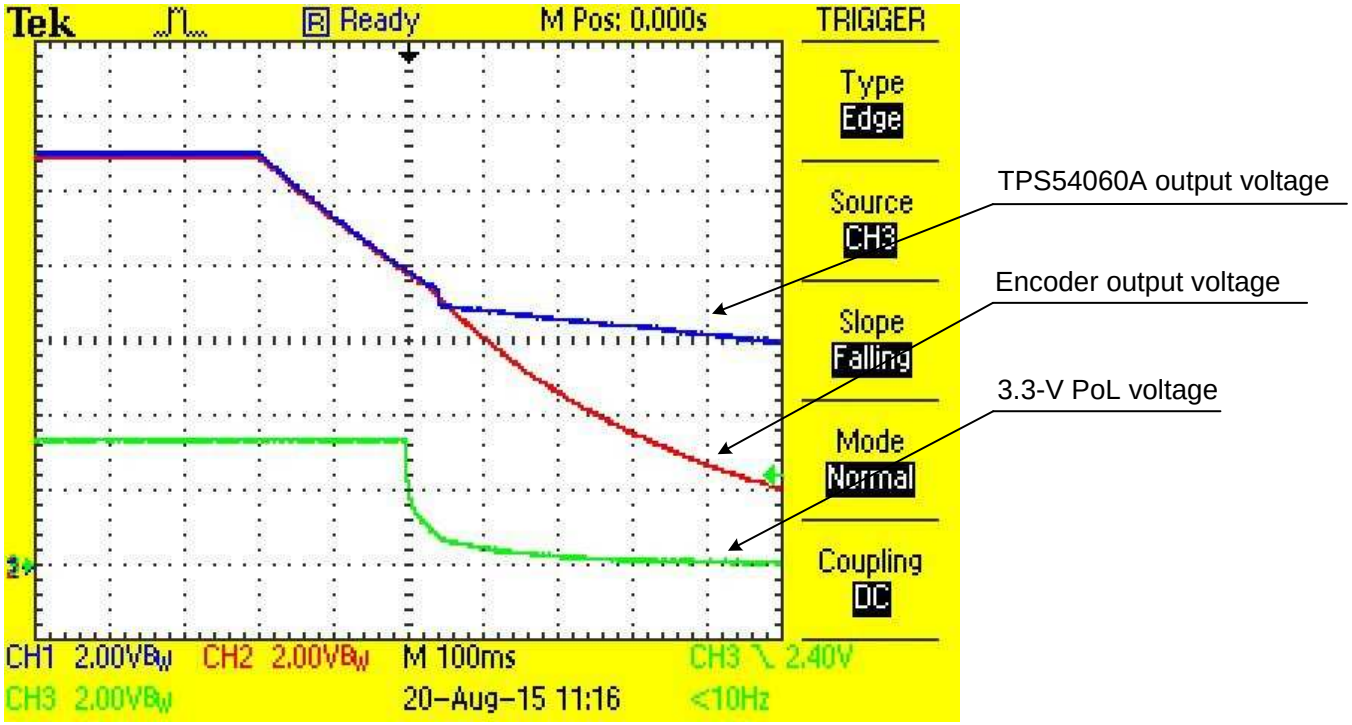


Figure 36. 11-V Encoder Power Supply Without Load Shutdown

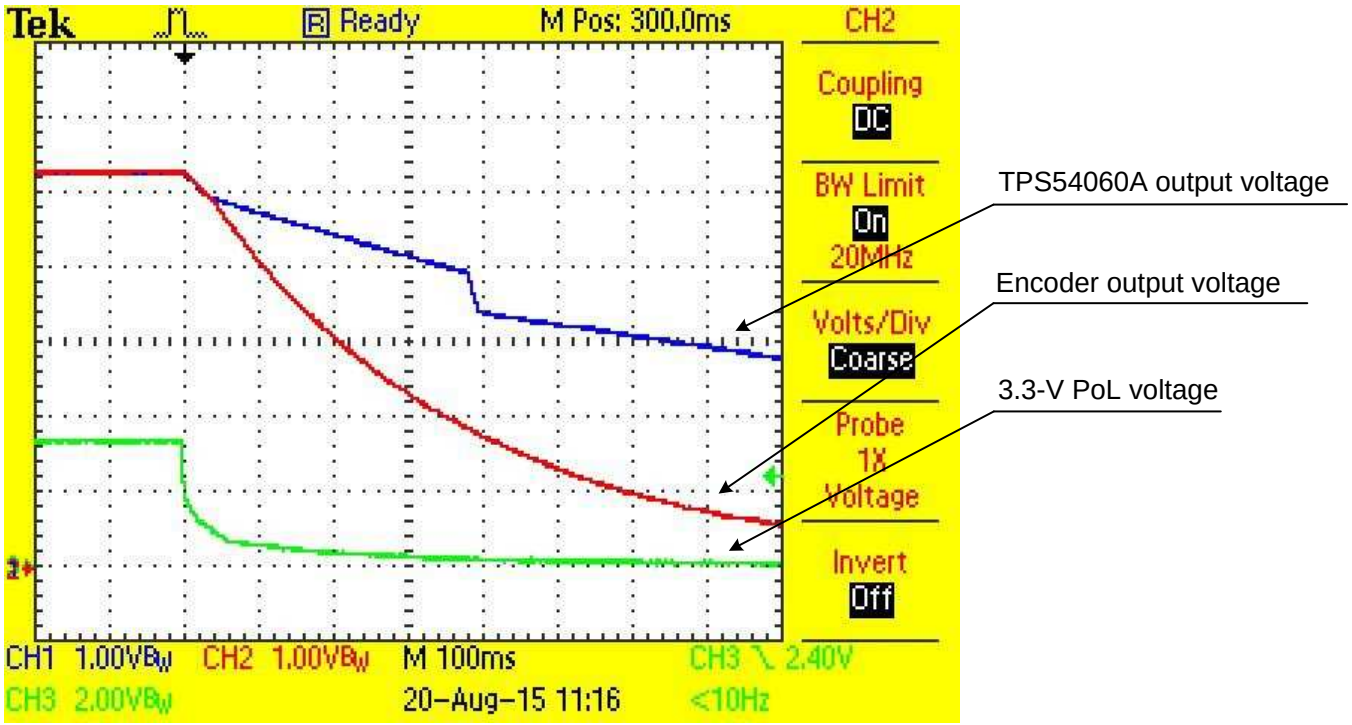


Figure 37. 5-V Encoder Power Supply Without Load Shutdown

6.2.7 Bode Plots

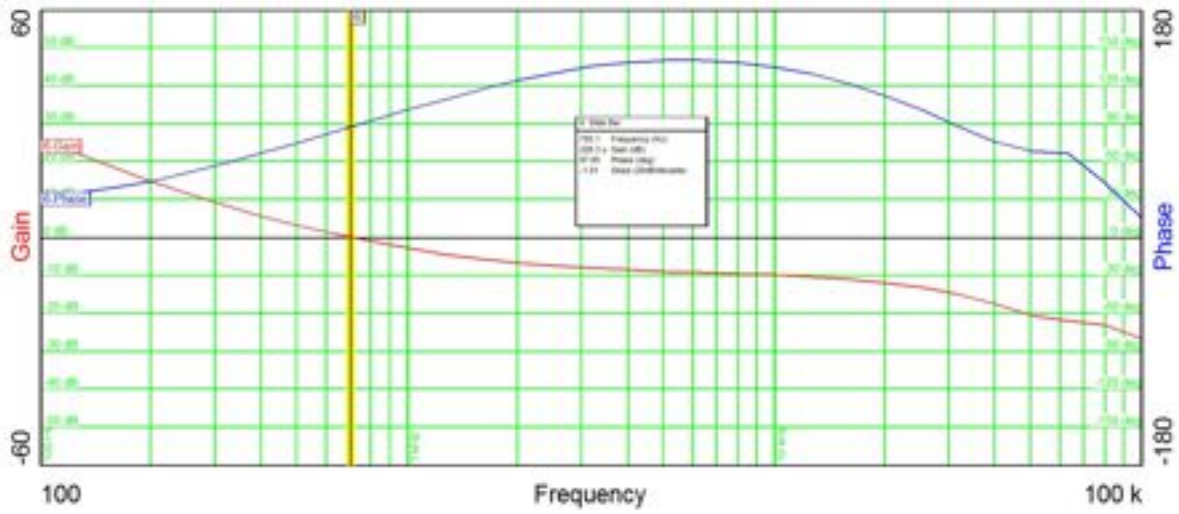


Figure 38. Bode Plot for 5-V Rail, 24-V Input, Full Load

Because all the encoders (except the 5-V BiSS encoders) could be supplied by the 11-V rail, particular attention is paid to the dynamic performance of the 11-V rail.

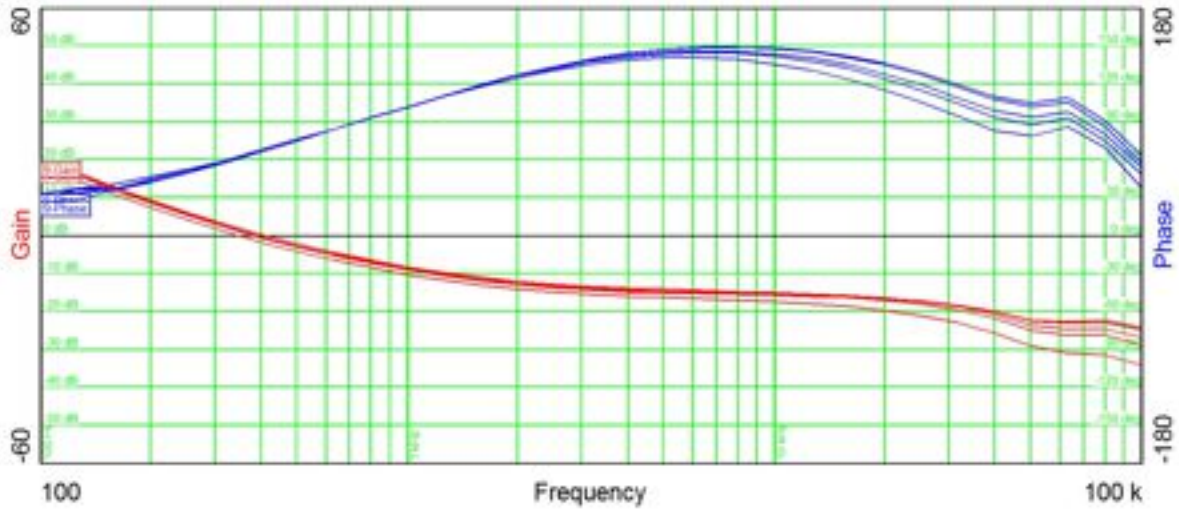


Figure 39. 11-V Rail Bode Plot Changes versus Input Voltage, Full Load

Table 30. System Bandwidth and Phase Margin (11-V Rail)

INPUT VOLTAGE	CROSS-OVER FREQUENCY	PHASE MARGIN
15 V	350 Hz	63 degrees
24 V	390 Hz	66 degrees
36 V	410 Hz	67 degrees
48 V	380 Hz	64 degrees
60 V	390 Hz	65 degrees

6.2.8 Synchronization

The TIDA-00179 offers also the possibility to synchronize the two power converters the TPS54060 and TPS54061. This allow a better EMI performance and reduces the input filter size and cost.

Yellow: TPS54061 switch node (phase)
Cyan: TPS54060A switch node (synchronized on the falling edge of the TPS54061 one)

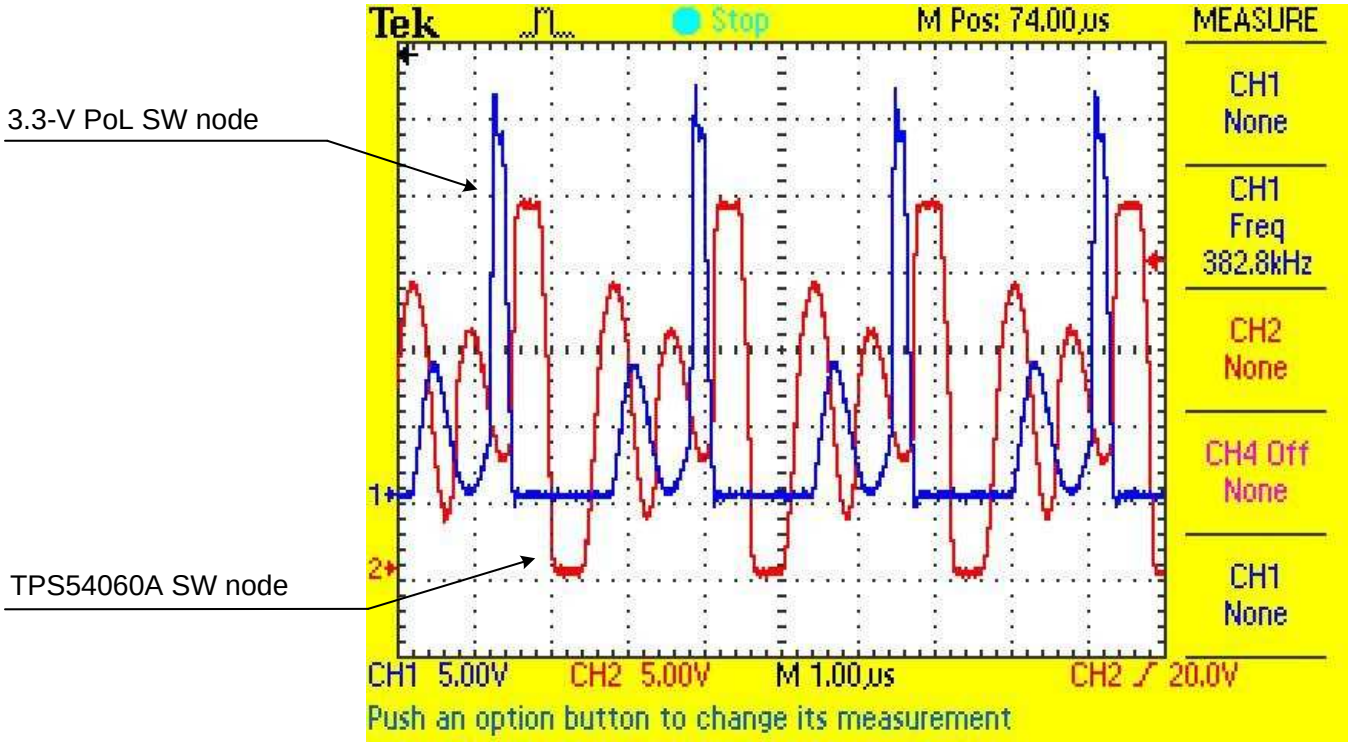


Figure 40. Synchronization of Two Switchers at Nominal Input Voltage (24 V)

6.2.9 Protections

To test the OCP, the output current slowly increases above the nominal 300-mA threshold, triggering the eFuse OCP.

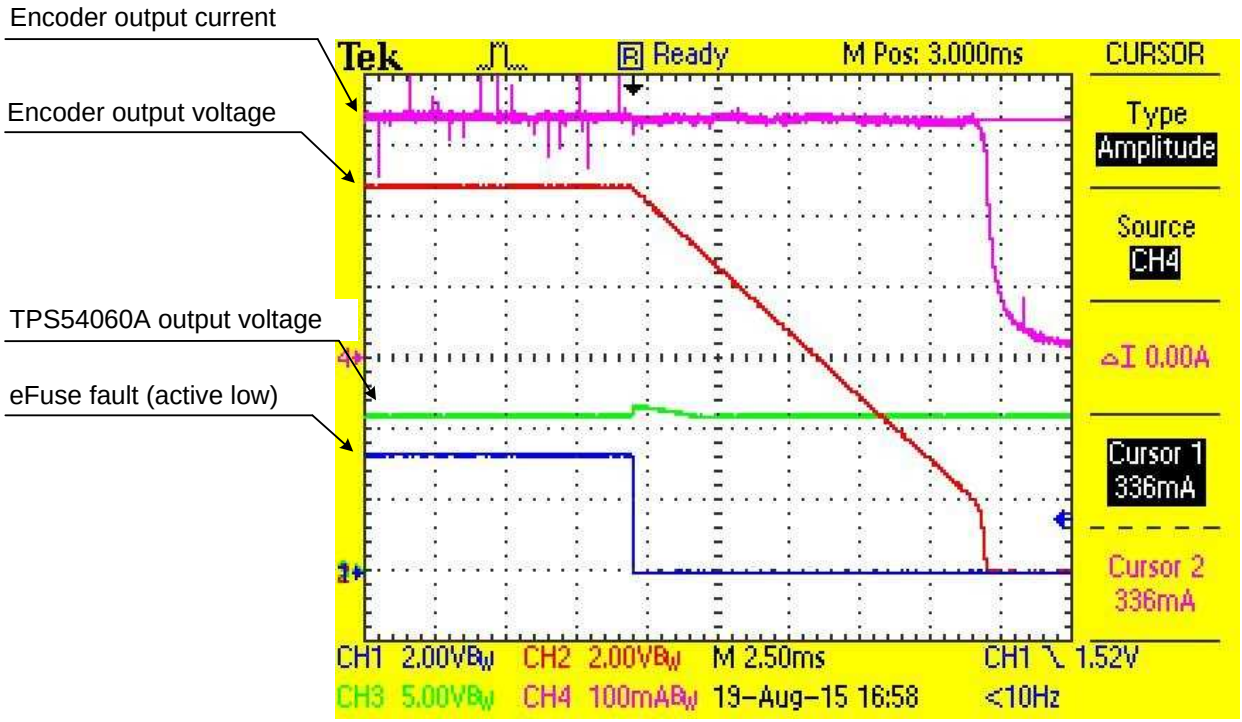


Figure 41. OCP

Start-up with the output in short circuit has been tested as well.

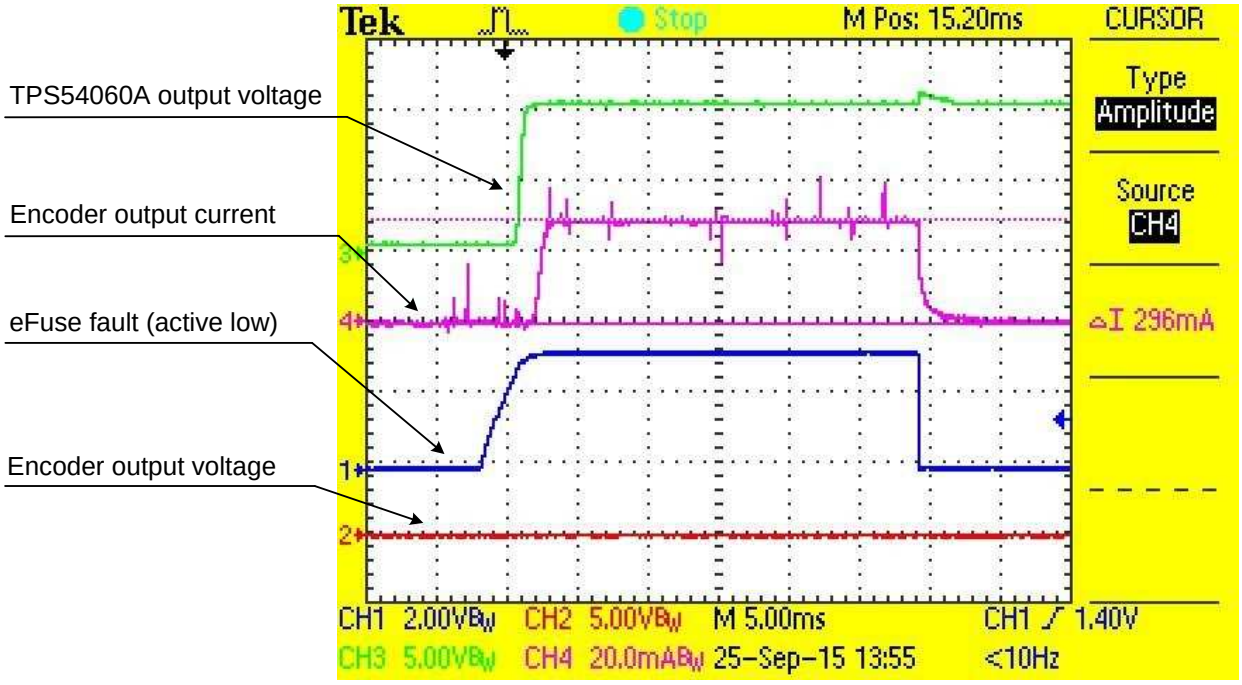


Figure 42. Encoder Power Supply Start-up (4-Wire Mode) With Output in Short Circuit

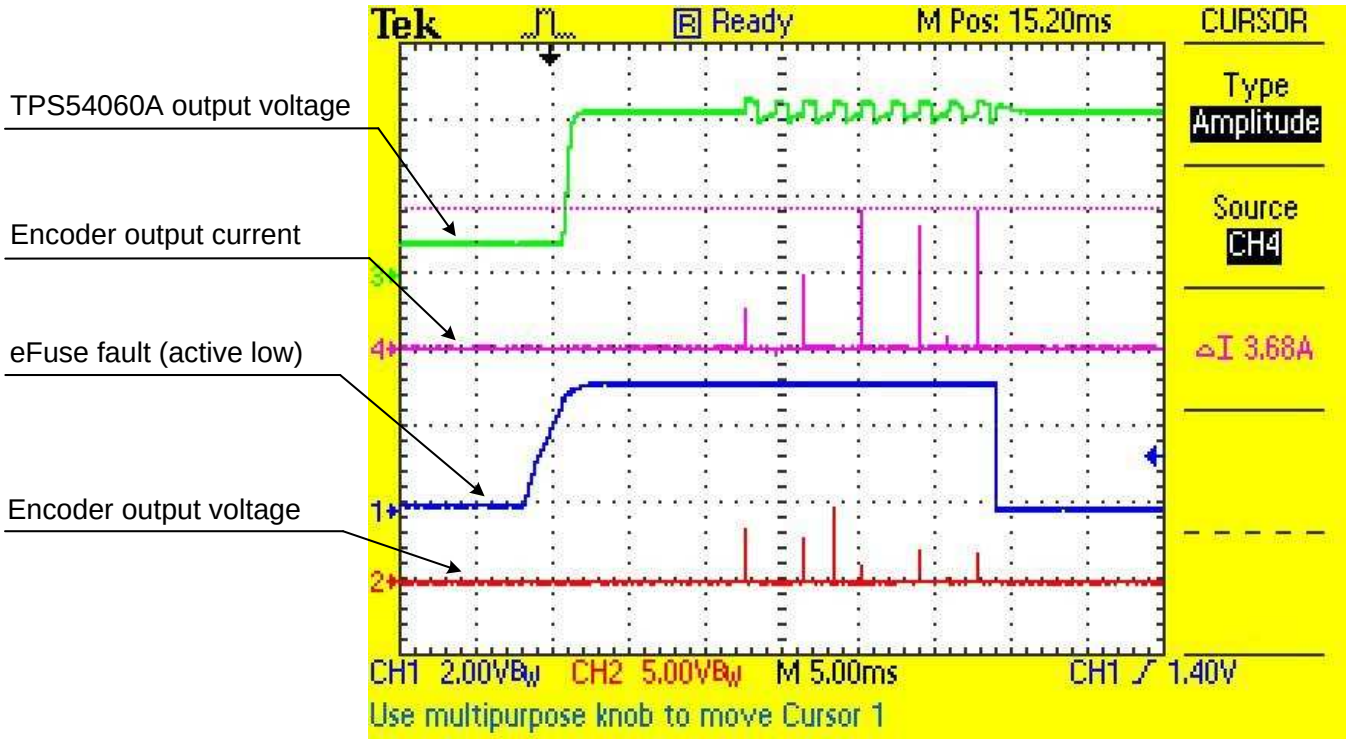


Figure 43. Encoder Power Supply Start-up (2-Wire HIPERFACE DSL Mode) With Output in Short Circuit

Note that many other protections are also covered by the TIDA-00179, such as UVP, OVP, and OTP. These are not tested here because they are IC performed (eFuse) and verified by the design.

6.3 3.3-V PoL Performance

6.3.1 Output Voltage Ripple

Despite the fact no real specification on the 3.3-V voltage rail ripple is defined, note how it is anyway well contained. Even at the worst case condition (60-V input, 0-mA output), the ripple is much lower than 150 mV_{PP}.

Table 31. 3.3-V Rail Voltage Ripple

INPUT VOLTAGE	OUTPUT CURRENT	OUTPUT VOLTAGE RIPPLE
15 V	0 mA	< 5 mV_{PP}
24 V	0 mA	< 5 mV_{PP}
36 V	0 mA	< 10 mV_{PP}
48 V	0 mA	≈ 70 mV_{PP}
60 V	0 mA	≈ 120 mV_{PP}
15 V	200 mA	< 5 mV_{PP}
24 V	200 mA	< 5 mV_{PP}
36 V	200 mA	< 10 mV_{PP}
48 V	200 mA	< 10 mV_{PP}
60 V	200 mA	≈ 100 mV_{PP}

6.3.2 Load and Line Regulation

Performances for the load and line regulation exceeded expectations (measured in Figure 44).

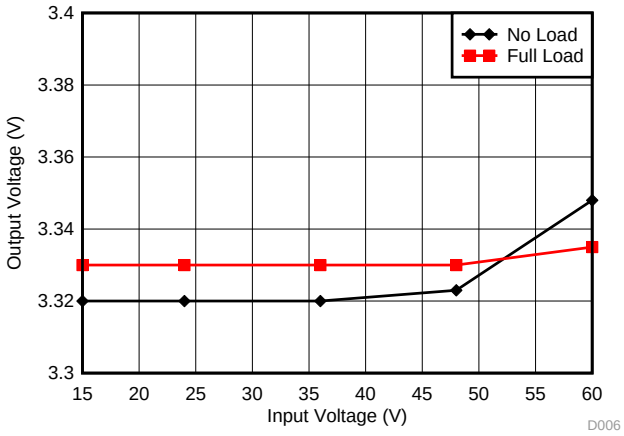


Figure 44. 3.3-V PoL

6.3.3 Efficiency

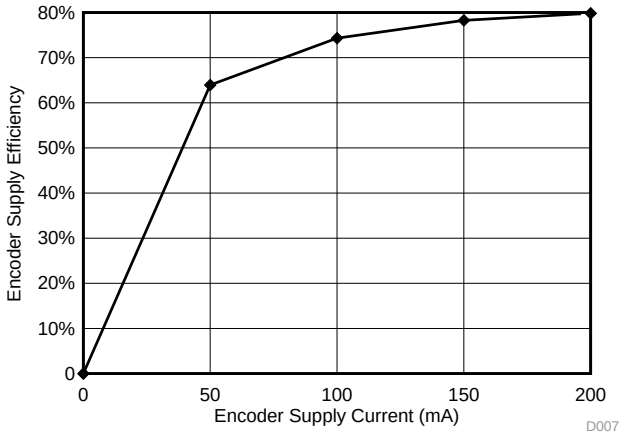


Figure 45. 3.3-V PoL Efficiency

6.3.4 Bode Plots

The 3.3-V PoL results are very stable with a crossover frequency (converter bandwidth) of 6 KHz and a phase margin of 73 degrees.

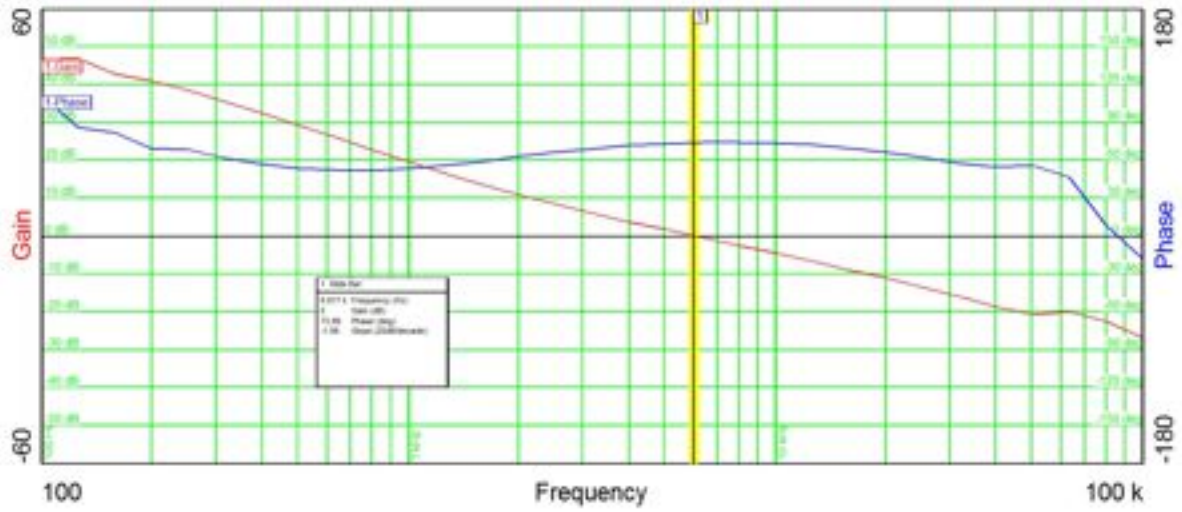


Figure 46. Bode Plot for 3.3-V Rail, 24-V Input, Full Load

6.4 System Performance With Encoders

6.4.1 Overview

The TIDA-00179 hardware was tested using various encoders from different manufacturers, in combination with the proper encoder connection cable to validated performance for cable length up to 100 m. For that purpose the reference design was connected to a host processor for the corresponding master protocol. For EnDat 2.2 tests, the reference design was connected to a Sitara AM437x Industrial Development Kit (IDK) to run the EnDat 2.2 master. The Sitara AM437x processor leverages the programmable real-time unit subsystem and industrial communication subsystem (PRU-ICSS) peripheral to implement the EnDat 2.2 master. The EnDat 2.2 master firmware is available for the Sitara AM437x processor as part of the SYS/BIOS industrial software development kit (SDK) for Sitara processors. A BiSS-C master is also available for Sitara AM437x, but was not tested.

For the HIPERFACE DSL tests the TIDA-00179 hardware was connected to a modified PGT-09-S DSL HIPERFACE DSL Programming Tool and Analyzer from Sick along with the corresponding software.

6.4.2 Test Setup

To test the system with the TIDA-00179 universal digital interface with an EnDat 2.2 position encoder, the EnDat 2.2 master implementation on Sitara AM4x Cortex A9 was used. The TIDA-00179 design was connected to four of the AM437x GPIO ports of ICSS0_PRU0, called EnDat1_CLK, EnDat1_OUT, EnDat1_IN and EnDat1_OUTEN, by using a corresponding adapter.

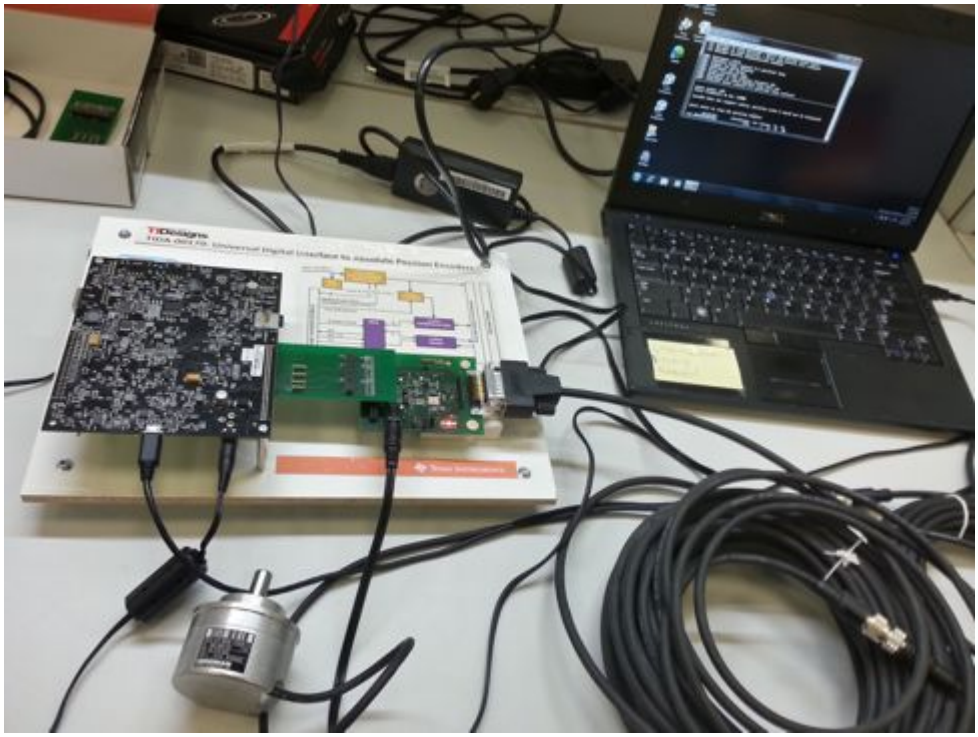


Figure 47. Setup for TIDA-00179 Test With HEIDENHAIN EnDat 2.2 Encoders

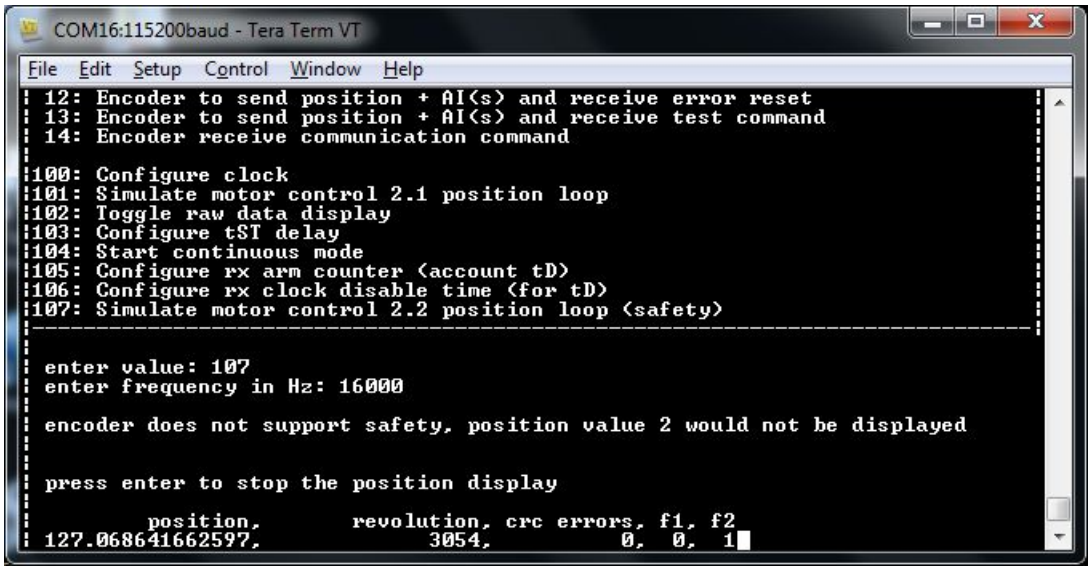


Figure 48. Sitara AM437x EnDat 2.2 Firmware Terminal Interface

For the HIPERFACE DSL IP Core (Master) a modified PGT-09-S DSL HIPERFACE DSL Programming Tool and Analyzer from Sick was used. The onboard RS-485 transceiver was removed from the PGT-09S PCB and the 3.3-V logic level IO signals DSL_OUT, DSL_IN and DSL_EN and GND on the solder pads were connected through wires to the TIDA-00179 host processor interface.

Figure 49. Setup for TIDA-00179 Test With 2-Wire HIPERFACE DSL Encoder

The HIPERFACE DSL Encoder Browser software with the PGT-09-S is used to validate the communication with the HIPERFACE DSL encoder.

6.4.3 Start-Up With Encoder

Different encoders have been tested at different working configurations. Voltage and current profiles have been acquired and reported in this section.

The tests are performed in the worst case conditions (minimum V_{IN} = 15 V) and at the nominal supply (24 V).

The following encoders have been tested:

- Wachendorff WDGF 58M (BiSS)
- HEIDENHAIN ROC 425 (EnDat 2.2)
- HEIDENHAIN ROQ 437 (EnDat 2.2)
- HEIDENHAIN ROQ 1035 (EnDat 2.2)
- Sick EKM 36 (2-wire HIPERFACE DSL)

Results are shown in Figure 50 to Figure 55:

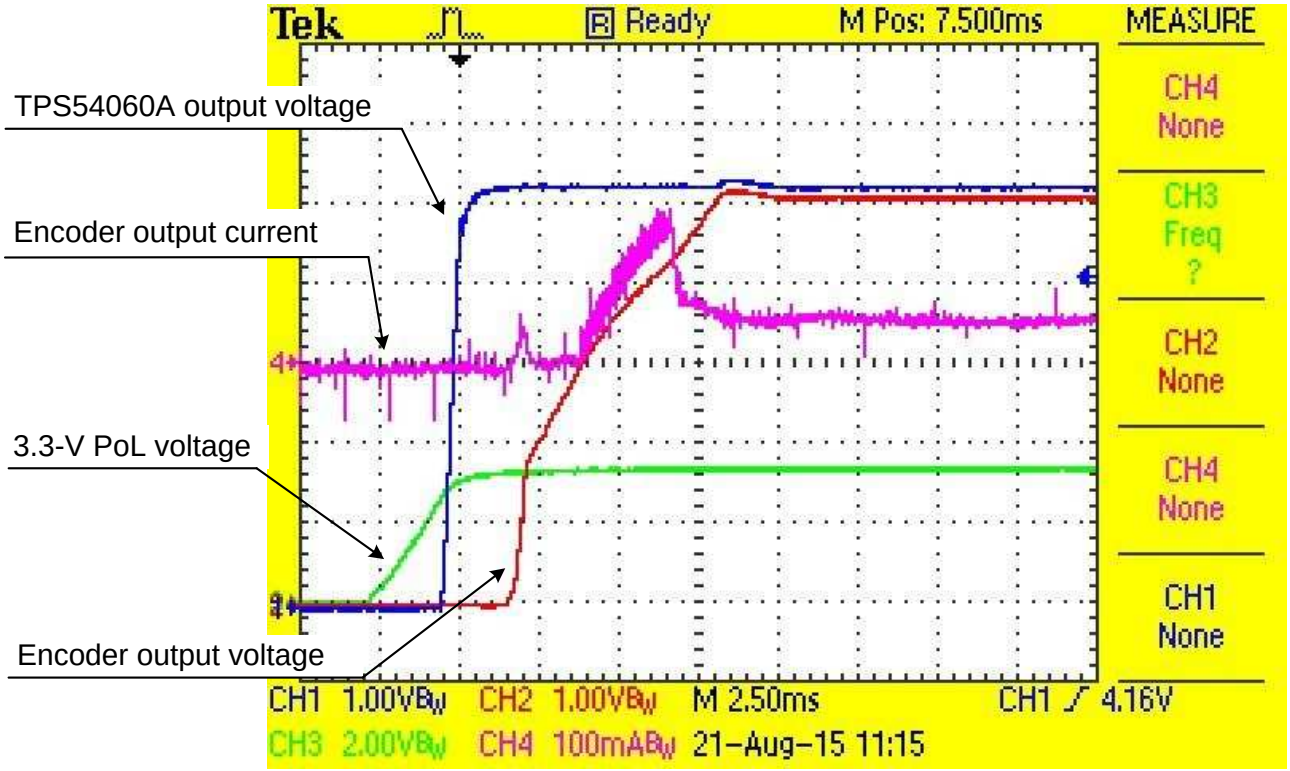


Figure 50. Encoder Power Supply Startup Sequence With BiSS WDGF 58M Encoder at 5 V

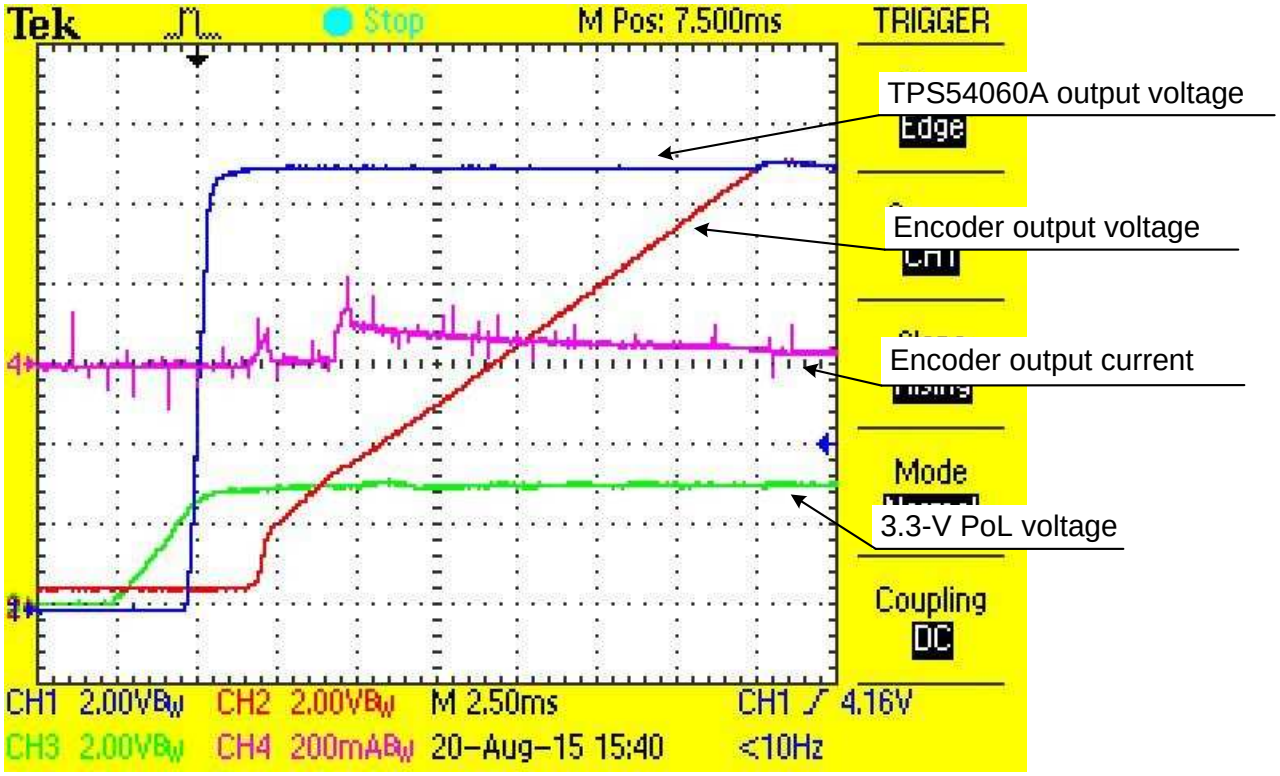


Figure 51. Encoder Power Supply Startup Sequence With EnDat 2.2 Encoder ROC 425 at 11 V

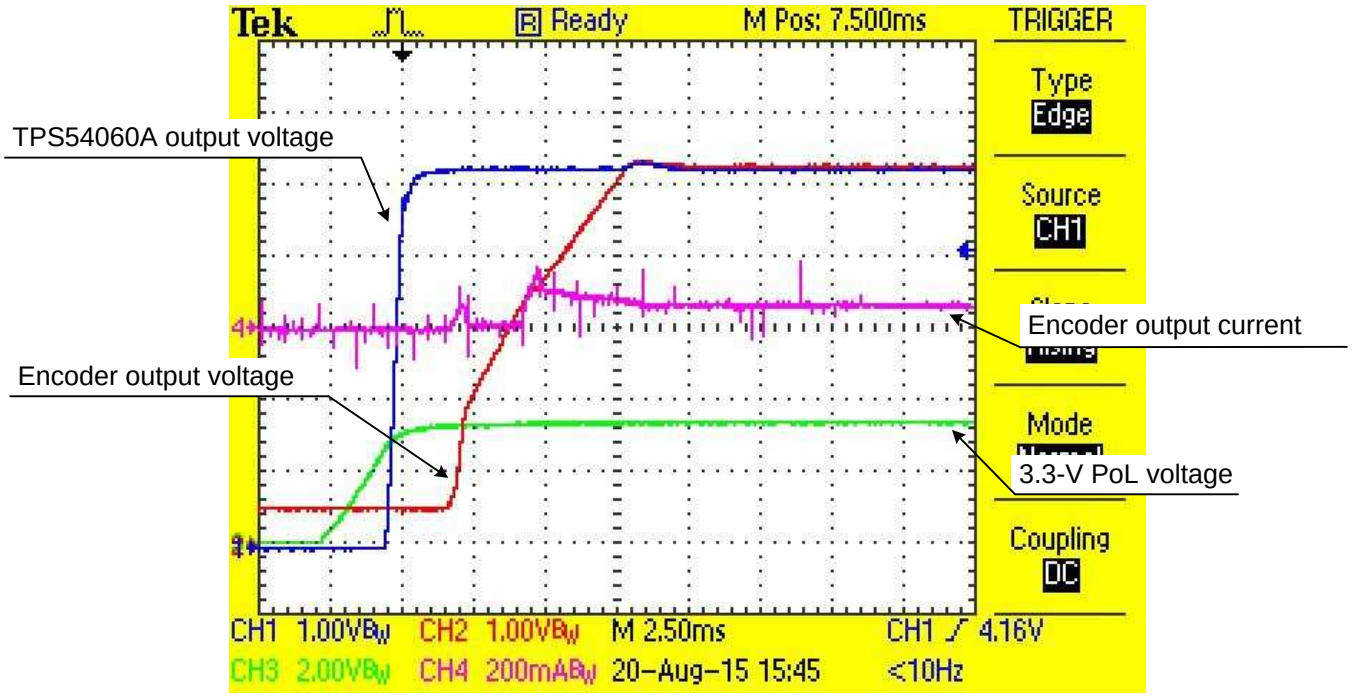


Figure 52. Encoder Power Supply Startup Sequence With EnDat 2.2 Encoder ROQ 437 at 5 V

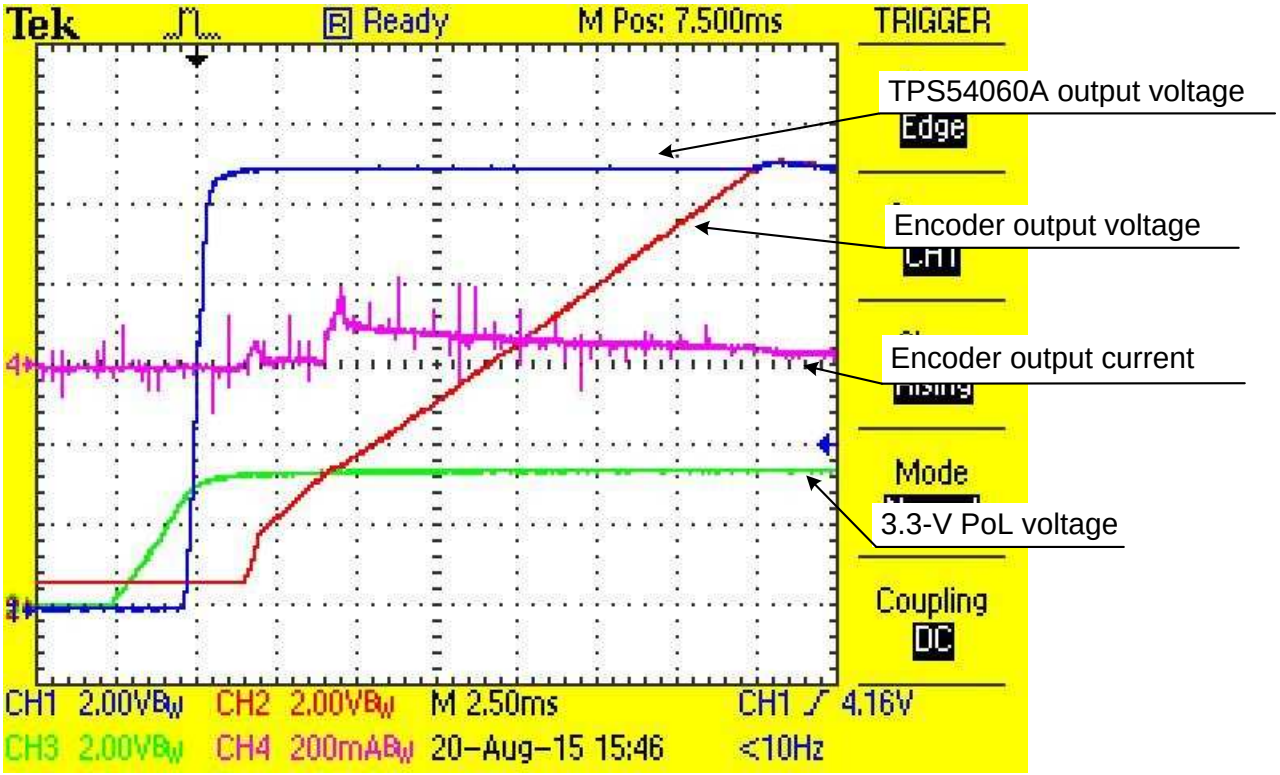


Figure 53. Encoder Power Supply Startup Sequence With EnDat 2.2 Encoder ROQ 437 at 11 V

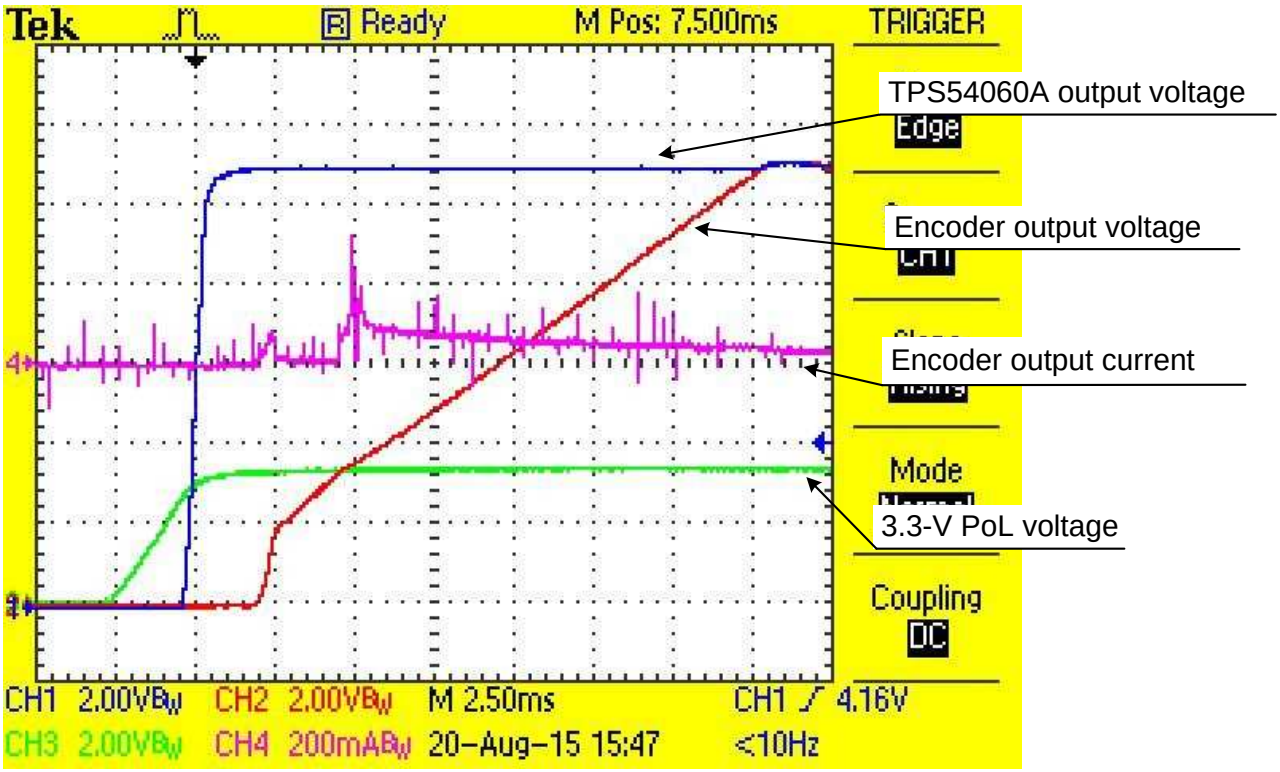


Figure 54. Encoder Power Supply Startup Sequence With EnDat 2.2 Encoder ROQ 1035 at 11 V

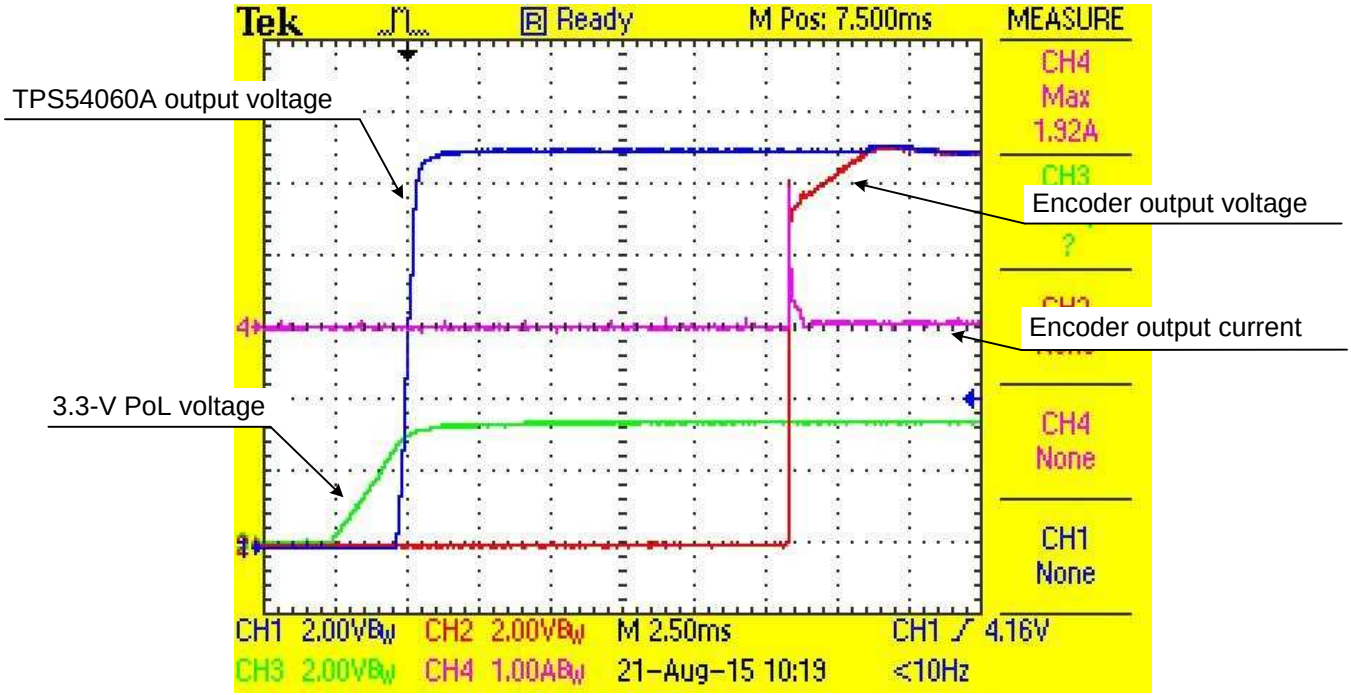


Figure 55. Encoder Power Supply Startup Sequence With HIPERFACE DSL 2-Wire EKM-36

Note that the start-up with the encoder shows some spikes on the current waveform because the LEM current probe (which has a large coil) is sensitive to noise at these small currents.

6.4.4 Reach Rate Tests With Encoders

Communication tests for EnDat 2.2 and HIPERFACE DSL encoders have been performed. The longest available cable (100 m) has been considered as worst case scenario.

Communication between the encoders and host processor (through TIDA-00179) properly occurs for all tested encoders with no transmission error. For EnDat 2.2, the test results for the maximum clock frequency versus cable length are shown in Figure 56.

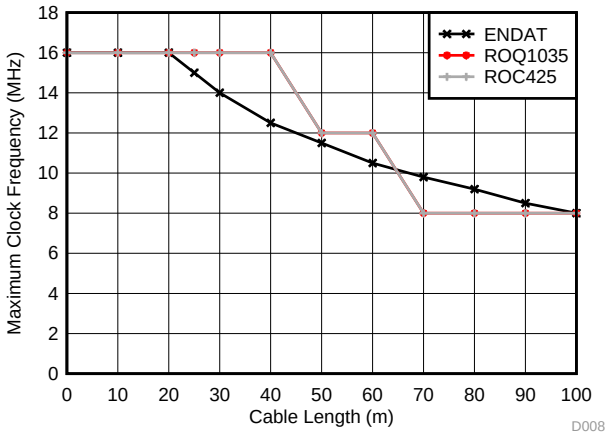


Figure 56. Reach Rate Tests for EnDat 2.2 Encoders

NOTE: Sitara AM437x EnDat 2.2 firmware GUI allowed only two settings for the EnDat 2.2 clock rate above 8 MHz, which were 12 MHz and 16 MHz.

For HIPERFACE DSL encoders, the encoder browser for the PGT-09-S DSL has been used again to check for communication errors in acquiring the position from the encoder. Different cable lengths have been tested; results are showed in Table 32:

Table 32. HIPERFACE DSL Communication Test Results

CABLE LENGTH (m)	COMMUNICATION ERRORS[1]
0	0
20	0
50	0
80	0
100	0

(1) Over 3 minutes

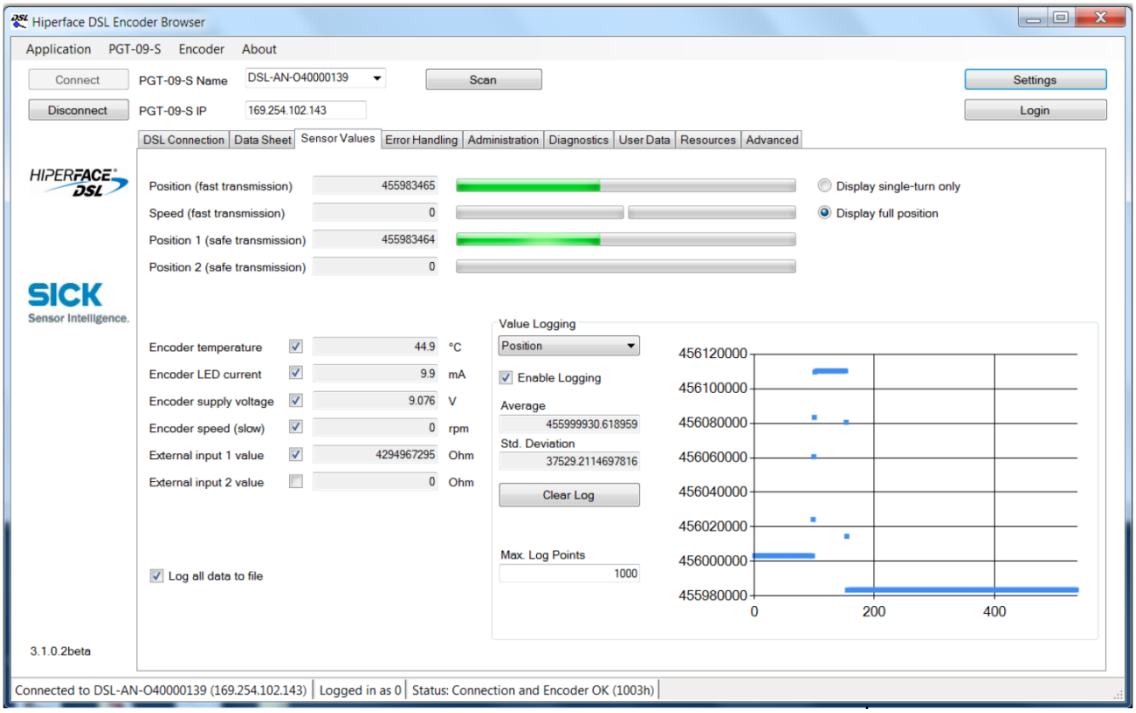


Figure 57. PGT-09-S DSL Screenshot With TIDA-00179 at 100-m Cable

6.5 EMC Test Results

The TI Design TIDA-00179 has been tested for IEC61000-4-2, 4-4, 4-5, and 4-6 (ESD, EFT, surge, and conducted RF) with test levels and performance criterion specified in the standard IEC 61800-3: "EMC immunity requirements and specific test methods applicable in adjustable speed, electrical-power drive systems".

The design is compliant to these standards and exceeds the voltage requirements.

Table 33. IEC618000-3 EMC Immunity Requirements for Second Environment and Measured Voltage Levels and Class

REQUIREMENTS					TIDA-00179 MEASUREMENTS		
PORT	PHENOMENON	BASIC STANDARD	LEVEL	PERFORMANCE (ACCEPTANCE) CRITERION	LEVEL	PERFORMANCE (ACHIEVED) CRITERION[1]	TEST
Enclosure ports	ESD	IEC61000-4-2	±4-kV CD or 8-kV AD, if CD not possible	B	±8-kV CD	B	PASS (EXCEED)
Ports for control lines and DC auxiliary supplies < 60 V	EFT	IEC61000-4-4	±2-kV/5-kHz, capacitive clamp	B	±4 kV	B	PASS (EXCEED)
	Surge 1.2/50 µs, 8/20 µs	IEC61000-4-5	±1 kV; Since shielded cable > 20 m, direct coupling to shield (2 Ω/500 A)	B	±2 kV	A	PASS (EXCEED)
	Conducted RF	IEC61000-4-6	0.15 to 80 MHz, 10 V/m, 80% AM (1 kHz)	A	20 V/m	A	PASS (EXCEED)

(1) Since the definition of the criterion A is customer specific, test results in class B are classified even if there was only a single CRC (communication) error.

The performance (acceptance) criterion is defined as follows:

Table 34. Performance (Acceptance) Criterion

PERFORMANCE (ACCEPTANCE) CRITERION	DESCRIPTION
A	The module shall continue to operate as intended. No loss of function or performance even during the test.
B	Temporary degradation of performance is accepted. After the test, the module shall continue to operate as intended without manual intervention.
C	During the test, loss of functions accepted, but no destruction of hardware or software. After the test, the module shall continue to operate as intended automatically, after manual restart, or power off, or power on.

6.5.1 Test Setup

The TI Design TIDA-00179 was tested at the testing laboratory of CSA Group Bayern in Strasskirchen, Germany. Figure 58 shows the basic setup for the TIDA-00179 design.

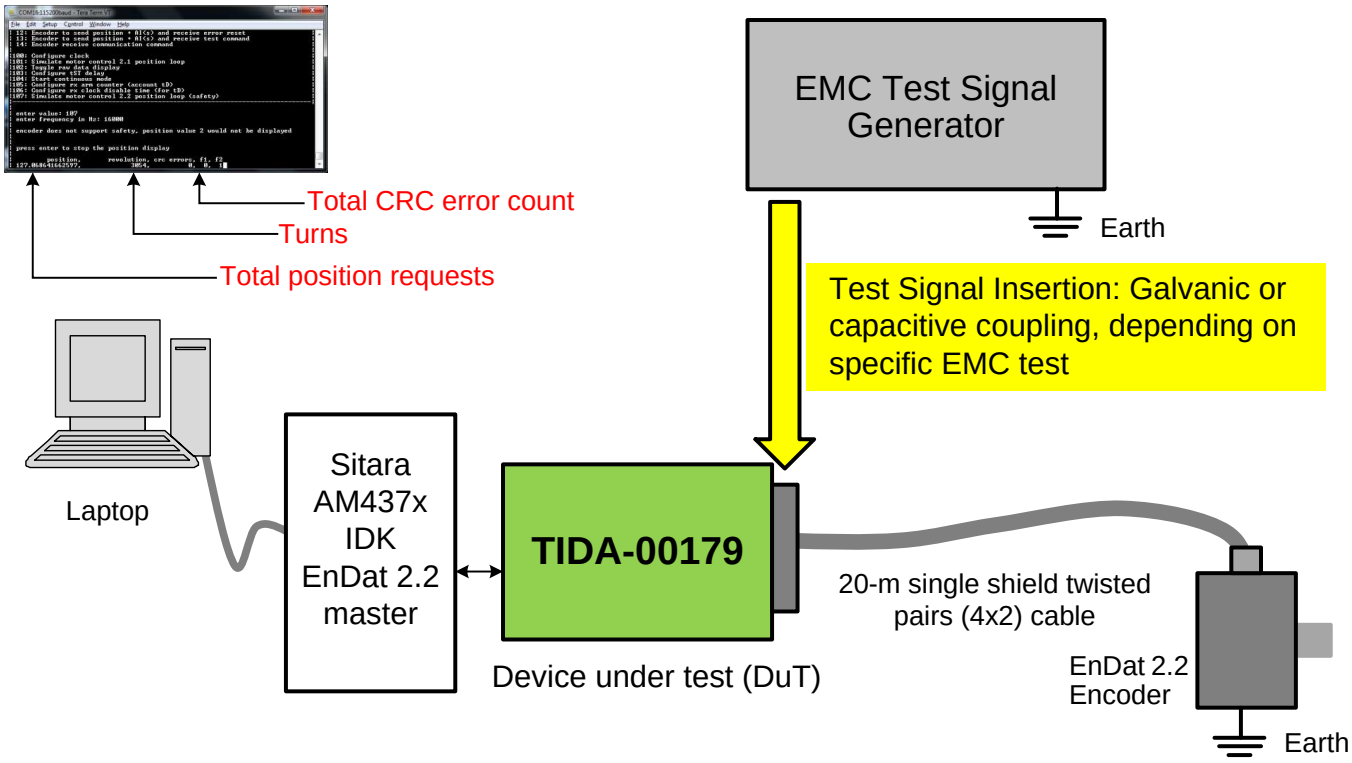


Figure 58. TIDA-00179 EMC Test Setup

To measure the TIDA-00179 EMC performance, an EnDat 2.2 encoder has been connected to the system and the number of the CRC errors that occur during the EMC test have been tracked and recorded.

Furthermore, since the encoder is not moved (standstill), the absolute position is monitored as well.

For this test, the encoder HEIDENHAIN ROQ 437 has been used. The EnDat 2.2 Master on the Sitara AM437x was configured for 8 MHz EnDat 2.2 clock. To emulate a typical use case the position was continuously requested at a 16 kHz update rate using the MOD command "encoder send position". The Sitara AM437x firmware implements a CRC error counter, which continuously counts the number of CRC error communication errors.

Pictures of the specific test setups for ESD, EFT, surge, and conducted RF are shown in the following sections.

6.5.2 IEC-61000-4-2 ESD Test Results

The ESD strike was applied to the SubD-15 female connector's shield. The shield was also connected to earth and the encoder was connected through a 22-m (1 m + 20 m + 1 m) shielded twisted pairs cable.

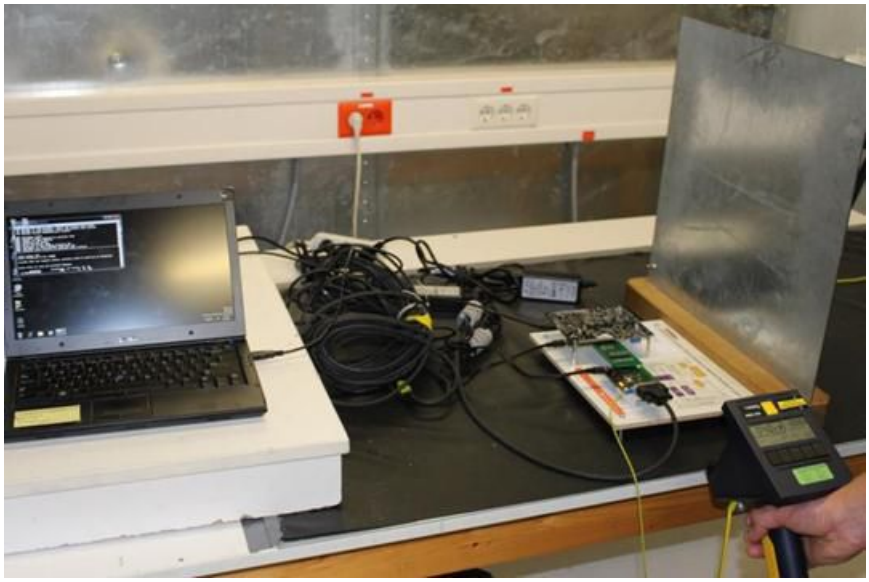


Figure 59. ESD Test Setup for TIDA-00179

Table 35 shows the complete ESD test results for contact and air discharge at voltage levels, which also exceed the requirements per IEC618000-3.

Table 35. ESD Test Results for TIDA-00179

PHENOMENON	BASIC STANDARD	LEVEL	TIDA-00176 CONNECTOR	ACHIEVED PERFORMANCE CRITERION	COMMENT
ESD	IEC61000-4-2	±4-kV contact discharge	SubD-15	B	
ESD	IEC61000-4-2	±6-kV contact discharge	SubD-15	B	Not required per IEC61800-3
ESD	IEC61000-4-2	±8-kV contact discharge	SubD-15	B	Not required per IEC61800-3

Table 36. Communication (CRC) Errors During ESD Test

CRC ERRORS	OCCURRENCE AT 4-kV CD	OCCURRENCE AT 6-kV CD	OCCURRENCE AT 8-kV CD
Number of CRC errors	1	4	11

The position angle before and after the ESD tests was the same value within the standard angle distribution.

6.5.3 IEC-61000-4-4 EFT Test Results

A picture of the EFT test setup for TIDA-00179 is shown in Figure 60. During the test, the SubD-15 female connector was connected to the encoder by using a 22-m (1 m + 20 m + 1 m) shielded twisted pairs cable.

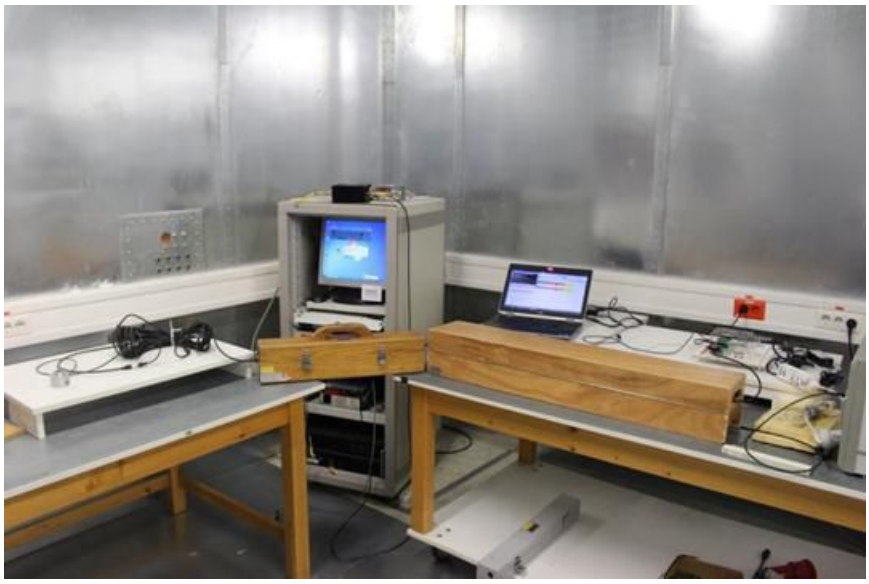


Figure 60. EFT Test Setup for TIDA-00179

Table 37. EFT Test Results for TIDA-00179

PHENOMENON	BASIC STANDARD	LEVEL	TIDA-00176 CONNECTOR	ACHIEVED PERFORMANCE CRITERION	COMMENT
EFT	IEC61000-4-4	±2-kV/5-kHz capacitive clamp	SubD-15	B	
EFT	IEC61000-4-4	±3-kV/5-kHz capacitive clamp	SubD-15	B	
EFT	IEC61000-4-4	±4-kV/5-kHz capacitive clamp	SubD-15	B	Not required per IEC61800-3

Table 38. Communication (CRC) Errors During EFT Test

CRC ERRORS	OCCURRENCE AT 2-kV EFT	OCCURRENCE AT 3-kV EFT	OCCURRENCE AT 4-kV EFT
Number of CRC errors	147 errors in 1.92M packets transmissions	1651 errors in 1.92M packets transmissions	2573 errors in 1.92M packets transmissions,
Packet error ratio	1 packet lost, 13,061 transmitted	1 packet lost, 1,163 transmitted	1 packet lost, 746 transmitted

The position angle before and after the EFT tests was the same value within the standard angle distribution.

6.5.4 IEC-61000-4-5 Surge Test Results

A picture of the surge test setup for TIDA-00179 is shown in Figure 61 and Figure 62. During the test, the SubD-15 female connector was connected to the encoder by using a 22-m (1 m + 20 m + 1 m) shielded twisted pairs cable.

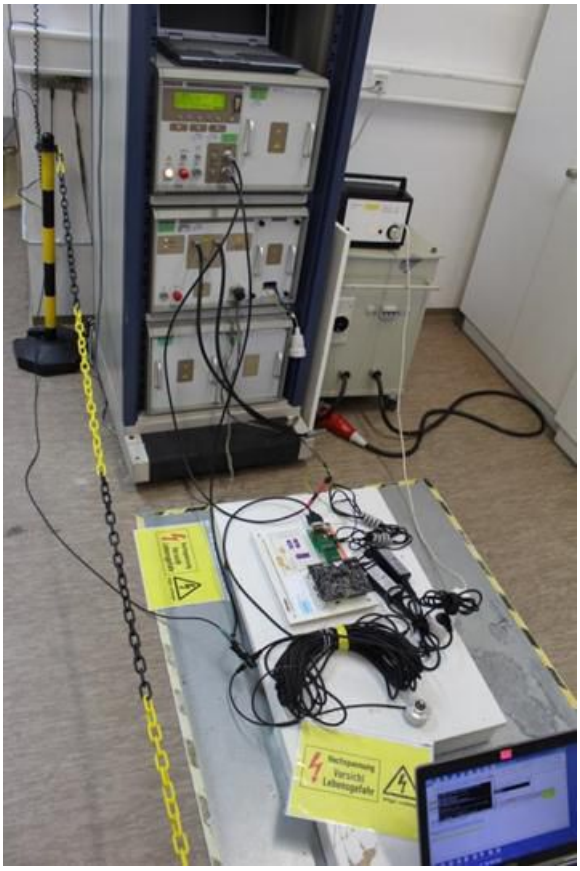


Figure 61. Surge Test Setup for TIDA-00179

Figure 62. Surge Test Setup for TIDA-00179 Details

Table 39. Surge Test Results for TIDA-00179

PHENOMENON	BASIC STANDARD	LEVEL	TIDA-00179 CONNECTOR	ACHIEVED PERFORMANCE CRITERION
Surge	IEC61000-4-4	±1 kV/2 Ω (20-m shielded cable)	SubD-15	A
Surge	IEC61000-4-4	±2 kV/2 Ω (20-m shielded cable)	SubD-15	A

There was no communication error occurred during the surge tests; neither the angle did not change before or after the tests (the measured difference of the absolute position was within normal distribution at a fixed angle).

6.5.5 IEC-61000-4-6 Conducted RF Test Results

A picture of the conducted RF test setup for TIDA-00179 is shown in Figure 63. During the test, the SubD-15 female connector was connected to the encoder by using a 22-m (1 m + 20 m + 1 m) shielded twisted pairs cable.

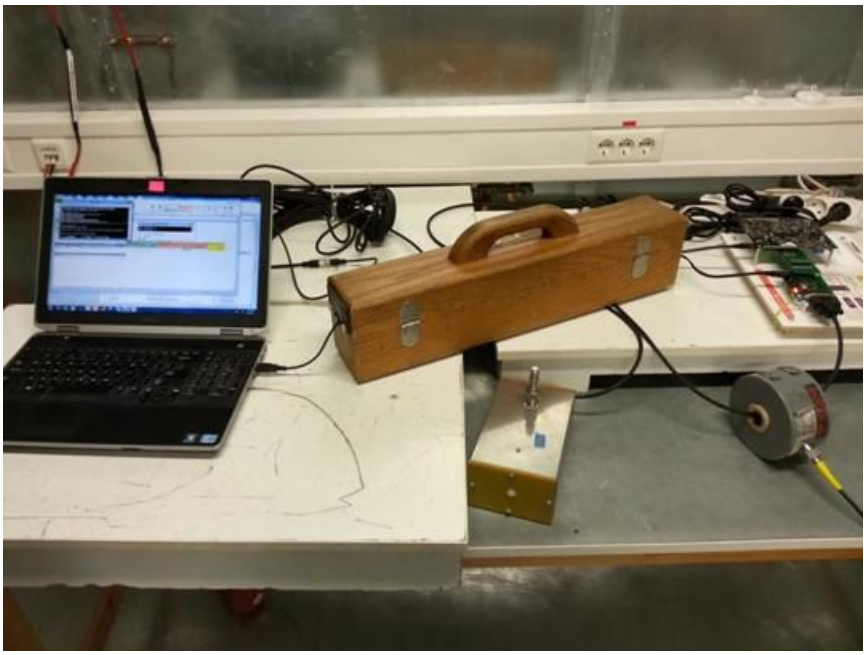


Figure 63. Conducted RF Test Setup for TIDA-00179

Table 40. Surge Test Results for TIDA-00179

PHENOMENON	BASIC STANDARD	LEVEL	TIDA-00179 CONNECTOR	ACHIEVED PERFORMANCE CRITERION
Conducted RF	IEC61000-4-6	0.15 to 80 MHz, 10 V/m, 80% AM (1 kHz)	SubD-15	A
Conducted RF	IEC61000-4-6	0.15 to 80 MHz, 20 V/m, 80% AM (1 kHz)	SubD-15	A

There was no communication error occurred during the surge tests; the angle did not change before or after the tests (the measured difference of the absolute position was within normal distribution at a fixed angle).

6.5.6 Additional ESD Test

This additional test proves the system robustness. In particular, a 15-kV air discharge has been applied directly to the Sub-D pins with unplugged encoder cable (on the Sub-D connector pins). After reconnecting the encoder cable, the software interface returns to communicate with the encoder properly.

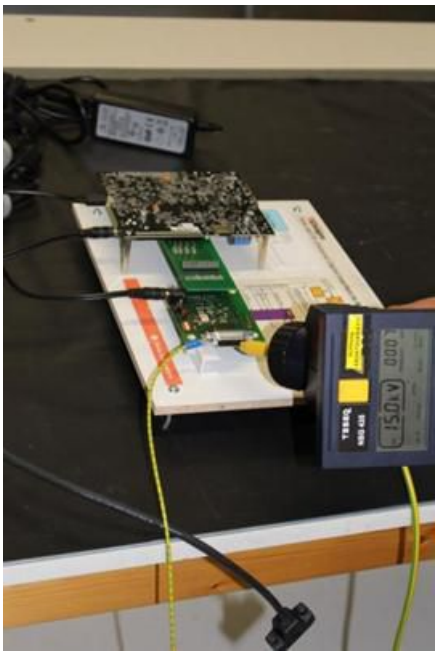


Figure 64. 15-kV Air Discharge ESD Test Setup

7 Design Files

7.1 Schematics

To download the schematics, see the design files at TIDA-00179.

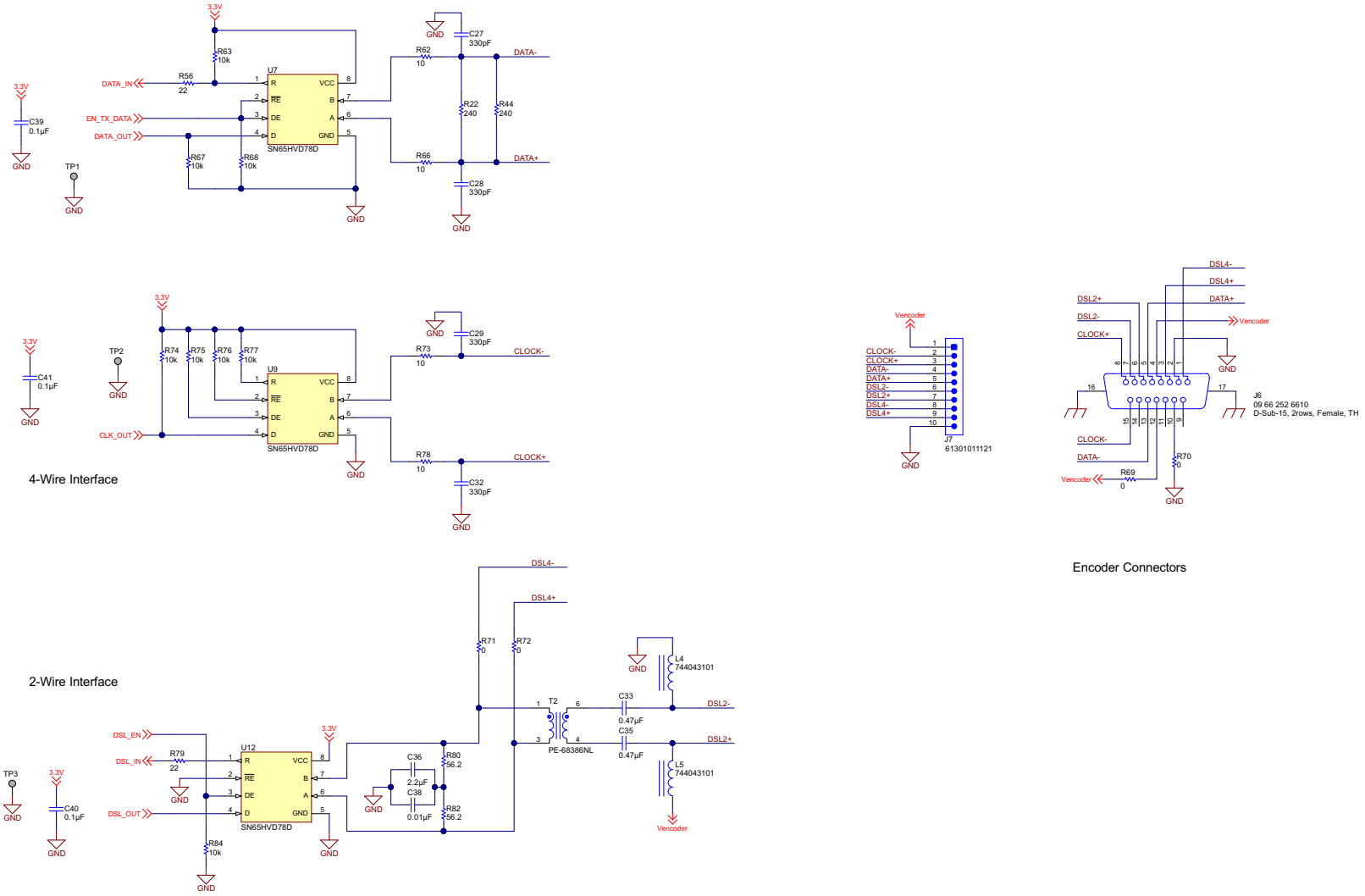


Figure 65. RS-485 Schematic

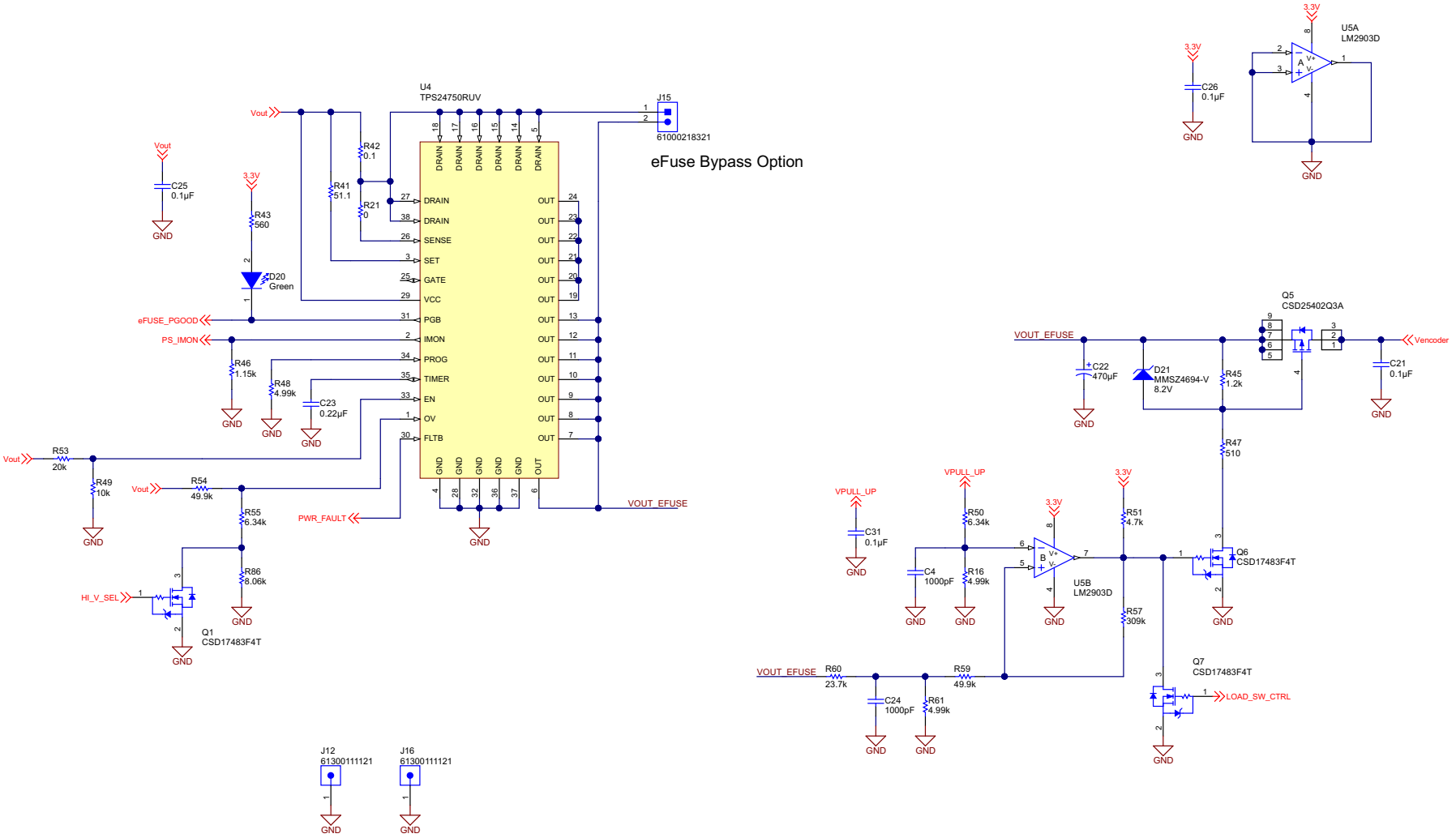


Figure 66. Protections Schematic

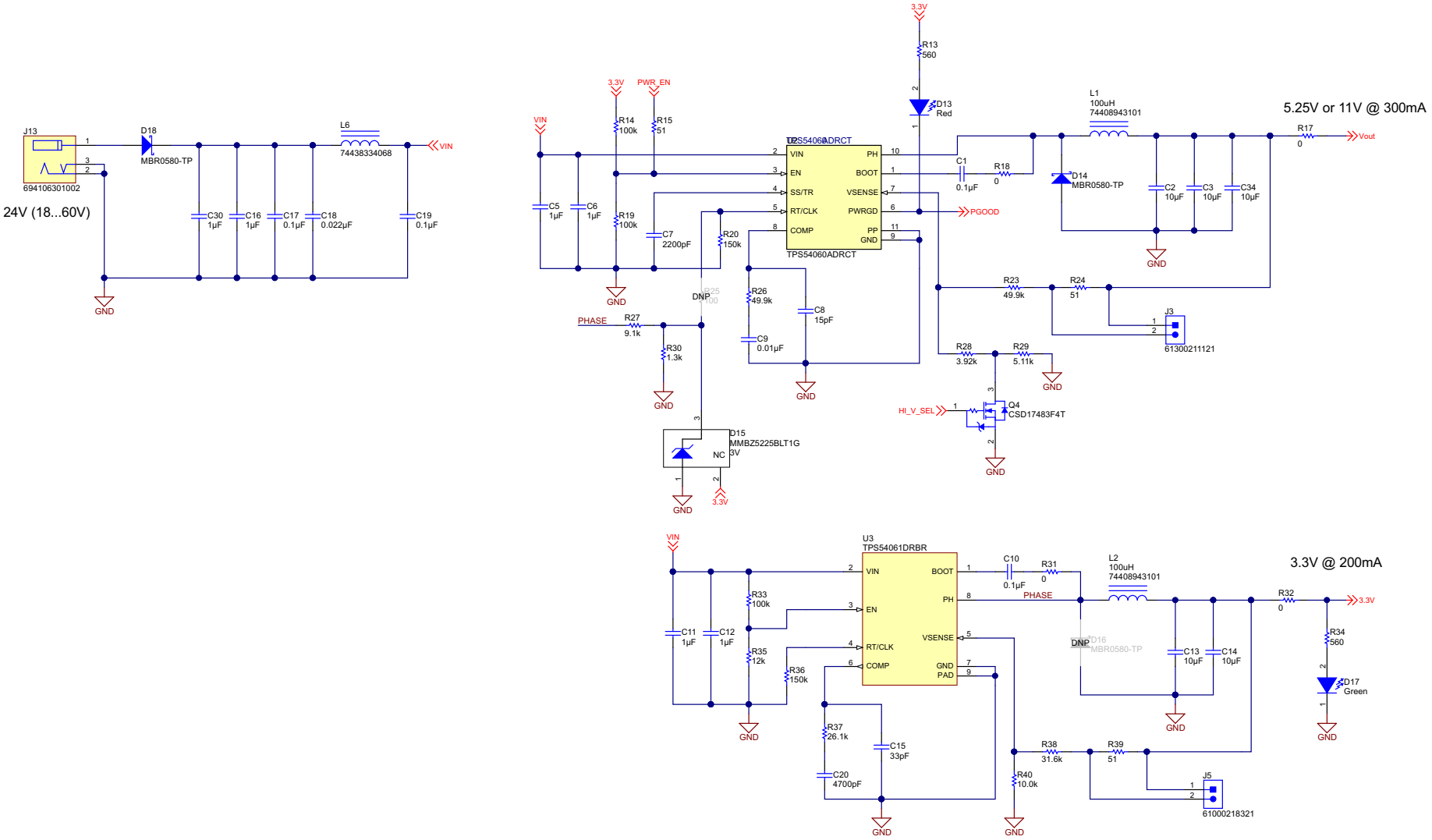


Figure 67. Power Schematic

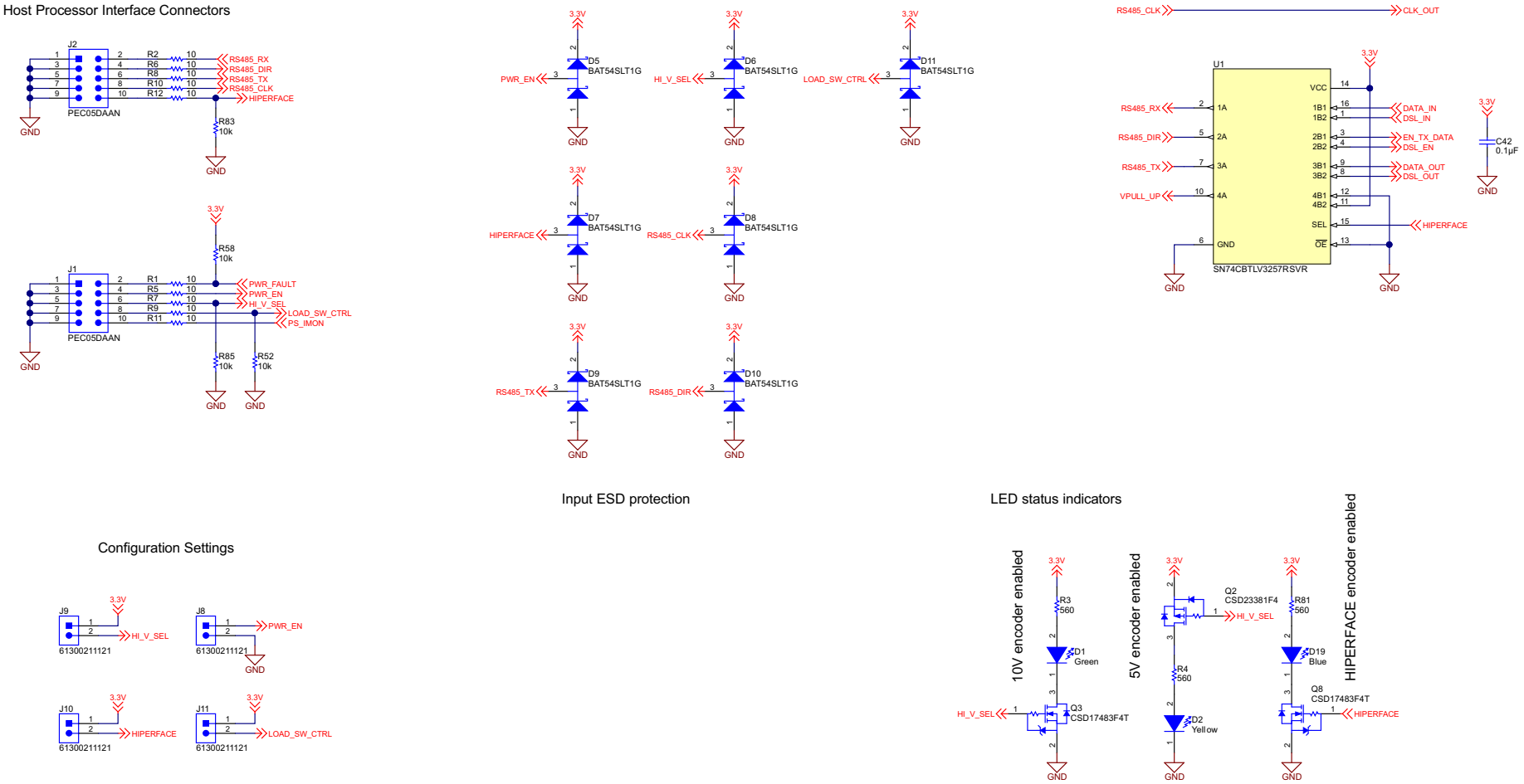


Figure 68. Host Interface MUX Schematic

7.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00179.

Table 41. BOM

ITEM	QTY	DESIGNATOR	VALUE	DESCRIPTION	MANUFACTURER	PARTNUMBER	PACKAGE REFERENCE
1	1	!PCB1		Printed Circuit Board	Any	TIDA-00179	
2	2	C1, C10	0.1uF	CAP, CERM, 0.1 µF, 100 V, +/- 10%, X7R, 0603	MuRata	GRM188R72A104KA35D	0603
3	5	C2, C3, C13, C14, C34	10uF	CAP, CERM, 10uF, 25V, +/-10%, X5R, 0805	TDK	C2012X5R1E106K125AB	0805
4	2	C4, C24	1000pF	CAP, CERM, 1000 pF, 25 V, +/- 10%, X7R, 0402	Wurth Elektronik	885012205044	0402
5	6	C5, C6, C11, C12, C16, C30	1uF	CAP, CERM, 1 µF, 100 V, +/- 10%, X7S, 0805	TDK	C2012X7S2A105K125AB	0805
6	1	C7	2200pF	CAP, CERM, 2200 pF, 16 V, +/- 10%, X7R, 0603_095	Wurth Elektronik	885012206036	0603_095
7	1	C8	15pF	CAP, CERM, 15 pF, 50 V, +/- 5%, C0G/NP0, 0402	Wurth Elektronik	885012005056	0402
8	1	C9	0.01uF	CAP, CERM, 0.01 µF, 16 V, +/- 10%, X7R, 0402	Wurth Elektronik	885012205031	0402
9	1	C15	33pF	CAP, CERM, 33 pF, 25 V, +/- 5%, C0G/NP0, 0402	Wurth Elektronik	885012005043	0402
10	2	C17, C19	0.1uF	CAP, CERM, 0.1 µF, 100 V, +/- 10%, X7R, 0805	Kemet	C0805C104K1RACTU	0805
11	1	C18	0.022uF	CAP, CERM, 0.022 µF, 100 V, +/- 10%, X7R, 0603	TDK	C1608X7R2A223K	0603
12	1	C20	4700pF	CAP, CERM, 4700 pF, 25 V, +/- 10%, X7R, 0402	MuRata	GRM155R71E472KA01D	0402
13	1	C21	0.1uF	CAP, CERM, 0.1 µF, 25 V, +/- 10%, X7R, 0603_095	Wurth Elektronik	885012206071	0603_095
14	1	C22	470uF	CAP, AL, 470 µF, 25 V, +/- 20%, 0.15 ohm, SMD	Wurth Elektronik	865080457015	D10xL10.5mm
15	1	C23	0.22uF	CAP, CERM, 0.22 µF, 16 V, +/- 10%, X7R, 0603_095	Wurth Elektronik	885012206048	0603_095
16	7	C25, C26, C31, C39, C40, C41, C42	0.1uF	CAP, CERM, 0.1 µF, 16 V, +/- 10%, X7R, 0603_095	Wurth Elektronik	885012206046	0603_095
17	4	C27, C28, C29, C32	330pF	CAP, CERM, 330 pF, 50 V, +/- 5%, C0G/NP0, 0603	Wurth Elektronik	885012006060	0603
18	2	C33, C35	0.47uF	CAP, CERM, 0.47 µF, 50 V, +/- 10%, X7R, 0805	Wurth Elektronik	885012207102	0805

Table 41. BOM (continued)

ITEM	QTY	DESIGNATOR	VALUE	DESCRIPTION	MANUFACTURER	PARTNUMBER	PACKAGE REFERENCE
19	1	C36	2.2uF	CAP, CERM, 2.2 µF, 25 V, +/- 10%, X7R, 0805	MuRata	GRM21BR71E225KA73L	0805
20	1	C38	0.01uF	CAP, CERM, 0.01 µF, 50 V, +/- 5%, C0G/NP0, 0805	MuRata	GRM2195C1H103JA01D	0805
21	3	D1, D17, D20	Green	LED, Green, SMD	Wurth Elektronik	150060GS75000	LED_0603
22	1	D2	Yellow	LED, Yellow, SMD	Wurth Elektronik	150060YS75000	LED_0603
23	7	D5, D6, D7, D8, D9, D10, D11	30V	Diode, Schottky, 30 V, 0.2 A, SOT-23	ON Semiconductor	BAT54SLT1G	SOT-23
24	1	D13	Red	LED, Red, SMD	Wurth Elektronik	150060RS75000	LED_0603
25	2	D14, D18	80V	Diode, Schottky, 80 V, 0.5 A, SOD-123	Micro Commercial Components	MBR0580-TP	SOD-123
26	1	D15	3V	Diode, Zener, 3 V, 225 mW, SOT-23	ON Semiconductor	MMBZ5225BLT1G	SOT-23
27	1	D19	Blue	LED, Blue, SMD	Wurth Elektronik	150060BS75000	LED_0603
28	1	D21	8.2V	Diode, Zener, 8.2 V, 500 mW, SOD-123	Vishay-Semiconductor	MMSZ4694-V	SOD-123
29	3	FID1, FID2, FID3		Fiducial mark. There is nothing to buy or mount.	N/A	N/A	Fiducial
30	3	H1, H2, H3		Machine Screw, Round, #4-40 x 1/4, Nylon, Philips panhead	B&F Fastener Supply	NY PMS 440 0025 PH	Screw
31	3	H5, H6, H7		Standoff, Hex, 0.5"L #4-40 Nylon	Keystone	1902C	Standoff
32	2	J1, J2		Header, 100mil, 5x2, Tin, TH	Sullins Connector Solutions	PEC05DAAN	Header, 5x2, 100mil, Tin
33	5	J3, J8, J9, J10, J11		Header, 2.54 mm, 2x1, Gold, TH	Wurth Elektronik	61300211121	Header, 2.54mm, 2x1, TH
34	2	J5, J15		Header, 2.54mm, 2x1, Gold, SMT	Wurth Elektronik	61000218321	Header, 2.54mm, 2x1, SMT
35	1	J6		D-Sub-15, 17Pos, TH	Harting	09 66 252 6610	D-Sub-15, 2rows, Female, TH
36	1	J7		Header, 2.54mm, 10x1, Gold, TH	Wurth Elektronik	61301011121	Header, 2.54mm, 10x1, TH
37	2	J12, J16		Header, 2.54 mm, 1x1, Gold, TH	Wurth Elektronik	61300111121	Header, 2.54 mm, 1x1, TH
38	1	J13		WR-DC DC Power Jack, R/A, TH	Wurth Elektronik	694106301002	WR-DC DC Power Jack, R/A, TH
39	2	L1, L2	100uH	Inductor, Shielded Drum Core, Ferrite, 100 µH, 0.52 A, 0.77 ohm, SMD	Wurth Elektronik	74408943101	4.8x3.8x4.8mm
40	2	L4, L5	100uH	Inductor, Shielded Drum Core, Ferrite, 100 µH, 0.3 A, 0.52 ohm, SMD	Wurth Elektronik	744043101	WE-TPC-M2

Table 41. BOM (continued)

ITEM	QTY	DESIGNATOR	VALUE	DESCRIPTION	MANUFACTURER	PARTNUMBER	PACKAGE REFERENCE
41	1	L6	6.8uH	Inductor, Shielded, 6.8 µH, 0.88 A, 0.3682 ohm, SMD	Wurth Elektronik	74438334068	SMD, 2-Leads, Body 3.2x3.2mm
42	6	Q1, Q3, Q4, Q6, Q7, Q8	30V	MOSFET, N/P-CH, 30 V, 1.5 A,	Texas Instruments	CSD17483F4T	
43	1	Q2	-12V	MOSFET, P-CH, -12 V, -2.3 A,	Texas Instruments	CSD23381F4	
44	1	Q5	-20V	MOSFET, P-CH, -20 V, -15 A, SON 3.3x3.3mm	Texas Instruments	CSD25402Q3A	SON 3.3x3.3mm
45	14	R1, R2, R5, R6, R7, R8, R9, R10, R11, R12, R62, R66, R73, R78	10	RES, 10 ohm, 5%, 0.25W, 0603	Vishay-Dale	CRCW060310R0JNEAHP	0603
46	6	R3, R4, R13, R34, R43, R81	560	RES, 560, 5%, 0.063 W, 0402	Vishay-Dale	CRCW0402560RJNED	0402
47	3	R14, R19, R33	100k	RES, 100 k, 5%, 0.063 W, 0402	Vishay-Dale	CRCW0402100KJNED	0402
48	3	R15, R24, R39	51	RES, 51, 5%, 0.063 W, 0402	Vishay-Dale	CRCW040251R0JNED	0402
49	3	R16, R48, R61	4.99k	RES, 4.99 k, 1%, 0.063 W, 0402	Vishay-Dale	CRCW04024K99FKED	0402
50	2	R17, R32	0	RES, 0 ohm, 5%, 0.1W, 0603	Vishay-Dale	CRCW06030000Z0EA	0603
51	7	R18, R21, R31, R69, R70, R71, R72	0	RES, 0, 5%, 0.063 W, 0402	Vishay-Dale	CRCW04020000Z0ED	0402
52	2	R20, R36	150k	RES, 150 k, 5%, 0.063 W, 0402	Vishay-Dale	CRCW0402150KJNED	0402
53	2	R22, R44	240	RES, 240, 5%, 0.1 W, 0603	Vishay-Dale	CRCW0603240RJNEA	0603
54	4	R23, R26, R54, R59	49.9k	RES, 49.9 k, 1%, 0.063 W, 0402	Vishay-Dale	CRCW040249K9FKED	0402
55	1	R27	9.1k	RES, 9.1 k, 5%, 0.063 W, 0402	Vishay-Dale	CRCW04029K10JNED	0402
56	1	R28	3.92k	RES, 3.92 k, 1%, 0.063 W, 0402	Vishay-Dale	CRCW04023K92FKED	0402
57	1	R29	5.11k	RES, 5.11 k, 1%, 0.063 W, 0402	Vishay-Dale	CRCW04025K11FKED	0402
58	1	R30	1.3k	RES, 1.3 k, 5%, 0.063 W, 0402	Vishay-Dale	CRCW04021K30JNED	0402
59	1	R35	12k	RES, 12 k, 5%, 0.063 W, 0402	Vishay-Dale	CRCW040212K0JNED	0402
60	1	R37	26.1k	RES, 26.1 k, 1%, 0.063 W, 0402	Vishay-Dale	CRCW040226K1FKED	0402
61	1	R38	31.6k	RES, 31.6 k, 1%, 0.063 W, 0402	Vishay-Dale	CRCW040231K6FKED	0402
62	1	R40	10.0k	RES, 10.0 k, 1%, 0.063 W, 0402	Vishay-Dale	CRCW040210K0FKED	0402
63	1	R41	51.1	RES, 51.1, 1%, 0.063 W, 0402	Vishay-Dale	CRCW040251R1FKED	0402
64	1	R42	0.1	RES, 0.1, 1%, 0.125 W, 0805	Panasonic	ERJ-6RSFR10V	0805
65	1	R45	1.2k	RES, 1.2 k, 5%, 0.063 W, 0402	Vishay-Dale	CRCW04021K20JNED	0402
66	1	R46	1.15k	RES, 1.15 k, 1%, 0.063 W, 0402	Vishay-Dale	CRCW04021K15FKED	0402
67	1	R47	510	RES, 510, 5%, 0.063 W, 0402	Vishay-Dale	CRCW0402510RJNED	0402

Table 41. BOM (continued)

ITEM	QTY	DESIGNATOR	VALUE	DESCRIPTION	MANUFACTURER	PARTNUMBER	PACKAGE REFERENCE
68	12	R49, R52, R63, R67, R68, R74, R75, R76, R77, R83, R84, R85	10k	RES, 10 k, 5%, 0.063 W, 0402	Vishay-Dale	CRCW040210K0JNED	0402
69	2	R50, R55	6.34k	RES, 6.34 k, 1%, 0.063 W, 0402	Vishay-Dale	CRCW04026K34FKED	0402
70	1	R51	4.7k	RES, 4.7 k, 5%, 0.063 W, 0402	Vishay-Dale	CRCW04024K70JNED	0402
71	1	R53	20k	RES, 20 k, 5%, 0.063 W, 0402	Vishay-Dale	CRCW040220K0JNED	0402
72	2	R56, R79	22	RES, 22, 5%, 0.063 W, 0402	Vishay-Dale	CRCW040222R0JNED	0402
73	1	R57	309k	RES, 309 k, 1%, 0.063 W, 0402	Vishay-Dale	CRCW0402309KFKED	0402
74	1	R58	10k	RES, 10 k, 5%, 0.1 W, 0603	Vishay-Dale	CRCW060310K0JNEA	0603
75	1	R60	23.7k	RES, 23.7 k, 1%, 0.063 W, 0402	Vishay-Dale	CRCW040223K7FKED	0402
76	2	R80, R82	56.2	RES, 56.2, 1%, 0.125 W, 0805	Vishay-Dale	CRCW080556R2FKEA	0805
77	1	R86	8.06k	RES, 8.06 k, 1%, 0.063 W, 0402	Vishay-Dale	CRCW04028K06FKED	0402
78	1	T2	785 uH	Transformers, Gate Drive , 785uH, SMT	Pulse Engineering	PE-68386NL	8.6x2.5x6.7 mm
79	1	U1		Low-Voltage 4-Bit 1-of-2 FET Multiplexer/Demultiplexer, RSV0016A	Texas Instruments	SN74CBTLV3257RSVR	RSV0016A
80	1	U2		Buck Inverting Buck-Boost Step Down Regulator with 3.5 to 60 V Input and 0.8 to 58 V Output, -40 to 150 degC, 10-Pin SON (DRC), Green (RoHS & no Sb/Br)	Texas Instruments	TPS54060ADRCT	DRC0010J
81	1	U3		Wide Input 60-V, 200-mA Synchronous Step-Down DC-DC Converter With Low IQ, DRB0008B	Texas Instruments	TPS54061DRBR	DRB0008B
82	1	U4		2.5 to 18 V Positive Voltage 10A Integrated Hot-Swap Controller, RUV0036A	Texas Instruments	TPS24750RUV	RUV0036A
83	1	U5		Dual Comparator, D0008A	Texas Instruments	LM2903D	D0008A
84	3	U7, U9, U12		3.3V-Supply RS-485 with IEC ESD Protection, D0008A	Texas Instruments	SN65HVD78D	D0008A
85	0	D16	80V	Diode, Schottky, 80 V, 0.5 A, SOD-123	Micro Commercial Components	MBR0580-TP	SOD-123
86	0	R25	100	RES, 100, 5%, 0.063 W, 0402	Vishay-Dale	CRCW0402100RJNED	0402

7.3 PCB Layer Plots

To download the layer plots, see the design files at TIDA-00179.

7.4 PCB Layout Guidelines

Because there are no noise-sensitive circuits in this design, no particular attentions are required in the layout design, except for the power management section for the purpose of the EMI and EMC compliance.

The design of a four-layer PCB with at least one complete ground plane has then been performed.

Layout guidelines can be also found in the datasheets of the TI parts used in the TIDA-00179.

7.4.1 TPS54060A and TPS54061

Bypass the VIN pin to ground with a low-ESR ceramic bypass capacitor with X5R or X7R dielectric.

Minimize the loop area formed by the bypass capacitor connections, the VIN pin, and the anode of the catch diode. The GND pin should be tied directly to the thermal pad under the IC.

Connect the thermal pad to any internal PCB ground planes using multiple vias directly under the IC.

Route the PH pin to the cathode of the catch diode and to the output inductor. Because the PH connection is the switching node, the catch diode and output inductor should be located close to the PH pins, and the area of the PCB conductor minimized to prevent excessive capacitive coupling.

The RT/CLK pin is sensitive to noise, so the RT resistor should be located as close as possible to the IC and routed with minimal lengths of trace. The additional external components can be placed approximately as shown in Figure 64 of the device's datasheet (SLVSB57).

7.4.2 TPS24750

Decoupling capacitors on VCC pin must have minimal trace lengths to the pin and to GND.

Traces to SET and SENSE must be short and run side by side to maximize common-mode rejection. Use Kelvin connections at the points of contact with R_{SENSE}.

High current carrying power path connections should be as short as possible and sized to carry at least twice the full-load current, more if possible.

Minimize connections to IMON pin after the previously described connections have been placed.

To operate at rated power, solder the PowerPad directly to the PC board’s GND plane directly under the device. The PowerPad is at GND potential and can be connected using multiple vias to inner layer GND.

7.4.3 SN65HVD78

Use VCC and ground planes to provide low inductance. Apply 100-nF to 220-nF bypass capacitors as close as possible to the VCC pins of the transceivers (and generally of all the ICs) on the board. Use at least two vias for VCC and ground connections of bypass capacitors and protection devices to minimize effective inductance of the vias.

Use 10-kΩ pullup and pulldown resistors for enable lines to limit noise currents in these lines during transient events. Insert pulse-proof resistors into the A and B bus lines.

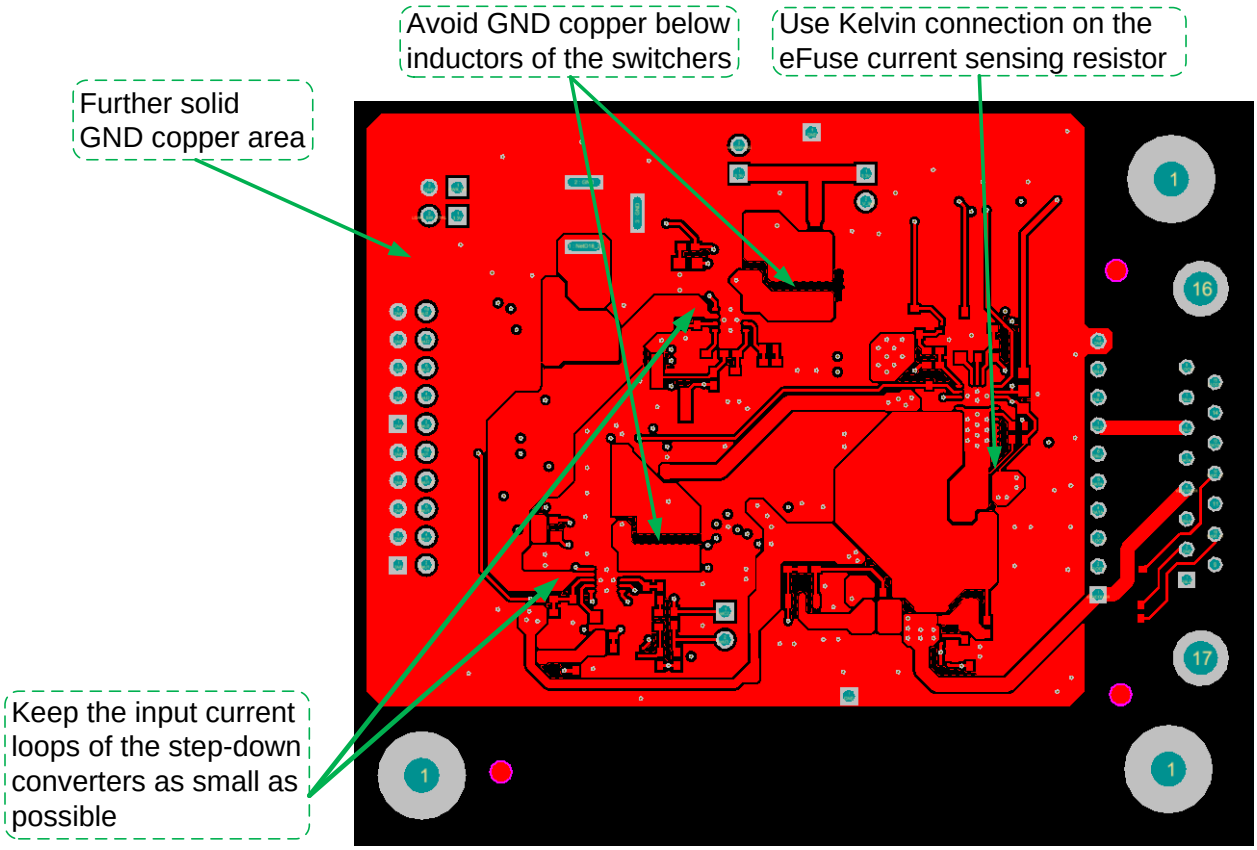


Figure 69. Top Layer

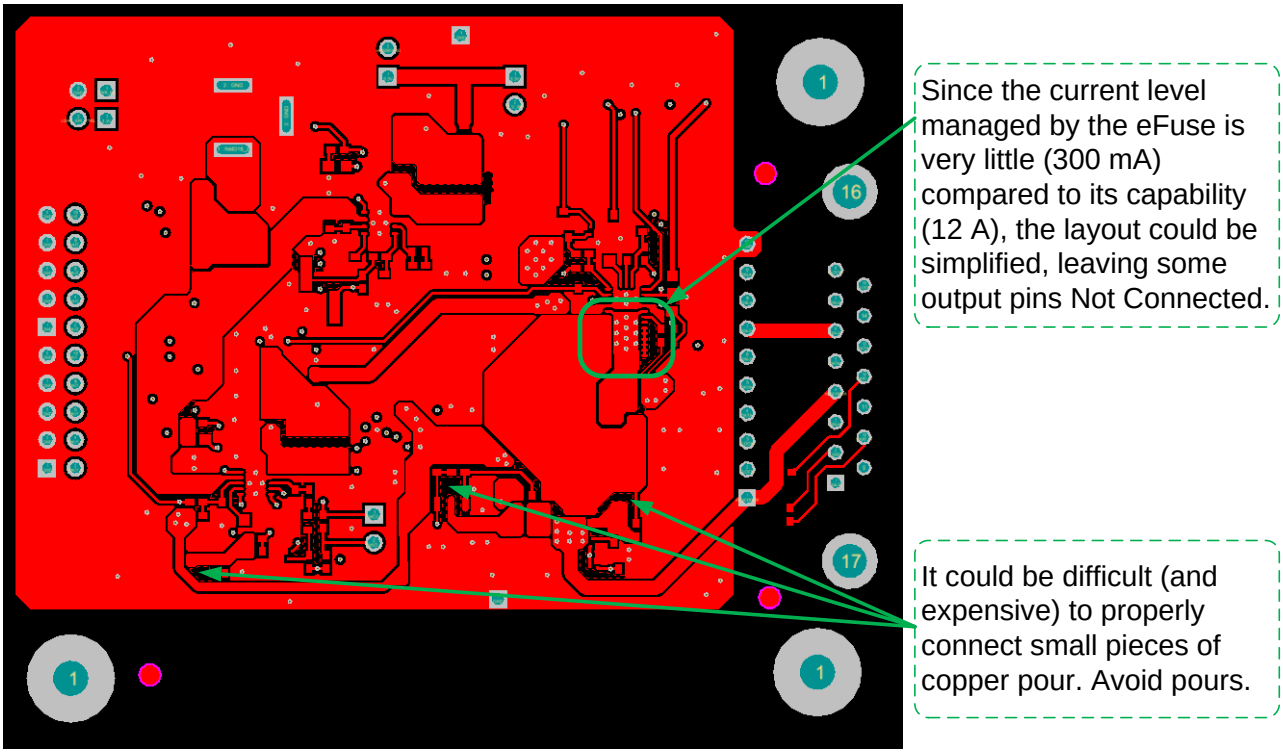


Figure 70. Top Layer—eFuse Layout

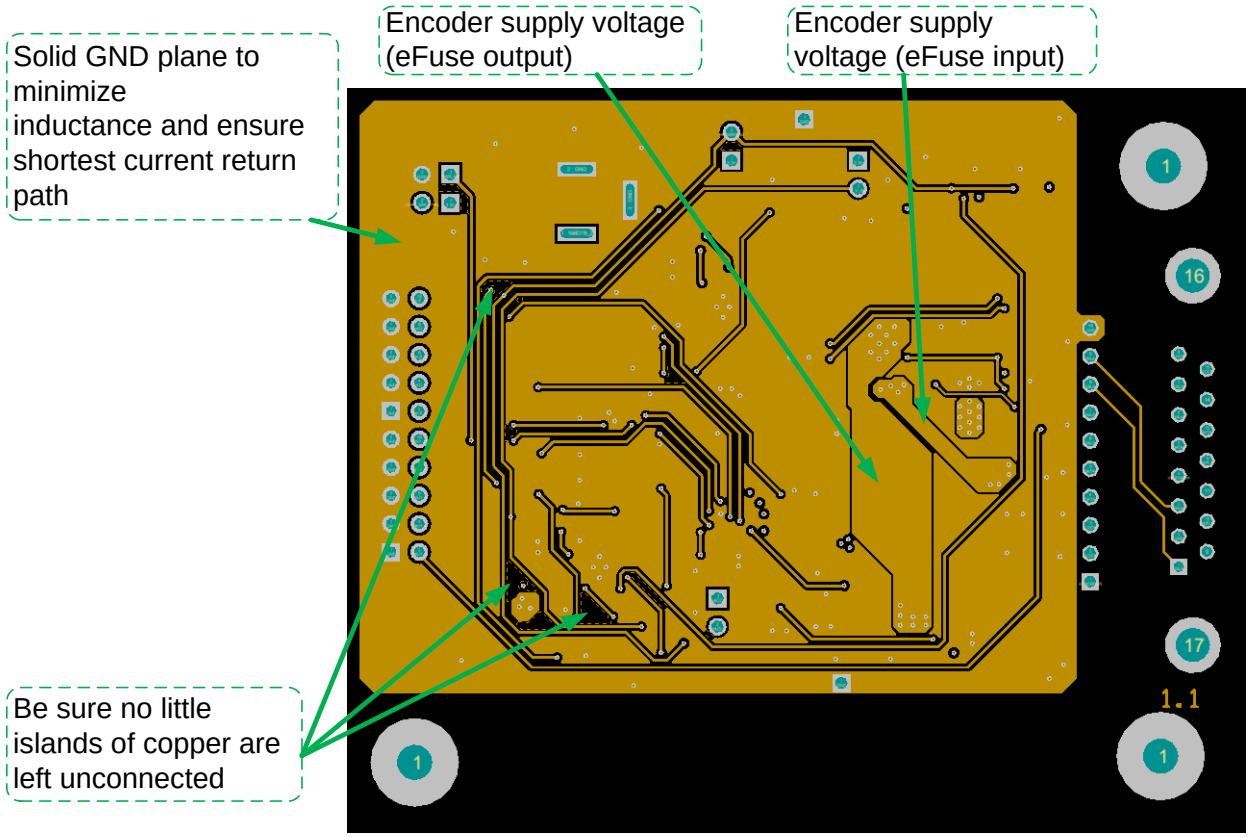


Figure 71. Mid-Layer 1—Power Plane

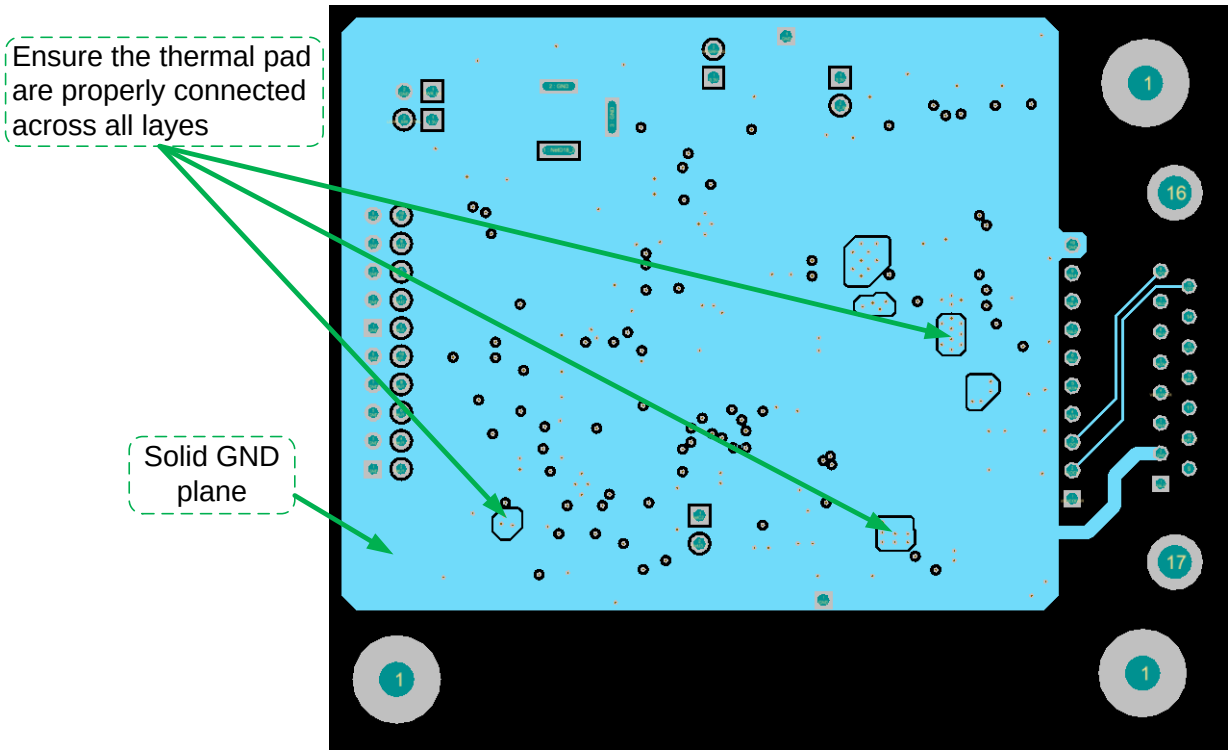


Figure 72. Mid-Layer 2—Power Plane (GND)

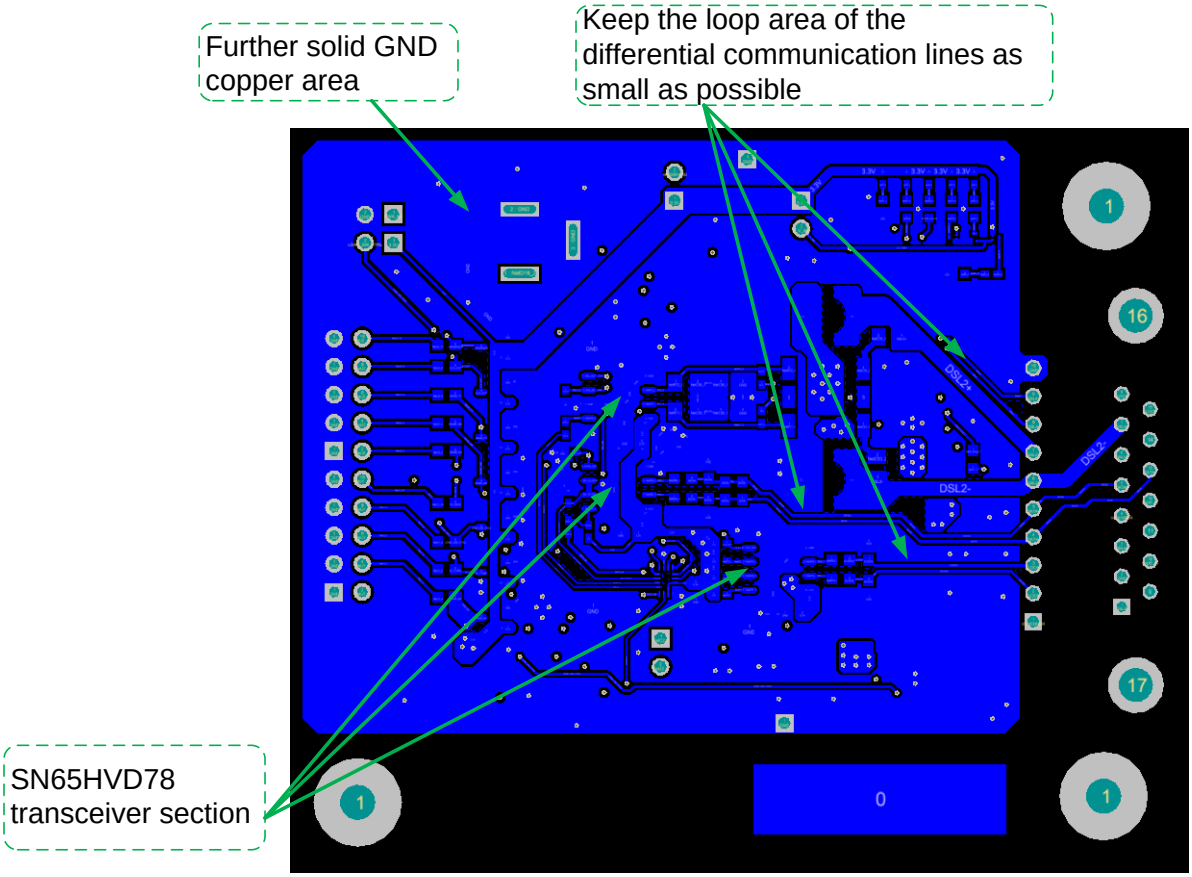


Figure 73. Bottom Layer

7.5 Altium Project

To download the Altium project files, see the design files at TIDA-00179.

7.6 Gerber Files

To download the Gerber files, see the design files at TIDA-00179.

7.7 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-00179.

8 References

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17. IEC, *Amendment 1 - Adjustable speed electrical power drive systems - Part 3: EMC requirements and specific test methods* [IEC 61800-3-am1 ed2.0 (2011-11)].

9 About the Author

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Revision History

Changes from Original (October 2015) to A Revision	Page
• Changed from preview page	1

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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