TI Designs

4- to 20-mA Current Loop Transmitter Reference Design

Design Overview

The TIDA-00648 TI Design is an industry standard 4- to 20-mA current loop transmitter. This design allows the injection of FSK-modulated digital data into the 4- to 20-mA current loop for HART communication. External protection circuitry is deployed in-place for compliance with regulatory IEC61000-4 standards, including EFT, ESD, and surge requirements. EMC compliance to IEC61000-4 is necessary to ensure that the design not only survives, but also performs as intended in a harsh and noisy industrial environment.

Design Resources

TIDA-00648	Tool Folder Containing Design Files
DAC161S997	Product Folder
TPS7A1601	Product Folder
MSP430F5172	Product Folder
TIDA-00459	Tool Folder
TIDA-00245	Tool Folder
TIDA-00349	Tool Folder

TI E2E™ Community

ASK Our E2E Experts

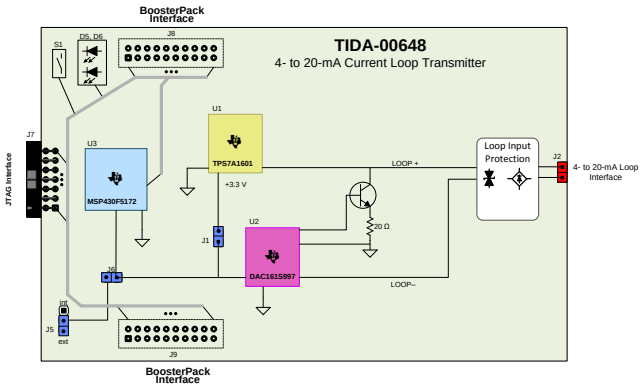
WEBENCH® Calculator Tools

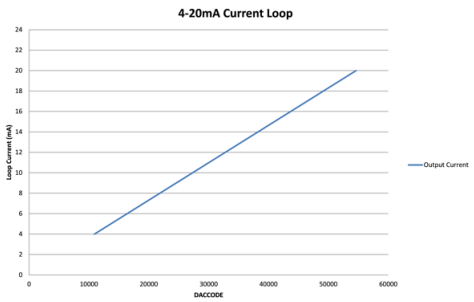
Design Features

- 4- to 20-mA Current-Loop Output Signal
- 8- to 33-V Input
- 16-Bit Resolution
- Loop-Error Detection and Reporting
- Programmable Output-Current Error Levels
- Simple HART Modulator Interfacing
- Reverse Input and Overvoltage Protection
- Designed to Meet IEC 61000 Requirements

Featured Applications

- Factory Automation and Process Control
- Sensors and Field Transmitters Actuator Control
- Actuator Control
- Building Automation
- Portable Instrumentation





1 Key System Specifications

Table 1. Key System Specifications

PARAMETERS	SPECIFICATIONS AND FEATURES
Output signal	Two-wire 4- to 20-mA current loop according to NAMUR NE-43
Power supply voltage range on loop interface terminals	8 V to 33 V
Continuous reverse input voltage	Up to –33-V DC
Compliance voltage	8 V
Supply current consumption	< 3.3 mA (to power all the functional blocks of the transmitter)
Error output currents	Low: 3.375 mA (typical) High: 21.75 mA (typical)
Reverse polarity protection	Continuous
Input current limit	<50 mA
Surge transient Immunity	Designed to meet IEC 61000-4-5: ±1-kV line-line (DM)
Operating temperature	–40°C to +85°C
Interface connector	Two-pin TH terminal block, 6 A, 3.5 mm for loop interface

2 System Description

Monitoring and maintaining process variables at the appropriate levels is extremely critical in industrial automation and process control. A sensor in the industrial environment is either continuously or periodically measuring vital parameters such as temperature, pressure, flow, and so forth. The primary challenge of sensing in industrial environments is conditioning low signal levels in the presence of high noise and high-surge voltage. For industrial process control instruments, analog 4- to 20-mA current loops are commonly used for analog signaling, with 4 mA representing the lowest end of the range and 20 mA the highest. The key advantages of the current loop are that the accuracy of the signal is not affected by voltage drop in the interconnecting wiring and the loop can supply the operating power to the device. Even if significant electrical resistance exists in the line, the current loop transmitter maintains the proper current, up to its maximum voltage capability. Such instruments are used to measure pressure, temperature, level, flow, pH, or other process variables. But a 4- to 20-mA current loop can also be used to control a valve positioner or other output actuator.

This TIDA-00648 reference design comes in a TI BoosterPack™ Plug-in Module to extend the functionality of the designs TI LaunchPad™ Development Kits and add a 4- to 20-mA interface. The design files include schematics, bill of materials (BOM), layer plots, Altium files, Gerber Files, and the TI MSP430™ MCU firmware.

3 Block Diagram

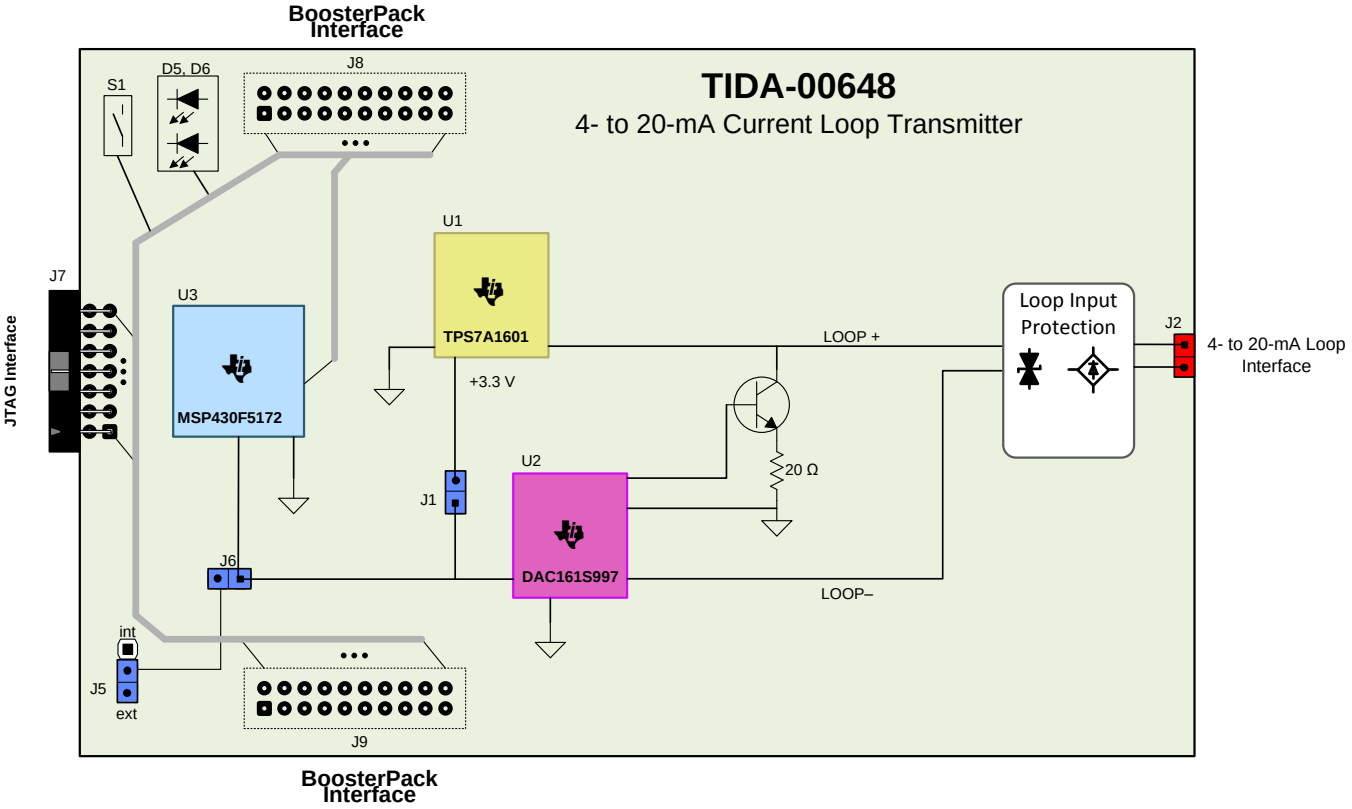


Figure 1. TIDA-00648 System Block Diagram

The goal of this reference design is to focus on the design of a two-wire, loop-powered 4- to 20-mA current loop transmitter that is robust, low-power, precise, and stable in the longterm. The board comes in a BoosterPack form factor and has the following additional features:

- **Loop input protection**:
  This feature protects the design against differential input surge pulses (according to EN 61000-4-5, up to ± 1 kV, 42 Ω), as well as against reverse input voltage (or the reverse connection of the nominal input voltage by miswiring). Surge pulses are clamped by an onboard transient-voltage-suppression (TVS) diode to a safe voltage level below 60 V. Reverse input voltage can be applied continuously. The complete circuitry functions even under reverse input voltage conditions, but the accuracy and other performance parameters experience degradation.
- **Current limiter and circuitry to protect the current sense circuitry inside a loop-powered transmitter**:
  Each sudden increase of the loop input voltage causes a sudden pulse current through the input capacitor of the power circuitry. An example of a sudden increase of the input voltage at the loop input terminals occurs during the initial power-up or during positive differential mode surge pulses. Because the loop current is sensed and controlled by the respective 4- to 20-mA DAC in a connected transmitter circuit, this pulse current flows through the sensitive current shunt inside this DAC. A maximum current rating for the current through this current shunt exists, which requires limiting the current below 50 mA in the case of a DAC161S997. A simple 200-Ω resistor and a dedicated active current source have been implemented for this purpose.

3.1 Highlighted Products

The TIDA-00648 reference design features the following devices:

- DAC161S997
  - 16-bit SPI-programmable DAC for 4- to 20-mA loops
- MSP430F5172
  - MSP430F51x2 ultra-low-power mixed-signal MCU
- TPS7A1601
  - 60-V, 5-µA I_Q, 100-mA, low-dropout voltage regulator

For more information on each of these devices, see the respective product folders at www.ti.com.

3.1.1 DAC161S997

The DAC161S997 is a very-low-power, 16-bit ΣΔ DAC for transmitting an analog output current over an industry standard 4- to 20-mA current loop. The DAC161S997 has a simple four-wire SPI for data transfer and configuration of the DAC functions. To reduce power and component count in compact loop-powered applications, the DAC161S997 contains an internal ultralow-power voltage reference and an internal oscillator. The low power consumption of the DAC161S997 results in additional current being available for the remaining portion of the system. The loop drive of the DAC161S997 interfaces to a HART modulator, allowing the injection of FSK-modulated digital data into the 4- to 20-mA current loop. This combination of specifications and features makes the DAC161S997 ideal for two- and four-wire industrial transmitters. The DAC161S997 is available in a 16-pin 4-mm × 4-mm WQFN package and is specified over the extended industrial temperature range of –40°C to +105°C.

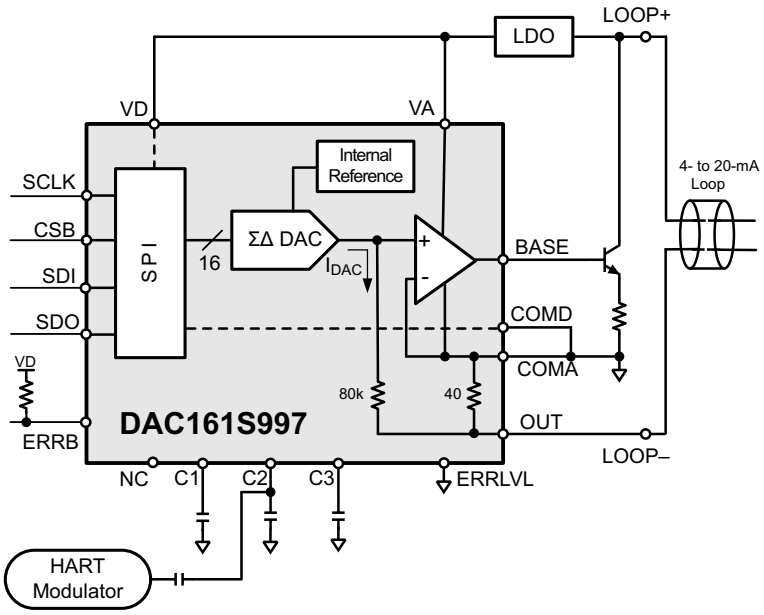


Figure 2. DAC161S997 Block Diagram

Some of the highlighted features of the DAC161S997 are:

- 16-bit resolution
- Very low supply current of 100 µA
- 5 ppmFS/°C gain error
- Pin-programmable power-up condition
- Loop-error detection and reporting

- Programmable output-current error levels
- Simple HART modulator interfacing
- Highly integrated feature set in small footprint WQFN-16 (4- × 4-mm, 0.5-mm pitch)

3.1.2 TPS7A1601

A wide input range is often required in industrial environments to protect large transients from damaging the LDO. The wide-input rating relaxes the design of external protection circuitry and minimizes protection circuitry cost and space. LDOs with a wide-input range safely regulate the output-power supply rail at a desired 3.3 V, even when encountering high voltage transients at the input. These high voltage transients cause high heat; therefore, a proper package must be selected to dissipate heat. An LDO with low quiescent current is the best choice for a 4- to 20-mA loop-powered sensor transmitter. Quiescent current is required to control internal circuitry that calibrates performance. The use of a FET as an internal pass device supports the ultralow 5 µA of quiescent current and a dropout voltage scaling that is almost linear with the output current of the LDO (see Figure 4). The LDO device selected for this application is TPS7A1601, which offers the following features:

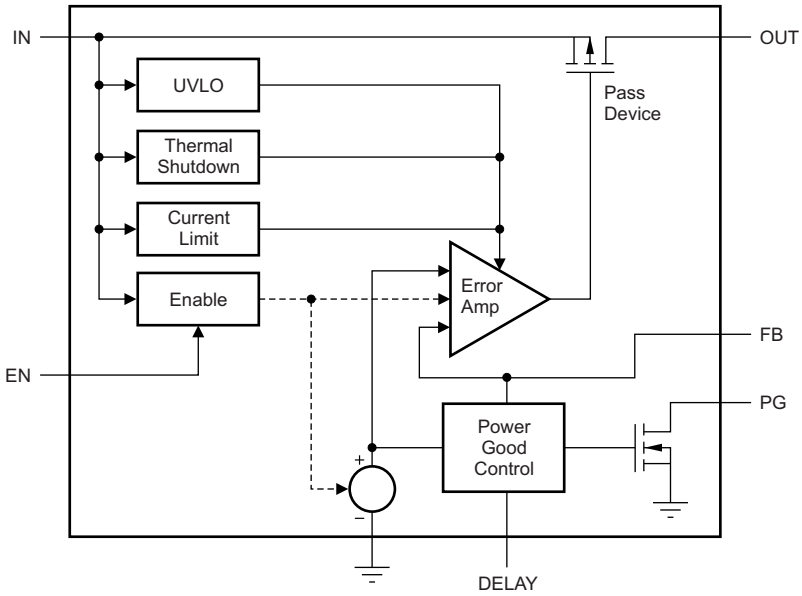


Figure 3. TPS7A1601 Block Diagram

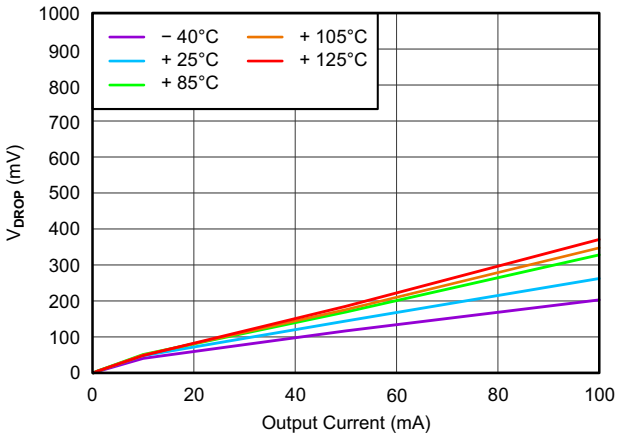


Figure 4. Dropout Voltage Versus Output Current

The LDO device selected for this application is TPS7A1601, which offers the following features:

- Wide input range 3 V to 60 V
- High accuracy — approximately 2%
- Low drop-out voltage — approximately 60 mV at 20 mA
- Power supply rejection ratio (PSRR) of 50 dB at 100 Hz
- Ultralow quiescent current — approximately 5 µA
- Stable with any ceramic capacitor from 2.2 µF to 100 µF
- High thermal performance package

3.1.3 MSP430F5172

The TI MSP430 family of ultralow-power MCUs consists of several devices featuring different sets of peripherals targeted for various applications. The MCU selected for this application is the MSP430F5172 (see Figure 5).

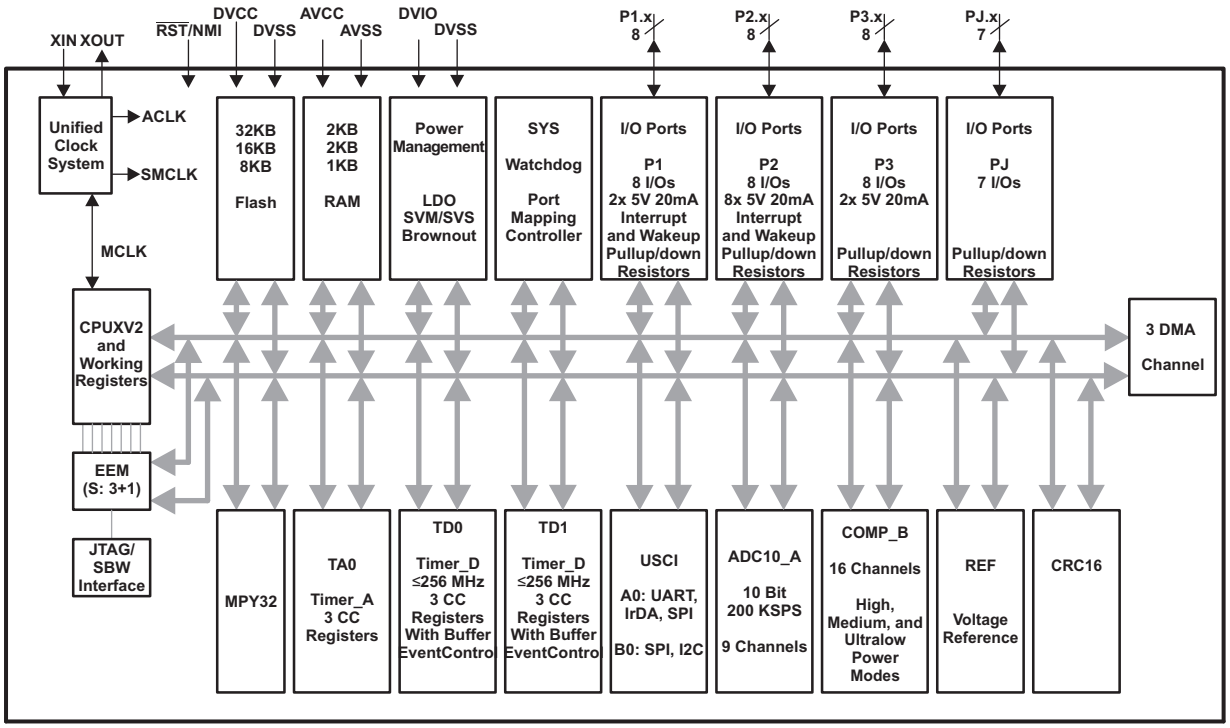


Figure 5. MSP430F51x2 Block Diagram

Some of the highlighted features of the MSP430F5172 are:

- Low supply-voltage range: 3.6 V down to 1.8 V
- Ultralow power consumption
  - Active mode (AM): 180 µA/MHz
  - Standby mode (LPM3 watchdog timer (WDT) mode, 3 V): 1.1 µA
  - Off mode (LPM4 RAM retention, 3 V): 0.9 µA
  - Shutdown mode (LPM4.5, 3 V): 0.25 µA
- Wake up from standby mode in less than 5 µs
- 16-bit reduced instruction set computing (RISC) architecture, extended memory, 40-ns instruction cycle time

- Flexible power-management system
  - Fully integrated LDO with programmable regulated core supply voltage
  - Supply voltage supervision, monitoring, and brownout
- Unified clock system
  - Frequency-locked control loop (FLL) for frequency stabilization
  - Low-power low-frequency internal clock source (VLO)
  - Low-frequency trimmed internal reference source (REFO)
  - 32-KHz crystals (XT1)
  - High-frequency crystals up to 25 MHz (XT1)
- Hardware multiplier supports 32-bit operations
- Three-channel DMA
- Up to twelve 5-V tolerant digital push/pull I/Os with up to 20-mA drive strength
- 16-bit timer TD0 with three capture/compare registers and support of high-resolution mode
- 16-bit timer TD1 with three capture/compare registers and support of high-resolution mode
- 16-bit timer TA0 with three capture/compare registers
- Universal serial communication interfaces (USCIs)
  - USCI_A0 supports:
    - Enhanced UART supports automatic baud-rate detection
    - IrDA encoder and decoder
    - Synchronous SPI
  - USCI_B0 supports:
    - I^2C
    - Synchronous SPI
  - 10-bit 200-ksps ADC
    - Internal reference
    - Sample-and-hold
    - Auto-scan feature
    - Up to eight external channels, two internal channels, including temperature sensor
  - Up to 16-channel on-chip comparator including an ultralow-power mode
  - Serial onboard programming, no external programming voltage required
  - Available in 40-pin QFN (RSB), 38-pin TSSOP (DA), and 40-pin die-sized BGA (YFF) packages

4 System Design Theory

A typical current-loop system basically consists of four components as Figure 6 show (typical current-loop system).

- Sensor (temperature, pressure, and so forth)
- 4- to 20-mA current loop transmitter
- Loop power supply
- Loop receiver (programmable logic controller (PLC))

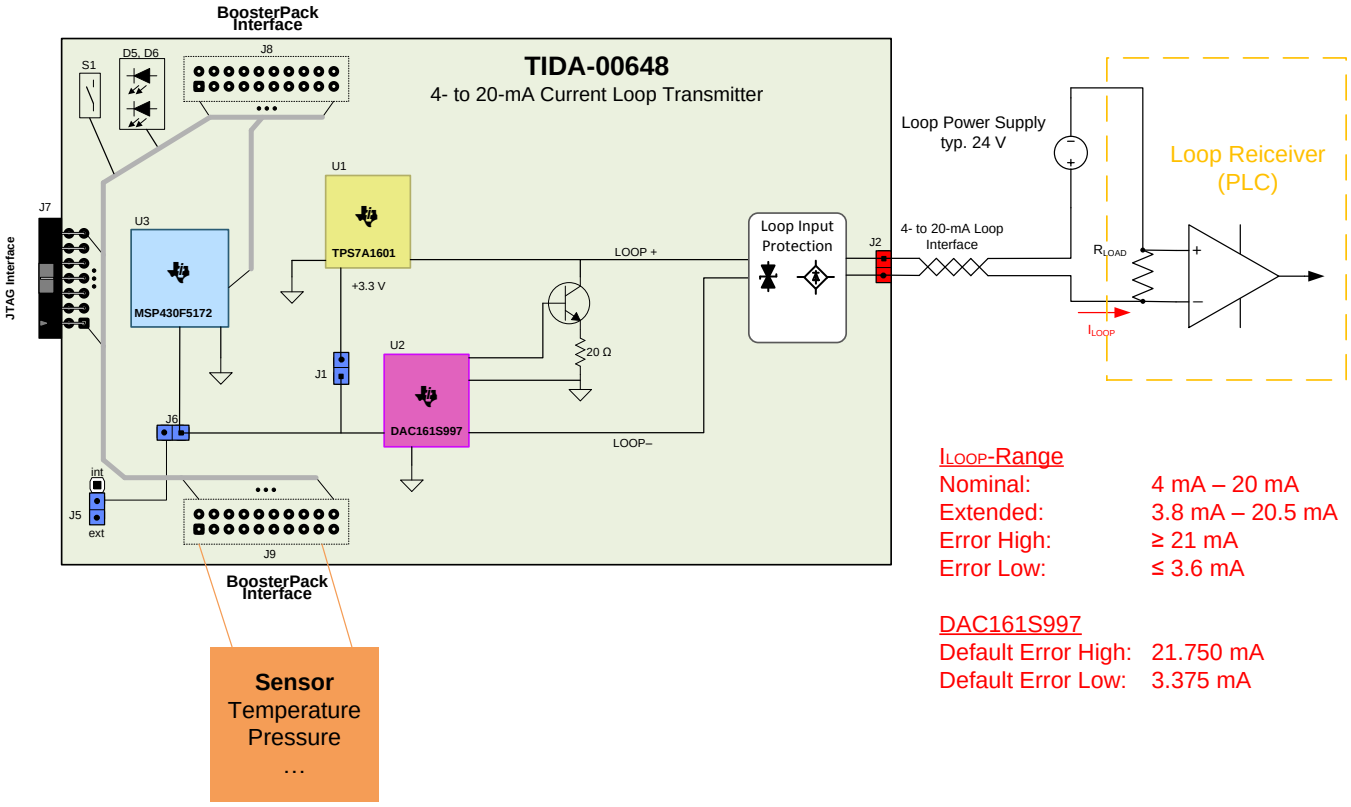


Figure 6. Typical Current-Loop System

A broad range of sensor-specific BoosterPacks are available from Texas Instruments (TI) as well as third parties. Adding sensor functionality to the board is simple using the BoosterPack approach of this TIDA-00648 reference design, which simply entails connecting any of these BoosterPacks.

The sensor converts a physical parameter (for example, temperature) to an equivalent voltage output. By regulating the current supplied by the loop power supply, the transmitter converts the output of the sensor to a proportional 4- to 20-mA DC current. The zero-value process variable is represented by 4 mA. The full scale process variable is represented by 20 mA. Therefore, a 16-mA span is available to represent the entire measurement information range. The current returns back to the power supply after flowing through a precision load resistor of the loop receiver. Because no system can directly measure the current, the receiver first converts the 4- to 20-mA loop current into a voltage that is easily measured by the analog input module of the PLC system and processed further.

Additional values or value ranges for I_{LOOP} are, for example, specified in the NAMUR recommendation [5], extending the working range from 3.8 mA to 20.5 mA to support activities like adjustment, calibration, and the detection of range overflow. Furthermore, loop currents below 3.6 mA or above 21 mA are recommended for use for the purpose of failure detection.

Choosing current over voltage as an information carrier is generally preferential for the following reasons:

- Current loops have inherent immunity against noise.
- Transmitting current signal over long distances does produce the voltage drop (also known as voltage loss or loop drop) across the loop because of wiring resistance. However, the magnitude of signaling is not affected when the loop power supply is high enough to compensate for these losses and still meets the compliance voltage requirement at the transmitter for the transmitter's proper operation.

Basic circuit theory shows that current is the same along the signal line, which means the same amount of current supplied by loop power supply always returns back to the source.

- The residual 4-mA current at zero-point allows easy detection of a wire-break condition. The residual 4-mA current at zero point also allows the transmitter to be powered up if the current requirement is within 4 mA. The current exceeds 20 mA for a short-circuit condition; therefore, current loops are self-monitoring.
- Choosing current over voltage minimizes the cost and simplifies the installation because signal current and transmitter power-supply current share the same pair of conductors.
- Choosing current over voltage minimizes the cost and simplifies the installation because signal current and transmitter power-supply current share the same pair of conductors.

The complete system is powered by the loop power supply, typically at a 24-V level. This power source forms together with the loop receiver (often a programmable logic controller (PLC)) and with the two-wire loop powered transmitter, the current loop. A two-wire cable is sufficient for the electrical connection.

Those two wires are used for powering the transmitter as well as transmitting the signal by controlling the loop current I_{LOOP}, which equals the total current consumption of the transmitter.

On the loop receiver side of the system, the loop current causes a voltage drop across the load resistance R_{LOAD} inside the receiver. This voltage drop is usually amplified and then converted into a digital signal for further processing inside the receiver. Typical receivers are, for example, PLCs.

Typical load resistance levels range from some tens of Ω to some hundreds of Ω. With an assumed R_{LOAD} of 500 Ω, which is exemplary, the voltage drop across this resistor changes from 2 V to 10 V for loop currents of 4 mA to 20 mA.

NOTE: This voltage drop reduces the voltage at the loop-input terminals J2. The higher the loop current, the less voltage is available to power the transmitter.

The minimal voltage level required to ensure that the operation of the transmitter is within its performance specification (at the loop-input terminal J2) is called the compliance voltage.

4.1 DAC Theory of Operation

The DAC converts the 16-bit input code in the DACCODE registers to an equivalent current output. The ΣΔ DAC output is a current pulse, which is then filtered by a third-order, resistor-capacitor circuit (RC), low-pass filter and boosted to produce the loop current (I_{LOOP}) at the device OUT pin.

Figure 7 shows the principle of operation of the DAC161S997 in the loop-powered transmitter (circuit details are omitted for clarity).

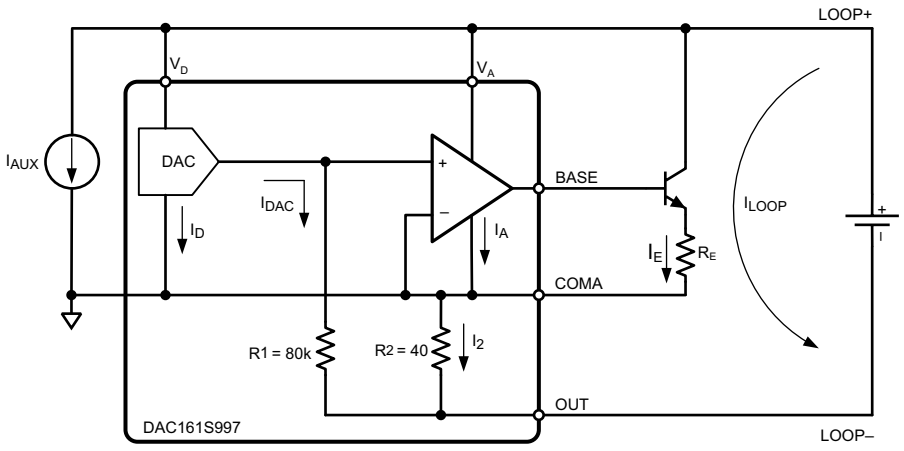


Figure 7. Loop-Powered Transmitter

In Figure 7, I_D and I_A represent supply (quiescent) currents of the internal digital and analog blocks. I_{AUX} represents the supply (quiescent) current of companion devices present in the system, such as the voltage regulator and the digital interface. Because both the control loop formed by the amplifier and the bipolar transistor force the voltage across R1 and R2 to be equal, under normal conditions, the I_{LOOP} is dependent only on I_{DAC} through the following relationship (see Equation 1).

$$I_{LOOP} = (1 + R1 / R2) \times I_{DAC}$$

where

- $I_{DAC} = f \times \text{DACCODE}$ (1)

Although I_{LOOP} has a number of component currents, $I_{LOOP} = I_{DAC} + I_D + I_A + I_{AUX} + I_E$, only I_E is regulated by the loop to maintain the relationship shown in Equation 1. Because only the magnitude of I_E is controlled, not the direction, there is a lower limit to I_{LOOP}. This limit is dependent on the fixed components (I_A and I_D) and on system implementation through I_{AUX}.

Equation 2 expresses the output current that is sourced by the OUT pin of the device.

$$I_{LOOP} = 24 \text{ mA} (\text{DACCODE} / 2^{16}) \quad (2)$$

The valid DACCODE range is the full 16-bit code space (0x0000 to 0xFFFF), resulting in the I_{DAC} range of 0 to approximately 12 µA. However, this range does not result in the I_{LOOP} range of 0 mA to 24 mA. The maximum output current sourced out of the OUT pin (I_{LOOP}) is 24 mA. The minimum output current is dependent on the system implementation. The minimum output current is the sum of the supply currents of the DAC161S997 internal blocks (I_A and I_D) and companion devices present in the system, I_{AUX}. The last component current, I_E, is theoretically controlled down to 0; however, because of the stability considerations of the control loop, TI advises not allowing the I_E to drop below 200 µA.

The graph in Figure 8 shows the DC transfer characteristic of the 4- to 20-mA transmitter, including the minimum current limits. The minimum current limit for the loop-powered transmitter is typically around 400 µA ($I_D + I_A + I_{AUX} + I_E$). The typical value for I_D is 57 µA and for the typical value for I_A is 43 µA. The value for I_E depends on the bipolar junction transistor (BJT) device used.

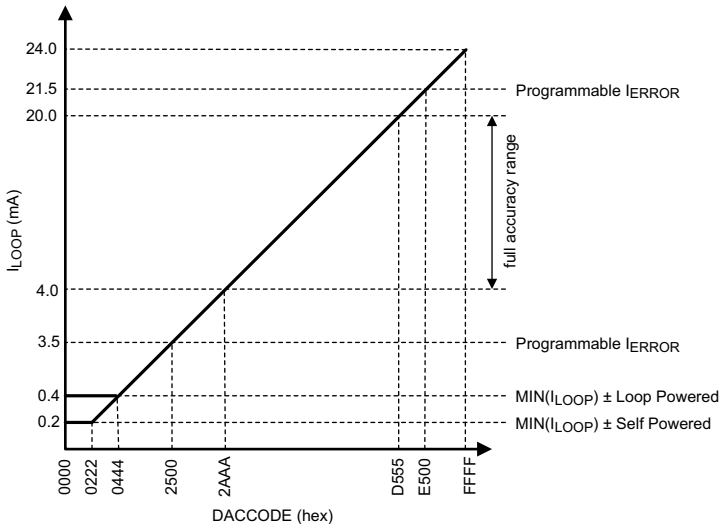


Figure 8. DAC-DC Transfer Function

The DAC161S997 cannot directly interface to the typical 4– to 20-mA loop because of the excessive loop supply voltage. The loop interface has to provide the means of stepping down the loop supply to 3.3 V. The TPS7A1601 device in this design is used to step down the loop voltage supply to 3.3 V and power the DAC161S997 and MSP430F5172. The user must consider that the quiescent current of the regulator has a direct effect on the minimum achievable I_{LOOP}.

The second component of the loop interface is the external NPN transistor (BJT). This device is part of the control circuit that regulates the output current of the transmitter (I_{LOOP}). Because the BJT operates over the wide current range, spanning at least 4 mA to 20 mA, degenerating the emitter is necessary to stabilize the transconductance of the transistor (g_m). The degeneration resistor of 20 Ω is suggested in typical applications. See Figure 7 for circuit details.

The NPN BJT must not be replaced with an N-channel field-effect transistor (FET) for the following reasons: discrete FETs typically have high threshold voltages (VT), in the order of 1.5 V to 2 V, which is beyond the BASE output maximum range; discrete FETs present higher load capacitance, which may degrade system stability margins; and the BASE output relies on the base current of the BJT for biasing.

4.2 Power Design

The TPS7A16xx family of ultralow-power voltage regulators offers the benefit of ultralow quiescent current, high-input voltage, and miniaturized, high-thermal performance packaging. The TPS7A16xx family of LDOs allow a maximum input voltage of 60 V, which makes these LDOs ideal for use in industrial applications where high-voltage transients are present. The TPS7A1601 has an adjustable output voltage range from 1.194 V to 20 V. The nominal output of the device is set by two external resistors R4 and R5, as Figure 9 shows. To set the LDO output voltage, V_{CC} = 3.3 V, the resistor divider components are calculated using Equation 3.

$$R4 = R5 \times \left(\frac{V_{CC}}{V_{REF}} - 1 \right) \quad (3)$$

where

- V_{REF} = LDO internal reference voltage = 1.193 V (typical)
- The selected values are R4 = 2.0 MΩ and R5 = 1.13 MΩ

Be attentive of board contamination when using high-value resistors. Board contaminants can significantly affect voltage accuracy. If board cleaning measures cannot be ensured, consider using a fixed voltage version of the TPS7A16 device or using resistors in the order of hundreds or tens of kΩ.

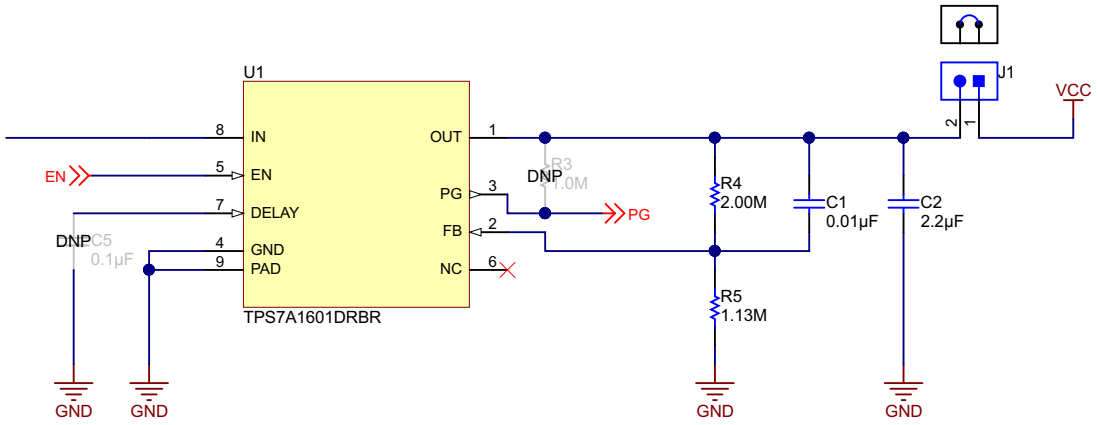


Figure 9. LDO Circuit With Feedback for Adjustable Output

Equation 4 calculates the maximum power dissipation within the LDO:

$$P_D = (V_{IN\_LDO} - V_{CC}) \times I_Q \quad (4)$$

Assume a worst-case scenario where the entire maximum loop power supply voltage, $V_{SUPPLY\ (MAX)}$ = 33 V, appears across the LDO input. The maximum allowed I_Q = 3.3 mA.

$$P_D = (33\ V - 3.3) \times 3.3\ mA = 98.01\ mW \quad (5)$$

The junction-to-ambient thermal resistance, θ_{JA}, of the TPS7A1601 device is 44.5°C/W.

For safe operation: $\theta_{JA} \times P_D + T_{A\ (MAX)}$.

The maximum junction temperature before the TPS7A1601 device shuts down is 170°C. From Equation 5, the worst-case junction temperature of the TPS7A1601 device is approximately 90°C, assuming an ambient temperature of 85°C. Therefore, a sufficient thermal-operating margin is available with the TPS7A1601 device, even accounting for the worse-case power dissipation.

4.3 Protection

4.3.1 Protection for IEC61000-4

The input overvoltage protection of this design protects all blocks and components of the transmitter that can be considered to have a more-or-less direct connection to the loop.

The nominal maximum input voltage expected is provided either by dedicated modules of the PLC or by a separate (DIN-rail) power supply. Possible overvoltage events are mainly transients and overvoltage pulses, which can be caused by the following events:

- Supply voltage overshoot during the power up of the power supply
- The presence of coupling and crosstalk between the loop cable and adjacent cables with large voltage or current transients on these adjacent cables
- Surge, burst, or ESD pulses leading to differential mode voltages (such pulses are used, for example, in EMC compliance testing during the approval procedure of the complete transmitter)

Out of these transients, the most critical pulse (according to the EN 61000-4-5 standard) is the 8/20-µs surge pulse coupled through a total resistance of 42 Ω and through a coupling capacitor of 0.5 µF differentially into the loop input. This power design was created with the intention of handling this critical surge pulse.

A bidirectional TVS diode (D3) and a ceramic capacitor (C3) are used to clamp any overvoltage transient on the loop input terminal J2 to a safe voltage level that is independent of the transient voltages polarity. This overvoltage clamping provides a safe voltage level to the BJT controlled by the 4- to 20-mA DAC inside the transmitter electronics.

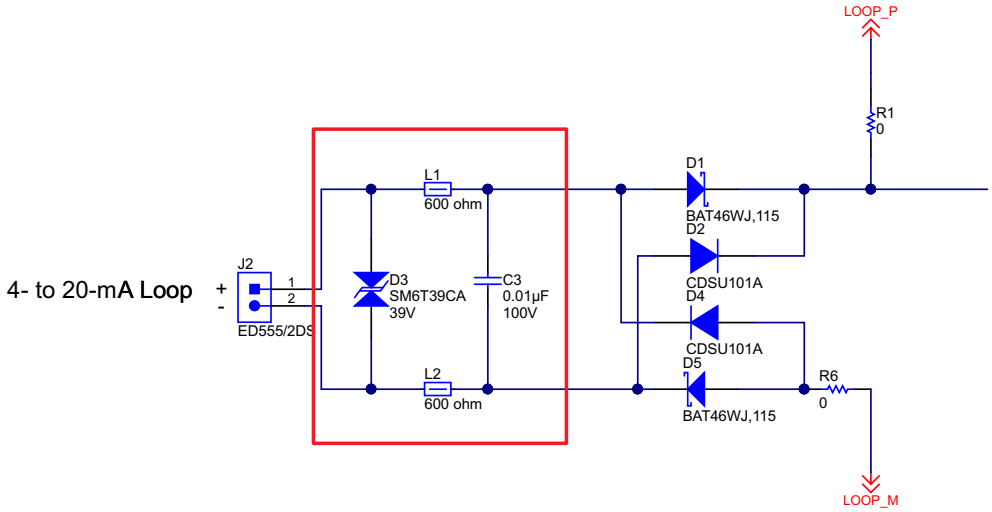


Figure 10. Input Overvoltage Protection

4.3.1.1 TVS Diode Selection D3

To choose the TVS appropriately for this design, the following requirements must be satisfied:

1. The TVS stand-off voltage V_{RM}, the voltage where the TVS does not conduct, must be higher than the maximum nominal loop-input voltage to prevent the TVS from conducting during normal operation. For most projects and applications, the condition *not conduct* can be considered to be fulfilled if the leakage current I_{RM} of the TVS at the given V_{RM} is less than 100 µA. However, the leakage current inside the protection block is not seen by the DAC at all, but adds to the loop current seen by the loop receiver, which causes an error. Therefore, for this design, a leakage current much less than 3 µA was targeted. Because the leakage currents usually grow with increased temperature, the I_{RM} specification of the TVS must be given not only at the maximum nominal loop-input voltage, but also at the maximum operating temperature (85°C) of the design.
2. The TVS peak current and peak pulse power specifications must be higher than the surge current and pulse power under the design-specific conditions. Most of the TVS diode manufacturers specify the device with respect to a 10/1000-µs double-exponential test pulse. However, the pulse used for surge test according to EN 61000-4-5 is an 8/20-µs pulse. Ideally, TVS manufacturers provide the specification for this shorter pulse, as well. If the specification is not provided, the *Peak-Pulse Power Versus Pulse Time* graph must be used, which shows how the peak-pulse power of the TVS is affected by shorter or longer pulse duration. For shorter pulse widths, the TVS can withstand a higher-peak pulse power. Locate the *Peak-Pulse Power Versus Pulse Time* graph in the respective TVS diode datasheet.
3. When the TVS conducts and becomes low impedance to clamp the voltage at a safe level, the TVS clamping voltage (V_{CL}) at the specific peak pulse current (I_{PP}) and at the maximum operating temperature of the design must be lower than the maximum recommended operating voltage of the circuits connected to that voltage. The affected parts in this design are:
   - TPS7A1601 – U1
   - BJT controlled by the 4- to 20-mA DAC
   - Diodes in the reverse-polarity protection
   - Input capacitor C3

The selected TVS is an SM6T39CA, which fulfils the following three requirements:

1. I_{RM} (max): 1 µA at V_{RM} = 33.3 V and at 85°C—this is much less than the required 3 µA
   I_{RM} (max): 0.2 µA at V_{RM} = 33.3 V and at 25°C
2. The data sheet specifications for the 8/20-µs pulse are as follows:
   I_{PP} (max): 57 A
   P_{PP} (max): 4 kW
   Both parameters are much higher than the application specific values:
   I_{PP}: is approximately 22.6 A
3. V_{CL} (MAX at 100°C) is approximately 55 V

4.3.1.2 Selection of Input Capacitor C3

To bypass the higher-frequency transient voltages caused by burst or ESD, a 10-nF ceramic X7R capacitor was selected. With the 100-V DC voltage rating of the capacitor, the device matches the clamping voltage of the TVS with plenty of margin.

4.3.2 Reverse Input Protection

The reverse input voltage protection enables a transmitter to withstand operation at reverse input voltage conditions on the loop input (J2). Examples of such conditions are as follows:

- Interchange of the two wires at the loop input terminals due to miswiring (interchange can last continuously)
- Negative differential-mode surge pulses (can occur due to lightning events or during testing by applying the negative 1-kV surge pulse, according to the EN 61000-4-5 standard)

The positive and negative input terminals are protected separately by protection diodes. Schottky diodes are preferred, due to their low forward voltage (VF). The huge, high-temperature reverse currents (IRs) of the Schottky diodes (hundreds of µA at > 85°C) do not matter if the diodes are forward biased.

One-way rectifiers, or half-wave rectifiers, can provide sufficient protection. One example is a circuit consisting of the diodes D1 and D5 (see Figure 11) that does not contain diodes D2 and D4. The disadvantage of half-wave rectifiers is that the rectifier diodes must withstand the sum of the rectifiers' output voltage (usually stored in the bypass capacitor on the input of the following block or blocks), plus the absolute value of an applied negative voltage. Using this design as an example, the sum of 33 V plus 60 V is close to 100 V.

In the case of using separate diodes for the positive and negative loop-input terminals, this voltage can divide equally. In real cases, this equal splitting cannot be guaranteed because of the wide spread of reverse currents between the two diodes, especially when Schottky diodes are used at high temperatures.

Another disadvantage of the half-wave rectifier configuration is the missing current, which normally keeps the blocks following the protection circuit alive during any negative input-voltage events. Therefore, a better solution is a full-wave rectifier configuration, which provides a perfect voltage clamp across the rectifier diodes to the absolute value of the input voltage. The full-wave rectifier configuration also ensures a continuous current delivery to the following blocks, even during reverse input-voltage events. Nevertheless, if the rectifier bridge is built using Schottky diodes only, the hundreds of µA of reverse current (IR) of these diodes add to the 1-µA IR of the TVS diode (D3). Therefore, the total error on the loop current measured by the loop receiver is no longer acceptable.

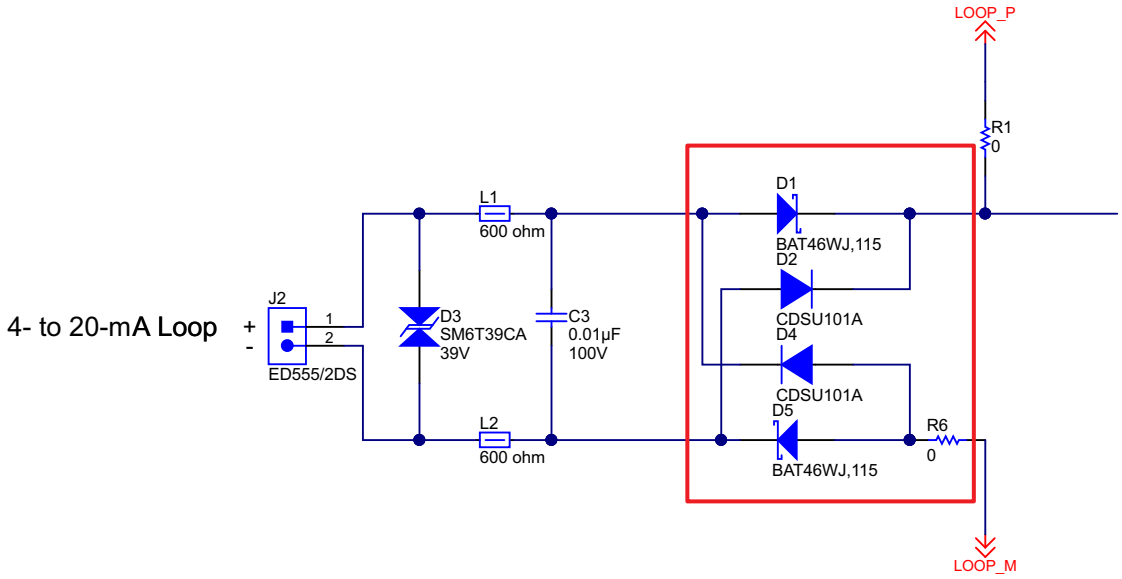


Figure 11. Input Reverse Protection

By using the mix of Schottky diodes and silicon diodes that the preceding Figure 11, the advantages of both diode types can be preserved. The two forward-biased Schottky diodes D1 and D5 cause a total worst-case FV drop of only 880 mV at 3.3 mA and –40°C. The two silicon diodes D2 and D4 prevent D1 and D5 from being stressed with more than 60 V during miswiring events or negative-differential surge pulses.

D2 and D4 are reverse biased, but add only 1 µA of additional reverse current IR at 85°C on the 1-µA IR of the TVS diode and the resulting 2-µA IR is within the design limit of 3 µA.

Even when the loop input voltage is applied in reverse direction on J2, the output of the protection circuitry provides a voltage with the correct polarity to the following blocks. In this situation, the silicon diodes D2 and D4 are now forward-biased; however, the total FV drop of those two diodes is now in the worst-case situation (almost 1.9 V), which is more than twice the total drop caused by the Schottky diodes (almost 900 mV total). The two Schottky diodes D1 and D5 are reverse-biased and as a whole contribute an additional 500-µA reverse current to the total leakage current of the protection circuitry.

The transmitter continues to work even with reverse loop-input voltage polarity; however, the transmitter is no longer capable of matching the accuracy specification of the transmitter. Nevertheless, one clear advantage is that the transmitter electronics do not lose power during negative transient events. This advantage means that the transmitter returns back to the full, typical performance after the transient without any time delay that a required restart of the transmitter's internal electronics requires.

4.3.3 Current Limiter and Circuitry to Protect Current-Sensing Circuitry

As Figure 12 shows, a dedicated circuit block is responsible for reducing any inrush or surge current. The main concern here is to protect the 40-Ω current sense resistor inside the DAC161S997. Inrush and surge currents are caused by sudden increase in the voltage applied to the loop input terminals. The inrush or surge current charges C4 from the voltage that C4 previously holds to the same voltage level as the input terminals. This charge can happen during the following events:

- During initial power-up – This occurrence is especially true when the loop power supply does not have a set, dedicated low-current limit.
- During sudden voltage step of a maximum 33 V (maximum input voltage)
- During 1-kV differential surge – This event is clamped by TVS diode D3 to approximately 60 V, which results in a voltage step of 52 V. These events occur under the assumption that the voltage on the loop input terminals is at the minimum V_{IN} of 8 V before the 1-kV surge.

The 200-Ω resistor (R2) serves as the passive type of current limiter. The active current limiter (which consists of Q2, Q3, and R20 to R22), provides an easy way to limit the current to a value programmable by R21. The active current limiter can be disabled (shorted) by populating R23.

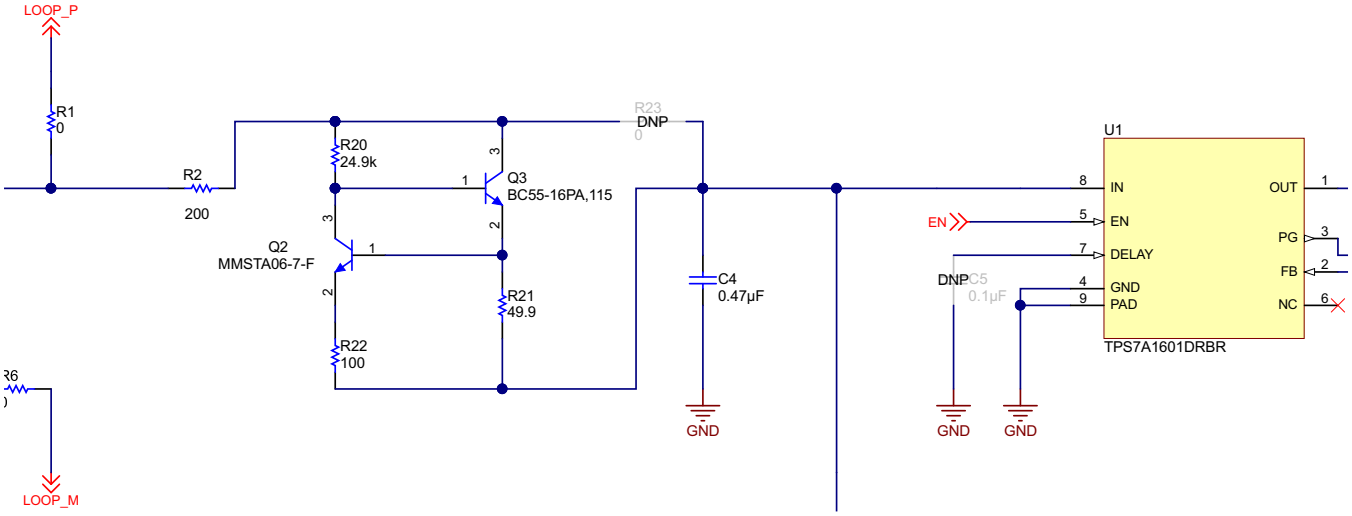


Figure 12. Current Limiter and Sense Resistor Protection

The main path for the current flow is controlled by Q3 in the following Figure 13. The calculation in Equation 6 provides the relation between the main currents:

$$I_{OUT} = I_{IN} + I_{R21} + I_{R22} \quad (6)$$

- The influence of Q2 and R22 on the current flow is negligible if the difference in voltage between V_{IN} and V_{OUT} (designated as $V_{IN} – V_{OUT}$) is less than 2.5 V.
- In this range of differences less than 2.5 V, the output current is completely provided by Q3 through R21. R20, R21, and the DC current gain of Q3 determine the value of I_{OUT}. R20 is biasing Q3 with the base current IB_{Q3}. For a $V_{IN} – V_{OUT}$ of 2.5 V, the I_{OUT} is in the range of 9 mA.
- For voltage differences larger than 2.5 V, Q2 activates and finally tries to keep the voltage across R21 at the sum of its base-emitter voltage V_{BE} and the voltage drop across R22.
- For a $V_{IN} – V_{OUT}$ from 3 V to 40 V, the I_{OUT} rises from 10 mA to slightly more than 15 mA (see Figure 14).
- R22 stabilizes the circuitry against temperature changes.

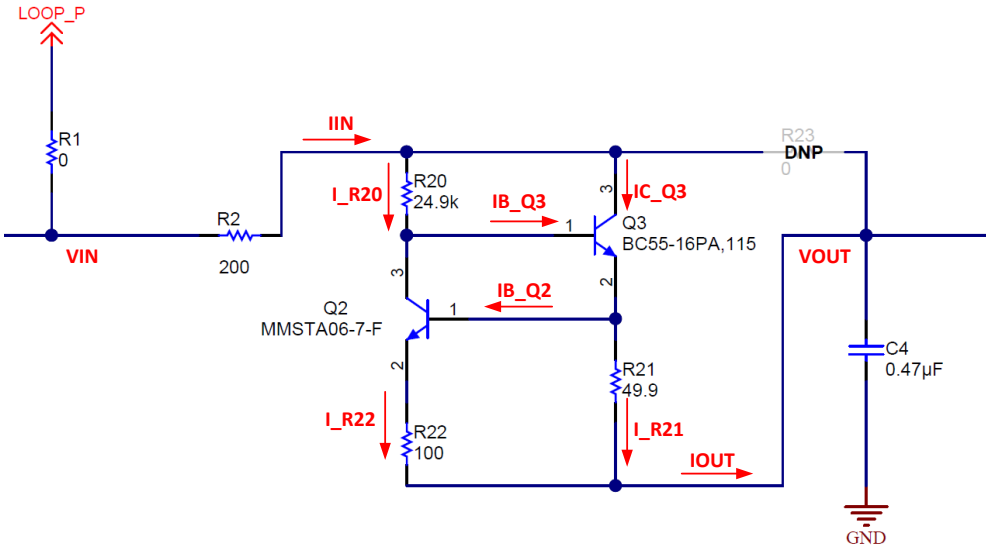


Figure 13. Active Current Limiter—Schematics and Operation

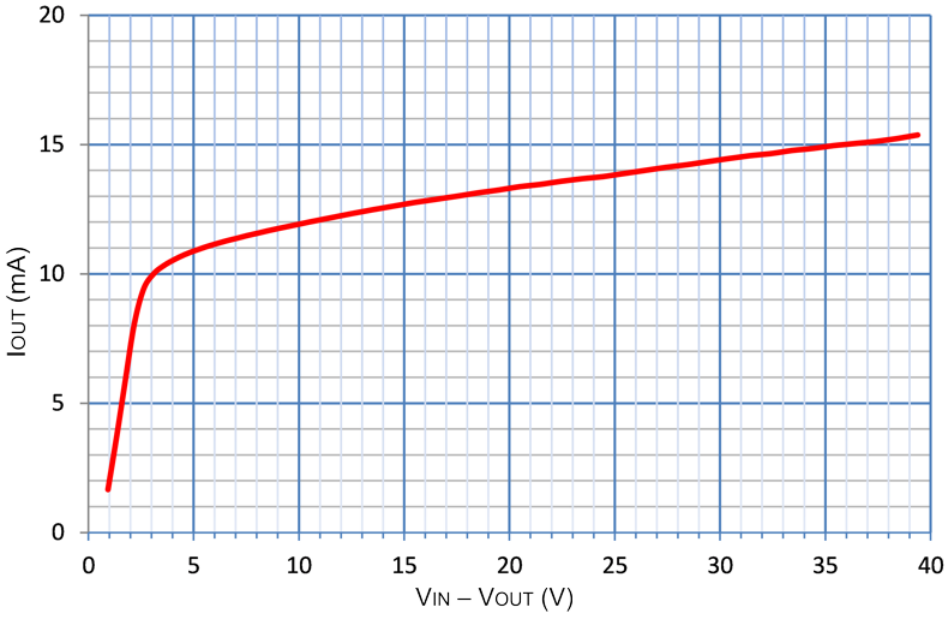


Figure 14. Active Current Limiter Characteristic—I_{OUT} Versus $V_{IN} - V_{OUT}$

5 Getting Started Hardware

5.1 Headers and Jumper Locations

Figure 15 shows the default jumper settings on the TIDA-00648 board.

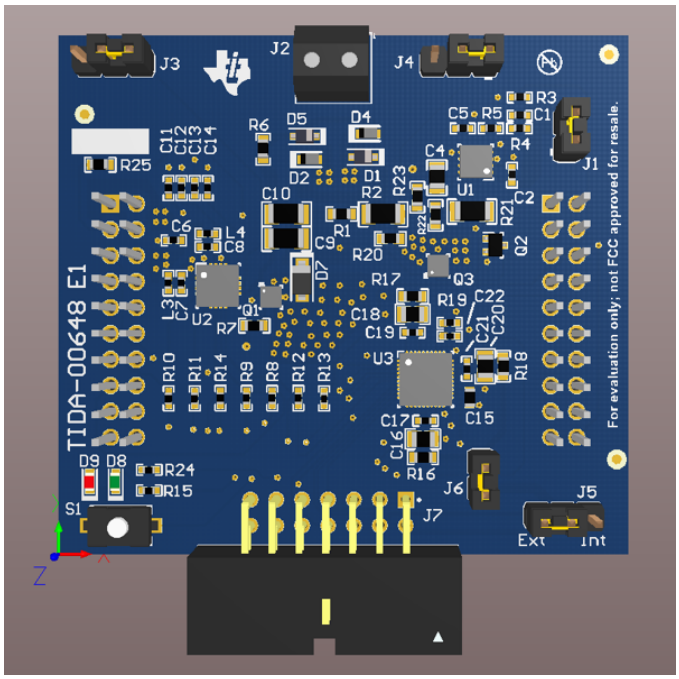


Figure 15. TIDA-00648 Board

Table 2 shows the different functions of the headers.

Table 2. Header Functions

HEADERS	DESCRIPTION
J1	J1 can be used to measure the current into the complete electronics of the transmitter.
J2	J2 is the connection for the 4- to 20-mA current loop.
J3	J3 sets the output current level at power up and under error conditions.
J4	J4 turns the TPS7A1601 on or off. If pin 1 and pin 2 are connected, the regulator is enabled; if pin 2 and pin 3 are connected, the regulator is off.
J5	If power from the TPS7A1601 device is used during debugging, ensure that pin 2 and pin 3 on jumper J5 are connected. If no local power source exists and the power from the debugger interface is used, ensure that pin 1 and pin 2 on jumper J5 are connected.
J6	J6 can be used to measure the current if the board is powered from the MSP-FET debugger.
J7	J7 is the JTAG and UART backchannel connector.
J8	J8 is the BoosterPack interface.
J9	J9 is the BoosterPack interface.

5.2 Power Options

The TPS7A1601 device supplies 3.3 V to the MSP430F5172 if a voltage in the range of 8 V to 33 V is supplied to the 4- to 20-mA loop. Normally, the DAC161S997 and the MSP430F5172 are powered from this 3.3 V. If this local 3.3-V supply from the TPS7A1601 device is used during debugging, ensure that pin 2 and pin 3 on jumper J5 are connected. If no local power source exists and the power from the debugger interface (MSP-FET) is used, ensure that pin 1 and pin 2 on jumper J5 are connected (see Figure 16). If the MSP-FET tool is used for powering the board, the TPS7A1601 device must also be disconnected by removing the jumper J1.

5.3 UART Backchannel

The UART backchannel function is implemented and supported with the MSP-FET tool. This UART backchannel can be used to communicate with the TIDA-00648 design. Figure 16 shows a schematic of the JTAG interface and UART backchannel.

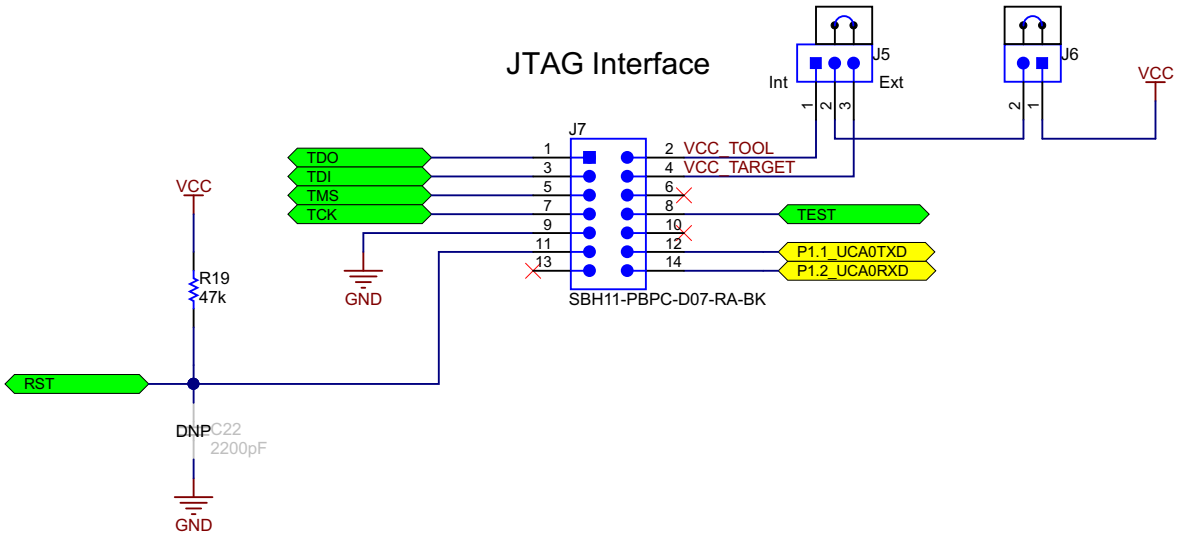


Figure 16. JTAG Interface and UART Backchannel

6 Getting Started Firmware

To download the software files for this reference design, see the link at TIDA-00648.

6.1 Software Setup

1. Install the TI Code Composer Studio™ (CCS) software before connecting the MSP-FET to the PC. While CCS installs, the USB drivers also install automatically. Be sure to use the latest CCS version; otherwise, the USB drivers may not be able to recognize the MSP-FET.
2. Connect the MSP-FET to a USB port on the PC with the provided USB cable.
3. The following procedure applies when using a Windows® operating system:
   (a) After connecting to the PC, the MSP-FET is recognized automatically because the USB device driver has already been installed, along with the integrated development environment (IDE).
   (b) If the driver has not been installed, the Found New Hardware wizard starts. Follow the instructions and point the wizard to the driver files.
   (c) The default installation pathway for CCS is *C:\ti\ccsv6\ccs_base\emulation\drivers\msp430\USB_CDC*.
4. After connecting to a PC, the MSP-FET performs a self-test. If the self-test passes successfully, the green LED remains on.
5. If an external power supply is used during debug operations, ensure that pin 2 and pin 3 are connected on jumper J5. If the user requires powering from the MSP-FET debugger interface because no external power connection exists, ensure that pin 1 and pin 2 are connected on jumper J5. If the MSP-FET tool is used for powering the board, the TPS7A1601 device must also be disconnected by removing the jumper J1.
6. Connect the MSP-FET with the 14-conductor cable to the JTAG connector J7 on the TIDA-00648 board.
7. Import the CCS project (*TIDA-00648_firmware.zip*) into CCS.
8. Compile and download the firmware to the MSP430F5172 device on the TIDA-00648 board.

6.2 Demo Software

Every time the S1 button is pressed, the output of the DAC increases by 1 mA, between 4 mA and 24 mA.

The output value of the DAC161S997 can be set over the UART. A UART backchannel function is implemented and supported for the MSP-FET tool. This UART backchannel can be used to communicate with the TIDA-00648 design. Sending a character ‘R’ resets the DAC161S997 output value to 0x0000. If a character ‘U’ is sent, the output value of the DAC161S997 is incremented by 1. The UART baud rate is 115200 baud.

6.3 Software Function Documentation

The *DAC161.c* file contains standard command and control operations for the DAC161S997 over SPI. Functions exist to setup, configure, and control the DAC161S997.

*void DAC161_Write_Regs (unsigned short *writeValues, unsigned char startReg, unsigned char lengthBytes)*

Description: This function executes a write register command to the DAC161S997. This function can be used to update one or more registers on the DAC161S997. No error checking is performed, so it is the responsibility of the user to make sure that they do not attempt to write past the end of the DAC161S997 registers.
Parameters:
**writeValues* – Pointer to the list of 8-bit register values to place in the DAC161S997
startReg – Address of the first register to write
lengthBytes – Number of registers to write

*void DAC161_Read_Regs (unsigned char *readValues, unsigned char startReg, unsigned char lengthBytes)*

Description: This function executes a read register command to the DAC161S997 and return the resultant data. This function can be used to read one or more registers from the DAC161S997. No error checking is performed, so it is the responsibility of the user to make sure that they do not attempt to read past the end of the DAC161S997 registers.

Parameters:
**readValues* – Pointer to the list of 8-bit register values to place in the DAC161S997
startReg – Address of the first register to read
lengthBytes – Number of registers to read

void Setup_DAC161 (unsigned short errConfig, unsigned short errLow_uA, unsigned short errHigh_uA)

Description: This function configures the DAC161S997.
Parameters:
errConfig – Error configuration for the DAC161S997
errLow_uA – Output level (mA) for a low error
lerrHigh_uA – Output level (mA) for a high error

void DAC161_Reset (void)

Description: This function sends an NOP command to the DAC161S997 on the SPI bus. The DAC161S997 detects a timeout and moves into an error state if it does not receive regular commands for the SPI master. This command can be used to notify the DAC161S997 that the system is still operational, but no change to the DAC161S997 is desired.
Parameters: None

void DAC161_Set_Out_Value_uA (unsigned long uAmps)

Description: The DAC161S997 is designed to be used in a 4- to 20-mA system. This function sets the desired output current.
Parameters: *uAmps* – Value in µA to output from the DAC161S997

void DAC161_Set_Out_Value (unsigned short value)

Description: This function sets the desired output of the DAC161S997 in a 16-bit hex value
Parameters: *value* – 16-bit hex value to output from the DAC161S997

unsigned char DAC161_Read_Status (void)

Description: This function returns the current value in the status register of the DAC161S997.
Parameters: None
Returns: DAC161S997 Status (DAC161_FERR_STS, DAC161_SPI_TIMEOUT_ERR, DAC161_LOOP_STS, DAC161_CURR_LOOP_STS)

void USCIB0_setupMasterSPI(void)

Description: This function initializes the USCI_B0 module for the SPI master.
Parameters: None

*void USCIB0_SPI_write (unsigned char *outData, unsigned char *inData, unsigned char length) unsigned char USCIB0_SPI_writeByte (unsigned char data)*

Description: This function performs an SPI communication sequence to read and write data on the SPI bus.
Parameters:
outData – Pointer to an array with the data that is to be written on the SPI bus
inData – Pointer to an array to place the data returned from the slave device (one byte for every byte sent, even the command byte)
length – Number of bytes to send and receive

7 Test Setup

A primary goal of the design is to avoid any negative impact from the protection circuitry on the total system performance. The term “system performance” relates especially to the accuracy of the loop current control. The basis for this accuracy is actually an accurate sensing of the loop current. Leakage currents (IR), which do not pass the 40-Ω current sense resistor inside the DAC161S997, are critical for this accuracy. The leakage current IR inside the protection block is not seen by the DA161S997 at all, but adds to the loop current seen by the loop receiver, which causes an error.

For the test setup, the backchannel UART of the MSP-FET tool was used to communicate with the MSP430F5172 device and set the different DAC output values (see Figure 17). The output of the 4- to 20-mA loop interface (see Figure 18) was recorded with an 8½ digits multimeter.

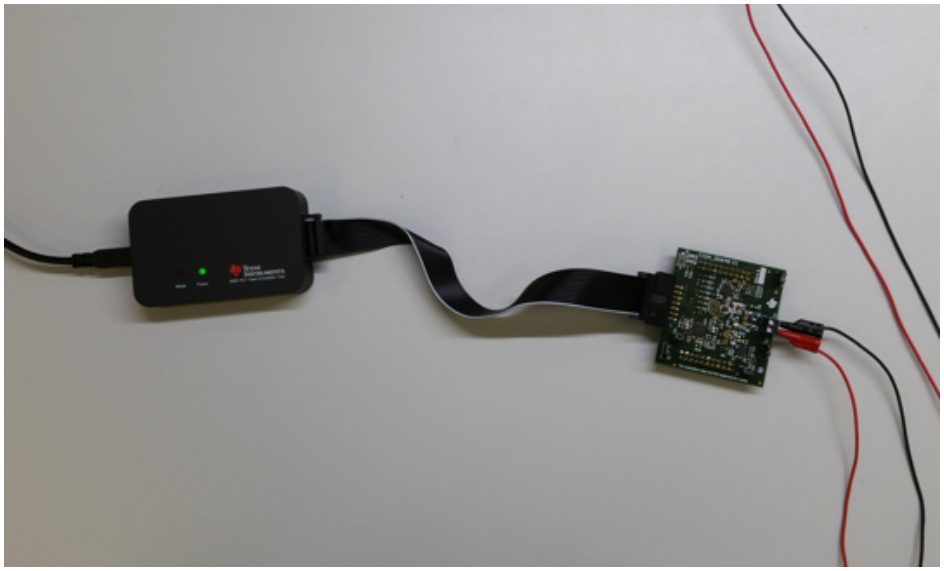


Figure 17. Test Setup

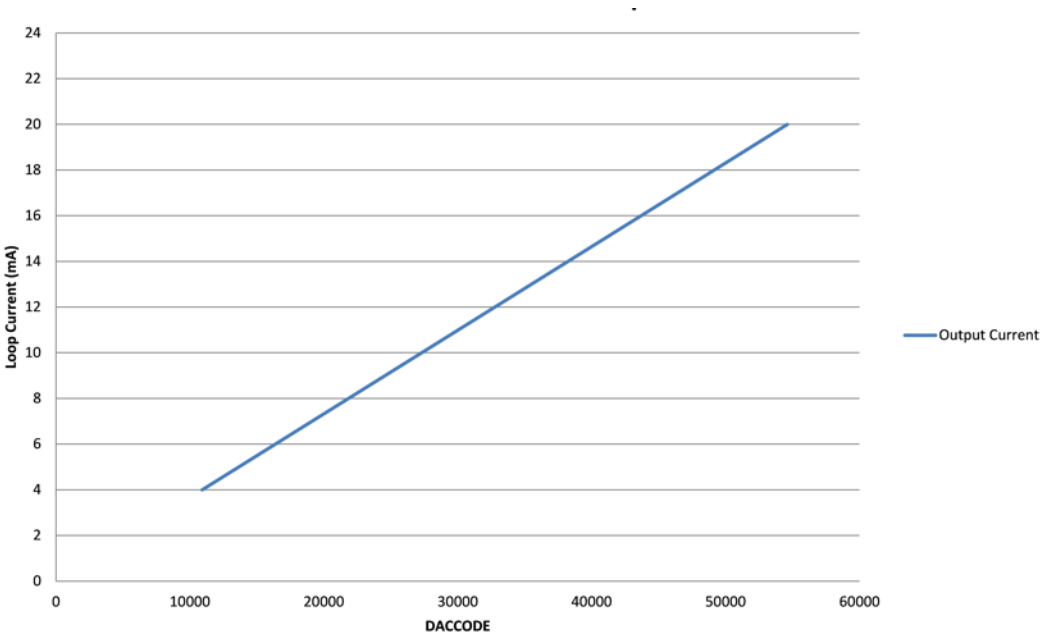


Figure 18. 4- to 20-mA Current Loop

8 Test Data

8.1 Loop Voltage Influence and DAC Noise Error

For the loop voltage influence test, the voltage was set to 8 V, 24 V, and 33 V and the corresponding loop current change was recorded. The DAC output was programmed for a fixed 4-mA output current for this measurement. 50 measurements were taken at each voltage setting. The total deviation of the loop current across the loop voltage without gain or offset calibration is visible in Figure 19.

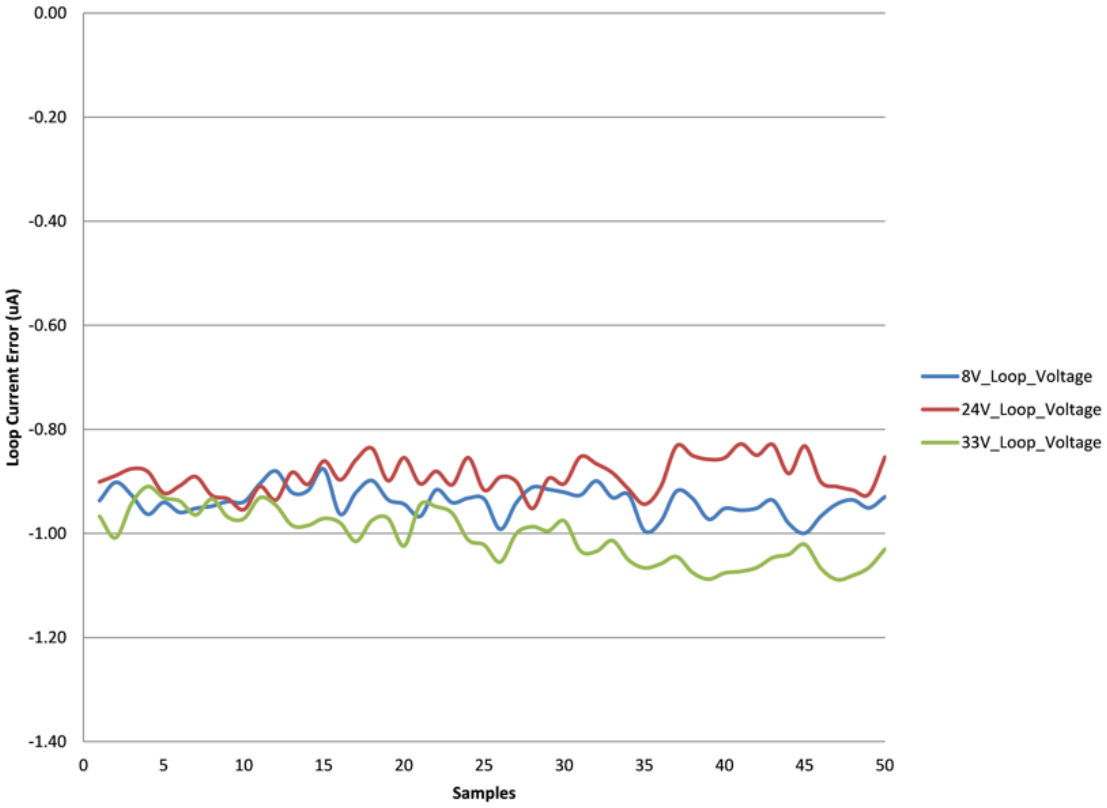


Figure 19. Loop Voltage Influence and DAC Noise Error

8.2 Loop Current Output Error

To perform the DAC error characterization, the MSP430F5172 device was programmed to generate the output loop current from 4 mA to 20 mA. The output current was increased by one DACCODE for every instance that a character 'U' was received on the UART backchannel. The output loop current was measured using an 8½ digits multimeter. Figure 20 shows the loop current output error. To increase the accuracy, the offset and gain can be calibrated in the MSP430F5172 software.

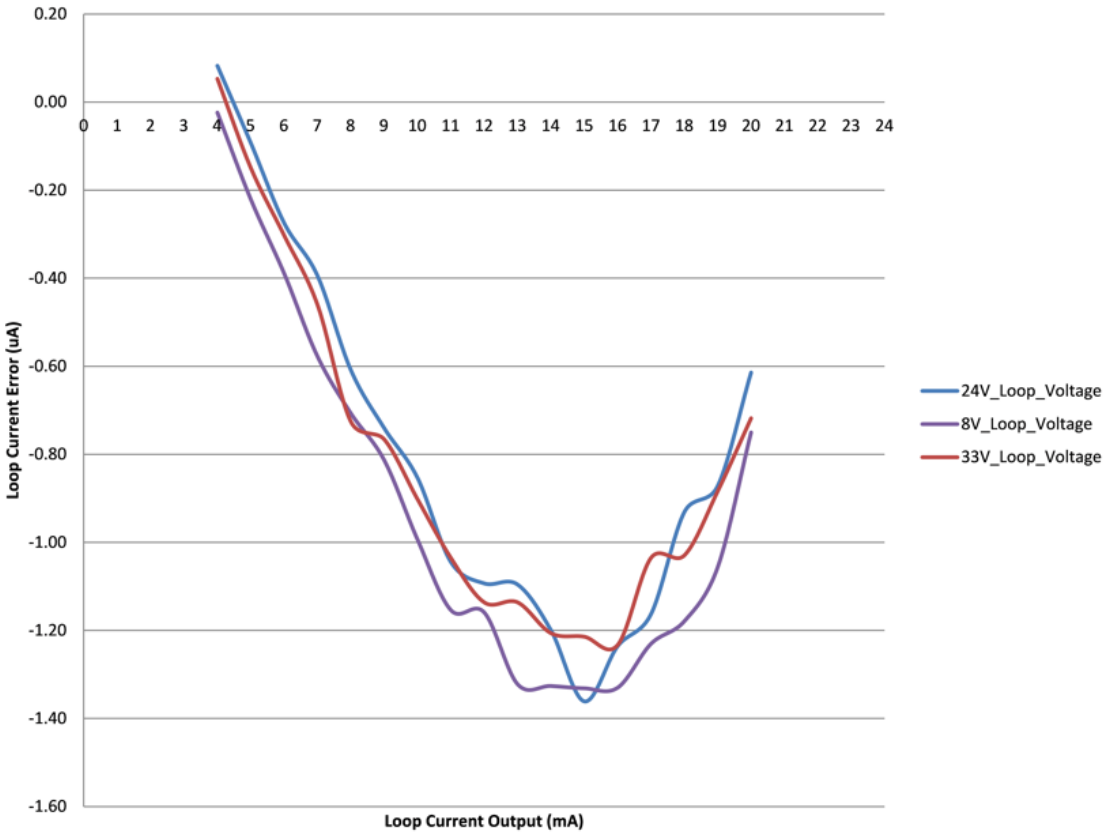


Figure 20. Loop Current Output Error

9 Design Files

9.1 Schematics

To download the schematics for each board, see the design files at TIDA-00648.

9.2 Bill of Materials

To download the bill of materials (BOM) for each board, see the design files at TIDA-00648.

9.3 PCB Layout Recommendations

The TIDA-00648 board has the form factor of a BoosterPack. TI BoosterPack™ Plug-in Modules help to unlock the full potential of LaunchPad-based projects. These innovative tools plug in to the header pins on the LaunchPad and allow the user to explore different applications that TI MCUs enable. To create a BoosterPack for specific needs, use the resources at http://www.ti.com/ww/en/launchpad/byob.html to create BoosterPack design files, obtain support from the community, and take an idea from concept, to PCB, and then product in a few easy steps.

9.3.1 Layout Prints

To download the layout prints for each board, see the design files at TIDA-00648.

9.4 Altium Project

To download the Altium project files for each board, see the design files at TIDA-00648.

9.5 Gerber Files

To download the Gerber files for each board, see the design files at TIDA-00648.

9.6 Assembly Drawings

To download the assembly drawings files for each board, see the design files at TIDA-00648.

10 Software Files

To download the software files for this reference design, see the design files at TIDA-00648.

11 References

1. Texas Instruments, *DAC161S997 SPI 16-Bit Precision DAC for 4-20 mA Loops*, DAC161S997 Data Sheet (SNAS621)
2. Texas Instruments, *60V, 5-µA I_Q, 100-mA, Low-Dropout Voltage Regulator with Enable and Power-Good*, TPS7A16 Data Sheet SBVS171
3. Texas Instruments, *MSP430F51x2 Mixed-Signal Microcontrollers*, MSP430F5x72 Data Sheet, SLAS619
4. Texas Instruments, *MSP430F51x2 Mixed Signal Microcontroller*, MSP430F5x72 User's Guide, SLAU208
5. NAMUR, NAMUR Recommendation NE 43: *Standardization of the Signal Level for the Failure Information of Digital Transmitters*, February 2003, (Worksheets)

12 About the Author

THOMAS SCHNEIDER is a Systems Engineer at Texas Instruments where he is responsible for developing reference design solutions for the industrial segment. Thomas brings to this role his wide experience in TI microcontrollers, especially MSP430. Thomas earned his Dipl.-Ing. (Univ.) degree in Electrical Engineering from the Technical University Munich (TUM) in Munich, Germany.

JÜRGEN SCHNEIDER is a systems engineer at Texas Instruments where he is responsible for developing TI-Designs for the industrial automation segment. He holds a Dipl.-Ing. (FH) degree in Industrial Electronics and has worked 13 years as a design engineer for semiconductor manufacturing equipment, telemetry systems, and electro-medical devices before joining TI in 1999. Jürgen has worked with TI as an analog field specialist, FAE, and systems engineer for power solutions. He presents at technical conferences and seminars and has been one of the presenters of the industry-wide known TI Power Supply Design Seminar for multiple years. Jürgen also has the distinguishment of being elected as a Member, Group Technical Staff.

IMPORTANT NOTICE FOR TI REFERENCE DESIGNS

Texas Instruments Incorporated ("TI") reference designs are solely intended to assist designers (“Buyers”) who are developing systems that incorporate TI semiconductor products (also referred to herein as “components”). Buyer understands and agrees that Buyer remains responsible for using its independent analysis, evaluation and judgment in designing Buyer’s systems and products.

TI reference designs have been created using standard laboratory conditions and engineering practices. **TI has not conducted any testing other than that specifically described in the published documentation for a particular reference design.** TI may make corrections, enhancements, improvements and other changes to its reference designs.

Buyers are authorized to use TI reference designs with the TI component(s) identified in each particular reference design and to modify the reference design in the development of their end products. HOWEVER, NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY THIRD PARTY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT, IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI REFERENCE DESIGNS ARE PROVIDED "AS IS". TI MAKES NO WARRANTIES OR REPRESENTATIONS WITH REGARD TO THE REFERENCE DESIGNS OR USE OF THE REFERENCE DESIGNS, EXPRESS, IMPLIED OR STATUTORY, INCLUDING ACCURACY OR COMPLETENESS. TI DISCLAIMS ANY WARRANTY OF TITLE AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, QUIET ENJOYMENT, QUIET POSSESSION, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS WITH REGARD TO TI REFERENCE DESIGNS OR USE THEREOF. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY BUYERS AGAINST ANY THIRD PARTY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON A COMBINATION OF COMPONENTS PROVIDED IN A TI REFERENCE DESIGN. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, SPECIAL, INCIDENTAL, CONSEQUENTIAL OR INDIRECT DAMAGES, HOWEVER CAUSED, ON ANY THEORY OF LIABILITY AND WHETHER OR NOT TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES, ARISING IN ANY WAY OUT OF TI REFERENCE DESIGNS OR BUYER’S USE OF TI REFERENCE DESIGNS.

TI reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques for TI components are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

Reproduction of significant portions of TI information in TI data books, data sheets or reference designs is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards that anticipate dangerous failures, monitor failures and their consequences, lessen the likelihood of dangerous failures and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in Buyer’s safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed an agreement specifically governing such use.

Only those TI components that TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components that have ***not*** been so designated is solely at Buyer's risk, and Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265