TI Designs

Fast Startup for Industrial Ethernet Applications With AM335x Processors

TI Designs

TI provides the system solution for integrated multi-protocol industrial Ethernet communication on Sitara™ processors. Fast startup after device power up has been defined by various industrial Ethernet standards. This TI Design describes:

- Fast startup analysis of key system components
- Example ARM® secondary bootloader in with fast start-up functionality
- NOR and SPI flash timing configuration example

Design Resources

TIDEP0049	Design Folder
AM3359	Product Folder
TLK110	Product Folder
DP83848I	Product Folder
TPS65910A3	Product Folder
TMDSICE3359 EVM	Tools Folder

TI E2E™ Community

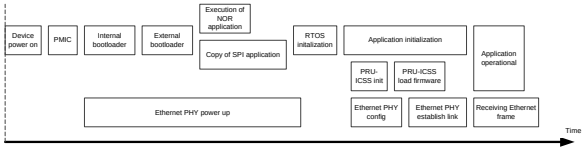
ASK Our E2E Experts
WEBENCH® Calculator Tools

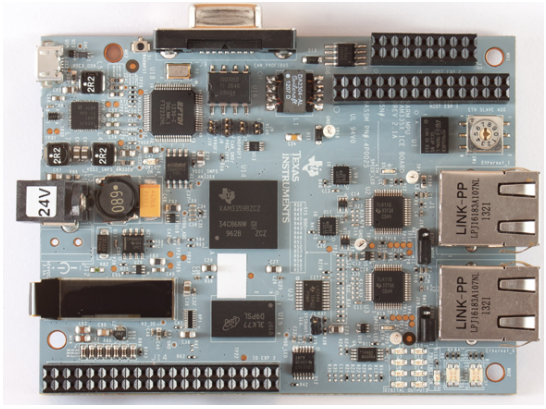
Design Features

- ARM Secondary Bootloader in Source Code Allows Customization
- Fast Start-up Timing Analysis of PMIC, Ethernet PHY, NOR and SPI Flash, and Bootloader
- ARM Bootloader Validated With TMDSICE3359 Industrial Communication Engine (ICE) EVM

Featured Applications

- Programmable Logic Controller (PLC)
- Industrial Sensor and I/O Modules
- Industrial Drives
- Industrial Communication Gateways
- Industrial Ethernet





An IMPORTANT NOTICE at the end of this TI reference design addresses authorized use, intellectual property matters and other important disclaimers and information.

1 System Description

In the past the startup or boot time of industrial slave devices has not been critical for many of the industrial applications. A start-up time of 10 seconds or more was assumed to be normal and okay for most of the applications.

With industrial communication moving into the automotive space, it is essential to speed up the startup time after power up of a slave device. One example is the robotic tool in car manufacturing lines—here, the robot has to exchange the tool. Because the tool uses industrial communication, it needs to respond to the robot arm within less than a second after powering up.

The industrial Ethernet standards PROFINET® and EtherNet/IP™ already take care of the startup time. The other fieldbus standardization bodies do not add anything to their standards yet.

This TI Design helps to understand the definition and requirements of fast startup and looks at the different system components that are involved in the fast startup sequence. The guide provides some system and configuration examples that support fast startup. Finally, the different aspects are demonstrated and measured on the TMDSICE3359 EVM.

1.1 Definition of Fast Startup

There are a variety of definitions for fast startup, which depends on the use case, the industrial Ethernet protocol, and the industrial application itself. Therefore, the user needs to define what fast startup means before implementing it.

As referred in Section 1, usually the startup time of PLC and I/O derives, motors, sensors, and actuators are in the range of 10 seconds or more. The startup time depends on a variety of components: hardware devices, boot configuration, bootloader, boot medium, initialization sequence, operation system, industrial communication stack, application, and so on. The following subsections describe how PROFINET and EtherNet/IP define fast startup before setting the target for this TI Design.

1.1.1 PROFINET Fast Startup

A PROFINET network consists of a controller (master) and a device (slave) instead of master and slave devices. The controller as well as the device can be data consumer, data producer, or both. Big car manufacturer lines often use PROFINET. Each car is made specific according to a customer order. Therefore, the final car requires a high level of customization. Factory robots that are versatile enough for this task need to be able to exchange their tools. Those tools are also controlled through PROFINET, and once the robot attaches the tool, it is powered up. Now the factory robot should be ready and not slow down the manufacturing line.

Therefore, the PROFIBUS Nutzerorganisation (PNO) and PROFIBUS International (PI) have defined the fast startup (FSU) procedure for PROFINET. They target a system startup to less than a second.

The FSU time in PROFINET is defined from the power up until an output can be set in the PN device. This requires that the PLC has established PN communication with the device and the device is able to exchange cyclic process data. This time has been defined by PNO as 500 ms.

The FSU requirement is valid starting with the second run-up only. During the first run, system provisioning is done and the initial parameter between the PLC and robot are established and negotiated. This information is then stored in the non-volatile storage (NVS) inside the tool to keep it preserved while the tool is powered down. The device must also store in NVS the device name and IP address permanently.

FSU for PROFINET defines that the Ethernet PHY must use a fixed configuration with auto-negotiation disabled. For two Ethernet port devices, configure one port with standard wiring and cross the second port's RX and TX. This allows the use of a standard Ethernet patch cable, which is most commonly used for Ethernet network wiring.

Typically, devices with FSU disabled or do not support FSU overall are passive on the network. Therefore, only the master would detect them if the controller (the master) would try to discover them. After power up, the device is actively sending a "DCP HELLO" service message to the PN network to allow the master to detect the slave device quickly.

With the factory settings of a device disable the FSU because the PLC first needs to provide it.

1.1.2 EtherNet/IP QuickConnect™

An EtherNet/IP network consists of a scanner (master) and an adapter (slave).

For EtherNet/IP, ODVA has defined QuickConnect as the name for fast startup. ODVA also refer to automotive applications, robots, tool changes, and frames as end applications. They want to support the quick exchange of tooling figures.

QuickConnect defines an overall time of 350 ms until the adapter is ready to send out the first message over the Ethernet network. This is the time for the adapter to allow an incoming TCP/IP connection. Overall, the specification allows 500 ms (like FSU for PROFINET) until the adapter has connected with the scanner and is able to set an output.

The first message of an adapter is a Gratuitous ARP, which advertises to the scanner that a new station is on the network. This allows 150 ms for the scanner and adapter to connect.

EtherNet/IP defines two classes of QuickConnect:

1. Class A: ≤ 350 ms
2. Class B: ≤ 2 s

Enable the QuickConnect feature through the configuration parameters, which are stored in NVS memory. It is disabled with the factory default settings as the scanner first needs to provision the adapter during the first run-up and enable the feature.

1.1.3 Other Industrial Ethernet Standards

Most of the other industrial Ethernet standards (Sercos III, PowerLink, EtherCAT, and so on) have not yet defined a fast startup process before the release of this TI Design. However, it should be in the manufacturer's interest to enable to speed up—at least from the hardware point of view.

1.1.4 This TI Design

This TI Design focuses on the part of the startup time from applying power to the device (power up) until the device is reaching the main() function.

The main() function initializes the board for operation (pinmux, task and stack initialization, and so on) and starts the operating system. The Industrial SDK examples for industrial Ethernet use the real-time operating system (RTOS) SysBios™ from Texas Instruments.

In a future step, the provider of the industrial Ethernet stack needs to do the optimization for speeding up the startup and initialization time of the stack. The provider is much more capable of supporting customer applications in that aspect. TI is not such provider; therefore, this TI Design focuses on the various aspects of the startup sequence, including hardware initialization, bootloader, boot medium, Ethernet PHY configuration, and bus timing enhancement.

2 Block Diagram

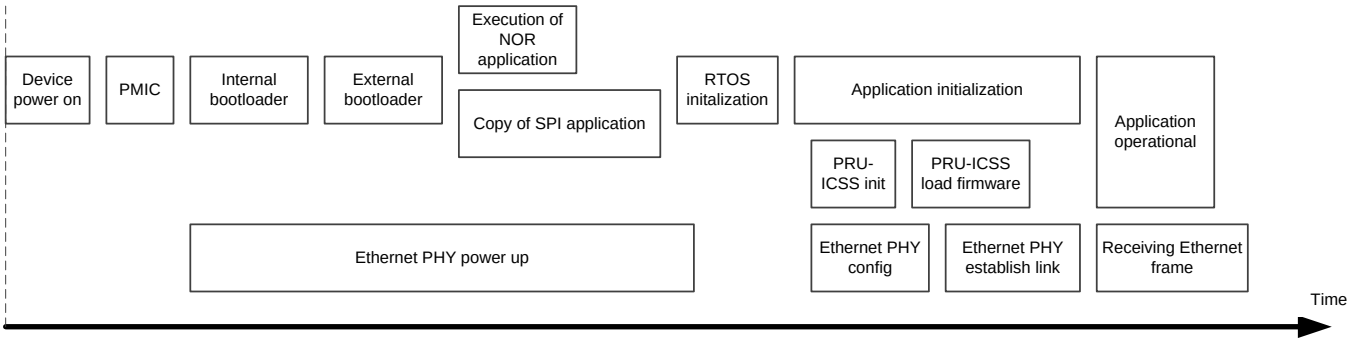


Figure 1. Startup System Block Diagram

2.1 Highlighted Products

2.1.1 AM3359 Processor

Up to 1-GHz Sitara™ARM® Cortex®-A8 32-bit RISC processor

- NEON™ SIMD coprocessor
- 32KB of L1 Instruction and 32KB of data cache with single-error detection (parity)
- 256KB of L2 cache with error correcting code (ECC)
- 176KB of on-chip boot ROM
- 64KB of dedicated RAM
- Emulation and debug JTAG
- Interrupt controller (up to 128 interrupt requests)

Programmable Real-Time Unit Subsystem and Industrial Communication Subsystem (PRU-ICSS)

- Supports protocols such as EtherCAT®, PROFIBUS, PROFINET, EtherNet/IP, and more
- Two PRUs
- 32-bit load and store RISC processor capable of running at 200 MHz
- 8KB of instruction RAM with single-error detection (parity)
- 8KB of data RAM with single-error detection (parity)
- Single-cycle 32-bit multiplier with 64-bit accumulator
- Enhanced GPIO module provides shift-in or shift-out support and parallel latch on external signal
- 12KB of shared RAM with single-error detection (parity)
- Three 120-byte register banks accessible by each PRU
- INTC for handling system input events
- Local interconnect bus for connecting internal and external masters to the resources inside the PRU-ICSS
- Peripherals inside the PRU-ICSS:
  - One universal asynchronous receiver and transmitter (UART) port with flow control pins, supports up to 12 Mb/s
  - One enhanced capture (eCAP) module
  - Two MII Ethernet ports that support industrial Ethernet, such as EtherCAT
  - One management data input and output (MDIO) port

On-chip memory (shared L3 RAM)

- 64KB of general-purpose on-chip memory controller (OCMC) RAM
- Accessible to all masters

External memory interfaces (EMIF)

- mDDR(LPDDR), DDR2, DDR3, and DDR3L controller:
  - mDDR: 200-MHz clock (400-MHz data rate)
  - DDR2: 266-MHz clock (532-MHz data rate)
  - DDR3: 400-MHz clock (800-MHz data rate)
  - DDR3L: 400-MHz clock (800-MHz data rate)
  - 16-bit data bus
  - 1GB of total addressable space
  - Supports one ×16 or two ×8 memory device configurations
- General-purpose memory controller (GPMC)
  - Flexible 8-bit and 16-bit asynchronous memory interface with up to seven chip selects (NAND, NOR, Muxed-NOR, or SRAM)
  - Uses BCH code to support 4-, 8-, or 16-bit ECC
  - Uses hamming code to support 1-bit ECC

See the AM3359 datasheet for a complete list of features [3].

2.1.2 TMDSICE3359 ICE EVM

Hardware specification

- AM3359 ARM Cortex-A8
- DDR3, NOR flash, and SPI flash
- Organize light-emitting diode (OLED) display
- TPS65910 power management
- 24-V power supply
- USB cable for JTAG interface and serial console

Software and tools

- SYS/BIOS real-time operating system (OS)
- Starterware base port
- TI's Code Composer Studio™ (CCS) integrated development environment (IDE)
- Application stack for industrial communication protocols
- Sample industrial applications

Connectivity

- PROFIBUS interface
- CANOpen
- EtherNet/IP
- PROFINET
- Sercos III
- Digital I/Os
- SPI
- UART
- JTAG

See the TMDSICE3359 website for complete list of features and design resources: www.ti.com/tool/tmdsice3359.

2.1.3 TLK110 Industrial Ethernet PHY

NOTE: A recommended alternative part is DP83848I. The device has the *same functionality* and *pinout* as the compared device but is *not* an exact equivalent.

TLK110 Industrial Temperature 10/100 Mb/s Ethernet Physical Layer Transceiver with the following features:

- Low power consumption
  - Single supply: < 205-mW PHY, 275 mW with center tap (typical)
  - Dual supplies: 126-mW PHY, 200 mW with center trap (typical)
- Programmable power back off to reduce PHY power up to 20% in systems with shorter cables
- Low deterministic latency supports IEEE1588 implementation
- Cable diagnostics
- Programmable fast link down modes, 10-µs reaction time
- Variable I/O voltages range: 1.8 to 3.3 V
- 3.3-V MAC interface
- Fixed TX clock to XI with programmable phase shift
- Auto-MDIX for 10/100 Mb/s
- Energy detection mode
- 25-MHz clock out
- MII and RMII capabilities
- Serial management interface (MDIO)
- IEEE 802.3u MII
- IEEE 802.3u auto-negotiation and parallel detection
- Error-free 100Base-T operation up to 150 meters under typical conditions
- Error-free 10Base-T operation up to 300 meter under typical conditions
- IEEE 802.3u ENDEC, 10Base-T transceiver and filters
- IEEE 802.3u PCS, 100Base-TX transceivers
- IEEE 1149.1 JTAG
- Integrated ANSI X3.263 compliant TP-PM physical sublayer with adaptive equalization and baseline wander compensation
- Programmable LED support link, 10/100-Mb/s mode, activity, and collision detect
- 10/100Mb/s packet BIST (built-in self test)
- HBM ESD protection on RD± and TX± of 16 kV
- 48-pin LQFP Package: 7 × 7 mm

2.1.4 DP83848I Industrial Ethernet PHY

DP83848I PHYTER™ QFP Single Port 10/100 Mb/s Ethernet Physical Layer Transceiver with the following features:

- Temperature ranges from –40°C to 85°C
- Low-power 3.3-V, 0.18-µm CMOS technology
- Low-power consumption: <270-mW typical
- 3.3-V MAC interface
- Auto-MDIX for 10/100 Mb/s
- Energy detection mode
- 25-MHz clock input
- SNI (configurable)
- RMII rev. 1.2 interface (configurable)
- MII serial management interface (MDC and MDIO)
- IEEE 802.3 MII
- IEEE 802.3 auto-negotiation and parallel detection
- IEEE 802.3 ENDEC, 10BASE-T transceivers and filters
- IEEE 802.3 PCS, 100BASE-TX transceivers and filters
- IEEE 1149.1 JTAG
- Integrated ANSI X3.263 compliant TP/PMD physical sub/layer with adaptive equalization and baseline wander compensation
- Error-free operation up to 150 meters
- Programmable LED support for link, 10/100 Mb/s mode, activity, duplex, and collision detect
- Single register access for complete PHY status
- 10/100 Mb/s packet BIST (built-in self test)

2.1.5 TPS65910A3 PMIC

TPS65910A3 integrated power-management unit features:

- Embedded power controller
- Two efficient step-down DC-DC converters for processor cores
- One efficient step-down DC-DC converter for I/O power
- One efficient step-up 5-V DC-DC converter
- SmartReflex™ compliant dynamic voltages management for processor cores
- Eight LDO voltage regulators and one real-time clock (RTC) LDO (internal purpose)
- One high-speed I^2C interface for general-purpose control commands (CTL-I^2C)
- Once high-speed I^2C interface for SmartReflex™ Class 3 control and command (SR-I^2C)
- Two enable signals multiplexed with SR-I^2C, configurable to control any supply state and processor core supply voltage
- Thermal shutdown protection and hot-die detection
- An RTC resource with
  - Oscillator for 32.768-kHz crystal or 32-kHz built-in RC oscillator
  - Date, time, and calendar
  - Alarm capability
- Once configurable GPIO
- DC-DC switching synchronization through internal or external 3-MHz clock

3 System Design Theory

3.1 Fast Startup System Description

Fast startup refers to the capability of the specific industrial device to be ready for operation within a minimum of time after device power up. As mentioned in Section 1, various industrial Ethernet standards define this time in a different way.

This TI Design measures the fast startup time until the main() function of the industrial application is reached. It does not include initializing the stack and establishing communication between the slave and master devices, as this is out of its scope. TI is not an industrial Ethernet stack provider, but refers to its partners who can support customers in their field of experience.

However, this TI Design uses different industrial applications like EtherNet/IP scanner, EtherCAT slave, and PROFINET device. The recommendations and optimizations for various system components are discussed in this section. This TI Design provides a bootloader with various components of fast startup optimization as sample code. Finally, this TI Design provides measurements of the startup sequence, which are performed on the TMDSICE3359 ICE EVM.

3.2 System Level Considerations

The designer must have an overlook at the complete startup sequence. The following lists the components that are involved with the TMDSICE335x ICE board (the customer application might have even more components that are out of the scope of this TI Design):

- AM335x processor SYSBOOT pins, latched in once the power is applied and reset signal is released from the processor
- Bootstrap pins of TLK110 industrial Ethernet PHY transceiver, latched in after power is applied and PHY reset signal is released
- The processor internal bootloader uses the SYSBOOT pins to decide the processor configuration and the boot medium. The internal bootloader loads the secondary bootloader from external memory
- The secondary bootloader, which resides on external memory, configures essential system components such as external memory like DDR, NOR or NAND memory, SPI memory, Ethernet PHY, essential pinmuxing, and others. It prepares the ground for the industrial application, which is executed next
- Industrial application, which includes the industrial Ethernet stack and the devices specific application.

Note that sometimes it is not possible to use the SYSBOOT and bootstrap pins to configure the device in an optimum way. This is okay as software does allow configuration after that time of release of reset. It is often okay that the external bootloader, which is the first software that the designer or customer can influence efficiently, configures.

3.3 Startup Components

The following subsections describe the system component involved with the startup sequence, what is configured by the processor or device, and the ways to optimize them for fast startup.

It also refers to the places where this optimization would make sense to get implemented (if applicable).

3.3.1 ICE Board Overview

The TMDICE3359 ICE EVM is used to as an example of the industrial device for fast startup. Therefore, this section shows the system block diagram and where to find the main system components.

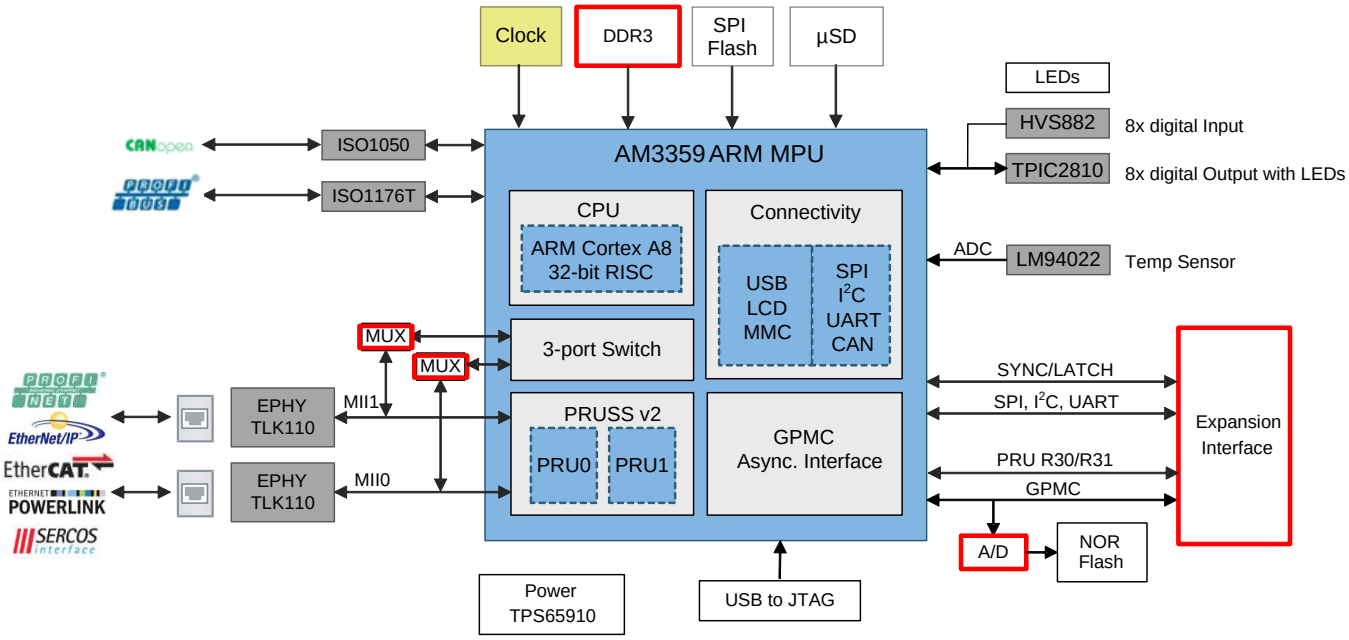


Figure 2. TMDSICE3359 ICE System Block Diagram

3.3.2 Power Management and PMIC

The TPS65910A3 is a power management integrated circuit (PMIC) that supports the startup sequence of the AM335x processor family. It follows the power rail sequence as referred in the processor data sheet. The power sequence and timing is programmed in the internal EEPROM of the PMIC; therefore, it is not possible to change any of the timing or sequence.

The current device takes ~16 ms from getting power, generating the different power rails for the processor, and releasing the processor from reset.

There are no further optimizations implemented with this TI Design for the PS65910A3.

3.3.3 Processor and SYSBOOT Pins

The AM335x processor supports 16 SYSBOOT pins that are latched in after power has been supplied and with the release of the processor reset signal. The SYSBOOT pins are used to configure processors as well the internal bootloader, which resides in the internal ROM.

The internal bootloader selects the boot media based on the SYSBOOT pins. Configure the correct boot sequence so that the internal bootloader does not try to boot from an unconnected memory.

See Section 26 of the AM3359 Technical Reference Manual for the SYSBOOT configuration pins and the selected boot sequence [4].

3.3.4 Internal Bootloader

The internal bootloader is stored in the ROM memory mask of the AM335x processor and cannot be changed by the user.

The internal bootloader uses the SYSBOOT pins to decide on the boot medium through the boot sequence. The ICE board has one jumper J5 to easily change the boot mode between SPI and NOR. It is also possible to change the remaining SYSBOOT pins on TMDSICE3359 ICE board by replacing the appropriate SYSBOOT pull-resistors (see Section 8.1).

The TMDSICE3359 ICE EVM is configured for SYSBOOT[4:0] as 0b110n0. The 'n' can be configured to '1' or '0' through J5.

Table 1. SYSBOOT Configuration Pins Supported by ICE

SYSBOOT [15:14]	SYSBOOT [13:12]	SYSBOOT [11:10]	SYSBOOT [9]	SYSBOOT [8]	SYSBOOT [7:6]	SYSBOOT [5]	SYSBOOT [4:0]	BOOT SEQUENCE			
00b = 19.2 MHz 01b = 24 MHz 10b = 25 MHz 11b = 26 MHz	00b (All other values reserved)	Don't care for ROM code	Don't care for ROM code	Don't care for ROM code	Don't care for ROM code	0 = CLKOUT1 disabled 1 = CLKOUT1 enabled	11000b	SPI0	MMC0	USB0	UART0
00b = 19.2 MHz 01b = 24 MHz 10b = 25 MHz 11b = 26 MHz	00b (All other values reserved	For XIP boot: 00b = non-muxed device 10b = muxed device x1b = reserved	Don't care for ROM code	0 = 8-bit device 1 = 16-bit device	Don't care for ROM code	0 = CLKOUT1 disabled 1 = CLKOUT1 enabled	11010b	XIP (MUX2)	UART0	SPI0	MMC0

In boot mode 0b11000, the ICE board boots from SPI0 first. If there is no valid image in SPI, the internal bootloader cycles through the boot sequence, which is MMC0, USB0, and UART0. In boot mode 0xb11010, the boot sequence is XIP (MUX2), which is connected to the NOR flash. If there is no valid image found, it will go cycle through UART0, SPI0, and MMC0.

It is essential to select the right boot modes through the SYSBOOT pins; otherwise, the internal bootloader tries to boot from a memory that contains no external secondary bootloader. Eventually, the bootloader times out and proceeds to the next boot sequence medium, but this takes some additional time.

The internal ROM bootloader loads the secondary bootloader.

If XIP is selected through the SYSBOOT configuration, the internal bootloader executes the code directly from the boot medium without copying the secondary bootloader or application to internal memory. If SPI is selected, the internal bootloader copies the secondary bootloader into internal memory, followed by jumping to the external bootloader entry address in internal memory.

3.3.5 Secondary Bootloader

The secondary bootloader is executed after the internal bootloader is completed. The secondary bootloader is either located in NOR memory (XIP) or it is executed from internal memory. The secondary bootloader is provided in source code through the industrial SDK. This TI Design also provides an enhanced secondary bootloader for evaluating the fast startup boot process.

The tasks of the secondary bootloader of the industrial SDK are the following:

- Reads out chip capabilities like max CPU frequency, type of device, and so on
- Configures the internal PLLs according to the chip capabilities
- Configures and enables the memory management unit (MMU) to allow faster CPU execution through code and data caching
- Configures external memory interface (DDR3)
- Configures peripherals (SPI and NOR timings, Ethernet PHY, PRU-ICSS, and so on)
- Determines where the industrial application is located
- For SPI, copies the industrial application into the DDR3 memory and jumps to the application entry point
- For NOR, jumps directly to the industrial application entry point in the NOR memory address (no copy needed)

NOTE: The industrial applications has to be compiled for the appropriate memory (NOR, DDR3, internal memory).

The internal bootloader disables the MMU again before jumping to the entry point of the industrial application.

The secondary bootloader can be modified and adopted by the customer.

For debug purposes, this TI Design configures a GPIO in the secondary bootloader to measure timing behavior. This is GPIO1_8.

Note that the secondary bootloader also has the default option to check if an inserted SD card has an valid industrial application. As this TI Design does not investigate this boot medium, the bootloader is optimized by removing the section to check for SD card image.

3.3.6 SPI Flash Boot Medium

When selecting SYSBOOT pins to boot through the SPI0 flash memory, the internal bootloader configures SPI0 pins and the SPI0 peripheral. To support a variety of SPI flash devices, the internal bootloader uses a rather moderate SPI clock speed of 12 MHz. This is to make booting from the SPI as compatible as possible to a variety of SPI flash devices.

The TMDSICE board has the SPI flash holding the secondary bootloader and the industrial application. The secondary bootloader initializes and configures the DDR3 memory before it copies the industrial application into the DDR3 memory. Note that AM335x does not support code execution from SPI directly; therefore, the ARM code needs to be copied over to DDR or internal memory first before getting executed.

To accelerate the SPI copy process of the external bootloader copying the industrial application from the SPI flash to the DDR/internal memory, it is essential to increase the SPI speed. As an example, the secondary bootloader uses 50 MHz (max frequency).

Note that configuration data (fast boot enabled, Ethernet PHY configuration) might be also stored by the industrial Ethernet stack inside the SPI flash. This information can be accessed as well by the secondary bootloader to perform required configuration tasks, for example the Ethernet PHY configuration.

The TMDSICE3359 ICE board uses the SPI flash memory type W25Q64 from Winbond.

3.3.7 NOR Flash Boot Medium

The NOR flash supports eXecution In Place (XIP), which means that the ARM core can directly execute code from the NOR flash. The NOR flash can be also get cached to speed up code execution.

The ICE board has stored the secondary bootloader and industrial application inside the NOR flash. First, the secondary bootloader initializes processor and board peripherals before it jumps to the entry point of the industrial application.

The internal bootloader configured the GPMC with a conservative timing to allow a variety of NOR flash to be interfaced. For fast boot, the GPMC timing needs to be fasten. However, there is one problem: It is not possible to reconfigure the GPMC bus timings for NOR if the ARM is executing from NOR. It would require for the secondary bootloader to get executed from internal memory before the GPMC/NOR timing can be adopted.

This TI Design tested the scenario that the secondary bootloader is in the SPI flash. As it is getting copied to the internal memory, the secondary bootloader can reconfigure the GPMC/NOR flash timing. After that (and the other baseline configuration), the secondary bootloader jumps to the entry point of the industrial application in NOR flash. Note that this does not require a copy of the industrial application to first copy it into DDR memory, as it was described for the SPI case.

The TMDSICE3359 ICE board uses the NOR flash memory type M29W160EB from Micron.

The bootloader has an example configuration for this NOR flash memory type to fast the XIP process after the secondary bootloader has configured the GPMC/NOR timing. Note that only the read access timing have been adopted by the secondary bootloader. If desired, the customer can also optimize (fasten) the NOR write timing.

3.3.8 Industrial Ethernet PHY

The Ethernet PHY plays an important role when establishing the communication with the PLC. The integration of the PHY on the industrial slave device has to be optimized for hardware and software in order to power up quickly, establish a link with the peer Ethernet PHY, so the industrial Ethernet fieldbus stack can communicate with the PLC. One item is to disable auto-negotiation, which takes a long time, and configure the PHY to operate in a fixed operating mode.

Therefore, look at the following five items:

Bootstrap Pins
The bootstrap pins allow for preconfiguring for a specific operating mode when the Ethernet PHY gets power applied and is taken out of reset. Preconfiguring allows to set the MDIO address of the PHY (that is, the programming interface) as well as to set fixed mode of operation. Note that the bootstrap configuration in the PHY can still get overwritten through the MDIO programming interface from the ARM application.

Setting the fixed mode of operation eliminates the need to program the PHY through MDIO. Instead, if the desired mode of operation has been configured, the ARM application does not need to wait for the PHY to be ready for operation. On the other hand, access through MDIO is quite fast; therefore, it would be still OK to make modifications once the PHY comes out of reset.

Power up Until PHY is Accessible Through MDIO Interface
Once power has been applied to the PHY and it has been taken out of reset, it takes a specific amount of time before the PHY is ready for operation. Check the datasheet of the PHY to learn more. The TLK110 on the TMDSICE3359 ICE board takes a time of approximately 200 ms until it is accessible through MDIO. Once it is accessible, the ARM application (bootloader, industrial application) can overwrite the bootstrap settings and configure the PHY in the desired operating mode.

If the bootstrap pins do not have the desired value, reset the PHY in the bootloader and configure the PHY through the MDIO in the industrial application. Note that the industrial application should not reset the PHY again; otherwise, the MDIO access is delayed again by 200 ms.

Auto-Negotiation Feature of PHY

Ethernet physical interfaces offer today an auto-negotiating feature. Once the physical connection between two Ethernet PHYs is in place, both PHYs negotiate their communication parameters automatically.

This negotiation affects following parameters:

- Cable RX/TX crossover
- Communication speed (10/100 Mb/s)
- Half duplex or full duplex

The negotiation itself can take multiple seconds. While this is great feature for Ethernet overall, it does not allow to support the fast startup functions of industrial Ethernet protocols. Therefore it is mandatory to disable the auto negotiation during machine use and to use a fixed configuration. This can be done after initial connection between master and slave and once the fast startup function is enabled.

Dual-Port Ethernet Devices

Most of the industrial Ethernet devices have two Ethernet ports. To simplify network plant wiring by using standard Ethernet patch cable, it is recommended to configure one port as MDI while configuring the second port as MDIX. This means that RX and TX line are swapped in the second port. By this, standard Ethernet patch cable (which are have a one-to-one connection or straight connection) can be used to wire the first slave port 2 to the second slave port 1, and so on.

Fixed MDIO Configuration Examples

PROFINET recommends to have fixed configuration for full duplex at 100 Mb/s, one port configured as MDI and second port as MDIX.

Table 2 shows an example for TLK110 and DP83848I to configure the fixed configuration settings.

- Auto-negotiation disabled
- Full-duplex
- 100 Mb/s
- MDI for port 1, MDIX for port 2

Table 2. TLK110 and DP83848I

TLK110		
REGISTER	**VALUE**	**COMMENT**
0X00	PHY1/PHY2 = 0X000_2100	100 Mb, full duplex, auto-neg disabled
0X19	PHY1 &= ~[(1<<15) | (1<<14)] PHY2 &= ~(1<<15) PHY2 |= (1<<14)	Port 1: Clear auto-MDI/X and set MDI Port 2: Clear auto-MDI/X and set MDIX
DP83848I		
REGISTER	**VALUE**	**COMMENT**
0X00	PHY1/PHY2 = 0X000_2100	100 Mb, full duplex, auto-neg disabled
0X19	PHY1 &= ~[(1<<15) | (1<<14)] PHY2 &= ~(1<<15) PHY2 |= (1<<14)	Port 1: Clear auto-MDI/X and set MDI Port 2: Clear auto-MDI/X and set MDIX

3.3.9 Industrial Ethernet Stack and Industrial Application

The industrial Ethernet stack has to support the fast startup or quick connect functionality. The stack is provided by a stack vendor of by the customer. Contact the appropriate person from the stack vendor or customer to know how to enable the fast startup function of the stack.

3.3.10 Industrial PLC and Field Devices

Once the industrial Ethernet stack is operating on the device, it needs to establish communication with the PLC to exchange process data. One note is that instead of the slave being passive on the network, it needs to generate some kind of "Hello" message to advertise to the PLC that a new slave is active on the bus. Both EtherNet/IP and PROFINET provide in the QuickConnect and FSU the connection and message exchange sequence between the device and the PLC.

3.4 Conclusion

Implementing fast startup on a device requires good planning of various hardware and software components.

The TMDSICE3359 ICE board has not been developed with fast startup as target; therefore, the user needs to compromise when testing the fast startup feature. However, there are additional options to configure, for example, the Ethernet PHY, even later in the sequence.

Use this TI Design as a starting point to understand the system components involved with fast startup. The bootloader also provides some examples that can be reused in customer projects.

4 Getting Started Hardware

4.1 TMDSICE3359 ICE Board Overview

The following figures show the TMDSICE3359 ICE components.

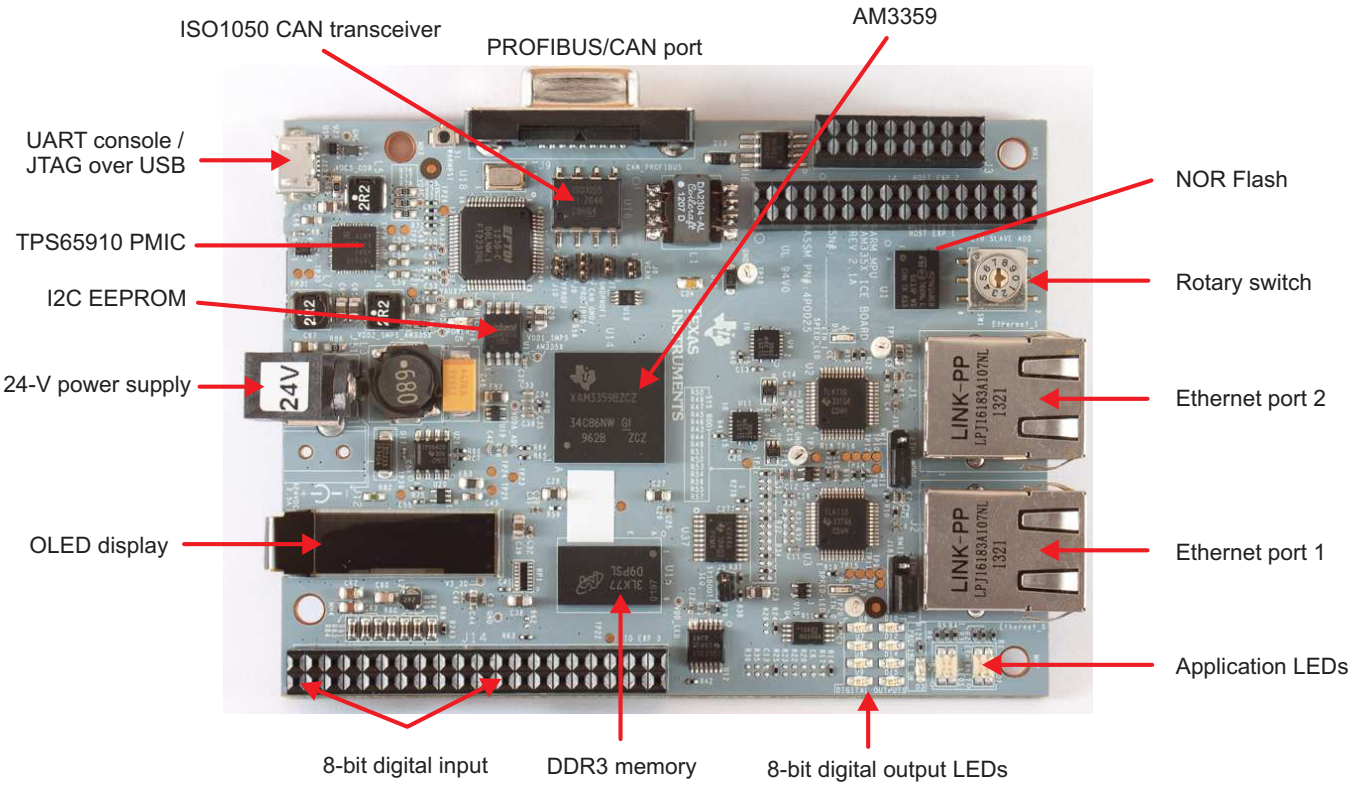


Figure 3. TMDSICE3359 ICE Top Side

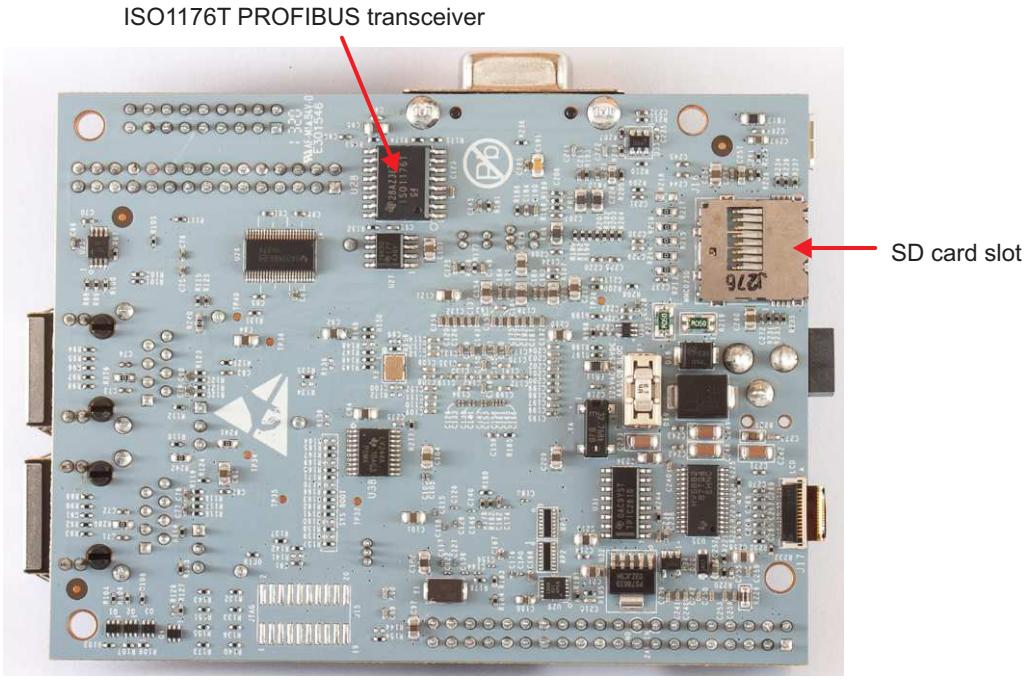


Figure 4. TMDSICE3359 ICE Bottom Side

The following signals are measured (see Section 8.1):

- VBAT
- PORZ
- SPI0_CS
- SPI0_CLK
- GPIO1_8 (bootloader GPIO used for timing measurement)
- PHY_RESET
- PHY_LINK
- SYS_WARM_RESET

4.2 Booting From SPI

When booting from SPI, J5 has to be set towards U12. A power cycle of the board is required to activate the SYSBOOT configuration.

4.3 Booting From NOR

When booting from NOR, J5 has to be set towards U37. A power cycle of the board is required to activate the SYSBOOT configuration.

5 Getting Started Software

5.1 CCS

The following hardware software is required:

- TMDSICE3359 ICEv2
- CCSv6 or higher
- Industrial SDK 1.1.0.8

5.1.1 Secondary Bootloader

Extract the bootloader source code files into following SDK path:

- C:\ti\am335x_sysbios_ind_sdk_1.1.0.8\sdk\starterware\build\armv7a\cgt_ccs\am335x\evmAM335x\bootloader

Import the bootloader into CCS.

The following build options are available to test fast startup. Select them by setting *Build Configuration → Set Active*:

- Fastboot_SPI: Configures SPI to 50 MHz, secondary bootloader and industrial application in SPI flash
- FB_SPIXIPNOR: Secondary bootloader in SPI flash and industrial application in NOR flash

In addition, the following #define can be used to enable or disable different configuration options:

- FASTBOOT_PHY: Enables configuration of the PHY in secondary bootloader
- FASTBOOT_SPINOR: Enables booting the secondary bootloader from SPI and followed by booting industrial application from NOR
- FASTBOOT_CONFIGNOR: Enables configuration of optimized NOR timing
- MEASURE_BOOT_TIME: Enables GPIO bank for toggling to measure boot time

5.2 Flashing the Secondary Bootloader

Follow the SPI and NOR flashing instructions in the *AM335x SYSBIOS Industrial SDK Getting Started Guide*, located at C:\ti\am335x_sysbios_ind_sdk_1.1.0.8\sdk\docs.

6 Test Setup

Use the following test setup:

- TMDSICE3359 ICE board
- Logic Analyzer LogicStudio 16 from LeCroy
- Windows® 7 PC with LogicStudio

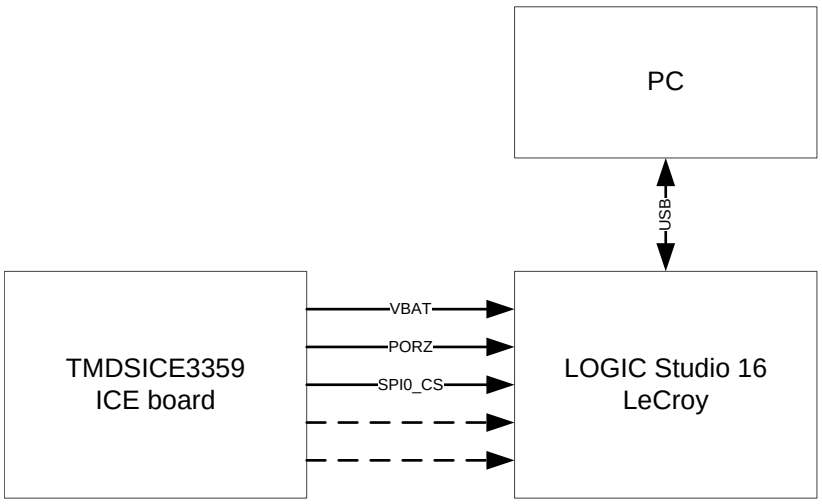


Figure 5. Test Setup

7 Test Data

A variety of measurements have been performed with different versions of the secondary bootloader. Each subsection describes a different test.

7.1 Baseline SPI Boot

Figure 6 shows the baseline SPI boot timing with the unmodified bootloader. The secondary bootloader and the industrial application are located in SPI flash memory.

The SPI0_CS signal shows two accesses to the SPI Flash. The first SPI0_CS access is the application loading of the secondary bootloader into the internal memory. The second SPI0_CS access is the loading of industrial application (EtherCAT) into the DDR memory.

- Secondary bootloader transferring industrial application to DDR memory: 1.069 s
- Total boot time: 1.19 s

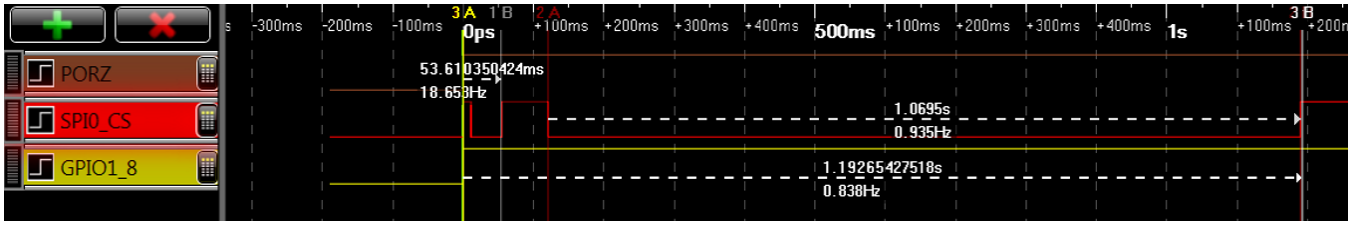


Figure 6. SPI Baseline

7.2 SPI Boot With Fastened SPI0_CLK

Figure 7 show the SPI boot time when SPI0_CLK is configured to support 50 MHz. The secondary bootloader and the industrial application are located in SPI flash memory.

The industrial application (EtherCAT) is loaded into the DDR memory with the second SPI_CS access.

- Secondary bootloader transferring industrial application to DDR memory: 26 ms
- Total boot time: 91 ms

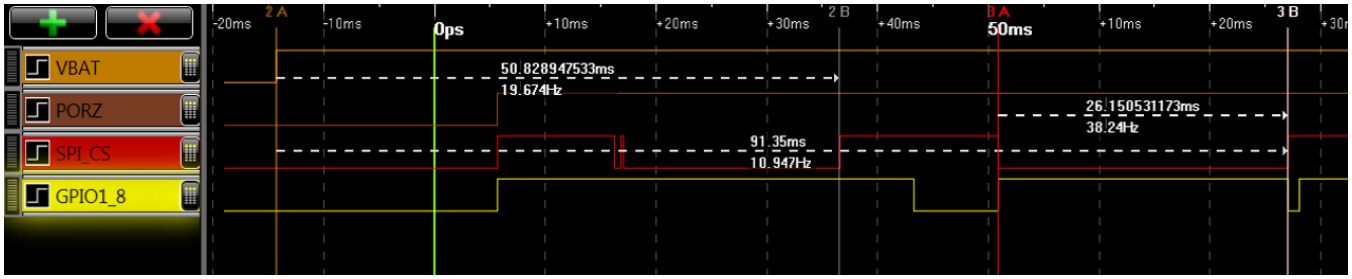


Figure 7. SPI0_CS Configured to 50 MHz

7.3 SPI Boot With NOR XIP

Figure 8 shows the boot time from SPI and XIP. The secondary bootloader is located in SPI flash and the industrial application is located in NOR flash. GPIO1_8 shows the transition or jump to the industrial application.

- Total boot time: 65 ms

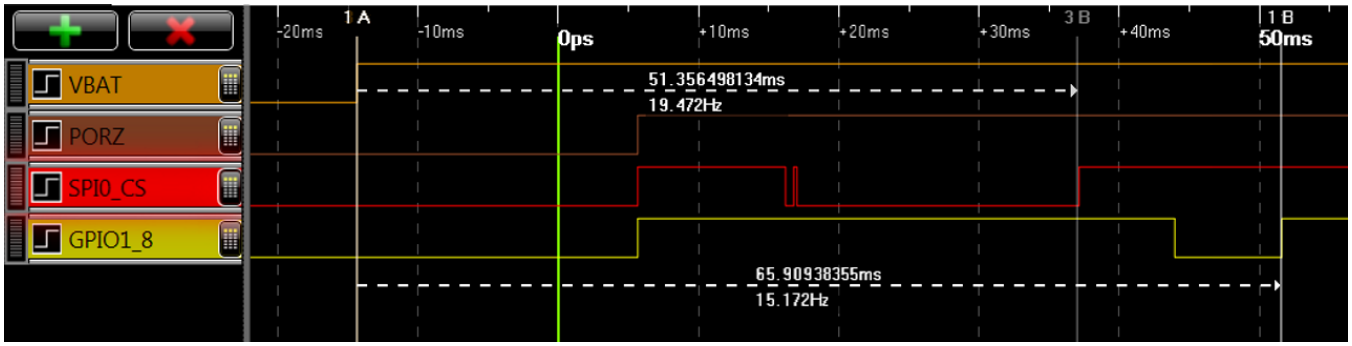


Figure 8. SPI Boot and XIP From NOR

7.4 PMIC Sequence

Time from VBAT to PMIC releasing PORZ: 20 ms

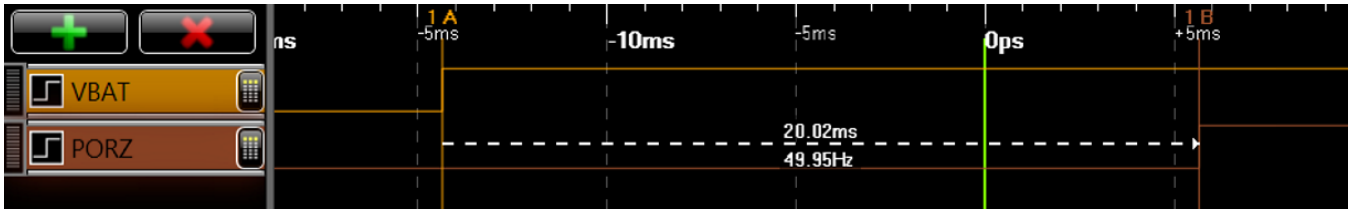


Figure 9. PMIC Sequence

7.5 First and Secondary Bootloader

SPI0_CS of first bootloader: 20 ms

SPI0_CS of secondary bootloader (SPI_CLK at 50MHz): 26 ms

Total boot time: 91 ms

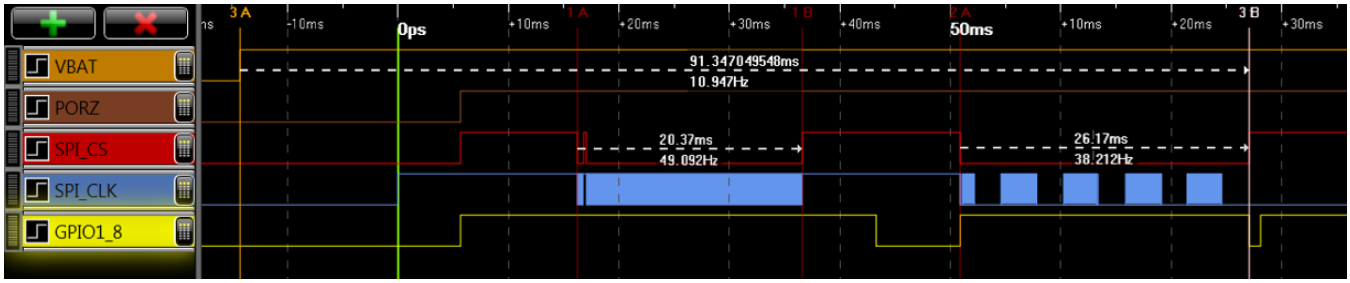


Figure 10. Boot Sequence of First and Secondary Bootloader

7.6 Ethernet PHY

Ethernet PHY is reset in secondary bootloader

From Reset to MDIO alive: 207 µs

Configuration of MDIO with fixed configuration to PHY link: 4.8 ms

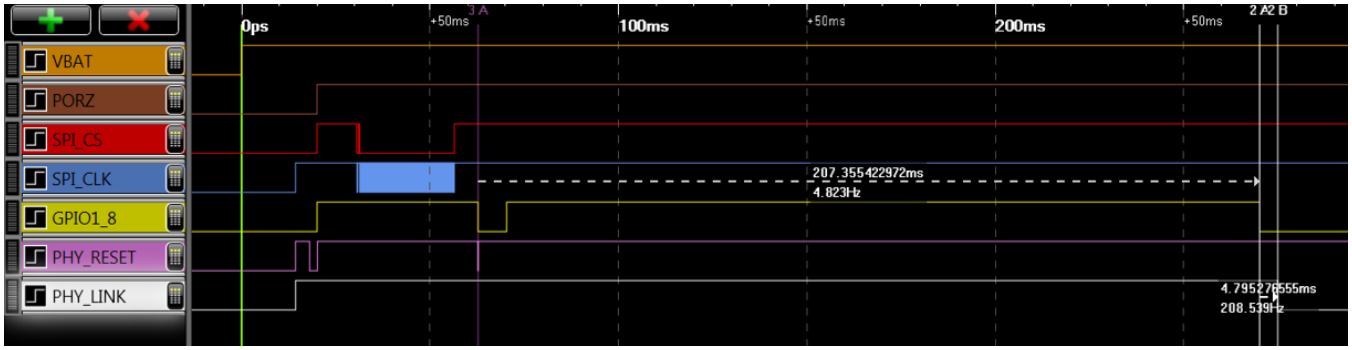


Figure 11. Ethernet PHY With Fixed Configuration

8 Design Files

8.1 Schematics

To download the schematics, see the design files at TIDEP0049.

8.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDEP0049.

8.3 Gerber Files

To download the Gerber files, see the design files at TIDEP0049.

8.4 Assembly Drawings

To download the assembly drawings, see the design files at TIDEP0049.

9 Software Files

To download the software files, see the design files at TIDEP0049.

10 References

1. Texas Instruments, E2E Community (http://e2e.ti.com/)
2. Texas Instruments, Code Composer Studio Download page (http://processors.wiki.ti.com/index.php/Download_CCS)
3. Texas Instruments, *AM335x Sitara™ Processors*, AM3359 Datasheet (SPRS717)
4. Texas Instruments, *AM335x Sitara™ Processors*, AM3359 Technical Reference Manual (SPRUH73)

11 Terminology

CCS— Code Composer Studio

ICSS— Industrial Communication Subsystem

PLC— Programmable Logic Controller

PRU— Programmable Real-time Unit

XIP— eXecute In Place

12 About the Author

THOMAS MAUER is a System Engineer in the Factory Automation and Control Team at Texas Instruments Freising, where he is responsible for developing reference design solutions for the industrial segment. Thomas brings to this role his extensive experience in industrial communications like Industrial Ethernet and fieldbuses and industrial applications. Thomas earned his electrical engineering degree (Dipl. Ing. (FH)) at the University of Applied Sciences in Wiesbaden, Germany.

INGOLF FRANK is a Systems Engineer in the Texas Instruments Factory Automation and Control team, focusing on programmable logic controller I/O modules. Ingolf works across multiple product families and technologies to leverage the best solutions possible for system level application design. Ingolf earned his electrical engineering degree (Dipl. Ing. (FH)) in the field of information technology at the University of Applied Sciences Bielefeld, Germany in 1991.

LARS LOTZENBURGER is a Systems Engineer at Texas Instruments where he is responsible for developing reference design solutions for the industrial segment. Lars brings to this role his extensive experience in analog and digital circuit development, PCB design, and embedded programming. Lars earned his diploma in electrical engineering from the University of Applied Science in Mittweida, Saxony, Germany.

Revision History

Changes from Original (September 2015) to A Revision	Page
• Changed from preview page	1

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

IMPORTANT NOTICE FOR TI REFERENCE DESIGNS

Texas Instruments Incorporated ("TI") reference designs are solely intended to assist designers (“Buyers”) who are developing systems that incorporate TI semiconductor products (also referred to herein as “components”). Buyer understands and agrees that Buyer remains responsible for using its independent analysis, evaluation and judgment in designing Buyer’s systems and products.

TI reference designs have been created using standard laboratory conditions and engineering practices. **TI has not conducted any testing other than that specifically described in the published documentation for a particular reference design.** TI may make corrections, enhancements, improvements and other changes to its reference designs.

Buyers are authorized to use TI reference designs with the TI component(s) identified in each particular reference design and to modify the reference design in the development of their end products. HOWEVER, NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY THIRD PARTY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT, IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI REFERENCE DESIGNS ARE PROVIDED "AS IS". TI MAKES NO WARRANTIES OR REPRESENTATIONS WITH REGARD TO THE REFERENCE DESIGNS OR USE OF THE REFERENCE DESIGNS, EXPRESS, IMPLIED OR STATUTORY, INCLUDING ACCURACY OR COMPLETENESS. TI DISCLAIMS ANY WARRANTY OF TITLE AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, QUIET ENJOYMENT, QUIET POSSESSION, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS WITH REGARD TO TI REFERENCE DESIGNS OR USE THEREOF. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY BUYERS AGAINST ANY THIRD PARTY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON A COMBINATION OF COMPONENTS PROVIDED IN A TI REFERENCE DESIGN. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, SPECIAL, INCIDENTAL, CONSEQUENTIAL OR INDIRECT DAMAGES, HOWEVER CAUSED, ON ANY THEORY OF LIABILITY AND WHETHER OR NOT TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES, ARISING IN ANY WAY OUT OF TI REFERENCE DESIGNS OR BUYER’S USE OF TI REFERENCE DESIGNS.

TI reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques for TI components are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

Reproduction of significant portions of TI information in TI data books, data sheets or reference designs is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards that anticipate dangerous failures, monitor failures and their consequences, lessen the likelihood of dangerous failures and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in Buyer’s safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed an agreement specifically governing such use.

Only those TI components that TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components that have ***not*** been so designated is solely at Buyer's risk, and Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265