

## TIDA-00605 Test Report

# Powering the Altera® Cyclone® IV with TPS65023 Power Management IC



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Figure 1 - Top Side

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## Feature Applications

- Factory Automation
- Motor Control
- Smart Grid
- Solar Inverters

## Description

The TIDA-00605 design is a compact, integrated power solution for Altera® Cyclone® IV SoC (out of the Cyclone® series family of products). This design showcases TPS65023 as an all-in-one IC used to supply the rails needed for powering the Cyclone® IV SoC. The TPS65023 offers simple, flexible output voltages and sequencing. The voltages on the DC/DC Converters can be set through software or via external resistor divider. This power management IC has a input range from 2.5 – 6V and can be run from a single 5V supply or from a single cell Li-Ion battery. This design has been tested and verified for industrial applications (-40°C to 105°C).

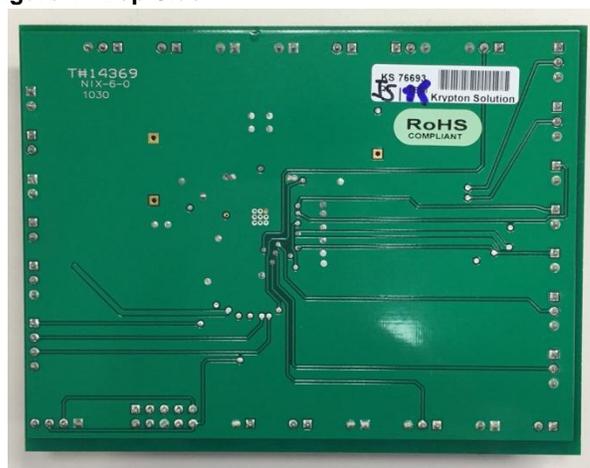


Figure 2 - Bottom Side

## TPS65023/Cyclone® IV Block Diagram [\(Return to Top\)](#)

### Power Supply Block Diagram

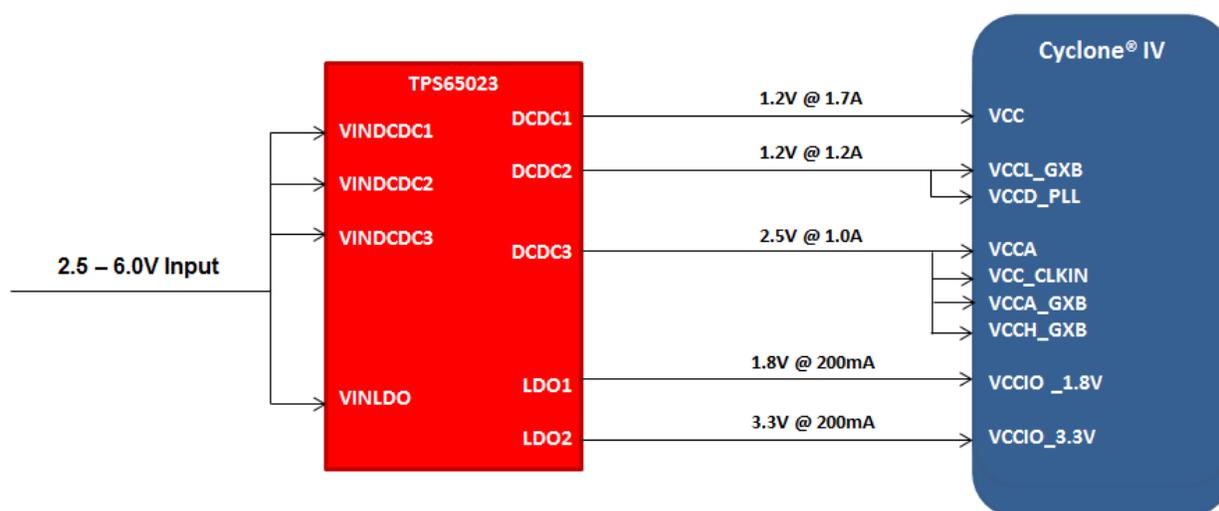


Figure 3 – Cyclone IV Block Diagram

### Typical Voltage and Current Requirements in End Applications

Depending on application and design on FPGA, current consumption can vary. The table below highlights the typical max currents each power output of the TPS65023 converters to the rails of the Cyclone IV. The VCCIO Rails on the Cyclone III range from 1.2 – 3.3V. The TPS65023 has 2 Linear Regulators that can supply the full range of Cyclone III's VCCIO.

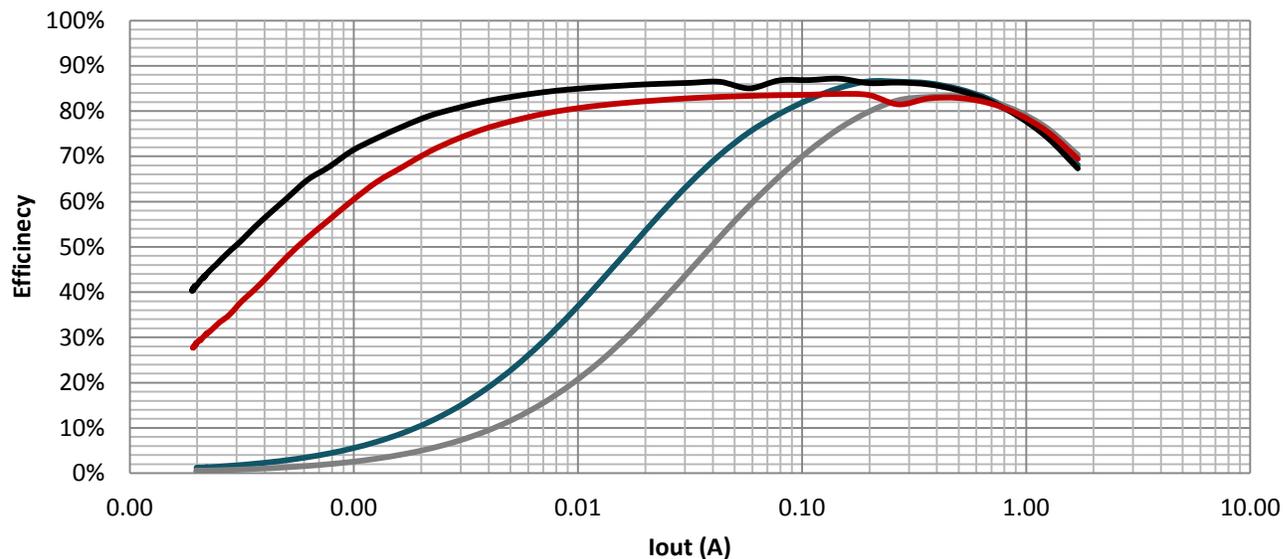
Cyclone IV Supply Rails	Voltage	Current Consumption (A)
VCC	1.2V	1.7
VCCL_GXB	1.2V	1.2
VCCD_PLL		
VCCA	2.5V	1.0
VCC_CLKIN		
VCCA_GXB		
VCCH_GXB		
VCCIO_1.8V	1.8V	0.200
VCCIO_3.3V	3.3V	0.200

**Note:** The current consumption numbers above are only estimates and the actual current consumption may vary depending on the application.

## Efficiency Curves [\(Return to Top\)](#)

DCDC1 ( $V_{out}=1.2V$ ) – VCC

### DCDC1 Efficiency vs Load Current @ $T_a=25^\circ C$



$V_{out} = 1.2V$

—  $V_{in} = 3.3V$  (PWM Mode)   
 —  $V_{in} = 5.0V$  (PWM Mode)  
—  $V_{in} = 3.3V$  (PFM/PWM)   
 —  $V_{in} = 5.0V$  (PFM/PWM)

Figure 4 - DCDC1 Efficiency @ 25C

DCDC2 (Vout=1.2V) – VCCL\_GXB, VCCD\_PLL

DCDC2 Efficiency vs Load Current @ Ta=25°C

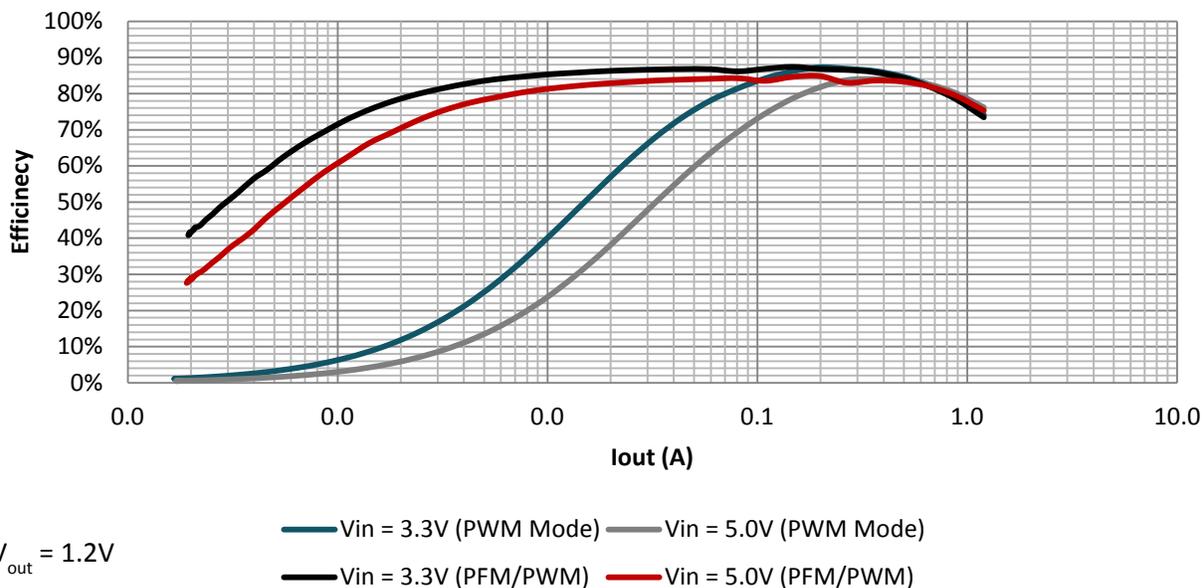


Figure 5 - DCDC2 Efficiency @ 25C

DCDC3 (Vout=2.5V) – VCCA, VCC\_CLKIN, VCCA\_GXB, VCCH\_GXB

DCDC3 Efficiency vs Load Current @ Ta=25°C

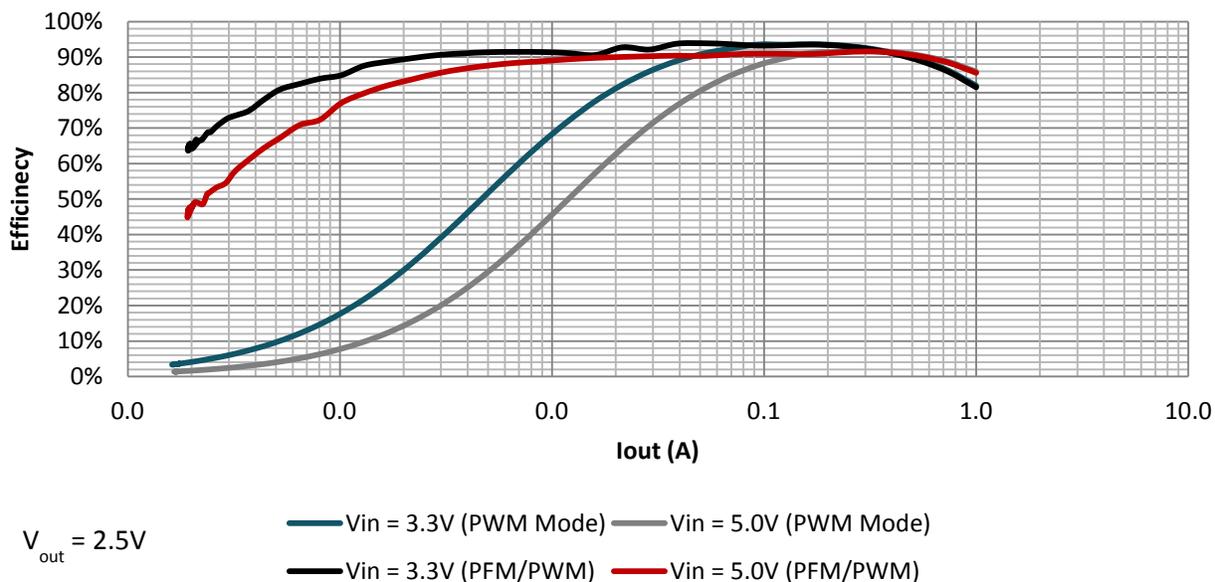


Figure 6 - DCDC3 Efficiency @ 25C

## Load Regulation [\(Return to Top\)](#)

DCDC1 ( $V_{out}=1.2V$ ) – VCC

### DCDC1 Load Regulation @ $T_a=25^\circ C$

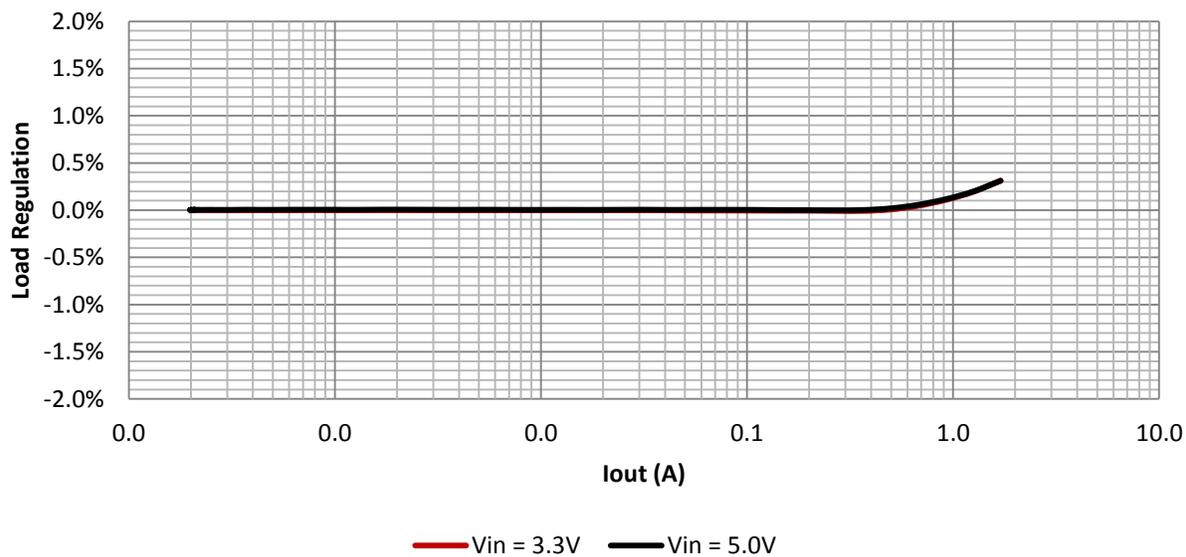


Figure 7 – DCDC1 Load Regulation @ 25C

DCDC2 ( $V_{out}=1.2V$ ) – VCCL\_GXB, VCCD\_PLL

### DCDC2 Load Regulation @ $T_a=25^\circ C$

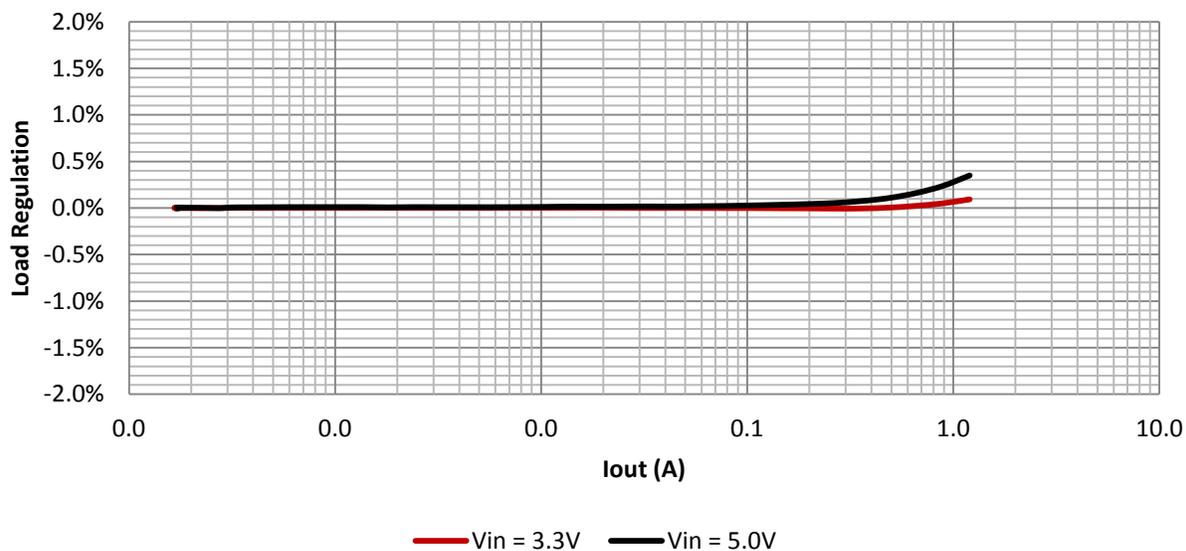


Figure 8 – DCDC2 Load Regulation @ 25C

DCDC3 (Vout=2.5V) – VCCA, VCC\_CLKIN, VCCA\_GXB, VCCH\_GXB

### DCDC3 Load Regulation @ Ta=25°C

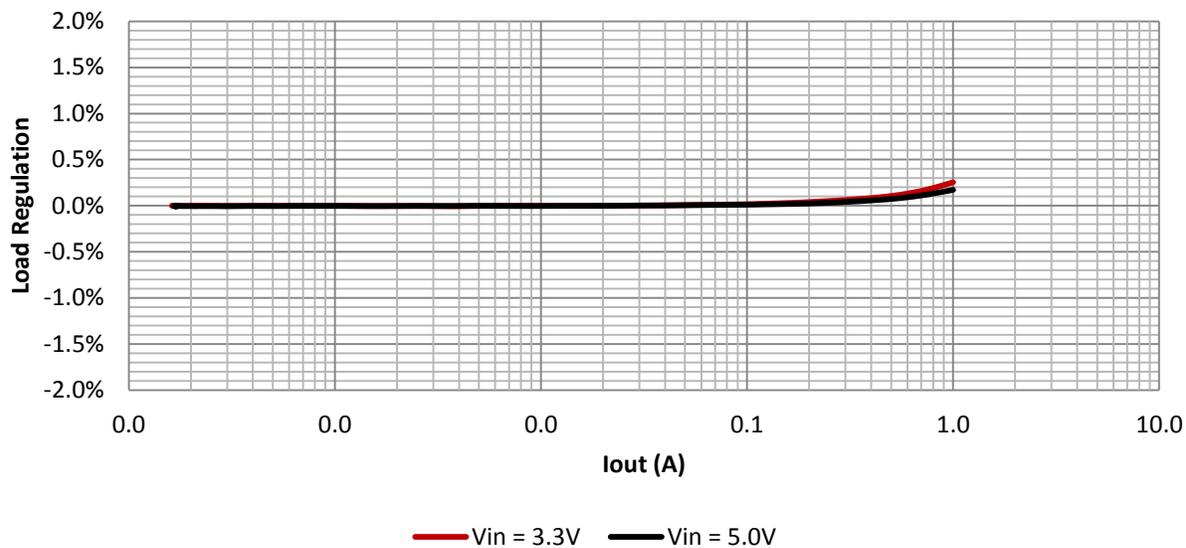
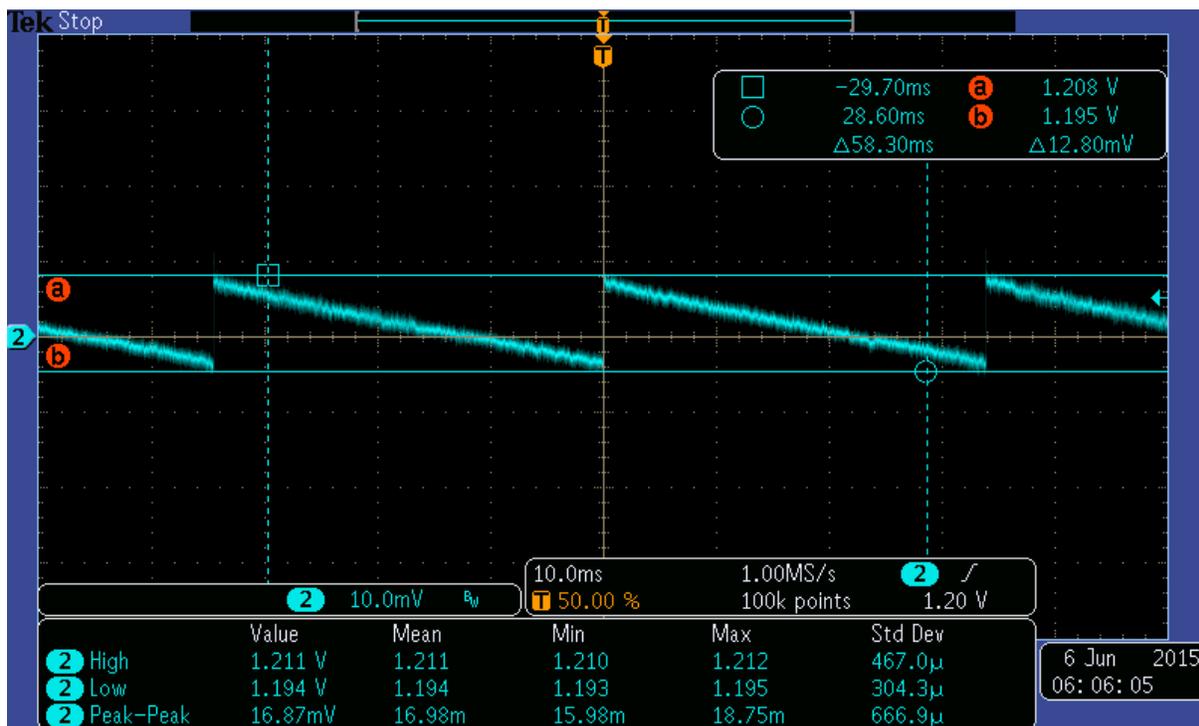


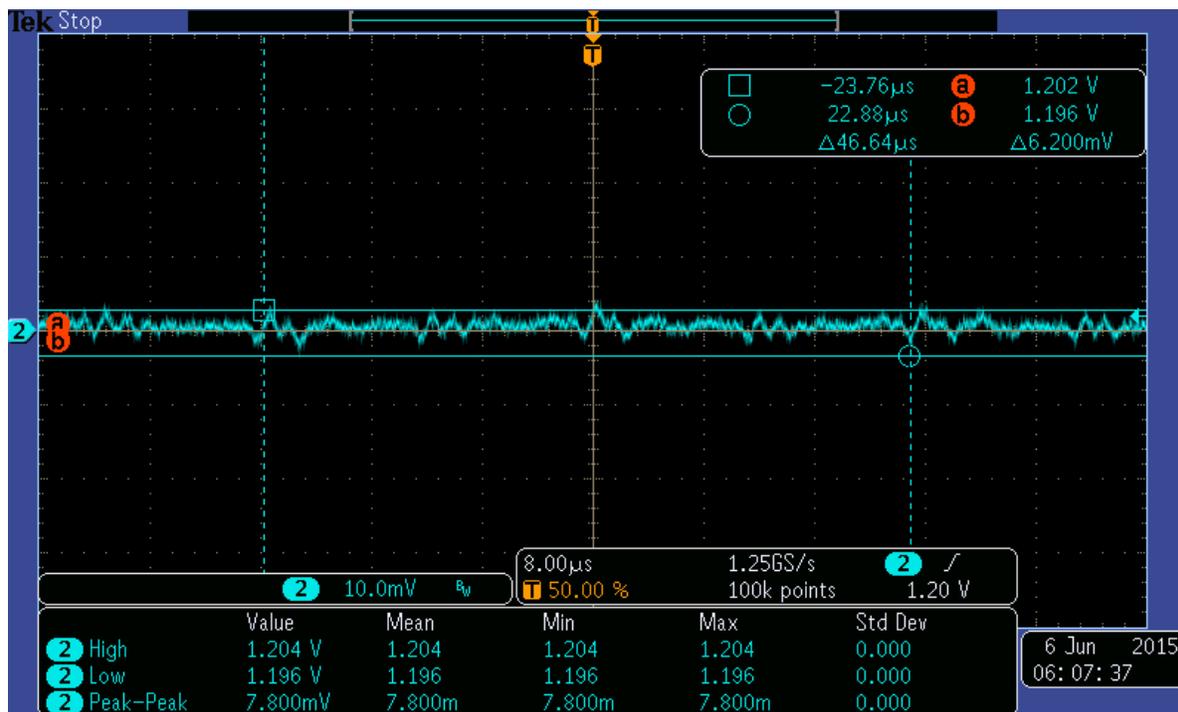
Figure 9 – DCDC3 Load Regulation @ 25C

### Output Ripple Voltage [\(Return to Top\)](#)

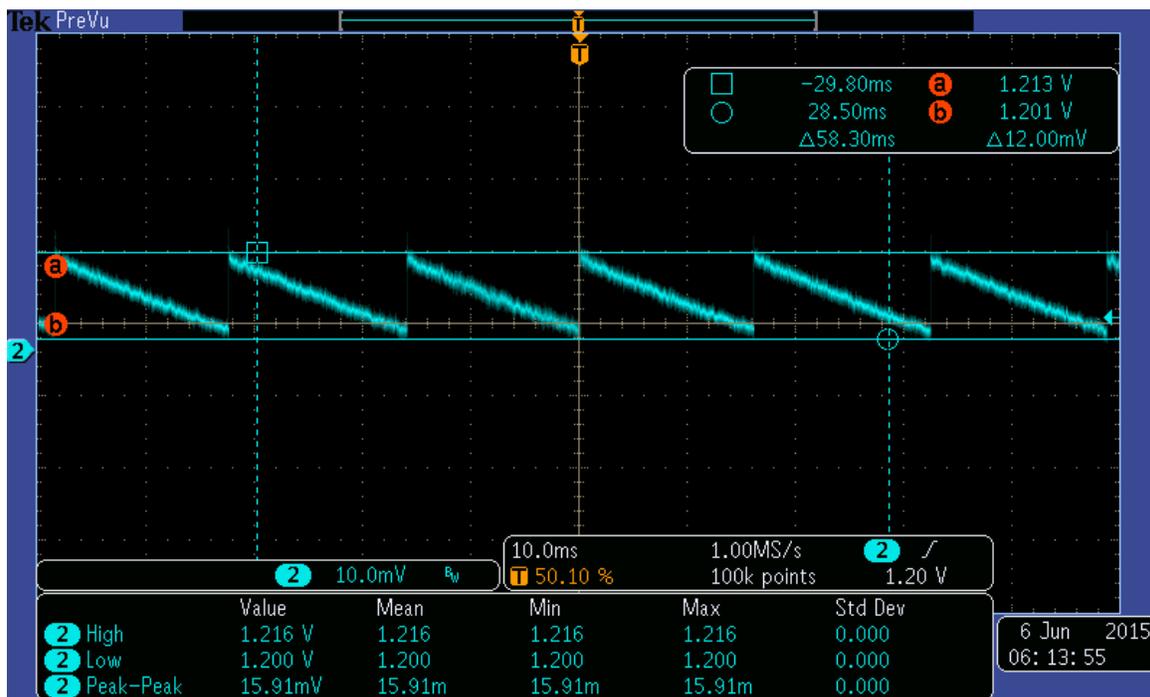
DCDC1 (Vout = 1.2V) – VCC (Light Load, PWM Mode)



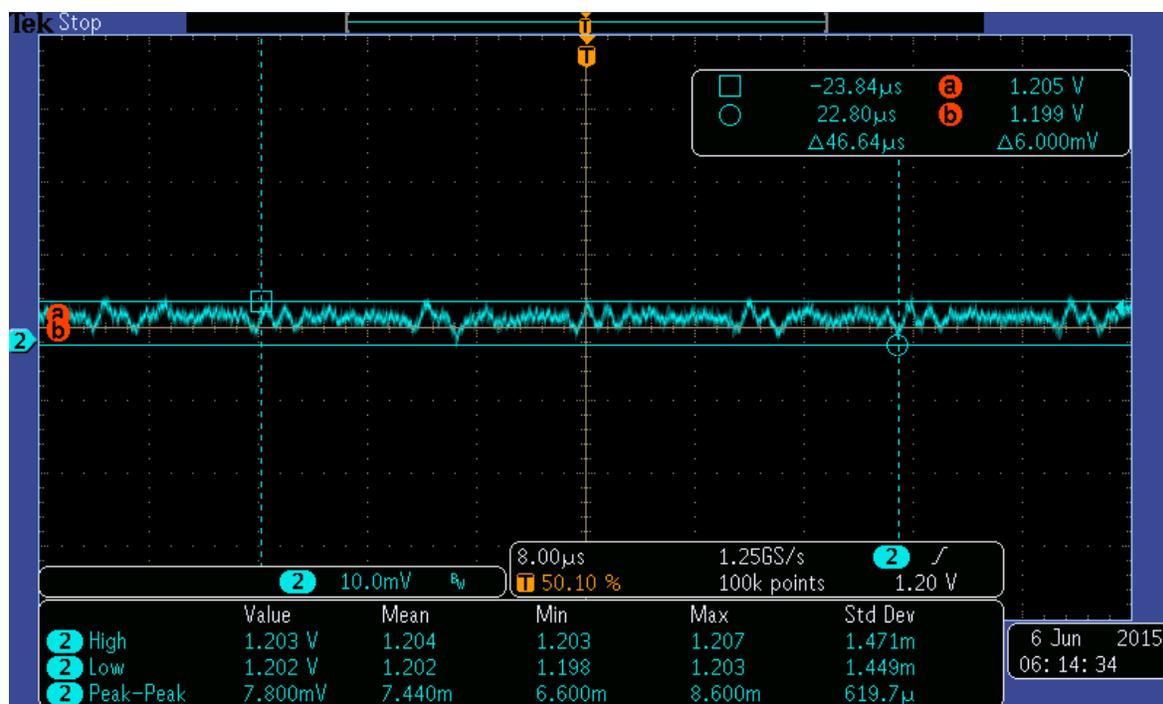
DCDC1 (Vout = 1.2V) – VCC (Max Typical Load)



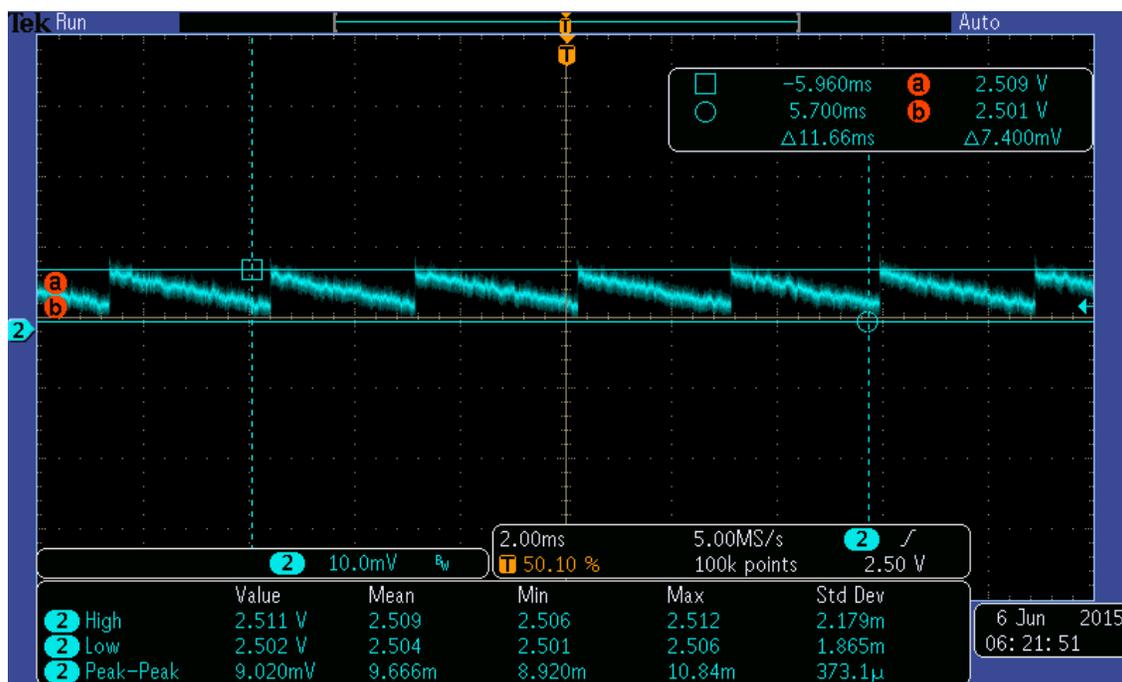
DCDC2 (Vout = 1.2V) – VCCL\_GXB, VCCD\_PLL (Light Load, PFM Mode)



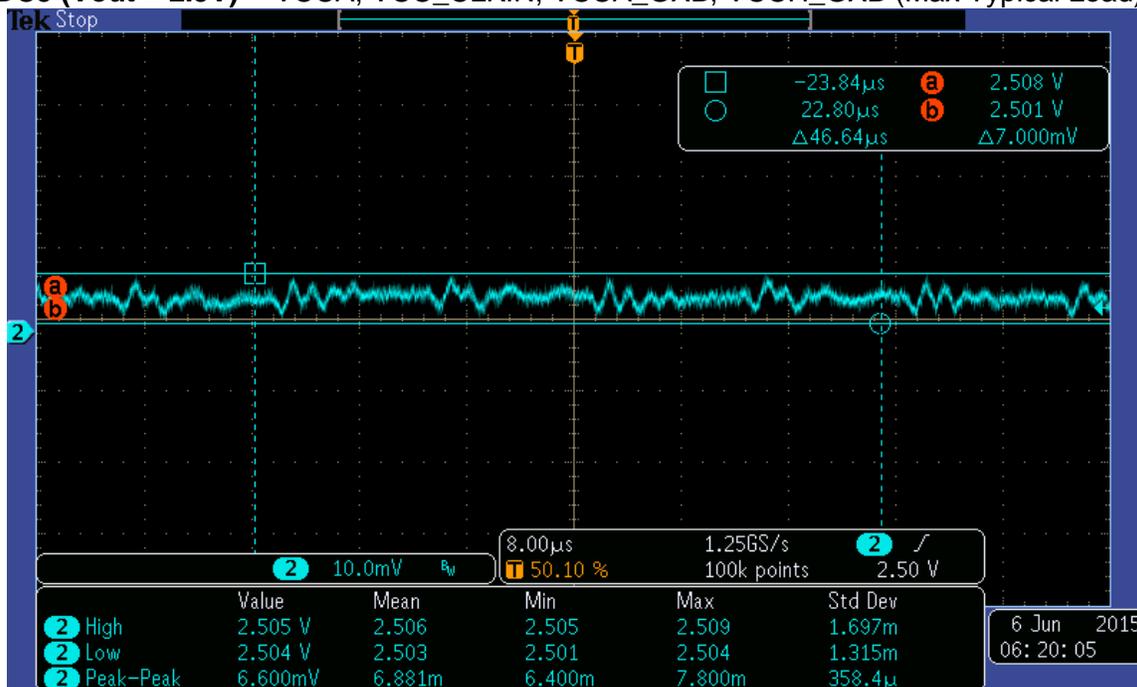
DCDC2 (Vout = 1.2V) – VCCL\_GXB, VCCD\_PLL (Max Typical Load)



DCDC3 (Vout = 2.5V) – VCCA, VCC\_CLKIN, VCCA\_GXB, VCCH\_GXB (Light Load, PFM Mode)



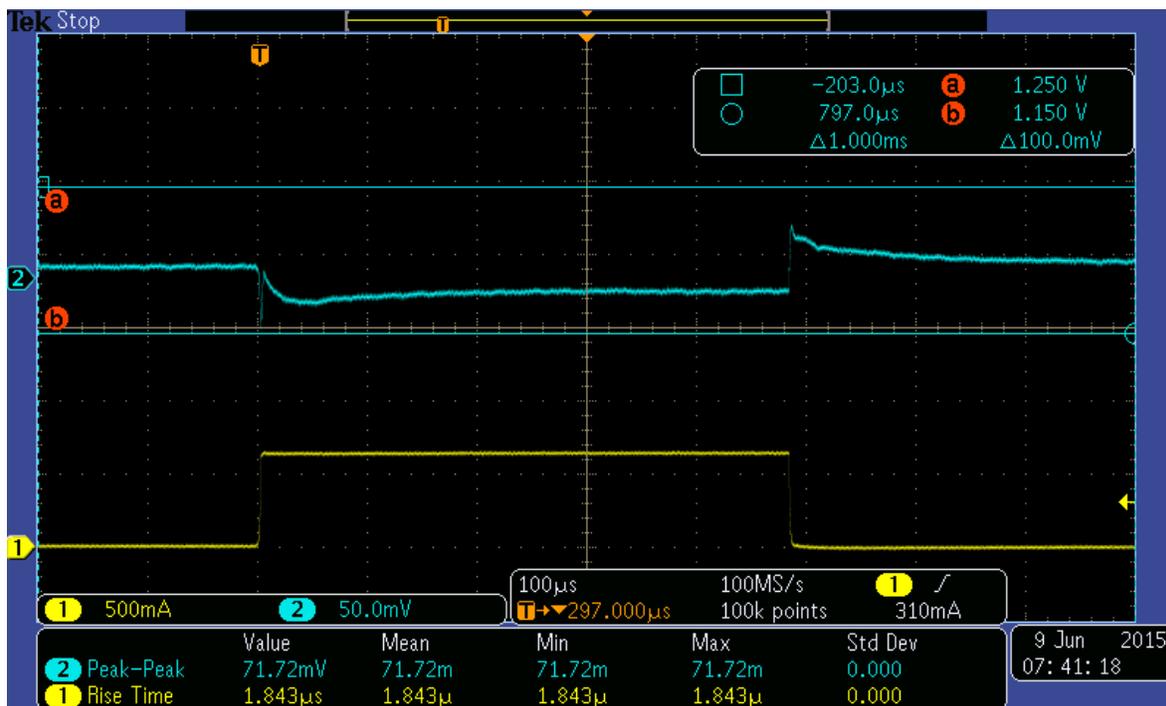
**DCDC3 (Vout = 2.5V) – VCCA, VCC\_CLKIN, VCCA\_GXB, VCCH\_GXB (Max Typical Load)**



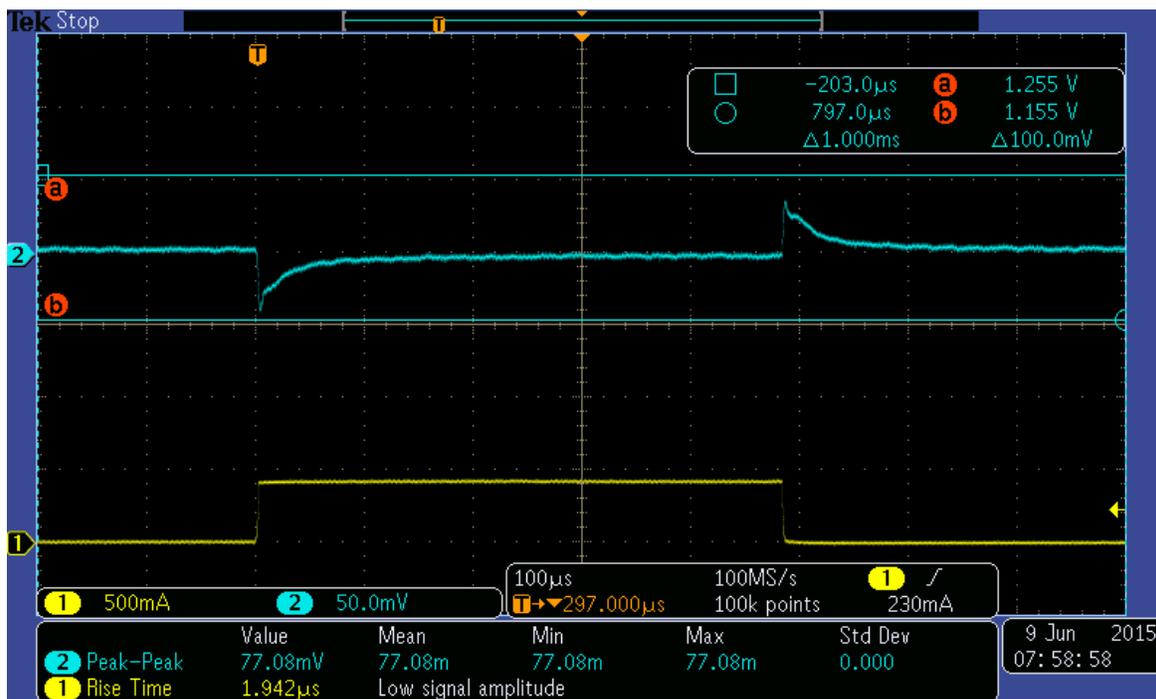
**Load Transients** ([Return to Top](#))

Load transients for each of the DC-DC converters were completed by applying a load step of 0mA to around 50% of the max load for the converter under test. Rise time and fall time were both set at 15µS. The regulators surpass specifications set for the Altera Cyclone Family.

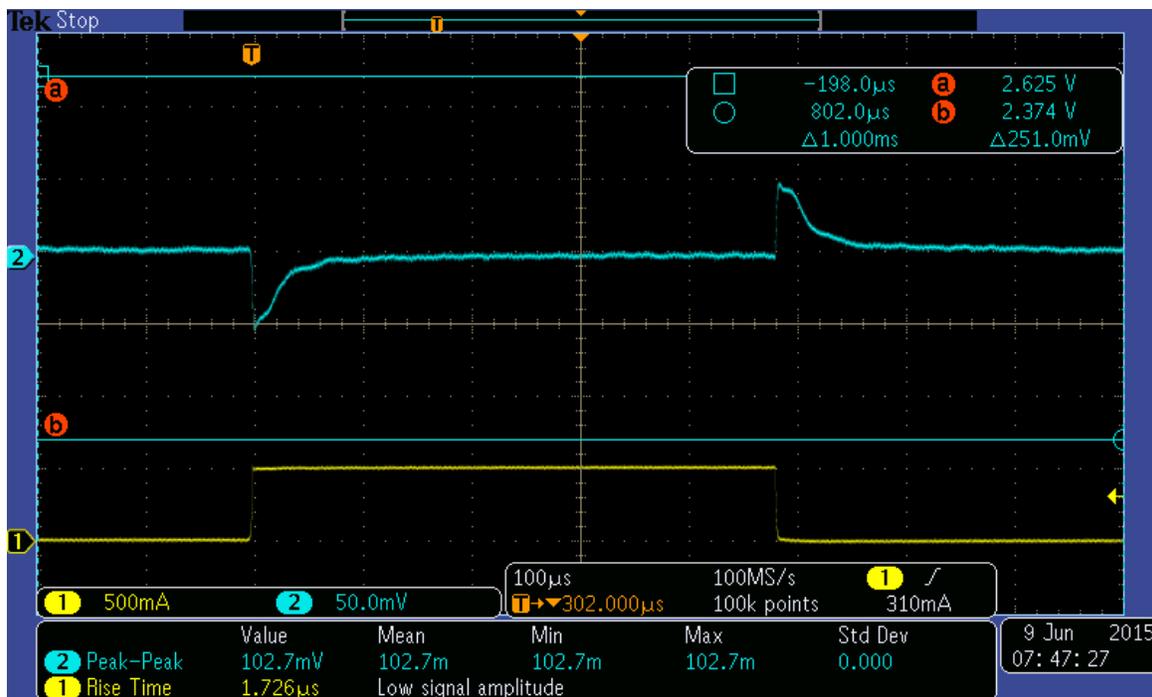
**DCDC1 (Vout = 1.2V) – VCC Load (0mA to 700mA, Rise Time: 15 $\mu$ S; Fall Time:15 $\mu$ S)**



**DCDC2 (Vout = 1.2V) – VCCL\_GXB, VCCD\_PLL Load Step (0mA to 500mA, Rise Time: 15 $\mu$ S; Fall Time:15 $\mu$ S)**



**DCDC3 (Vout = 1.5V) – VCCA, VCC\_CLKIN, VCCA\_GXB, VCCH\_GXB Load Step (0mA to 500mA, Rise Time: 15 $\mu$ S; Fall Time:15 $\mu$ S)**



## Design Considerations [\(Return to Top\)](#)

### Altera® Cyclone® IV Recommended Power Considerations

For reference, the power requirements from the Altera Cyclone IV datasheet are shown below:

<b>Power Supply</b>	<b>Description</b>
V <sub>CCINT</sub>	Core voltage power supply
V <sub>CCA</sub>	PLL analog power supply
V <sub>CCD_PLL</sub>	PLL digital power supply
V <sub>CCIO</sub>	I/O banks power supply
V <sub>CC_CLKIN</sub>	Differential clock input pins power supply
V <sub>CCH_GXB</sub>	Transceiver output (TX) buffer power supply
V <sub>CCA_GXB</sub>	Transceiver physical medium attachment (PMA) and auxiliary power supply
V <sub>CCL_GXB</sub>	Transceiver PMA and auxiliary power supply

### Power Sequencing Requirements

The signals can be driven into the I/O pins before or during power up or power down without damaging the device. Cyclone IV devices support power up or power down of the V<sub>CCINT</sub>, V<sub>CCA</sub>, and V<sub>CCIO</sub> pins in any sequence to simplify the system level design. The individual power supply ramp-up and ramp-down rates can range from 50  $\mu$ s to 50 ms. The power ramp must be monotonic.

Although power sequencing is not a requirement for correct operation, Altera recommends considering the power-up timing of each rail to prevent problems with long-term device reliability when designing a multi-rail powered system. You can reduce the device in-rush current with proper sequencing and voltage regulator design.

### Decoupling Capacitors

For each power supply, you must choose a network of bulk and ceramic decoupling capacitors. Cyclone IV devices include on-die decoupling capacitors to provide high-frequency decoupling. These low-inductance capacitors suppress power noise for excellent signal integrity performance and reduce the number of external PCB decoupling capacitors, saving board space, reducing cost, and greatly simplifying the PCB design.

### TPS65023 Power Sequencing

Though the Altera Cyclone IV does not require a specific power sequencing to ensure proper power up and power down, the TPS65023 offers flexible, customer driven power sequencing. This is achieved by providing separate enable pins for each switch-mode converter and a common enable signal for the LDOs. The table below shows the Pins used in the TPS65023 to create a customized, customer driven power sequence.

PIN NAME	I/O	FUNCTION
DEFDCDC3	I	Defines the default voltage of the VDCDC3 switching converter. DEFDCDC3 = 0 defaults VDCDC3 to 1.8 V, DEFDCDC3 = VCC defaults VDCDC3 to 3.3 V.
DEFDCDC2	I	Defines the default voltage of the VDCDC2 switching converter. DEFDCDC2 = 0 defaults VDCDC2 to 1.8 V, DEFDCDC2 = VCC defaults VDCDC2 to 3.3 V.
DEFDCDC1	I	Defines the default voltage of the VDCDC1 switching converter. DEFDCDC1 = 0 defaults VDCDC1 to 1.2 V, DEFDCDC1 = VCC defaults VDCDC1 to 1.6 V.
DCDC3_EN	I	Set DCDC3_EN = 0 to disable and DCDC3_EN = 1 to enable the VDCDC3 converter
DCDC2_EN	I	Set DCDC2_EN = 0 to disable and DCDC2_EN = 1 to enable the VDCDC2 converter
DCDC1_EN	I	Set DCDC1_EN = 0 to disable and DCDC1_EN = 1 to enable the VDCDC1 converter
HOT_RESET	I	The $\overline{\text{HOT\_RESET}}$ pin generates a reset ( $\overline{\text{RESPWRON}}$ ) for the processor. $\overline{\text{HOT\_RESET}}$ does not alter any TPS65023, TPS65023B settings except the output voltage of VDCDC1. Activating $\overline{\text{HOT\_RESET}}$ sets the voltage of VDCDC1 to its default value defined with the DEFDCDC1 pin. $\overline{\text{HOT\_RESET}}$ is internally de-bounced by the TPS65023, TPS65023B.
RESPWRON	O	RESPWRON is held low when power is initially applied to the TPS65023, TPS65023B. The VRTC voltage is monitored: RESPWRON is low when VRTC < 2.4 V and remains low for a time defined by the external capacitor at the TRESPWRON pin. RESPWRON can also be forced low by activation of the $\overline{\text{HOT\_RESET}}$ pin.
TRESPWRON	I	Connect a capacitor here to define the RESET time at the $\overline{\text{RESPWRON}}$ pin (1 nF typically gives 100 ms).

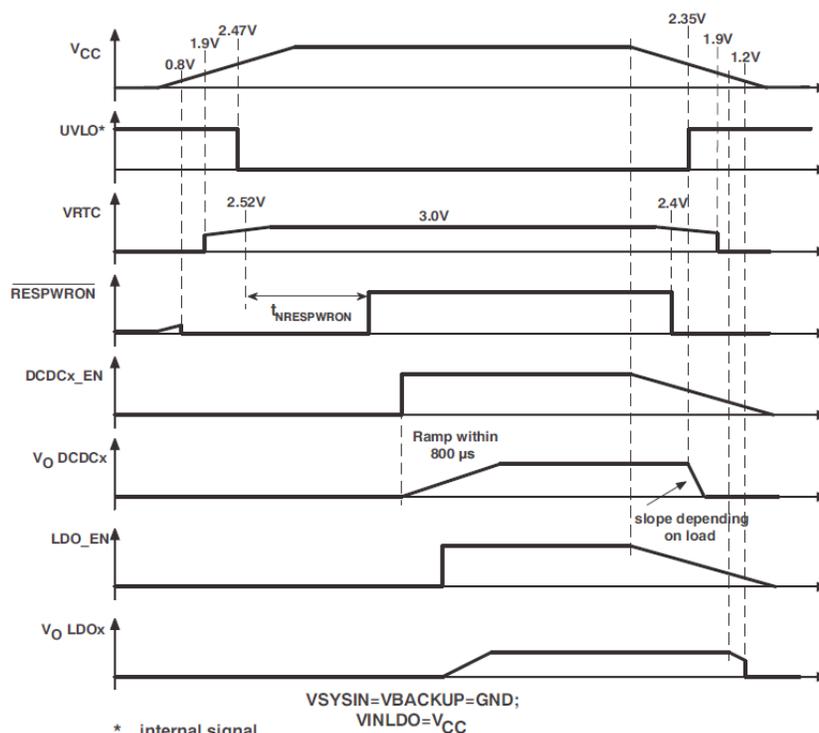


Figure 10 – TPS65023 Example Startup Sequence

### Inductor Selection for Buck Converters:

Each of the converters in the TPS65023, TPS65023B typically use a 2.2 µH output inductor. Larger or smaller inductor values are used to optimize the performance of the device for specific operation conditions. The selected inductor has to be rated for its dc resistance and saturation current. The dc resistance of the inductance influences directly the efficiency of the converter. Therefore, an inductor with lowest dc resistance should be selected for highest efficiency. For a fast transient response, a 2.2-µH inductor in combination with a 22-µF output capacitor is recommended. [The equation below](#) calculates the maximum inductor current under static load conditions. The saturation current of the inductor should be rated higher than the maximum inductor current as calculated with [the equation below](#). This is needed because during heavy load transient the inductor current rises above the value calculated.

$$\Delta I_L = V_{out} \times \frac{1 - \frac{V_{out}}{V_{in}}}{L \times f}$$

$$I_{Lmax} = I_{outmax} + \frac{\Delta I_L}{2}$$

with:

f = Switching Frequency (2.25 MHz typical)

L = Inductor Value

$\Delta I_L$  = Peak-to-Peak inductor ripple current

$I_{LMAX}$  = Maximum Inductor current

The following inductors have been used with the TPS6023:

Device	VALUE	TYPE	MANUFACTURER
All Converters	2.2 $\mu$ H, 2.5 A, 100 m $\Omega$	LPS4012-222LMB	Coilcraft
	2.2 $\mu$ H, 1.7 A, 59 m $\Omega$	VLCF4020T-2R2N1R7	TDK
For DCDC2 or DCDC3	2.2 $\mu$ H, 1.6 A, 90 m $\Omega$	LQH32PN2R2NN0	Murata
For DCDC1	1.5 $\mu$ H, 1.75 A, 68 m $\Omega$	LQH32PN1R5NN0	Murata
All Converters	2.2 $\mu$ H, 2.2 A, 80 m $\Omega$	PST25201B-2R2MS	Cyntec

### Output Capacitor Selection

TPS65023, TPS65023B allow the use of small ceramic capacitors with a typical value of 10  $\mu$ F for each converter without having large output voltage under and overshoots during heavy load transients. Ceramic capacitors having low ESR values have the lowest output voltage ripple and are recommended.

At light load currents, the converters operate in PSM and the output voltage ripple is dependent on the output capacitor value. The output voltage ripple is set by the internal comparator delay and the external capacitor. The typical output voltage ripple is less than 1% of the nominal output voltage.

CAPACITOR VALUE	CASE SIZE	COMPONENT SUPPLIER	COMMENTS
22 $\mu$ F	1206	TDK C3216X5R0J226M	Ceramic
22 $\mu$ F	1206	Taiyo Yuden JMK316BJ226ML	Ceramic
22 $\mu$ F	0805	TDK C2012X5R0J226MT	Ceramic
22 $\mu$ F	0805	Taiyo Yuden JMK212BJ226MG	Ceramic
10 $\mu$ F	0805	Taiyo Yuden JMK212BJ106M	Ceramic
10 $\mu$ F	0805	TDK C2012X5R0J106M	Ceramic

## Input Capacitor Selection

Because of the nature of the buck converter having a pulsating input current, a low ESR input capacitor is required for best input voltage filtering and minimizing the interference with other circuits caused by high input voltage spikes. Each dc-dc converter requires a 10- $\mu$ F ceramic input capacitor on its input pin VINDCDCx. The input capacitor is increased without any limit for better input voltage filtering. The VCC pin is separated from the input for the dc-dc converters. A filter resistor of up to 10R and a 1- $\mu$ F capacitor is used for decoupling the VCC pin from switching noise. Note that the filter resistor may affect the UVLO threshold since up to 3 mA can flow via this resistor into the VCC pin when all converters are running in PWM mode.

## Low Ripple Mode

Low ripple mode can be enabled over I2C for all the DCDC converters if operated in PFM mode. For an output current less than approximately 10 mA, the output voltage ripple in PFM mode is reduced, depending on the actual load current. The lower the actual output current on the converter, the lower the output ripple voltage. For an output current above 10 mA, there is only minor difference in output voltage ripple between PFM mode and low ripple PFM mode. As this feature also increases switching frequency, it is used to keep the switching frequency above the audible range in PFM mode down to a low output current.

## Power Supply Recommendations

The device is designed to operate with an input voltage supply range between 2.5V and 6.0V. This input supply can be from a single cell Li-Ion battery or other externally regulated supply. The low power section of the control circuit for the step-down converters DCDC1, DCDC2 and DCDC3 is supplied by the Vcc pin while the circuitry with high power such as the power stage is powered from the VINDCDC1, VINDCDC2 and VINDCDC3 pins. For proper operation of the step-down converters, VINDCDC1, VINDCDC2, VINDCDC3 and Vcc need to be tied to the same voltage rail. Step-down converters that are planned to be not used, still need to be powered from their input pin on the same rails than the other step-down converters and Vcc.

LDO1 and LDO2 share a supply voltage pin which can be powered from the Vcc rails or from a voltage lower than Vcc e.g. the output of one of the step-down converters as long as it is operated within the input voltage range of the LDOs. If both LDOs are not used, the VINLDO pin can be tied to GND.

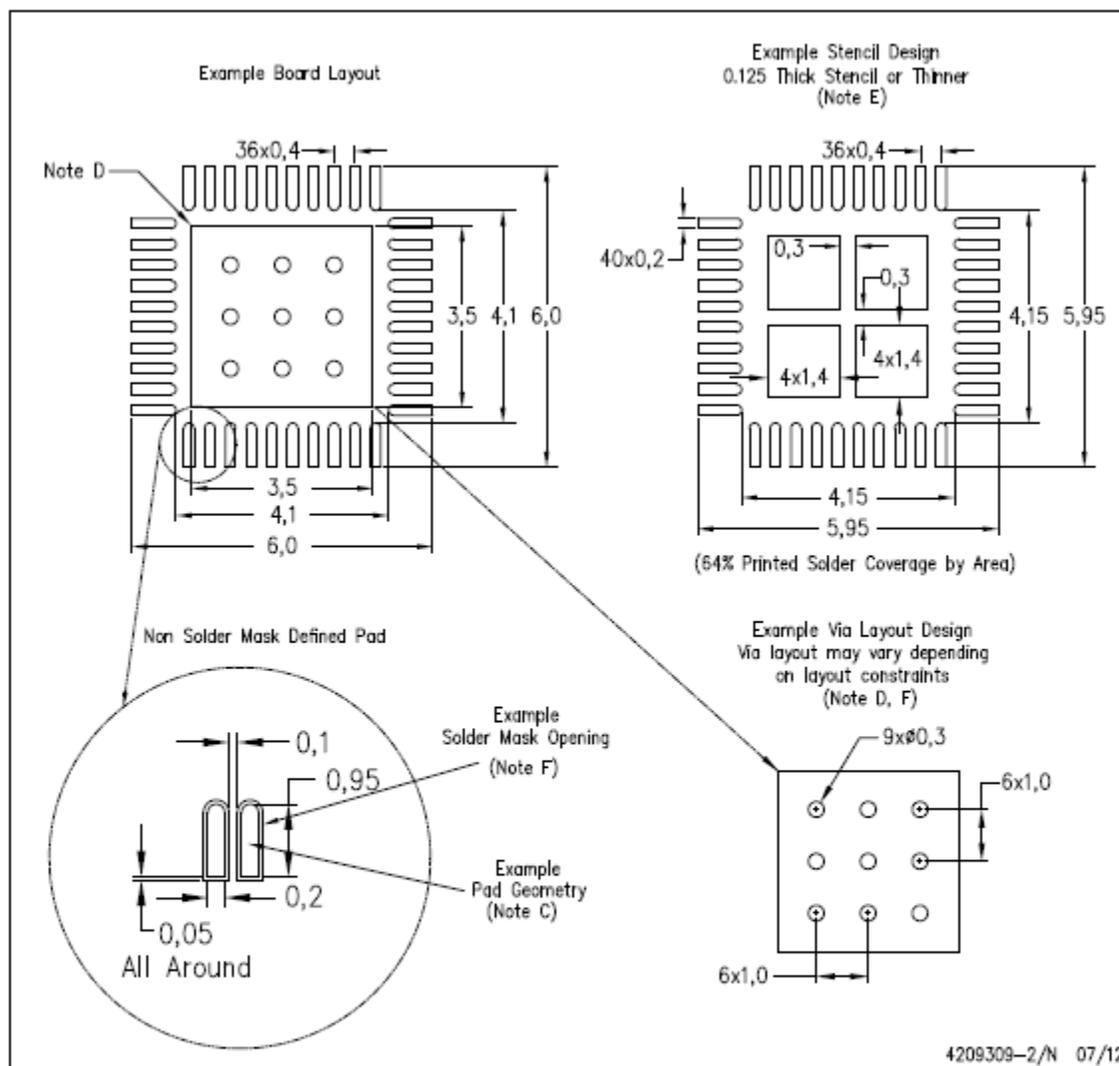
## Layout Guidelines

- Provide a low impedance ground path
  - Use wide and short traces for the main current paths.
- The input capacitors should be placed as close as possible to the IC pins as well as the inductor and output capacitor
- Connect the PGND pins of the device to the PowerPAD™ land of the PCB
- Connect the analog ground connections (AGND) to the PGND at the PowerPAD™
- Keep the common path to the AGND pins, which returns the small signal components, and the high current of the output capacitors as short as possible to avoid ground noise.
- The VDCDCx line should be connected right to the output capacitor and routed away from noisy components and traces

## QFN Package Information

RSB (S-PWQFN-N40)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. [SLUA271](#), and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.



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