

TI Designs – Precision: Verified Design Current Shunt & Voltage Measurement Reference Design for EV/HEV Automotive Battery Monitoring



TI Designs – Precision

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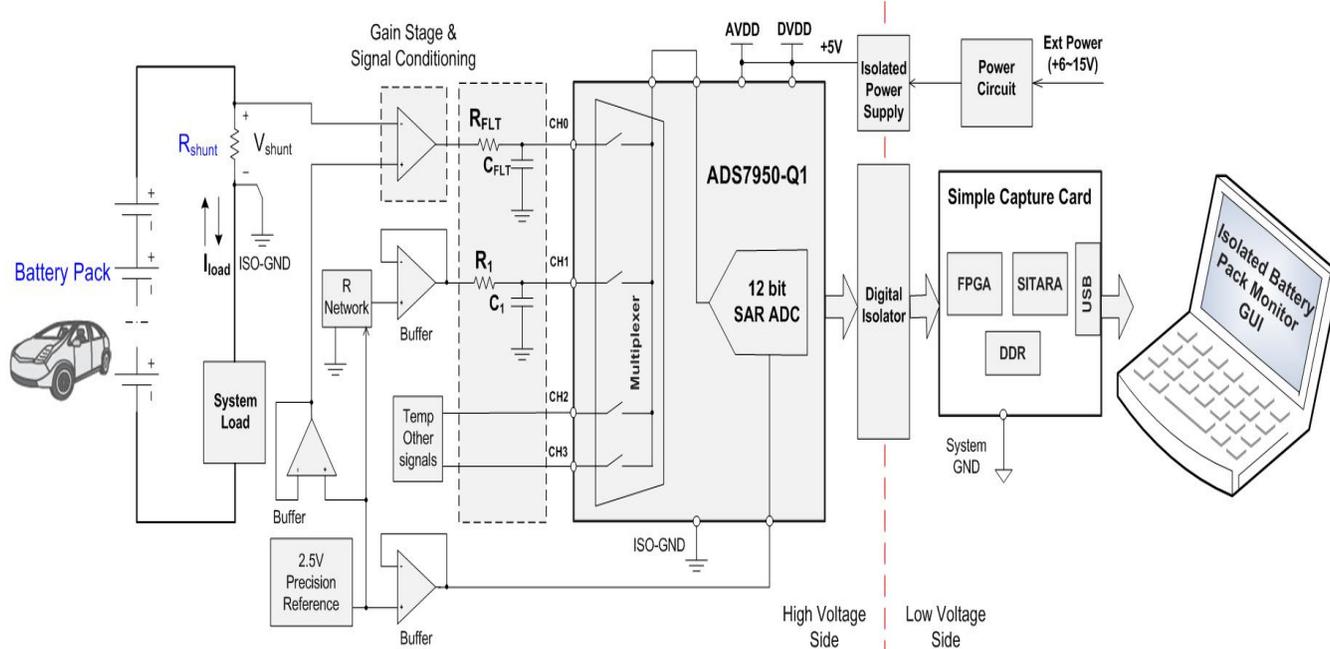
Design Resource

[TIPD201](#)
[TINA-TI™](#)
[ADS7950-Q1](#)
[OPA2320-Q1](#)
[REF5025A-Q1](#)
[ISO7240CF-Q1](#)
[ISO7242C-Q1](#)
[DCR010505](#)
[REG104](#)

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Circuit Description

Precision monitoring of battery current, voltage and temperature for a battery pack is necessary in an electric vehicles (EVs), hybrid electric vehicles (HEVs) or plug-in hybrid vehicles (PHEVs). This TI precision design describes an isolated measurement system using an automotive qualified, multi-channel precision successive approximation register (SAR) based analog to digital converter (ADC), ADS7950-Q1 along with digital isolators and an isolated power supply. This isolated input design with four-wire shunt is well suited for such applications using high and low voltage automotive battery packs. It can be used to monitor the current from -5 to +5A and extremely high voltage (up to 750V) of automotive battery.



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1 Design Summary

The primary objective for this design is to accurately measure the output current and higher output voltage of a battery pack in an automotive system.

The key design requirements are as follows:

- Isolated Sense Current (bidirectional): -5A to +5A
- Accuracy for Current Measurement (in %FSR): 0.05%FSR
- Isolated Measurable Voltage: DC to 750V
- Accuracy for Voltage Measurement (in %FSR): 0.05%FSR

This design goals and performance are summarized in [Table 1](#). [Figure 1](#) depicts the measured current error for higher common-mode voltage of the design¹.

Table 1: Comparison of Theoretical and Measured Performance

Parameter	Goal	Measured Value	Remark for Measured Result
Current Measurement Error (%FSR, Calibrated)	0.05	0.024	Maximum Positive Error
		-0.030	Maximum Negative Error
Voltage Measurement Error (%FSR, Uncalibrated)	0.05	0.035	Maximum Error

1. The tests were implemented with 100V common mode voltage limited by the test equipments.

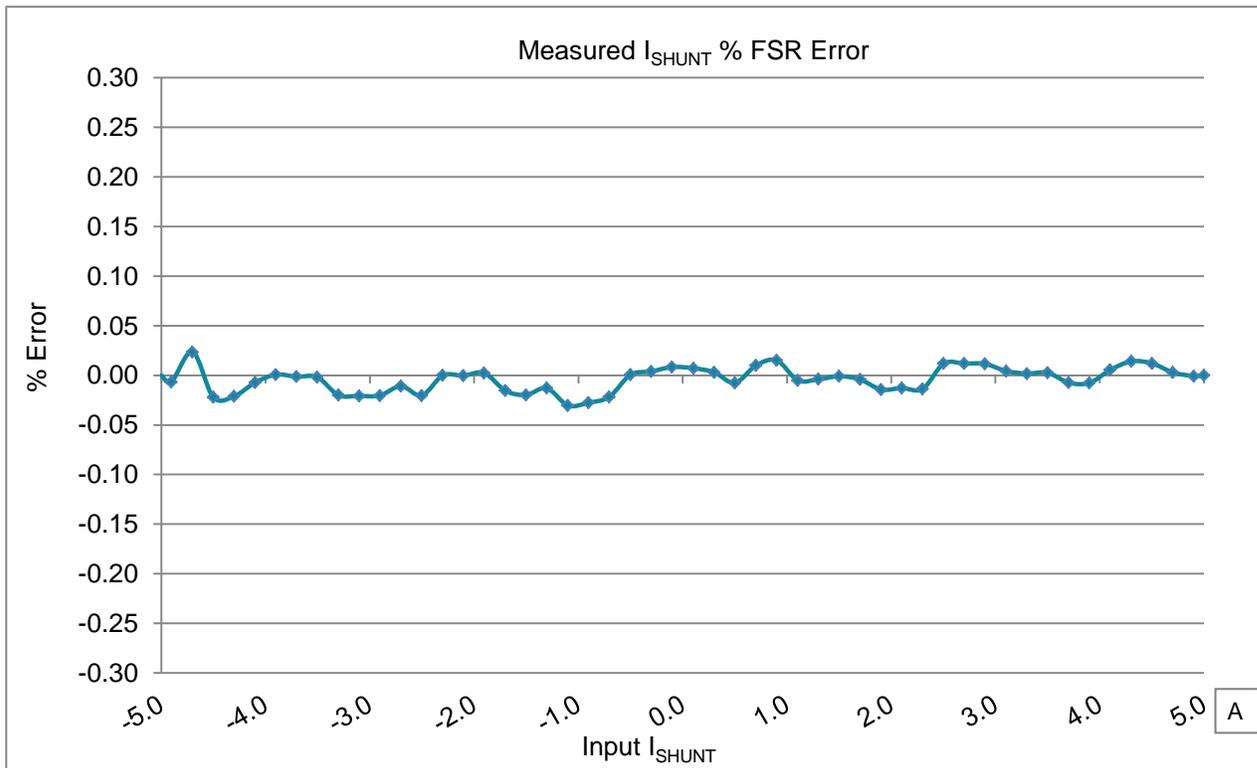


Figure 1: Measured System Error for Isolated Current Measurement ($V_{CM}=100V$)

2 Theory of Operation

Electric vehicles (EVs), hybrid electric vehicles (HEVs) and plug-in hybrid vehicles (PHEVs) are becoming very popular. These vehicles provide several performance and ecological advantages over conventional vehicles. Most EV/HEV/PHEV vehicles implement a stack of batteries containing many cells. The voltage level of the battery stacks will vary depending on the vehicle's requirements set by the manufacturers. A real time monitoring system of the battery stack is necessary to prevent the discharge of the car battery beyond a point where it can be used to restart the car. The battery output current and battery voltage must also be measured in this kind of monitoring system to diagnose any fault conditions.

This design provides a unique solution of current monitoring and voltage measurement with an isolated acquisition system for this automotive battery pack application. In this design, the input battery current is transformed into an analog voltage signal with a precision current shunt resistor. The sensed voltage across the shunt is amplified and adjusted by a precision signal conditioning circuit and then fed into the multichannel inputs of an automotive AEC-Q100 qualified successive approximation register (SAR) analog-to-digital converter (ADC), ADS7950-Q1. The current measurement path is shown in the red dotted line box of Figure 2.

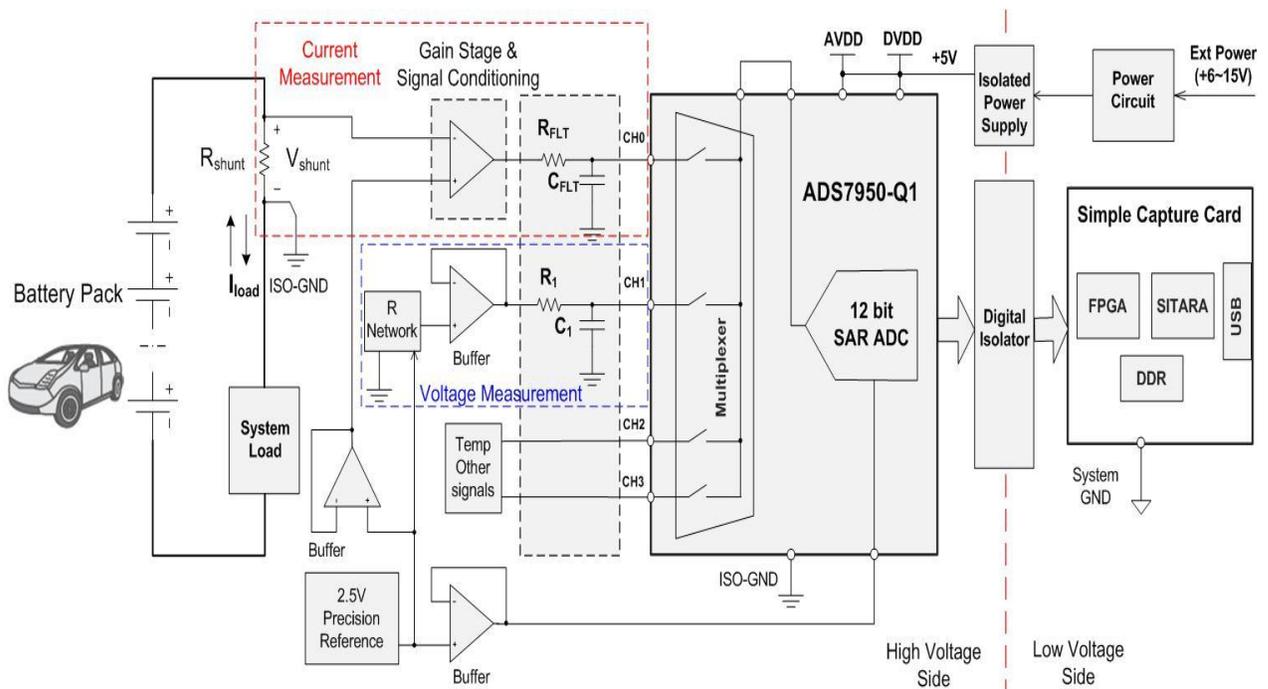


Figure 2: Isolated Battery Pack Monitoring System

A second input channel (CH1) of ADS7950-Q1 is used to measure the high common-mode voltage (battery voltage). This voltage measurement path is shown in the blue dotted line box of Figure 2. One of the remaining channels (CH2 and CH3) of the device can be used to measure the battery stack's temperature for temperature compensation or over temperature monitoring. The last channel (CH2 or CH3) can be used as a power supply monitoring circuit by measuring the output voltage of a resistor divider between an isolated +5V analog power supply and ground. The Simple Capture Card from Texas Instruments is a digital interface board between the test board and a laptop or PC with monitor graphical user interface (GUI) software for further data analysis.

2.1 Isolated Current Shunt Measurement

One of the most popular current measurement methods is to use a precision current shunt resistor. By definition it is the most accurate and linear method of current measurement and widely used in automotive, power control, and industrial systems.

When inserting a known shunt resistor (R_{shunt}) into the current loop, the current (I_{load}) will flow through the shunt and generate a voltage drop across the shunt resistor (V_{shunt}) that is proportional to the value of the shunt resistor. This differential voltage drop on the shunt resistor can be measured by a data acquisition circuit, and then the expected current can be calculated using Equation (1):

$$I_{load} = \frac{V_{shunt}}{R_{shunt}} \tag{1}$$

In addition to the current measurement accuracy for the automotive battery pack, another design challenge is to measure the current with the high common-mode voltage generated by the battery pack and system load for high side current sensing, which is usually in the order of several hundreds of volts.

This design introduces an isolated system for measuring bipolar current, being supplied by or sourced, to the battery pack. It also accounts for high input common-mode voltage by designing the acquisition system using floating power supplies. The block diagram is shown in Figure 3.

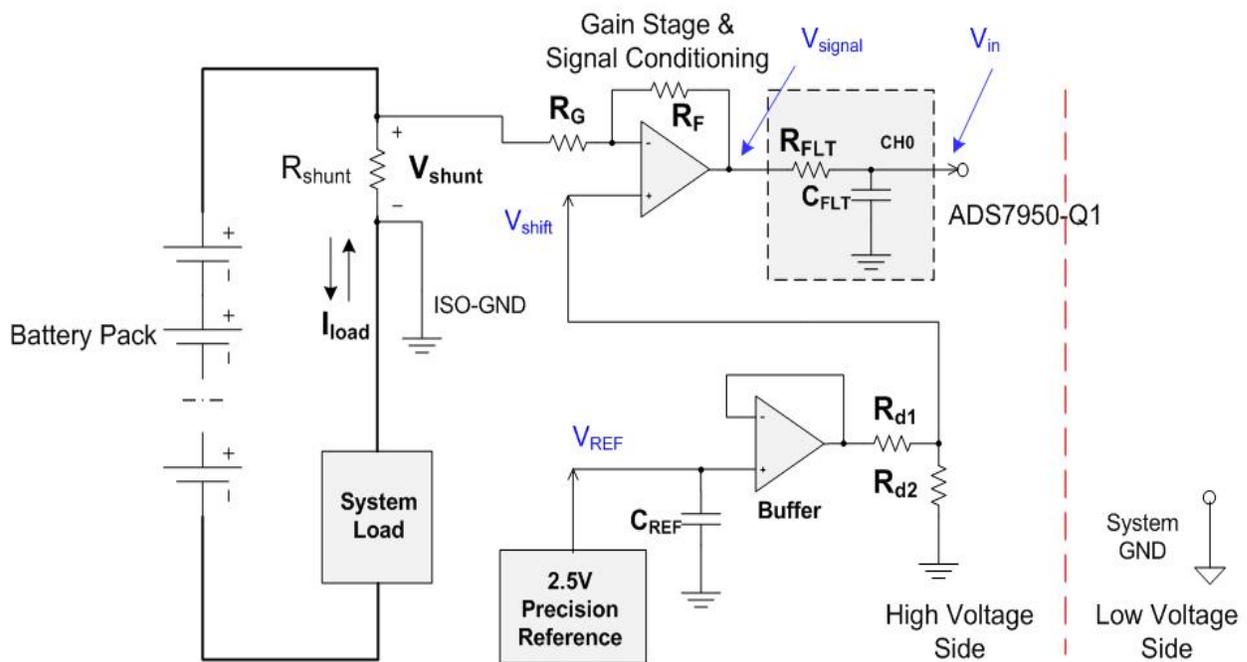


Figure 3: Isolated Current Shunt Measurement

2.1.1 Shunt Resistor Stage

The differential voltage output across the shunt resistor when a load current, I_{load} is flowing through it can be represented by Equation (1).

The polarity of voltage V_{shunt} can be positive or negative depending on the charging or discharging status of the battery pack.

2.1.2 Gain and Signal Conditioning Stage

In order to utilize the maximum input dynamic range of ADC, this sensed differential voltage (V_{shunt}) signal needs to be amplified and adjusted to meet the ADC input requirement. This requires a precision amplifier, used in a non-inverting configuration for signal amplification and conditioning as shown in Figure 3.

The voltage (V_{signal}) at the output of the signal conditioning circuit is given by:

$$V_{signal} = V_{shunt} \times \left(-\frac{R_F}{R_G} \right) + V_{shift} \times \left(1 + \frac{R_F}{R_G} \right) \quad (2)$$

$$Gain_{signal} = -\frac{R_F}{R_G} \quad (3)$$

Where, V_{shift} is the shift voltage and comes from the resistance divider by precision reference voltage.

$$V_{shift} = V_{REF} \times \frac{R_{d2}}{R_{d1} + R_{d2}} \quad (4)$$

$$V_{signal} = V_{shunt} \times \left(-\frac{R_F}{R_G} \right) + V_{REF} \times \frac{R_{d2}}{R_{d1} + R_{d2}} \times \left(1 + \frac{R_F}{R_G} \right) \quad (5)$$

2.1.3 RC-Filter

A low pass resistor–capacitor (RC) filter is necessary between the SAR ADC and signal conditioning stage. This RC-filter can act as anti-aliasing filter to reject any unwanted signals and noise with frequencies outside the band of interest. The voltage sampled at the input of the ADC must be settled within $\frac{1}{2} \times \text{LSB}$ (least significant bit) during the acquisition time. The capacitor C_{FLT} of RC-filter helps to reduce the kick-back noise on the switched-capacitor input of SAR ADC and also provides a “charge bucket” to quickly charge the input sampling capacitor (C_{SH}) during the sampling process. To meet these requirements, generally the C_{FLT} can be determined by equation (Reference 1):

$$C_{FLT} \geq 20 \times C_{SH} \quad (6)$$

A higher value of C_{FLT} implies better attenuation against the ADC kick-back noise and better effect of RC-filter. However, it may degrade the phase margin of the driving amplifier, thus making it unstable. This may result in settling issues with the input signal, leading to larger error with higher sampling rate of ADC. The series resistor R_{FLT} acts as an isolation resistor to stabilize the driving amplifier.

$$\frac{1}{R_{FLT} \times C_{FLT}} = \frac{1}{\tau} \geq \frac{\ln \left[\frac{2 \times V_{FSR}}{\text{LSB}} \right]}{t} \quad (7)$$

Where, $t = t_{ACQ}$, V_{FSR} is the full scale range of ADC.

A combination of Equation (6) and Equation (7) can be used to determine the value of R_{FLT} .

The -3dB cut-off frequency for this front-end low pass RC-filter can be calculated using Equation (8):

$$f_{FLT_3dB} = \frac{1}{2\pi R_{FLT} \times C_{FLT}} \quad (8)$$

2.1.4 Amplifier in Gain Stage

The amplifier selection is highly dependent on the input signal and the sampling rate of the ADC. Referring to the discussion in Section 2.1.2, the current measurement accuracy is highly limited by the amplifier in this stage. Hence, an appropriate precision amplifier is necessary for high accuracy current shunt measurement. The key specifications for the amplifier selection are listed as follow:

- **Low Input Offset:** Input offset voltage is typically the biggest factor affecting the system's accuracy for measuring current. This is because the shunt output voltage is generally very small, generally of the order of 10~ 100mV, due to which the amplifier offset, has a big impact on the measurement accuracy.
- **Low Offset Drift:** Offset drift is critical to maintain the system accuracy over temperature. It is also important to minimize drift because calibrating drift error is very complicated and may require additional hardware.
- **Low Bias Current:** The input bias current of the amplifier will affect the current that flows through the shunt, thus affecting the voltage drop across the shunt. Hence, it is preferred to use amplifiers with low input bias current for system accuracy.
- **Low Noise:** The inherent noise of amplifier can also affect the measurement accuracy, especially when configuring the amplifier with higher noise gain.
- **Small-Signal Bandwidth:** This bandwidth should guarantee no attenuation of the input signal. In general, the amplifier should be selected based on Equation (9):

$$Unity - GainBandwidth \geq 4 \times \frac{1}{2\pi R_{FLT} \times C_{FLT}} \quad (9)$$

- **Rail-to-rail input and output:** This design completely utilizes the full scale voltage swing range of ADC, therefore an amplifier supporting rail-to-rail input and output (RRIO) ability is needed.

2.2 Isolated High Voltage Measurement

Direct measurement of the battery pack voltage may be extremely challenging because these packs of individual cells may contain many units. According to the cell configurations, the battery packs may have potentials of several hundreds of volts. In such systems it is often desirable to measure the voltage of each individual cell, but it complicates the overall system design. This precision design introduces a direct high voltage measurement method for battery packs in the automotive application. The high voltage common mode output of the battery stack is eliminated by creating isolated power supplies using the same common mode voltage. As a result, the measured battery voltage is independent of the common mode voltage, hence it relaxes the requirement to make use of high common mode voltage difference amplifier or current shunt monitor in this design.

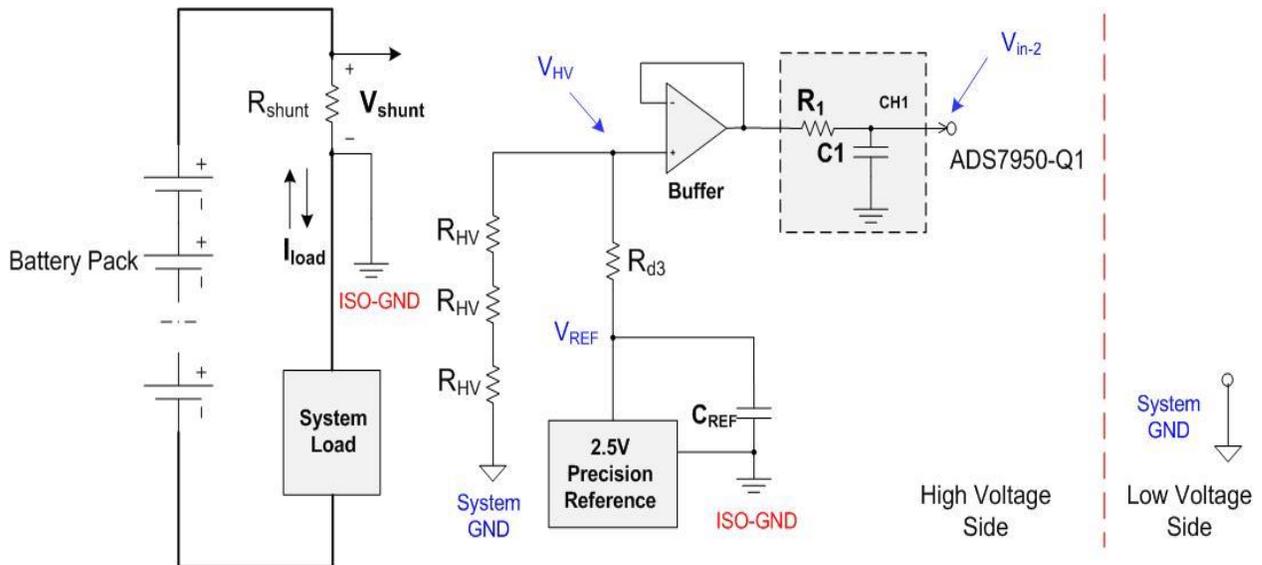


Figure 4: Isolated High Voltage Measurement

The direct solution of measuring high voltage is shown in above Figure 4. It's achieved by the resistor divider made up of three same value individual resistors (R_{HV}) and one smaller resistor (R_{d3}) between the isolated ground (ISO-GND) and the ground (System GND) which is non-isolated ground of the system.

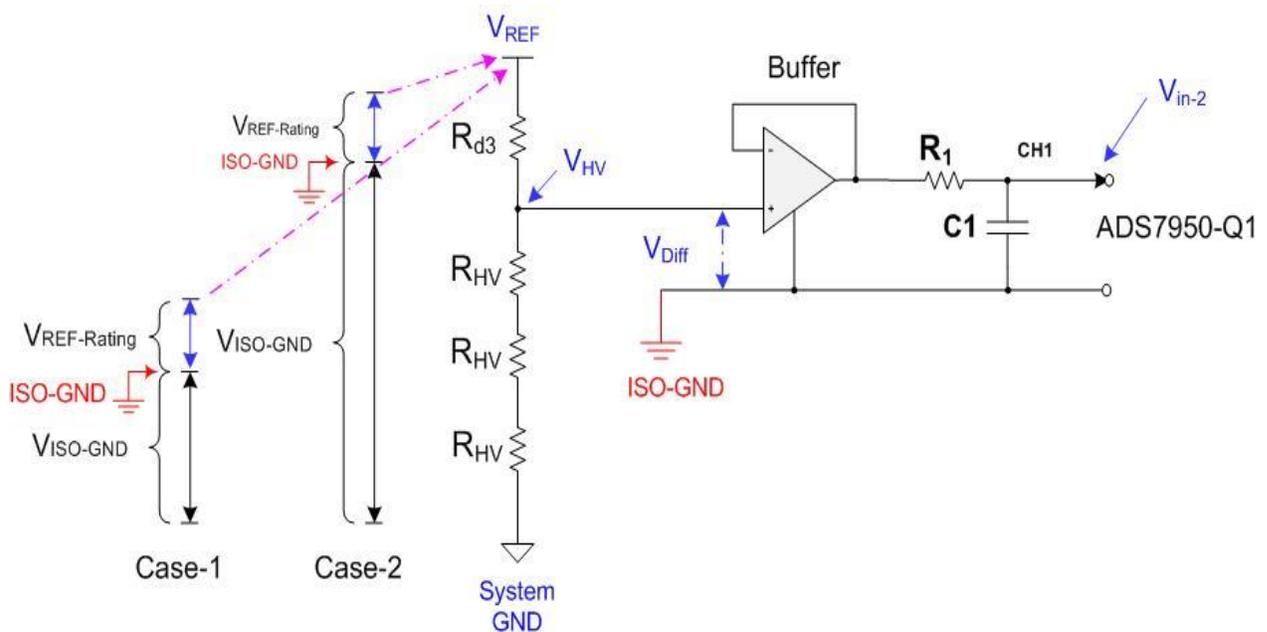


Figure 5: Simplified Schematic for High Voltage Measurement

Figure 5 shows a simplified schematic from above figure, V_{REF_Rating} is the rated output voltage of voltage reference, for instance, if the voltage reference is 2.5V reference, $V_{REF_Rating} = 2.5V$. $V_{ISO-GND}$ is the absolute voltage of the isolated ground of the board which changes with the voltage of battery pack ($V_{Battery}$). Because V_{Shunt} is a small voltage, $V_{Battery}$ is roughly equal to $V_{ISO-GND}$. The absolute voltage of V_{REF} referenced to the system GND is the sum of V_{REF_Rating} and $V_{ISO-GND}$. Whether the voltage of $V_{ISO-GND}$ is low or high (Case-1 and Case-2) shown in Figure 5, V_{REF} can be calculated by the equation:

$$V_{REF} = V_{ISO-GND} + V_{REF_Rating} \quad (10)$$

This V_{REF} is always divided by the resistor divider made up of three resistors (R_{HV}) and a resistor (R_{d3}). The absolute divided voltage at the dividing point is shown in Equation (11):

$$V_{HV} = \frac{3R_{HV}}{3R_{HV} + R_{d3}} \times V_{REF} \quad (11)$$

The voltage difference corresponding to isolated ground:

$$V_{Diff} = V_{HV} - V_{ISO-GND} \quad (12)$$

This difference voltage will be buffered and filtered then output as V_{in-2} to the 2nd channel of ADC, which will be sampled by ADC:

$$V_{in-2} = V_{Diff} \quad (13)$$

Based on above Equation (10), (11), (12) and (13):

$$V_{Battery} \approx V_{ISO-GND} = \frac{3R_{HV}}{R_{d3}} \times V_{REF_Rating} - \frac{3R_{HV} + R_{d3}}{R_{d3}} \times V_{in-2} \quad (14)$$

After the bias resistors (R_{HV} and R_{d3}) are confirmed and the voltage reference is selected, also V_{in-2} is sampled by ADC and the value can be calculated, then the voltage of battery pack ($V_{Battery}$) will be known.

RC-Filter:

The requirements for passive RC-filter (R_1 and C_1) are same as the RC-filter components in the isolated current measurement path in Section 2.1.3.

Buffer Amplifier:

The buffer amplifier will provide the necessary isolation between resistor divider and ADC, and is required to drive the input of ADC especially at higher sampling rates. A proper buffer amplifier should be selected, and the selection criteria can be referred to Section 2.1.4. The key considerations for the selection of buffer amplifier in the voltage measurement path are:

- **Lower Output Impedance**
- **Minimized Input Offset**
- **Smaller Offset Drift**
- **Higher Input Impedance**
- **Higher Bandwidth**
- **Unity-Gain Stable**

2.3 Precision Voltage Reference Circuit

Usually, an external voltage reference circuit is used in a data acquisition system if the ADC does not have an internal reference. This external reference is used to provide an accurate voltage for ADC reference input and biasing of other components in the signal chain. In order to achieve the optimum system performance, it is important to design an appropriate filter and buffer circuit at the output of the voltage reference.

The circuit used in this design uses precision reference voltage at multiple instances for performing the following different functions:

- Voltage reference for multichannel ADC: V_{REF_ADC}
- Level shifting voltage for isolated Current Shunt: V_{shift}
- Voltage reference for isolated Voltage Measurement: V_{REF}

The reference circuit designed in this system is shown in below [Figure 6](#). The reference output (V_{REF}) is used for isolated voltage measurement because there is another buffer in the voltage measurement path.

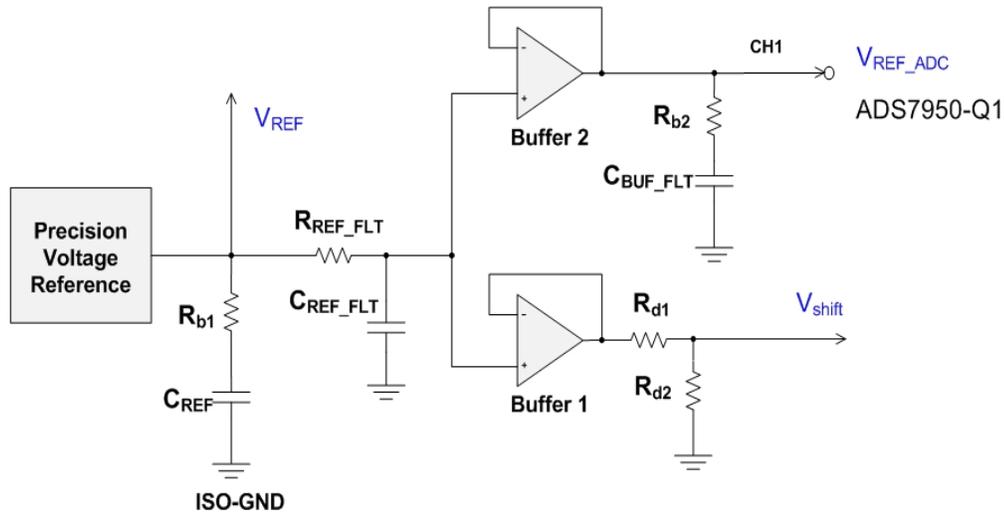


Figure 6: Voltage Reference Circuit

2.3.1 Low Pass Filter on Reference

The objective for the filter design (R_{REF_FLT} & C_{REF_FLT}) is to keep the bandwidth low enough such that the intrinsic noise from the reference will not contribute to any degradation in the performance of the system.

The maximum limit for -3dB cut-off frequency of the RC-filter (f_{REF_3dB}) can be determined by the Equation (15) (Reference 1):

$$f_{REF_3dB} \leq \frac{2 \times I_{Q_REF} (\mu A)}{(10000 nV / \sqrt{HZ})^2} \times \frac{2}{\pi} \times \left[\frac{1}{9} \times \frac{V_{FSR}^2}{8} \times 10^{\frac{SNR(dB)}{10}} - \left(\frac{V_{1/f_REF_PP}}{6.6} \right)^2 \right] \quad (15)$$

I_{Q_REF} : Quiescent current for voltage reference

V_{1/f_REF_PP} : 1/f noise for voltage reference

SNR : Signal to Noise Ratio for ADC

V_{FSR} : Full Scale Range for ADC

After calculating f_{REF_3dB} and selecting the value of C_{BUF_FLT} according to the recommendation in the datasheet of voltage reference, the value of R_{BUF_FLT} can be calculated using Equation (16):

$$R_{REF_FLT} = \frac{1}{2\pi f_{REF_3dB} \times C_{REF_FLT}} \quad (16)$$

2.3.2 Reference Buffer and Capacitor

The reference input of a SAR ADC is a dynamic load for external voltage reference, hence a reference buffer (Buffer 2) is necessary to regulate the voltage in order to make sure that the voltage variation on the reference input (ΔV_{REF}) is less than 1LSB error at the start of each conversion. This requirement can be achieved by using a capacitor (C_{BUF_FLT}) combined with the buffer to drive the ADC reference input pin.

The minimum value of capacitor (C_{BUF_FLT}) can be obtained by the following equation (Reference 1):

$$C_{BUF_FLT} \geq \frac{2}{3} \times \frac{I_{REF} \times T_{CONV_MAX} \times 2^N}{V_{REF}} \quad (17)$$

I_{REF} : Reference current specified in the ADC's datasheet

T_{CONV_MAX} : Maximum ADC conversion time

The value of C_{BUF_FLT} derived from above equation is high enough to make the driving buffer amplifier unstable, so a series resistor (R_{b2}) is recommended to isolate their output and make the reference circuit stable. The value of R_{b2} depends on the output impedance of the buffer amplifier and voltage reference as well as on the signal frequency. Typically the value of R_{b2} should be between 0.1Ω to 2Ω.

After the passive components are confirmed, an appropriate reference buffer amplifier should be determined. The key considerations for the selection of buffer amplifier are same as the buffer amplifier of voltage measurement described in Section 2.2.

2.3.3 Buffer for Level Shift

As shown in Figure 6, R_{d1} and R_{d2} are used as a resistor divider, which create level shift voltage (V_{shift}) for the current measurement shown in Equation (18). From this equation, it is clear that the accuracy and drift performance of both resistors will have a direct influence to measured accuracy of load current in battery pack monitoring system.

$$V_{shift} = V_{REF} \times \frac{R_{d2}}{R_{d1} + R_{d2}} \quad (18)$$

The level shift output voltage (V_{shift_out}) after the amplification can be calculated as:

$$V_{shift_out} = V_{shift} \times \left(1 + \frac{R_F}{R_G} \right) \quad (19)$$

The reference buffer (Buffer 1) will also have a direct impact on the sampling accuracy of input current, so it is critical to select an amplifier such that this error can be minimized. The key specifications for the selection of the buffer amplifier are the same as discussed Section 2.3.2.

2.4 Digital Isolators

There are four digital interface lines used for standard SPI bus of the ADC, SCLK (Clock), SDI (MOSI), SDO (MISO) and /CS (Chip select). Generally, the digital isolation of SPI bus only requires single quad channel digital isolator and shown in Figure 7.

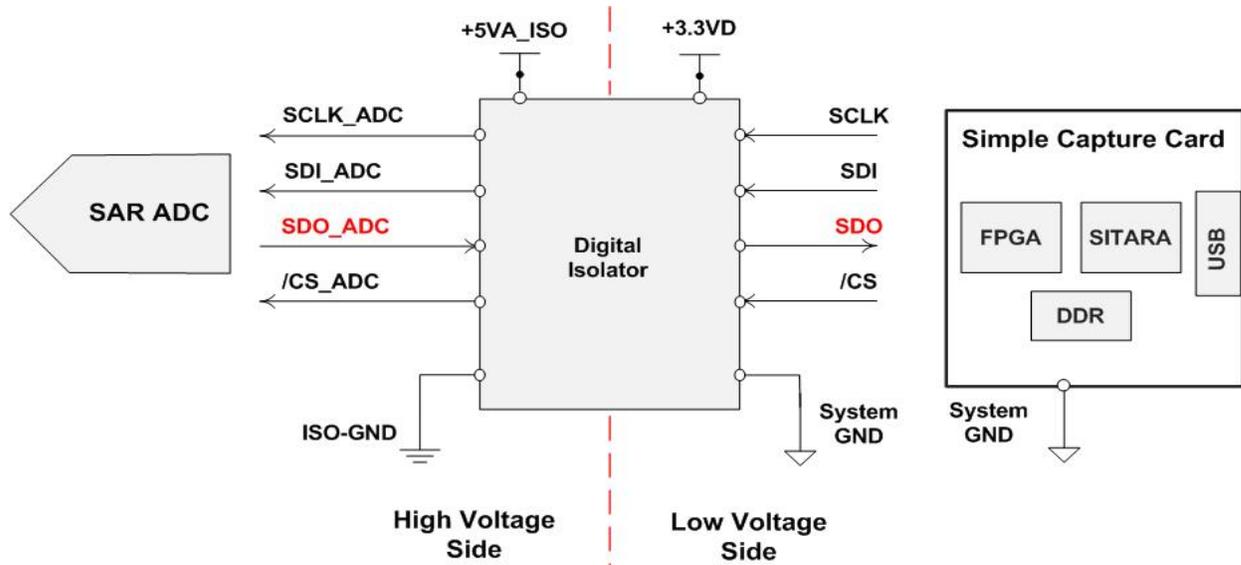


Figure 7: General Digital Isolator Circuit

When a digital isolator is used to isolate the SPI signals, a propagation delay is introduced by the digital isolator on all channels. For instance, ISO7241C-Q1 has a minimum propagation delay of 20ns and maximum delay of 50ns with +5VA_ISO and +3.3VD power supplies. This delay will lead to a timing mismatch between SCLK and SDO signals, despite the fact that SDO_ADC is matched to SCLK_ADC. This is because there is a delay between SCK and SCLK_ADC and another delay between SDO_ADC and SDO, which is in opposite direction. So the total timing skew between SDO and normal SCLK gets doubled, as shown by the dotted line in Figure 8. This timing mismatch makes it extremely difficult to read data through the digital isolator at a fast throughput without introducing errors.

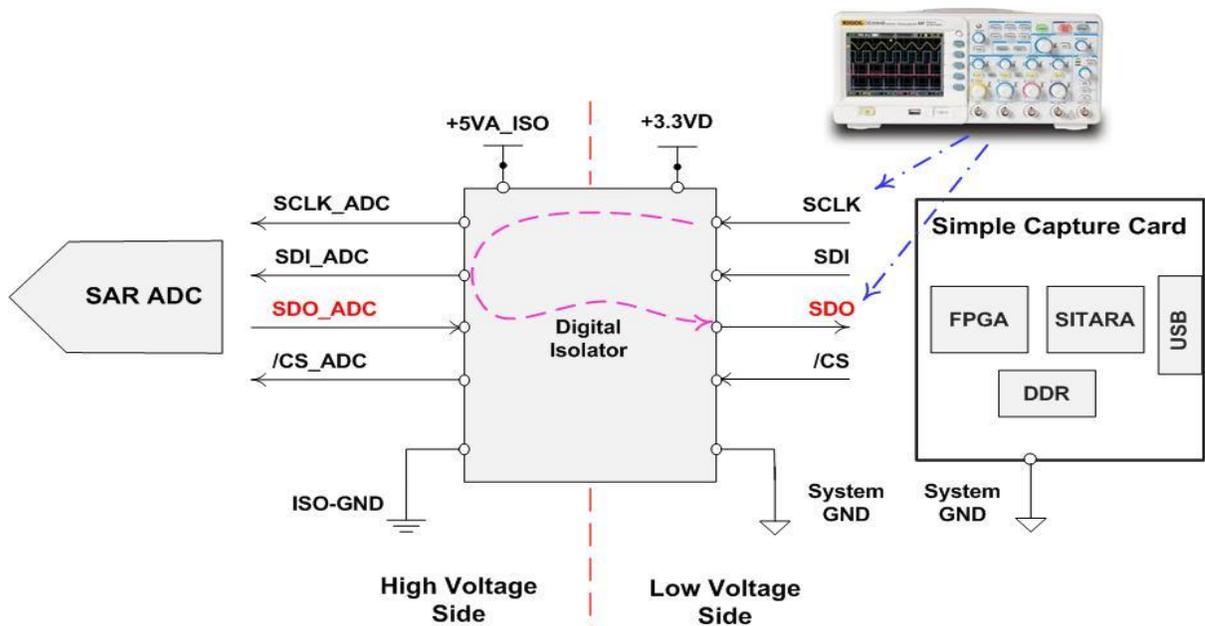


Figure 8: Propagation Delay with Digital Isolator

When an oscilloscope is used to check the signal waveforms from the low voltage Simple Capture Card side, a propagation delay will be clearly observed between SCLK and SDO signals.

There are some solutions which can be used to resolve this timing mismatch. One of them is to adjust the timing of SDO from the FPGA by software or logic to match the SCLK signal. Another solution is to feed back the SCLK_ADC signal to the low voltage FPGA/CPU side through the digital isolator. This returned clock signal can then be used to retrieve the data on SDO line as the delays are now matched and the two signals are synchronized.

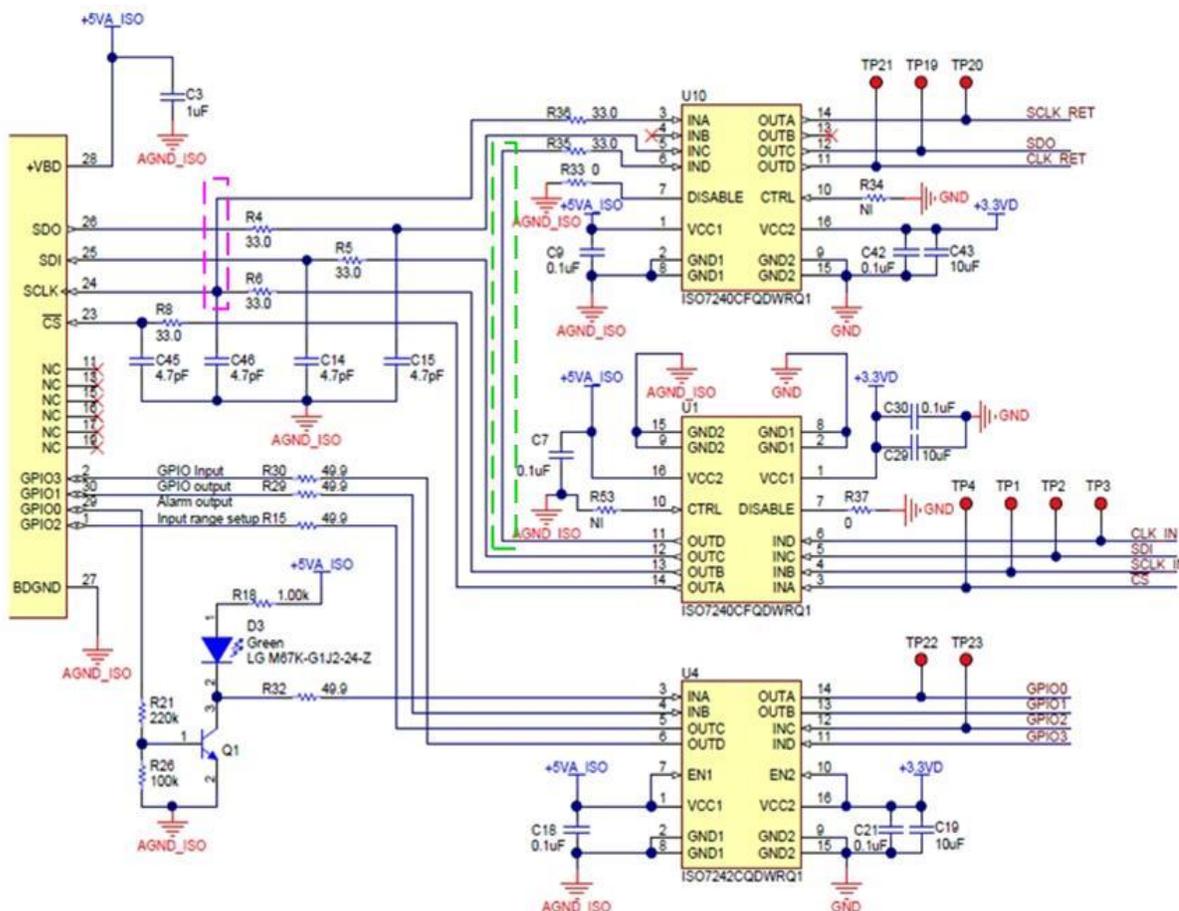


Figure 9: Digital Isolator Solution in Precision Design

This precision design utilizes the second solution where either the returned SCLK (SCLK_RET) shown in the pink dotted line box of Figure 9 or one dedicated clock returned signal (CLK_RET) shown in the green dotted line box of Figure 9 can be used to get correct sampling data. The U4 digital isolator is used to isolate two GPIO signals, one Alarm signal and one ADC's input range configuration input signal. The GND in the schematic is the system ground (System GND).

2.5 Isolated Power Supply

In order to keep the design as simple as possible, one +5V to +5V isolated DC-DC converter (DCR010505) is used for generating an isolated power supply in this design. This regulated output voltage is supplied to ADC analog supply (+VA) and digital supply (+VBD) and, to the isolated side of digital isolator directly. The key design considerations for this isolated power supply are:

- 1W galvanically-isolated DC-DC converter
- +5V input to +5V isolated output

- Regulated output
- 1000Vrms isolation
- High-efficiency, Low noise

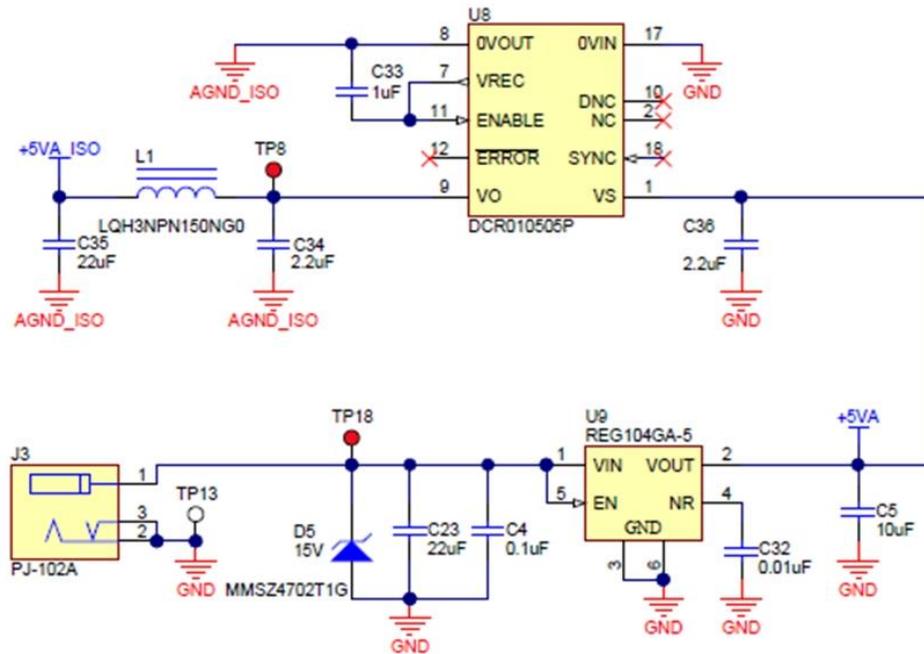


Figure 10: Isolated Power Supply

A low-noise, low-dropout linear regulator, REG104-5 is used to convert external power supply (+6V~+15V) to +5V output supply providing to DCR010505 directly, the block diagram is shown in Figure 10. The GND in the schematic is the system ground (System GND).

3 Component Selection

3.1 ADC Selection

The primary objective of this design is to provide an optimum solution for monitoring several important parameters of automotive battery packs, including current, voltage, temperature and system power supply. This necessitates the use of a multi-channel ADC for designing this battery monitoring system. This solution also requires careful design of isolation circuit in order to handle the high common mode voltages of the battery. From the perspective of designing the digital isolation circuit, a serial interface is preferred to minimize the number of channels through the digital isolator. Based on the above requirements, a multichannel input, serial interface, automotive qualified SAR ADC is selected. The ADS7950-Q1 is a 12-bit 1MSPS, 4-channel, and AEC-Q100 qualified SAR ADC which is a good choice to design this system. The ADS7950-Q1 family offers device variants with 8, 12 or 16 channels which make it easier for system designers to select the proper ADC in their system when more monitoring channels are required.

The default input range on ADS7950-Q1 is 0~+2.5V, but it will be configured to 0~+5V range by the dedicated Range pin (Pin 1) in this design to maximize the utilization of dynamic range for higher measurement accuracy.

3.2 Selection for Current Measurement Path

3.2.1 Shunt Resistor Selection

The selection criteria and tradeoffs for selecting a current shunt resistor are provided below:

- Increasing R_{shunt} will increase the voltage drop on the shunt, which helps to relax the requirements on the voltage offset (V_{OS}) and input bias current offset (I_{OS}) of back-end amplifier.
- Larger value of R_{shunt} can produce self-heating due to increased power dissipation $P = I^2 \times R_{shunt}$. The temperature drift changes the nominal resistance of the shunt, thus affecting the measurement accuracy.
- Smaller R_{shunt} requires larger gain configuration on the amplifier to match the full dynamic range of ADC, which results in higher noise and affects overall system accuracy.
- It is critical to select a shunt resistor with low temperature coefficient and tolerance as these parameters have a direct impact on the measurement accuracy.

This design is specified to measure a maximum current of $\pm 5A$. Based on the considerations described above, the value of the shunt is selected to create a maximum voltage drop of $\pm 100mV$.

$$R_{shunt} = \frac{V_{shunt}}{I_{load}} = \frac{100mV}{5A} = 20m\Omega \quad (20)$$

The power dissipation on the shunt:

$$P = I^2 \times R = 5^2 \times 0.02 = 0.5W \quad (21)$$

Four-terminal current sense resistors typically have very low temperature coefficient and thermal resistance. Furthermore four-terminal resistors with Kelvin sensing connection can provide higher measurement accuracy. Hence, LVK20R020DER from Ohmite company is selected for this design.

The specifications for this component are given below:

- Resistor value = 20m Ω
- Tolerance = 0.5%
- Temperature coefficient = 50ppm/ $^{\circ}\text{C}$
- Power rating = 0.75W
- Four-terminal with Kevin connect capability
- Package = 2010 small surface mount as shown in [Figure 11](#).



Figure 11: Shunt Resistor - LVK20R020DER

3.2.2 Gain and Bias Resistors Selection

Gain Resistors:

The bipolar $\pm 100\text{mV}$ voltage drop across the shunt resistor needs to be amplified to meet the input dynamic range (V_{FULL_Range}) of ADS7950-Q1 for maximum performance, which is 5V for current measurement channel. A small headroom of 0.5V ($V_{headroom}$) is reserved on the ADC input to avoid any signal clipping. The ADC also requires an external voltage reference of 2.5V. The same precision voltage is also used to create the bias voltage ($V_{shift_out} = 2.5\text{V}$) for the level shifting circuit, which is the midpoint of V_{FULL_Range} . The amplifier gain can now be calculated by Equation (22):

$$V_{shunt} \times Gain_{signal} + V_{shift_out} = V_{Full_Range} \pm V_{headroom} \quad (22)$$

$$Gain_{signal} = -20 \frac{V}{V}$$

According to Equation (2):

$$\frac{R_F}{R_G} = 20 \quad (23)$$

Larger resistors will cause more noise and error but smaller gain resistors will lead to smaller load impedance to shunt resistor with inverting configuration and current draw from the measurement system. To balance the tradeoff, a 0.1% tolerance precision resistor equal to 102k Ω is selected as R_F and another 0.1% tolerance precision resistor equal to 5.1k Ω is selected as R_G . The temperature coefficient for both of resistors is equal to 25ppm/ $^{\circ}\text{C}$.

Bias Resistors:

Resistors, R_{d1} and R_{d2} are used to create level shift voltage (V_{shift}) for the current measurement, this also requires high precision resistors are required as it has a direct impact on the measurement accuracy of current. Based on the Equation (19) and Equation (23), the value of V_{shift} should be equal to +119mV.

According to Equation (18), R_{d1} can be selected as 43k Ω and R_{d2} can be selected as 2.15k Ω . Both resistors have 0.1% tolerance and temperature coefficient of 25ppm/ $^{\circ}$ C.

3.2.3 RC-filter Components Selection

When operating at $V_{REF} = 2.5V$ and $V_{FSR} = 2 \times V_{REF} = 5V$, the least significant bit (LSB) size for ADS7950-Q1 is given by $LSB = 5/2^{12} V$. Substituting $t = t_{ACQ} = 325ns$ in Equation (7), we get:

$$\frac{1}{R_{FLT} \times C_{FLT}} = \frac{1}{\tau} \geq \frac{\ln \left[\frac{2 \times 5 \times 2^{12}}{5} \right]}{325 \times 10^{-9}} \quad (24)$$

$$R_{FLT} \times C_{FLT} \leq 36.07 \times 10^{-9} \quad (25)$$

The specified value of input capacitor in ADS7950-Q1 datasheet is 15pF, according to Equation (6),

$$C_{FLT} \geq 20 \times 15 pF = 300 pF$$

A standard value capacitor is selected for C_{FLT} :

$$C_{FLT} = 330 pF \quad (26)$$

A NP0/C0G type capacitor should be chosen for C_{FLT} due to high stability, smaller voltage and frequency coefficient features.

Then the maximum value R_{FLT} can be calculated according to Equation (25) and (26):

$$R_{FLT} \leq 111.2 \Omega \quad (27)$$

A 0.1% tolerance precision resistor equal to 100 Ω is selected as R_{FLT} for this design.

3.2.4 Amplifier Selection in Gain Stage

Using the selected values of C_{FLT} and R_{FLT} , the minimum unity gain bandwidth for this amplifier can be calculated according to Equation (9).

$$Unity - GainBandwidth \geq 4 \times \frac{1}{2\pi R_{FLT} \times C_{FLT}} = 19.3 MHz \quad (28)$$

Also according to the key specification requirements discussed in Section 2.1.4, a precision automotive qualified amplifier OPA2320-Q1 is chosen for this design because of its extremely good specifications:

- Low Offset Voltage: 40uV/150 μ V (typ/max)
- Low Input Bias Current: 0.2 pA/0.9 pA (typ/max)
- Unity Gain Bandwidth: 20 MHz

- Low Noise: 7 nV/√Hz at 10kHz
- High CMRR: 114 dB
- Rail-to-Rail: Input and Output
- Slew Rate: 10 V/μs
- Unity-Gain Stable

3.3 Selection for Voltage Measurement Path

Resistors Selection:

The target of this precision design is measuring up to 750V automotive battery pack voltage, therefore three individual 1MΩ resistors are selected for R_{HV} , one 10kΩ resistor is chosen for R_{d3} . ADS7950-Q1's full scale range of voltage measurement channel is set to 0~+2.5V ($V_{in-2} = 2.5V$), and also this ADC requires a 2.5V external precision voltage reference, hence $V_{REF_Rating} = 2.5V$.

According to the selected resistors and Equation (14), the maximum and minimum measurable battery voltages are:

$$V_{Batter_Max} = \frac{3R_{HV}}{R_{d3}} \times V_{REF_Rating} = \frac{3 \times 1M}{10k} \times 2.5 = 750V \quad (29)$$

$$\begin{aligned} V_{Battery_Min} &= \frac{3R_{HV}}{R_{d3}} \times V_{REF_Rating} - \frac{3R_{HV} + R_{d3}}{R_{d3}} \times V_{in-2} \\ &= \frac{3 \times 1M}{10k} \times 2.5 - \frac{3 \times 1M + 10k}{10k} \times 2.5 = -2.5V \end{aligned} \quad (30)$$

By changing the values of R_{HV} and R_{d3} , this circuit can be achieved to measure up to 1000Vrms voltage of automotive battery pack, which is limited by the isolation voltage of the isolated power supply and digital isolators in the design.

RC-Filter Components Selection:

The requirements for passive RC-filter (R_1 and C_1) are same as the RC-filter components (R_{FLT} and C_{FLT}) in the isolated current measurement path selected in Section 3.2.3. The same value and type resistor and capacitor can be used for R_1 and C_1 .

Buffer Amplifier Selection:

The buffer amplifier in this voltage measurement path is similar to the amplifier selected in isolated current measurement path in Section 3.2.4. The same precision OPA2320-Q1 can be used here.

3.4 Selection for Voltage Reference Circuit

The external reference used to drive the ADS7950-Q1 in this design is the REF5025-Q1 from TI, which is an AEC-Q100 qualified 2.5V precision voltage reference. As mentioned in the data sheet of ADS7950-Q1, it requires a capacitance of 10μF between the REF and System GND pin.

According to the detailed information in Section 2.3.1 and Section 2.3.2, $C_{BUF_FLT} = 10\mu\text{F}$, $C_{REF} = 10\mu\text{F}$ (refer to the calculation in Reference 1). A series resistor of 0.47Ω is used for R_{b2} with the $10\mu\text{F}$ C_{BUF_FLT} capacitor together close to ADS7950-Q1 for smooth power-up of the required voltage reference. Another series resistor of 0.1Ω is used for R_{b1} with the $10\mu\text{F}$ C_{REF} capacitor close to voltage reference (REF5025-Q1) for same purpose.

The value of capacitor C_{REF_FLT} is selected as $1\mu\text{F}$ to keep the thermal noise of the capacitor at a minimum value. The value of R_{REF_FLT} is selected as $1\text{k}\Omega$ for this design to create a low pass filter that can eliminate most of broadband noise. The -3dB cut-off frequency of this filter is shown in Equation (31):

$$f_{REF_3dB} = \frac{1}{2\pi R_{REF_FLT} \times C_{REF_FLT}} = 159.2\text{Hz} \quad (31)$$

The buffer amplifiers for reference and level shifter circuit have similar requirements as the amplifier selected in the gain and signal conditioning stage of the current measurement signal path. An OPA2320-Q1 precision amplifier is used for the reference buffer to ADC and the level shifting buffer for isolated current measurement path.

3.5 Selection for Digital Isolator

As introduced in Section 2.4 and shown in Figure 9, two automotive AEC-Q100 qualified digital isolators ISO7240CF-Q1 are used for SPI interface isolation as U1 and U10, and another qualified ISO7242C-Q1 is selected for the isolation of General Purpose Input Output (GPIO) signals as U4.

4 TINA Model Simulation

The TINA-TI™ SPICE Model can be used to check transient response and evaluate if there are any signal settling problems in entire signal chain of sampling channel and reference driver design. These simulations also help to verify if the circuit design is proper and the values of selected components are appropriate.

4.1 Transient Simulation for Current Measurement Input Channel

Figure 12 shows the TINA-TI™ schematic for the current measurement path using component values obtained in the design process. The TINA model accurately models the switched-capacitor input structure of ADS7950-Q1, and is used to simulate the input settling behavior. In order to utilize the full input dynamic range of the ADS7950-Q1 (0 ~ +5V), the maximum sensed voltage on shunt resistor should be ideally equal to 125mV. For simulation purposes, a DC source is used to create the Thevenin equivalent circuit for the actual current source and shunt resistor. In order to avoid signal clipping, a maximum DC voltage of 120mV is used as input for the transient simulation. A voltage meter V_{error} is used to check settling error between amplifier's output and the settled signal on ADS7950-Q1's internal sampling capacitor.

Corresponding to +5V input range, the size of least significant bit (LSB) for ADS7950-Q1 is:

$$LSB = \frac{5V}{2^{12}} = 1.22mV, \text{ so } 1/2 \text{ LSB} = 610\mu V \quad (32)$$

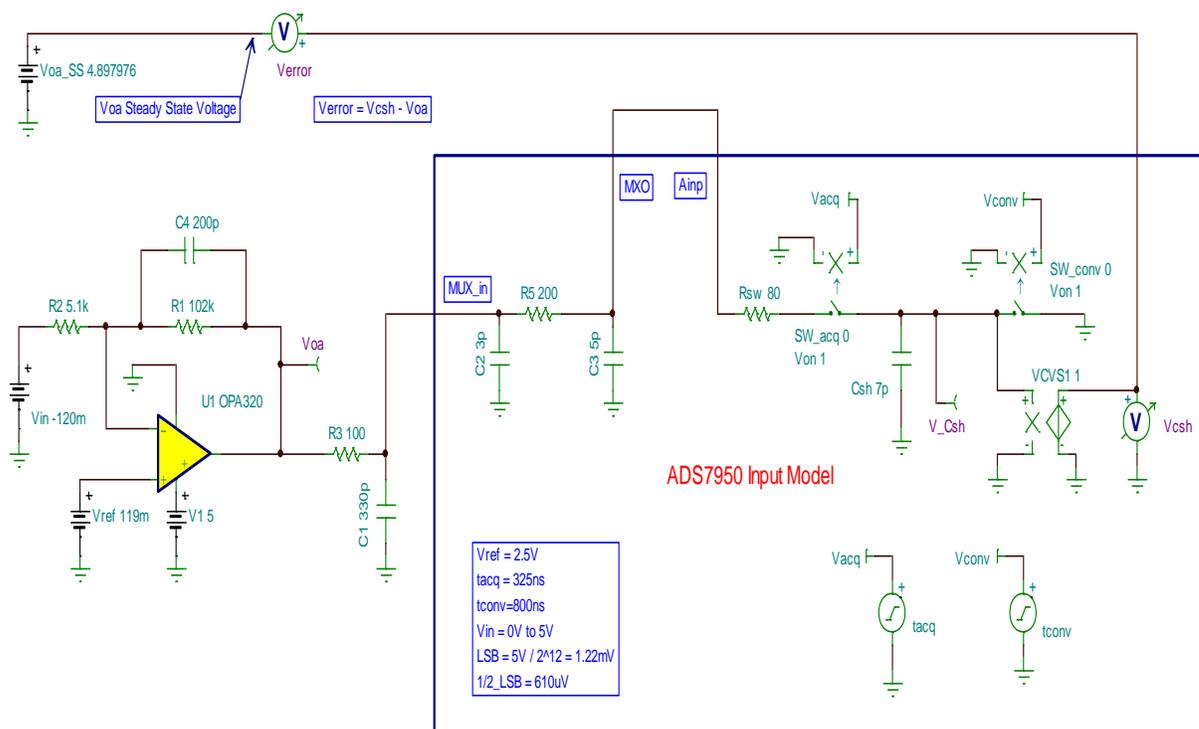


Figure 12: TINA Simulation for Current Measurement Input Channel

According to the simulation results shown in Figure 13, at the end of t_{acq} (ADC acquisition time) the voltage error between input signal and settled signal is $V_{error} = 3.40205nV$, which is much less $1/2 \text{ LSB}$. This implies that the circuit in Figure 12 is designed properly and can achieve accurate signal settling on ADC's internal sampling capacitor.

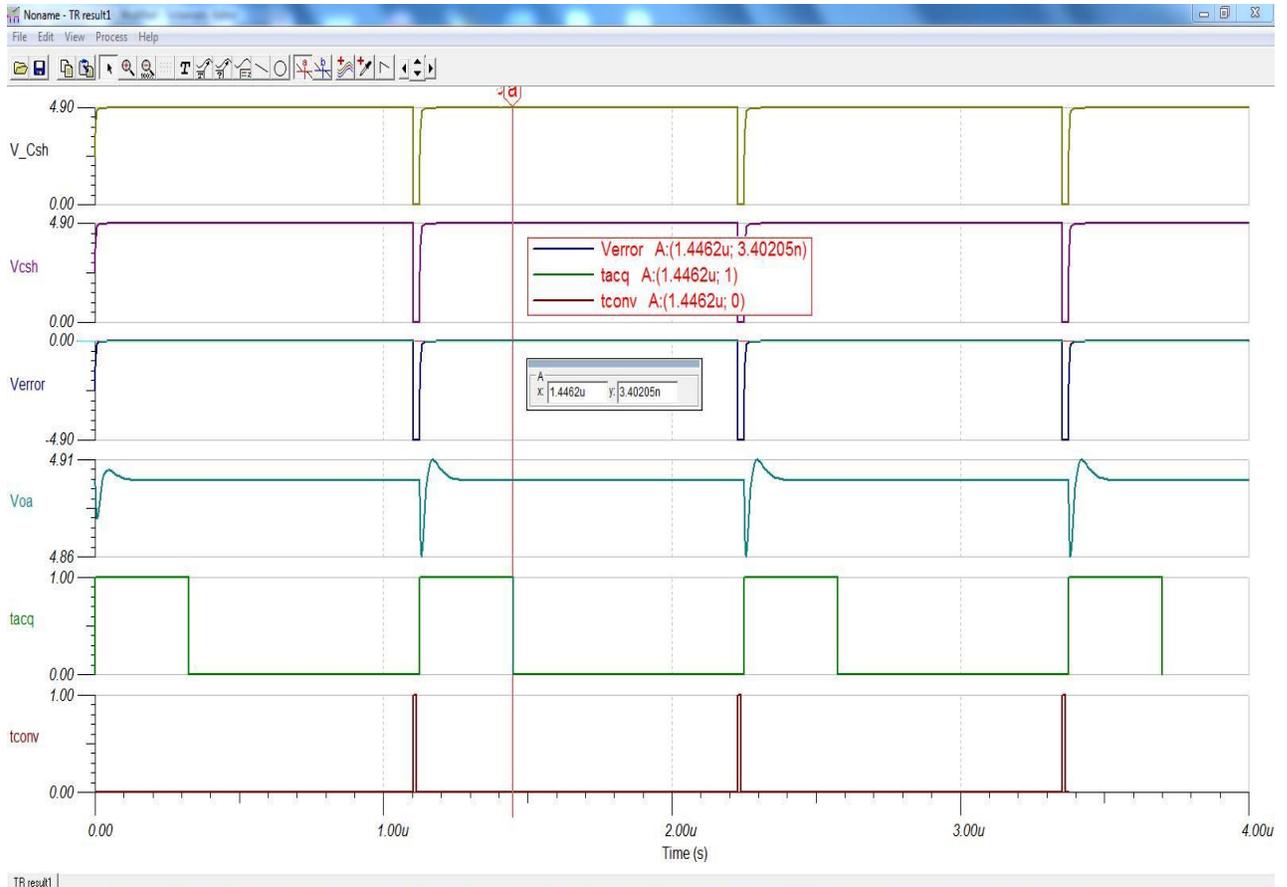


Figure 13: Simulation Result for Current Measurement Input Channel

4.2 Transient Simulation for Reference Driver Circuit

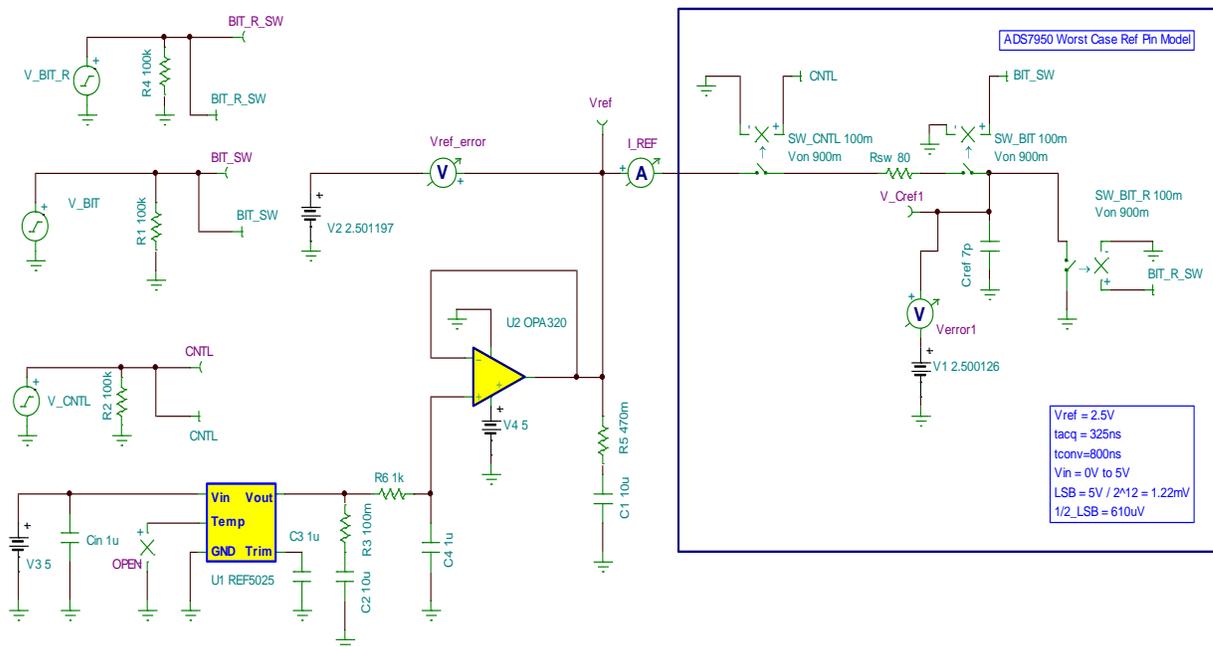


Figure 14: TINA Simulation for Reference Driver Path

The simulation model of the reference driver circuit can be used to check the settling behavior on the voltage reference input of the ADC. This ensures that the reference voltage is settled before the beginning of every new conversion. This simulation helps to establish that the reference driver circuit is designed properly. The complete schematic for the reference driver circuit is shown in [Figure 14](#).

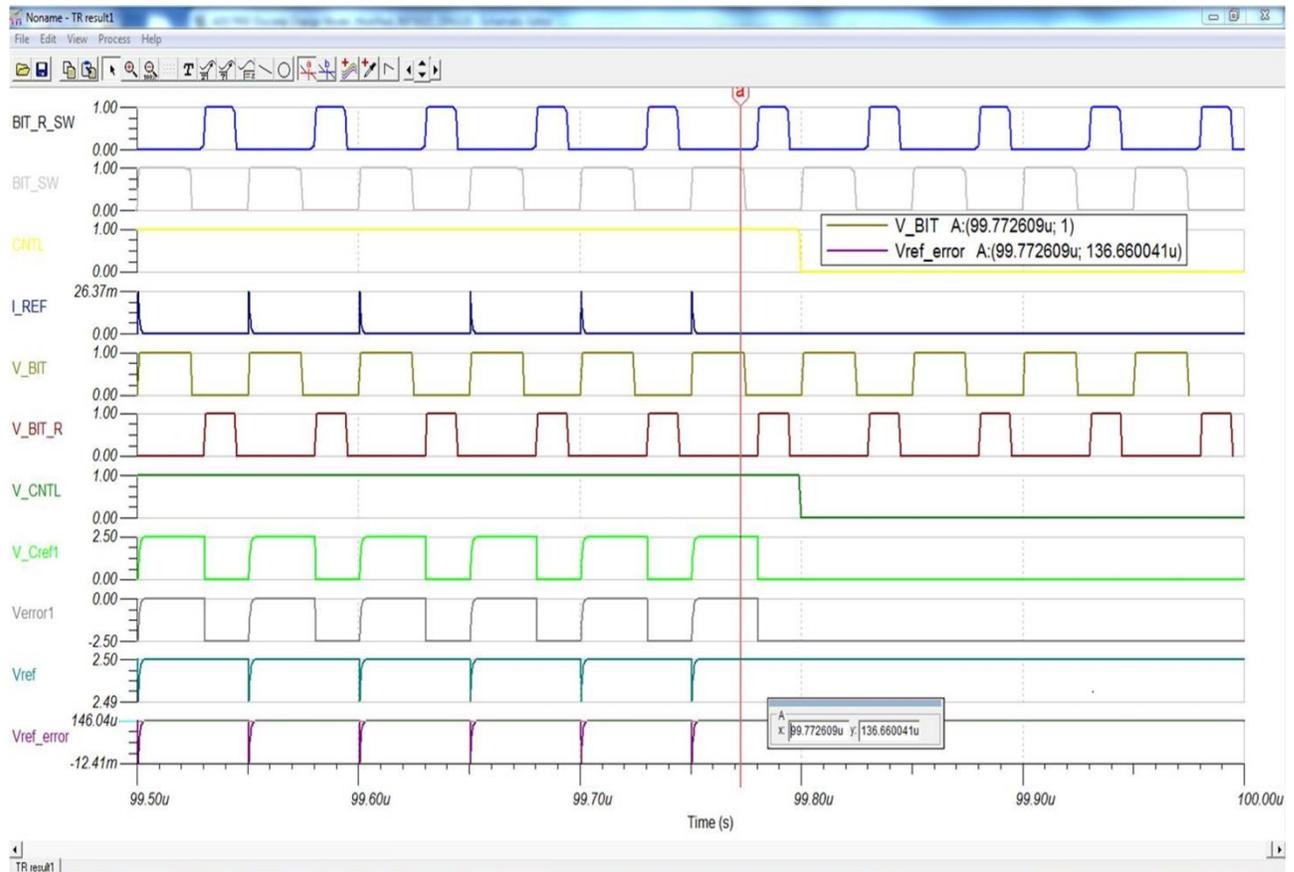


Figure 15: Simulation Result for Reference Driver Path

The transient response simulation result is provided in [Figure 15](#). BIT_SW runs continuously at the ADC clock frequency and internal capacitor C_{ref} is switched into the reference pin by SW_BIT for charging process during first half of the clocking period. For the other half of the clocking period, C_{ref} is switched out and discharged through SW_BIT_R switch. Hence, the same analytical approach of input signal is used for voltage reference path, at the end of charging process the voltage error between internal capacitor C_{ref}

and external reference driver output is $V_{error} \approx 136.66\mu V = 0.112LSB$, which verify that the external voltage reference signal is fully settled on ADC's reference input pin.

5 Verification & Measured Performance

The measurement results for this TI Precision Design are listed in this section. [Figure 16](#) shows the experimental setup used for validating the performance of the isolated current and voltage measurement circuits described in this design. The isolated current shunt is located on the Device Under Test (DUT) board. The precision current source is used for this test. A Simple Capture Card from Texas Instruments is utilized as a digital interface board to get sampled data from DUT and communicate with monitor graphical user interface (GUI) software for further data analysis. A high voltage power supply can be used to provide higher common mode voltage. A current meter (AM1) is used to measure actual current flowing through shunt resistor. When performing this test, a digital multi-meter (VM1) is utilized to measure the shunt voltage which is four-terminal Kelvin connection with AM1 current meter to reduce the measurement error.

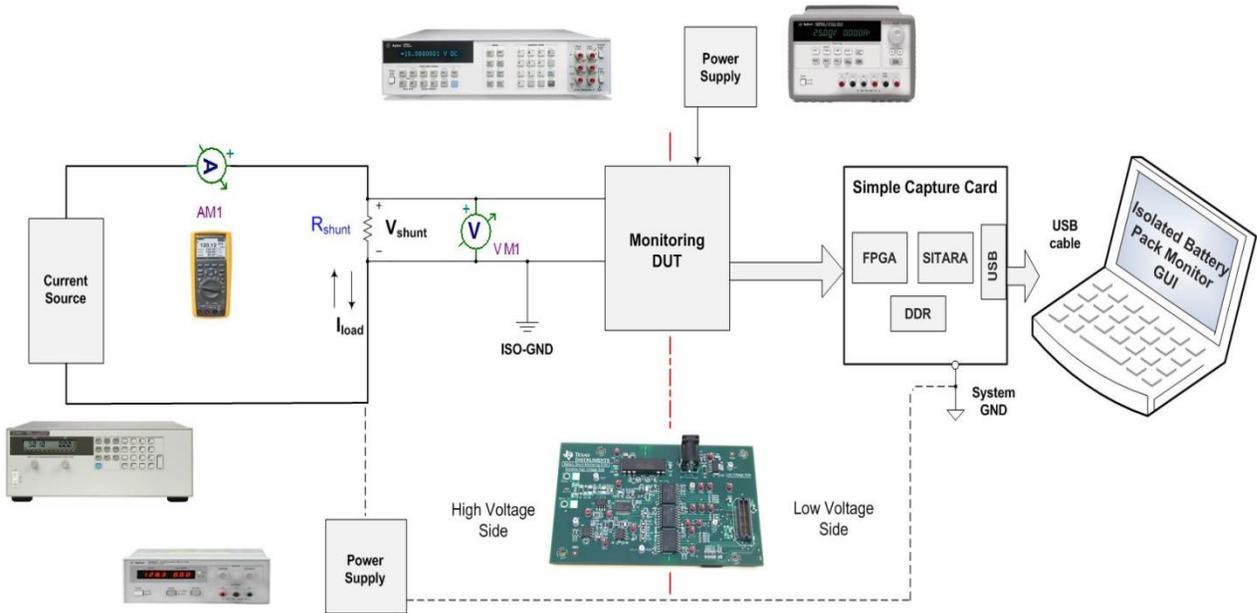


Figure 16: Test Setup

The following sections describe multiple test conditions for the verification process, which are utilized to verify the function and accuracy of this monitoring system.

5.1 Transfer Function

Figure 17 depicts the transfer function of the current measurement channel for up to 100V common mode voltage with measured input current flowing through the shunt resistor as the input variable and the output codes sampled from the ADS7950-Q1 DUT board as the output variable.

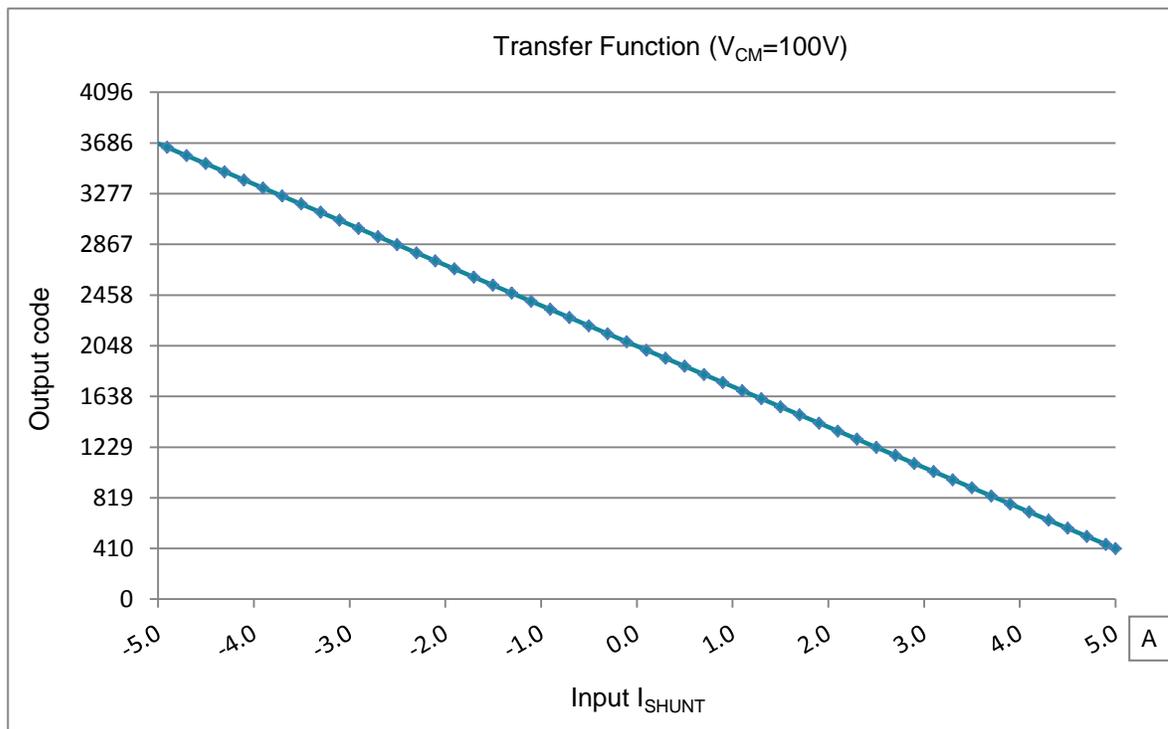


Figure 17: Transfer Function of the System ($V_{CM}=100V$)

5.2 System Error for Current Measurement

The data from Figure 17 is exported to a spreadsheet in order to calculate the error as a percent of the full-scale range (% FSR_{error} , 5A is used as the full-scale range for this design). Equation (33) is used to calculate % FSR_{error} for every tested load current.

$$FSR_{error} = \frac{I_{error}}{I_{FSR}} \times 100 = \frac{I_{calculate} - I_{actual}}{I_{FSR}} \times 100 \quad (33)$$

In order to accurately calculate the system error, the tests are performed from +5A and +4.9A to -4.9A and -5A with a 0.2A step. The same tests are repeated for different common-mode voltages. The system Gain and Offset calibration technique shown in the Appendix B is implemented for the data analysis and error calculation of current measurement.

Figure 18 shows the measured current error (% FSR_{error} , calibrated) based on the transfer function shown in Figure 17 for 100V common-mode voltage of a battery pack. According to Equation (33), this error is obtained by subtracting the actual input current from the calculated input load current, obtained from sampled output code by ADS7950-Q1 precision ADC.

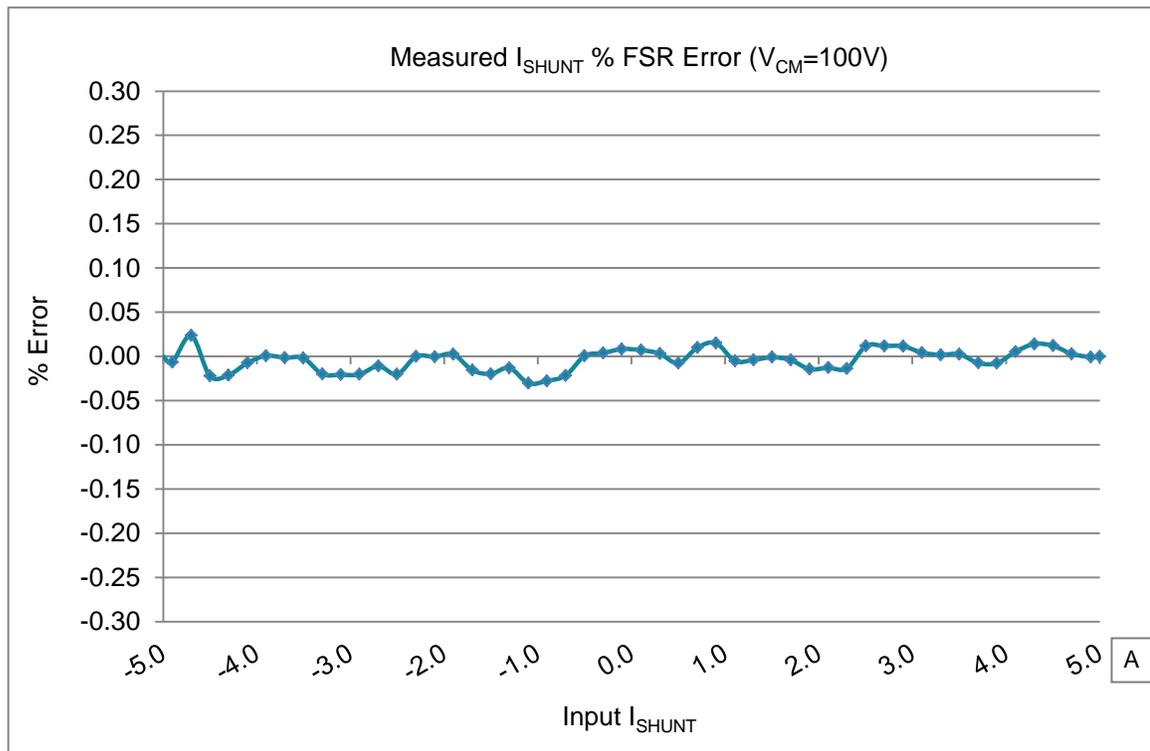


Figure 18: Measured Current Error ($V_{CM}=100V$)

Based on the test result, the maximum positive % FSR_{error} for 100V common-mode voltage was found to be 0.024%, and the maximum negative % FSR_{error} was -0.030%, which meets our design goal of 0.05%.

Using the same method, Figure 19 shows the measured system error (% FSR_{error} , calibrated) for 25V common-mode voltage of a battery pack. Based on the test result, the maximum positive % FSR_{error} for 100V common-mode voltage was found to be 0.024%, and the maximum negative % FSR_{error} was -0.026%, which also falls within the original design goals.

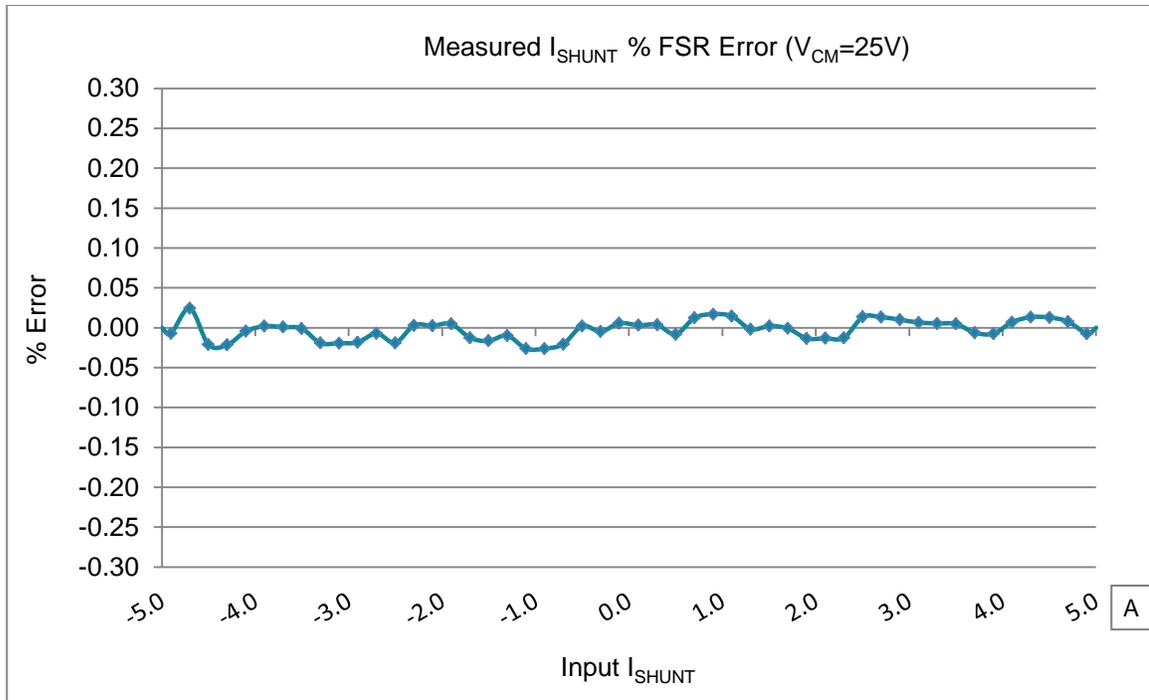


Figure 19: Measured Current Error ($V_{CM}=25V$)

5.3 System Error for Voltage Measurement

The system error analysis of voltage measurement is achieved by second channel of ADS7950-Q1 according to the test setup in Figure 16. The voltage error is the error between the calculated voltage based on the sampled code and the actual common mode voltage, and it is represented as a percent of the full-scale range ($\%FSR_{error}$, 750V for this design) using the same method in Section 5.2. The test was implemented from 0V to +120V by a 5V step and the result is shown in Figure 20, the measured maximum voltage error is 0.035% ($\%FSR_{error}$, uncalibrated), which meets the design goal of 0.05%.

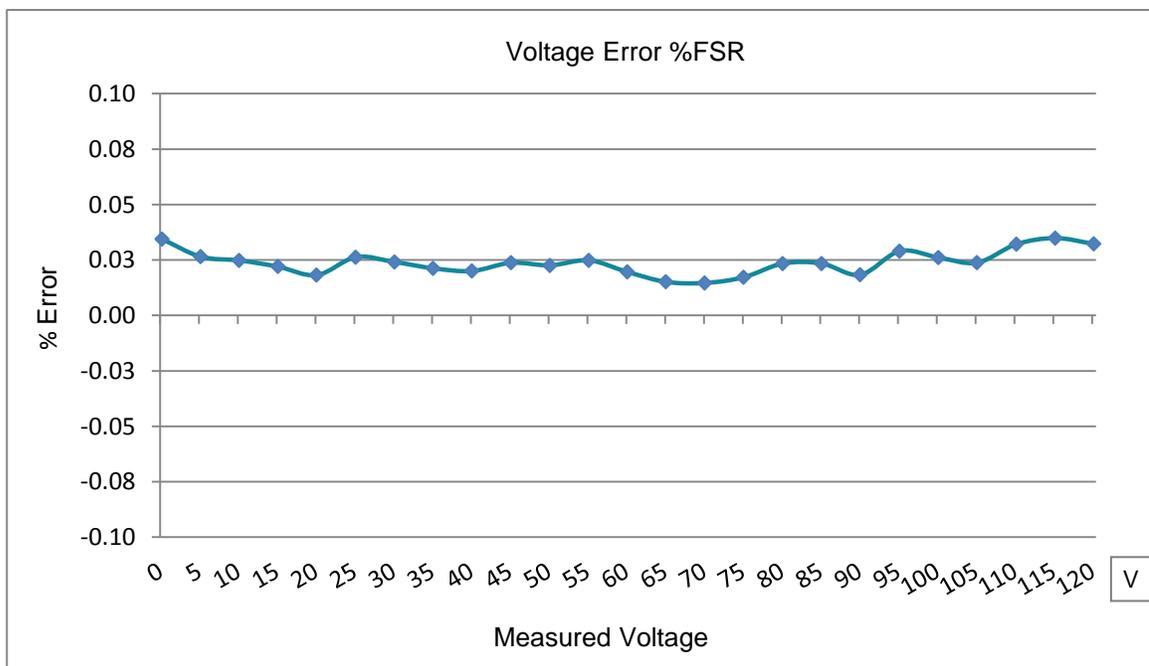


Figure 20: Measured Voltage Error

5.4 AC Measurement

The ac performance test can be utilized to verify the simulations and check any problems of system design and component selection. The system ac performance of current channel was measured for a 1kHz, sinusoidal signal. Figure 21 shows the frequency domain plots of the acquired signal using the 1MSPs maximum sampling rate of ADS7950-Q1. From this result, the ac performance is much closer to the specifications of ADC, and the front-end circuit in this design doesn't degrade the ADC performance.

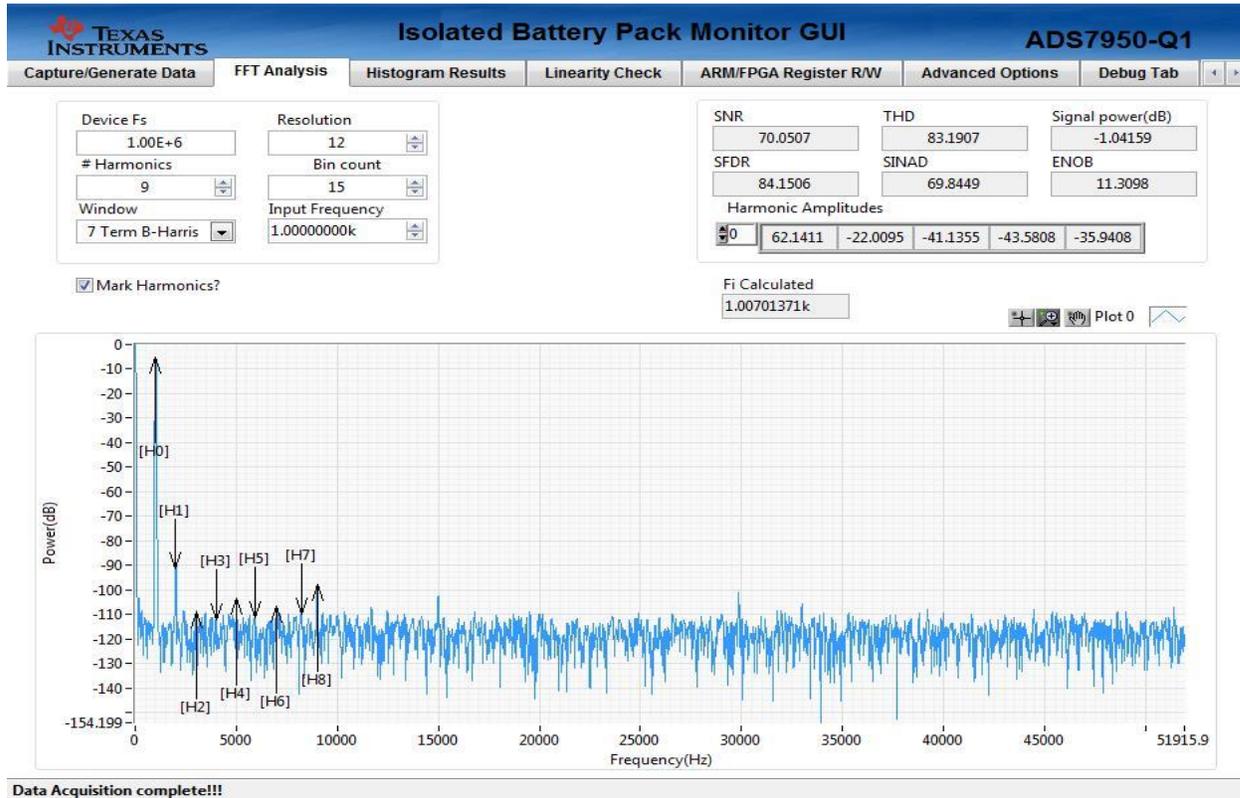


Figure 21: AC Performance Check

6 PCB Design

The electrical schematic and Bill of Materials for this design can be found in the Appendix A.

PCB Layout

The layout of a current measuring system is equally important as choosing the correct shunt resistor and the proper analog digital converter. Poor layout techniques could result in severed traces, messy loops, signal path oscillations, magnetic contamination which all can contribute to the worse system performance.

No right angle or orthogonal connection: Avoid right angle or orthogonal connections for traces carrying current because these kinds of routings could result in current crowding, localized heating of the trace and trace resistance change.

Arcs or 45 degree trace connection: Utilize either arcs or 45 degree crossed traces in routing large current flow traces will maintain uniform current flow throughout the trace.

Wide and balanced trace to shunt: Make the traces wide and balanced between the connectors and shunt resistor can reduce the trace resistance, thus avoiding cross traces.

Inner side connection: Connect current sense lines to the inner side of the shunt resistor footprint to get the optimal performance.

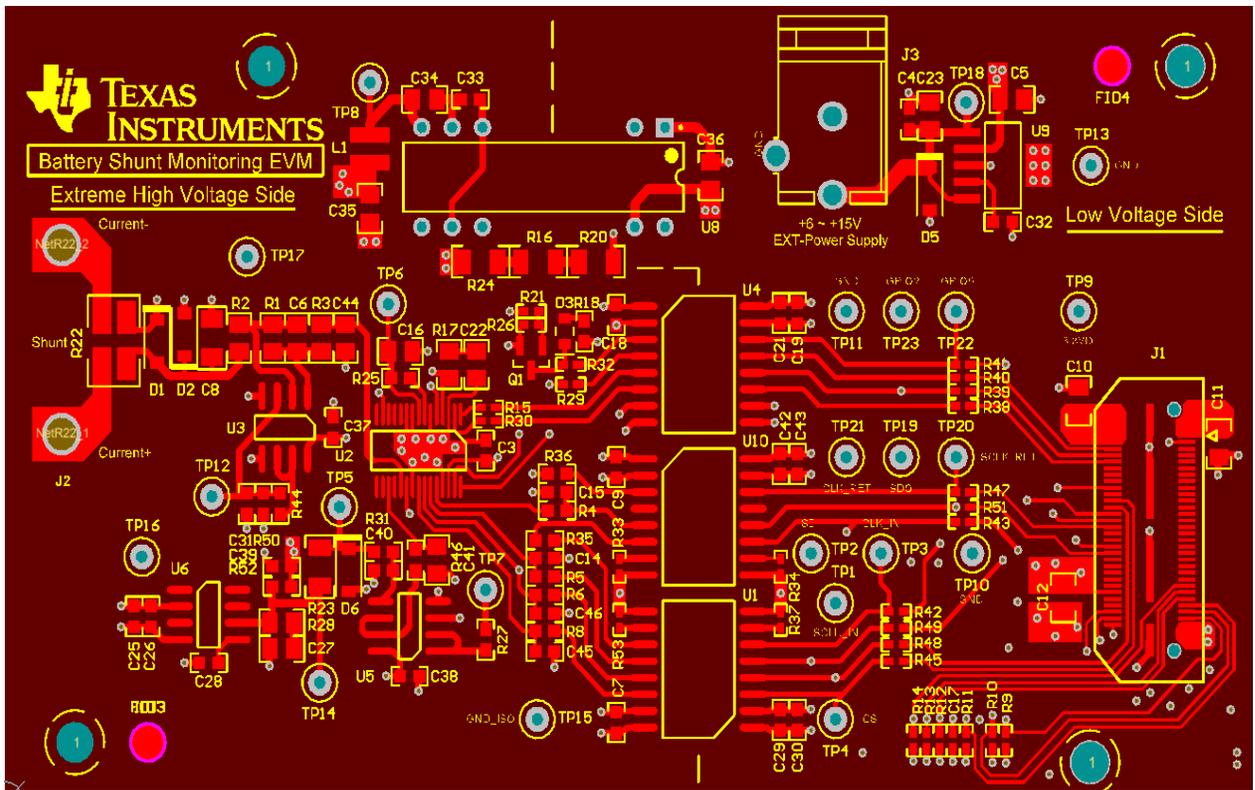


Figure 22: Top Layer Layout _ L1

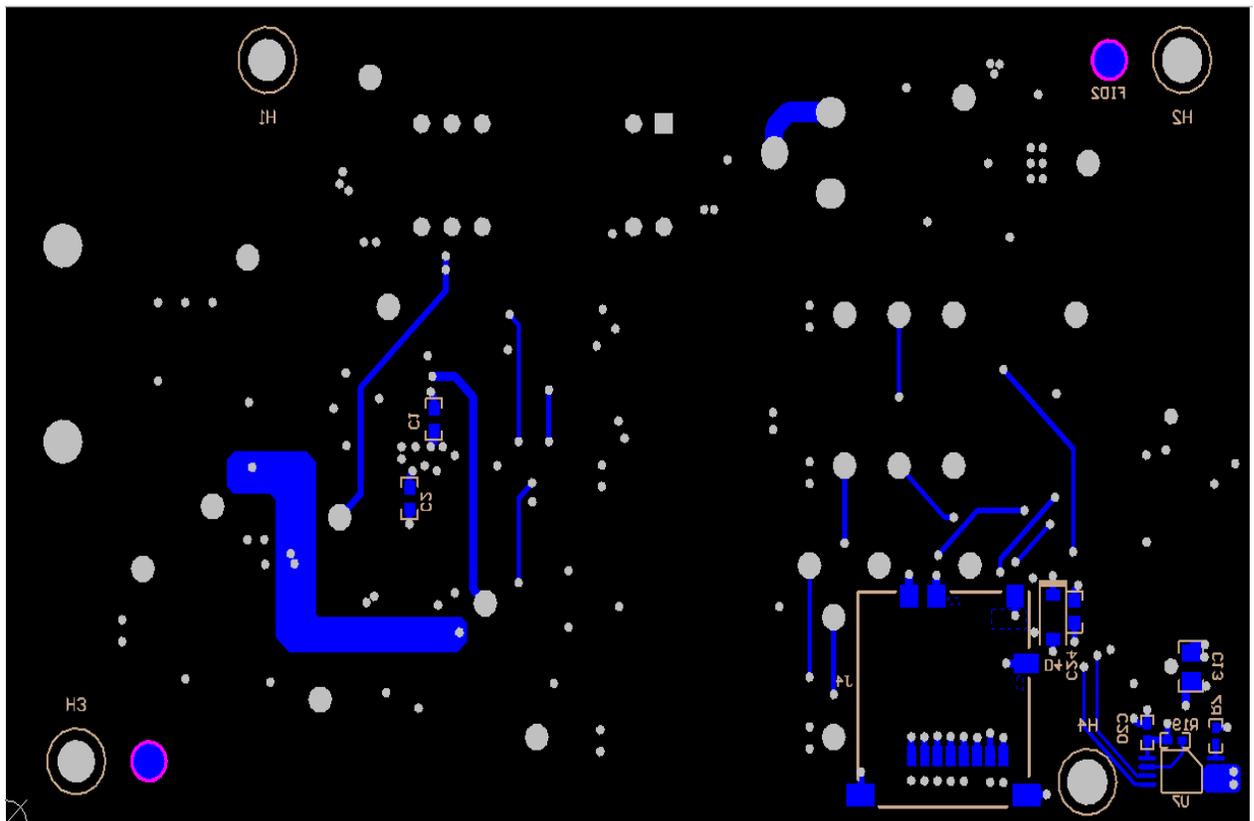


Figure 23: Bottom Layer Layout _ L4

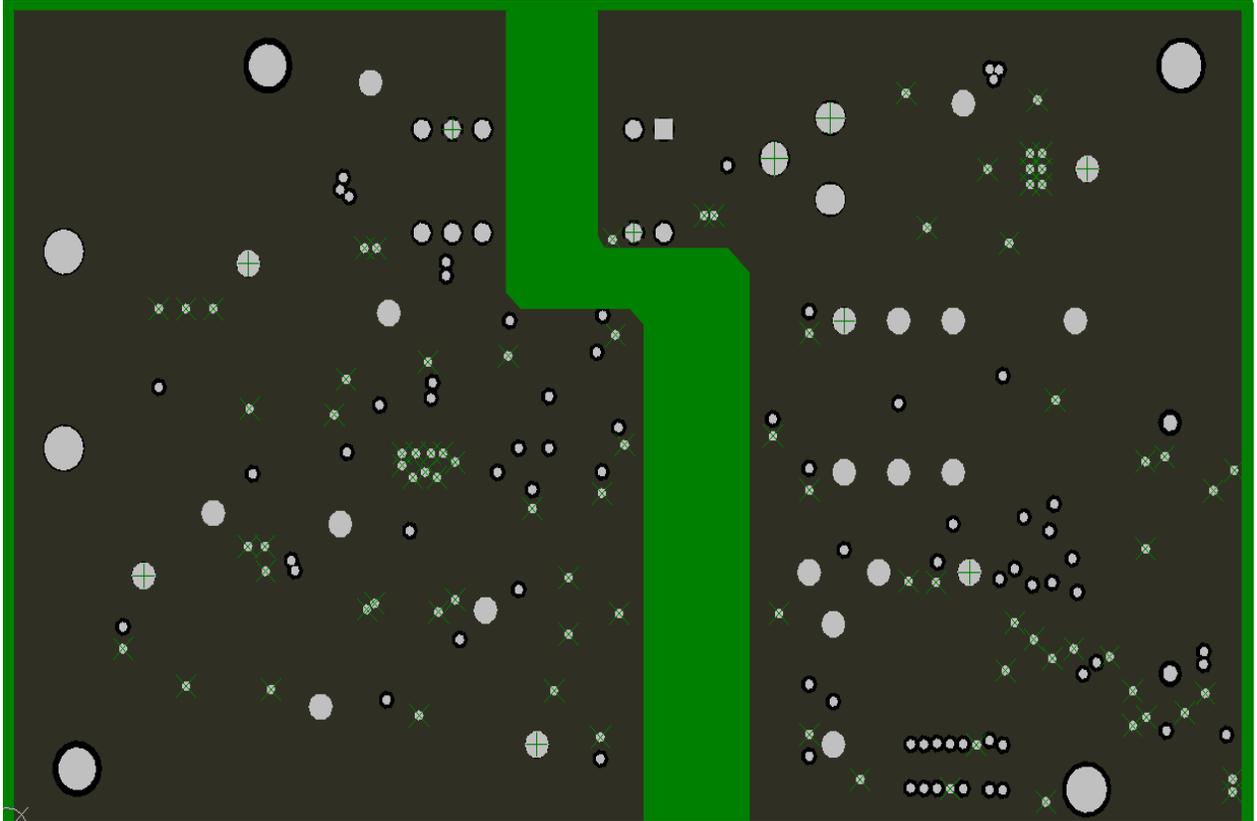


Figure 24: Ground Layer Layout _ L2

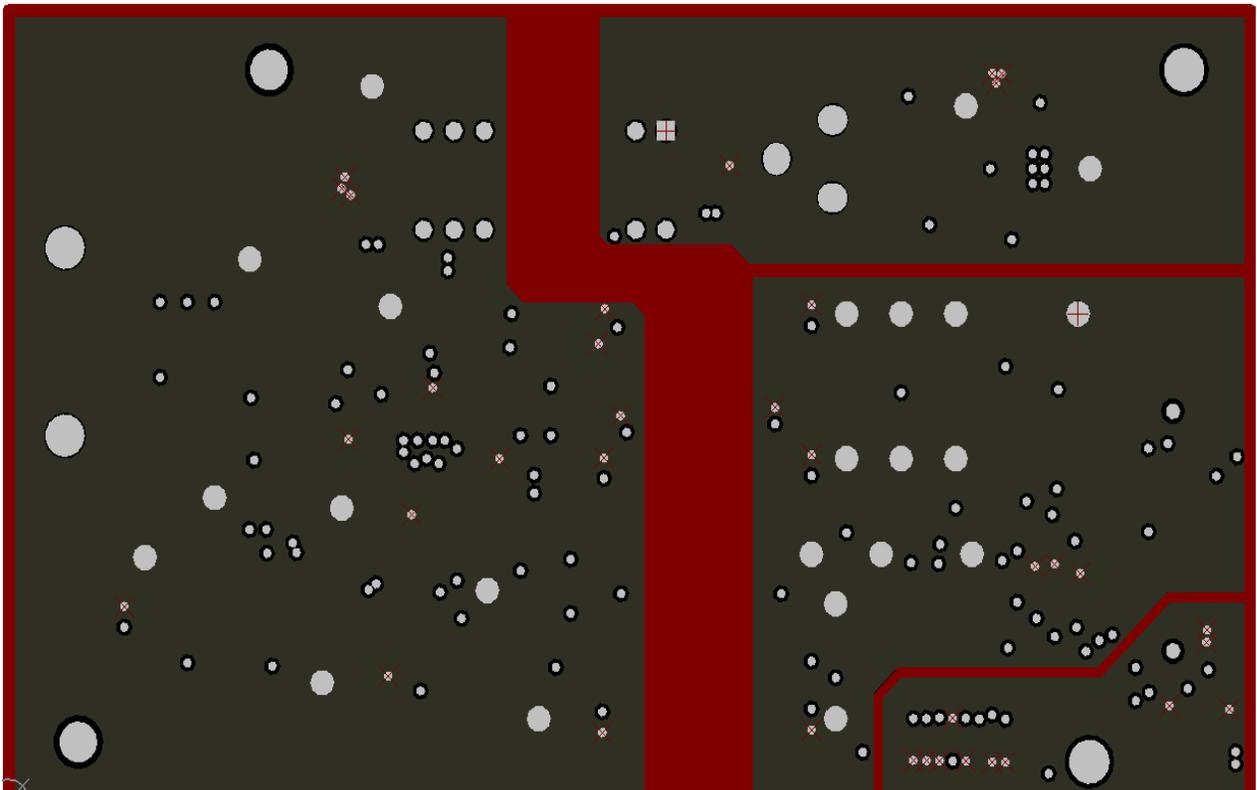


Figure 25: Power Layer Layout _ L3

7 Modifications

The components selected for this design are optimized to meet the design goals mentioned in Section 1 at the beginning of this design. However, there are other current sensing solutions which can be used. For instance, INA213A-Q1 and INA225-Q1, automotive qualified precise current shunt monitors from Texas Instruments can be other choices to sense the load current, connected to ADS7950-Q1 to achieve an isolated current measurement for automotive battery pack monitoring application.

Figure 26 shows a circuit utilizing INA213A-Q1 (Gain=50) to measure the load current by an 8mΩ shunt resistor, measuring the battery voltage by a resistor divider circuit. IG1 is a ±5App (peak-peak), 1kHz sinusoidal current signal source. The battery voltage is set to 100V in this TINA circuit.

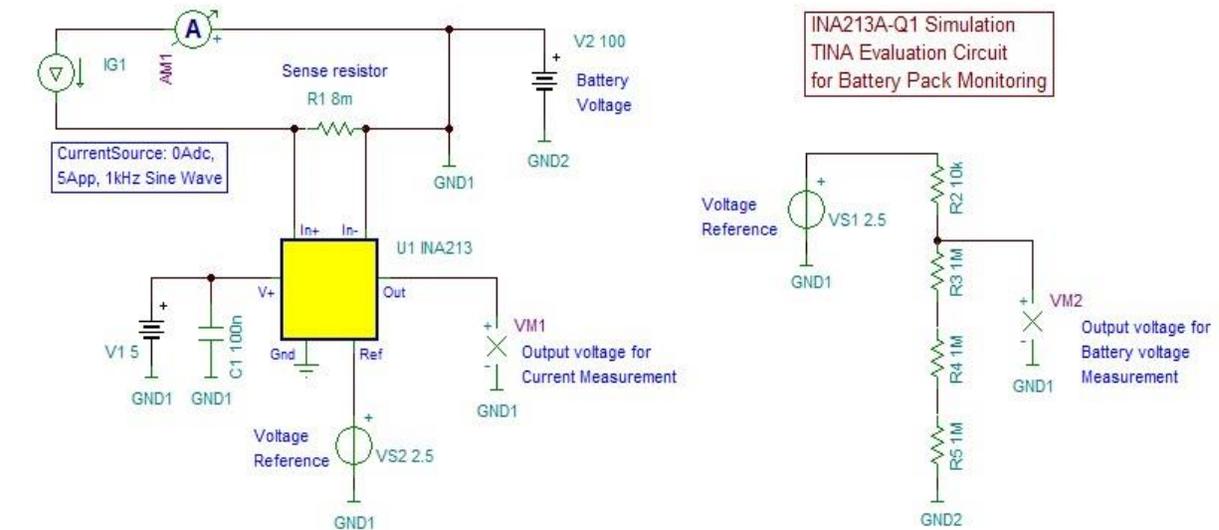


Figure 26: INA213A-Q1 Monitoring Solution

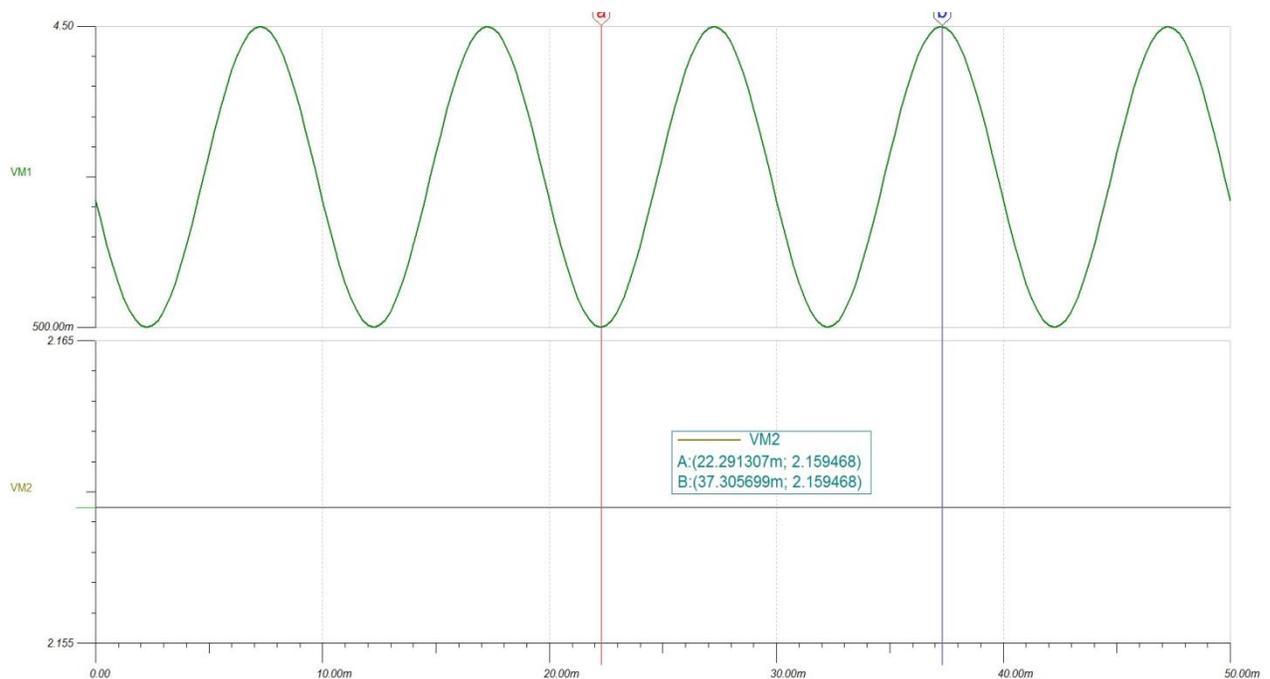


Figure 27: Simulation Result for INA213A-Q1 Monitoring Solution

The simulation result is shown in [Figure 27](#). The VM1 is a sensed voltage signal after the amplification of INA213-Q1, this is an output signal varying with the current signal and its amplitude sweeps from 0.5V to 4.5V, which can precisely meet the input requirement of ADS7950-Q1 with 0.5V headroom voltage.

According to the Equation (11) and (12), the difference voltage (V_{diff}) fed to ADS7950-Q1 can be calculated as below:

$$V_{REF} = V_{Battery} + V_{REF_Rating} = 100 + 2.5 = 102.5V$$

$$V_{HV} = \frac{3M}{3M + 10k} \times (100 + 2.5) = 102.159468V$$

$$V_{diff} = V_{HV} - V_{ISO-GND} = 102.159468V - 100V = 2.159468V$$

The VM2 in [Figure 27](#) is a divided voltage signal for battery voltage measurement, which is stable and the value is 2.159468V, this simulated signal value is exactly same as the calculated result. This voltage signal can be fed to ADS7950-Q1 and the sampled code can be retrieved, then the battery voltage can be calculated with the code according to Equation (14).

8 About the Author

Dale Li is an Application Engineer in the Precision Analog, SAR ADC team at Texas Instruments based in Tucson, Arizona. Before joining TI since 2007, Dale was a system design and application engineer in several different industries.

9 Acknowledgements & References

9.1 Acknowledgements

Special thanks to Tim Green at Precision Linear team of Texas Instruments for his significant contributions to this design, including the solution and model. Also thanks to, Luis Chioye and Rafael Ordonez at SAR ADC team of Texas Instruments for their many suggestions and discussions during the whole process.

9.2 References

1. Vinay Agarwal; 18-Bit, 1-MSPS Data Acquisition (DAQ) Block Optimized for Lowest Power, TI Precision Designs, available: [TIPD113](#)
2. ADS7950-Q1 Datasheet, available: [ADS7950-Q1](#)

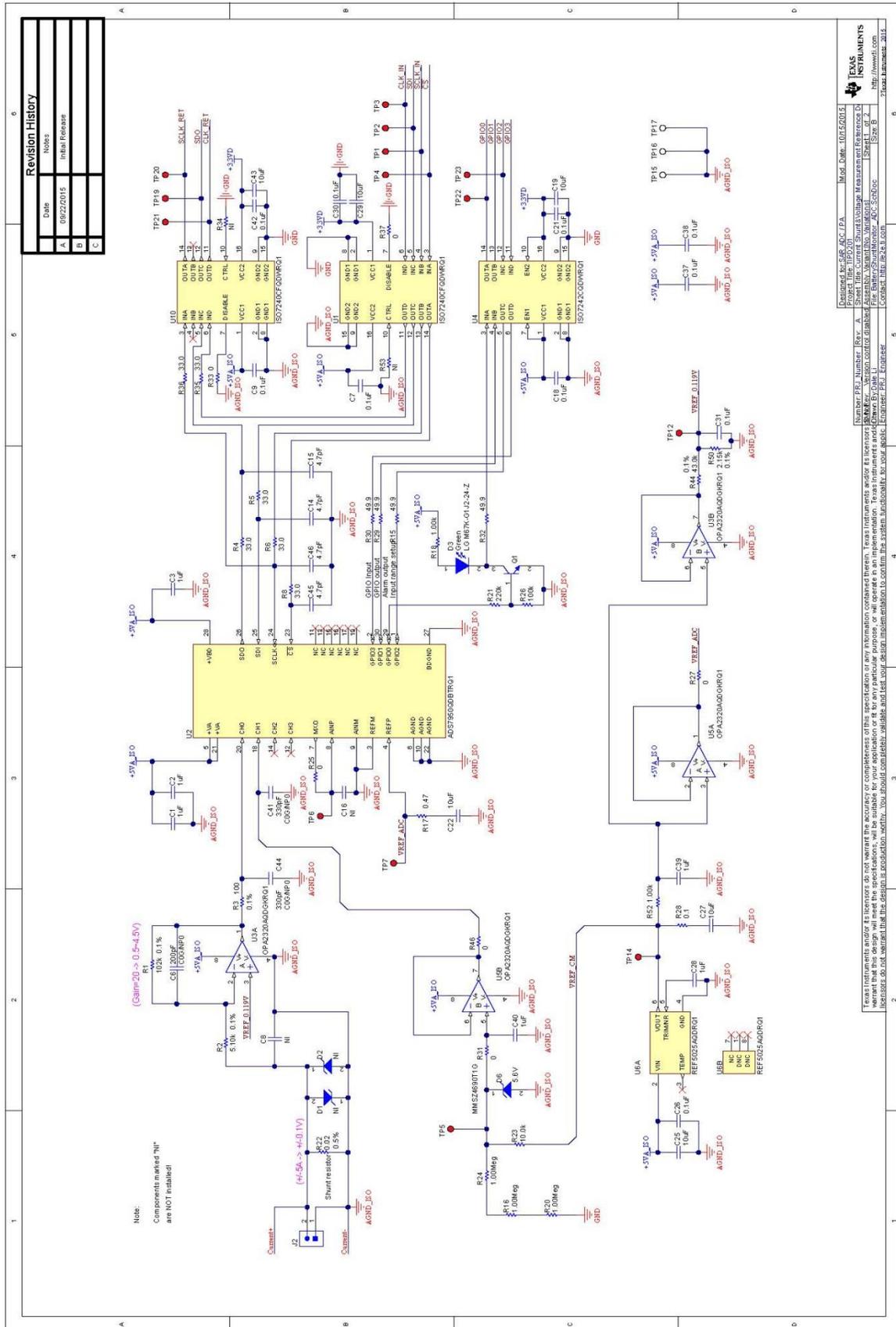


Figure 29: Electrical Schematic - Power and Interface

A.2 Bill of Materials

ITEM	Quantity	Manufacturer	PartNumber	Designator	Description	Value
1	8	Taiyo Yuden	UMK107AB7105KA-T	C1, C2, C3, C24, C28, C33, C39, C40	CAP, CERM, 1 uF, 50 V, +/- 10%, X7R, 0603	1uF
2	11	Kemet	C0603C104K5RACTU	C4, C7, C9, C18, C21, C26, C30, C31, C37, C38, C42	CAP, CERM, 0.1uF, 50V, +/-10%, X7R, 0603	0.1uF
3	7	Samsung	CL21A106KAFN3NE	C5, C10, C11, C12, C13, C22, C27	CAP, CERM, 10uF, 25V, +/-10%, X5R, 0805	10uF
4	1	MuRata	GRM2165C2A201JA01D	C6	CAP, CERM, 200 pF, 100 V, +/- 5%, COG/NP0, 0805	200pF
5	1	TDK	NI	C8	Not Installed	
6	4	AVX	06035A4R7CAT2A	C14, C15, C45, C46	CAP, CERM, 4.7 pF, 50 V, +/- 5%, COG/NP0, 0603	4.7pF
7	1	AVX	NI	C16	Not Installed	
8	2	TDK	C1005X7R1H104K	C17, C20	CAP, CERM, 0.1uF, 50V, +/-10%, COG/NP0, 0402	0.1uF,NI
9	4	TDK	C1608X5R1E106M080AC	C19, C25, C29, C43	CAP, CERM, 10uF, 25 V, +/- 20%, X5R, 0603	10uF
10	2	TDK	C2012X5R1V226M125AC	C23, C35	CAP, CERM, 22 uF, 35 V, +/- 20%, X5R, 0805	22uF
11	1	TDK	C1608X7R1H103K	C32	CAP, CERM, 0.01uF, 50V, +/-10%, X7R, 0603	0.01uF
12	2	TDK	C2012X5R1H225K125AB	C34, C36	CAP, CERM, 2.2uF, 50V, +/-10%, X5R, 0805	2.2uF
13	2	AVX	08051A331JAT2A	C41, C44	CAP, CERM, 330 pF, 100 V, +/- 5%, COG/NP0, 0805	330pF
14	1	Susumu Co Ltd	RG2012P-1023-B-T5	R1	RES, 102k ohm, 0.1%, 0.125W, 0805	102k
15	1	Susumu Co Ltd	RG2012P-512-B-T5	R2	RES, 5.10k ohm, 0.1%, 0.125W, 0805	5.10k
16	1	Susumu Co Ltd	RG2012P-101-B-T5	R3	RES, 100 ohm, 0.1%, 0.125W, 0805	100
17	6	Vishay-Dale	CRCW060333R0FKEA	R4, R5, R6, R8, R35, R36	RES, 33.0 ohm, 1%, 0.1W, 0603	33
18	7	Vishay-Dale	CRCW040210K0FKED	R7, R9, R10, R11, R12, R13, R14	RES, 10.0k ohm, 1%, 0.063W, 0402	10.0k
19	14	Vishay-Dale	CRCW040249R9FKED	R15, R29, R30, R32, R38, R39, R40, R41, R42, R43, R45, R47, R48, R49	RES, 49.9 ohm, 1%, 0.063W, 0402	49.9
20	3	Vishay-Dale	CRCW12061M00FKEA	R16, R20, R24	RES, 1.00Meg ohm, 1%, 0.25W, 1206	1.00M
21	1	Panasonic	ERJ-6RQFR47V	R17	RES, 0.47 ohm, 1%, 0.125W, 0805	0.47
22	2	Yageo America	RT0603BRD071KL	R18, R52	RES, 1.00 k, 0.1%, 0.1 W, 0603	1.00k
23	1	Vishay-Dale	NI	R19	Not Installed	
24	1	Vishay-Dale	CRCW0402220KJNED	R21	RES, 220k ohm, 5%, 0.063W, 0402	220k
25	1	Ohmite	LVK20R020DER	R22	RES, 0.02 ohm, 0.5%, 0.75W, 2010	0.02
26	1	Vishay-Dale	CRCW120610K0FKEA	R23	RES, 10.0k ohm, 1%, 0.25W, 1206	10.0k
27	4	Vishay-Dale	CRCW06030000Z0EA	R25, R27, R31, R46	RES, 0, 5%, 0.1 W, 0603	0
28	1	Vishay-Dale	CRCW0402100KFKED	R26	RES, 100k ohm, 1%, 0.063W, 0402	100k
29	1	Panasonic	ERJ-6RSJR10V	R28	RES, 0.1 ohm, 5%, 0.125W, 0805	0.1
30	3	Yageo America	RC0402JR-070RL	R33, R37, R51	RES, 0 ohm, 5%, 0.063W, 0402	0, 0, 0, 0, 0
31	2	Yageo America	NI	R34, R53	Not Installed	
32	1	Susumu Co Ltd	RG1608P-433-B-T5	R44	RES, 43.0 k, 0.1%, 0.1 W, 0603	43.0k
33	1	Susumu Co Ltd	RG1608P-2151-B-T5	R50	RES, 2.15 k, 0.1%, 0.1 W, 0603	2.15k
34	1	Vishay-Dale	CRCW04020000Z0ED	R54	RES, 0, 5%, 0.063 W, 0402	0
35	2	ON Semiconductor	NI	D1, D2	Not Installed	
36	1	OSRAM	LG M67K-G1J2-24-Z	D3	LED, Green, SMD	Green
37	1	ON Semiconductor	MMSZ4686T1G	D4	Diode, Zener, 3.9V, 500mW, SOD-123	3.9V

ITEM	Quantity	Manufacturer	PartNumber	Designator	Description	Value
38	1	ON Semiconductor	MMSZ4702T1G	D5	Diode, Zener, 15V, 500 mW, SOD-123	15V
39	1	ON Semiconductor	MMSZ4690T1G	D6	Diode, Zener, 5.6V, 500mW, SOD-123	5.6V
40	1	ON Semiconductor	BC847CLT1G	Q1	Transistor, NPN, 45V, 0.1A, SOT-23	0.7V
41	1	Samtec	QTH-030-01-F-D-A	J1	Connector, 60-pin Header, .5mm pitch	QTH-030-01-F-D-A
42	1	MuRata	LQH3NPN150NG0	L1	Inductor, Wirewound, Ferrite, 15 uH, 0.37A, 0.91 ohm, SMD	15 uH
43	1	On-Shore Technology	ED555/2DS	J2	Terminal Block, 6A, 3.5mm Pitch, 2-Pos, TH	
44	1	CUI Inc.	PJ-102A	J3	Connector, DC Jack 2.1X5.5 mm, TH	
45	1	Molex	502570-0893	J4	SD Memory Card Connector	
46	17	Keystone	5000	TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP12, TP14, TP18, TP19, TP20, TP21, TP22, TP23	Test Point, Miniature, Red, TH	Red
47	6	Keystone	5002	TP10, TP11, TP13, TP15, TP16, TP17	Test Point, Miniature, White, TH	White
48	2	Texas Instruments	ISO7240CFQDWRQ1	U1, U10	Automotive Quad, 4/0, 25 Mbps Digital Isolator, 3.3 V/5 V, -40 to +125 degC, 16-pin SOIC	
49	1	Texas Instruments	ADS7950QDBTRQ1	U2	Automotive 12-Bit, 1 MSPS, 4-Channel, Single-Ended, MicroPower, Serial Interface ADC	
50	2	Texas Instruments	OPA2320AQDGKRQ1	U3, U5	Automotive Precision, 20MHz, 0.9pA, Low-Noise, RRIO, CMOS Operational Amplifier	
51	1	Texas Instruments	ISO7242CQDWRQ1	U4	Automotive Quad Channels, 2/2, 25 Mbps Digital Isolator, -40 to +125 degC, 16-pin SOIC	
52	1	Texas Instruments	REF5025AQDRQ1	U6	Automotive Catalog, Low Noise, Very Low Drift, Precision Voltage Reference, -40 to 125 degC, 8-pin SOIC	
53	1	Atmel	AT24C32D-XHM-T	U7	Automotive grade I2C Serial EEPROM 32-Kbit (4096 x 8), TSSOP-8	
54	1	Texas Instruments	DCR010505P	U8	Miniature, 1 W Isolated Regulated DC-DC Converter, 10-pin DIP	
55	1	Texas Instruments	REG104GA-5	U9	Single Output Fast Transient Response LDO, 1 A, Fixed 5 V Output, 2.1 to 15 V Input, 6-pin SOT-223	

Figure A-3: Bill of Materials

Appendix B.

B.1 Gain and Offset Calibration

Gain and offset errors from the components of the signal path can contribute to errors affecting the whole system. However, these errors can be calibrated in order to achieve higher accuracy. The calibration can be performed by feeding two known reference input signals and calculating a calibration gain and offset to compensate for the input readings. The achievable accuracy using calibration is largely dependent on the accuracy of the known references fed into the acquisition system.

The equations used to measure the actual gain and offset of whole acquisition system and calculate the calibration gain and offset are derived as follows. Using two known signals (xL , yL) and (xH , yH), the actual system offset and gain errors can be calculated and then the calibration gain and offset can be known using the following formulas.

$$y = (x \times Gain_{act}) + Offset_{act}$$

$$Gain_{act} = \frac{yH - yL}{xH - xL}$$

Where, $Gain_{act}$ = actual Gain,

$Offset_{act}$ = actual Offset,

xL = known low input signal; xH = known high input signal,

yL = output for xL , yH = output for xH .

$$Offset_{act} = yL - (xL \times Gain_{act})$$

The calibration equation is shown in Equation (34):

$$x = (y \times Gain_{cal}) - Offset_{cal} \quad (34)$$

$$Gain_{cal} = \frac{xH - xL}{yH - yL} \quad (35)$$

$$Offset_{cal} = yL \times Gain_{cal} - xL \quad (36)$$

Where, $Gain_{cal}$ = Gain calibration factor,

$Offset_{cal}$ = Offset calibration factor.

The system calibration process involves the following five basic steps:

1. Measure the signal connected to the input of the whole acquisition system.
2. Read the ADC output codes when known signals are applied on the input of system, (yL and yH).
3. Calculate the system gain calibration factor ($Gain_{cal}$) using Equation (35).
4. Calculate the system offset calibration factor ($Offset_{cal}$) using Equation (36).
5. Cycle through all codes applying the calibration Equation (34).

Cautions and Warnings

WARNING:

The test for high voltage is dangerous, especially for hundreds of volts or higher, it can possibly cause deaths, so please proceed with maximum caution and never handle the device or test alone.

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