TI Designs

Interface to Sin/Cos Encoder With Sitara AM437x

TI Designs

The TIDA-00178 reference design is an EMC-compliant industrial interface to Sin/Cos position encoders. Applications include industrial drives, which require accurate speed and position control.

The design uses a 16-bit dual sample ADC with drop-in compatible 14- or 12-bit versions available, allowing for optimization of performance and cost. The TIDA-00178 provides a direct connection to Sitara AM437x using SPI and QEP. For quick evaluation, it features a 60-pin connector that directly fits the AM437x IDK. An example firmware for Sitara AM437x IDK is provided, which outputs the measured angle from the Sin/Cos encoder with up to a 28-bit resolution through the Sitara's USB virtual COM port.

Design Resources

TIDA-00178	Design Folder
ADS8354	Product Folder
THS4531A	Product Folder
TLV3202	Product Folder
REF2025	Product Folder
TPS5401	Product Folder
SN74LVC3G17	Product Folder
TIDA-00176	Tools Folder
Sitara AM437x IDK	Tools Folder

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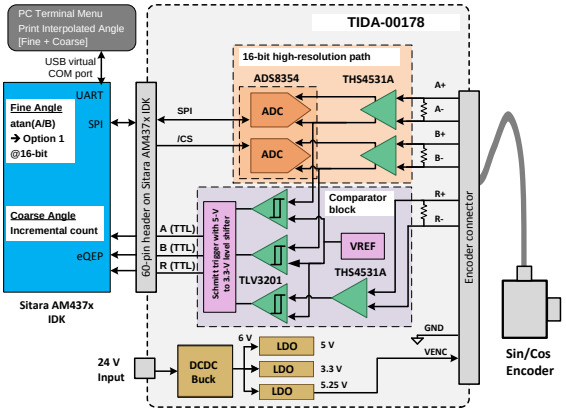
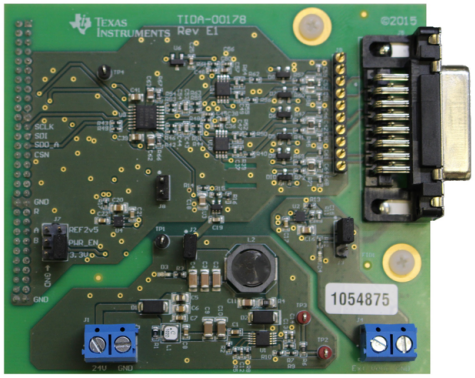
Design Features

- EMC-Compliant Industrial Interface Design for Sin/Cos Encoders With 1-V_{PP} Differential Output at 2.5-V Offset, Input Frequencies up to 500 kHz
- High-Resolution Interpolated Position, up to 28-bit Resolution, Cable Length Tested up to 70 m
- Fully Differential Analog Signal Chain for High Common-Mode Noise Immunity With Dual 16-Bit ADC With Drop-in Compatible 14- or 12-bit ADC Pending Desired Resolution
- Easy to Connect to Sitara AM437x With SPI and QEP Interface, Connects Directly to AM437x IDK 60-Pin Header
- Example Firmware for Sitara AM437x With High-Resolution Angle Calculated at 32 kHz and Angle Data Send Through USB Virtual COM Port for Easy Performance Evaluation
- Designed for IEC61000-4-2,4-4, and 4-5 (ESD, EFT, and Surge EMC Immunity Requirements)

Featured Applications

- Servo Drives
- Industrial Drives
- Factory Automation and Control





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1 System Description

1.1 TI Design Overview

This TI design implements an industrial temperature, EMC-compliant interface to Sin/Cos incremental position encoders with 1-V_{PP} differential analog output signals and frequencies up to 500 kHz and a 5-V supply voltage. The major building blocks of this TI design are the dual path analog signal chain, the high-speed comparator block, the power management block, and the interfaces to the Sin/Cos encoder as well as the interface to the Sitara AM437x processor for digital signal processing and high-resolution position calculation. A simplified system block diagram is shown in Figure 1, with the TI hardware design represented by the box in light green.

To allow for easy evaluation of this TI design, an example firmware is provided for the Sitara AM437x Industrial Development Kit. The AM437x host processor calculates the high-resolution angle position for the analog signal path. This path is leveraging the external 16-bit dual ADC through SPI. The angle is calculated with up to 28-bit resolution and output for evaluation through USB virtual COM port.

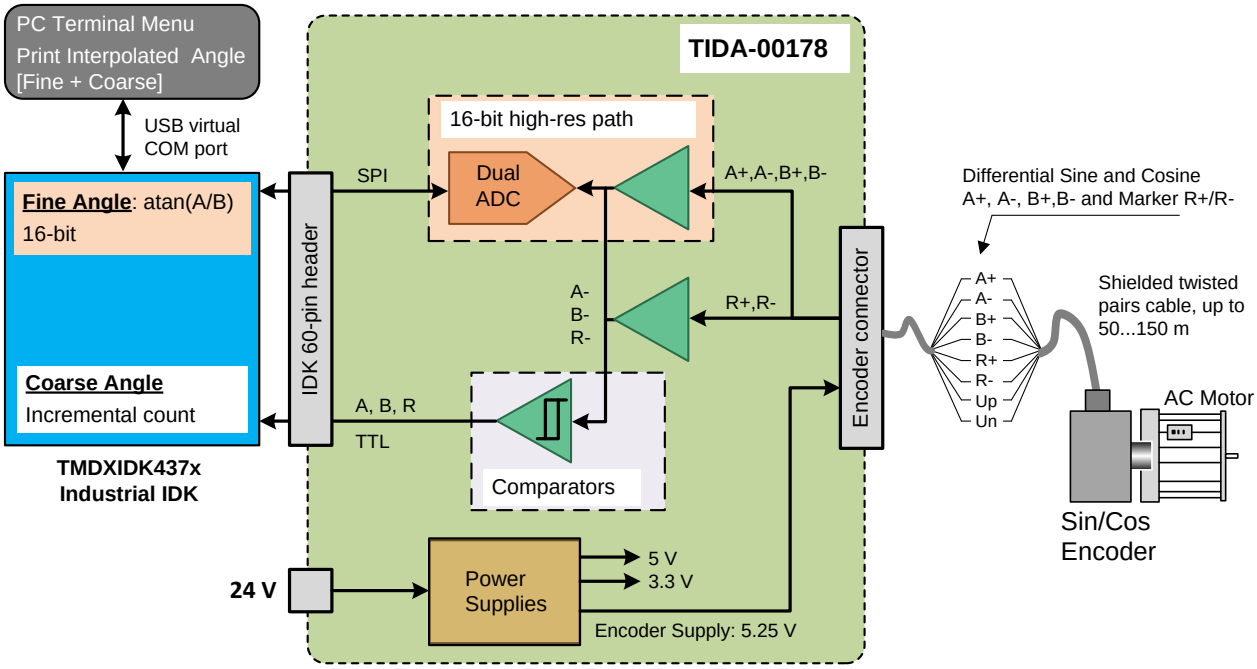

Figure 1. Simplified System Block Diagram of TIDA-00178 With Sitara Industrial Development Kit

The analog signal chain provides a 120-Ω termination with EMC protection. The differential 1-V_{PP} sine and cosine input signals are amplified and level-shifted, respectively. The signal path option is provided using an onboard external high-speed, high-resolution dual 16-bit simultaneous sampling ADC with SPI.

The comparator block features a high-speed, low-propagation delay and adjustable hysteresis for better noise immunity and converts the analog signals A, B, and the marker R into digital signals with 3.3-V TTL-level to interface to a quadrature encoder pulse module like the QEP peripheral on the Sitara AM437x processor.

The onboard wide input range 24-V power supply provides the necessary voltages for analog signal chain as well as the 5.25-V supply voltage for the Sin/Cos encoder.

The Sin/Cos encoder can be either connected to a 15-pin shielded Sub-D connector or a 10-pin header. The interface to the host processor provides the digital signals for SPI and A, B, and R with 3.3-V I/O. The digital output signals A, B, and R are often referred to as "ABZ" signals.

The design is designed to meet the IEC61000-4-2, 4-4, and 4-5 (ESD, EFT, and Surge) as specified in the IEC 61800-3 standard for EMC immunity requirements and specific test methods applicable in adjustable speed, electrical-power drive systems.

1.2 Analog Sin/Cos Incremental Encoder

Incremental rotary or linear position encoders are used in many applications to measure angular or linear position and speed. Depending on the application, encoders with TTL/HTL-output signals or analog sinusoidal output signals are used. The latter is often referred as a Sin/Cos encoder. Analog Sin/Cos incremental encoders enable high-resolution position measurement. The high quality of the sinusoidal incremental signals permits high interpolation factors for digital speed control. Application areas include electrical motors, machine tools, printing machines, woodworking machines, textile machines, robots, and handling devices as well as various types of measuring, testing, and inspection devices.

1.2.1 Sin/Cos Encoder Output Signals

There are typically two sensing methods implemented with encoders, either based on optical or inductive sensing. With optical rotary encoder, the encoder disc modulates a light beam whose intensity is sensed by photo-electrical cells. These produce two 90-degree phase-shifted sinusoidal incremental signals A and B. B lags A with clockwise rotating viewed from the shaft of the encoder. The number of periods of the signals A and B over one mechanical revolution equals the line count N of the encoder. A further track carries the reference marker R, which occurs once per mechanical revolution. The reference marker allows for an absolute angle position measurement.

The frequency of the of the Sin/Cos encoder's differential output signal depends on the line count of the encoder as well as the mechanical speed, as outlined in Equation 1.

$$f_{A\_B}(\text{Hz}) = N \times (\text{rpm}) \times \frac{1}{60} \quad (1)$$

N represents the Sin/Cos encoder line count and v the encoder shaft mechanical speed in rpm.

Figure 2 provides an overview on the output frequency for encoders with line counts N = 100, 1000, and 2000 versus the mechanical speed.

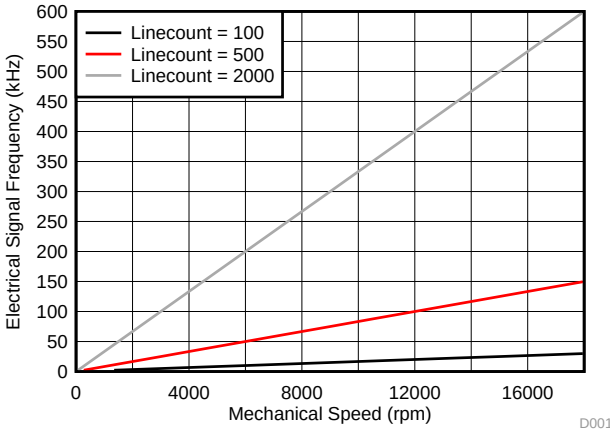

Figure 2. Electrical Frequency of SinCos Encoder Output Signals A and B versus Mechanical Speed and Line Count

For example, a Sin/Cos encoder with a line count of N = 2000 running at a mechanical speed of 12000 rpm outputs the signals A and B with a frequency of 400 KHz.

Sin/Cos encoders with a 1-V_{PP} interface provide the differential analog output signals A (A+, A–) and B (B+, B–) with 1 V_{PP} and typically a 2.5-V DC offset. The differential reference mark signal R (R+, R–) is typically slightly lower amplitude and the peak occurs only once per revolution. Figure 3 shows the differential output signals A, B, and R. Note that A, B, and R represent the differential signal of A+ minus A–, B+ minus B–, and R+ minus R–, respectively.

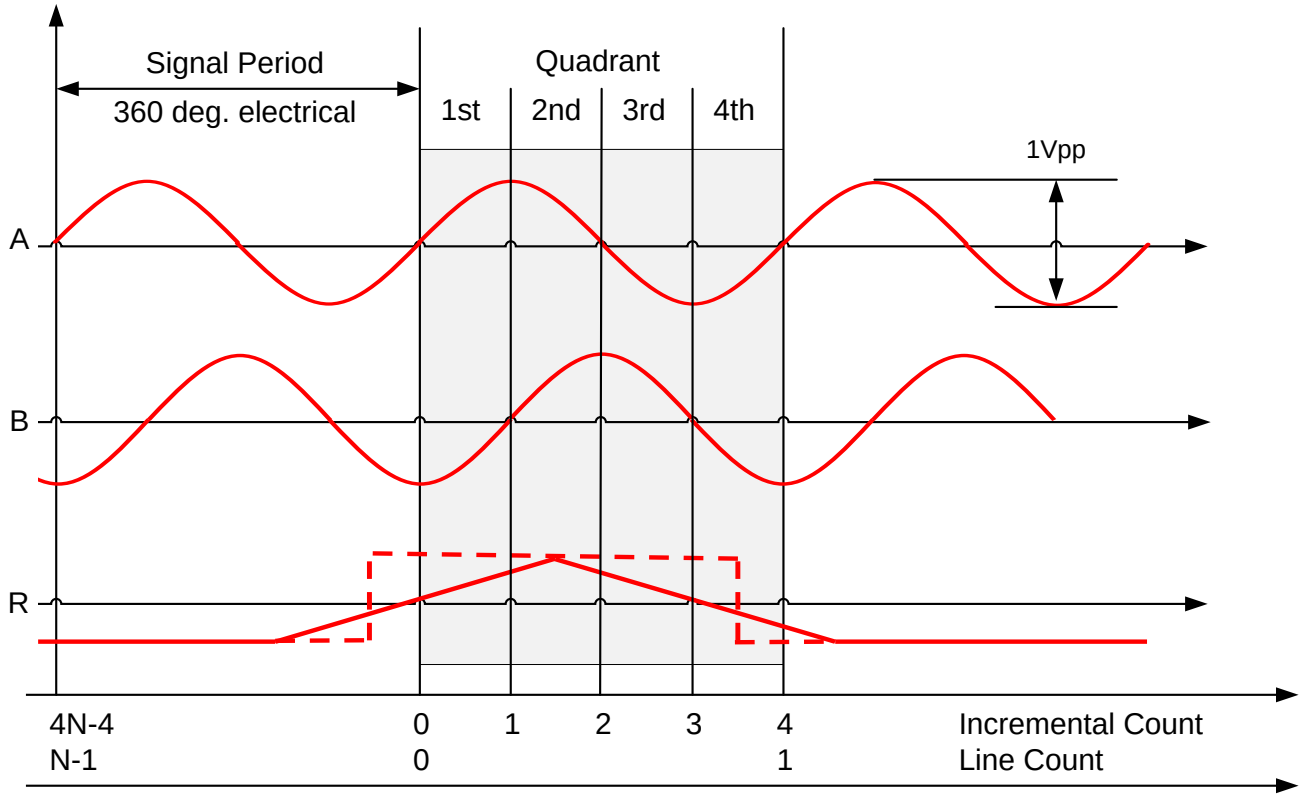

Figure 3. Output Voltage Signals A, B, and Marker R of Sin/Cos-Encoders With N Line Counts per Revolution

1.2.2 Sin/Cos Encoder Electrical Parameter Examples

To understand the requirements for an electrical interface module to Sin/Cos encoders, some example industrial Sin/Cos encoder models have been analyzed. The corresponding parameters are listed in Table 1.

Table 1. Encoders Supply Voltage Examples

SIN/COS ENCODER MODEL	SUPPLY VOLTAGE	CURRENT CONSUMPTION
#1	5 V ±0.5-V DC	< 120 mA
#2	5V ±10%	150 mA
#3	5 V ±5%	70 mA (min)

The power supply of the Sin/Cos encoder needs to be within the above specifications.

The analog signal chain need to be specified to at least meet the following requirements with respect to signal amplitudes, offset, and maximum frequency.

Table 2. Encoder Output Signals A, B Examples

SIN/COS ENCODER MODEL	SIGNAL LEVEL A, B	DC OFFSET	LINE COUNT N	LIMIT FREQUENCY (–3 dB)
#1	0.6 to 1.2-V_{PP} 1-V_{PP} typical	2.5 V ±0.5 V	50 to 5000	≥ 180 kHz
#2	1 V_{PP} (20%, –40%)	2.5 V ±0.5 V	—	120 kHz
#3	1 V_{PP} (±10%)	2.5 V ±100 mV	1024 or 2048	400 kHz

Table 3. Encoder Output Signals Marker R Example

SIN/COS ENCODER MODEL	USABLE COMPONENT G AT REFERENCE MARK	QUIESCENT VALUE H OUTSIDE REFERENCE MARK	DC OFFSET
#1	0.5-V_{PP} typical, 0.2-V_{PP} min	–1.7 V	2.5 V

Table 4. Encoder Mechanical Parameter Example

SIN/COS ENCODER MODEL	SYSTEM ACCURACY	SHAFT MECHANICAL SPEED
#1	1/20 of grating period	< 16000 RPM

1.3 Method to Calculate High-Resolution Position With Sin/Cos Encoders

1.3.1 Theoretical Approach

1.3.1.1 Overview

From a hardware perspective, typically two approaches can be realized that impact mainly the requirements for the A/D converter.

With the "over-sampling method", both sine and cosine signal would be sampled at least four times higher than the maximum sine and cosine frequency. The incremental count as well as the phase calculation would be done by subsequent digital signal processing on a host processor. That method would not need comparators, but rather high-speed dual sampling ADCs.

The typically used "under-sampling method" uses separate hardware blocks to calculate the incremental count and the interpolated incremental phase. The advantage of that method is that the sampling frequency and bandwidth of the ADC can be lower compared to the first method, as it does not impact the incremental count but only the interpolated phase. However, the under-sampling method requires a comparator each for sine and the cosine to generate the digital quadrature encoded signals A and B, which drive a directional up and down counter, often referred to as quadrature encoded pulse counter. The analog bandwidth of the dual sampling ADC needs to be at least equal to the maximum sine/cosine frequency. The under-sampling method is outlined in Figure 4.

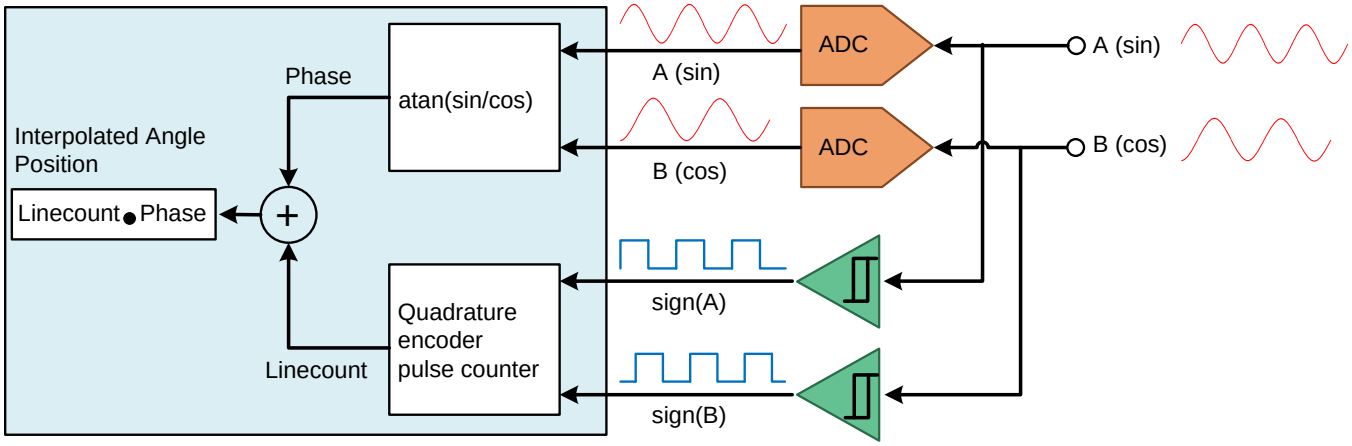

Figure 4. Signal Processing Block Diagram for Interpolated Angle Calculation

The total interpolated angular position is composed of coarse and fine angle. The interpolated angle is determined by the actual incremental line count and the phase within this incremental line. The phase within the incremental line is derived from the analog sine and cosine signals A and B at any specific time instant. Both the actual incremental count and the actual analog sine and cosine signals have to be latched at the same time. The fine angle is the phase of the sine and cosine, calculated with the inverse tangent function. The total interpolated angle is a compound of the coarse and fine angle, as shown in the simplified block diagram in Figure 1. The corresponding Equation 2 through Equation 4 are explained in the next section.

1.3.1.2 Coarse Resolution Angle Calculation

The incremental count and thus the incremental coarse angle can be determined by a counter that counts up when A is the leading sequence and counts down when B is the leading sequence. When digitized, both edges of A and B are counted. Therefore, one incremental count is equivalent to a 90° phase shift of both signals A and B (see Figure 3). The incremental count starts from 0 with the maximum incremental count $incr_{MAX}$ per Equation 2, where N is the line count:

$$incr_{MAX} = (4 \times N) - 1 \tag{2}$$

The incremental position Φ_{incr} can be calculated as:

$$\Phi_{incr}[deg] = \frac{360}{4 \times N} \times incr + \Phi_0 \tag{3}$$

where incr is the actual incremental count, N is the total line count, and Φ_0 the zero angle, determined by the reference marker R if used.

1.3.1.3 Fine Resolution Angle Calculation

The phase $\varphi_{A,B}$ of the sinusoidal signals A and B is used to interpolate the angle between two consecutive line counts, or four incremental steps, which are equivalent to each other. The phase $\varphi_{A,B}$ can be calculated by Equation 4:

$$\phi_{A,B}[deg] = \begin{cases} 90° + \tan^{-1}\left(\frac{B}{A}\right) & \text{if} \quad A \geq 0 \\ 270° + \tan^{-1}\left(\frac{B}{A}\right) & \text{if} \quad A < 0 \end{cases} \tag{4}$$

Only the ratio of the amplitudes of A and B is used, which is a common function of the encoder's rotation speed and supply voltage and do not affect the result.

1.3.1.4 Interpolated High-Resolution Angle Calculation

When the incremental count incr is matched to the phase $\varphi_{A,B}$ according to Table 5, the total interpolated angle Φ_{TOTAL} is calculated as:

$$\Phi_{TOTAL}[deg] = \left(\frac{360°}{N} \cdot (incr >> 2)\right) + \left(\phi_{A,B} \cdot \frac{1}{360°} \cdot \frac{360°}{N}\right) + \Phi_0 \tag{5}$$

CAUTION

The sinusoidal signals A and B and the incremental count incr must be latched simultaneously.

Table 5. Example for Relation Between Incremental Count to Phase and Phase Quadrant

INCREMENTAL COUNT	PHASE	QUADRANT
0	0 ≤ Phase < 90	1
1	90 ≤ Phase < 180	2
2	180 ≤ Phase < 270	3
3	270 ≤ Phase < 360	4
4	0 ≤ Phase < 90	1

1.3.1.5 Practical Implementation for Non-Ideal Synchronization

Practically, the digitized signals A_{TTL} and B_{TTL}, which are input to the quadrature encoder pulse counter, typically have a phase shift compared to the analog signals. This is mainly due to hysteresis and propagation delay of the comparators, as well as due to non-ideal synchronization between latching the incremental count and sampling the analog inputs A and B.

The impact of the hysteresis on the phase shift is almost independent of the signal frequency, but almost inverse proportional to the signal amplitude. The impact of a propagation delay and a non-ideal synchronization between sampling the analog signal and latching the incremental count is almost independent of the amplitude, but proportional to the frequency. Therefore, the maximum phase shift occurs at maximum Sin/Cos encoder frequency with minimum amplitude.

This means that at each transition to the next quadrant, the incremental counter is not updated immediately because of the phase lag, for example, as shown for the first quadrant in Figure 5.

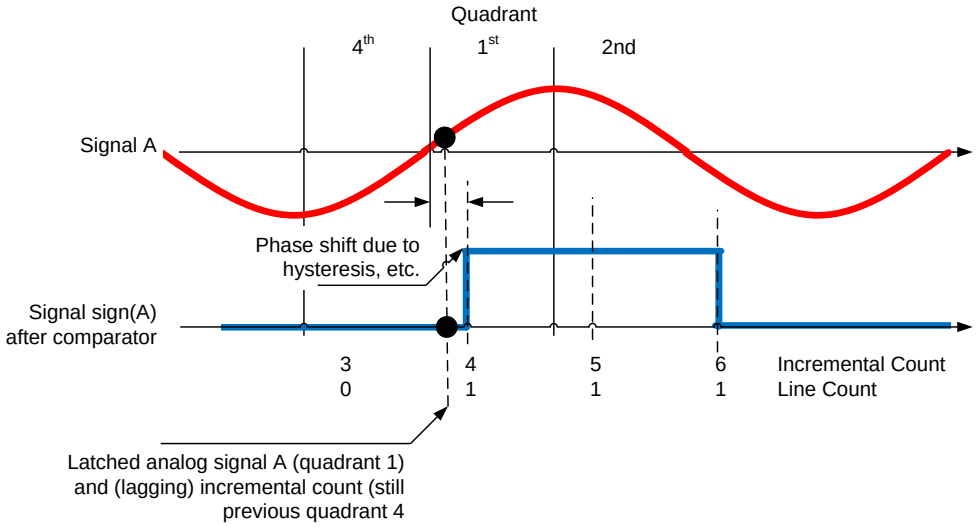

Figure 5. Phase Shift of A_{TTL} versus Analog Signal A Due to Phase Lag

The factors outlined cannot be omitted; therefore, a method needs to be applied to detect and correct these corner cases. Due to the ambiguity or the lower 2 bits of incremental line count and the analog phase, a correction method as outlined in Table 6 can be applied as long as the phase shift remains less than ±90°.

Since only the phase information is used to identify the quadrant, there are only two exceptions to consider, which occur during the transition from quadrant 4 to quadrant 1, or quadrant 1 to quadrant 4, depending on the rotation direction.

Table 6. Correction Method

INCREMENTAL COUNT (incr)	PHASE $\varphi_{A,B}$	CORRECTION METHOD
incr%4 = 3	0 ≤ Phase < 90	incr = incr + 1 if incr > 4 × N – 1, then incr = 0
incr%4 = 0	270 ≤ Phase < 360	incr = incr – 1 if incr < 0, then incr = 4 × N – 1

CAUTION

The correction method only works if the phase shift between the analog A and B and the digital signal A_{TTL} and B_{TTL} is less than ±90°.

A worst case calculation for this design is outlined in Section 1.4.

1.3.1.6 Resolution, Accuracy, and Speed Considerations

The ideal interpolated angle resolution is a function of the Sin/Cos encoder's line count and the resolution of the dual ADC. The equivalent interpolated angle resolution can be calculated as:

$$\Phi_{RESOLUTION}[bit] = \log 2(2 \times N) + ADC_{RESOLUTION}[bit] \quad (6)$$

Figure 6 illustrates the achievable interpolated angle resolution as a function of the line count for no interpolation, interpolation with an ideal 12-bit, and a 16-bit dual ADC.

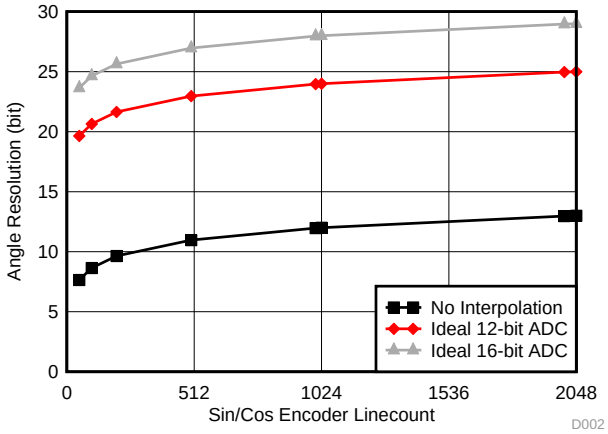

Figure 6. Ideal Interpolated Angle Resolution versus Line Count versus ADC Resolution

The ideal resolution with a Sin/Cos encoder with 2048 line counts using a 16-bit dual ADC equals 28-bit if the ADC's full-scale input range is used.

This high resolution is typically not required for position control, but is for very precise speed control, especially at lower mechanical speed. Figure 7 outlines the ideal speed resolution derived at a sample rate of 1.6 kHz without low-pass filtering. This assumes the industrial drive's speed closed-loop control runs 10 times lower than the current closed-loop control and PWM at 16 kHz.

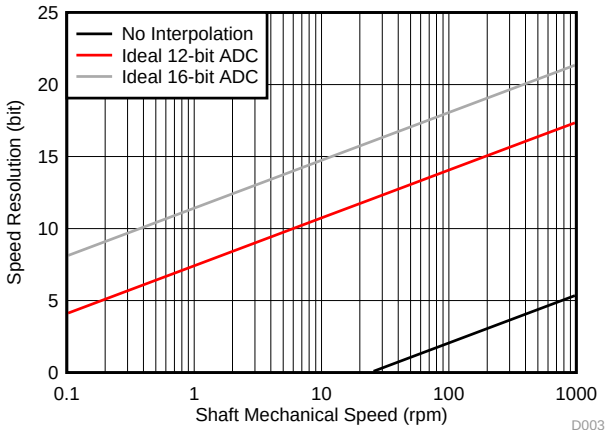

Figure 7. Ideal Speed Resolution versus Mechanical Speed at 1.6-kHz Sample Rate and Encoder With 1000 Line Count

Practically, low-pass filtering will be applied and improves resolution and immunity to noise; however, this is with a filter specific propagation (group) delay or latency.

1.4 Sin/Cos Encoder Parameters Impact on Analog Circuit Specification

To specify the analog circuit as outlined in Section 4, the following Sin/Cos encoder signal parameters (including support for longer cables) have been considered:

- Sin/Cos minimum and maximum peak-to-peak amplitude: Differential 0.3 to 1.2 V_{PP}, full-scale input range with at least 50% headroom (1.8 V_{PP})
- Sin/Cos offset voltage range: 2.5 V ±1 V
- Sin/Cos maximum frequency: 500 kHz
- Sin/Cos maximum slew rate: >2 V/µs
- Sin/Cos line termination: 120 Ω ±1%
- Encoder supply voltage and current: 5 V ±5%, 200 mA

1.4.1 Analog Signal Chain Design Consideration for Phase Interpolation

The high-resolution analog signal chain supports 16-bit resolution to provide a high interpolated angle resolution, especially for precision speed control.

The differential analog amplifier's AC noise floor and distortions should match the 16-bit resolution. With respect to a 1-V_{PP} input, this equals around 15 µV.

- Input voltage noise: 15 µV / √(1 MHz) = 15 nV/√(Hz)
- Input current noise: 15 µV / √(1 MHz) / R_{INPUT}, for R_{INPUT} = 1k equals 15 pA/SQRT(Hz)

Gain and offset are rather DC parameters and their drift is typically very slow as mainly related to temperature or aging. Initial offset and gain can be calibrated during initialization with specific algorithms even during the run time. Therefore, the requirements for these parameters can be slightly relaxed. The gain and offset drift over temperature each must be in the range of 10 LSB. With respect to a 1-V_{PP} input signal, this equals around 150 µV.

- Offset drift [0°C to 85°C]: 150 µV/85°C ~ 2 µV/°C
- Gain drift: [0°C to 85°C]: 160 ppm/85°C ~ 2 ppm/°C

For the gain setting, matched resistors (same package) are recommended.

1.4.2 Comparator Function System Design for Incremental Count

Referring back to Figure 5, the total propagation delay between the analog signal and the digital signals A_{TTL} and B_{TTL} at 500 kHz should be less than 90°, equivalent to 500 ns. The hardware should not contribute more than around 50 to 70% (equivalent to 250 to 350 ns) to leave headroom for, for example, hardware related offset and temperature drift, phase shift due to analog low-pass or decoupling filters, and non-ideal synchronization in the subsequent host processor.

The hysteresis contribution to the delay with a 160-mV hysteresis (±80 mV) at a minimum 0.3-V_{PP} input to the comparator is around 32°, or 180 ns at a 500-kHz signal frequency.

In this consideration, the comparator's propagation needs to be added to the hysteresis. This means the lower the comparator's propagation delay, the more headroom is available to increase the hysteresis or apply other means to increase the system's noise immunity.

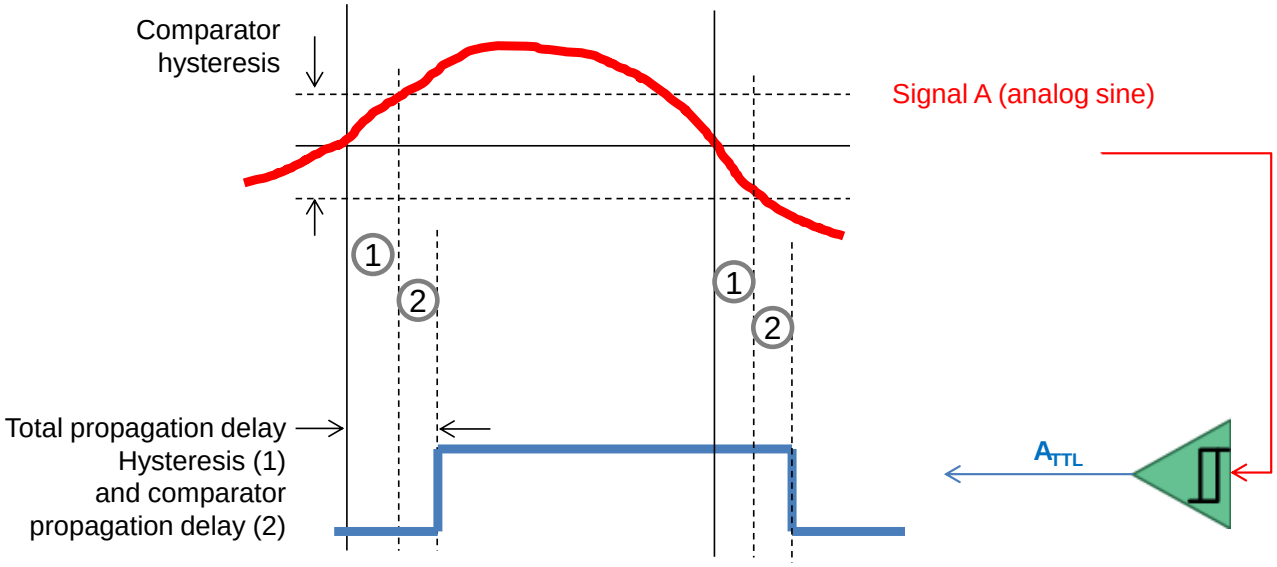

Figure 8. Signal Delay on Comparator With Hysteresis

2 Design Features

As outlined in Section 1, this TI design realizes an industrial temperature range, EMC-compliant interface to Sin/Cos incremental position encoders with differential 1-V_{PP} analog output signals A, B, and index marker R with input frequencies up to 500 kHz and a 5-V supply voltage. The major building blocks of this TI design are the dual path analog signal chain, the high-speed comparator block, the power management block, and the interfaces to the Sin/Cos encoder as well as a 60-pin interface connector, which directly fits the AM437x Industrial Development Kit.

To allow an easy evaluation of this TI design, an example application firmware is provided for the Sitara AM437x IDK. The AM437x calculates the high-resolution angle position for both signal paths using the external 16-bit ADC through SPI and outputs the angle position data with up to 28-bit resolution through the USB virtual COM port.

TIDA-00178 features overview:

- Wide input voltage range: 24 V (17 to 36 V) with reverse polarity protection provides the necessary voltages for analog signal chain as well as the 5.25 V for the Sin/Cos encoder
- Encoder interface: Sub-D15 or 10-pin header interface to 5-V Sin/Cos encoders with differential output signals A, B, and marker R from 0.3-V to 1.2-V_{PP} at 2.5-V ±1-V offset, input bandwidth up to 500 kHz
- Analog signal processing: Onboard high-speed, high-resolution dual 16-bit simultaneous sampling ADC with SPI. High-speed, low-propagation delay comparators with adjustable 170-mV hysteresis for better noise immunity to convert the analog signals A, B, and R to 3.3-V TTL signals often referred as ABZ signals
- High-resolution interpolated angle position, up to 28-bits resolution, cable length tested up to 70 m
- Developed to meet IEC61000-4-2, 4-4, and 4-5 (ESD, EFT, and Surge) as specified in the standard IEC 61800-3 EMC immunity requirements and specific test methods applicable in adjustable speed, electrical-power drive systems
- Direct plug-in compatible interface to Sitara AM437x IDK
- Example application firmware for Sitara AM437x MPU with a high-resolution dual angle position calculation at 32 kHz. User interface through USB virtual COM port for easy performance evaluation

2.1 Sin/Cos Encoder Interface

The design offers either a shielded Sub-D15 female connector compatible to HEIDENHAIN encoder test equipment or an 8-pin header connector to interface to 5-V Sin/Cos encoders with differential output signals A, B, and marker R.

Table 7. Sin/Cos Encoder Interface

PARAMETER	TYPICAL VALUE	COMMENT
Encoder supply voltage	5.25 V (±5%), 200 mA	5.25 V was chosen for an additional 0.25-V margin to compensate for voltage drop over longer cables. Adjustable to, for example, 5 V through feedback resistor change
Input signals	A+ ,A–, B+, B–, R+, R–	120-Ω differential line termination
Input level and common mode voltage range for A+, A–, B+, B–	0.3-V – 1.2 V_{PP}, 2.5 V ±1.0-V common mode	
Input level and common mode voltage range for R+, R–	0.2-V – 0.85V_{PP}, 2.5 V ±1.0-V common mode	

2.2 Host Processor Interface

The high-resolution path for signals A+, A– and B+, B– features a high-speed, high-resolution dual 16-bit simultaneous sampling ADC with a differential input and SPI output. The main features of this functional block are outlined in Table 8.

Table 8. 16-Bit High-Resolution Channel With ADC and SPI Output

PARAMETER	TYPICAL VALUE	COMMENT
Gain A, B	5.0 (0.1%)	0.1% resistors
Gain drift A, B	25 ppm/°C	0.1% resistors
Offset, A, B	< 10 LSB (at 16-bit)	Un-calibrated
Offset drift, A, B	< 0.15 LSB/°C	
Bandwidth (–3 dB)	≥ 500 kHz	
Quantization	16-bit	FSR = ±5 V (ADS8354) Drop-in compatible 14- or 12-bit versions available
Sampling frequency	Up to 700 kSPS	
Data output format A, B	16-bit 2's complementary	
Serial interface (SPI slave)	3.3 V, up to 24-Mhz SPI clock	Dual 16-bit data per SPI frame

The comparator block features high-speed, low-propagation delay comparators with an adjustable 100-mV hysteresis for better noise immunity to converts the analog signals A, B, and R to 3.3-V TTL.

Table 9. Comparators

PARAMETER	TYPICAL VALUE	COMMENT
Digital output signals A, B, and R	3.3-V TTL	
Hysteresis	~170 mV (±85mV)	For increased noise immunity, adjustable through feedback resistor change
Propagation delay	~40 ns	Low propagation delay
Maximum phase delay (propagation delay and hysteresis)	< 60°	at 0.3 V_{PP}, 500-kHz input

2.3 Evaluation Firmware

To allow for a quick evaluation of the TIDA-00178 design, an example application firmware for Sitara AM4377 MPU is provided, where the interpolated high-resolution angle is calculated for the 16-bit dual ADC ADS8354. A user interface through the USB virtual COM port at 115000 baud allows for an easy performance evaluation.

The user interface through the virtual COM port at 115000 baud supports the following features:

- Selection of Sin/Cos encoder line count: up to 32000
- Hardware synchronized sampling of the external dual sampling 16-bit ADC through SPI and the incremental counter with a synchronization delay of less than 200 ns
- High resolution angle in 32-bit, float format. Angle scaled per unit from 0 to 0.9999999, up to 28-bit interpolated angle resolution
- Automatic absolute position initialization after first occurrence of index marker R
- Menu to support display mode at 10 Hz or data dump mode at 200-Hz update rate for total angle, incremental angle and phase with both, the 16-bit dual ADC (ADS8354) on the TIDA-00178 design
- Diagnostic error message, when encoder not connected or when differential input voltage below 0.3 V_{PP}.

2.4 Power Management

The TI design features a 24-V DC input with wide input voltage range from 17 to 36 V and reverse polarity protection. The onboard power management is split into a DC/DC buck that generates an intermediate 6-V rail and three LDOs, which generate the corresponding 3.3-V, 5-V, and 5.25-V rails.

The 5.25-V encoder supply features a LDO with very low noise and an enable pin. Therefore, the Sin/Cos encoder supply voltage can be turned off through the host processor if desired.

Table 10. TIDA-00178 Voltage Rails

PARAMETER	VOLTAGE	CURRENT	COMMENT
Input	24 V (17 to 36 V)	150 mA	Wide input voltage with reverse polarity protect
Intermediate rail	6 V (±5%)	500 mA	Intermediate rail. High-efficiency (> 80%) DC/DC buck power supply
Encoder supply	5 V (±5%)	250 mA	5.25 V was chosen for an additional 0.25-V margin to compensate for voltage drop over longer cables. Adjustable to, for example, 5 V through feedback resistor change
5-V supply rail	5 V (±5%)	100 mA	High-precision signal chain supply
3.3-V supply rail	3.3 V (±5%)	100 mA	Low-precision signal chain supply

2.5 EMC Immunity

The design meets ESD, EFT, and Surge requirements per IEC61000-4-2, 4-4, and 4-5 with levels specified in the IEC 61800-3 standard "EMC immunity requirements for adjustable speed, electrical-power drive systems". The subD-15 connector to the position encoder can be accessed and shielded encoder cables are used to connect to the encoder. Since the encoder cable can exceed 30 m, ESD, EFT, and Surge apply per Table 11 for use in Environment 2.

Table 11. EMC Immunity Requirements

PORT	PHENOMENON	BASIC STANDARD	LEVEL	PERFORMANCE (ACCEPTANCE) CRITERION
Sin/Cos encoder interface connecter	ESD	IEC61000-4-2	±4-kV CD or 8-kV AD, if CD not possible	B
	Fast transient burst (EFT)	IEC61000-4-4	±2 kV/5 kHz, capacitive clamp	B
	Surge 1.2/50 µs, 8/20 µs	IEC61000-4-5	±1 kV; since shielded cable > 20 m, direct coupling to shield (2-Ω source impedance)	B

The performance (acceptance) criterion is defined as follows:

Table 12. Performance (Acceptance) Criterion

PERFORMANCE (ACCEPTANCE) CRITERION	DESCRIPTION
A	The module must continue to operate as intended with no loss of function or performance even during the test
B	Temporary degradation of performance is accepted. After the test, the module must continue to operate as intended without manual intervention.
C	During the test, loss of functions accepted, but no destruction of hardware or software. After the test, the module must continue to operate as intended automatically, after manual restart, power off, or power on.

3 System Block Diagram

The system block diagram of this design is shown in Figure 9. The major building blocks of this TI design are:

- The 16-bit high-resolution dual path and a high-speed comparator block
- The power management and the interfaces to the Sin/Cos encoder
- The Sitara AM437x IDK 60-pin expansion header or port for signal processing and high-resolution position calculation

To allow for an easy evaluation of the TIDA-00178 design, an example firmware is provided for the AM437x IDK, which outputs the angle position through the virtual COM port.

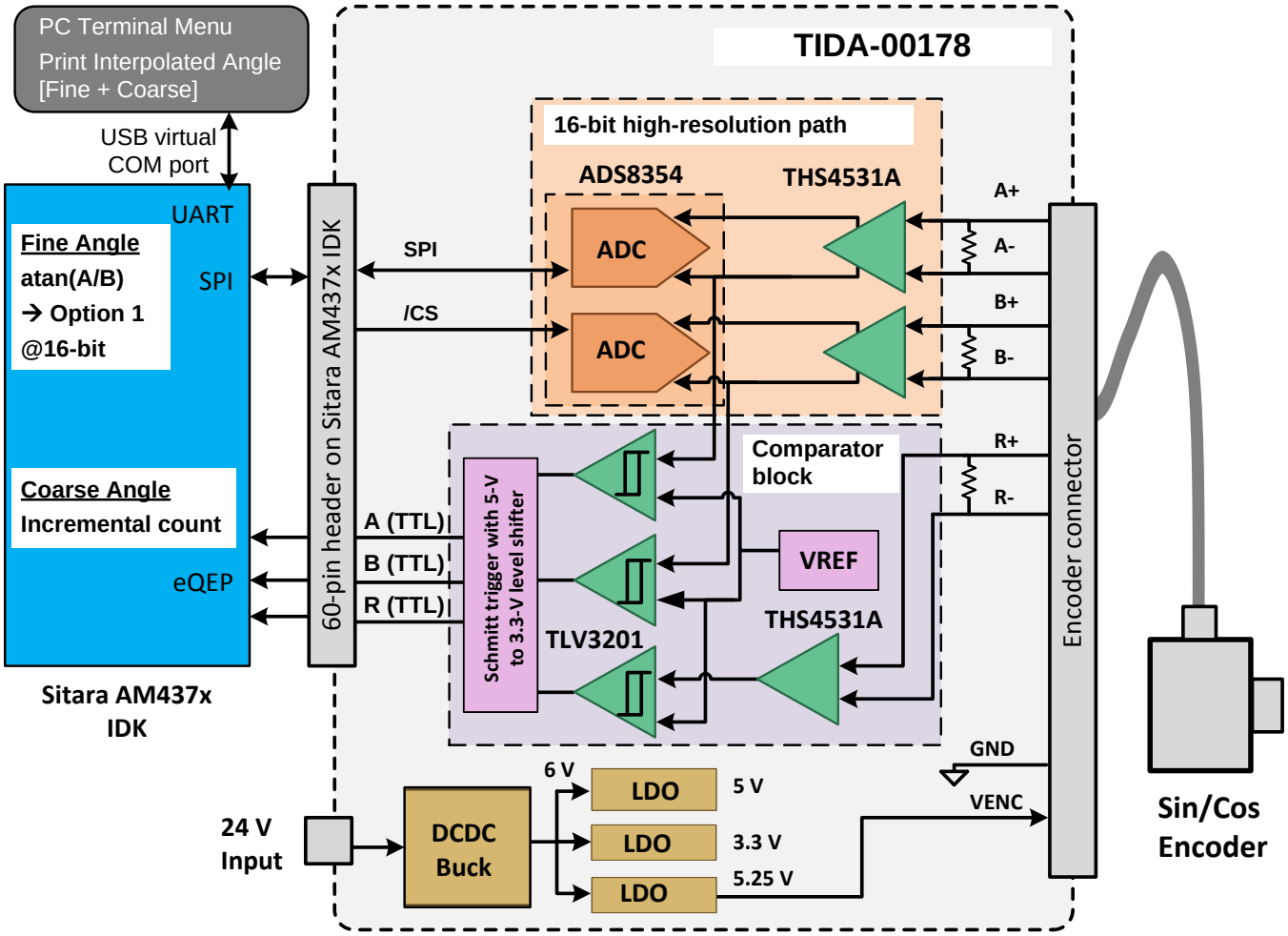

Figure 9. System Block Diagram of TIDA-00178 With Sitara Industrial Development Kit

The analog signal chain features a 120-Ω termination with EMC protection. The differential 1-V_{PP} sine and cosine input signals are amplified and level-shifted, respectively. The signal path is using an onboard external high-speed, high-resolution, dual 16-bit simultaneous sampling ADC with SPI.

The comparator block features a high-speed, low-propagation delay and adjustable hysteresis for better noise immunity and converts the analog signals A, B, and the marker R into digital signals with 3.3-V TTL-level to interface to a quadrature encoder pulse module like the QEP peripheral on the Sitara AM437x processor.

The onboard wide input range 24-V power supply provides the necessary voltages for the analog signal chain as well as the 5.25-V supply voltage for the Sin/Cos encoder.

4 Circuit Design and Component Selection

4.1 Analog Signal Chain

Figure 10 provides and overview on the analog signal chain subsystem and the comparator subsystem. The analog signal chain provides a high-resolution signal path with increased common-mode noise immunity featuring fully differential amplifiers and a fully differential dual 16-bit ADC with SPI output.

The comparator sub-system generates TTL level outputs for signals A, B, and R at a very low-propagation delay.

Each subsystem is explained in the following sections.

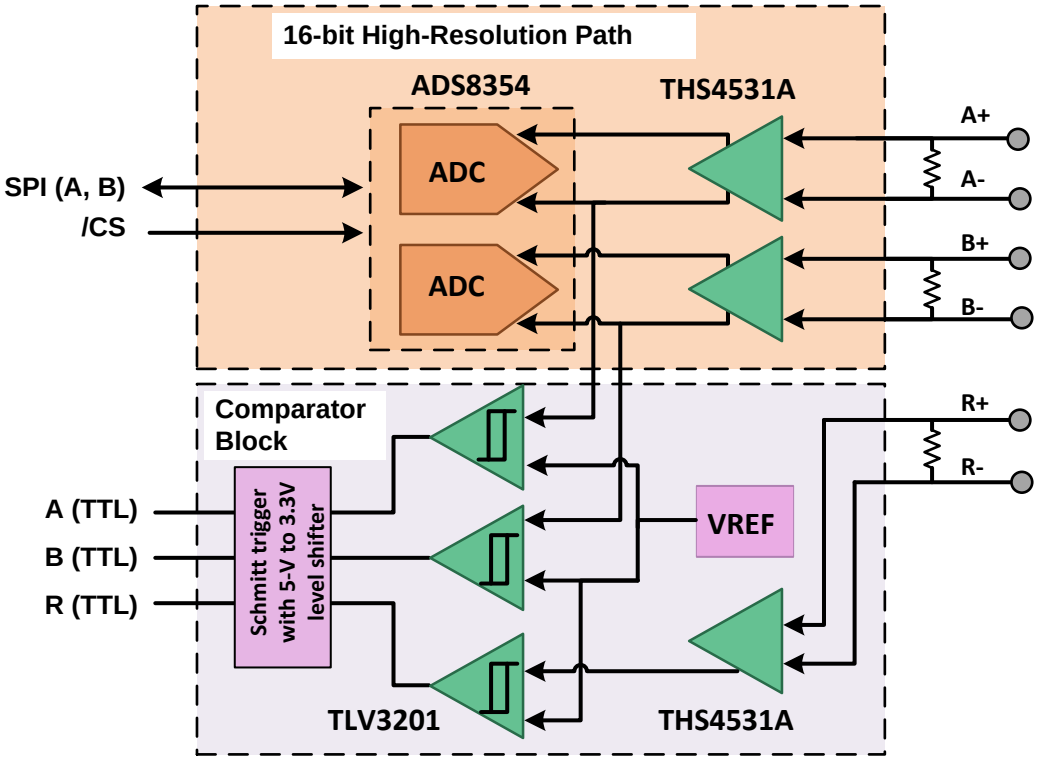

Figure 10. Analog Signal Chain

4.1.1 High-Resolution Signal Path With 16-Bit Dual Sampling ADC

4.1.1.1 Component Selection

A high-precision dual-channel ADC is required to fulfill the design requirements. The ADS8354 has been selected for the following reasons:

- The device has a high resolution (16-bit) with high precision (superb THD and SNR performance of –93-dB SNR, –100-dB THD).
- Drop-in pin-compatible 14-bit and 12-bit versions are flexible pending required resolution versus cost optimization.
- Its high speed (700 kSPS) and bandwidth support at least 500-kHz analog input signals.
- Dual channel with true differential inputs and dual and independent reference voltages improve immunity against common mode noise.
- Dual channel, simultaneous sampling of two channels ensure zero phase shift between the sin and cos input signals A and B.
- Sample point triggered by hardware (falling edge of /CS) allows the host processor to precisely synchronize the sample point with the incremental counter latch.
- Sample-and-hold circuit returns to sample mode after completing the conversion process, thus relatively long sample times settle to 16-bit accuracy.
- Dual, programmable, and buffered 2.5-V internal references provide common mode bias voltage to the amplifier to almost cancel offset and offset drift related errors.
- Serial interface to host processor (dual data) with up to 24-MHz clock frequency minimizes latency.
- The device is fully specified over the extended industrial temperature range: –40°C to 125°C.
- The device is contained in a small package.

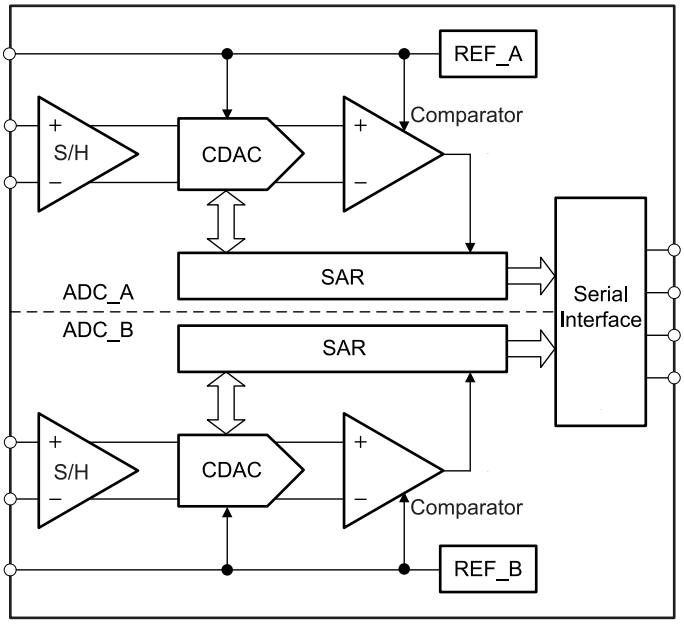

Figure 11. ADS8354 Block Diagram

To leverage the ADS8354 performance, a fully differential, high-speed amplifier with a configurable output common mode voltage, like the THS45xx family, is required.

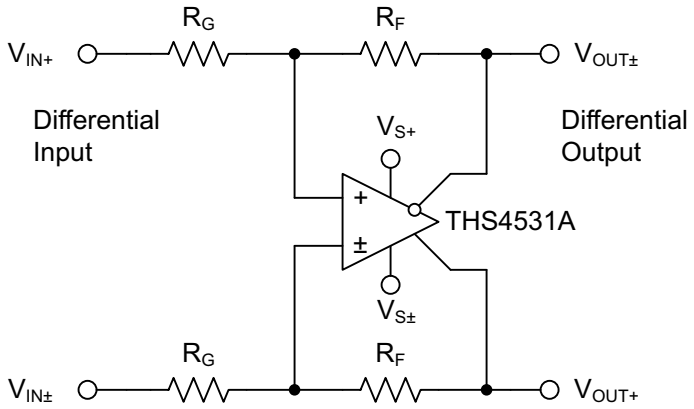

Figure 12. Differential Input to Differential Output Amplifier

The signal remains fully differential. The gain and filtering is defined by the input and feedback resistors and capacitors. The gain is set by the ration of R_F/R_G and the output common mode voltage is set by the input signal V_{OCM}. To low-pass filter the signal, a capacitor is placed parallel to the R_F resistor.

The THS4531A is a fully differential architecture and was chosen as it can drive the ADS8354 and meets the AC and DC requirements specified in Section 1.4. A single amplifier topology per package was used instead of the dual differential amplifier per package like the THS4532 for flexibility and easier PCB routing.

The key parameters of the THS4531A for use in this design are:

- Fully-differential architecture with adjustable output common mode voltage
- High gain bandwidth: 27 MHz (6 MHz at G = 5)
- Low distortions, THD –120 dBc at 1 kHz (1 V_{RMS}, R_L = 2 kΩ)
- Low input voltage noise: 10 nV/√Hz (f = 1 kHz)
- Very low offset, V_{OS}: ±100 µV
- Very low offset drift, V_{OS} Drift: ±2 µV/°C (Industrial temperature range)
- Single 5-V supply to leverage same supply than ADS8354
- Rail-to-rail output (RRO) and negative rail input (NRI) to maximize input and output signal swing

4.1.1.2 Input Signal Termination and Protection

Each of the differential input signals are terminated with 120-Ω resistors. COG capacitors are added for differential and common mode HF noise rejection. The differential low-pass filter's cut-off frequency (–3 dB) is around 6 MHz. The 10-Ω (1%) pulse-proof resistor in conjunction with diodes clamp to the 5-V rail or GND for ESD protection with input current limitation. Figure 13 shows the TIDA-00178 schematics of the input stage for the encoder's differential signals B+ (B_P) and B– (B_M).

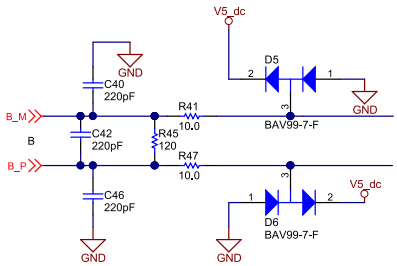

Figure 13. Termination for Analog Inputs

Look at the encoder signals B+/B– (named "B_P – B_M" in the schematic) signal conditioning block schematic from left to right to distinguish the following parts and functions:

- The HF noise suppression COG capacitors: C40, C42, and C46. For a higher common-mode rejection, an additional 220-pF COG capacitor might be placed in parallel to the 220-pF capacitor from each differential input to GND. The low-pass cut-off frequency (–3 dB) is around 6 MHz.
- The impedance matching/termination resistor 120 Ω: R45
- Current limiting resistors with pulse proof current: R41, R47
- Clamping diodes / op-amp input protections (D5 and D6) to the 5-V rail and GND

The LP filters are designed to guarantee the proper functionality and performance at the speed provided in the system specifications.

4.1.1.3 Differential Amplifier THS4531A and 16-Bit ADC ADS8354

The two primary circuits required to maximize the performance of a high-precision, successive approximation register (SAR) ADCs are the input driver and the reference driver circuits. For more information on the amplifier requirements driving the ADC input, refer to the ADS8354 datasheet, Section 9.1.

The THS4531A has been minded to work in combination with the ADS8354. The common-mode / DC-level of the input signal (2.5 V nominal) is provided to the THS4531A directly from the reference output of the ADS8354 itself to minimize potential offset and drift errors.

The differential input full scale range of the ADS8354 was configured to $\pm 2 \times V_{REF}$. With the reference voltage of V_{REF} = 2.5 V, this yields a full-scale range (FSR) of ±5 V. The maximum Sin/Cos encoder's differential input voltage is 1.2 V_{PP}. A voltage higher than 1.35 V_{PP} should still be detected as a failure. A safety margin of 50% is added to the maximum peak-to-peak voltage, which is then 1.8 V_{PP}. To match the ADC full-scale input range, the gain of the THS4531A should be 5.5. However, to remain in the linear output voltage range of the THS4531A at a 5-V supply, which is at least 0.25 to 4.8 V, the gain should be reduced by around 10%; therefore, the ideal differential amplifier gain would be 5.

To ensure minimum gain error and especially drift between the channels, high-precision, resistors with a 0.1% accuracy are required. To minimize noise, the feedback resistors should be chosen in the lower kΩ range (see Section 1.4).

Due to the gain of 5, a typical 1-V_{PP} input signal leverages around 50% of the ADC FSR, which results in a loss of 1-bit of precision, thus yielding an equivalent 15-bit resolution. The lower input voltage of 0.6 V_{PP} will leverage around 25% of the FSR, which equals typically a 14-bit resolution.

Figure 14 shows the schematics of the high-resolution analog signal path. The 0.1% gain setting resistors are R40, R39, and R50, R52 for channel B and R56, R55 and R62, R64 for channel A are chosen rather low impedance with 1k and 5k to minimize current noise. A feedback capacitor each, C37, C47 and C49, C57 is added for HF noise filtering with a 3-dB cut-off frequency of 9 MHz.

The series 10-Ω resistors R44, R51 and the two parallel capacitors C43 and C44 (R59, R63, C53, and C54 for ADS8354 channel B) form the anti-aliasing filter. The filter capacitor C43 and C44 (C53 and C54), connected across the ADC inputs, filters the noise from the front-end drive circuitry, reduces the sampling charge injection, and provides a charge bucket to quickly charge the internal sample-and-hold capacitors during the acquisition process. As a rule of thumb, the value of this capacitor should be at least 10 times the specified value of the ADC sampling capacitance. For these devices, the input sampling capacitance is equal to 40 pF. The capacitor should be a COG- or NPO-type because these capacitor types have a high-Q, low-temperature coefficient, and stable electrical characteristics under varying voltages, frequency, and time.

Additional 3-Ω series damping resistors R42 and R46 (R53, R54) are placed between the charging capacitor and the ADC's switched capacitor. This helps reduce and eliminate potential ringing when the ADC input is transitioning from the hold to the sample state.

To minimize the impact of an offset drift of the ADC reference REFIO_A and REFIO_B, the ADC references are used to bias the common mode output voltage of the THS4531A. To buffer and decouple the V_{OCM} signal at the THS4531A, small RC filters R48/C45 and R61/C56 are added close to each pin.

The ADS8354 reference voltages REFIO_A and REFIO_B are decoupled with 10-µF capacitors C62 and C63, respectively, and a 0.22-Ω resistor (R66, R67) is added in series to avoid high-frequency oscillations.

To optimize the layout for cross-talk with a minimum use of vias for the critical signals A+, A– and B+, B–, the following connections have been made:

1. The differential input signal A (A+, A–) has been fed into the ADS8354 input channel B.
2. The differential input signal B (B+, B–) has been fed into the ADS8354 input channel A.

This results in the following hardware relationship. The ADS8354 channel B equals the Sin/Cos encoder signal A. The ADS8354 channel A equals the Sin/Cos encoder signal B.

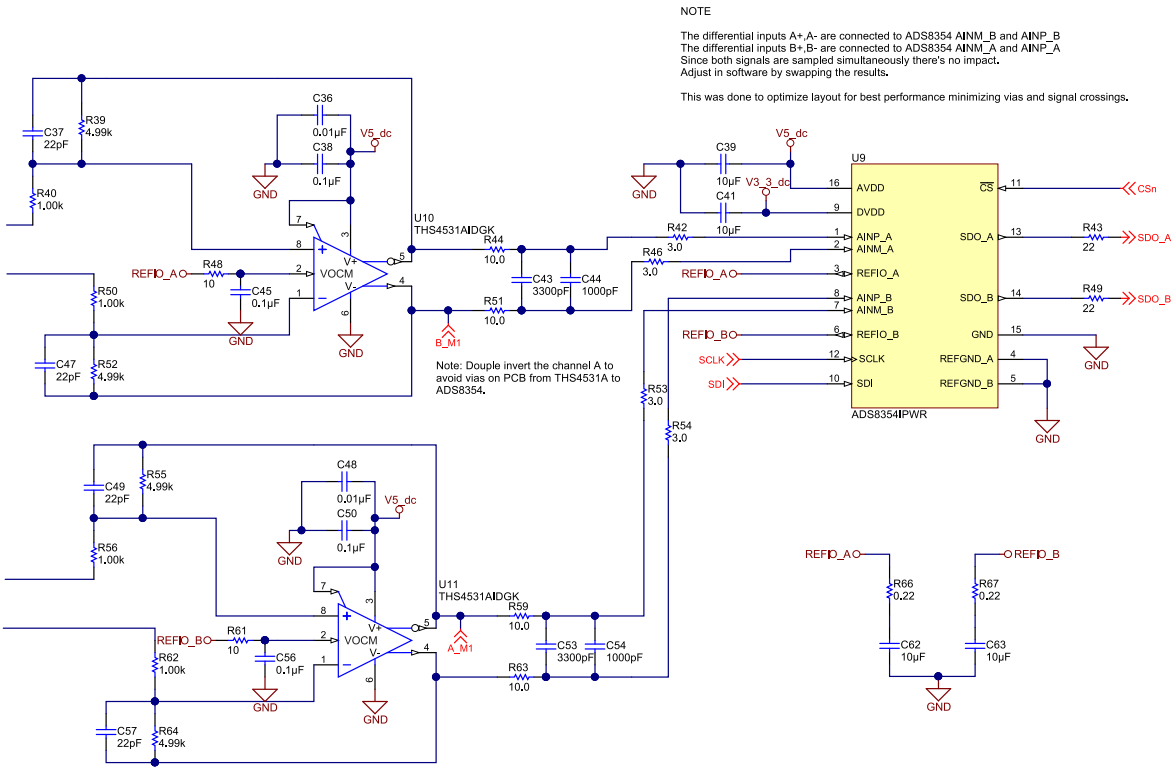

Figure 14. Sin and Cos Signal Chain With Dual THS4531A and ADS8354

NOTE: Channels are swapped for optimum performance layout and minimize the numbers of vias.

The configuration of the ADS8354 registers through the serial interface is explained in Section 4.3.

4.1.2 Comparator Subsystem for Digital Signals A, B, and R

The comparators are required to detect the zero-crossing of the analog signals A and B, as well as the zero index pulse with the marker R and generate the corresponding digital 3.3-V TTL-compatible signals A_{TTL}, B_{TTL}, and R_{TTL}, often referred to as ABZ. As outlined in Section 1.4, a low propagation delay comparator offers additional margin to the system.

The comparators selected are the TLV3201 (single) and TLV3202 (dual), 40 ns, microPOWER, push-pull output comparators with the following main characteristics:

- Low propagation delay of typical 40 ns
- Low input offset voltage of typical 1 mV, to ensure minimum drift of switching threshold
- Push-pull outputs, to drive the input of a I/O host processor
- Industrial temperature range

The TLC372 dual comparator with a 250-ns propagation delay is a lower cost option, depending on the overall system propagation delay and maximum frequency. The advantage of the TLV320x family is that it allows other components to add more delay while still keeping the required 500-ns maximum delay at 500 kHz. For example, a larger hysteresis would increase the propagation delay while improve immunity against noise.

4.1.2.1 Comparator With Hysteresis and Level Shifter

The TLV370x is configured as inverting the comparator to detect the zero-crossing of the analog sin and cosine signals A and B as well as the index pulse R. Figure 15 shows the corresponding schematics for the signal A.

To compensate for the inverted configuration, the negative differential output of the THS4531A was an input to the comparator.

The switching threshold is set by the reference voltage V_{REF} = 2.5 V (REF2025). For each comparator, the reference input is taken from the REF2025 and decoupled with a 10-ohm series resistor and a 100-nF capacitor.

A hysteresis is added for better noise immunity. The hysteresis (V_{TH+} – $V_{TH–}$) of a non-inverting comparator can be calculated per Equation 7:

$$V_{Hystereis} = \left(V_{Out\_High} - V_{Oout\_low}\right) \times \frac{R_G}{R_F} \tag{7}$$

with V_{Out_High} the high-level and V_{Out_Low} the low level comparator output voltage, R_F the feedback and R_G the input resistor into the non-inverting comparator input.

For the configuration of this design as outlined in Figure 15, the hysteresis has been set to around 174 mV per Equation 8. Because R19 are magnitudes lower than R22, it can be neglected.

$$V_{Hystereis} = 5\ V \times \frac{R_{22}}{R_{23}} \approx 174\ mV \tag{8}$$

The upper and lower switching thresholds V_{TH+} and $V_{TH–}$ are defined per Equation 9 and Equation 10 with the reference voltage V_{REF} = 2.5 V.

$$V_{TH+} = 2.5\ V \times \left(1 + \frac{R_{22}}{R_{23}}\right) = 2.58\ V \tag{9}$$

$$V_{TH–} = \left(5\ V - 2.5\ V\right) \times \left(1 - \frac{R_{22}}{R_{23}}\right) = 2.41\ V \tag{10}$$

CAUTION

The lower threshold is a function of the supply voltage. However, the supply voltage tolerance of this design 5%, as typical with most designs. A ±5% tolerance with the 5-V supply voltage would affect the lower threshold by only by ±17 mV, resulting V_{TH-} range from approximately 2.39 to 2.43 V, and thus still acceptable.

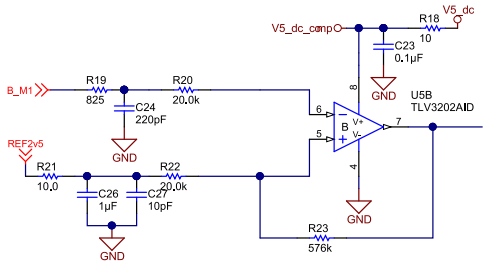

Figure 15. Signal B Comparator With Hysteresis

The 5-V supply of each comparator is decoupled with a 1-Ω series resistor and 100-nF capacitor to minimize switching noise from the comparator to the 5-V rail. The RC low pass comprised of R19 and C24 is added to compensate some of the phase delay of the anti-aliasing filter and ensure minimum phase shift between the analog signal into the ADC and the TTL signal at the comparator's output. R19 has been chosen high enough to minimize unbalanced load of the THS4531A differential outputs to ensure it does not impact the performance of the 16-bit analog path.

The hysteresis allows for a clean digital signal, which avoids fast switching due to noise around the zero crossing point. The hysteresis, however, introduces an additional propagation delay, which depends on the analog signal amplitude $V_{IN\_PEAK-PEAK}$ at the comparator input.

$$\phi_{Hysteresis} \sim \sin^{-1}\left(\pm\frac{173\ mV}{V_{IN\_PEAK-PEAK}}\right) \tag{11}$$

Assuming a minimum input voltage of 0.3 V_{PP} at the differential amplifier:, the output of the differential- to single-ended amplifier (gain = 5) will have an amplitude of 0.75 V_{PP} at the comparator (from 0 to 100 kHz) and around 0.54 V_{PP} at 500 kHz due to the signal chain attenuation of approximately –2.7 dB. The hysteresis' phase delay of the digital signals A, B, and R will be around 19 degrees for a 0.54-V_{PP} input at the comparator. At 500 kHz, this would translate into a propagation delay of around 106 ns. This is the worst case scenario.

To level shift the signals down to a 3.3-V I/O for the host processor, a Schmitt trigger SN74LVC3G17 was used. This Schmitt trigger has three inputs and outputs that fit the A, B, and R signals. Using a 3.3-V supply, the maximum propagation delay of the Schmitt trigger is 5.4 ns, assuming an input signal slew rate of less than 1 ns. Therefore, hysteresis of the Schmitt trigger can be neglected and only the propagation delay is considered. The propagation delay of the TLV3201 is 40 ns.

Using a 500-kHz signal on the comparator block, this delay would translate into an overall delay of around 151 ns or below 27°.

The comparators for the signals B and R have the same settings. Also, the buffering and gain stage for the index marker R is identical to the signals A and B. This is to ensure the phase of the index marker R is exactly in phase with the signal A and B up to a 500-kHz signal frequency. This ensures the zero index marker R will occur as specified, slightly before the rising edge of signals A and B. The index marker R defines the absolute zero position; therefore, the exact relation to signals A and B is required to avoid any position offset.

4.2 Power Management

The power management consists DC/DC buck to generate a 6-V intermediate rail from the 24-V input voltage. The encoder supply voltage and the 5-V and 3.3-V rails are derived from the intermediate voltage, as shown in Figure 16.

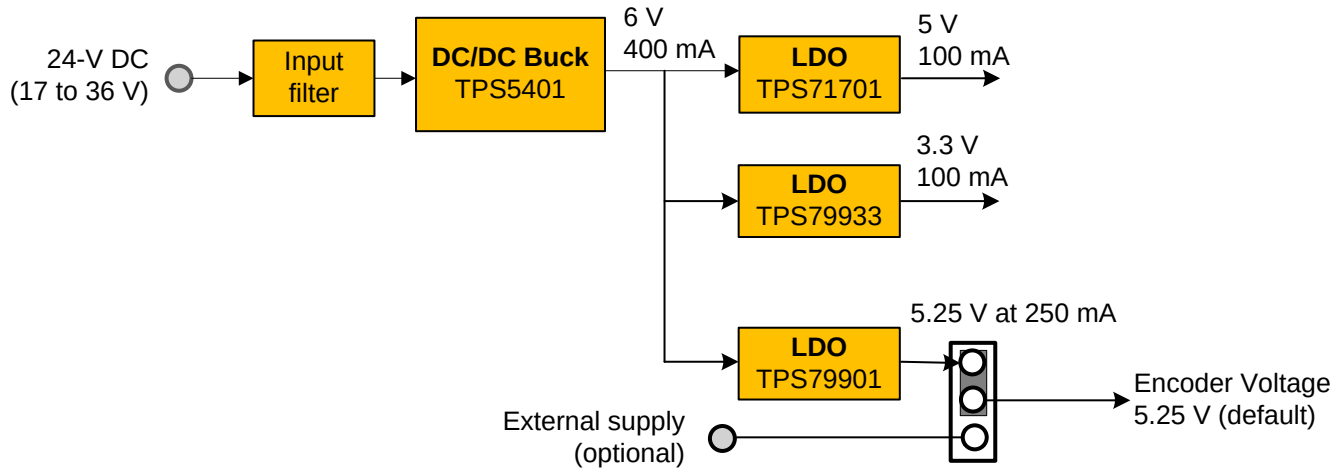

Figure 16. Power Management Solution

Because of the high performance required by the system or solution, most of the power rails are provided by low-noise LDOs. The drawback is the limited efficiency and low output current capability. The maximum output current is limited by the thermal performance, due to the high power losses.

To reduce the voltage drop across the LDO a high-efficiency DC/DC switching converter to generate a 6-V intermediate rail from the 24-V input is us. Minimize the noise introduced by the switcher solution by proper layout and component selection.

4.2.1 24-V Input to 6-V Intermediate Rail

A DC-DC switching converter is provided to achieve the intermediate voltage rail of 6 V that supplied the three LDOs. This is a mandatory choice because the high VIN / VOUT ratio makes any LDO unsuitable for the power conversion. The efficiency of any LDO could be simply calculated as VOUT / VIN that, in the worst case (maximum VIN), would lead to 5.25 V / 36 V ≈ 14%. The remaining 86% of the power consumption is dissipated by the LDO package: having indeed a maximum current of 200 mA would lead to 36 V × 200 mA × 86% = 6.2 W power dissipated on the LDO package that would simply and quickly blow up any reasonable package.

Starting with the input filter, conducted EMI is generated by the normal operation of switching circuits. Large discontinuous currents are generated by the power switches turn on and off very fast. In a buck topology, large discontinuous currents (high di/dt) are present at the input of the converter. The selected values for the input filter are shown in Figure 17.

For more details about how to design an input EMI filter, see SNVA489.

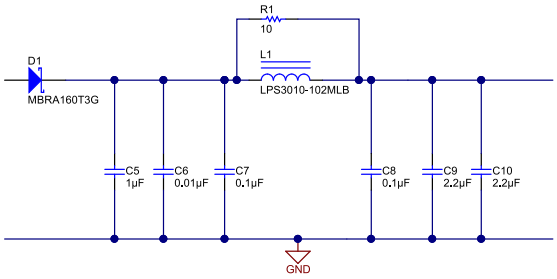

Figure 17. Input Filter Including Reverse Polarity Protection

The DC/DC buck converter has been designed to meet the following specifications:

- Input voltage: V_{IN} = 17 to 36 V, 24-V nominal
- Output voltage: 6 V at 500 mA
- Switching frequency: 500-kHz nominal
- Output voltage ripple: max 25 mV_{PP}
- Efficiency: > 80% at full load
- Non-isolated topology

The TPS5401 is selected because this is a buck converter with an integrated FET, 3.5- to 42-V input voltage and 0.8- to 39-V output voltage at a 500-mA output current. Its frequency can be adjusted from 100 kHz to 2.5 MHz or can be synchronized with an external clock. It can also be enabled and disabled. These features make the TPS5401 a very good fit to the specifications previously listed.

Note that the TPS5401 is pin-to-pin compatible with the TPS54040A, which is a higher cost version of the TPS5401 with similar performance but more accurate output voltage and enable threshold.

The TPS5401 is also pin-to-pin compatible with the TPS54140A, TPS54240, TPS54340, and TPS54540. This widens the part selection and offers the possibility to modulate costs or power level (in case of future system upgrades).

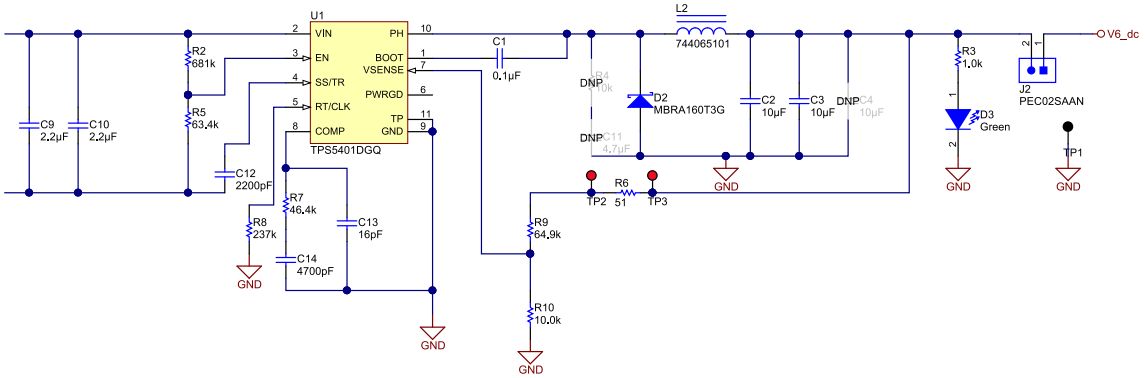

Figure 18. Schematic of 24-V to 6-V DC-DC Buck Converter With TPS5401

For a detailed explanation of the design process, refer to the TPS5401 datasheet and the TI Design TIDA-00180.

On a typical application, the output voltage is set thanks to a simple resistor divider network. Equation 12 gives the value of the upper resistor according to the output voltage, the reference voltage (0.8 V for the TPS5401), and the lower resistor (with R10 usually fixed to 10 kΩ).

$$R_7 = R_{10} \times \frac{V_{OUT} - 0.8\ V}{0.8\ V} \quad (12)$$

With V_{OUT} = 6 V and R10 = 10 kΩ, R7 yields 65 kΩ.

The tolerance of the 6-V output voltage will be 6 V±7%. This assumes feedback resistors with a 1% tolerance and the internal bandgap tolerance from the TPS5401 of ±3.5%.

The switching frequency is set with R8 = 237 kΩ to 500 kHz.

On the TPS5401 schematics, some components are marked as do not populate (DNP). This is the case of the snubber network formed by R4 and C11. The snubber network is not needed with the TPS5401.

4.2.2 Encoder Supply

A 5.25-V supply for the encoder has been selected to meet a typical 5-V (±5%) encoder supply specification and have a 0.25-V additional margin to compensate for voltage drop across longer cables used to connect the encoder.

The LDO that provides the 5.25 V to the encoder has to provide also an enable pin. In this way, it is possible to power-cycle the turn-off or power-cycle the encoder supply from a host processor if desired to, for example, turn-off the voltage at the encoder connector in case no encoder is connected.

The LDOs do not need a specific description, except for the allowed range of output capacitor or ESR for stability purpose; the main design involves the SMPS, as this affects all the main performances (noise, EMI, efficiency, cost, and board space).

The TPS79901 has been designed to provide a little higher voltage than the nominal 5 V (5.25 V), using part of the greater accuracy of the LDO to reduce the thermal stress on it. 5.25 V ±2% is within the allowed supply range of the encoder (5 V ±5%). In this way, the power it has to dissipate is

$$P_{LDO\_MAX} = \left(V_{LDO\_IN} - V_{LDO\_OUT}\right) \times i_{LDO\_MAX} = \left(6\ V - 5.25\ V\right) \times 250\ mA = 187\ mW \quad (13)$$

With a 5-V encoder voltage, the maximum power dissipation would increase to 250 mW.

With a R_{thja} ≈ 180°C/W, the TPS79901 junction temperature will increase less than 34°C versus the ambient temperature when working at maximum load current of 250 mA. For example, at an ambient temperature of 85°C, the junction will be 120°C.

The output voltage of the TPS79901 LDO is set with 1% feedback resistors R11 and R13 according to Equation 14, where 1.193 V is the nominal value of the TPS79901 reference voltage:

$$V_{ENC\_VCC} = 1.193\ V \times \left(1 + \frac{R_{11}}{R_{13}}\right) = 1.193 \times \left(1 + \frac{340\ k}{100\ k}\right) = 5.25\ V \quad (14)$$

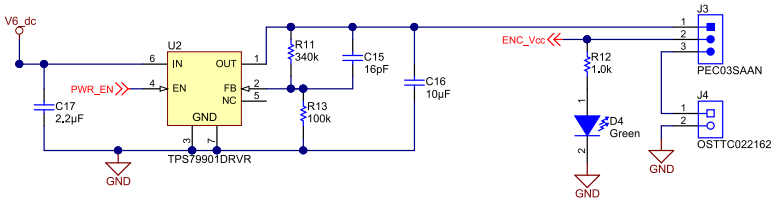

Figure 19. Schematic of 5.25-V LDO for Encoder Supply

A jumper selects between the 5.25-V LDO output and an optional external supply if desired. The signal PWR_EN is a default pullup, but it can be asserted to low from the Sitara AM437x host processor to disable or power cycle the encoder supply voltage (see Section 4.3).

4.2.3 Signal Chain Power Supply 5 V and 3.3 V

Because of the low current demanded by the analog signal chain as described in Section 4.1, and in order to achieve a high performance with very low noise, the LDO is again a mandatory choice. Because of the high PSRR featured by TI LDOs, the AC noise generated by the switcher is blocked and does not affect the noise sensitive analog parts like the ADCs and the input buffers and amplifiers.

The 5-V rail is dedicated to the analog buffers and amplifiers as well as to the analog supply voltage of the ADS8354 ADC. The 3.3 V is dedicated to the digital supply of the ADS8354 and the comparators to ensure a 3.3-V interface to the host processor without the need for I/O level shifters. Because of the low power consumption of the selected components, an LDO each was selected for the 3.3-V and 5-V rails with a nominal output current of 100 mA. A fixed 3.3-V LDO TPS79933 was used for the 3.3-V rail; the TPS71701 was used for the 5-V rail. The schematic is shown in Figure 20.

The 5-V output voltage is set by the feedback resistors R15 and R16 with the TPS71701 V_{REF} = 0.8 V, according to Equation 15.

$$V_{5V} = V_{REF} \cdot \left(1 + \frac{R_{15}}{R_{16}}\right) = 0.8\ V \cdot \left(1 + \frac{845\ k}{160\ k}\right) = 5.02\ V \tag{15}$$

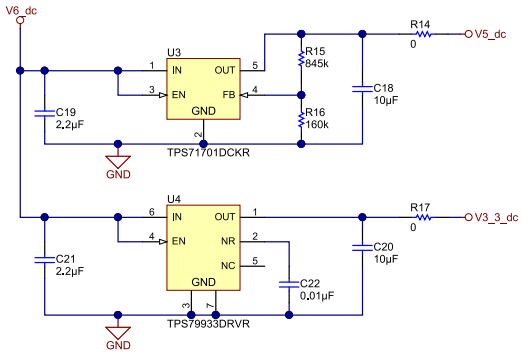

Figure 20. Schematic for 5-V and 3.3-V Point-of-Load for Signal Chain

4.3 Interface to Sitara AM437x

4.3.1 Signal Description

A 60-pin header interface is available to directly connect to the Sitara AM437x IDK. The header provides the necessary signals to calculate the high-resolution interpolated angle using the ADS8354 dual 16-bit ADC and the comparator's incremental output signals ABZ.

The interface is compliant to 3.3-V I/O systems. To have a solid GND connection, all odd pins are assigned to GND. The signals available are listed in Table 13.

Table 13. TIDA-00178 Interface Connector to Host MCU

FUNCTION	SIGNALS	I/O (3.3 V)	COMMENT
16-bit high-resolution output channel for A, B with ADS8354 and SPI (slave)	SDI (I)	Digital input	Data input for serial communication. Used for configuration of dual sampling mode
	/CS (I)	Digital input	Chip-select signal; active low. Falling edge of /CS latches the analog input (Hold) and initiates a new conversion. Use falling edge of /CS to latch QEP counter on host processor synchronously, like on Piccolo MCU
	SCLK (I)	Digital input, up to 24 MHz	Clock for serial communication
	SDO_A (O)	Digital output	Data output for serial communication, channel A and channel B. 16-bit 2's complementary data on each channel A and channel B. Input to output signal gain = 5.
Digital quadrature encoded signals A, B and index marker R	A_{TTL} (O)	Digital output	160-mV hysteresis for A, B, and R, configurable
	B_{TTL} (O)	Digital output	
	R_{TTL} (O)	Digital output	

For details on the connector pin assignment, refer to Section 6.

CAUTION

In order to synchronize the analog input sample of the ADS8354 16-bit dual sampling ADC with a QEP incremental counter module, use the /CS signal to the ADS8354 to latch the QEP counter. For an MPU like Sitara, the /CS needs to be connected to the eQEP Strobe input pin EPEPxS, where x is the module number. The Sitara AM437x eQEPx module can be configured to latch the QEP counter on a falling edge of the EQEPxS pin.

4.3.2 High-Resolution Path Using 16-bit Dual ADC ADS8354 With Serial Output

This section outlines the configuration of the ADS8354 through the serial interface. This is split into programming the full-scale input voltage range with the internal ADS8354 reference as well as the serial data transfer.

4.3.2.1 ADS8354 Input Full Scale Range Output Data Format

For this design, the ADS8354 is intended to be configured for a ±2 × V_{REF} input range. The internal reference voltage V_{REF} should be set to 2.5 V to yield ±5-V FSR.

Table 14. ADS8354 Transfer Characteristic for TIDA-00178

INPUT VOLTAGE: AINP_x – AINM_x	MODE	INPUT VOLTAGE	OUTPUT CODE (HEX)
< –5 V	±2 × V_{REF} range	NFSC	8000
–5 V + 1 LSB		FSR	8001
–1 LSB		–1 LSB	FFFF
0		0	0000
5 V – 1 LSB		PFSR – 1 LSB	7FFF

The output date format for each channel A and B is 16-bit signed integer output (2's complementary).

4.3.2.2 ADS8354 Serial Interface

The ADS8354 uses the serial clock (SCLK) to synchronize data transfers in and out of the device. The /CS signal defines one conversion and serial transfer frame. A frame starts with a /CS falling edge and ends with a /CS rising edge. Between the start and end of the frame, a minimum of N SCLK falling edges must be provided to validate the read or write operation. As shown in Table 15, N depends upon the interface mode used to read the conversion result. When N SCLK falling edges are provided, the write operation attempted in the frame is validated, and the internal user-programmable registers are updated on the subsequent /CS rising edge. This /CS rising edge also ends the frame. If /CS is brought high before providing N SCLK falling edges, the write operation attempted in the frame is not valid.

Table 15. ADS8354 SCLK Falling Edges for Valid Write Operation

INTERFACE MODE	MINIMUM SCLK FALLING EDGES REQUIRED TO VALIDATE WRITE OPERATION N
32-CLK, dual-SDO mode (default)	32
32-CLK, single-SDO mode	48
16-CLK, dual-SDO mode	16
16-CLK, single SDO mode	32

The example firmware on the F28069M Piccolo MCU initializes the ADS8354 in the 32-CLK, single SDO mode.

For more details on the serial interface mode, read and write operation, refer to the ADSxx54 datasheet.

4.3.2.3 ADS8354 Conversion Data Read

As outlined in Table 15, the device provides four different interface modes to the user. These are applicable for reading the conversion result as well. These modes offer flexible hardware connections and firmware programming. In the 32-CLK interface modes, the device uses an internal clock to convert the sampled analog signal. The conversion is completed during the first 16 periods of SCLK, and the conversion result can be read on the subsequent SCLK falling edges. All devices in the family (that is, ADS8354, ADS7854, and ADS7254) support the 32-CLK interface modes. In addition to the 32-CLK interface modes, the ADS7854 and ADS7254 also support the 16-CLK interface modes. By using the 16-CLK interface modes, the same throughput can be achieved at much lower SCLK speeds.

The example firmware on the Sitara AM437x IDK initializes the ADS8354 in the 32-CLK, single SDO mode.

The 32-CLK, single-SDO mode provides the option of using only one SDO pin (SDO_A) to read conversion results from both ADCs (ADC_A and ADC_B). SDO_B remains in 3-state and can be treated as a no connect (NC) pin. Figure 21 shows a detailed timing diagram for this mode.

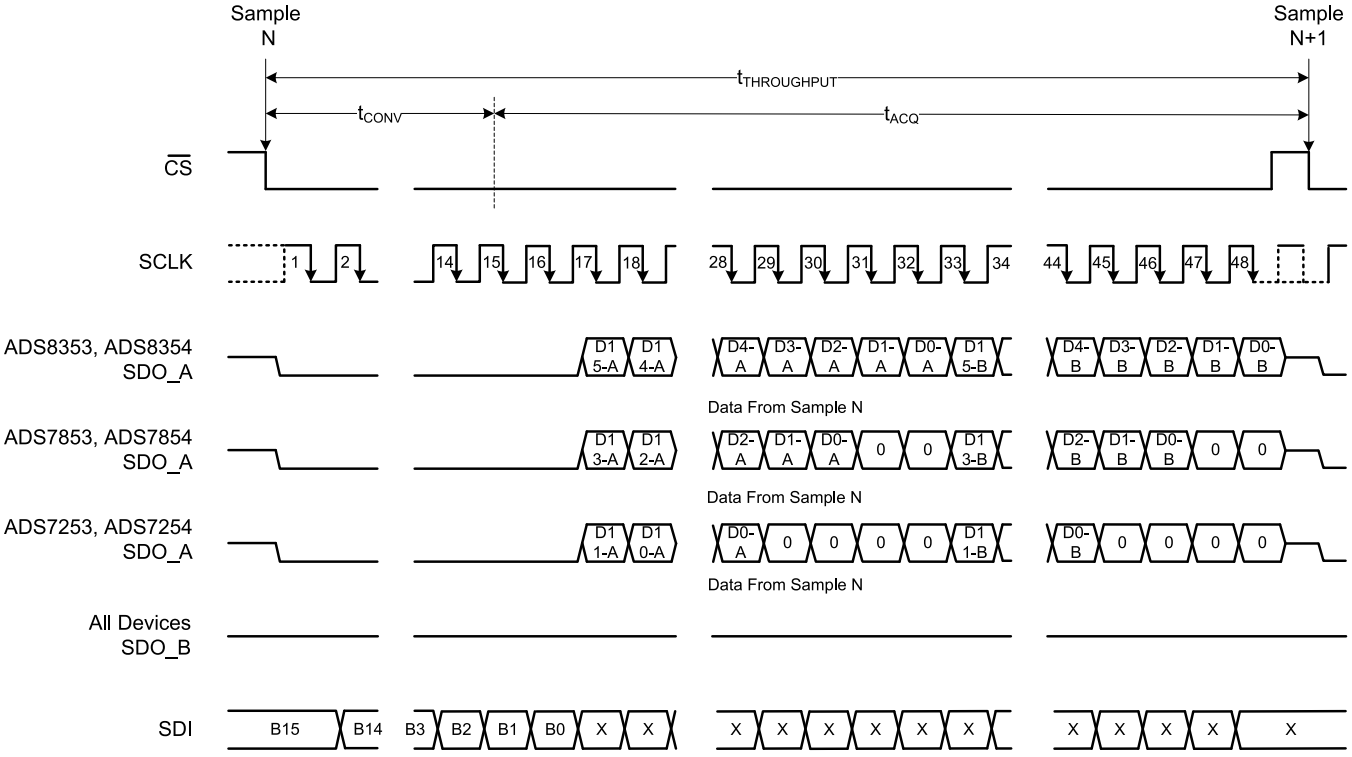

Figure 21. 32-CLK, Single-SDO Mode Timing Diagram

A /CS falling edge brings the serial data bus out of 3-state and also outputs a 0 on the SDO_A pin. The device converts the sampled analog input during the conversion time (tCONV). SDO_A reads 0 during this period. After completing the conversion process, the sample-and-hold circuit goes back into sample mode. The device outputs the MSB of ADC_A on the SDO_A pin on the 16th SCLK falling edge. The subsequent SCLK falling edges are used to shift out the conversion result of ADC_A followed by the conversion result of ADC_B on the SDO_A pin. In this mode, at least 48 SCLK falling edges must be given to validate the read or write frame. A /CS rising edge ends the frame and puts the serial bus into 3-state.

Refer to the ADSxx54 datasheet for more details.

4.3.2.4 ADS8354 Register Configuration

To select the modes as outlined in the previous sections, the ADS8354 registers REFDAC_A, REFDAC_B, and CFR are programmed as follows.

REFDAC_X and CFR are 16-bit registers and are programmed as shown in Table 16, with the upper 4 bits selecting write/read mode and corresponding register.

Table 16. ADS8354 Register Configuration

REGISTER	DATA (HEX)	COMMENT
REFDAC_A	9FF8	Write mode to REFDAC_A, selects VREF_A = 2.5 V
REFDAC_B	AFF8	Write mode to REFDAC_B, selects VREF_B = 2.5 V
CFR	8640	Write mode to CFR, selects 32-CLK dual SDO mode with A and B on SDO_A, FSR = ±2 × V_{REF}, select internal V_{REF}

Refer to the ADSxx54 data sheet for more details.

4.4 Encoder Connector

Two connector options are available for interface to Sin/Cos encoders. The default connector is a shielded SubD-15 female connector. The other option is a 10-pin header. For details on the connector assignment, refer to Section 6.

4.5 Design Upgrades

Ensure the 5.25-V LDO Output Enable pin is not floating through signal PWR_EN: Although a connector J-7, pin 4 is available to ensure the input to the LDO is always terminated with either pulled-up (Jumper J7:4-6) or pulled-down (Jumper: J7 4-3), an additional pull-up of 10k from U2, pin 4 to 3.3 V (V3_3_dc) is recommended.

5 Software Design

5.1 Overview

To allow for easy evaluation of the TIDA-00178 hardware reference design with the Sitara AM437x, an example firmware is provided for the AM437x IDK, which allows for evaluating TIDA-00178 with Sin/Cos incremental position encoders. A user menu through USB virtual COM port is provided to initialize the line count of selected Sin/Cos encoder and print the calculated high-resolution angle information along with other user-selectable data.

The main peripherals leveraged on the Sitara are the McSPI peripheral to read the dual high-resolution 16-bit data signals $A_{16\text{-bit}}$ and $B_{16\text{-bit}}$. The quadrature encoder pulse (eQEP2) module is used for directional up-down incremental count based on the signals A_{TTL} and B_{TTL} and the zero index marker R_{TTL} for absolute position initialization. The DMtimer7 timer is used to generate periodic interrupts to trigger a new angle measurement. A 32-kHz period was chosen. The UART peripheral was used to implement the user interface at 115000 baud through a virtual COM port.

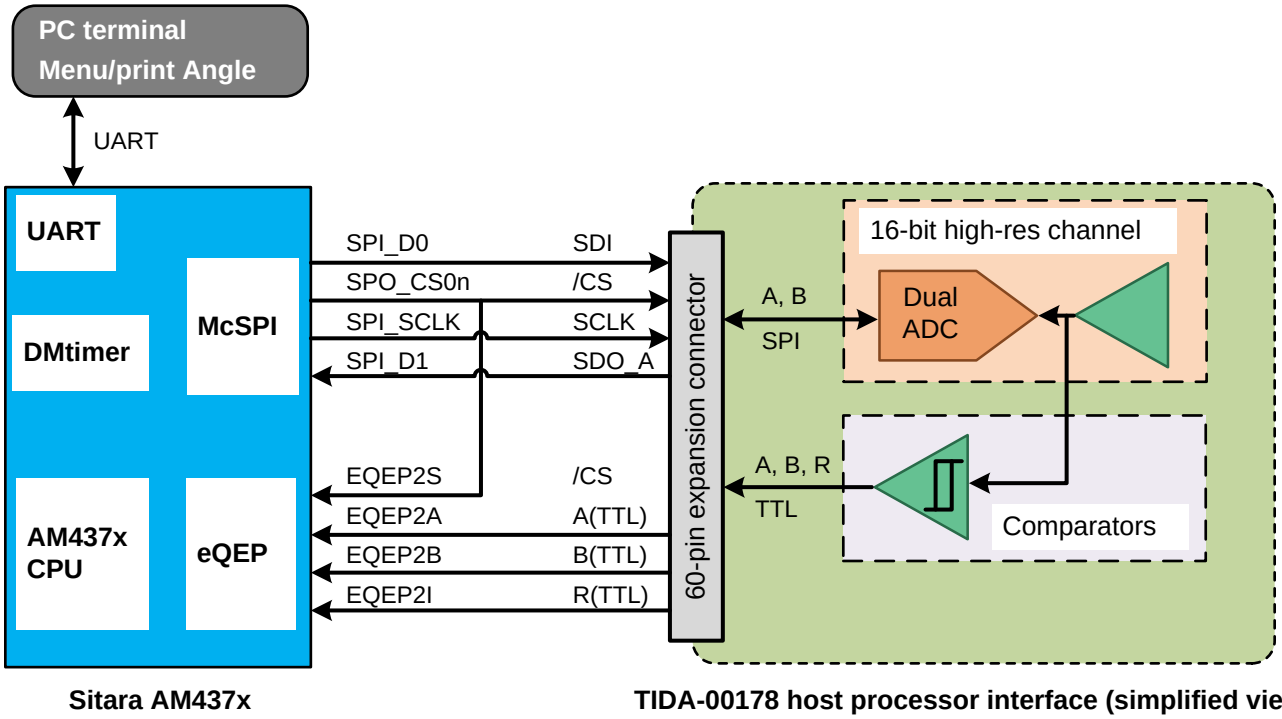

Figure 22. Sitara AM437x Peripheral Module and Pin Assignment to TIDA-00178 Host Processor Interface

5.2 Sitara AM437x Firmware

The example firmware is developed and compiled for the Sitara AM437x and leverages the peripheral modules outlined in Figure 23.

The firmware leverages am437x_sysbios_ind_sdk. The firmware basically consists of three functional blocks.

The Sitara framework, as outlined in Figure 23, the algorithm to synchronously sample the required data and calculate the interpolated angle as well as the UART terminal-based user interface.

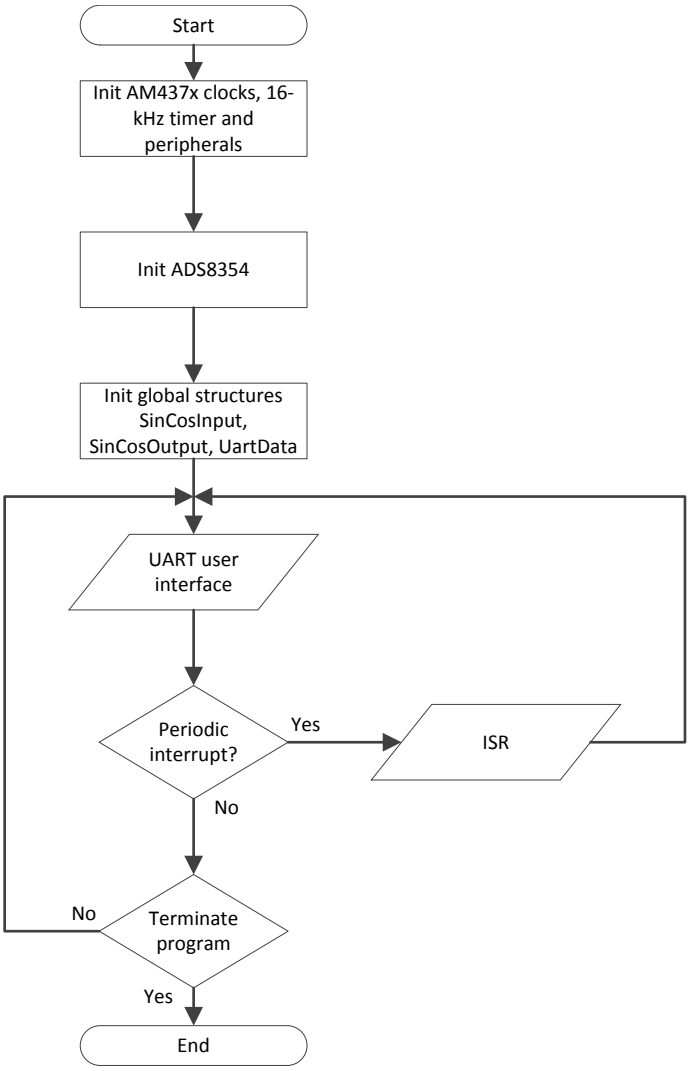

Figure 23. Flowchart of Sin/Cos Encoder Framework

The AM437x framework initializes the AM437x CPU clock to 600-MHz, the GPIO multiplexers, the peripherals like McSPI, UART, and the DmTimer based periodic timer and interrupt. It also configures the external 16-bit dual ADC ADS8354 through McSPI as outlined in Section 4.3.2.4. The McSPI is configured as an SPI master with the serial clock of 24 MHz. This is the maximum SPI clock for the ADS8354 converter.

After initialization, the program invokes the UART-based user interface and serves the period interrupt service routine interrupt service routine (ISR). The period ISR implements the synchronized data capture, calculation of intermediate phase and total interpolated angle based on the external 16-bit ADC ADS8354. It follows the algorithms outlined in Section 1.

The flowchart of the ISR is shown in Figure 24.

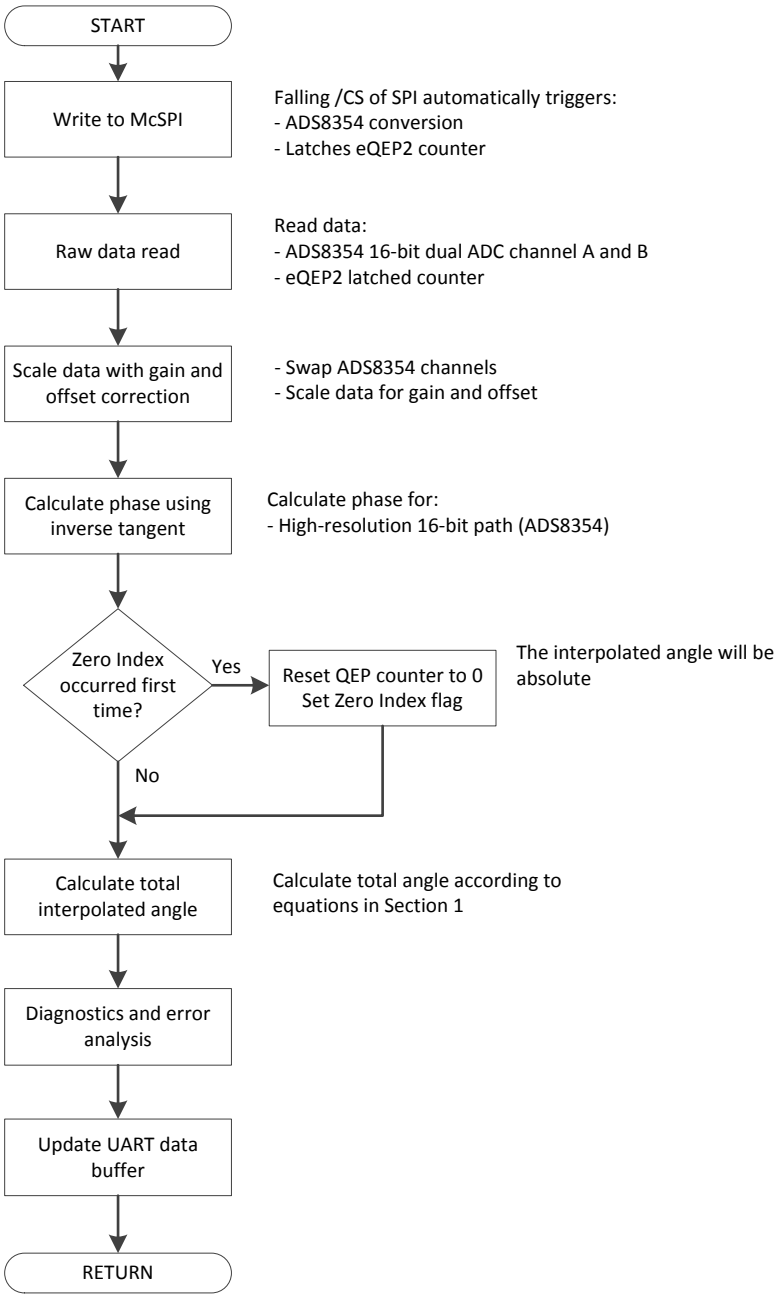

Figure 24. Flowchart of Sin/Cos Encoder Main ISR With Interpolated Angle Calculation

5.3 User Interface

To allow for quick evaluation, a virtual COM port-based user interface was implemented. Any terminal interface at 115000 baud like Tera Term can be used.

The user interface allows the user to enter the line count of the connect Sin/Cos encoder before the program reaches the main menu. The menu provides options for the user to select either a basic display mode with just the high-resolution angle printed or an expert display mode, both with a 10-Hz update rate. Further menu items are data dump modes at a 200-Hz update rate, intended write to a file for post analysis.

The flowchart of the user interface is shown in Figure 25.

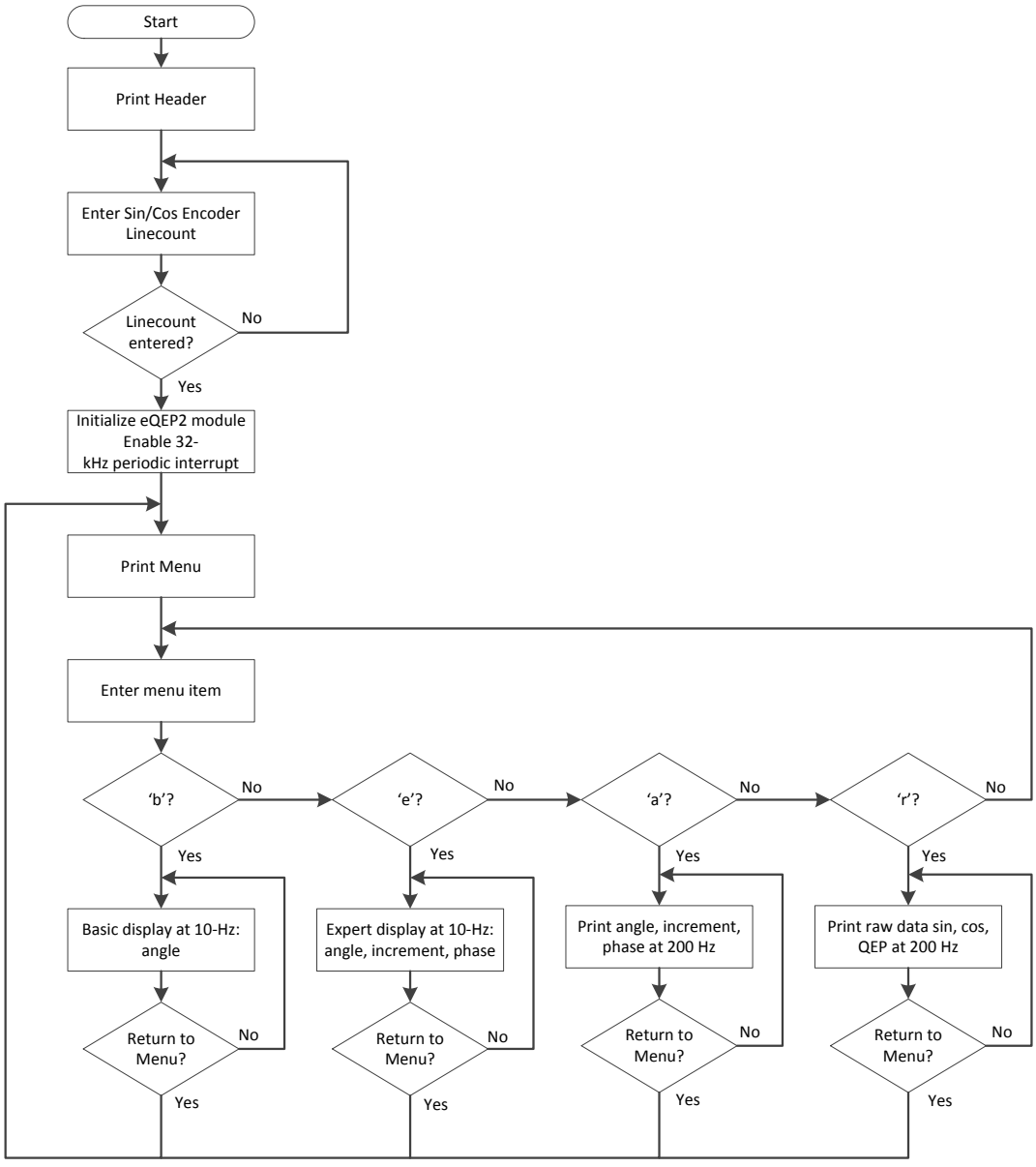

Figure 25. Flowchart of UART Terminal User Interface

Table 17 through Table 20 outline the data output format for each of the four menu items. In data dump mode, a "tab" is included as delimiter between the data in each row.

Table 17. Basic Display Mode Output Format and Data Scaling

MENU	COLUMN 1	COLUMN 2	COLUMN 3	COLUMN 4	COLUMN 5
'b' basic display	Total angle with ADS8354 (Scale)	—	—	—	—
Data format	Float (0° to 360°)	—	—	—	—

Table 18. Expert Display Mode Output Format and Data Scaling

MENU	COLUMN 1	COLUMN 2	COLUMN 3	COLUMN 4
'e' expert display	Total angle with ADS8354 (Scale)	Marker index R occurred	Incremental count	Phase ADS8354 (Scale)
Data format	Float (0° to 360°)	Flag (Yes/No)	Integer	Float (0 to 1.0)

Table 19. Angle Data Dump Menu Format and Scaling

MENU	COLUMN 1	COLUMN 2	COLUMN 3	COLUMN 4
'd' angle dump	Total angle with ADS8354 (Scale)	Incremental count	Phase ADS8354 (Scale)	Periodic tick (Scale)
Data format	Float (0° to 360°)	Integer	Float (0 to 1.0)	Integer (66 µs)

Table 20. Raw Data Dump Menu Format and Scaling

MENU	COLUMN 1	COLUMN 2	COLUMN 3	COLUMN 4	COLUMN 5
'r' raw data	Incremental count (Software)	Incremental count (Latch on /CS)	Input A+/A–, ADS8354 (Scale)	Input B+/B–, ADS8354 (Scale)	Periodic tick (Scale)
	Integer	Integer	Float (V_{PP})	Float (V_{PP})	Integer (66 µs)

5.4 Using Firmware on AM437x IDK With microSD Card

When using the firmware, rename the file "TIDA-00178_SinCosEncoder_AM437x_app.bin" to "app". This app file then needs to be copied to a microSD card, which has the bootloader for the IDK.

To generate the bootloader, see the following web page:

http://processors.wiki.ti.com/index.php/AM437x_SYSBIOS_Industrial_SDK_02.00.00.02_User_Guide#Bootloader

On this web page, read the section "Bootloader" on how to generate and use the bootloader for the AM437x IDK.

When powered, the AM437x IDK will boot the app file from the microSD card, and run the application.

By connecting the terminal program, the application is ready to be used from the PC.

5.5 Software Improvements

While creating the software, it was found out that there is a jitter on the normal peripherals of the AM437x device. This jitter causes a limitation on usage of the hardware.

The jitter is due to non-deterministic clock tree of the used peripherals and the interrupt control unit. To avoid this jitter, use the PRU core of the Sitara to ensure deterministic execution of the code. This was not done for this project, and the code was used as is with the jitter limitation. The jitter was measured to be 200 ns for this example code.

6 Getting Started

6.1 TIDA-00178 PCB Overview

Figure 26 shows a photo of the top side of the TIDA-00178 PCB. The headers and default jumper settings are explained in Section 6.2.

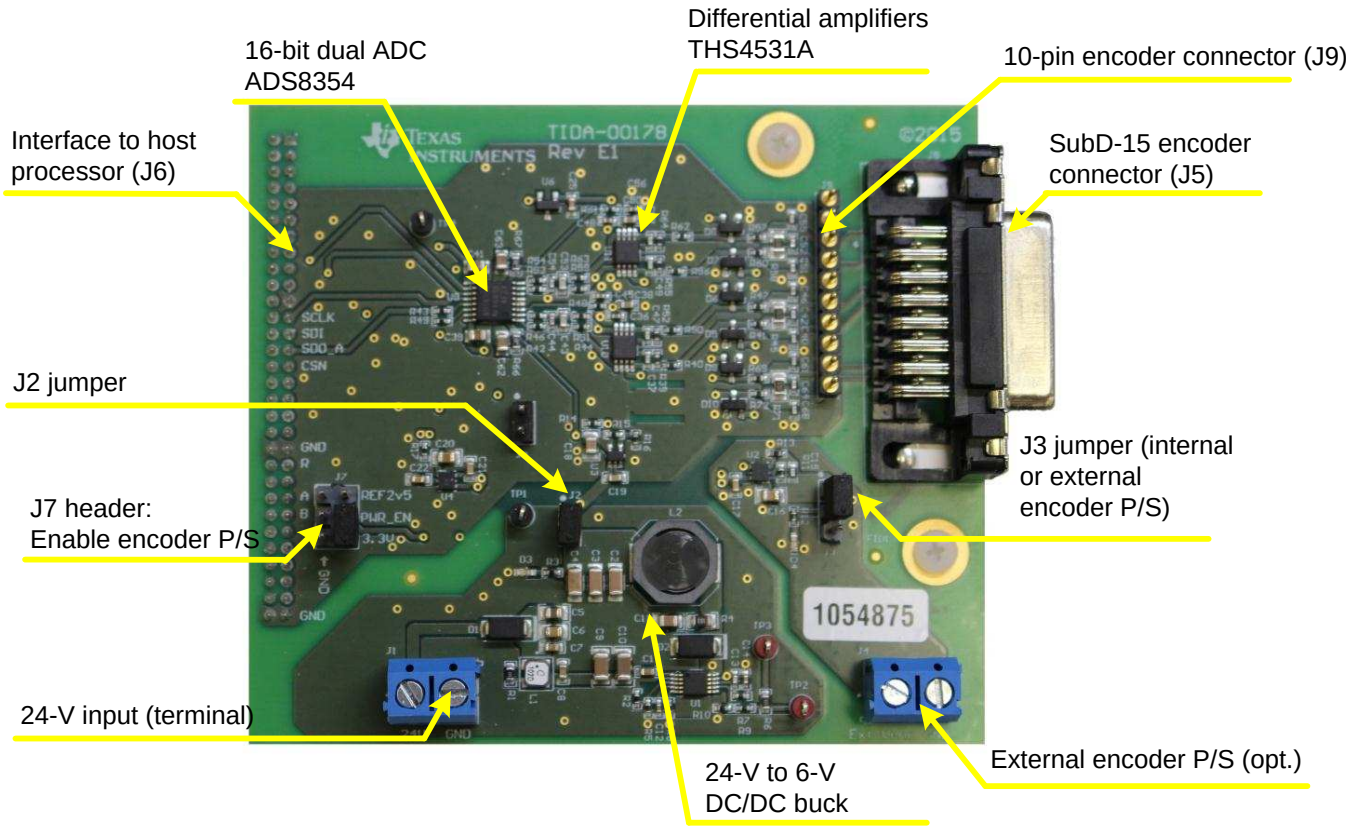

Figure 26. TIDA-00178 Board Picture

6.2 Connectors and Jumper Settings

6.2.1 Connector and Jumpers Overview

The connector assignment and jumper settings are outlined in Table 21 through Table 29.

Table 21. 24-V Input (J1)

PIN	DESCRIPTION
1	24-V input voltage (17 to 36 V)
2	GND

Table 22. J2

PIN	DESCRIPTION
1	Output of TPS54040A (default 6 V)
2	6-V supply rail

Table 23. J3

PIN	DESCRIPTION
1	5.25-V supply (default)
2	V_ENC (encoder supply voltage)
3	External supply

Table 24. External Encoder Supply Connector (J4)

PIN	DESCRIPTION
1	Encoder supply VCC
2	Encoder supply GND

If desired, an external supply voltage other than the 5.25-V encoder supply voltage can be applied through connector J5.

Table 25. Encoder DSUB15 Connector (J5)

PIN	DESCRIPTION	PIN	DESCRIPTION
1	A+	2	Encoder supply GND
3	B+	4	Encoder supply VCC (default 5.25 V)
5	NC	6	NC
7	R-	8	NC
9	A-	10	Reserved
11	B-	12	Reserved
13	NC	14	R+
15	NC		

Table 26. Host Processor Interface (J6)

PIN	DESCRIPTION (3.3-V I/O)	PIN	DESCRIPTION (3.3-V I/O)
1		2	
3		4	
5		6	
7		8	
9		10	
11		12	
13		14	
15		16	
17		18	
19		20	
21	GND	22	
23	SCLK (ADS8354)	24	
25	SDI (ADS8354)	26	
27	SDO_A (ADS8354)	28	
29	/CS (ADS8354)	30	
31		32	
33		34	
35		36	
37		38	
39	GND	40	GND
41	R (TTL)	42	
43	/CS(Strobe)	44	
45	A (TTL)	46	
47	B (TTL)	48	
49		50	
51		52	
53		54	
55		56	
57		58	
59	GND	60	GND

For detailed signal descriptions on the host processor interface, refer to Section 4.3.

Table 27. Header J7 with Encoder Supply Enable (J7)

PIN	DESCRIPTION	PIN	DESCRIPTION
1	GND	2	REFIO (2.5 V)
3	GND	4	ENABLE encoder supply voltage (5.25 V)
5	GND	6	3.3 V

Table 28. Index Test Point (J8)

PIN	DESCRIPTION
1	R–
2	R+

Table 29. Encoder 10SIL100 Connector (J9)

PIN	DESCRIPTION	PIN	DESCRIPTION
1	Encoder supply VCC (default 5.25 V)	2	Encoder supply GND
3	A+	4	A–
5		6	B–
7	B+	8	
9	R–	10	R+

6.2.2 Default Jumper Configuration

Prior to working with the TIDA-00178 board, ensure the following default jumper settings are applied (see Figure 26).

Table 30. Default Jumpers Settings

HEADER	JUMPER SETTING
J3	Insert a jumper between J2 pins 1-2 to enable the 6-V intermediate rail connected the three LDOs.
J4	Insert a jumper between J3 pins 1-2 to route the onboard 5.25-V encoder supply to the encoder connectors.
J7	Insert a jumper between J7 pins 4-6 to enable the 5.25-V encoder supply.

6.3 Design Evaluation

6.3.1 Prerequisites

The following hardware equipment and software is required to allow evaluation of the TIDA-00178 TI design.

Table 31. Prerequisites

EQUIPMENT	COMMENT
24-V power supply	24-V output power supply with at least a 250-mA output current
TIDA-00178 hardware	For default jumper settings per Section 6.2
Three jumpers for board settings	2 pins, 100 mil
TIDA-00178 firmware	Download from TIDA-00178 design folder
Sitara AM437x IDK	Available through TI eStore
USB cable	Mini USB type A to USB type A cable
MicroSD card	Needed to boot from the IDK
PC terminal program	Any terminal program, like for example Tera Term
Sin/Cos Encoder with 1-V_{PP} output signals	For example, ROD480

6.3.2 Hardware Setup

Follow these steps:

1. Connect the TIDA-00178 board with Sitara AM437x IDK using the 60-pin header.
2. Verify the TIDA-00178 is configured with the default three jumper settings per Section 6.2.2.
3. Connect a Sin/Cos encoder to the TIDA-00178 board, by using either the SubD-15 connector (J5) or the SIL-10 connector (J9).
4. Flash the microSD card with the TIDA-00178 application firmware (see Section 5.4).
5. Insert the microSD card into the Sitara IDK SD Card cage.

6. Apply 24 V to the J1 connector of the TIDA-00178 board and 24 V to the Sitara AM437x IDK.
7. Connect the USB micro cable from the Sitara AM437x IDK to the PC.

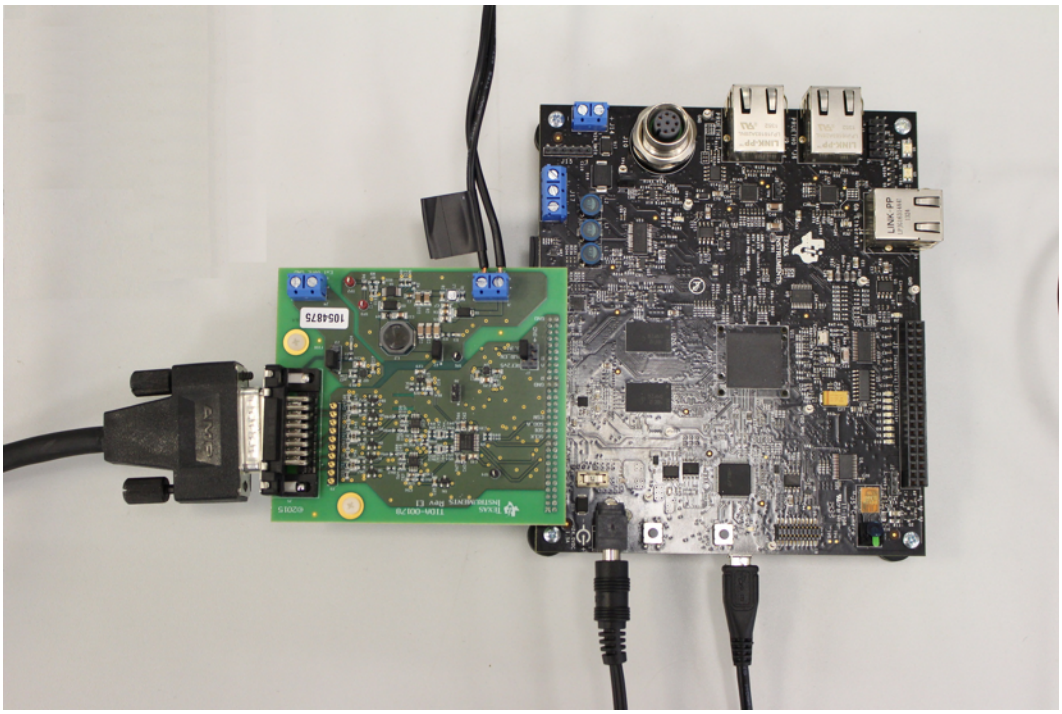

Figure 27. TIDA-00178 Board Mounted With the Sitara AM437x IDK

Also refer to the Sitara AM437x IDK prerequisites at: http://www.ti.com/tool/tmdxidk437x.

6.3.3 Terminal Setup

Follow these steps:

1. Ensure the pre-flashed microSD card is inserted into the microSD Card cage (see Section 5.4).
2. Invoke a terminal program, like Tera Term, that can connect to the virtual COM port.
3. Setup the terminal program in Serial Console mode and set the parameters to: Baud Rate = 115200, Data = 8-bit, Parity = None, Stop = 1-bit, Flow Control = None
4. Press the reset button of the Sitara AM437x IDK (next to the 24-V DC jack).

The terminal program should display the start screen of TIDA-00178 as shown in Figure 28.

Trouble-shooting: If no connection is established, the VCP driver of the USB virtual com port TI XDS100 Channel B needed to be enabled under Windows® 7 Device Manager.

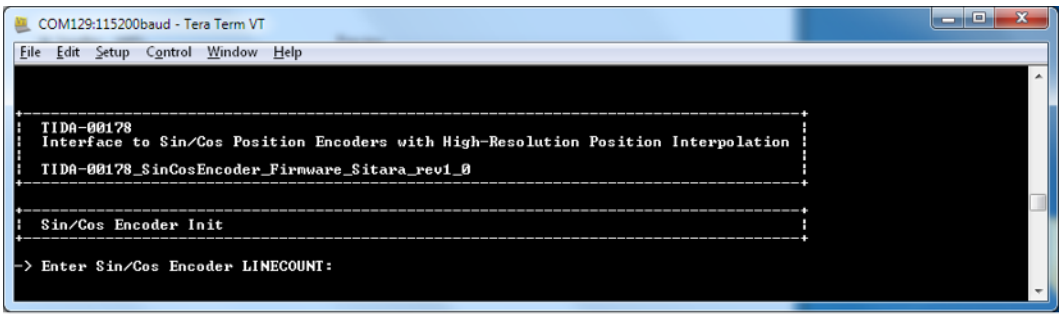

Figure 28. TIDA-00178 User Interface at Start-Up

6.3.4 User Interface

After startup, the user interface requires to enter the Sin/Cos encoder line count in decimal. After the line count is entered, the main menu is available as shown in Figure 29.

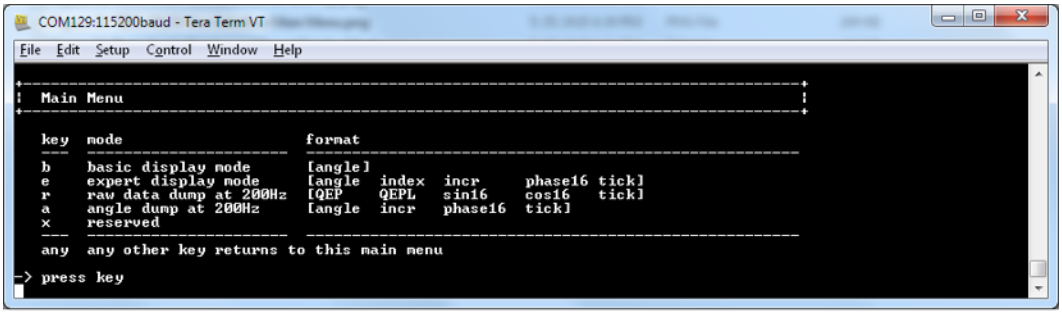

Figure 29. TIDA-00178 User Interface Main Menu

Four menus are available. Each can be selected by pressing the characters b, e, r, or a. The menu item x is reserved for internal test modes during software development.

Press 'b' or 'e' to select the basic or expert display mode, which will print the interpolated angle in degrees or additional information. Note that initially the total angle is not absolute since the index has not occurred. This can be recognized by the Increments Marker set to "No" in the expert display mode. Slowly turn the encoder in clockwise direction until the Increments marker changes to "Yes". Now the interpolated angle is absolute with respect to the index marker position. To return to the main menu, press any key.

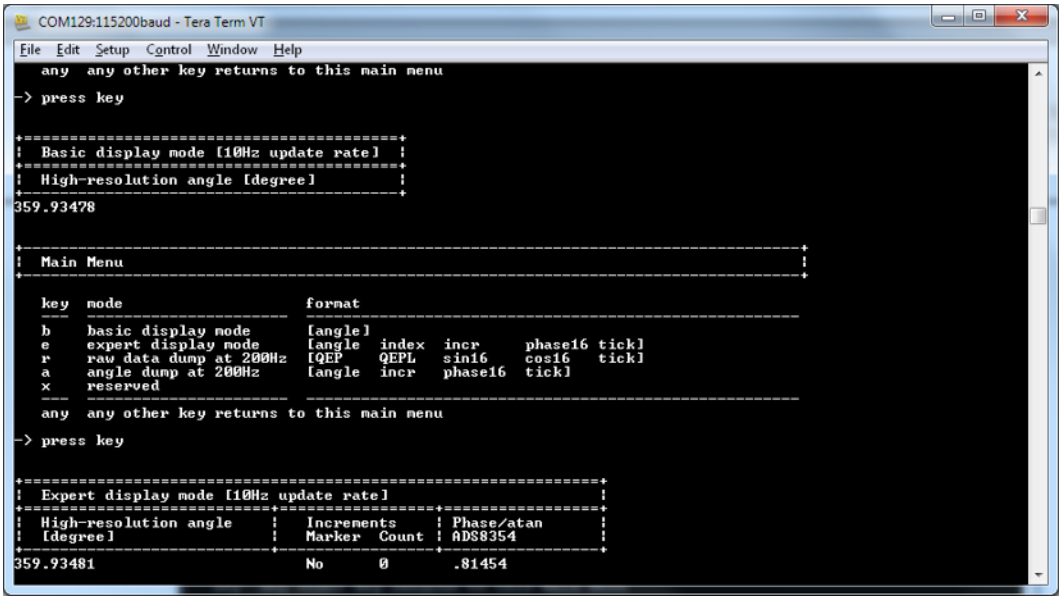

Figure 30. Basic Angle Display and Expert Display Mode

Press 'a' to start an angle data dump at a 200-Hz update rate. The data format is as outlined in Section 5. A screenshot is shown in Figure 31. Press any key to stop and return to the main menu.

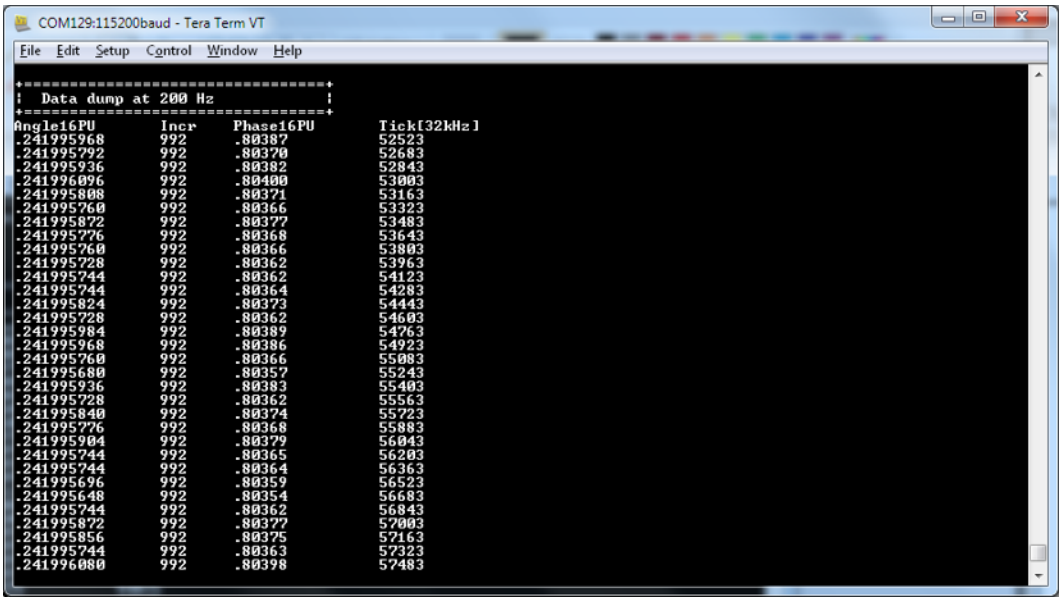

Figure 31. Angle Dump Mode at 200-Hz Update Rate

Press 'r' to start a raw data dump at a 200-Hz update rate. The data format is as outlined in Section 5. A screenshot is shown in Figure 32. Press any key to stop and return to the main menu.

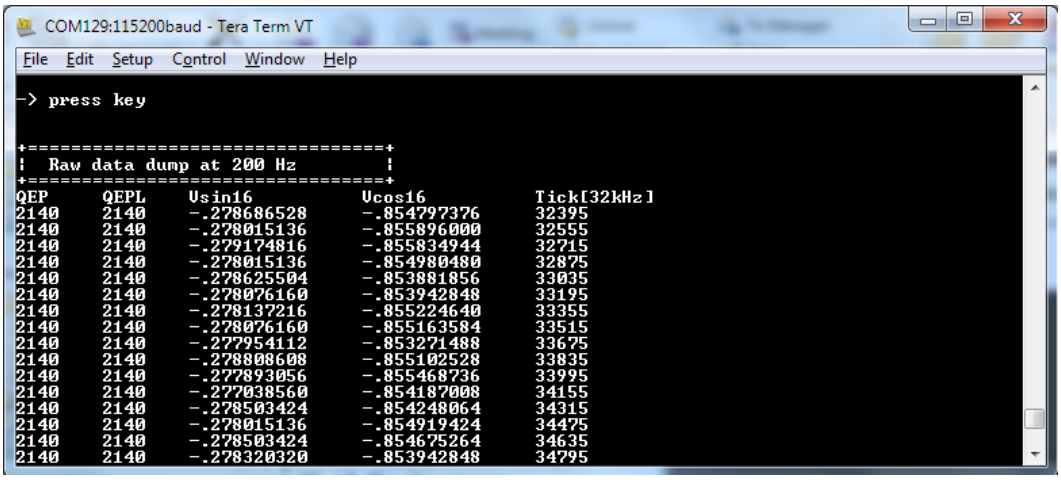

Figure 32. Raw Data Dump Mode at 200-Hz Update Rate

7 Test Results

Tests were done to characterize each individual functional block as well as the entire board. In particular, the following tests were conducted:

- Analog signal chain
- Power management
- Full system with Sin/Cos encoder signal emulation and Sin/Cos encoder

Tests were done at room temperature around 25 degrees. If not mentioned specifically, room temperature applies.

The following equipment has been used for the TIDA-00178 testing session:

Table 32. Test Equipment for TIDA-00178 Performance Tests

TEST EQUIPMENT	PART #
Programmable 16-bit waveform generator	Keysight (Agilent) 33600A
Low speed oscilloscope (suitable for power supply tests)	Tektronix TDS794D
High speed oscilloscope (suitable for analog signal tests)	Tektronix TDS784C
24 V at 2.5-A SMPS (power brick)	V-infinity 3A-621DN24
True RMS multimeter	Fluke 179
Differential probes	Tektronix P6630
Single ended probes	Tektronix P6139A
Programmable thermal chamber	Voetsch VT 4002
Programmable electronic load module	Chroma 63103
Control module for electronic load module	Chroma 6314
HEIDENHAIN shielded cables, PUR M23 male/female (4 × 2 × 0.14 mm; 4 × 0.5mm), 10 m, 20 m, 50 m	#298399-10,-20,-50
HEIDENHAIN M23/Sub-D15 Male Adapter Cable, 1 m	#310196-01
HEIDENHAIN Sin/Cos Encoders	ROD480-2000, ROD480-1024, ROD486-2048

7.1 Analog Performance Tests

Figure 33 shows a picture of the TIDA-00178 analog signal chain tests.

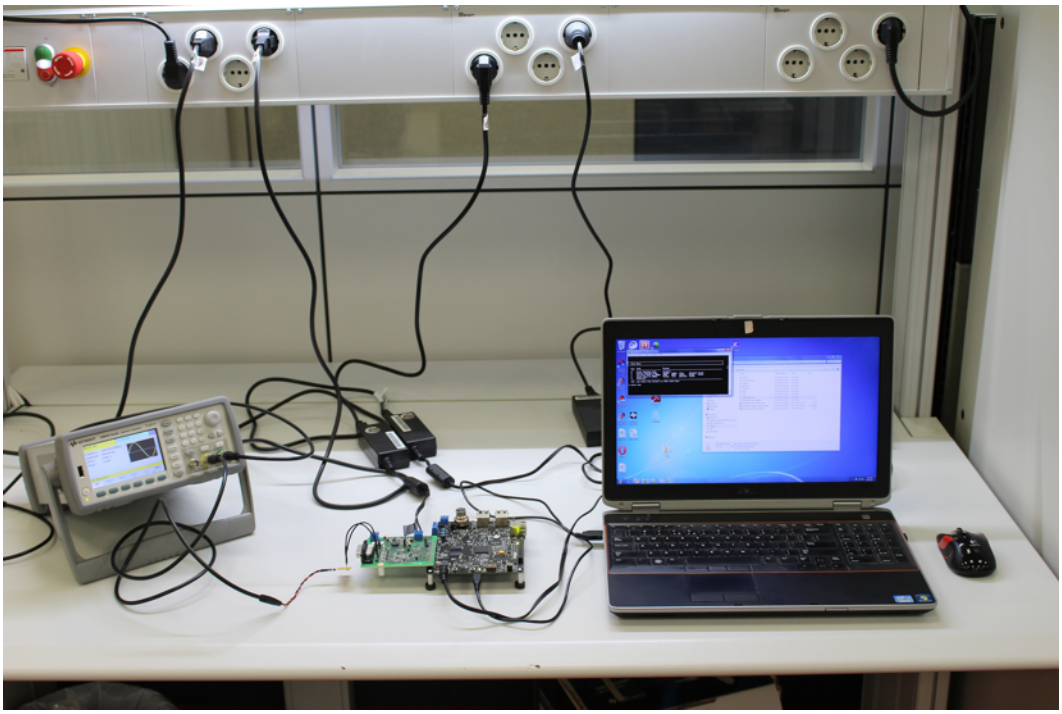

Figure 33. Picture of Test Setup for TIDA-00178 Analog Signal Chain Performance Tests

The high-resolution 16-bit signal path featuring fully differential amplifiers THS4531A and the dual 16-bit ADC ADS8353 have been tested. For the purpose, a dual output programmable function generator has been used. The inputs signals are applied at the connector J9 (differential inputs A, B, and R). The output waveforms have been collected at different probe points, depending on the signal path that was analyzed.

7.1.1 High-Resolution Signal Path

The measurements have been taken on the high-precision, high-resolution signal path. A sinusoidal signal with 1 V_{PP} was injected at the encoder connector J9 inputs A+,A– and B+, B– and the differential analog signals was measured at the ADS8354 differential inputs. Figure 34 outlines the input and output signals measured for the test.

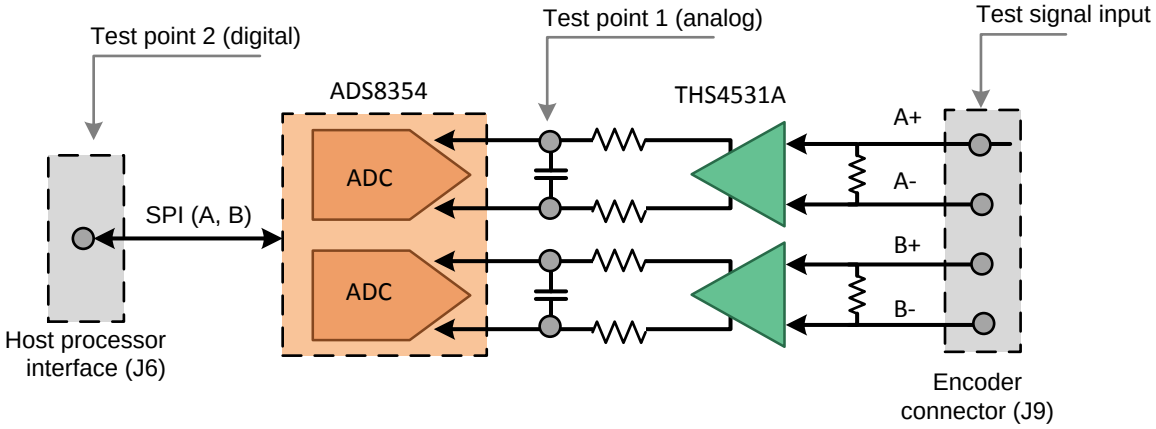

Figure 34. High-Resolution Signal Chain Measurement Points

7.1.1.1 Bode Plot of Analog Path From Encoder Connector to ADS8354 Input

Figure 35 shows the magnitude and phase response, which is mainly defined by the THS4531A gain setting of 5 and the passive first order low-pass filter comprised of two 10-Ω series resistors and the 4.4-nF parallel capacitor.

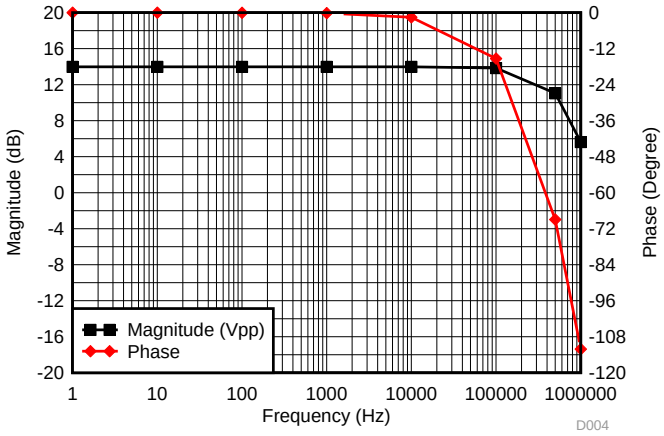

Figure 35. Bode Plot for the High-Resolution Analog Signal Chain From the Encoder Differential Input to ADS8354 Differential Input

7.1.1.2 Performance Plots (DFT) for Entire High-Resolution Signal Path

For the following tests, the entire high-resolution signal chain, featuring the differential amplifier THS4531A connected through an RC filter to the dual 16-bit ADC ADS8354 has been tested. A sinusoidal test signal has been injected at the encoder differential input pins and the 16-bit digital data has been analyzed.

The analysis has been done in the frequency domain to evaluate the performance on the Signal-to-Noise Ratio (SNR), Total-Harmonic-Distortions (THD), Signal-to-Noise And Distortion (SINAD), and Effective Number of Bits (ENOB). Essentially, all these parameters are different ways of quantifying the noise and distortion performance of an ADC based on a Fast-Fourier Transform (FFT) analysis. A brief introduction on the theory of signal-to-noise measurement with ADCs is provided at the end of this section.

For the test, a 100-Hz sine wave at an amplitude of $0.6V_{PP}$ is generated. This is the same signal that a low output of Sin/Cos encoder would be.

The input signal is applied to one of the input channels A+,A– or B+, B– at a time, while the other channel is unconnected. The purpose is to measure and highlight the ultra-low cross-talk level among the two channels A and B (or sine and cosine, respectively).

The DC input is used to ensure the best noise performance (since no noise comes from the input or source). The 100-Hz sine wave is used to measure the effective number of bits on the two parallel channels.

Both channels A and B were sampled at 32 kHz and 8192 consecutive 16-bit samples were acquired for each channel A and B. The DFT has been calculated for the collected data.

The following figures show the DFT of the entire high-resolution channel with a sinusoidal input voltage of a $0.6\text{-}V_{PP}$ amplitude and 100 Hz. This equals around a –6-dB input level versus the theoretical full scale range input.

The input signal was applied either to the channel A or channel B. The other channel was left open in order to measured cross-talk too.

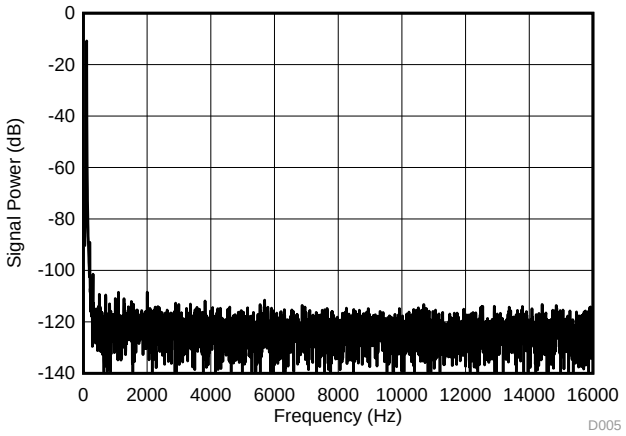

Figure 36. DFT of 16-Bit Channel A Output With 600-mV_{PP} 100-Hz Sine Wave Input Applied on Input A

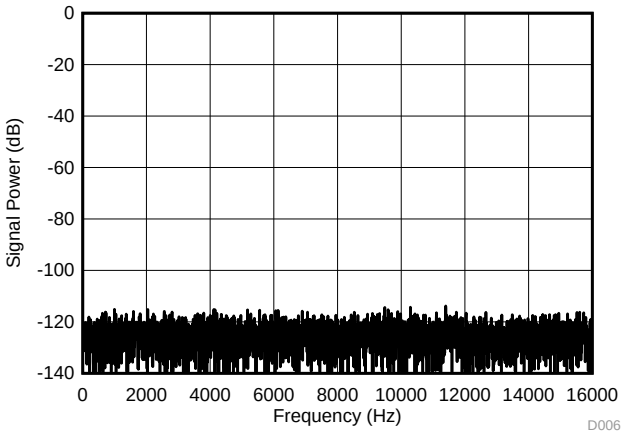

Figure 37. DFT of 16-Bit Channel B Output With 600-mV_{PP} 100-Hz Sine Wave Input Applied on Input A

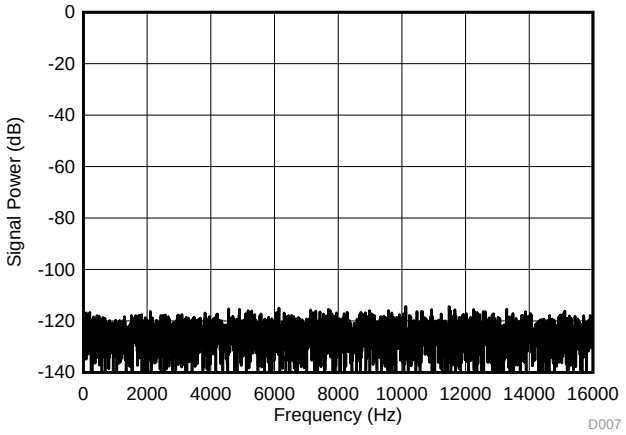

Figure 38. DFT of 16-Bit Channel A Output With 600-mV_{PP} 100-Hz Sine Wave Input Applied on Input B

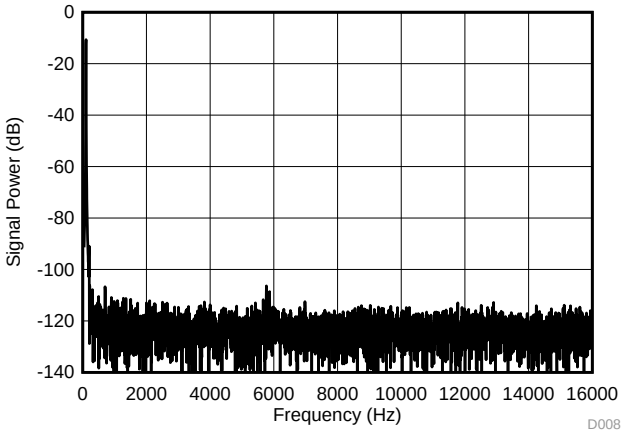

Figure 39. DFT of 16-Bit Channel B Output With 600-mV_{PP} 100-Hz Sine Wave Input Applied on Input B

These figures are referred to the theoretical full scale input range. To achieve these results, a very aggressive notch filter was used to filter the frequency of the test signal.

The reason why this test was done with a 100-Hz signal is due to the jitter of the Sitara software implementation. The Sitara triggers the SPI transfer, which starts the ADS8354 conversion (hold mode). This jitter causes a non-deterministic measurement error, which translates into a noise floor. The noise floor is proportional to the input signal amplitude and frequency. The jitter on the SPI /CS is due to the current setup of the clocking tree and interrupt structure chosen. For more information, see Section 5.5.

The previous pictures also highlighted that there is basically no cross-talk between the two analog channels for sine (signal A+, A–) and cosine (B+, B–). The spectrum (DFT) is half the sampling frequency (the second half of the spectrum is a specular copy of the first half, so it is not shown in the plots). The Hann function (http://en.wikipedia.org/wiki/Hann_function) is used for windowing the data to obtain cleaner plots in the frequency domain.

7.1.2 Comparator Subsystem With Digital Output Signals A_{TTL}, B_{TTL}, and R_{TTL}

In this section, the performance of the comparator with hysteresis that converts the single-ended analog signals A, B, and R into digital signals was tested.

The focus was on the propagation delay of the comparator output signals A_{TTL}, B_{TTL}, and R_{TTL} at the host connector J6 versus the analog input at the ADS8354 for the high-resolution path as well as the single-ended analog signals for the analog path.

The aim of the test was to measure the overall signal delay of the comparator path versus the analog path, considering the delays introduced by hysteresis, phase shift due to low-pass filtering, and the propagation delay of the comparator itself.

Because all three channels (A, B, and R) were done absolutely identical with regards to the comparator output, measurements have only been conducted with channel A.

The analog signals were both measured with a single-ended probe; therefore, on the differential input of the ADS8354, only the positive differential signal was measured versus GND.

For the test sinusoidal, input signals were injected at the encoder connector J9, A_P, A_M (sine), and B_P, B_M (cosine) as well as P_M and R_P.

For the high-resolution path, the amplitude was set to 1.0 V_{PP} (typical) and 0.3 V_{PP} (minimum) with 100 Hz and 500 kHz (maximum) to test the worst case scenario for the propagation delay. For the analog path, the measurement was conducted at 0.3 V_{PP} with 100 Hz and 500 kHz as corner cases.

Test results are shown in the following figures.

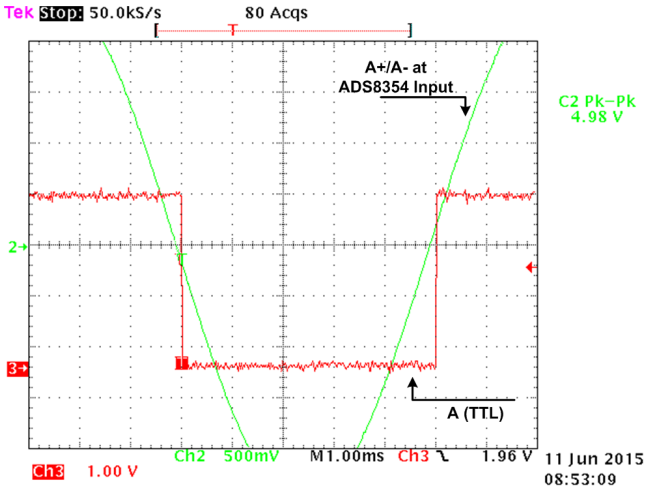

Figure 40. Comparator Output A_{TTL} versus Differential Input to ADS8354 With Input 1.0 V_{PP}, 100 Hz at Encoder Connector J9-3, J9-4

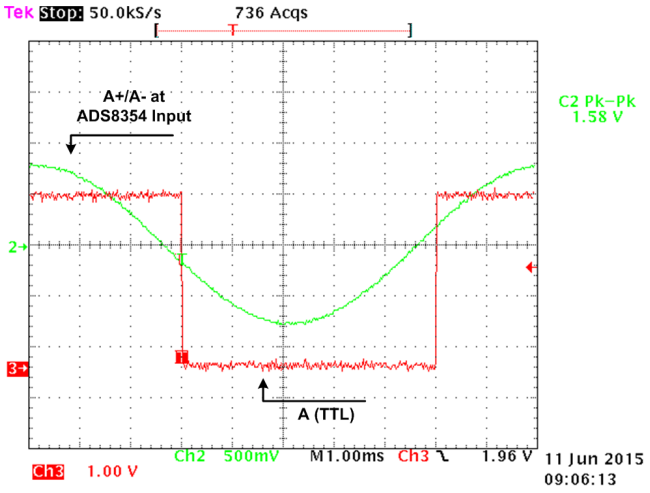

Figure 41. Comparator Output A_{TTL} versus Differential Input to ADS8354 With Input 0.3 V_{PP}, 100 Hz at Encoder Connector J9-3, J9-4

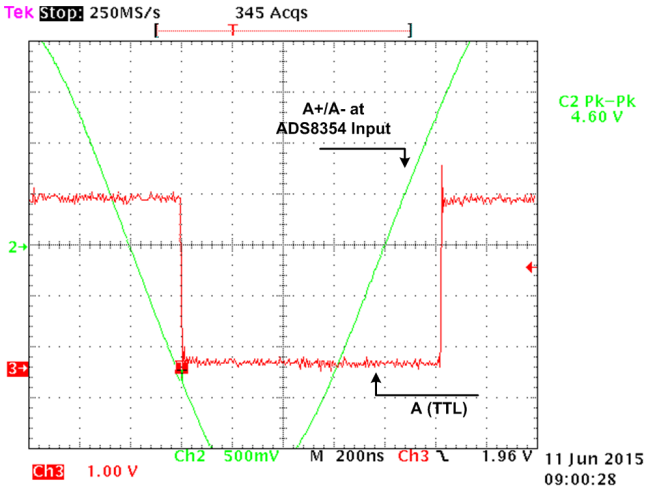

Figure 42. Comparator Output A_{TTL} versus Differential Input to ADS8354 With Input 1.0 V_{PP}, 500 kHz at Encoder Connector J9-3, J9-4

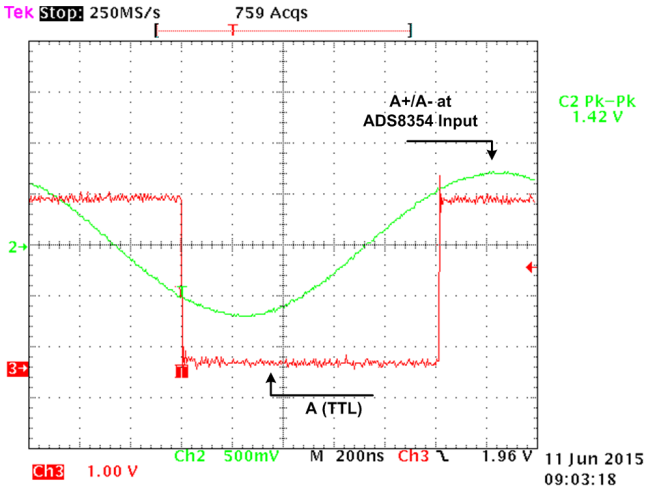

Figure 43. Comparator Output A_{TTL} versus Differential Input to ADS8354 With Input 0.3 V_{PP}, 500 kHz at Encoder Connector J9-3, J9-4

As expected, the maximum overall phase shift including RC filter decoupling networks occurs at 500 kHz with the lowest input amplitude and is in total around 260 ns, equal to 46.8 degrees, (well below 90° and within the 60° specification per Section 2). The very low propagation delay of the TLV3201 with typically 40 ns has a major impact on this low number. This also gives a major margin to compensate all the possible spreads in the parameters influencing the amount of phase delay like due to low-pass filters, and so on.

The propagation delay at 100 Hz is almost the same than for the high-resolution channel, since the delay at lower frequencies is dominated by the amplitude-dependent hysteresis.

7.2 Power Supply Tests

7.2.1 24-V DC/DC Input Supply

The following tests were performed to characterize the DC/DC buck converter, which converts the 24-V input supply to a 6-V intermediate rail.

7.2.1.1 Load-Line Regulation

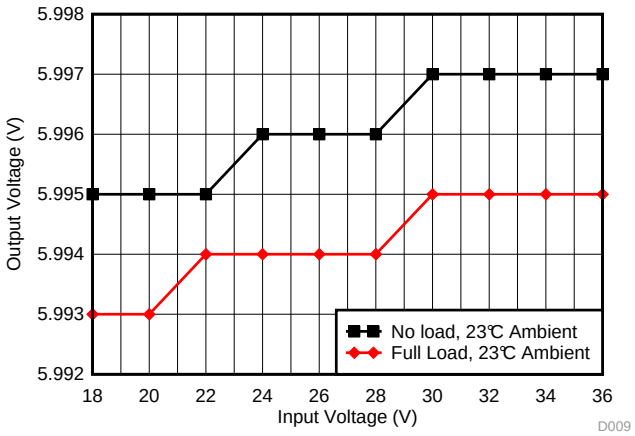

Figure 44. Load-Line Regulation

Line-load regulation is within the ±10-mV range over the full working conditions. V_{OUT} is the expected 6 V ±2% (regulator's accuracy) plus the accuracy of the resistor divider R7/R10.

7.2.1.2 Output Voltage Ripple

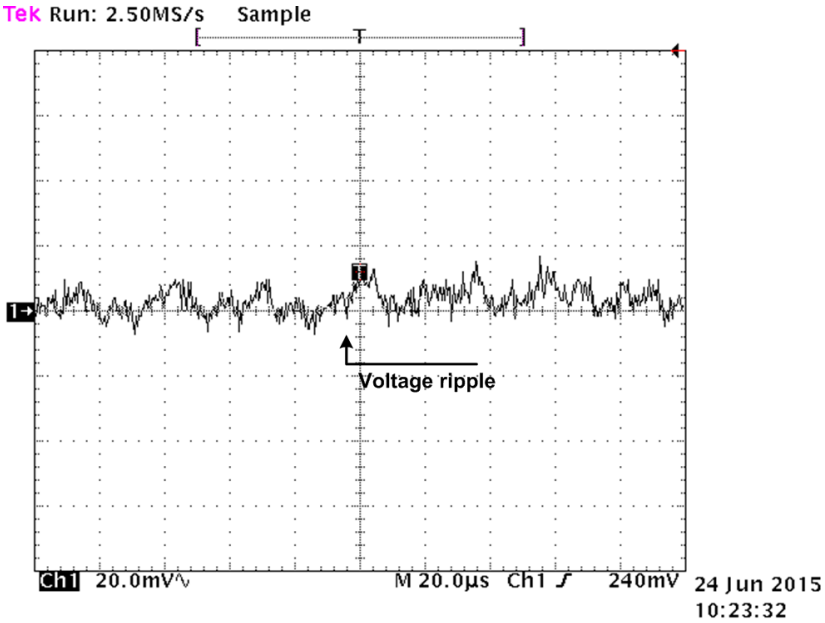

Figure 45. Output Voltage Ripple at 24-V Input, No Load, at 25°C Ambient Temperature

The VOUT ripple meets the required 20 mV_{PP}.

7.2.2 Encoder Power Supply Output Voltage

The output voltage of the LDO providing the supply for the encoder is well regulated and meets the specification requirements, as for the following measurements.

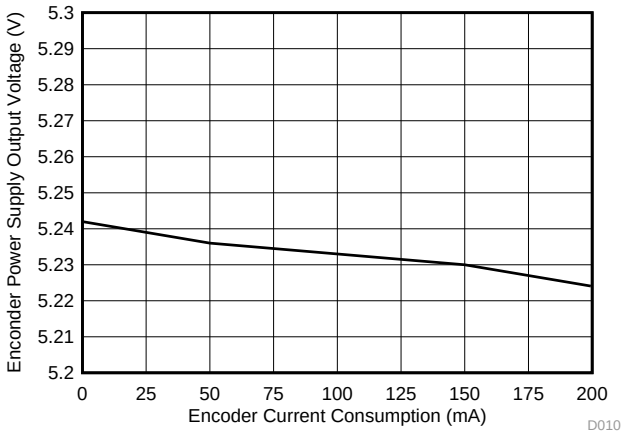

Figure 46. Encoder Power Supply Output Voltage versus Load Current (0 to 200 mA)

7.2.3 5-V and 3.3-V Point-of-Load

The output voltages of the two LDO to generate the point-of-load providing the supply for the signal chain block are well regulated and meet the specification requirements. Measurements are shown in Table 33. The nominal current consumption on the 3.3-V and 5-V rails was measured with a Sin/Cos encoder connected and the Sitara IDK triggering a new measurement at 32 kHz.

Table 33. Measured Output Voltage

SPECIFIED OUTPUT VOLTAGE	MEASURED VOLTAGE AT NOMINAL LOAD	NOMINAL CURRENT
5.0 V	5.05 V	7.13 mA
3.3 V	3.31 V	0.05 mA

7.3 System Performance

7.3.1 Sin/Cos Encoder Output Signal Emulation

For this purpose, the encoder output signals have been emulated using a 16-bit programmable dual-output signal generator Keysight (Agilent) 33600A. Sinusoidal test signals were injected into the differential inputs A+,A– and B+,B–.

In this section, the system level performance have been measured. In particular:

- Accuracy over one electrical period (phase)
- Accuracy over one revolution at maximum input frequency of 500 kHz. Here, the encoder emulation was based on 2000 signal periods equal to one emulated revolution

The tests were done at room temperature and have been repeated at 70° to check the error drift versus temperature.

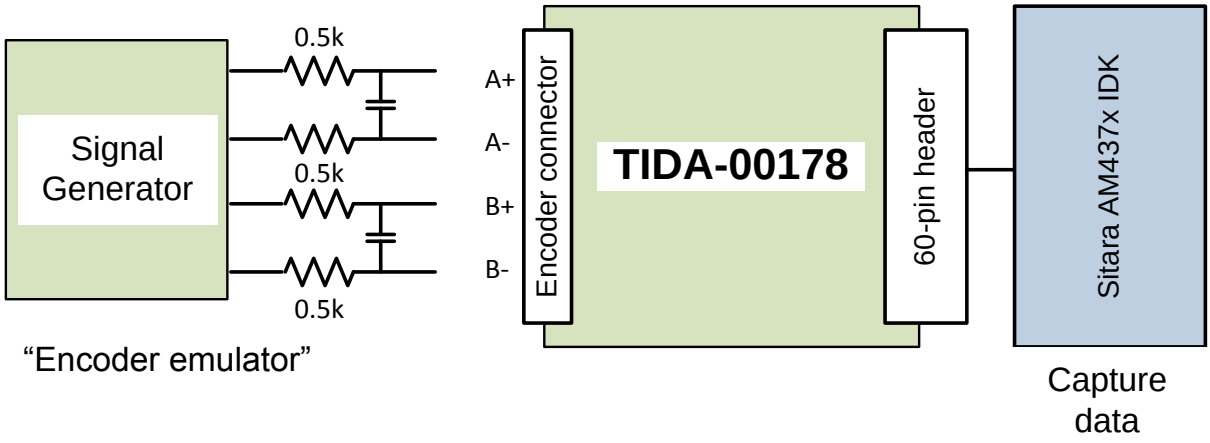

Figure 47. Test Setup for Encoder Signal Emulation

7.3.1.1 One Period (Incremental Phase) Test

The first tests showed that the error injected by the dual output signal generator was much worse than the TIDA-00178 accuracy, spoiling completely the purpose of the tests. Noise and error sources for could be summarized as:

- Gain error (amplitude of A not equal to the amplitude of B)
- Phase shift error (not exactly 90° constant as expected)
- Offset error (average of A and B signal is not equal to 0)
- HF noise due to the quantization error of the function generator
- Frequency error (frequency of A is not equal to B, even if the signal are "coupled")

CAUTION

In order to reduce the quantization error or noise introduced by the function generator, an RC low-pass filter with 1 kΩ and 1 µF is inserted between the signal generator and the TIDA-00178 inputs (the 1K resistor is actually a series of two 500-Ω resistors to keep the network balanced) on the input.

To eliminate gain, offset, phase shift, and frequency error between the two channels, the following setup was applied: Only one output signal, filtered as previously described, was applied to both inputs A and B at the encoder connector J5 of the TIDA-00178, thus feeding with the same signal. This will eliminate the limitation of the function generator. Furthermore, any mismatch amongst the two channels of the ADS8354 (and their respective signal conditioning paths) can be better evaluated.

The data acquired from the ADS8354 should ideally show two streams of raw identical data, while any mismatch at this level comes from the mismatch of the two channels and not from the input itself. This can be also used to calibrate the system because offset and gain error corrections could be performed to completely balance the A and B channels.

The data has been acquired at a 32-kHz sample rate using the Sitara IDK connected to the TIDA-00178, as outlined in Section 6.

After the ADS8354 channel A and B data has been acquired by the Sitara host processor, the 32-bit raw data has been dumped into an Excel® file. Then the raw data for channel B has been exactly phase shifted by 90°. After that, the phase has been calculated using the inverse tangent of the raw data A and 90° phase shifted raw data B.

This test has been done for the 0.6-V_{PP} amplitude and a frequency of 10 Hz. The result is shown in the following figures.

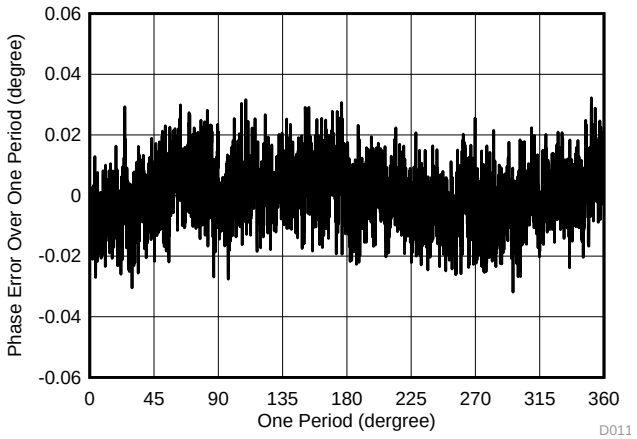

Figure 48. Phase Error at 25°C Ambient Over One Signal Period When 0.6-V_{PP}, 10-Hz Input is Applied

Within one incremental line (one signal period = 360°), the phase error remains well within ±0.025°. This corresponds to an error ±0.025/360 = 0.0069%. With respect to the 16-bit resolution, this only equals around ±2.5 LSB only. The noise distribution is even within ±0.0125 (±1.25 LSB).

The phase error with the double period is due to a non-ideal 90° phase shift between the two signals A and B. For more information on phase error interpretation, see the design guide for the TIDA-00178.

Note that an error of ±0.025° over one signal period will correspond to a total error of ±13 micro-degrees (0.045 arc seconds) for an encoder with 2000 line counts.

The same tests have been performed in the thermal chamber at a nominal 70°C to evaluate the system performance drift and, in particular, the absolute error on the angular position.

Again, the double frequency modulation comes from the non-perfect matching (90° phase shift, and so on) of the two input signals.

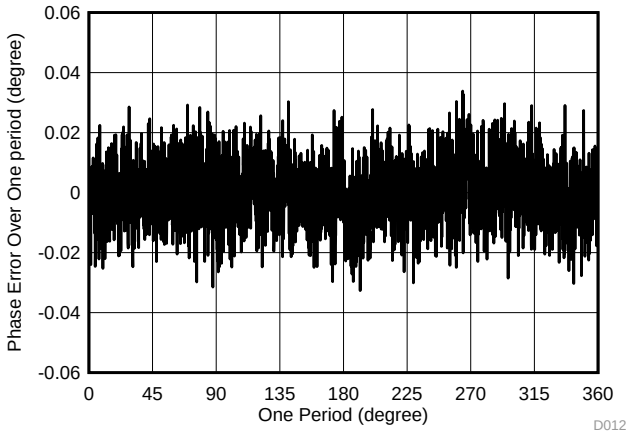

Figure 49. Phase Error at 70°C Ambient Over One Signal Period (One Revolution/2000) When 0.6-V_{PP}, 10-Hz Input is Applied

Within one incremental line (one signal period = 360°), the phase error remains well within ±0.03°. This corresponds to an error ±0.03/360 = ±0.0083%. With respect to 16-bit resolution, this equals to around ±3 LSB. The noise distribution is even within ±0.015 (±1.5 LSB).

Note that an error of ±0.03° over one signal period will correspond to a total error of ±15 micro-degrees (0.054 arc seconds) for an encoder with 2000 line counts.

The low drift versus temperature is aligned to the expectation, also because of the characteristics of the selected op-amps and matched resistors used for the analog signal conditioning.

7.4 Sin/Cos Encoder System Tests

Systems tests have been done with Sin/Cos encoders ROD480-2000 and ROD480-1024 with a cable length of 1 m and 71 m.

7.4.1 Zero Index Marker R

The first test was to verify the synchronization and skew between the digital output signals A, B, and R available at the TIDA-00178 host processor interface connector J6, pin 45 (A_{TTL}), pin 47 (B_{TTL}), and pin 41 (R_{TTL}). This test verifies the proper configuration of the TIDA-00178 comparator subsystem.

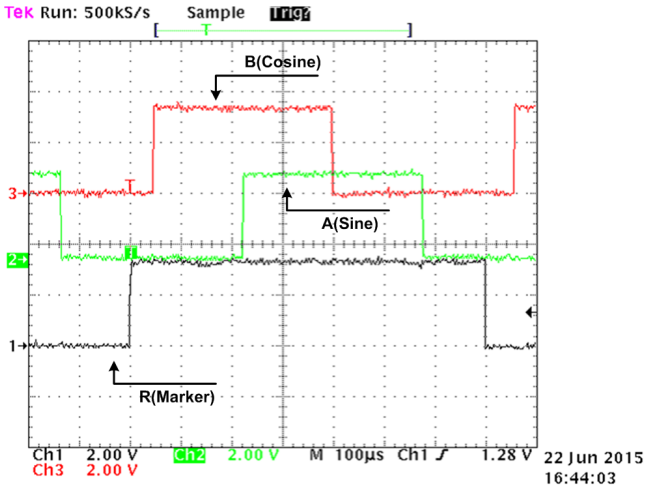

Figure 50. Measured TTL Signals A, B, and R at TIDA-00178 Comparators Output J6-12, 14, and 18 With Encode in CCW Rotation

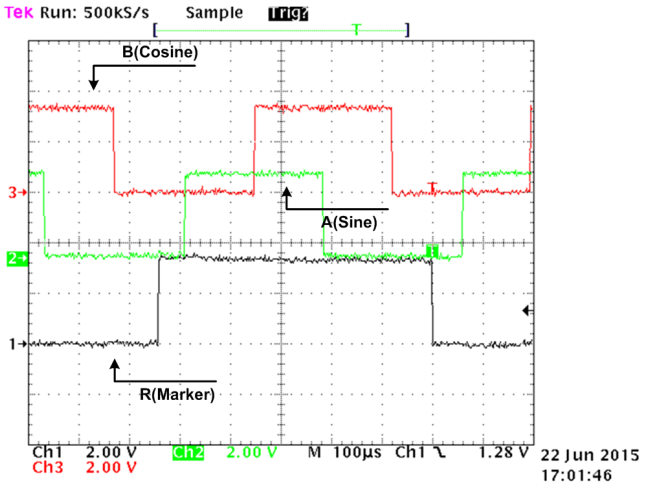

Figure 51. Measured TTL Signals A, B, and R at TIDA-00178 Comparators Output J6-12, 14, and 18 With Encode in CW Rotation

The transitions on the comparator output signal R occur only when both A and B are low as expected. The sequence between A, B, and R signals depends on the rotation direction of the Sin/Cos encoder shaft. In the above plots, the encoder is turned clockwise (CW) and counter clockwise (CCW) to show that the index has a different position compared to the Sin and Cos signals depending on the direction of the encoder.

A closer look to the skew between A, B, and R has been done at a higher speed of around 400 rpm, for falling and rising edge of R. The rising and falling edge of R still occurs when both signals A and B are low. This is the case for both CCW and CW directions.

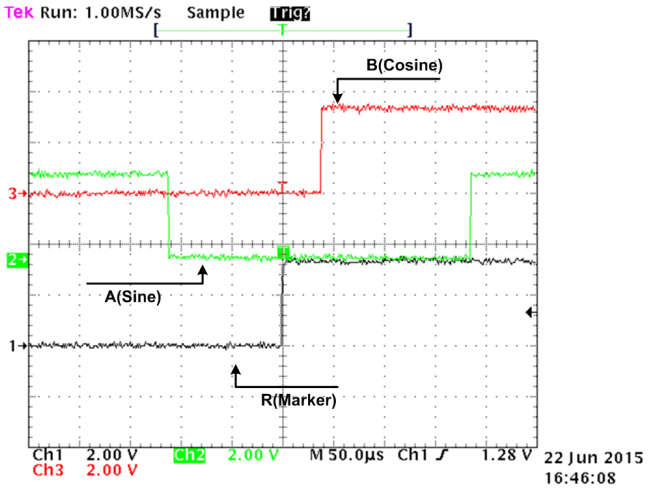

Figure 52. Rising Index Signal R versus A and B With Encode in CCW Rotation

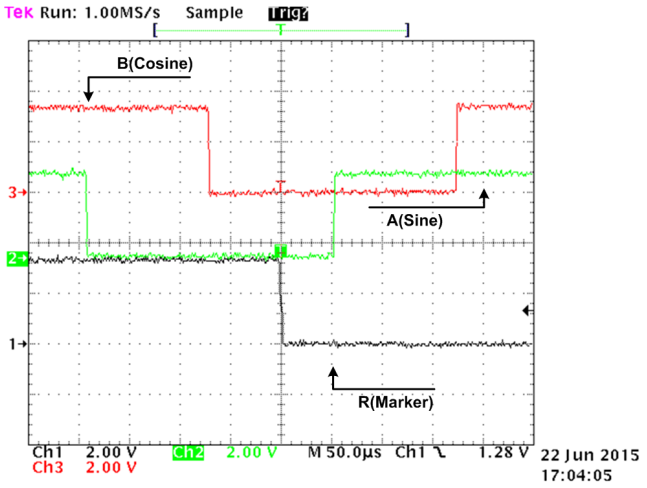

Figure 53. Falling Index Signal R versus A and B With Encode in CW Rotation

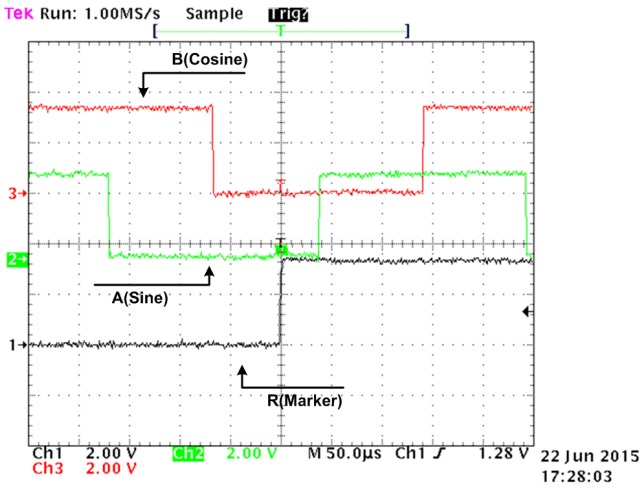

Figure 54. Rising Index Signal R versus A and B With Encode in CW Rotation

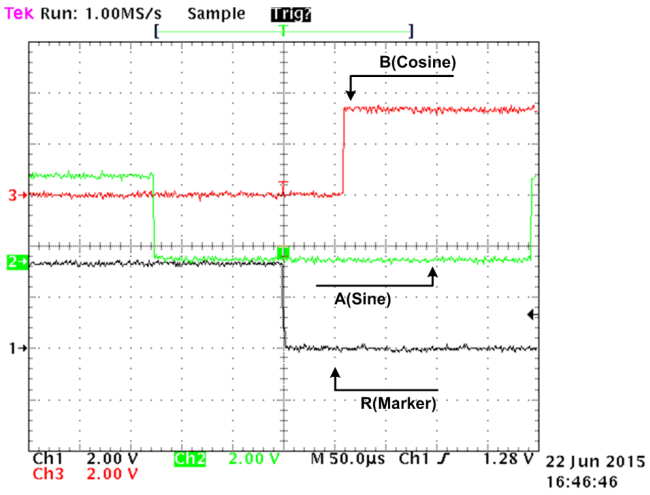

Figure 55. Falling Index Signal R versus A and B With Encode in CCW Rotation

7.4.2 Functional System Tests

The following static angle tests have been done with a ROD480-1024 Sin/Cos Encoder at 1-m and 71-m cable length. Total accuracy measurements with a precision better than 0.003° (10 arc seconds) were not possible due to a lack of a mechanical precise enough encoder test bench. A picture of the test setup is shown in Figure 56.

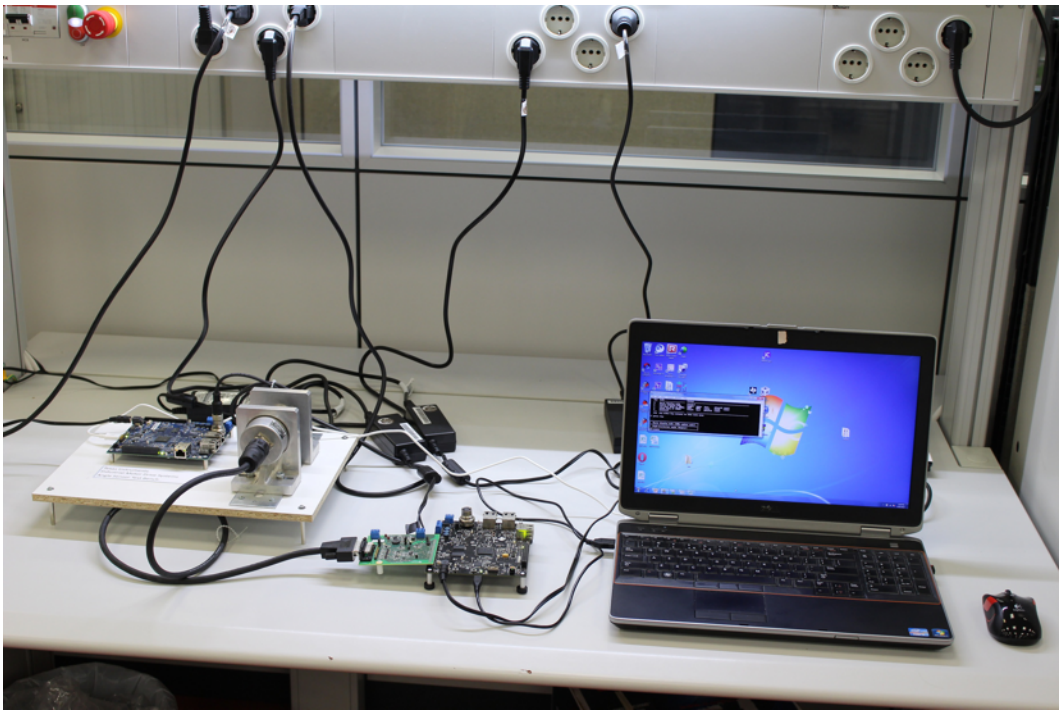

Figure 56. TIDA-00178 Test Setup With 1-m Cable (Varies From 1 to 70 m) and ROD4800-1024 Sin/Cos Encoder

Figure 57 and Figure 58 show the measured angle with the ROD480-1024 (1024 line count) over time for a static angle at 1-m and 70-m cable length accordingly. The shaft was not fixed.

Note that the absolute angle for the 1-m and 71-m measurements slightly change due mechanical vibrations when unscrewing the 1-m cable from the encoder and mounting the 70-m cable instead.

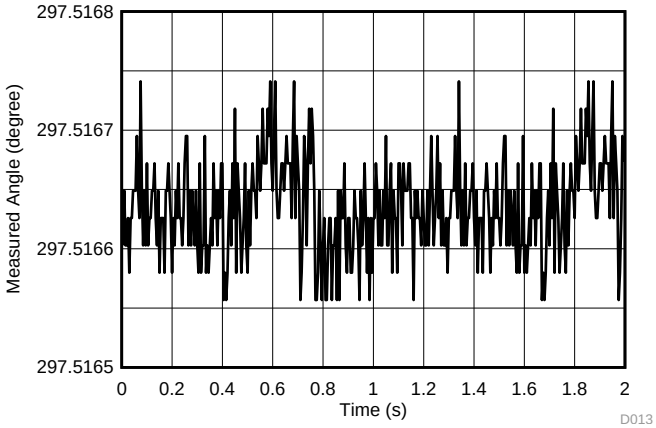

Figure 57. System Test, Measured Angle Distribution With ROD480-1024 at 1-m Cable Length

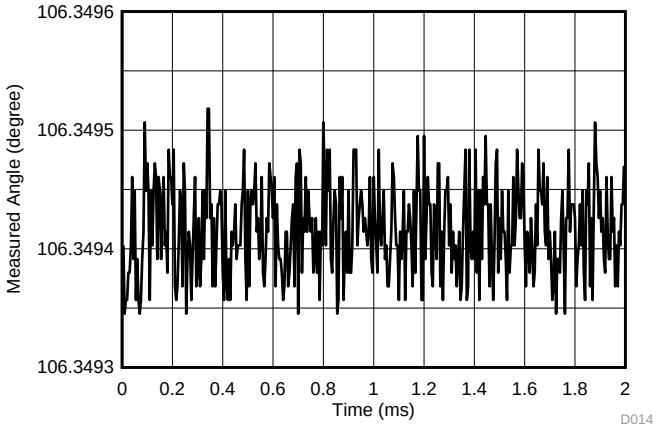

Figure 58. System Test, Measured Angle Distribution With ROD480-1024 at 71-m Cable Length

The measured angle with the ROD480-1024 has a noise distribution of ±0.0001 degrees (0.36 arc seconds). There is no significant difference between the 1-m and 71-m measurements because the attenuation of the cable was around –1.5 dB at 0 Hz.

To verify the basic accuracy and repeatability of the TIDA-00178 design with a Sin/Cos encoder, the ROD480-1024 Sin/Cos encoder was mechanically coupled with an EnDat 2.2 encoder ROQ437. The ROD480-1024 was connected through a 71-m cable. A picture of the test setup is shown in Figure 56.

Figure 59 shows the angle difference between the TIDA-00178 connected to a ROD480-1024 Sin/Cos encoder and a ROQ437 EnDat 2.2 absolute encoder, where the absolute angle was read through the Sitara AM437x EnDat 2.2 Master. The absolute angle exhibits a cosine-shape error, which is due to a non-ideal, non-centric coupling of the two shafts with a small run-out.

The encoder was turned multiple times and the angle was captured accordingly to check repeatability as well.

As expected, however, the mechanical setup was not accurate and precise enough to draw conclusions on the overall absolute system accuracy. Therefore, the tests conducted in Section 7.3 based on encoder emulation are more representative to the performance to be expected from the TIDA-00178 reference design.

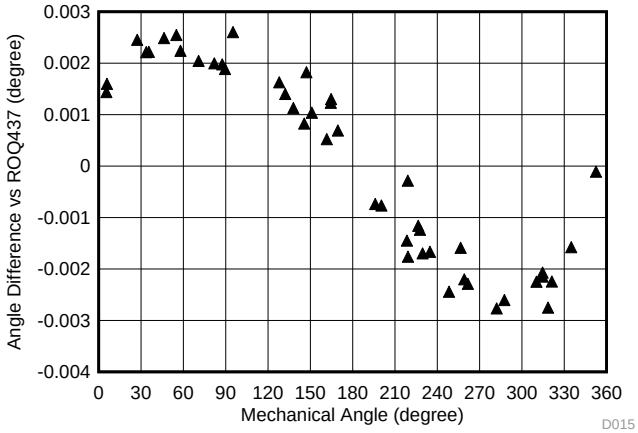

Figure 59. Basic System Accuracy Test With Sin/Cos Encoder at 71-m Cable Length

8 Design Files

8.1 Schematics

To download the schematics, see the design files at TIDA-00178.

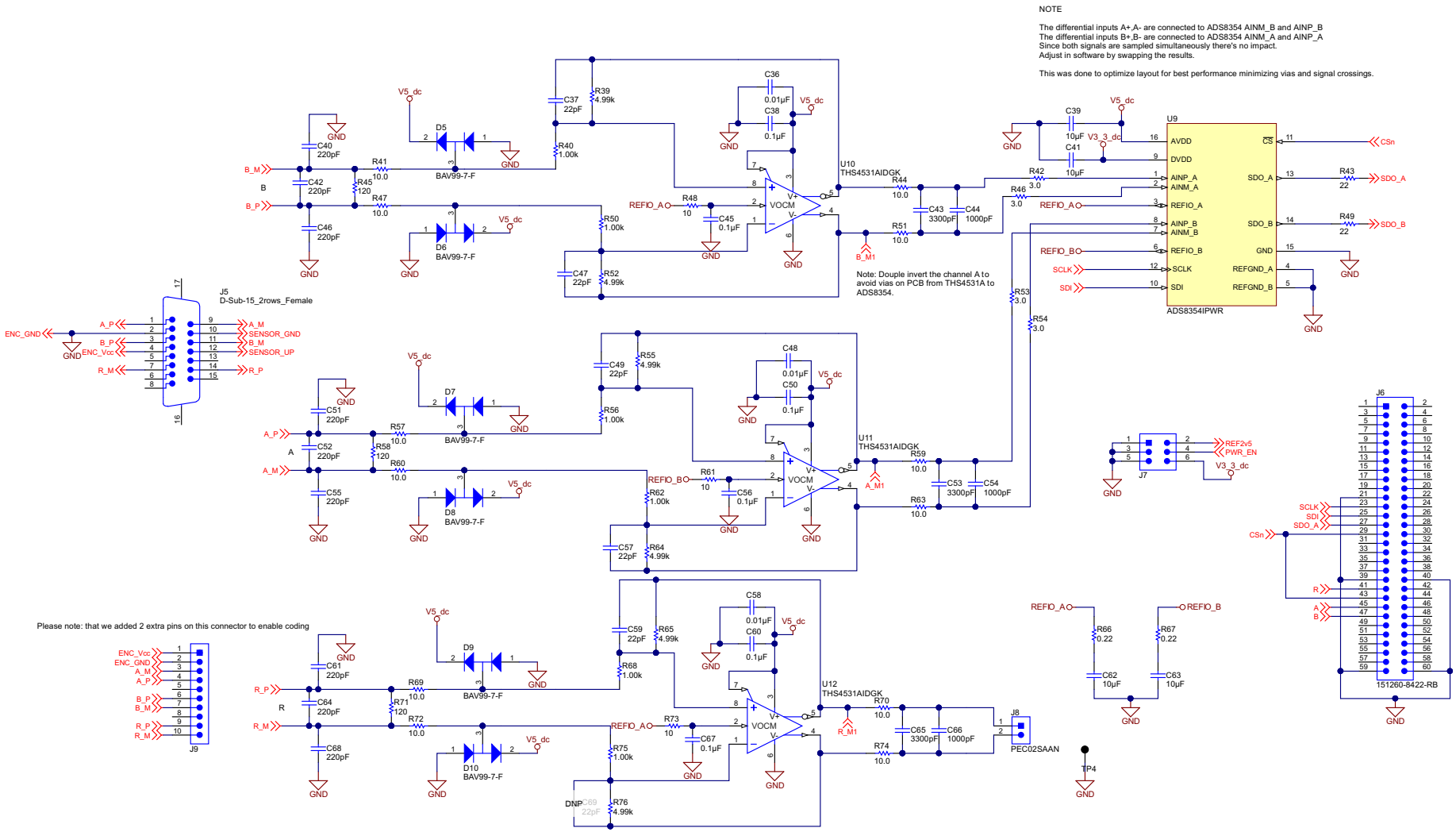

Figure 60. Schematic of High-Resolution Analog Path With 16-Bit ADC

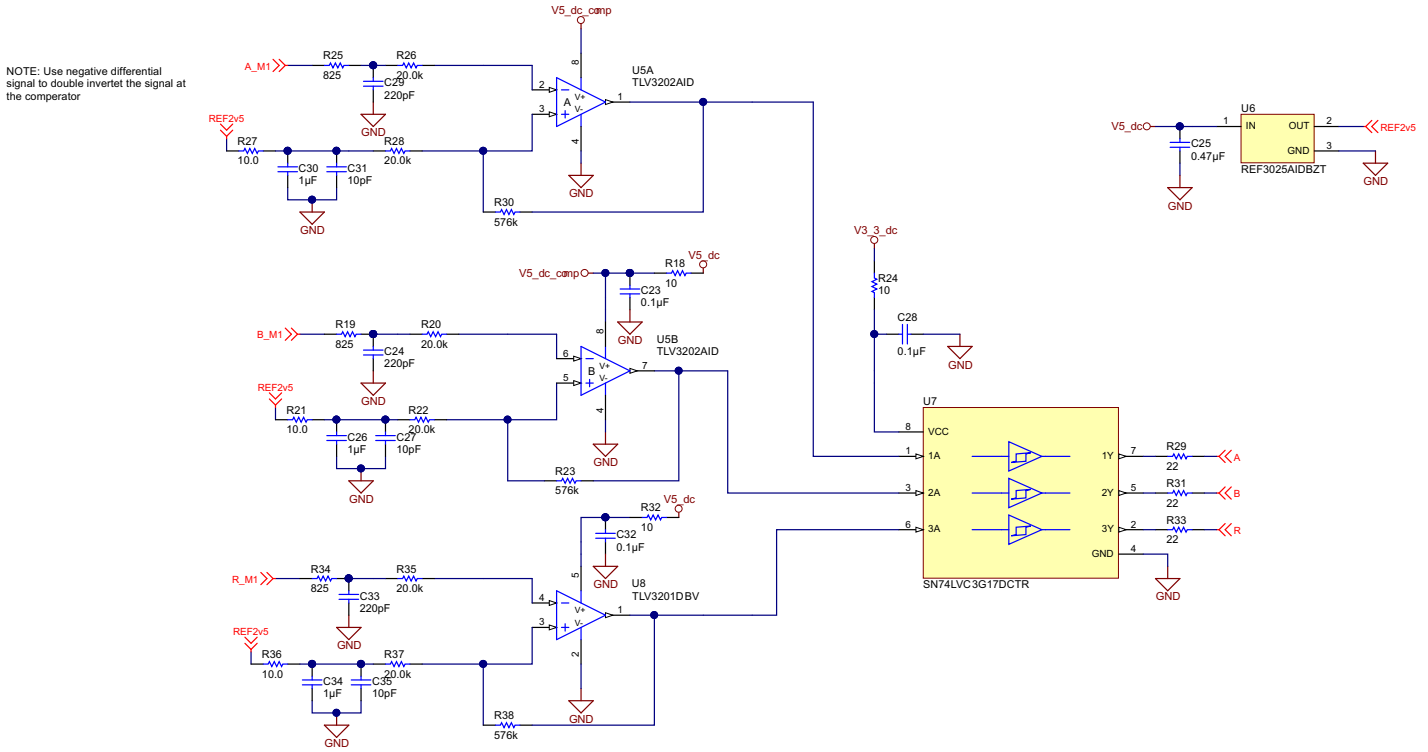

Figure 61. Schematic of Level Shifter and Comparators

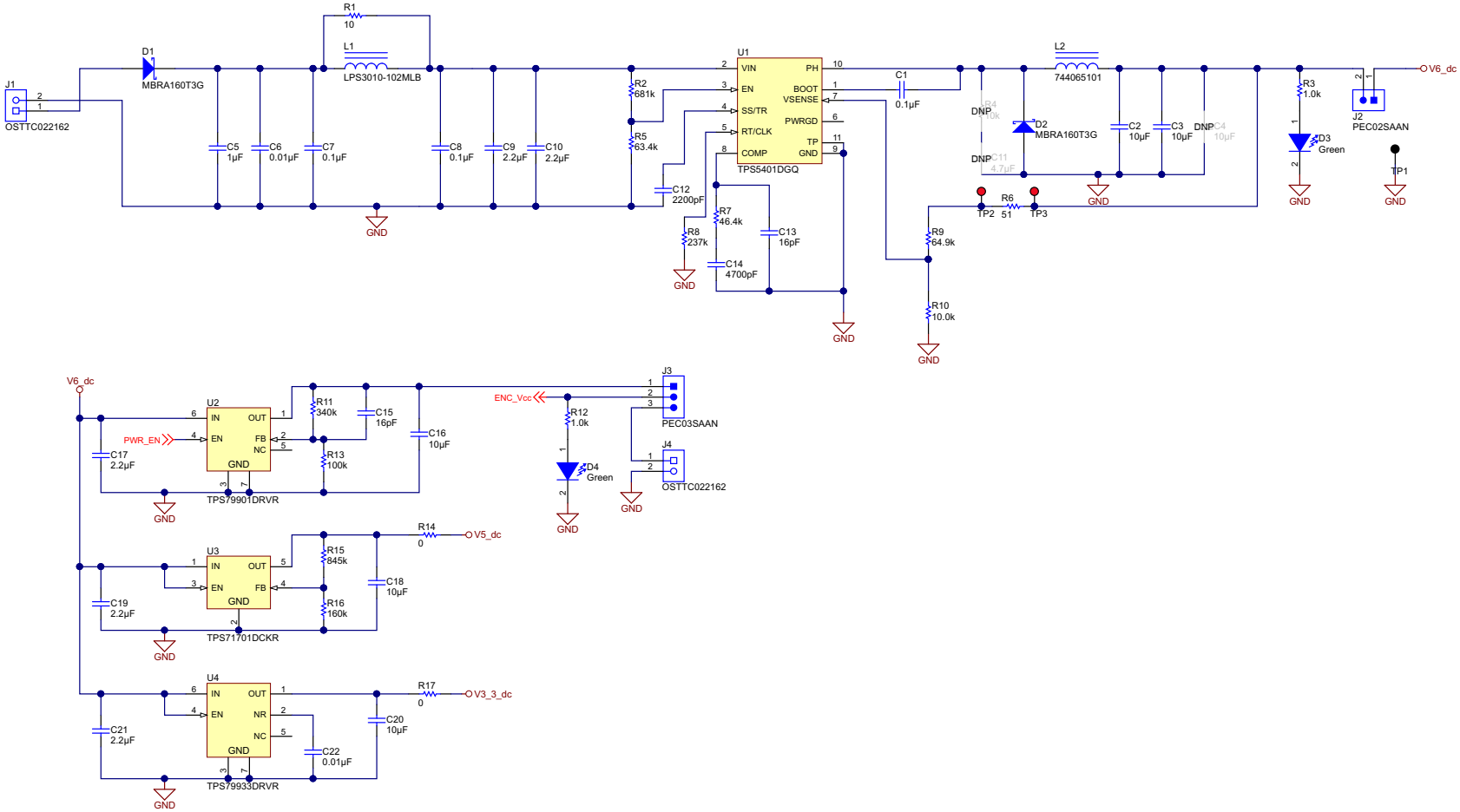

Figure 62. Schematic of Power Management

8.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00178.

Table 34. BOM

QTY	DESIGNATOR	DESCRIPTION	MANUFACTURER	PARTNUMBER	PACKAGE REFERENCE	FITTED
1	!PCB1	Printed Circuit Board	Any	TIDA-00178		Fitted
3	C1, C7, C8	CAP, CERM, 0.1 µF, 50 V, +/- 10%, X7R, 0603	MuRata	GRM188R71H104KA93D	0603	Fitted
2	C2, C3	CAP, CERM, 10 µF, 50 V, +/- 10%, X5R, 1206_190	TDK	CGA5L3X5R1H106K160AB	1206_190	Fitted
1	C5	CAP, CERM, 1 µF, 50 V, +/- 10%, X7R, 0805	MuRata	GRM21BR71H105KA12L	0805	Fitted
1	C6	CAP, CERM, 0.01 µF, 50 V, +/- 10%, X7R, 0805	MuRata	GRM216R71H103KA01D	0805	Fitted
2	C9, C10	CAP, CERM, 2.2uF, 50V, +/-10%, X5R, 1206	MuRata	GRM31CR61H225KA88L	1206	Fitted
1	C12	CAP, CERM, 2200 pF, 16 V, +/- 10%, X5R, 0402	MuRata	GRM155R61C222KA01D	0402	Fitted
2	C13, C15	CAP, CERM, 16 pF, 50 V, +/- 5%, C0G/NP0, 0402	MuRata	GRM1555C1H160JA01D	0402	Fitted
1	C14	CAP, CERM, 4700 pF, 16 V, +/- 10%, X7R, 0402	MuRata	GRM155R71C472KA01D	0402	Fitted
3	C16, C18, C20	CAP, CERM, 10 µF, 16 V, +/- 10%, X5R, 0805	MuRata	GRM219R61C106KA73D	0805	Fitted
3	C17, C19, C21	CAP, CERM, 2.2 µF, 16 V, +/- 10%, X5R, 0603	MuRata	GRM188R61C225KE15D	0603	Fitted
1	C22	CAP, CERM, 0.01 µF, 16 V, +/- 10%, X7R, 0603	MuRata	GRM188R71C103KA01D	0603	Fitted
6	C23, C28, C32, C38, C50, C60	CAP, CERM, 0.1 µF, 16 V, +/- 10%, X7R, 0603	MuRata	GRM188R71C104KA01D	0603	Fitted
12	C24, C29, C33, C40, C42, C46, C51, C52, C55, C61, C64, C68	CAP, CERM, 220 pF, 50 V, +/- 5%, C0G/NP0, 0402	MuRata	GRM1555C1H221JA01D	0402	Fitted
1	C25	CAP, CERM, 0.47 µF, 10 V, +/- 10%, X7R, 0603	Kemet	C0603C474K8RACTU	0603	Fitted
3	C26, C30, C34	CAP, CERM, 1 µF, 16 V, +/- 10%, X7R, 0603	MuRata	GRM188R71C105KA12D	0603	Fitted
3	C27, C31, C35	CAP, CERM, 10 pF, 50 V, +/- 5%, C0G/NP0, 0603	MuRata	GRM1885C1H100JA01D	0603	Fitted
3	C36, C48, C58	CAP, CERM, 0.01 µF, 16 V, +/- 10%, X7R, 0402	TDK	C1005X7R1C103K	0402	Fitted

Table 34. BOM (continued)

QTY	DESIGNATOR	DESCRIPTION	MANUFACTURER	PARTNUMBER	PACKAGE REFERENCE	FITTED
5	C37, C47, C49, C57, C59	CAP, CERM, 22 pF, 50 V, +/- 1%, C0G/NP0, 0402	MuRata	GRM1555C1H220FA01D	0402	Fitted
2	C39, C41	CAP, CERM, 10 µF, 16 V, +/- 10%, X7R, 0805_140	Samsung	CL21B106KOQNNNE	0805_140	Fitted
3	C43, C53, C65	CAP, CERM, 3300 pF, 50 V, +/- 5%, C0G/NP0, 0603	MuRata	GRM1885C1H332JA01D	0603	Fitted
3	C44, C54, C66	CAP, CERM, 1000 pF, 50 V, +/- 5%, C0G/NP0, 0402	MuRata	GRM1555C1H102JA01D	0402	Fitted
3	C45, C56, C67	CAP, CERM, 0.1 µF, 16 V, +/- 10%, X7R, 0402	MuRata	GRM155R71C104KA88D	0402	Fitted
2	C62, C63	CAP, CERM, 10 µF, 10 V, +/- 10%, X7R, 0805_140	MuRata	GRM21BR71A106KE51K	0805_140	Fitted
2	D1, D2	Diode, Schottky, 60V, 1A, SMA	ON Semiconductor	MBRA160T3G	SMA	Fitted
2	D3, D4	LED, Green, SMD	OSRAM	LG L29K-G2J1-24-Z	1.7x0.65x0.8mm	Fitted
6	D5, D6, D7, D8, D9, D10	Diode, Switching, 75 V, 0.3 A, SOT-23	Diodes Inc.	BAV99-7-F	SOT-23	Fitted
3	FID4, FID5, FID6	Fiducial mark. There is nothing to buy or mount.	N/A	N/A	Fiducial	Fitted
2	H1, H2	Machine Screw, Round, #4-40 x 1/4, Nylon, Philips panhead	B&F Fastener Supply	NY PMS 440 0025 PH	Screw	Fitted
2	H3, H4	Standoff, Hex, 0.5"L #4-40 Nylon	Keystone	1902C	Standoff	Fitted
2	J1, J4	Terminal Block, 2-pole, 200mil, TH	On-Shore Technology	OSTTC022162	THD, 2-Leads, Body 10.16x7.6mm, Pitch 5.08mm	Fitted
2	J2, J8	Header, 100mil, 2x1, Tin, TH	Sullins Connector Solutions	PEC02SAAN	Header, 2 PIN, 100mil, Tin	Fitted
1	J3	Header, 100mil, 3x1, Tin, TH	Sullins Connector Solutions	PEC03SAAN	Header, 3 PIN, 100mil, Tin	Fitted
1	J5	D-Sub-15, 17Pos, TH	Harting	09 66 252 6610	D-Sub-15, 2rows, Female, TH	Fitted
1	J6	Header, 2mm, 30x2, Gold, TH	3M	151260-8422-RB	Header, 30x2, 2mm, TH	Fitted
1	J7	Header, 100mil, 3x2, Tin, TH	Sullins Connector Solutions	PEC03DAAN	3x2 Header	Fitted
1	J9	Header, 100mil, 10x1, TH	Mill-Max	800-10-010-10-001000	Header, 10x1, 100mil, TH	Fitted
1	L1	Inductor, Shielded Drum Core, Ferrite, 1 µH, 1.5 A, 0.09 ohm, SMD	Coilcraft	LPS3010-102MLB	LPS3010	Fitted
1	L2	Inductor, Shielded Drum Core, Ferrite, 100 µH, 0.9 A, 0.33 ohm, SMD	Wurth Elektronik eiSos	744065101	WE-TPC-XLH2	Fitted
1	R1	RES, 10 ohm, 5%, 0.25W, 0603	Vishay-Dale	CRCW060310R0JNEAHP	0603	Fitted

Table 34. BOM (continued)

QTY	DESIGNATOR	DESCRIPTION	MANUFACTURER	PARTNUMBER	PACKAGE REFERENCE	FITTED
1	R2	RES, 681 k, 1%, 0.063 W, 0402	Vishay-Dale	CRCW0402681KFKED	0402	Fitted
2	R3, R12	RES, 1.0 k, 5%, 0.063 W, 0402	Vishay-Dale	CRCW04021K00JNED	0402	Fitted
1	R5	RES, 63.4 k, 1%, 0.063 W, 0402	Vishay-Dale	CRCW040263K4FKED	0402	Fitted
1	R6	RES, 51 ohm, 5%, 0.1W, 0603	Vishay-Dale	CRCW060351R0JNEA	0603	Fitted
1	R7	RES, 46.4 k, 1%, 0.063 W, 0402	Vishay-Dale	CRCW040246K4FKED	0402	Fitted
1	R8	RES, 237 k, 1%, 0.063 W, 0402	Vishay-Dale	CRCW0402237KFKED	0402	Fitted
1	R9	RES, 64.9 k, 1%, 0.063 W, 0402	Vishay-Dale	CRCW040264K9FKED	0402	Fitted
1	R10	RES, 10.0 k, 1%, 0.063 W, 0402	Vishay-Dale	CRCW040210K0FKED	0402	Fitted
1	R11	RES, 340 k, 1%, 0.063 W, 0402	Vishay-Dale	CRCW0402340KFKED	0402	Fitted
1	R13	RES, 100 k, 5%, 0.063 W, 0402	Vishay-Dale	CRCW0402100KJNED	0402	Fitted
2	R14, R17	RES, 0, 5%, 0.063 W, 0402	Vishay-Dale	CRCW04020000Z0ED	0402	Fitted
1	R15	RES, 845 k, 1%, 0.063 W, 0402	Vishay-Dale	CRCW0402845KFKED	0402	Fitted
1	R16	RES, 160 k, 5%, 0.063 W, 0402	Vishay-Dale	CRCW0402160KJNED	0402	Fitted
6	R18, R24, R32, R48, R61, R73	RES, 10, 5%, 0.063 W, 0402	Vishay-Dale	CRCW040210R0JNED	0402	Fitted
3	R19, R25, R34	RES, 825, 1%, 0.063 W, 0402	Vishay-Dale	CRCW0402825RFKED	0402	Fitted
2	R20, R26	RES, 20.0 k, 1%, 0.1 W, 0603	Yageo America	RC0603FR-0720KL	0603	Fitted
15	R21, R27, R36, R41, R44, R47, R51, R57, R59, R60, R63, R69, R70, R72, R74	RES, 10.0, 1%, 0.063 W, 0402	Vishay-Dale	CRCW040210R0FKED	0402	Fitted
4	R22, R28, R35, R37	RES, 20.0 k, 1%, 0.063 W, 0402	Vishay-Dale	CRCW040220K0FKED	0402	Fitted
3	R23, R30, R38	RES, 576 k, 1%, 0.063 W, 0402	Vishay-Dale	CRCW0402576KFKED	0402	Fitted
3	R29, R31, R33	RES, 22, 5%, 0.1 W, 0603	Vishay-Dale	CRCW060322R0JNEA	0603	Fitted
6	R39, R52, R55, R64, R65, R76	RES, 4.99 k, 0.1%, 0.063 W, 0402	Panasonic	ERA-2AEB4991X	0402	Fitted
6	R40, R50, R56, R62, R68, R75	RES, 1.00 k, 0.1%, 0.063 W, 0402	Panasonic	ERA-2AEB102X	0402	Fitted
4	R42, R46, R53, R54	RES, 3.0, 5%, 0.063 W, 0402	Vishay-Dale	CRCW04023R00JNED	0402	Fitted
2	R43, R49	RES, 22, 5%, 0.063 W, 0402	Vishay-Dale	CRCW040222R0JNED	0402	Fitted
3	R45, R58, R71	RES, 120, 1%, 0.4 W, 0805	Rohm	ESR10EZPF1200	0805	Fitted
2	R66, R67	RES, 0.22, 1%, 0.1 W, 0603	Panasonic	ERJ-3RQFR22V	0603	Fitted
2	TP1, TP4	Test Point, Miniature, Black, TH	Keystone	5001	Black Miniature Testpoint	Fitted
2	TP2, TP3	Test Point, Miniature, Red, TH	Keystone	5000	Red Miniature Testpoint	Fitted

Table 34. BOM (continued)

QTY	DESIGNATOR	DESCRIPTION	MANUFACTURER	PARTNUMBER	PACKAGE REFERENCE	FITTED
1	U1	Buck Step Down Regulator with 3.5 to 42 V Input and 0.8 to 39 V Output, -40 to 150 degC, 10-Pin MSOP-PowerPAD (DGQ), Green (RoHS & no Sb/Br)	Texas Instruments	TPS5401DGQ	DGQ0010D	Fitted
1	U2	Single Output High PSRR LDO, 200 mA, Adjustable 1.2 to 6.5 V Output, 2.7 to 6.5 V Input, with Low IQ, 6-pin SON (DRV), -40 to 85 degC, Green (RoHS & no Sb/Br)	Texas Instruments	TPS79901DRVR	DRV0006A	Fitted
1	U3	Single Output LDO, 150 mA, Adjustable 0.9 to 6.2 V Output, 2.5 to 6.5 V Input, with High-Bandwidth PSRR, 5-pin SC70 (DCK), -40 to 125 degC, Green (RoHS & no Sb/Br)	Texas Instruments	TPS71701DCKR	DCK0005A	Fitted
1	U4	Single Output High PSRR LDO, 200 mA, Fixed 3.3 V Output, 2.7 to 6.5 V Input, with Low IQ, 6-pin SON (DRV), -40 to 85 degC, Green (RoHS & no Sb/Br)	Texas Instruments	TPS79933DRVR	DRV0006A	Fitted
1	U5	40-ns, microPOWER, Push-Pull Output Comparators, D0008A	Texas Instruments	TLV3202AID	D0008A	Fitted
1	U6	2.5 V, 50 ppm / degC, 50 uA Series (Bandgap) Voltage Reference, -40 to 125 degC, 3-pin SOT-23 (DBZ), Green (RoHS & no Sb/Br)	Texas Instruments	REF3025AIDBZT	DBZ0003A	Fitted
1	U7	Triple Schmitt-Trigger Buffer, DCT0008A	Texas Instruments	SN74LVC3G17DCTR	DCT0008A	Fitted
1	U8	40-ns, microPOWER, Push-Pull Output Comparators, DBV0005A	Texas Instruments	TLV3201DBV	DBV0005A	Fitted
1	U9	Dual, High-Speed, 16-, 14-, and 12-Bit, Simultaneous-Sampling, Analog-to-Digital Converters, PW0016A	Texas Instruments	ADS8354IPWR	PW0016A	Fitted
3	U10, U11, U12	Ultra Low Power, Rail-to-Rail Output, Fully-Differential Amplifier, DGK0008A	Texas Instruments	THS4531AIDGK	DGK0008A	Fitted
0	C4	CAP, CERM, 10 µF, 50 V, +/- 10%, X5R, 1206_190	TDK	CGA5L3X5R1H106K160AB	1206_190	Not Fitted
0	C11	CAP, CERM, 4.7 µF, 50 V, +/- 10%, X5R, 0805	TDK	C2012X5R1H475K125AB	0805	Not Fitted
0	C69	CAP, CERM, 22 pF, 50 V, +/- 1%, C0G/NP0, 0402	MuRata	GRM1555C1H220FA01D	0402	Not Fitted

Table 34. BOM (continued)

QTY	DESIGNATOR	DESCRIPTION	MANUFACTURER	PARTNUMBER	PACKAGE REFERENCE	FITTED
0	FID1, FID2, FID3	Fiducial mark. There is nothing to buy or mount.	N/A	N/A	Fiducial	Not Fitted
0	R4	RES, 10k ohm, 5%, 0.125W, 0805	Vishay-Dale	CRCW080510K0JNEA	0805	Not Fitted

8.3 PCB Layout Guidelines

The following figures provide layout guidelines specific to the TIDA-00178 design.

Because of the sensitivity of the analog signal conditioning parts, the design of a four-layer PCB with at least one complete ground plane is highly recommended, this will improve the noise immunity of the system.

Particular attention is also necessary when routing the two sine/cosine signals (to avoid cross-talk problems and interferences); also the power management section (the switcher TPS5401, in particular) should be properly routed and well separated from the sensitive part of the board to avoid the latter catching noise from the switcher.

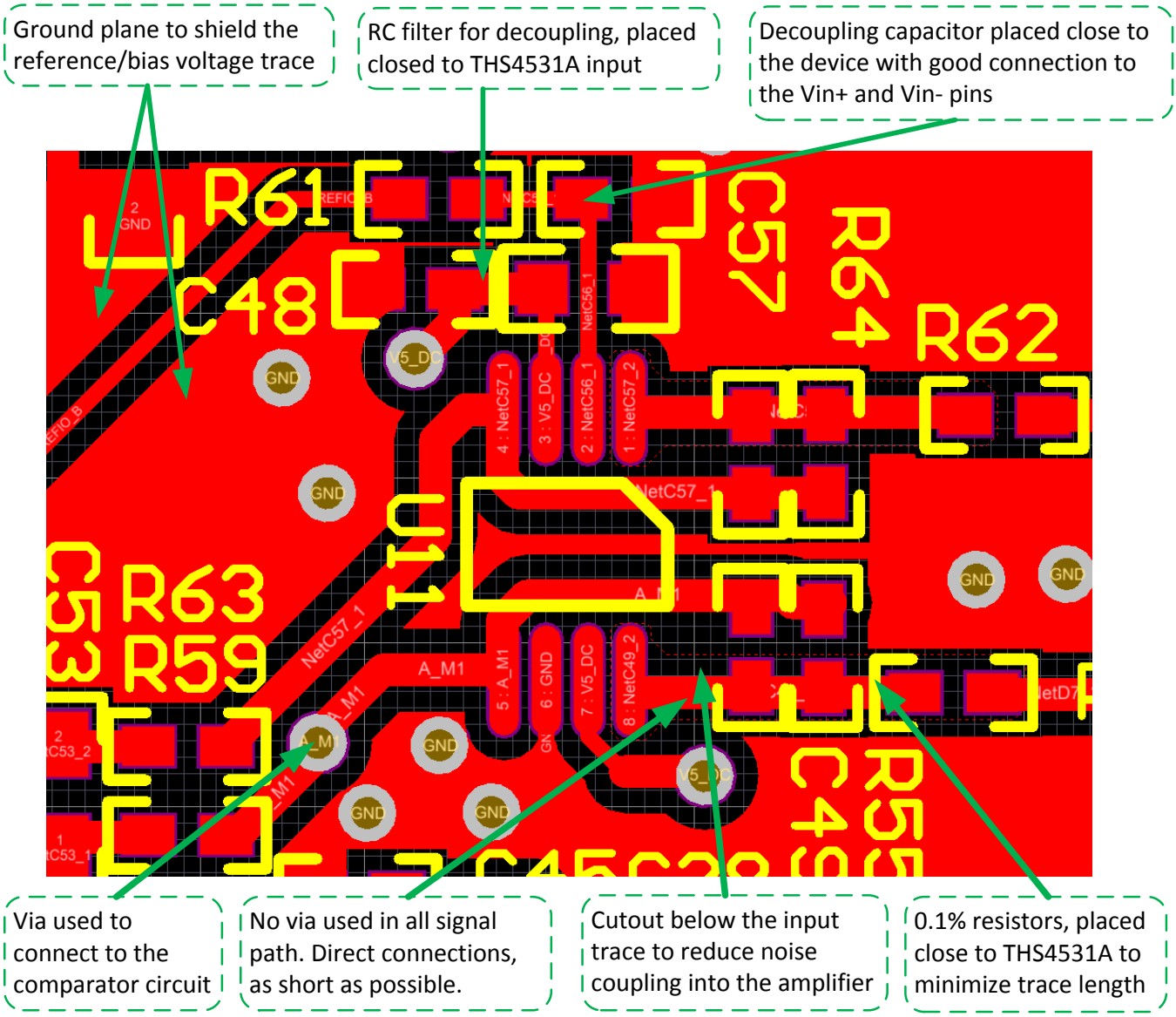

Figure 63. THS4531A Layout

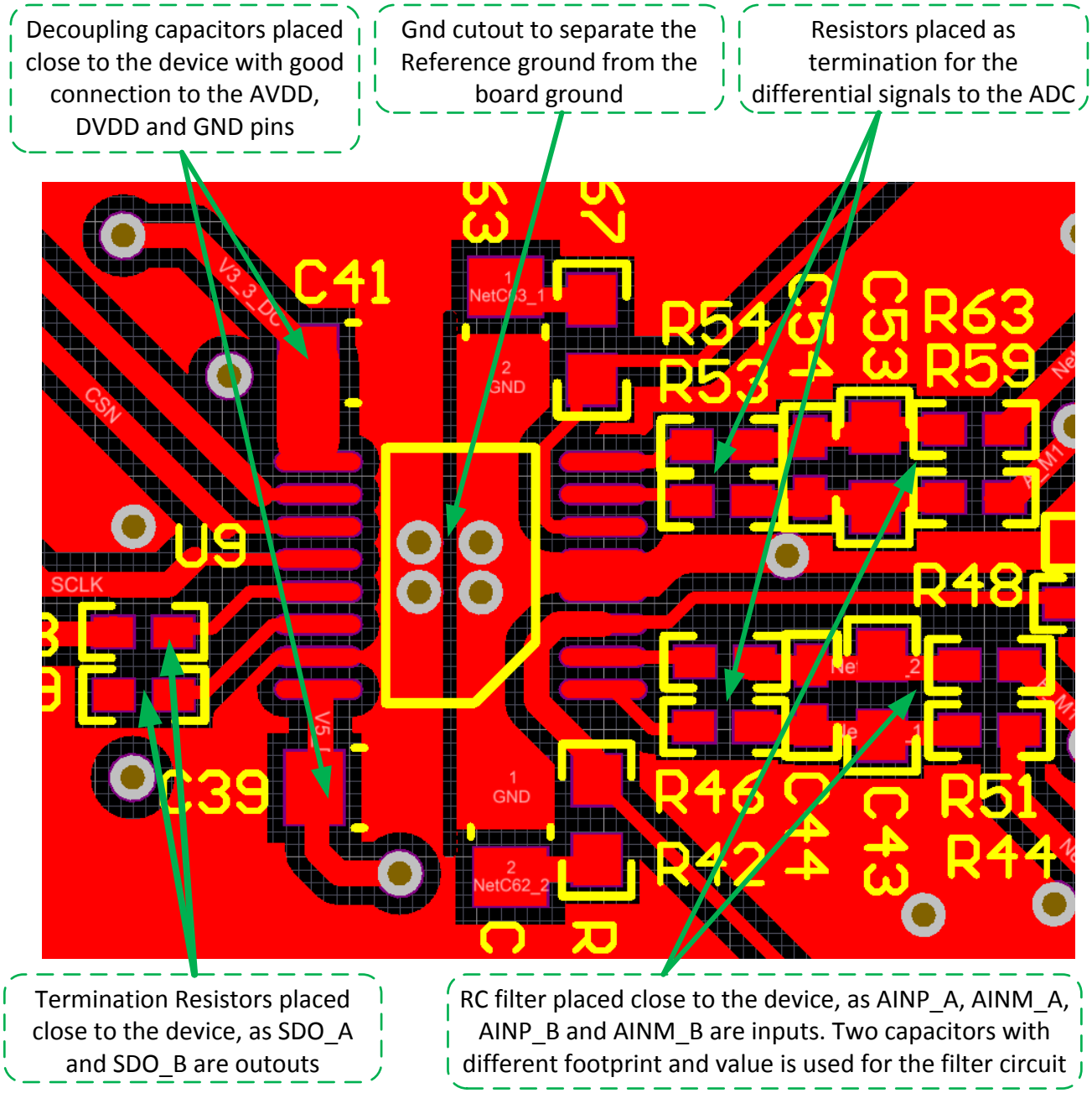

Figure 64. ADS8354, 16-Bit ADC Layout

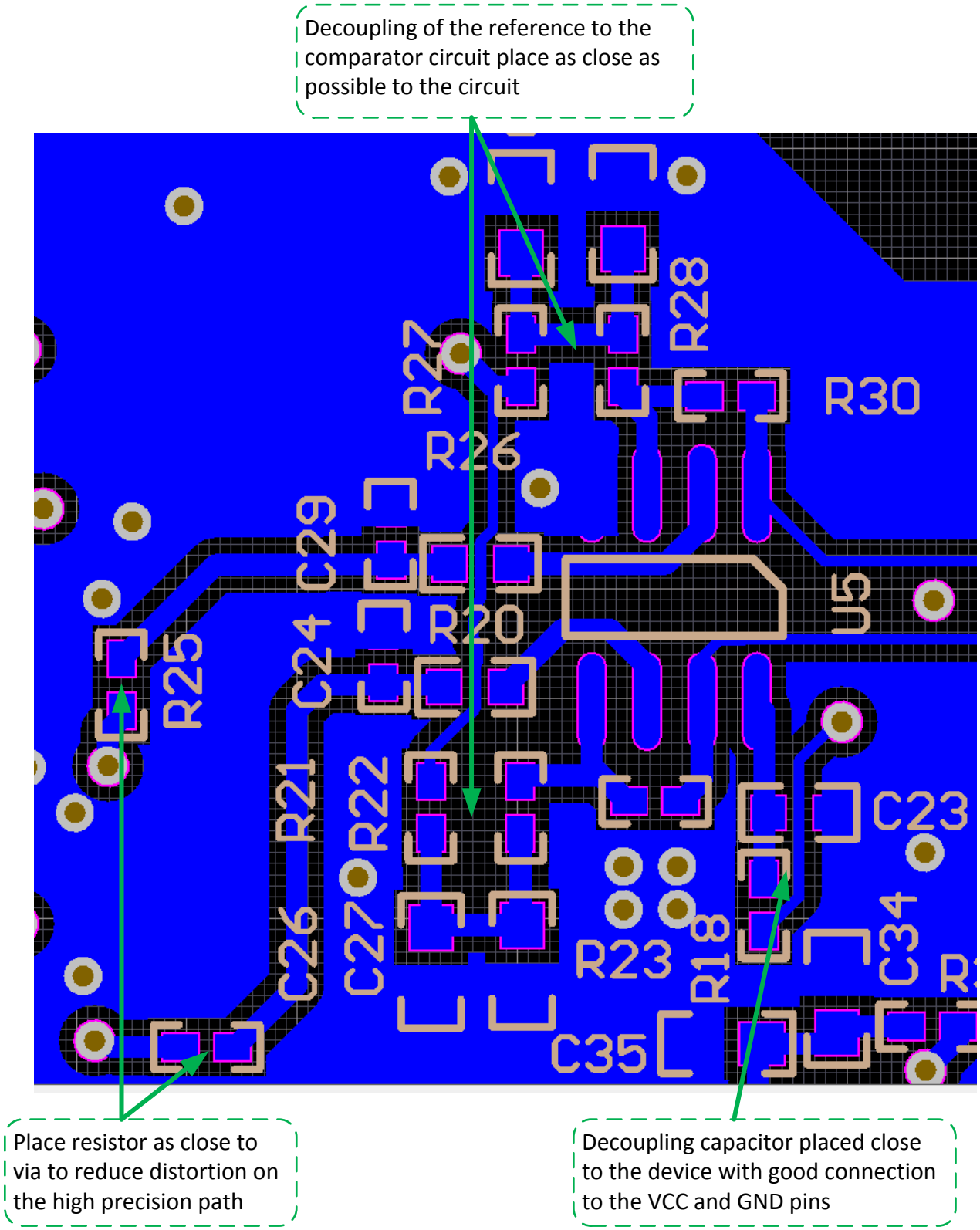

Figure 65. TLV3202 Layout

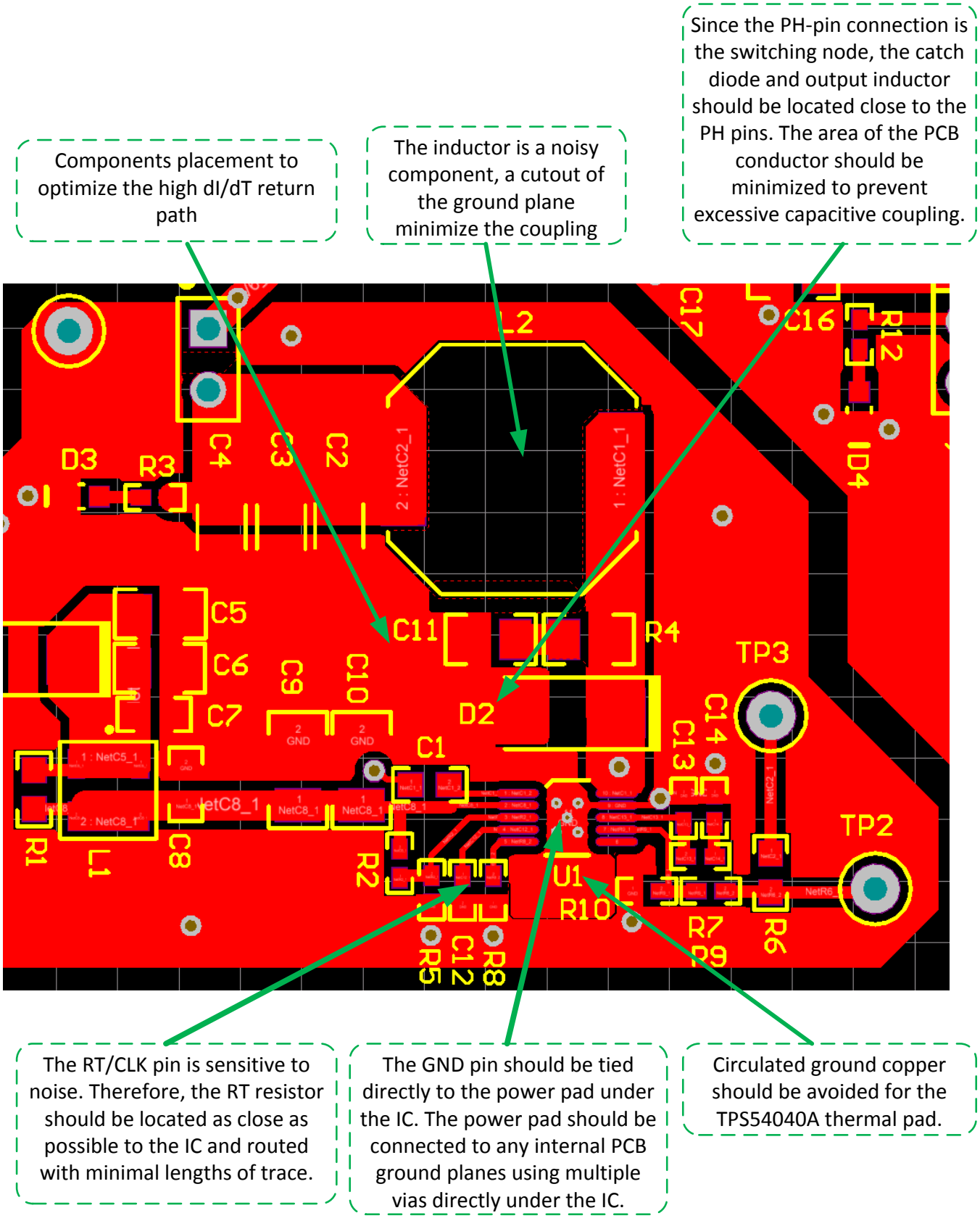

Figure 66. TPS5401 Layout

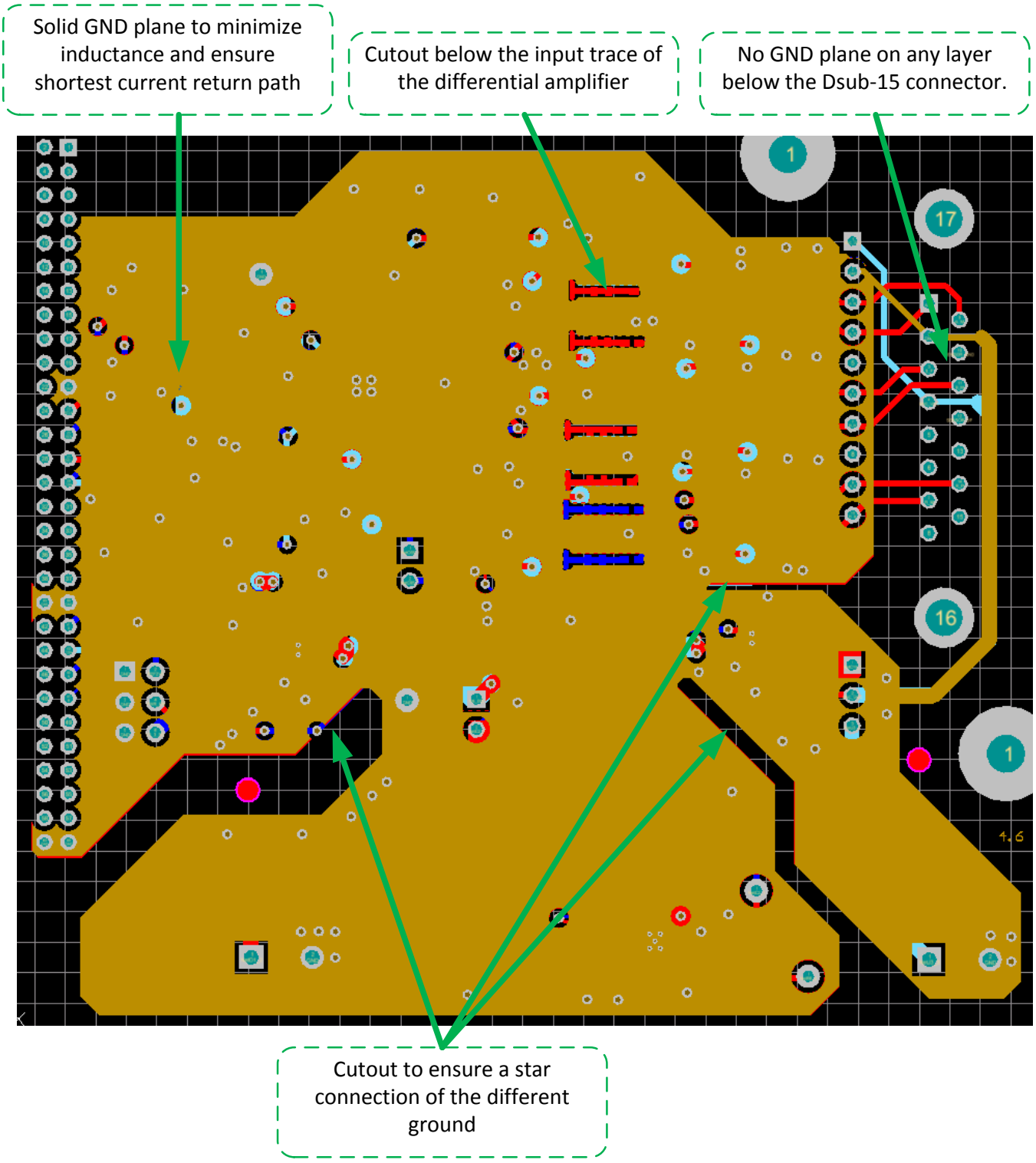

Figure 67. GND Layer

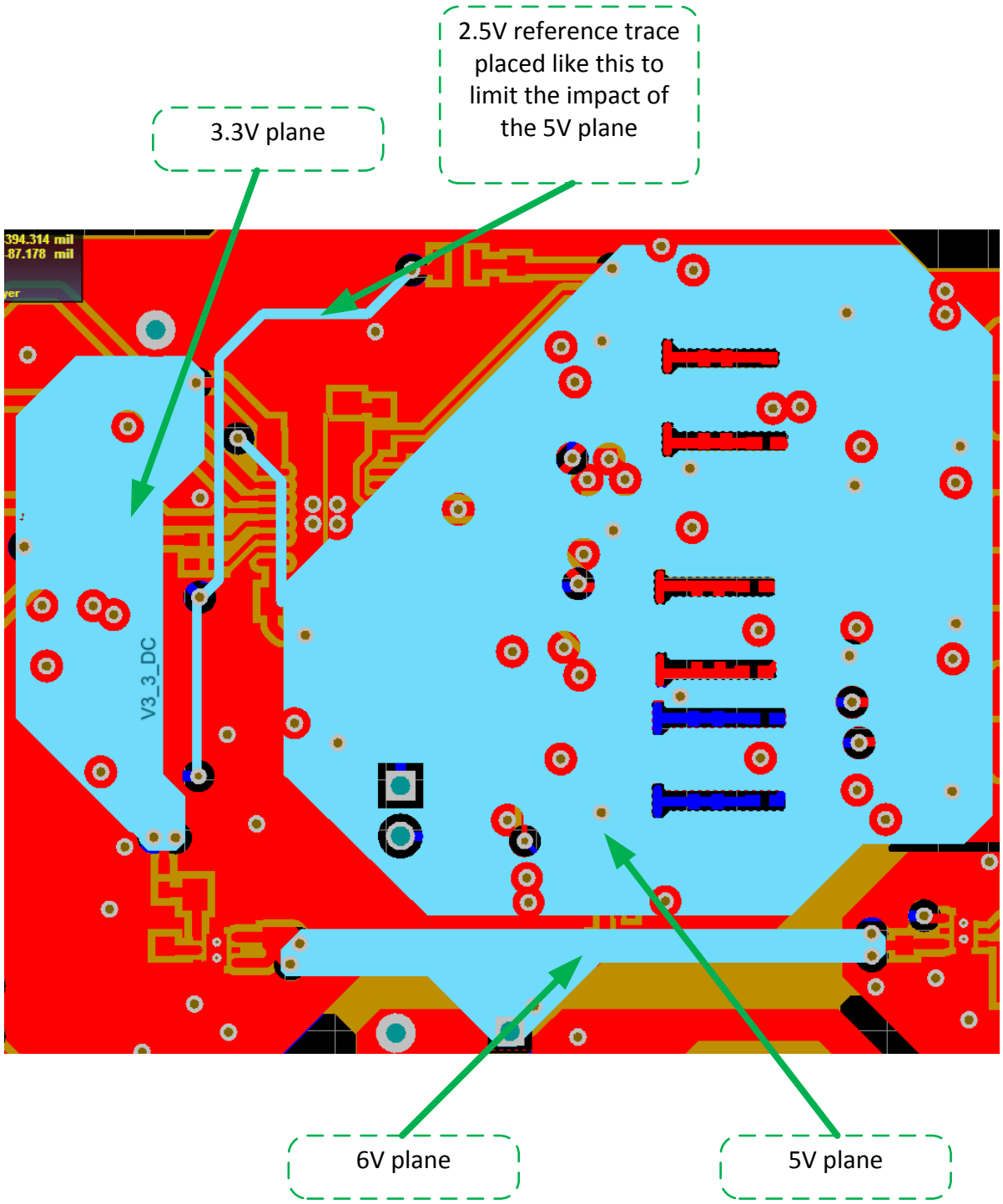

Figure 68. Supply Layer

8.3.1 Layer Plots

To download the layer plots, see the design files at TIDA-00178.

8.4 Altium Project

To download the Altium project files, see the design files at TIDA-00178.

8.5 Gerber Files

To download the Gerber files, see the design files at TIDA-00178.

8.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-00178.

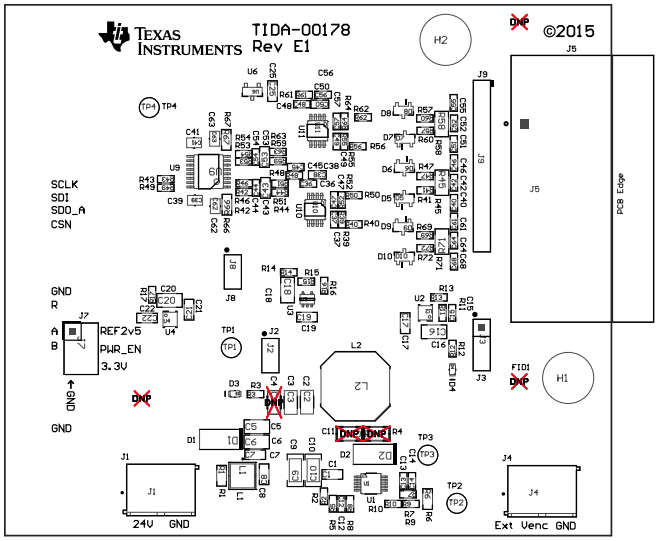

Figure 69. Top Assembly Drawing

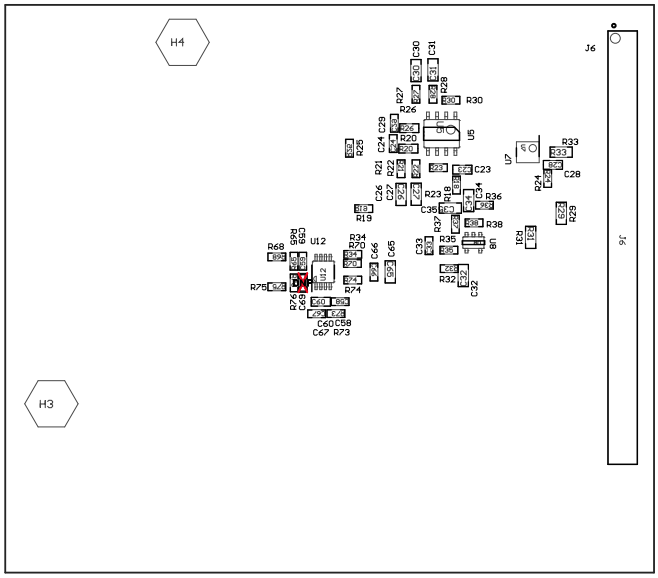

Figure 70. Bottom Assembly Drawing

8.7 Software Files

To download the software files, see the design files at TIDA-00178.

9 References

1. Texas Instruments, *18-Bit, 1MSPS Data Acquisition Block (DAQ) Optimized for Lowest Distortion and Noise*, TIPD115 Verified Design Reference Guide (SLAU515).
2. Texas Instruments, *AN-2162 Simple Success With Conducted EMI From DC-DC Converters*, (SNVA489).
3. Texas Instruments, *TMS320F240 DSP-Solution for High-Resolution Position with Sin/Cos-Encoders*, TMS320F240 Application Report (SPRA496).
4. IEC 61800-3 ed2.0 (2004-08), *Adjustable speed electrical power drive systems - Part 3: EMC requirements and specific test methods*, [IEC 61800-3 ed2.0 (2004-08)].
5. IEC 61800-3-am1 ed2.0 (2011-11), *Amendment 1 - Adjustable speed electrical power drive systems - Part 3: EMC requirements and specific test methods*, [IEC 61800-3-am1 ed2.0 (2011-11)].
6. Heidenhain, *Interfaces of HEIDENHAIN Encoders*, March 2015, Brochure #1078628-21 (www.heidenhain.com).
7. Heidenhain, *Rotary Encoders*, November 2014, Brochure #349529-2E (www.heidenhain.com).

10 About the Authors

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Revision History

Changes from Original (June 2015) to A Revision	Page
• Changed from preview page	1

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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