TI Designs

Isolated Current and Voltage Measurement Using Fully Differential Isolation Amplifier

Design Overview

This TI design demonstrates using the AMC1100-based AFE to measure voltage and current. This design details measuring voltage inputs in an input- to-output isolation configuration and measuring current inputs in a channel-to-channel isolation configuration. This design also demonstrates power isolation, which makes the design a complete subsystem to measure isolated voltages and currents. This AFE can be used in applications that require replacing CTs with shunts. Shunts and potential dividers are available onboard to directly connect current and voltage inputs. The AMC1100 isolation amplifiers have a low nonlinearity error and an accuracy of < 0.5%.

Design Resources

TIDA-00555	Tool Folder Containing Design Files
AMC1100	Product Folder
SN6501	Product Folder
TLV704	Product Folder
TPS7A30	Product Folder
TPS7A6533-Q1	Product Folder
CSD17571Q2	Product Folder
ADS131E08EVM-PDK	Tool Folder
MSP430FR5869	Product Folder

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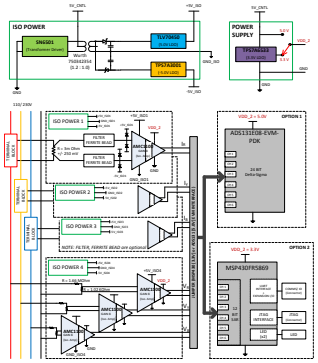
Design Features

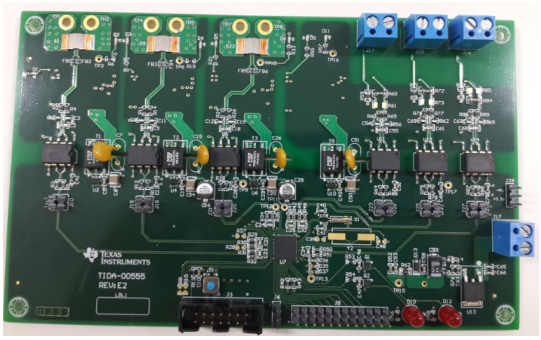
Voltage and Current Measurement Using:

- Channel-Isolated Current Inputs and Group Isolated Voltage Inputs Based on AMC1100 Fixed-Gain, Fully Differential Amplifiers
- Provision to Interface to ADS131E08 ADC, Multi-Channel Simultaneous Sampling, 24-Bit, Delta-Sigma (ΔΣ), and EVM for Performance Testing
- Onboard Shunt for Three Current Inputs and Potential Dividers for Three Voltage Inputs
- Low-Side Supply Configurable to 3.3 V or 5 V
- Accuracy Performance Over Full-Scale Input (175-mV RMS) for Current and Voltage < ±0.5% for 5% to 100%
- Isolated Power Supply Generated Using SN6501 Transformer Driver
- Can Be Interfaced to MCU With AMC1100 Low-Side Supply Configured to 3.3 V

Featured Applications

- Portable and Advanced Power Quality Analyzer
- Protection Relays, IEDs, and Fault Recorders





1 System Description

Grid infrastructure applications include protection, control, and monitoring systems. Some of the grid infrastructure end applications are multifunction protection relays, transformer and motor monitoring systems, power quality analyzers, and many others. These systems can be rack-mounted (AC mains operated) or portable (battery operated). The portable systems have requirements for separate (individual) and fully galvanically-isolated channels to measure the AC-DC voltage and current inputs.

Protection relays are intelligent electronic devices (IEDs) that receive analog signals from the secondary side of current transformers (CTs) and voltage transformers (VTs). The relays detect whether or not the protected unit is in a stressed condition. A trip signal is sent by protective relays to the circuit breakers to disconnect the faulty components from the power system, if necessary. Protective relays are categorized based on the equipment type protected, such as generators, transmission lines, transformers, and loads.

A protection relay has the following functional blocks:

- CPU
- Digital signal processor (DSP) for processing analog input from CT or VT
- Digital I/O
- DC analog I/O
- Power supply
- Communications

The analog input requirements include the following:

- Current and voltage inputs
  - Secondary of CT, secondary of potential divider
- Number of current and voltage channels for protection relays
  - 4 to 16 channels
- Measurement accuracy
  - 0.2% to 1%

Accurately measuring current and voltage is a critical requirement for the function of a protection relay.

The voltage is measured using a potential transformer or potential divider (multiple series resistors in a divider). Using a potential divider reduces the board size and improves linearity performance in comparison to a potential transformer. The potential divider-based voltage measurement is limited in that it does not provide the isolation that potential transformers provide. Voltage isolation is required for systems that are expected to conform to safety standards.

Current transformers are commonly used to measure current. The current input has a wide dynamic range in comparison to the voltage inputs. The system performance depends on the type of current transformers used.

Some of the key current sensor requirements are:

- Measurement accuracy—from DC to 400 Hz
- Drift with time, frequency, and temperature
- Linearity and phase shift
- Saturation
- Reliability
- Cost
- Size
- Safety (isolation) and electromagnetic compatibility (EMC) performance

To achieve the required performance standards listed above, select CTs with a higher level of accuracy.

Some advantages of using CTs are that they provide galvanic isolation, have low power loss, and are not affected by common-mode noise input. Some of the associated disadvantages of using CTs is that they tend to be bulky and expensive if the user requires a higher level accuracy. These bulky-sized CTs are disadvantageous to multifunction protection relay platforms, which are required to measure more channels. External magnetic fields also affect the performance of CTs because they saturate the CTs during fault conditions, when high currents flow. Continuous exposure to a magnetic field or frequent exposure to overloads reduces the usable life of the CTs. An alternative to using CTs to measure current is using shunts. Shunts are low-value metal strips made with Manganin® alloys. The shunt performance follows most of the previously mentioned requirements. Shunts do have limitations in that they do not have isolation, which is required for use in three-phase applications.

1.1 Isolation Methods

The following options detail the different isolation methods available:

Input-to-output isolation: In this case, all channels are referenced to the same ground. The isolation amplifiers require power supplies on both sides of the isolation barrier.

Channel-to-channel isolation: In this case, each input channel is referenced to the ground separately. The isolation amplifiers require separate power supplies on the input side of the isolation barrier and can share a common power supply on the output side.

1.2 Input Configurations

The inputs can be applied in the following configurations:

Single-ended:

The lowest cost configuration is a single-ended, unbalanced, grounded input. This input works well with a floating source that has relatively low differential impedance. The IN+ terminal impedance to ground must be high in comparison to the source differential impedance to avoid loading. For ground-referenced sources, this type of input implies that the signal and instrument grounds must be identical. The two voltages are typically not the same, but if the levels are close to each other and the signal is relatively large, the user can make the measurement.

Differential:

Differential input amplifiers are most commonly used in measurement systems because they provide a high gain for the algebraic difference between their two input signals or voltages, but a low gain for the voltages common to both inputs. Making differential voltage measurements is another means of reducing noise in analog input signals. A differential input is balanced because the gains and impedances of the two inputs are the same. Neither input is directly connected to ground, so a differential input can deal with single-ended-grounded or off-ground differential sources. Nevertheless, there is a limit to the maximum signal that each input can handle because the amplifiers are referenced to ground.

1.3 TI Design Advantages

1.3.1 Voltage Measurement Input-to-Output Isolation

The voltage inputs are attenuated by the onboard potential dividers and these inputs demonstrate the following in Table 1:

Table 1. Voltage Measurement

PARAMETERS	DESCRIPTION
Voltage inputs providing input-to-output isolation	Three fully-differential isolation amplifiers are used to measure the three-phase voltage inputs.
Power supply for providing input-to-output isolation	One DC-DC converter is used to generate the isolated power supply. The same power supply is connected to all three isolation amplifiers on the high-voltage side.
Ground reference	This is a group isolated reference, which means that all of the amplifiers share a common ground reference.

1.3.2 Channel-to-Channel Isolation

The current inputs are applied across the onboard shunt and demonstrates the following in Table 2:

Table 2. Current Measurement

PARAMETERS	DESCRIPTION
Current inputs providing channel-to-channel isolation	Three fully-differential isolation amplifiers are used to measure the three-phase current inputs.
Power supply for providing channel-to-channel isolation	Three separate DC-DC converters are used to generate the high-voltage side power supplies.
Ground reference	Each current input has its own reference. Each reference is isolated from all other circuits.

1.3.3 ADC Interface

The following list details the steps for interfacing the isolation amplifier to the ADC:

(A) Isolation amplifier of the common-mode DC output: The user can configure the isolation amplifier for a 1.3-V or 2.5-V DC common-mode output with the 3-V or 5-V low-side supply (output side).

(B) Interface to delta-sigma ADC ADS131E08: A provision to interface the amplifier output to a TI delta-sigma modulator is available. When using the ADS131E08 device the common-mode voltage is configured to 2.5 V.

(C) Interface to MCU: An onboard MCU with a 12-bit differential input has been provided. When using the MCU, the common-mode voltage is configured to 1.29 V.

2 Key System Specifications

Table 3. Design Requirements

SERIAL NUMBER	PARAMETERS	SPECIFICATIONS
1	Isolated current inputs (with onboard shunt)	Three
2	Isolated voltage inputs (with onboard potential divider)	Three
3	Measurement frequency	DC, 50 Hz, 60 Hz
4	Current measurement accuracy	< ±0.5%, for 5% to 100% of AMC1100 input full scale
5	Voltage measurement accuracy	< ±0.5%, for 5% to 100% of AMC1100 input full scale
6	Amplifier output interface – Option 1 (with output common-mode voltage set to 2.55 V, typical)	Interfaced to ADS131E08
7	Amplifier output interface – Option 2 (with output common-mode voltage set to 1.29 V, typical)	MSP430FR5869
8	DC power supply input	5-V DC
9	Power supply	Isolated 5 V and –5 V, non-isolated 3.3 V
10	Selectable output signal common-mode voltage	Option to select 5-V ADC or 3.3-V low-side power supply

3 Block Diagram

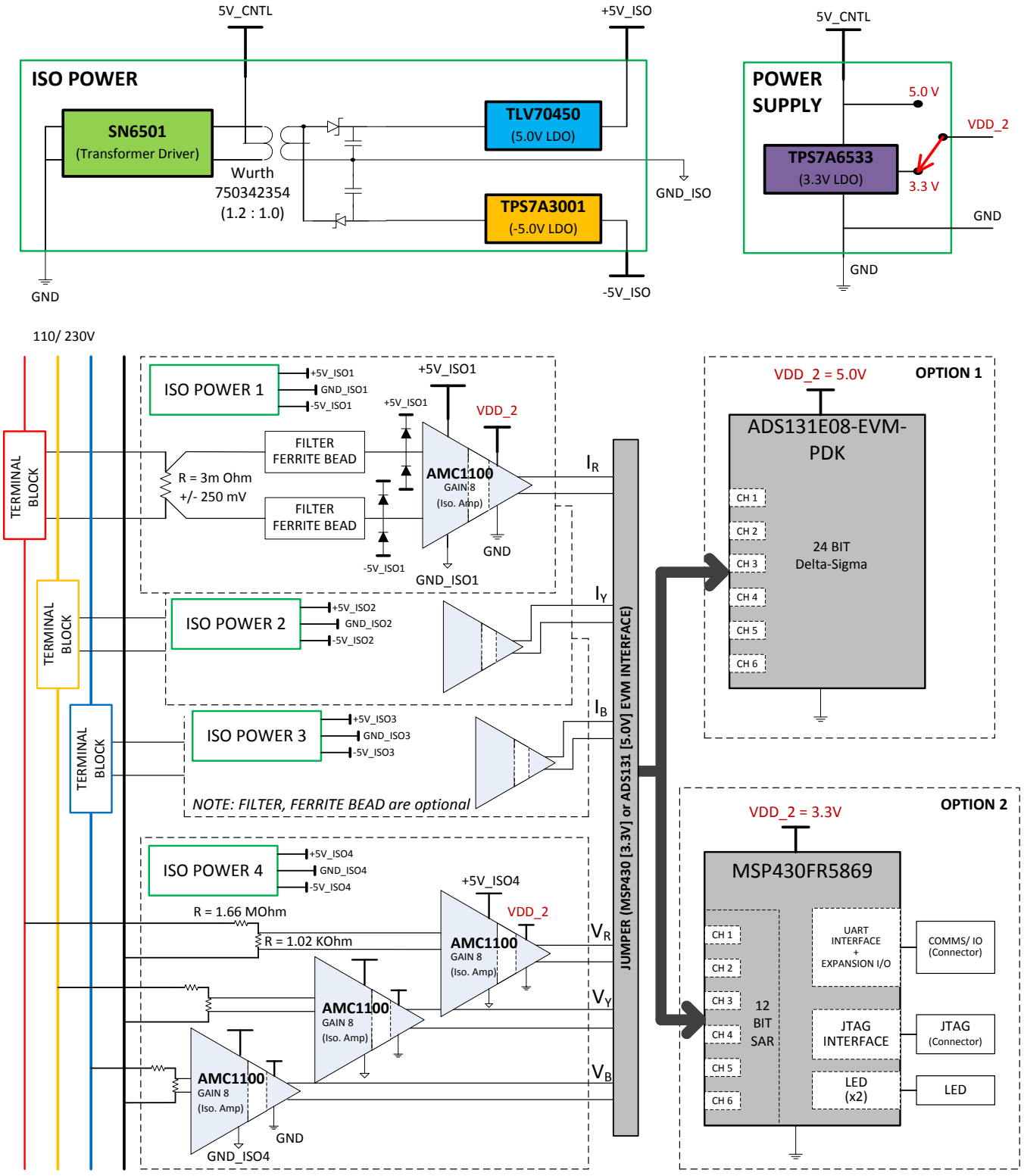


Figure 1. TIDA-00555 Functional Block Diagram

3.1 Highlighted Products

3.1.1 AMC1100—Fully Differential Isolation Amplifier

The AMC1100 is a precision isolation amplifier with an output separated from the input circuitry by a silicon dioxide (SiO2) barrier that is highly resistant to magnetic interference. This barrier is certified to provide galvanic isolation of up to 4250 V_{PEAK}, according to UL1577 and the IEC60747-5-2 standard. When used in conjunction with isolated power supplies, this device prevents noise currents on a high common-mode voltage line from entering the local ground and interfering with or damaging sensitive circuitry.

The AMC1100 input is optimized for direct connection to shunt resistors or other low voltage level signal sources. The excellent performance of the device enables accurate current and voltage measurement in energy-metering applications. The output signal common-mode voltage is automatically adjusted to either the 3.3-V or 5-V low-side supply.

The AMC1100 is fully specified over the extended industrial temperature range of –40°C to +105°C. The gullwing-8 (DUB) package part is used in this design. The following Figure 2 shows the AMC1100 functional block diagram.

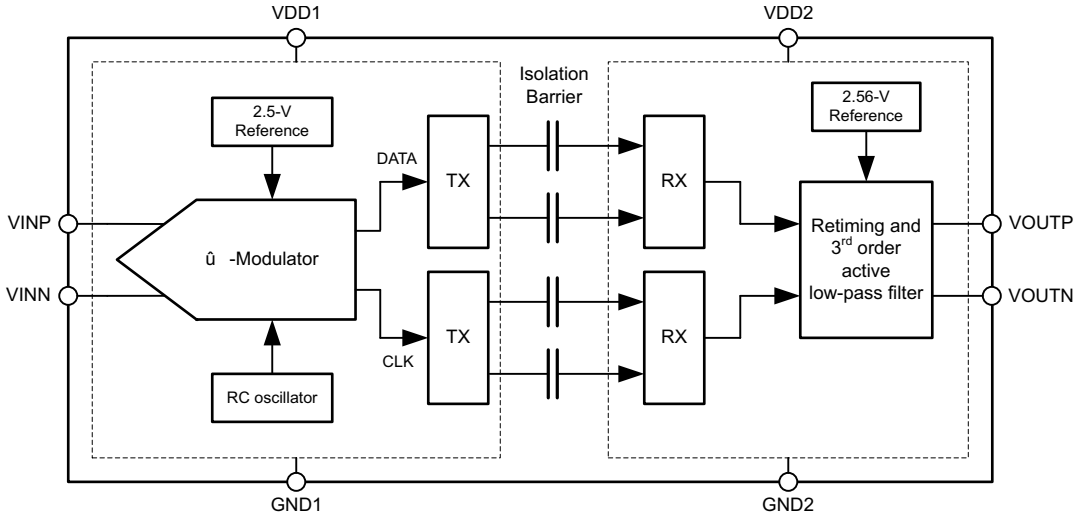


Figure 2. AMC1100 Functional Block Diagram

Key features:

- ±250-mV input voltage range optimized for shunt resistors
- Very low nonlinearity: 0.075% max at 5 V
- Low offset error: 1.5 mV max
- Low noise: 3.1 mV_{RMS} typical
- Low high-side Supply Current: 8 mA max at 5 V
- Input bandwidth: 60 KHz min
- Fixed gain: 8 (0.5% accuracy)
- High common-mode rejection ratio: 108 dB
- Low-side operation: 3.3 V or 5 V

3.1.2 SN6501—Transformer Driver

The SN6501 is a monolithic oscillator and power-driver, which is specifically designed for small-form factor, isolated power supplies in isolated interface applications. The device drives a low-profile, center-tapped transformer primary from a 5-V DC power supply. The secondary can be wound to provide any isolated voltage based on the transformer turns ratio.

The SN6501 consists of an oscillator followed by a gate drive circuit that provides the complementary output signals to drive the ground referenced N-channel power switches. The internal logic ensures break-before-make action between the two switches.

The SN6501 is available in a SOT-23 (5) package and is specified for operation at temperatures ranging from –40°C to 125°C. The following Figure 3 shows the SN6501 functional block diagram.

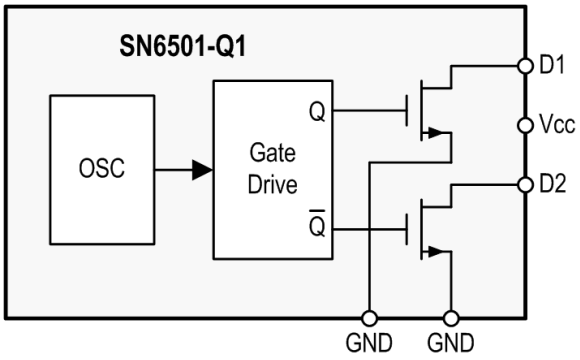


Figure 3. SN6501 Functional Block Diagram

Key features:

- Push-pull driver for small transformers
- Single 3.3-V or 5-V supply
- High primary-side current drive:
  - 5-V supply: 350 mA (max)
  - 3.3-V supply: 150 mA (max)
- Low ripple on rectified output allows small output capacitors
- Small 5-pin SOT-23 package

3.1.3 TLV704—Low-Dropout Regulator

The TLV704 series of low-dropout (LDO) voltage regulators are ultralow quiescent current devices designed for extremely power-sensitive applications. Quiescent current is virtually constant over the complete load current and ambient temperature range. These devices are an ideal power-management attachment for low-power MCUs, such as the TI MSP430™ MCU.

The TLV704 device operates over a wide-operating input voltage of 2.5 V to 24 V. For this reason, the device is an excellent choice for both battery-powered systems as well as industrial applications that undergo large line transients.

The TLV704 device is available in a 3-mm × 3-mm SOT23-5 package, which is ideal for cost-effective board manufacturing. The device is specified for operation at temperatures from –40°C to 125°C. The following Figure 4 shows the TLV704 functional block diagram.

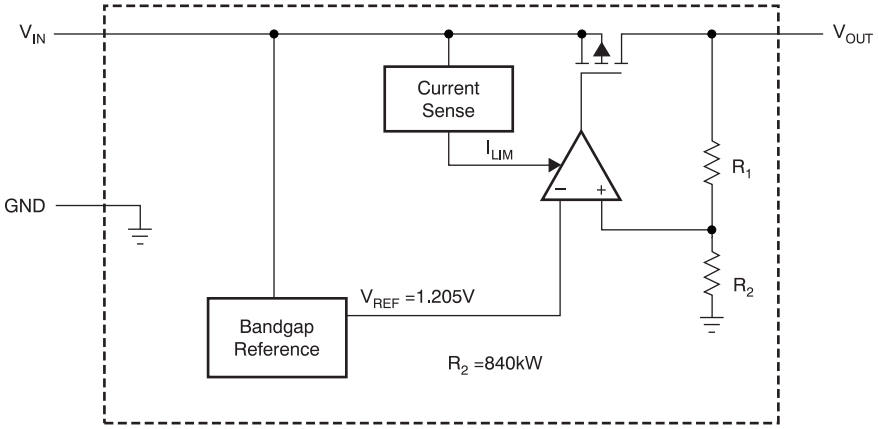


Figure 4. TLV704 Functional Block Diagram

Key Features:

- Wide input voltage range: 2.5 V to 24 V
- Low 3.2-µA quiescent current
- Ground pin current: 3.4 µA at 100-mA I_{OUT}
- Stable with a low-ESR, 1-µF typical output capacitor
- Operating junction temperature: –40°C to 125°C
- Available in an SOT23-5 package

3.1.4 TPS7A30—Negative Linear Regulator

The TPS7A30 series of devices are negative, high-voltage (–35 V), ultralow-noise (15.1 μV_{RMS}), 72-dB power supply rejection ratio (PSRR) linear regulators that can source a maximum load of 200 mA.

These linear regulators include a CMOS logic-level-compatible enable pin and capacitor-programmable soft-start function that allows for customized power-management schemes. The linear regulator features include built-in current limit and thermal shutdown protection to safeguard the device and system during fault conditions.

The TPS7A30 family is designed using bipolar technology, and is ideal for high-accuracy, high-precision instrumentation applications where clean voltage rails are critical to maximize system performance. This design makes the device an excellent choice to power operational amplifiers, ADCs, digital-to-analog converters (DACs), and other high-performance analog circuitry.

In addition, the TPS7A30 family of linear regulators is suitable for post DC-DC converter regulation. By filtering out the output voltage ripple inherent to DC-DC switching conversion, maximum system performance is provided in test and measurement applications.

The TPS7A30 is available in a high thermal performance, MSOP-8 PowerPAD™ integrated circuit package and is specified for operation at temperatures from –40°C to 125°C. The following Figure 5 shows the TPS7A30 functional block diagram.

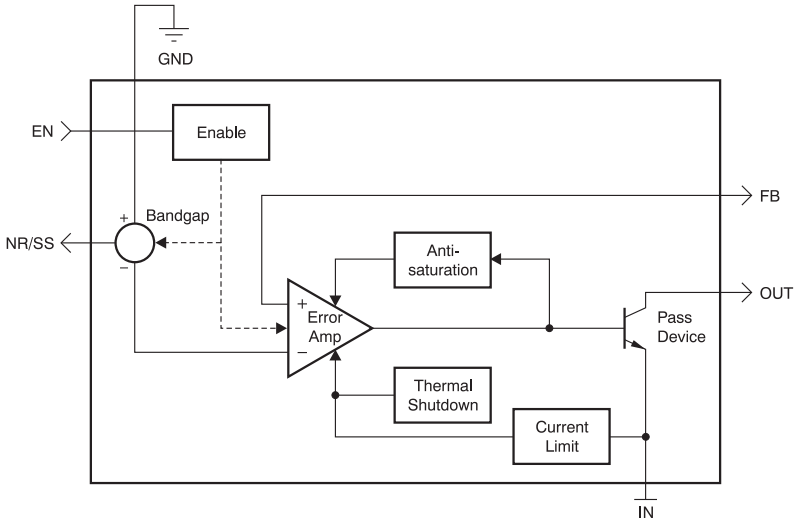


Figure 5. TPS7A30 Functional Block Diagram

Key features:

- Input voltage range: –3 V to –35 V
- Adjustable output: –1.18 V to –33 V
- Maximum output current: 200 mA
- Dropout voltage: 216 mV at 100 mA
- Stable with ceramic capacitors ≥ 2.2 µF
- CMOS logic-level-compatible enable pin
- Built-in, fixed, current limit and thermal shutdown protection
- Available in high thermal performance MSOP-8 PowerPAD™ package
- Operating temperature range –40°C to +125°C

3.1.5 TPS7A6533—Low Dropout Regulator

The TPS7A6533 is a low-dropout linear voltage regulator designed for low power consumption and quiescent current less than 25 µA in light-load applications. This device feature integrated overcurrent protection and is designed to achieve stable operation even with low-equivalent series resistance (ESR) ceramic output capacitors. A low-voltage tracking feature allows for a smaller input capacitor.

The TPS7A6533 device is available in a thermally enhanced power package - three-Pin TO-252 and is specified for operation at temperatures from –40°C to 150°C. The following Figure 6 shows the TPS7A6533 functional block diagram.

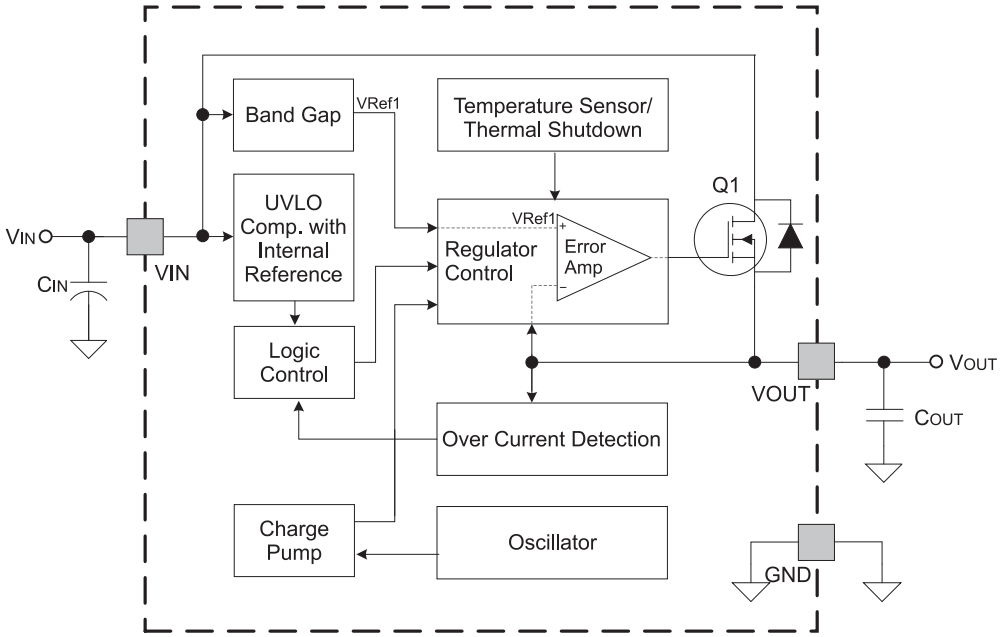


Figure 6. TPS7A6533 Functional Block Diagram

Key features:

- LDO voltage 300 mV at I_{OUT} = 150 mA
- 4- to 40-V wide input voltage range with up to 45-V transients
- 300-mA maximum output current
- 25-µA (typical) ultralow quiescent current at light loads
- 3.3-V fixed output voltage with ±2% tolerance
- Low-ESR ceramic output stability capacitor
- Integrated fault protection
  - Short-circuit and overcurrent protection
  - Thermal shutdown
- Low input-voltage tracking
- Thermally enhanced power package: 3-pin TO-252 (KVU /DPAK)

3.1.6 ADS131E08— 24-Bit, Delta-Sigma (ΔΣ) ADC

The ADS131E08 is a multichannel, simultaneous sampling, 24-bit, delta-sigma (ΔΣ), analog-to-digital converter (ADC) with a built-in programmable gain amplifier (PGA), internal reference, and an onboard oscillator.

The ADS131E08 incorporate features commonly required in industrial power monitoring, control, and protection applications. The ADS131E08 inputs can be independently and directly interfaced with a resistor-divider network or a transformer to measure voltage. The inputs can also be interfaced to a current transformer or Rogowski coil to measure current. With high integration levels and exceptional performance, the ADS131E08 family enables the creation of scalable industrial power systems at significantly reduced size, power, and low overall cost.

The ADS131E08 have a flexible input multiplexer per channel that can be independently connected to the internally-generated signals for test, temperature, and fault detection. Fault detection can be implemented internal to the device, using the integrated comparator with digital-to-analog converter (DAC)-controlled trigger level. The ADS131E08 can operate at data rate as high as 64 kSPS.

This complete analog front-end (AFE) solution is packaged in a TQFP-64 package and is specified over the industrial temperature range of –40°C to +105°C. The following Figure 7 shows the ADS131E08 functional block diagram.

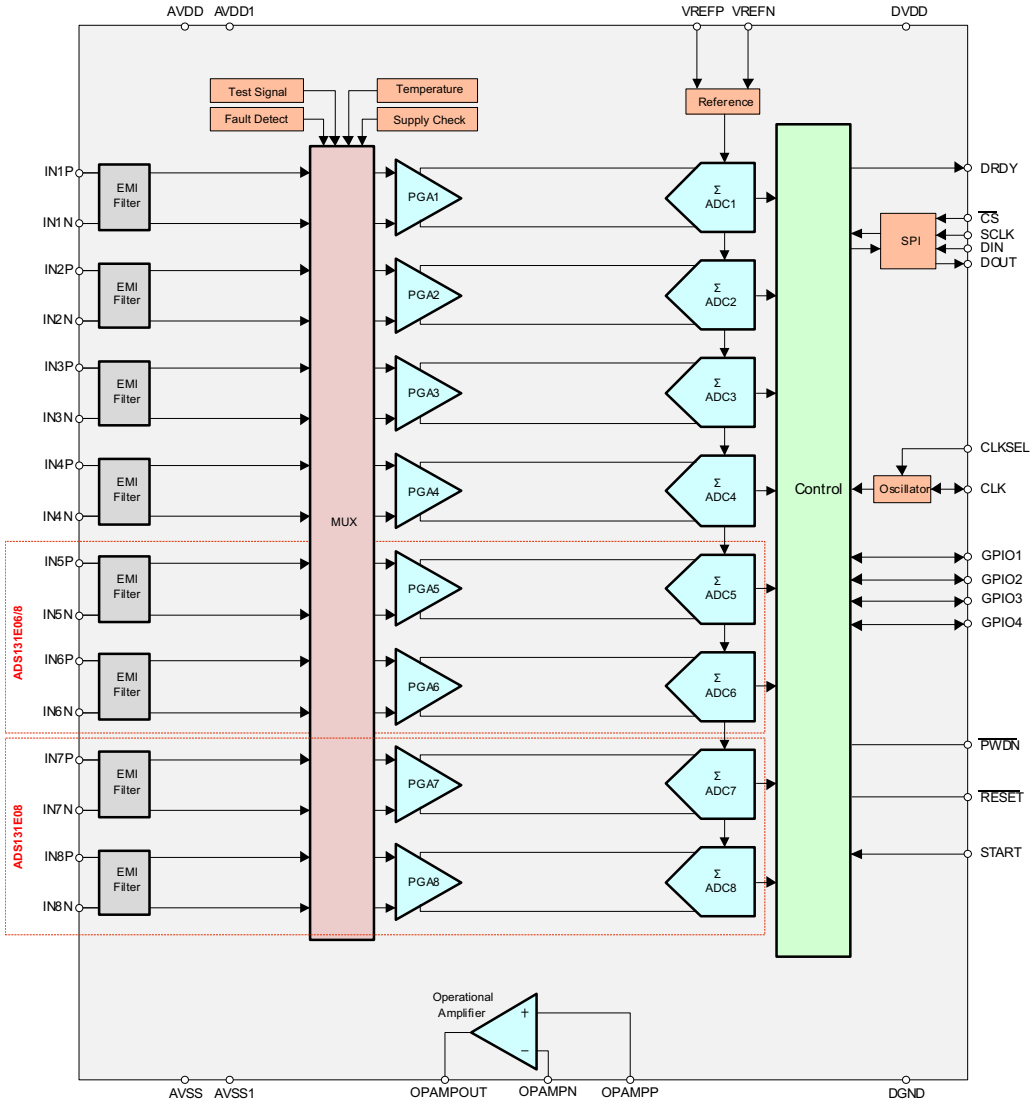


Figure 7. ADS131E08 Functional Block Diagram

Key features:

- Optimized eight differential current and voltage inputs
- Outstanding performance:
  - Exceeds class 0.1 performance
  - Dynamic range at 1 kSPS: 118 dB
  - Crosstalk: –110 dB
  - Total harmonic distribution (THD): –90 dB at 50 Hz and 60 Hz
- Supply range:
  - Analog: 3 V to 5 V (unipolar) ±2.5 V (bipolar, allows DC coupling)
  - Digital: 1.8 V to 3.6 V
- Low power: 2 mW per channel
- Data rates: 1, 2, 4, 8, 16, 32, and 64 kSPS
- Programmable gains (1, 2, 4, 8, and 12)
- Fault detection and device testing capability
- SPI data interface and four general purpose input and output (GPIOs) pins

3.1.7 MSP430FR5869—Mixed-Signal Microcontroller

The MSP430FR5869 is an embedded microcontroller with a 16-bit reduced instruction set computing (RISC) architecture up to a 16-MHz clock with optimized ultra-low-power (ULP) Modes. The MSP430FR5869 device has 12 bit successive approximation register (SAR) ADC. ADC input can be single ended or differential. Up to 16 single-ended or 8 differential external analog inputs can be interfaced with the MSP430FR5869. Device has built-in segment liquid-crystal display (LCD) driver and scan interface.

The MSP430 ULP ferroelectric RAM (FRAM) platform combines uniquely-embedded FRAM and an integrated ultra-low-power system architecture, allowing innovators to increase performance at lowered energy budgets. FRAM technology combines the speed, flexibility, and endurance of SRAM with the stability and reliability of flash at much lower power. The following Figure 8 shows the MSP430FR5869 functional block diagram

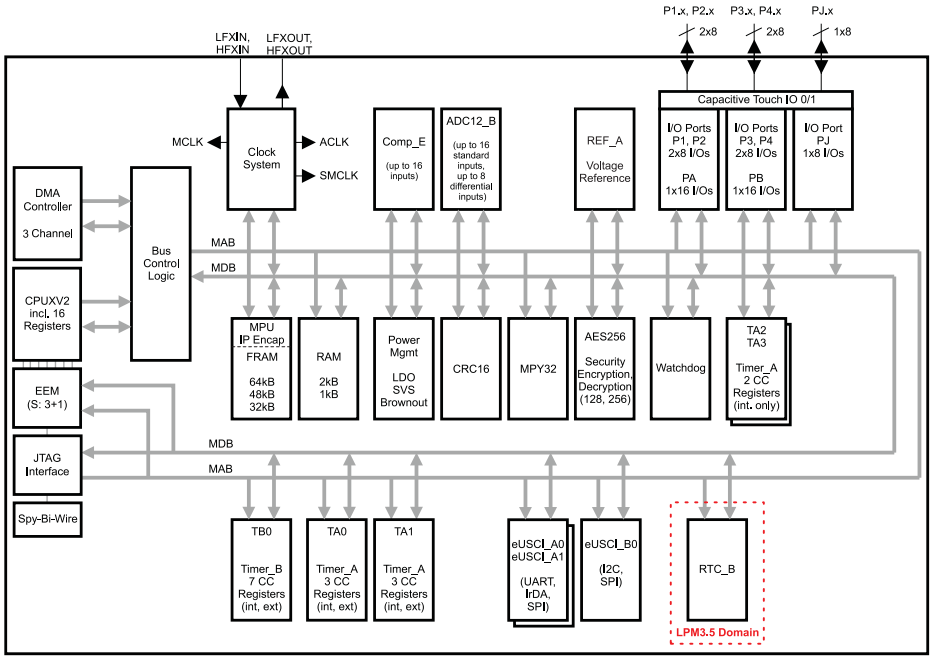


Figure 8. MSP430FR5869 Functional Block Diagram

Key features:

- Embedded MCU
  - 16-bit RISC architecture up to 16-MHz clock
  - Wide supply voltage range: 1.8 V to 3.6 V (minimum supply voltage is restricted by supply voltage supervisor (SVS) levels)
- Optimized Ultralow-power modes
- Ultralow-power ferroelectric RAM (FRAM)
  - Up to 64KB of nonvolatile memory
  - Fast write at 125 ns per word (64KB in 4 ms)
  - 10^{15} write cycle endurance
- Intelligent digital peripherals
- High performance analog
  - 16-channel analog comparator
  - 12-bit ADC with internal reference and sample-and-hold and up to 16 external input channels
- Multifunction input and output ports
- Enhanced serial communication
  - eUSCI_A0 and eUSCI_A1 support
    - Universal asynchronous receiver/transmitter (UART) with automatic baud-rate detection
    - Serial peripheral interface (SPI) at rates up to 10 Mbps
  - eUSCI_B0 supports
    - I^2C with multiple slave addressing
    - SPI at rates up to 8 Mbps
  - Hardware UART and I^2C bootstrap loader (BSL)
- Flexible clock system
- Operating Temperature Range: –40°C to +85°C

4 System Design Theory

4.1 Isolated Measurement

The AMC1100 offers a configurable output common-mode voltage through VDD2 (low-side power supply).

Table 4. Configurable Output Common-Mode Voltage

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output common-mode voltage	2.7 V ≤ VDD2 ≤ 3.6 V	1.15	1.29	1.45	V
	4.5 V ≤ VDD2 ≤ 5.5 V	2.4	2.55	2.7	

The ADC can have an input range within 0 V to 2.5 V or 0 V to 5 V.

The ADS131E08EVM-PDK AVCC value is up to 5 V. The AMC1100 VDD2 must be set to 5 V when interfacing with the ADS131E08EVM-PDK.

The MSP430FR5869 supply voltage AVCC is 3.3 V. The AMC1100 VDD2 must be set to 3.3 V when interfacing to the MSP430FR5869.

4.1.1 Isolated Current Measurement

The TIDA-00555 design provides a provision for measuring three current inputs. The shunts are used to measure the input current. The shunt value can be calculated as the following Equation 1:

$$R_{SHUNT} = V_{SHUNT\_MAX} / I_{IN\_MAX} \times 1000 \quad (1)$$

where

- R_{SHUNT} is the shunt value in mΩ
- I_{IN_MAX} is the maximum input current
- V_{SHUNT_MAX} is the acceptable maximum output voltage across a shunt for the maximum input current

The design uses an isolation amplifier to achieve current signal isolation. The filter circuit consists of resistors and a capacitor and its placement follows the shunt resistor. The filtered voltage is applied to the isolation amplifier.

The following Figure 9 shows the current measurement section of the TIDA-00555.

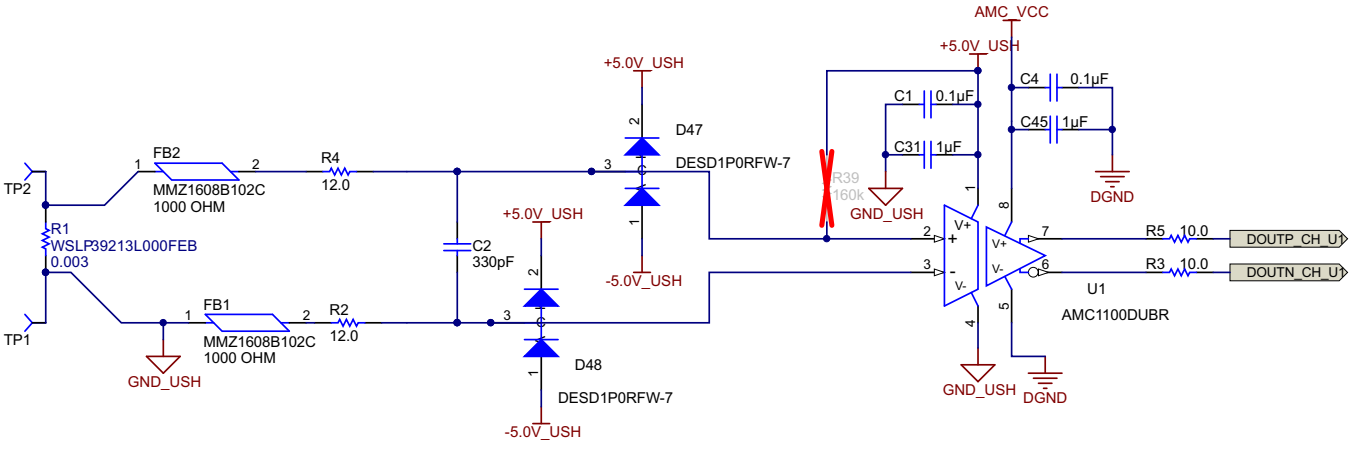


Figure 9. Circuit Diagram of U Current Input

Using Equation 1, the user can calculate the shunt value. This design uses a 3-mΩ shunt.

4.1.2 Isolated Voltage Measurement

The TIDA-00555 design provides a provision for measuring three voltage channels. The following Figure 10 shows one of the voltage input circuits.

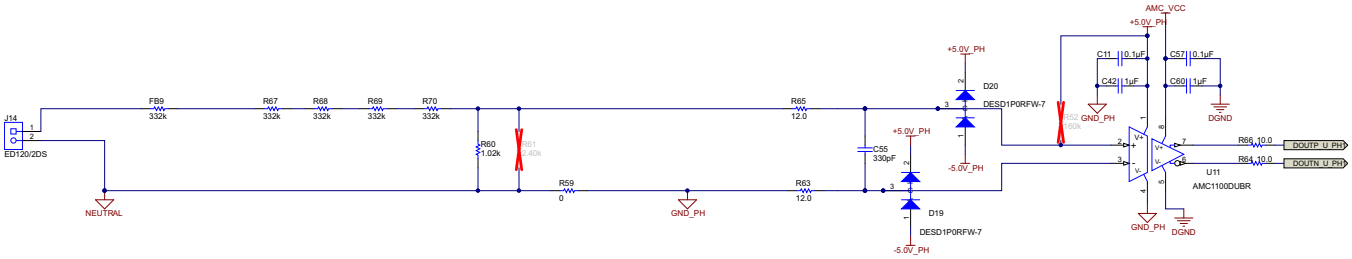


Figure 10. Circuit Diagram of U Voltage Input

A ferrite bead can be used across FB9 when used in a noisy environment or when the voltage divider resistance is to be reduced.

The voltage divider resistor values for the AC input voltage channel is selected to ensure that the input to the AMC1100 is less than the differential input range at the maximum AC input voltages.

Potential divider calculation:

Max sensing voltage → V_{MAX}	= 276 V_{RMS} (+20% of 230 V)
Peak max sensing voltage → V_{MAX_PK}	= V_{MAX} × 1.414
	= 390 V

The peak voltage output of the resistor divider used for measurement must be less than the input voltage range of the AMC1100, which is 250 mV.

The potential divide ratio must be selected such that the output voltage is less than the AMC1100 voltage at the maximum input voltage. To reduce loading, the impedance specified for the measurement circuit is > 1 MΩ. An impedance of 1.66 MΩ has been chosen.

This design uses a 1.02-KΩ for R60 as the following Equation 2 shows.

$$R60 \le V_{OUT} / (V_{MAX\_PK} - V_{OUT}) \times 1.66\ M\Omega$$
$$\le 1.064\ K\Omega \quad (2)$$

where

- V_{MAX_PK} = 390 V
- V_{OUT} ≤ 250 mV

4.2 Power Supply

4.2.1 Isolated Power Supply

The following Figure 11 shows the design of the isolated power supply.

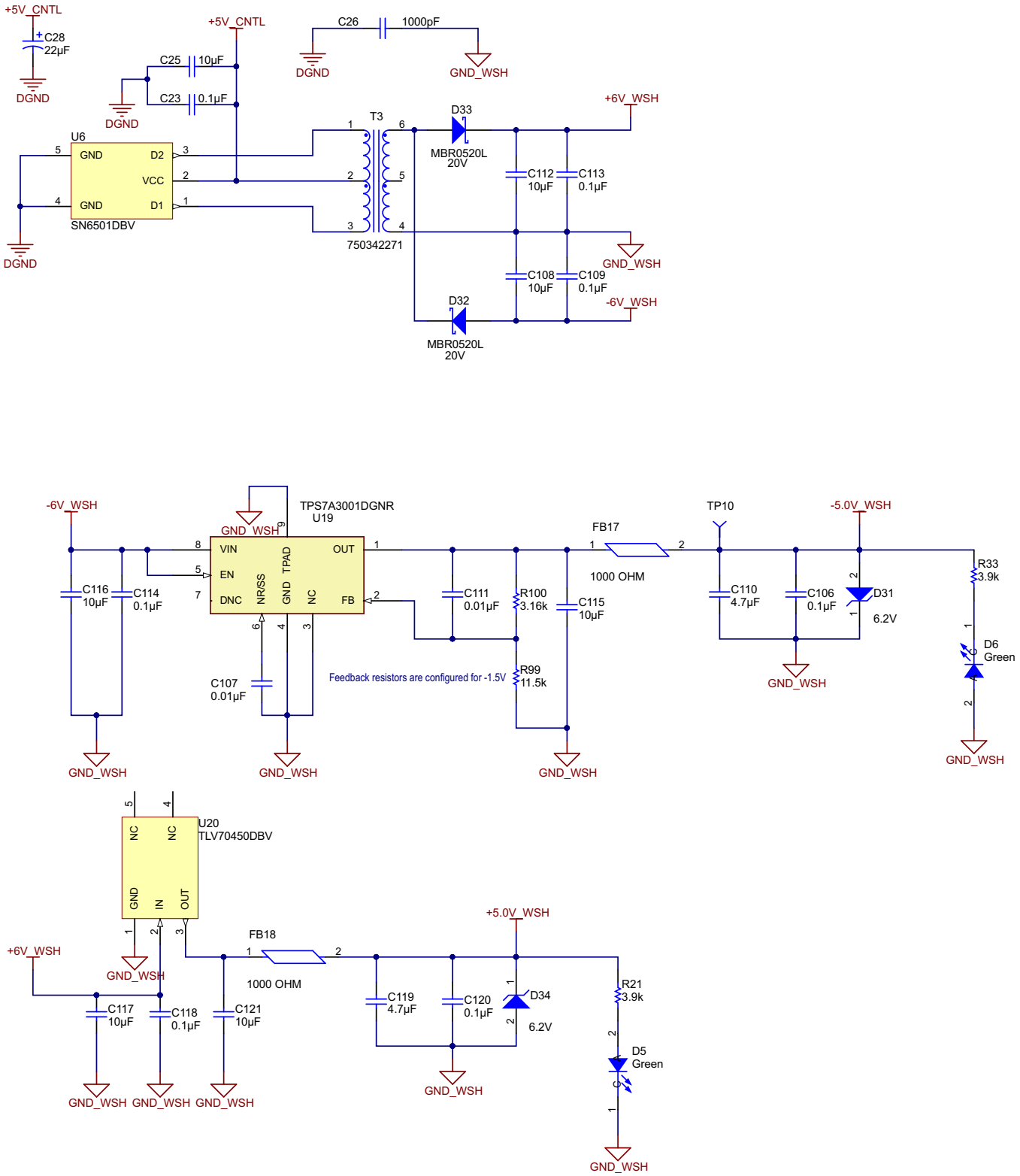


Figure 11. Isolated Power Supply and Zener Protection Schematics

Some design features of the isolated power supply are:

- The use of an SN6501 device, which is a monolithic oscillator and power-driver specifically designed for small-form factor, isolated power supplies in isolated interface applications. The SN6501 oscillator drives a low-profile, center-tapped transformer primary from a 5-V DC power supply. The TIDA-00555 design uses a transformer with a 1.64:1 turns ratio to generate ±6 V.
- The use of a TLV70450DBV, which is an ultralow IQ (quiescent current), high V_{IN} LDO for modulator operation on the isolated side is used to convert the 6 V to 5 V required for the AMC1100 operation.
- The use of a TPS7A3001DGNR, which is a negative, high-voltage, ultralow-noise linear regulator for protection on the isolated side. The TPS7A3001DGNR regulator is used to convert the –6 V to –5 V required to operate the AMC1100.
- The use of three current and three voltage channels. Three current channels are isolated from each other and three voltage channels are group isolated and share a single isolated power supply. Protection is provided at each input channel with the overvoltage at 5-V DC and –5-V DC.

NOTE: This reference design uses a custom-designed transformer. Please contact Würth as required.

4.2.2 Non-Isolated Power Supply

The following Figure 12 shows the design of the non-isolated power supply with Zener protection.

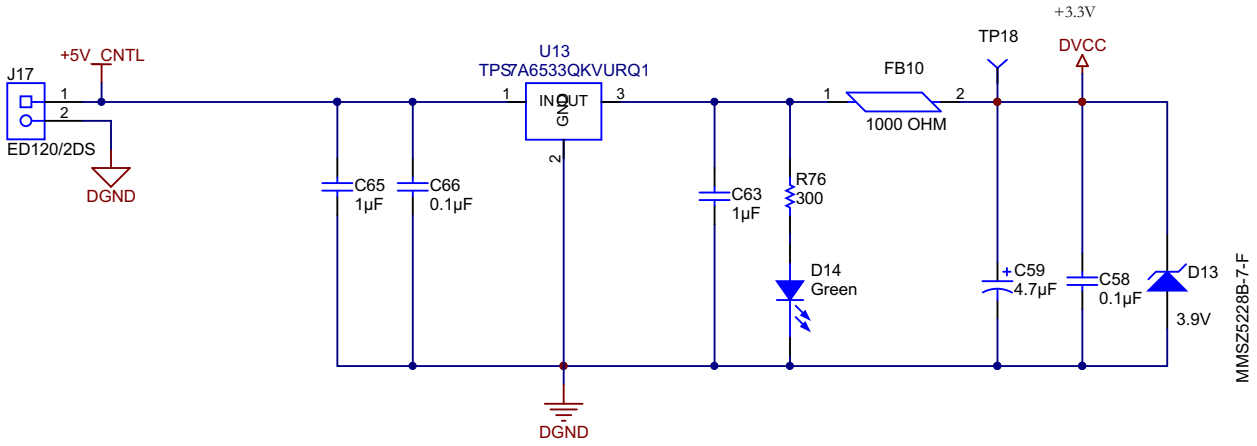


Figure 12. Non-Isolated Power Supply With Zener Protection

To power the measurement module, connect an external DC supply on the two-pin terminal block J17. This design uses the TPS7A6533-Q1 LDO, for which a 5-V DC input must be applied. The DVCC for the measurement module is 3.3 V. The power supply is protected against overvoltage and uses a light-emitting diode (LED) to indicate the power supply status.

4.3 ADS131E08EVM-PDK

The ADS131E08EVM-PDK is a performance demonstration kit (PDK) intended for evaluating the ADS131E08 low-power, 24-bit, simultaneously sampling, eight-channel ADC. The digital SPI control interface is provided by the MMB0 modular EVM motherboard that connects to the ADS131E08 evaluation board. The ADS131E08EVM-PDK is designed to expedite evaluation and system development. The MMB0 motherboard allows the ADS131E08EVM to be connected to the computer through an available USB port.

For more details on how to use the MMB0 as part of the ADS131E08EVM-PDK, refer to the *Performance Demonstration Kit for the ADS131E08* User's Guide (SBAU200). The following Figure 13 shows a board image of the ADS131E08EVM-PDK.

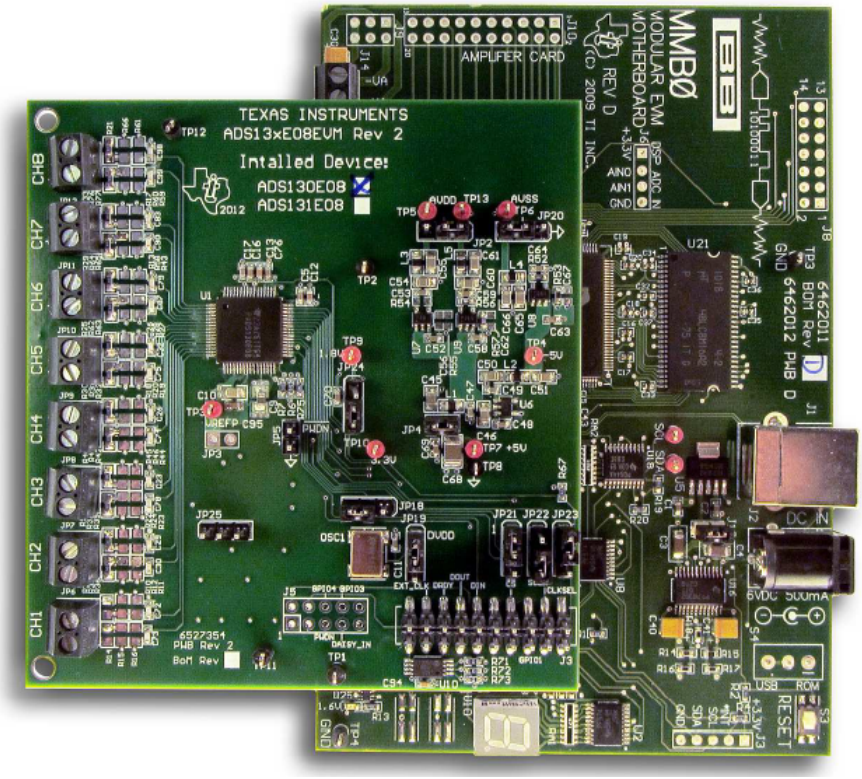


Figure 13. ADS131E08EVM-PDK Board Image

Supported features of the EVM are:

Hardware features:

- Configurable for bipolar or unipolar supply operation
- Configurable for internal and external clock through jumper settings
- Analog test signals can be applied easily using screw terminals

Software features:

- Analysis tools, including a virtual oscilloscope, histogram, and fast Fourier transform (FFT)
- Access to a variety of register contents, including data rate, PGA options, and more
- Set ADS131E08 register settings with easy-to-use, graphical user interface (GUI) software

The ADS131E08EVM mounts on the MMB0 board with connectors J1, J2, and J3. The main power supplies (5 V, 3 V, and 1.8 V) for the front-end board are supplied by the host MMB0 board through connector J3. All other power supplies required for the front-end board are generated onboard by power management devices.

The ADS131E08 digital signals (including SPI signals, some GPIO signals, and some control signals) are available at connector J1. These signals can be used to interface with the MSP430FR5869 on the TIDA-00555 board. These signals are used to interface to the MMB0 board DSP in the EVM.

Table 5 shows the pinout configuration for this connector.

Table 5. J1 Connector Pinout Configuration

SIGNAL	J1 PIN NUMBER		SIGNAL
START/CS	1	2	CLKSEL
CLK	3	4	GND
NC	5	6	GPIO1
CS	7	8	RESET
NC	9	10	GND
DIN	11	12	GPIO2
DOUT	13	14	NC/START
DRDY	15	16	SCL
EXT_CLK	17	18	GND
NC	19	20	SDA

The analog signals can be applied at terminal blocks J5 through J12 (also marked as CH1 to CH8 on the board). For TIDA-00555 interface testing, the AVDD is set to 5 V and the AVSS is set to 0 V on this EVM.

NOTE: The user must ensure a 5-V unipolar analog power supply configuration on the ADS131E08EVM-PDK board. The IC U6 must be changed from TPS73230 (3 V) to TPS73250 (5 V) to configure a unipolar analog power supply to 5 V. The grounds of the ADS131E08EVM-PDK and TIDA-00555 board must be connected together using jumper wire.

4.4 MCU

4.4.1 MCU Interfacing

The TIDA-00555 design interfaces with the MSP430FR5869 MCU. The user can interface three current and three voltage channels with the SAR ADC of the MSP430FR5869. The ADC has a 12-bit resolution and can be configured to measure differential input.

Figure 14 shows a schematic of the MSP430FR5869.

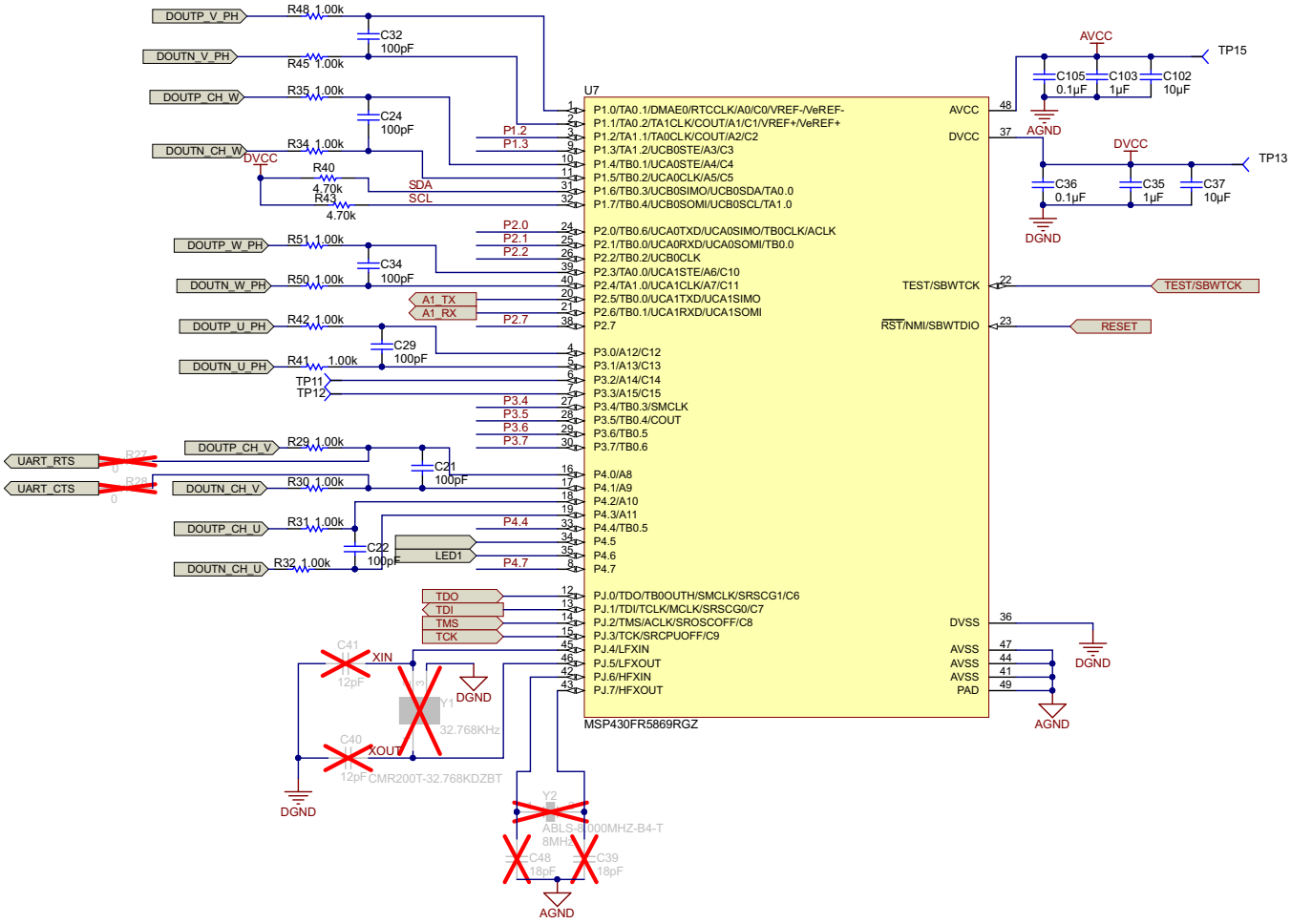


Figure 14. MSP430FR5869 MCU Schematic

Figure 15 shows the expansion interface. Different expansion options are available in this design:

- SPI: To utilize the full input range of the AMC1100, an ADC with a 0- to 5-V input range is required, such as the ADS131Exx. To measure at full scale, connect the SPI of the MCU with the ADS131E08 EVM, which interfaces with the AMC1100 output. Alternatively, the SPI can be used to communicate with the graphical user interface (GUI).
- UART: The user can implement RS232 communication by connecting the RS232 chip externally to the UART.
- I^2C: The inputs may require calibration based on the accuracy of the sensing devices used. In the case of this design, the user can connect an EEPROM to the I^2C interface to store the calibration values. This I^2C interface can be used to interface to the temperature sensor, real-time clock (RTC), or any other I^2C interface-based peripherals.
- GPIO: The inputs of the general-purpose input and output (GPIO) pin can be used as input or output, timer inputs, or pulse-width modulation (PWM) outputs. These inputs and outputs can be used when feature enhancements are required.

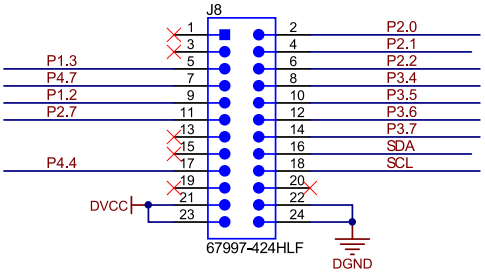


Figure 15. Expansion Interface

LED indication:

Two LEDs are available on the design board. Both LEDs can be configured based on the user's specification. Figure 16 shows the LED schematic.

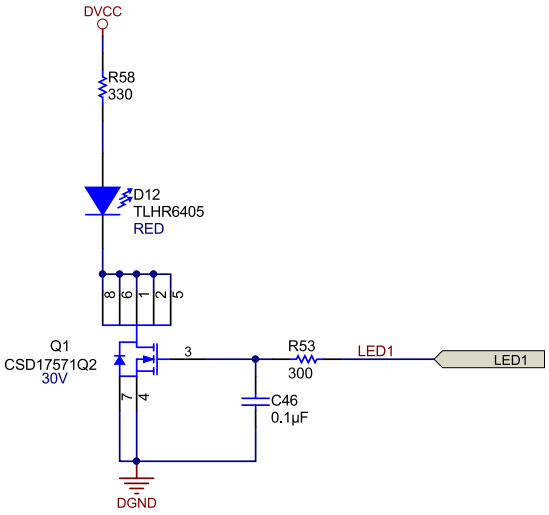


Figure 16. LED Schematic

NOTE: The applied analog signal must satisfy limits of the ADC's analog input voltage range.

4.4.2 MCU Programming

The MSP430 family supports the standard JTAG interface that requires four signals for sending and receiving data. The JTAG signals are shared with the GPIO. The TEST/SBWTCK pin is used to enable the JTAG signals. In addition to these signals, the RST/NMI/SBWTDIO pin is required to interface with the MSP430 development tools and device programmers.

Figure 17 shows the JTAG programming connector schematic. For further details on interfacing to development tools and device programmers, see the *MSP430 Hardware Tools* User's Guide (SLAU278). For a complete description of the features of the JTAG interface and its implementation, see the *MSP430 Programming Via the JTAG Interface* User's Guide (SLAU320).

The connector J3 is the JTAG programming interface connector for the TIDA-00555 design.

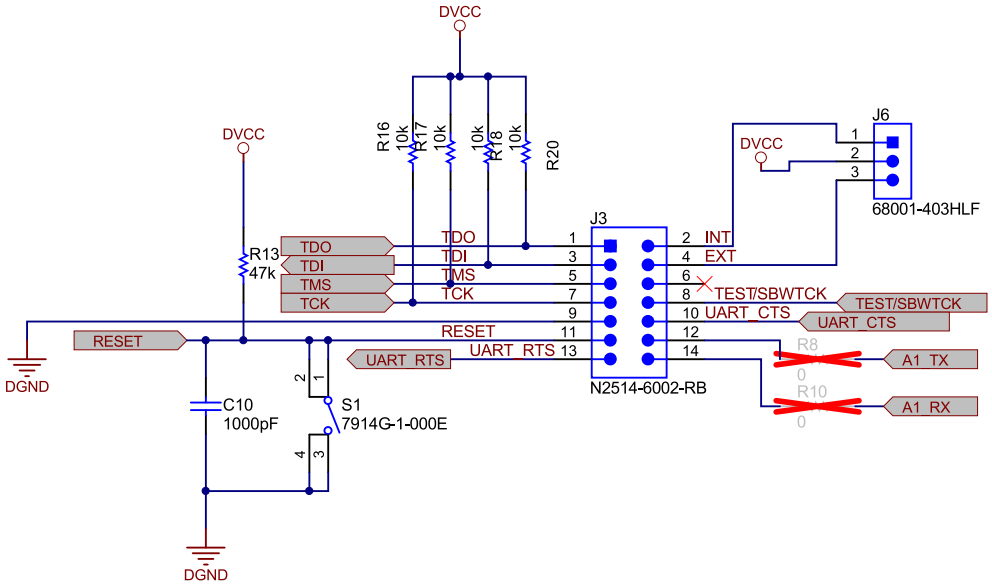


Figure 17. JTAG Programming Connector

4.4.3 MCU—Initialization and RMS Computation

Initializing the watch dog timer

Disable the watchdog timer

Initializing the oscillator port pins

Set the port bits PJ.4, PJ.5, PJ.6, and PJ.7 if the LF clock or HF clock is required. Clear the LOCKLPM5 bit in register PM5CTL0.

Initializing FRAM

Configure the FRAM control register FRCTL0 (using the password) for one wait state because the clock is configured for 16 MHz.

Initializing the oscillator

Unlock the CS registers with the CSCTL0_H register using the CSKEY password.
Using register CSCTL1, select DCORSEL (= 1) and DCOFSEL (= 4) to select 16 MHz.
Using register CSCTL2, select SELS and SELM as the DCO clock (SELA defaults to the VLO clock and can be changed to the desired setting).
Using register CSCTL3, select the divider A, divider S, and divider M values as 1.
Lock the CS registers using the CSCTL0_H register.

Initializing the port pins

To initialize the ADC port pins A0 and A1:
Set P1SEL0: bit0 and bit1 high
Set P1SEL1: bit0 and bit1 high
To initialize the ADC port pins A4 and A5:
Set P1SEL0: bit4 and bit5 high
Set P1SEL1: bit4 and bit5 high
To initialize the ADC port pins A6 and A7:
Set P2SEL0: bit2 and bit3 high
Set P2SEL1: bit2 and bit3 high

To initialize the ADC port pins A12 and A13:
Set P3SEL1: bit0 and bit1 high
To initialize the ADC port pins A14 and A15:
Set P3SEL1: bit2 and bit3 high
To initialize the ADC port pins A8 and A9:
Set P4SEL1: bit0 and bit1 high
To initialize the ADC port pins A10 and A11:
Set P4SEL1: bit2 and bit3 high
Initializing the LED pins:
Set P4DIR: bit5 and bit6 high to set the port direction
Set P4OUT: bit5 and bit6 high

Enabling the internal reference

Enable the internal reference using register REFCTL0:
Enable bit0 to turn ON the internal reference
Enable bit4 and bit5 to select the voltage reference (2.5 V)
To allow the reference voltage to settle, TI recommends the use of a delay

Initializing the ADC for differential inputs

Set the ADC control register ADC12CTL0 as follows:
Enable sample and hold0, bit4 (64 clock cycles)
Enable sample and hold1, bit4
Enable the ADC12MSC bit to enable multiple sample conversion (to enable sequence of conversions)
Enable the ADC12ON bit
Set the ADC control register ADC12CTL1 as follows:
Enable the ADC12SHP to source the SAMPCON signal from the sampling timer (timer B)
Set ADC12CONSEQx (bits 2–1) to 01b to choose the sequence of channels
Set ADC12SHSx = {3} to select Timer B0 as the sampling timer source
Set ADC12SSELx = 11b to select the SMCLK as the ADC clock source
In the ADC control register ADC12CTL2, set the ADC12RES bits to 10b, which forces the ADC to operate in 12-bit mode

ADC channel selection

ADC channel selection
Select ADC channel0 in differential mode with VeREF+ as positive reference and VeREF– as negative reference in ADC12MCTL0 register.
Select ADC channel4 in differential mode with VeREF+ as positive reference and VeREF– as negative reference in ADC12MCTL1 register.
Select ADC channel6 in differential mode with VeREF+ as positive reference and VeREF– as negative reference in ADC12MCTL2 register.
Select ADC channel8 in differential mode with VeREF+ as positive reference and VeREF– as negative reference in ADC12MCTL3 register.
Select ADC channel10 in differential mode with VeREF+ as positive reference and VeREF– as negative reference in ADC12MCTL4 register.
Select ADC channel12 in differential mode with VeREF+ as positive reference and VeREF– as negative reference in ADC12MCTL5 register.
Select ADC channel14 in differential mode with VeREF+ as positive reference and VeREF– as negative reference in ADC12MCTL6 register. Also enable the end of conversion sequence bit.
In the ADC interrupt, enable register ADC12IER0 and enable bit 6. Doing this enables the ADC interrupt when the analog-to-digital conversion is complete and the ADC12MEM6 is filled with the conversion result.

Initializing the timer for ADC sampling

Initializing the timer
Set the TB0R register value to 0
Set the TB0CCR0 register to 2500 (sampling interval)
Set the TB0CCTL1 to mode 3 (set/reset)
Set the TB0CTL register as follows:
TBSSEL bits to 11b (SMCLK)
CNTL bits to 00b (16 bits)
MC bits to 11b (up/down mode)
Enable the TBCLR bit

Processing the ADC interrupt

An ADC interrupt occurs if the ADC interrupt enable bit is set and the analog-to-digital conversion is complete. The results are available from the registers ADC12MEM0 to ADC12MEM6. The results are copied to the results [] array.
Set a flag using a (volatile) variable to indicate the data is available.
Enable Analog-to-digital conversion using the register ADC12CTL0 (ADC12ENC bit).

Root mean square (RMS) value computation

As soon as the device initialization is over, the program counter waits for a flag (that indicates the data is available). When the flag is set, the data is copied from the results array into In_data[sample_count] (where n = 1 to 8 and sample_count = 0 to 63).
Then the sample value is corrected for an offset of 2048 and is made absolute (sign is ignored). The sample counter is incremented. The results are collected in the same way (using the aforementioned procedure) for all 64 samples. For each cycle, 64 samples of data are collected.
After obtaining the 64 samples, the root mean square is computed in the following manner:
Each sample (of the 64 samples) is squared and added in a float variable sum.
The sum is divided by 64 in a float variable temperature.
The square root of the temperature is then calculated. The resulting value is the RMS for a particular channel. This process of RMS computation is used for channels A0, A4, A6, A8, A10, A12, and A14.

5 Getting Started

5.1 Connectors

The following Table 6 explains the different connectors on the board and their usage.

Table 6. Connectors

INPUT AND OUTPUT TYPE	DESCRIPTION	CONNECTORS
Current I/P	Channel 1	TP2, TP1
	Channel 2	TP5, TP4
	Channel 3	TP8, TP7
Voltage I/P	Channel 1	J14.1 wrt J14.2
	Channel 2	J15.1 wrt J15.2
	Channel 3	J16.1 wrt J16.2
VDD2 (AMC_VCC) selection option	5-V DC or 3.3-V DC	For 5 V: short J28.3 and J28.2
		For 3.3 V: short J28.1 and J28.2
Power supply input	5-V DC	J17.1 wrt J17.2
Interfacing AMC1100 with MSP430FR5869 (AMC_VCC must have 3.3-V DC for this)	For current sensing: Jumper between (short) these connectors	J10.1 – J10.2
		J11.1 – J11.2
		J18.1 – J18.2
		J19.1 – J19.2
		J20.1 – J20.2
		J21.1 – J21.2
	For voltage sensing: jumper between (short) these connectors	J22.1 – J22.2
		J23.1 – J23.2
		J24.1 – J24.2
		J25.1 – J25.2
		J26.1 – J26.2
		J27.1 – J27.2
MSP430FR5869 programming	JTAG	J3
Interfacing AMC1100 with ADS131E08EVM-PDK 1. Configure AMC_VCC on the TIDA-00555 board to 5 V 2. Connect the differential output from TIDA-00555 board to ADS131EVMPDK terminal blocks J5 through J12 (also marked as CH1 to CH8 on the EVM board)	For current measurement:	J10.2 wrt J11.2
		J18.2 wrt J19.2
		J20.2 wrt J21.2
	For voltage measurement:	J22.2 wrt J23.2
		J24.2 wrt J25.2
		J26.2 wrt J27.2

The following Figure 18 shows the TIDA-00555 interface connectors with a brief application description.

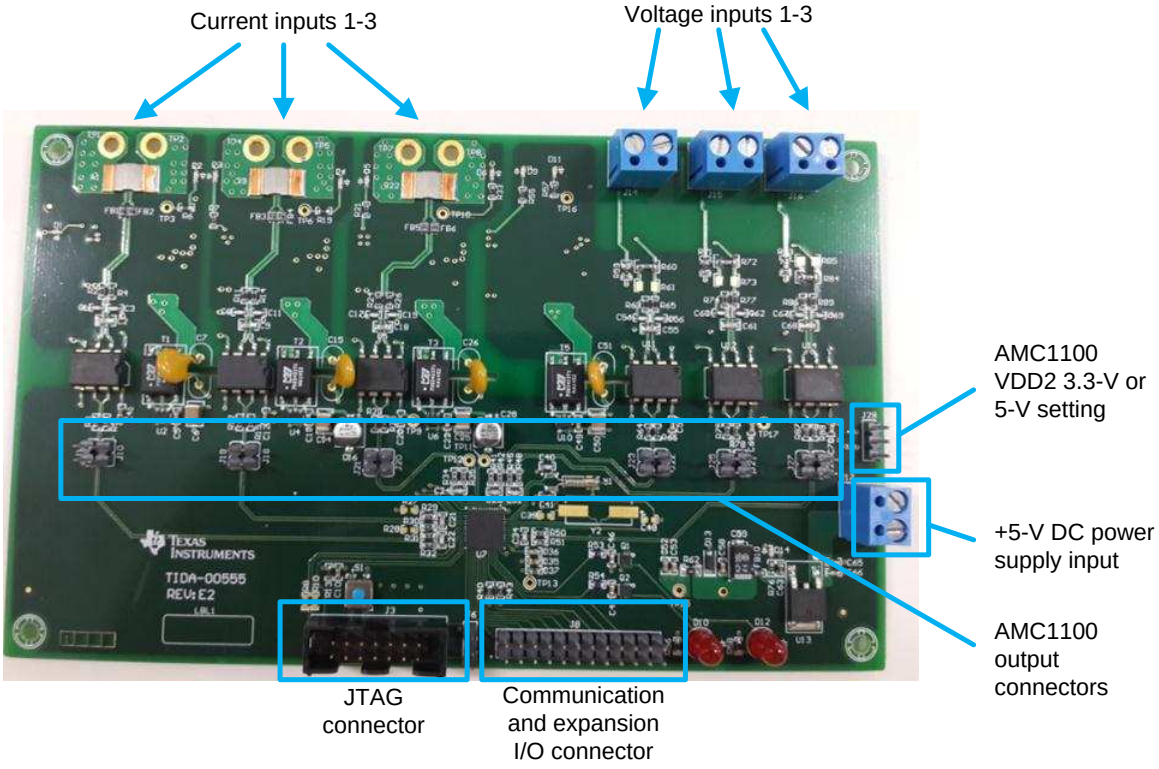


Figure 18. TIDA-00555 Interface Connectors

5.2 DC Power Supply Input Voltage

The power supply input is 5-V DC. Be sure to consider the initial inrush current during the power supply selection.

5.3 AC Signal Input Range

The differential input voltage of the AMC1100 device is ±250 mV as the following Equation 3 shows.

$$V_{Peak\_AMC} = 250 \text{ mV}$$

$$V_{Peak\_AMC\_RMS} = 250 \text{ mV} / 1.414 \approx 175 \text{ mV} \quad (3)$$

This design uses 175 mV as a full-scale input for AC signals.

5.3.1 Current Input Range

The shunt resistor used in this design is 3 mΩ and the power rating is 5 W.

To calculate the maximum input current for the shunt, use $P = I^2R$ to solve the following Equation 4 and Equation 5:

$$I_{max} \le (P / R)^{0.5} \le 40.8 \text{ A} \quad (4)$$

$$I_{min} = V_{Peak\_AMC\_RMS} \times 5\% / R_{shunt} = 2.9 \text{ A} \quad (5)$$

NOTE: When selecting the shunt to measure current, ensure that the input to AMC1100 does not exceed the maximum input at the maximum input current rating.

5.3.2 Voltage Input Range

The input voltage range for this design is 15 V to 300 V.

NOTE: Ensure that the input to the AMC1100 does not exceed the maximum rated input for the maximum expected AC input voltage for scenarios where changing the potential divider value may be required.

6 Test Setup

The following Figure 19 and Figure 20 show physical images of the test equipment; Figure 21 shows the ADS131E08EVM-PDK board used for testing the TIDA-00555 design.

Figure 19. 5-V DC Source

Figure 20. Programmable Power Source

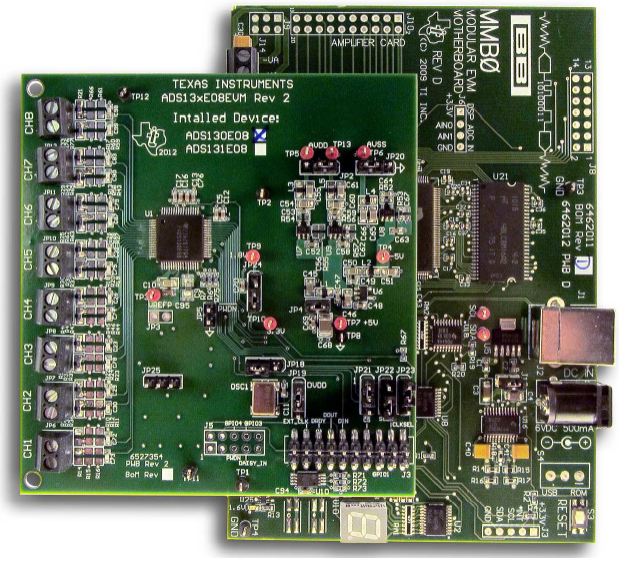


Figure 21. ADS131E08EVM-PDK EVM

6.1 Test Setup Connections

6.1.1 Test Setup for Interfacing TIDA-00555 With ADS131E08EVM-PDK

The TIDA-00555 board is interfaced with the ADS131E08EVM-PDK through the AMC1100 output jumper interface. Set the AMC_VCC pin to 5 V. The programmable power source, PTS3.3C, is used to provide voltage and current of the required amplitude and frequency. The ADS131E08EVM GUI is installed on the computer, which can be used to modify the ADS131E08 device settings and to capture the ADC values. Connect the J1 USB connector to the system for communication. Connect the power adaptor to J2 of the ADS131E08EVM-PDK. A 5-V DC input powers the TIDA-00555 board.

As Table 6 notes, the connections must be made as per the specifications in the "Interfacing AMC1100 with ADS131E08EVM-PDK" row under the "INPUT AND OUTPUT TYPE" column and the AMC_VCC must be set to 5 V. The following Figure 22 shows the test setup for testing the TIDA-00555 design with the ADS131E08EVM-PDK.

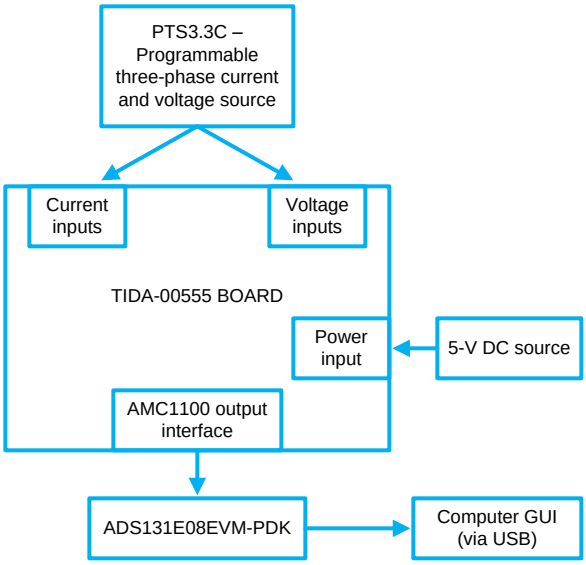


Figure 22. Test Setup Using ADS131E08EVM-PDK

NOTE: Ensure that 5-V DC is applied to the TIDA-00555 board before applying input voltages or currents.

6.1.2 Test Setup for Interfacing AMC1100 With MSP430FR5869

TIDA-00555 board is interfaced with the MSP430FR5869 device through AMC1100 output jumper interface. The AMC_VCC is set as 3.3 V. The programmable power source PTS3.3C is used to generate voltage and current of the required amplitude and frequency. The ADC values are captured through test firmware developed on the watch window for the CCS software. A JTAG connection is required for the CCS interface. The TIDA-00555 board is powered through an external 5-V DC power supply.

As Table 6 notes, the jumper settings must be set as per the specifications in the "Interfacing AMC1100" row under the "INPUT AND OUTPUT TYPE" column and the AMC_VCC must be set to 3.3 V. The following Figure 23 shows the test setup for testing the MSP430FR5869 device.

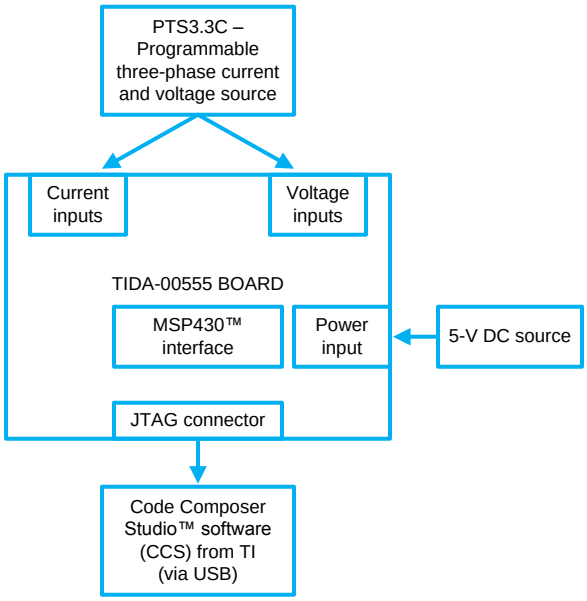


Figure 23. Test Setup MSP430FR5869

7 Test Data

7.1 Functional Testing

Table 7 shows the onboard power supply measurement.

Table 7. TIDA-00555 Measured PSU Voltage Levels

PARAMETERS	MEASURED PARAMETER	MEASURED VALUE (V-DC)
Power supply	+5-V DC input	5.029
Isolated power supply – Channel U	+5V_USH	4.98
Isolated power supply – Channel V	+5V_VSH	4.95
Isolated power supply – Channel W	+5W_WSH	5.00
Isolated common power supply – Voltage channel	+5V_PH	4.97
Non-isolated power supply	3.3	3.281

7.2 Performance Testing

Please note the following before analyzing the accuracy performance results:

- Measured output voltage mV: This is the output voltage measured without applying gain and offset calibration.
- % Error: The is the output measurement error after applying offset and gain calibration.
- The DC offset is zero (not applicable) when no offset is mentioned.

NOTE: Be sure to consider the gain factor and offset when calculating.

7.2.1 Accuracy Test (Amplifier Output) for Voltages

7.2.1.1 Accuracy Testing at 50 Hz

The AMC1100 output voltage is measured with a 6 ½ digital multimeter (DMM). The error is calculated for the measured output voltage versus the expected output voltage. The gain factor and offset have been applied for error calculation.

Table 8, Table 9, and Table 10 show the measured accuracy of three voltage channels. Figure 24 shows a plot of the complete voltage channel accuracy.

Table 8. Voltage Channel U

AC INPUT VOLTAGE ADJUSTED AS % OF FULL SCALE (100% = 175 mV)	APPLIED INPUT VOLTAGE (V)	MEASURED INPUT VOLTAGE (V)	EXPECTED OUTPUT VOLTAGE (mV)	MEASURED OUTPUT VOLTAGE (mV)	ERROR
3%	9	9.00163	42.668	42.41	0.13%
5%	15	15.0017	71.109	70.641	0.08%
10%	30	30.0018	142.211	141.162	0.00%
20%	60	60.0018	284.413	282.407	0.03%
30%	90	90.0017	426.615	423.585	0.02%
41%	120	120.005	568.833	564.933	0.05%
51%	150	150.006	711.040	706.286	0.07%
61%	180	180.013	853.275	847.661	0.08%
71%	210	210.005	995.440	989.17	0.11%
81%	240	240.01	1137.666	1130.736	0.13%
91%	270	270.013	1279.882	1271.06	0.05%
102%	300	300.013	1422.084	1412.68	0.07%

Table 8. Voltage Channel U (continued)

AC INPUT VOLTAGE ADJUSTED AS % OF FULL SCALE (100% = 175 mV)	APPLIED INPUT VOLTAGE (V)	MEASURED INPUT VOLTAGE (V)	EXPECTED OUTPUT VOLTAGE (mV)	MEASURED OUTPUT VOLTAGE (mV)	ERROR
112%	330	330.006	1564.253	1554.42	0.11%
122%	360	360.016	1706.503	1696.37	0.14%

The gain factor for this voltage channel U is 1.0074.

Table 9. Voltage Channel V

AC INPUT VOLTAGE ADJUSTED AS % OF FULL SCALE (100% = 175 mV)	APPLIED INPUT VOLTAGE (V)	MEASURED INPUT VOLTAGE (V)	EXPECTED OUTPUT VOLTAGE (mV)	MEASURED OUTPUT VOLTAGE (mV)	ERROR
3%	9	9.00163	42.668	42.457	0.15%
5%	15	15.0017	71.109	70.675	0.04%
10%	30	30.0018	142.211	141.288	0.00%
20%	60	60.0018	284.413	282.483	–0.03%
30%	90	90.0017	426.615	423.767	–0.02%
41%	120	120.005	568.833	565.096	–0.01%
51%	150	150.006	711.040	706.492	0.01%
61%	180	180.013	853.275	847.973	0.02%
71%	210	210.005	995.440	989.473	0.05%
81%	240	240.01	1137.666	1131.109	0.07%
91%	270	270.013	1279.882	1272.78	0.09%
102%	300	300.013	1422.084	1414.99	0.15%
112%	330	330.006	1564.253	1555.94	0.12%
122%	360	360.016	1706.503	1697.51	0.12%

The gain factor for this voltage channel V is 1.0065.

Table 10. Voltage Channel W

AC INPUT VOLTAGE ADJUSTED AS % OF FULL SCALE (100% = 175 mV)	APPLIED INPUT VOLTAGE (V)	MEASURED INPUT VOLTAGE (V)	EXPECTED OUTPUT VOLTAGE (mV)	MEASURED OUTPUT VOLTAGE (mV)	ERROR
3%	9	9.00163	42.668	42.438	0.12%
5%	15	15.0017	71.109	70.657	0.02%
10%	30	30.0018	142.211	141.267	–0.01%
20%	60	60.0018	284.413	282.49	–0.02%
30%	90	90.0017	426.615	423.771	–0.01%
41%	120	120.005	568.833	565.124	0.00%
51%	150	150.006	711.040	706.515	0.02%
61%	180	180.013	853.275	847.957	0.03%
71%	210	210.005	995.440	989.508	0.06%
81%	240	240.01	1137.666	1131.056	0.08%
91%	270	270.013	1279.882	1272.63	0.09%
102%	300	300.013	1422.084	1413.99	0.09%
112%	330	330.006	1564.253	1555.34	0.09%
122%	360	360.016	1706.503	1697.36	0.12%

The gain factor for this voltage channel W is 1.0066.

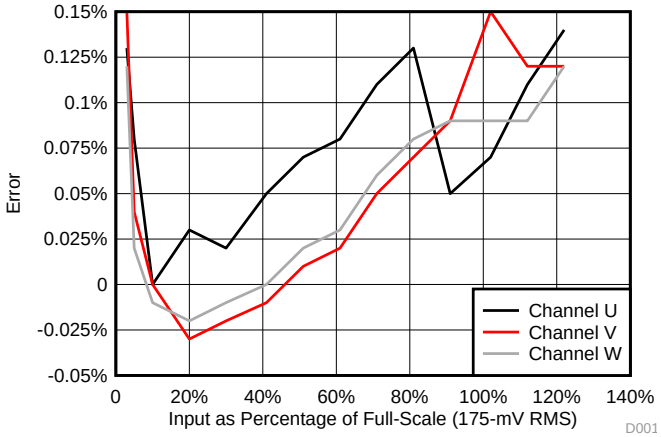


Figure 24. Voltage Measurement Error for U, V, and W Channels

7.2.1.2 Accuracy Testing at 60 Hz

The AMC1100 output voltage is measured with a 6½ digital multimeter (DMM). The error is calculated for the measured output voltage versus the expected output voltage. The gain factor and offset has been applied for error calculation.

Table 11, Table 12, and Table 13 show the measured accuracy of three voltage channels. Figure 25 shows a plot of the complete voltage channel accuracy.

Table 11. Voltage Channel U

AC INPUT VOLTAGE ADJUSTED AS % OF FULL SCALE (100% = 175 mV)	APPLIED INPUT VOLTAGE (V)	MEASURED INPUT VOLTAGE (V)	EXPECTED OUTPUT VOLTAGE (mV)	MEASURED OUTPUT VOLTAGE (mV)	ERROR
2%	6	6.0189	28.530	28.3619	0.15%
5%	15	15.0016	71.109	70.6535	0.10%
10%	30	30.0009	142.207	141.163	0.00%
51%	150	150.005	711.035	706.378	0.08%
102%	300	300.003	1422.037	1412.75	0.08%
122%	360	360.021	1706.527	1696.64	0.16%

The gain factor for this voltage channel U is 1.0074.

Table 12. Voltage Channel V

AC INPUT VOLTAGE ADJUSTED AS % OF FULL SCALE (100% = 175 mV)	APPLIED INPUT VOLTAGE (V)	MEASURED INPUT VOLTAGE (V)	EXPECTED OUTPUT VOLTAGE (mV)	MEASURED OUTPUT VOLTAGE (mV)	ERROR
2%	6	6.0189	28.530	28.4032	0.08%
5%	15	15.0016	71.109	70.6985	0.01%
10%	30	30.0009	142.207	141.317	–0.02%
51%	150	150.005	711.035	706.563	–0.01%
102%	300	300.003	1422.037	1414.13	0.07%
122%	360	360.021	1706.527	1697.71	0.11%

The gain factor for this voltage channel V is 1.0063.

Table 13. Voltage Channel W

AC INPUT VOLTAGE ADJUSTED AS % OF FULL SCALE (100% = 175 mV)	APPLIED INPUT VOLTAGE (V)	MEASURED INPUT VOLTAGE (V)	EXPECTED OUTPUT VOLTAGE (mV)	MEASURED OUTPUT VOLTAGE (mV)	ERROR
2%	6	6.0189	28.530	28.3506	0.00%
5%	15	15.0016	71.109	70.6781	0.04%
10%	30	30.0009	142.207	141.277	0.00%
51%	150	150.005	711.035	706.567	0.03%
102%	300	300.003	1422.037	1414.15	0.10%
122%	360	360.021	1706.527	1697.46	0.12%

The gain factor for this voltage channel W is 1.0066.

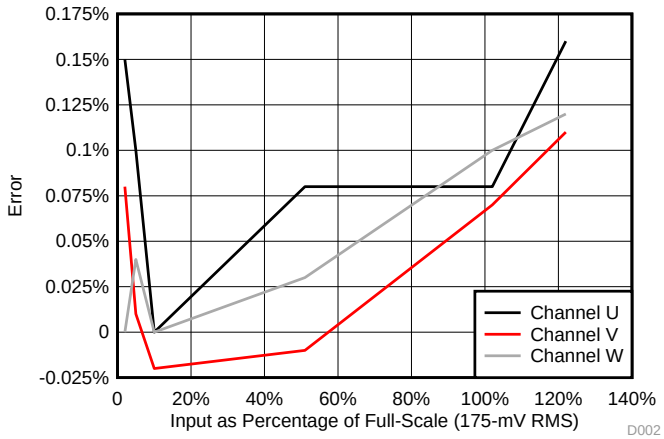


Figure 25. Voltage Measurement Error for U, V, and W Channels

7.2.2 Accuracy Test (Amplifier Output) for Current Inputs

The AMC1100 output voltage is measured with a 6½ DMM. The error is calculated for the measured output voltage versus the expected output voltage. The gain factor and offset have been applied for error calculation.

7.2.2.1 Accuracy Testing at 50 Hz

Table 14. Current Channel U

AC INPUT CURRENT ADJUSTED AS % OF FULL SCALE (100% = 175 mV)	APPLIED INPUT CURRENT (A)	MEASURED INPUT CURRENT (A)	EXPECTED OUTPUT VOLTAGE (mV)	MEASURED OUTPUT VOLTAGE (mV)	ERROR
3%	1.74	1.74176	41.802	41.691	–0.07%
5%	2.9	2.9098	69.835	69.561	–0.19%
10%	5.8	5.80215	139.252	138.857	–0.08%
20%	11.6	11.619	278.856	277.915	–0.14%
30%	17.4	17.4092	417.821	416.98	0.00%
40%	23.3	23.3033	559.279	557.789	–0.07%
50%	29	29.0385	696.924	694.879	–0.09%
60%	34.8	34.8134	835.522	833.262	–0.07%
70%	40.69	40.747	977.928	975.537	–0.04%

The gain factor for this current channel U is 1.002 and the offset voltage is 0 mV.

Table 15. Current Channel V

AC INPUT CURRENT ADJUSTED AS % OF FULL SCALE (100% = 175 mV)	APPLIED INPUT CURRENT (A)	MEASURED INPUT CURRENT (A)	EXPECTED OUTPUT VOLTAGE (mV)	MEASURED OUTPUT VOLTAGE (mV)	ERROR
3%	1.74	1.74171	41.801	41.728	–0.02%
5%	2.9	2.90179	69.643	69.479	–0.02%
10%	5.8	5.80121	139.229	138.838	–0.02%
20%	11.6	11.6122	278.693	277.605	–0.11%
30%	17.4	17.4205	418.092	416.175	–0.17%
40%	23.3	23.3249	559.798	557.137	–0.19%
50%	29	29.0096	696.230	693.506	–0.10%
60%	34.8	34.8485	836.364	832.984	–0.11%
70%	40.69	40.7023	976.855	973.8212	–0.02%

The gain factor for this current channel V is 1.003 and the offset voltage is 0.1 mV.

Table 16. Current Channel W

AC INPUT CURRENT ADJUSTED AS % OF FULL SCALE (100% = 175 mV)	APPLIED INPUT CURRENT (A)	MEASURED INPUT CURRENT (A)	EXPECTED OUTPUT VOLTAGE (mV)	MEASURED OUTPUT VOLTAGE (mV)	ERROR
3%	1.74	1.7419	41.806	41.613	0.05%
5%	2.9	2.90163	69.639	69.28	0.09%
10%	5.8	5.80164	139.239	138.423	0.09%
20%	11.6	11.6112	278.669	276.661	–0.01%
30%	17.4	17.4133	417.919	414.7402	–0.04%
40%	23.3	23.3168	559.603	555.307	–0.04%
50%	29	29.0031	696.074	691.087	0.01%
60%	34.8	34.7942	835.061	829.5899	0.08%
70%	40.69	40.7166	977.198	970.394	0.04%

The gain factor for this current channel W is 1.0075 and the offset voltage is 0.1 mV.

7.2.2.2 Accuracy Testing at 60 Hz

Table 17 shows the measured accuracy for current input.

Table 17. Current Channel U

AC INPUT CURRENT ADJUSTED AS % OF FULL SCALE (100% = 175 mV)	APPLIED INPUT CURRENT (A)	MEASURED INPUT CURRENT (A)	EXPECTED OUTPUT VOLTAGE (mV)	MEASURED OUTPUT VOLTAGE (mV)	ERROR
5%	2.9	2.90186	69.645	69.5134	0.08%
10%	5.8	5.80084	139.220	138.858	0.01%
30%	17.4	17.4091	417.818	416.395	–0.07%
50%	29	29.0187	696.449	693.819	–0.11%

The gain factor for this current channel U is 1.0027.

7.2.3 Accuracy Measurement With ADS131E08EVM-PDK

The ADS131E08 EVM is set to capture 4000 samples per channel for all the selected channels simultaneously. The sampling rate for all the selected channels is set to 4000 samples per second.

7.2.3.1 Voltage Inputs

The AMC1100 voltage output channel outputs are interfaced with the ADS131E08EVM-PDK. The ADC readings are captured using the GUI. The error is calculated for the measured output voltage versus the expected output voltage. The gain factor and offset are considered for error calculation.

7.2.3.1.1 Accuracy Testing at 50 Hz

Table 18, Table 19, and Table 20 show the measured accuracy of three voltage channels interfaced with the ADS131E08 EVM at 50 Hz. Figure 26 shows a plot of the complete voltage channel accuracy.

Table 18. Voltage Channel U

AC INPUT VOLTAGE ADJUSTED AS % OF FULL SCALE (100% = 175 mV)	APPLIED INPUT VOLTAGE (V)	MEASURED INPUT VOLTAGE (V)	EXPECTED OUTPUT VOLTAGE (mV)	MEASURED OUTPUT VOLTAGE (mV)	ERROR
3%	9	9.00191	42.670	42.379363	0.02%
5%	15	15.0012	71.107	70.644618	0.02%
10%	30	30.0016	142.210	141.31064	0.01%
20%	60	60.001	284.409	282.60711	0.00%
30%	90	90.002	426.616	423.93822	0.01%
41%	120	120.003	568.823	565.30856	0.01%
51%	150	150.003	711.026	706.70846	0.02%
61%	180	180.014	853.280	848.06935	0.02%
71%	210	210.01	995.463	989.55665	0.04%
81%	240	240.011	1137.670	1131.085	0.05%
91%	270	270.011	1279.873	1272.619	0.06%
102%	300	300.01	1422.070	1414.716	0.11%
112%	330	330.013	1564.287	1560.785	0.41%
122%	360	360.007	1706.460	1704.688	0.53%

The gain factor for this voltage channel U is 1.0063 and the offset voltage is –0.03 mV.

Table 19. Voltage Channel V

AC INPUT VOLTAGE ADJUSTED AS % OF FULL SCALE (100% = 175 mV)	APPLIED INPUT VOLTAGE (V)	MEASURED INPUT VOLTAGE (V)	EXPECTED OUTPUT VOLTAGE (mV)	MEASURED OUTPUT VOLTAGE (mV)	ERROR
3%	9	9.00191	42.670	42.440106	0.10%
5%	15	15.0012	71.107	70.687369	0.05%
10%	30	30.0016	142.210	141.31216	0.00%
20%	60	60.001	284.409	282.59258	0.00%
30%	90	90.002	426.616	423.91904	0.00%
41%	120	120.003	568.823	565.2852	0.01%
51%	150	150.003	711.026	706.66896	0.02%
61%	180	180.014	853.280	848.05075	0.02%
71%	210	210.01	995.463	989.54322	0.04%
81%	240	240.011	1137.670	1131.092	0.06%
91%	270	270.011	1279.873	1272.681	0.07%
102%	300	300.01	1422.070	1415.007	0.14%
112%	330	330.013	1564.287	1559.042	0.30%
122%	360	360.007	1706.460	1701.568	0.35%

The gain factor for this voltage channel V is 1.0064.

Table 20. Voltage Channel W

AC INPUT VOLTAGE ADJUSTED AS % OF FULL SCALE (100% = 175 mV)	APPLIED INPUT VOLTAGE (V)	MEASURED INPUT VOLTAGE (V)	EXPECTED OUTPUT VOLTAGE (mV)	MEASURED OUTPUT VOLTAGE (mV)	ERROR
3%	9	9.00191	42.670	42.431612	0.04%
5%	15	15.0012	71.107	70.668776	–0.02%
10%	30	30.0016	142.210	141.27833	–0.06%
20%	60	60.001	284.409	282.5431	–0.06%
30%	90	90.002	426.616	423.82926	–0.06%
41%	120	120.003	568.823	565.19325	–0.04%
51%	150	150.003	711.026	706.57305	–0.03%
61%	180	180.014	853.280	847.91399	–0.03%
71%	210	210.01	995.463	989.42785	–0.01%
81%	240	240.011	1137.670	1130.977	0.01%
91%	270	270.011	1279.873	1272.658	0.03%
102%	300	300.01	1422.070	1415.515	0.14%
112%	330	330.013	1564.287	1559.402	0.29%
122%	360	360.007	1706.460	1701.654	0.32%

The gain factor for this voltage channel W is 1.0060.

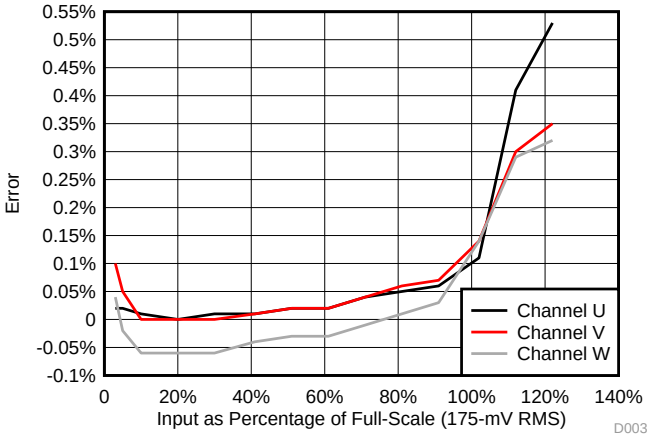


Figure 26. Voltage Measurement Error for U, V, and W Channels

7.2.3.1.2 Accuracy Testing at 60 Hz

Table 21, Table 22, and Table 23 show the measured accuracy of three voltage channels interfaced with the ADS131E08 EVM at 60 Hz. Figure 27 shows a plot of the complete voltage channel accuracy.

Table 21. Voltage Channel U

AC INPUT VOLTAGE ADJUSTED AS % OF FULL SCALE (100% = 175 mV)	APPLIED INPUT VOLTAGE (V)	MEASURED INPUT VOLTAGE (V)	EXPECTED OUTPUT VOLTAGE (mV)	MEASURED OUTPUT VOLTAGE (mV)	ERROR
2%	6	5.99894	28.435	28.235	–0.06%
3%	10	9.99875	47.395	47.053	–0.08%
10%	30	29.9989	142.197	141.167	–0.08%
51%	150	149.998	711.002	706.138	–0.04%
102%	300	299.996	1422.004	1413.426	0.04%
122%	360	359.995	1706.404	1696.782	0.08%

The gain factor for this voltage channel U is 1.0065.

Table 22. Voltage Channel V

AC INPUT VOLTAGE ADJUSTED AS % OF FULL SCALE (100% = 175 mV)	APPLIED INPUT VOLTAGE (V)	MEASURED INPUT VOLTAGE (V)	EXPECTED OUTPUT VOLTAGE (mV)	MEASURED OUTPUT VOLTAGE (mV)	ERROR
2%	6	5.99894	28.435	28.231	–0.09%
3%	15	9.99875	47.395	47.055	–0.09%
10%	30	29.9989	142.197	141.183	–0.09%
51%	150	149.998	711.002	706.256	–0.04%
102%	300	299.996	1422.004	1413.663	0.04%
122%	360	359.995	1706.404	1696.919	0.07%

The gain factor for this voltage channel V is 1.0063.

Table 23. Voltage Channel W

AC INPUT VOLTAGE ADJUSTED AS % OF FULL SCALE (100% = 175 mV)	APPLIED INPUT VOLTAGE (V)	MEASURED INPUT VOLTAGE (V)	EXPECTED OUTPUT VOLTAGE (mV)	MEASURED OUTPUT VOLTAGE (mV)	ERROR
2%	6	5.99894	28.435	28.240	–0.03%
3%	15	9.99875	47.395	47.052	–0.07%
10%	30	29.9989	142.197	141.153	–0.08%
51%	150	149.998	711.002	706.080	–0.04%
102%	300	299.996	1422.004	1413.257	0.04%
122%	360	359.995	1706.404	1696.422	0.07%

The gain factor for this voltage channel W is 1.0066.

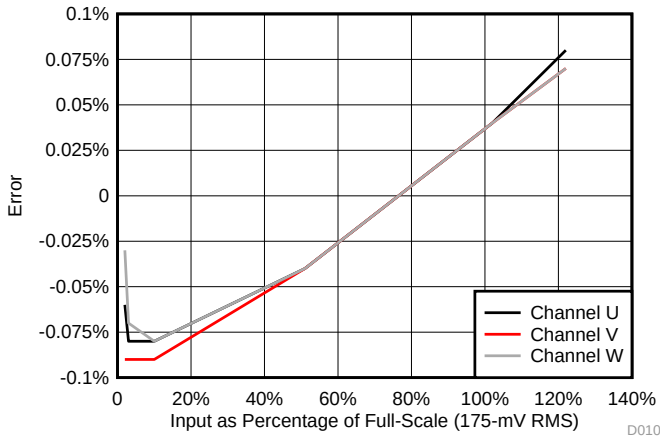


Figure 27. Voltage Measurement Error for U, V, and W Channels

7.2.3.2 Current Channels

The current is applied to the TIDA-00555 board. The AMC1100 device output is interfaced with the ADS131E08EVM-PDK. The voltage is measured with the help of GUI. The error is calculated for the measured output voltage versus the expected output voltage. The gain factor and offset are considered for error calculation.

7.2.3.2.1 Accuracy Testing at 50 Hz

Table 24, Table 25, and Table 26 show the measured accuracy of three current channels interfaced with the ADS131E08 EVM at 50 Hz. Figure 28 shows a plot of the current channels accuracy.

Table 24. Current Channel U

AC INPUT CURRENT ADJUSTED AS % OF FULL SCALE (100% = 175 mV)	APPLIED INPUT CURRENT (A)	MEASURED INPUT CURRENT (A)	EXPECTED OUTPUT VOLTAGE (mV)	MEASURED OUTPUT VOLTAGE (mV)	ERROR
3%	1.74	1.742	41.808	41.820999	0.03%
5%	2.9	2.90205	69.649	69.714486	0.09%
10%	5.8	5.80095	139.223	139.3378	0.08%
20%	11.6	11.6226	278.942	278.84538	–0.03%
30%	17.4	17.4269	418.246	417.99734	–0.06%
40%	23.3	23.3276	559.862	559.47625	–0.07%
50%	29	29.0402	696.965	696.40271	–0.08%
60%	34.8	34.8308	835.939	835.70755	–0.03%
70%	40.69	40.7069	976.966	977.75811	0.08%

The gain factor for this current channel U is 1.

Table 25. Current Channel V

AC INPUT CURRENT ADJUSTED AS % OF FULL SCALE (100% = 175 mV)	APPLIED INPUT CURRENT (A)	MEASURED INPUT CURRENT (A)	EXPECTED OUTPUT VOLTAGE (mV)	MEASURED OUTPUT VOLTAGE (mV)	ERROR
3%	1.74	1.74185	41.804	41.682783	–0.09%
5%	2.9	2.9019	69.646	69.501195	–0.01%
10%	5.8	5.80164	139.239	138.9524	–0.01%
20%	11.6	11.6185	278.844	277.98499	–0.11%
30%	17.4	17.4127	417.905	416.66374	–0.10%
40%	23.3	23.3034	559.282	557.85246	–0.06%
50%	29	29.0295	696.708	694.17819	–0.16%
60%	34.8	34.8232	835.757	832.92478	–0.14%
70%	40.69	40.6919	976.606	974.92866	0.03%

The gain factor for this current channel V is 1.002.

Table 26. Current Channel W

AC INPUT CURRENT ADJUSTED AS % OF FULL SCALE (100% = 175 mV)	APPLIED INPUT CURRENT (A)	MEASURED INPUT CURRENT (A)	EXPECTED OUTPUT VOLTAGE (mV)	MEASURED OUTPUT VOLTAGE (mV)	ERROR
3%	1.74	1.74195	41.807	41.800349	–0.02%
5%	2.9	2.90174	69.642	69.679989	0.05%
10%	5.8	5.80167	139.240	139.3155	0.05%
20%	11.6	11.6113	278.671	278.72151	0.02%
30%	17.4	17.4101	417.842	417.75809	–0.02%
40%	23.3	23.3165	559.596	559.23481	–0.06%
50%	29	29.0204	696.490	695.82914	–0.09%
60%	34.8	34.8236	835.766	835.13199	–0.08%
70%	40.69	40.6931	976.634	977.22413	0.06%

The gain factor for this current channel W is 1.

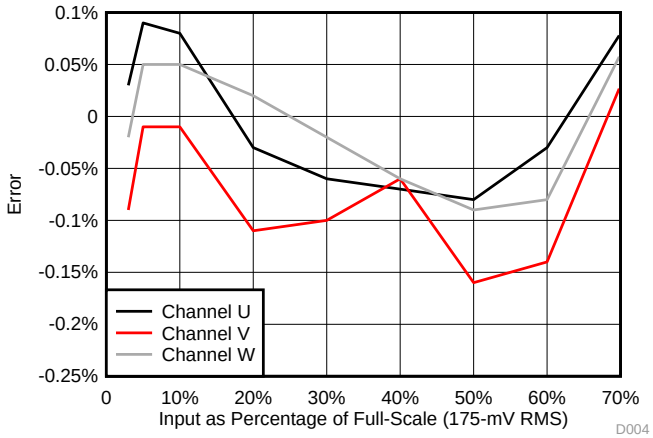


Figure 28. Current Measurement Error for U, V, and W Channels

7.2.3.2.2 Accuracy Testing at 60 Hz

Table 27, Table 28, and Table 29 show the measured accuracy of three current channels interfaced with the ADS131E08 EVM at 60 Hz. Figure 29 shows a plot of the current channels accuracy.

Table 27. Current Channel U

AC INPUT CURRENT ADJUSTED AS % OF FULL SCALE (100% = 175 mV)	APPLIED INPUT CURRENT (A)	MEASURED INPUT CURRENT (A)	EXPECTED OUTPUT VOLTAGE (mV)	MEASURED OUTPUT VOLTAGE (mV)	ERROR
5%	2.9	2.90181	69.643	69.73167	0.05%
10%	5.8	5.80172	139.241	139.375	0.06%
30%	17.4	17.4179	418.030	417.8353	–0.06%
50%	29	29.0169	696.406	696.0715	–0.06%

The gain factor for this current channel U is 1 and the offset voltage is 0.05 mV.

Table 28. Current Channel V

AC INPUT CURRENT ADJUSTED AS % OF FULL SCALE (100% = 175 mV)	APPLIED INPUT CURRENT (A)	MEASURED INPUT CURRENT (A)	EXPECTED OUTPUT VOLTAGE (mV)	MEASURED OUTPUT VOLTAGE (mV)	ERROR
5%	2.9	2.90179	69.643	69.49884	–0.01%
10%	5.8	5.80185	139.244	138.949	–0.01%
30%	17.4	17.418	418.032	416.5698	–0.15%
50%	29	29.0181	696.434	693.9939	–0.15%

The gain factor for this current channel V is 1.002.

Table 29. Current Channel W

AC INPUT CURRENT ADJUSTED AS % OF FULL SCALE (100% = 175 mV)	APPLIED INPUT CURRENT (A)	MEASURED INPUT CURRENT (A)	EXPECTED OUTPUT VOLTAGE (mV)	MEASURED OUTPUT VOLTAGE (mV)	ERROR
5%	2.9	2.90177	69.642	69.67551	0.03%
10%	5.8	5.80194	139.247	139.2847	0.02%
30%	17.4	17.4171	418.010	417.623	–0.10%
50%	29	29.0181	696.434	695.6959	–0.11%

The gain factor for this current channel W is 1.

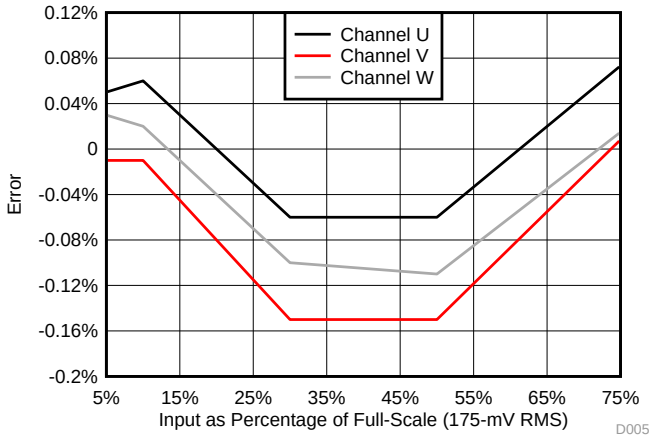


Figure 29. Current Measurement Error for U, V, and W Channels

7.2.4 Accuracy Testing With AMC1100 Interfaced to MSP430FR5869

As Table 6 notes, the jumper settings must be set for the MCU interfacing mode and the AMC_VCC must be set to 3.3 V. Figure 23 shows the test setup for testing the MSP430FR5869.

A test code is used to capture the samples. The voltages and currents are applied to the AMC1100 inputs. The measured data is monitored using the watch window in TI's Code Composer Studio™ software.

Table 30. Current Channel U

AC INPUT CURRENT ADJUSTED AS % OF FULL SCALE (100% = 175 mV)	INPUT CURRENT (A)	MEASURED INPUT CURRENT (A)	EXPECTED OUTPUT VOLTAGE (mV)	MEASURED OUTPUT VOLTAGE (mV)	ERROR
5%	2.9	2.90161	69.63864	68.35082	–0.09%
10%	5.8	5.8023	139.2552	137.1446	0.11%
30%	17.4	17.4184	418.0416	410.9592	–0.17%
61%	34.8	34.8254	835.8096	824.2146	0.12%

The gain factor for this current channel U is 1.015 and the offset voltage is –0.2 mV.

Table 31. Voltage Channel U

AC INPUT VOLTAGE ADJUSTED AS % OF FULL SCALE (100% = 175 mV)	INPUT VOLTAGE (V)	MEASURED INPUT VOLTAGE (V)	EXPECTED OUTPUT VOLTAGE (mV)	MEASURED OUTPUT VOLTAGE (mV)	ERROR
5%	15	15.0014	71.10777	69.087	0.09%
10%	30	30.0028	142.2155	139.1089	0.26%
30%	90	90.0073	426.6414	417.9469	0.09%
61%	180	180.011	853.2658	836.0237	0.02%

The gain factor for this current channel U is 1.02 and the offset voltage is –0.7 mV.

Table 32. Current Channel V

AC INPUT CURRENT ADJUSTED AS % OF FULL SCALE (100% = 175 mV)	INPUT CURRENT (A)	MEASURED INPUT CURRENT (A)	EXPECTED OUTPUT VOLTAGE (mV)	MEASURED OUTPUT VOLTAGE (mV)	ERROR
5%	2.9	2.90166	69.640	67.88915	–0.13%
10%	5.8	5.80197	139.247	135.9357	–0.21%
30%	17.4	17.4207	418.097	409.4901	–0.03%
60%	34.8	34.7998	835.195	817.7155	–0.10%

The gain factor for this current channel V is 1.02 and the offset voltage is –0.3 mV.

Table 33. Voltage Channel V

AC INPUT VOLTAGE ADJUSTED AS % OF FULL SCALE (100% = 175 mV)	INPUT VOLTAGE (V)	MEASURED INPUT VOLTAGE (V)	EXPECTED OUTPUT VOLTAGE (mV)	MEASURED OUTPUT VOLTAGE (mV)	ERROR
5%	15	15.0022	71.112	69.21503	–0.21%
10%	30	30.0023	142.213	138.9232	–0.20%
30%	90	90.0036	426.624	417.0604	–0.36%
61%	180	180.0035	853.230	836.8823	–0.09%

The gain factor for this voltage channel V is 1.018 and the offset voltage is –0.5 mV.

Table 34. Current Channel W

AC INPUT CURRENT ADJUSTED AS % OF FULL SCALE (100% = 175 mV)	INPUT CURRENT (A)	MEASURED INPUT CURRENT (A)	EXPECTED OUTPUT VOLTAGE (mV)	MEASURED OUTPUT VOLTAGE (mV)	ERROR
5%	2.9	2.90163	69.639	67.9379	–0.06%
10%	5.8	5.80137	139.233	136.1316	0.09%
30%	17.4	17.4133	417.919	407.8141	–0.15%
60%	34.8	34.7942	835.061	815.5334	–0.08%

The gain factor for this current channel U is 1.023 and the offset voltage is 0.015 mV.

Table 35. Voltage Channel W

AC INPUT VOLTAGE ADJUSTED AS % OF FULL SCALE (100% = 175 mV)	INPUT VOLTAGE (V)	MEASURED INPUT VOLTAGE (V)	EXPECTED OUTPUT VOLTAGE (mV)	MEASURED OUTPUT VOLTAGE (mV)	ERROR
5%	15	15.0017	71.109	69.01031	–0.02%
10%	30	30.0019	142.211	138.344	–0.13%
30%	90	90.0014	426.613	416.974	0.11%
61%	180	180.008	853.252	834.5764	0.12%

The gain factor for this voltage channel W is 1.023 and the offset voltage is –0.5 mV.

7.2.5 Additional Testing

The TIDA-00555 design can also be used to measure DC or a 400-Hz signal.

7.2.5.1 Accuracy Testing at 400 Hz

Table 36, Table 37, and Table 38 show the measured accuracy of three voltage channels tested with a 400-Hz input. Figure 30 shows a plot of the voltage channel accuracy at 400 Hz.

Table 36. Voltage Channel U

AC INPUT VOLTAGE ADJUSTED AS % OF FULL SCALE (100% = 175 mV)	APPLIED INPUT VOLTAGE (V)	MEASURED INPUT VOLTAGE (V)	EXPECTED OUTPUT VOLTAGE (mV)	MEASURED OUTPUT VOLTAGE (mV)	ERROR
5%	15	15.0017	71.109	70.6745	0.09%
10%	30	30.0019	142.211	141.196	0.00%
51%	150	150.005	711.035	706.574	0.10%
102%	300	300.014	1422.089	1413.21	0.10%
122%	360	360.023	1706.536	1697.15	0.18%

The gain factor for this voltage channel U is 1.0073 and the offset voltage is 0.015 mV.

Table 37. Voltage Channel V

AC INPUT VOLTAGE ADJUSTED AS % OF FULL SCALE (100% = 175 mV)	APPLIED INPUT VOLTAGE (V)	MEASURED INPUT VOLTAGE (V)	EXPECTED OUTPUT VOLTAGE (mV)	MEASURED OUTPUT VOLTAGE (mV)	ERROR
5%	15	15.0017	71.109	70.7128	0.01%
10%	30	30.0019	142.211	141.318	–0.03%
51%	150	150.005	711.035	706.785	0.02%
102%	300	300.014	1422.089	1414.44	0.09%
122%	360	360.023	1706.536	1698.34	0.14%

The gain factor for this voltage channel V is 1.0063 and the offset voltage is 0.04 mV.

Table 38. Voltage Channel W

AC INPUT VOLTAGE ADJUSTED AS % OF FULL SCALE (100% = 175 mV)	APPLIED INPUT VOLTAGE (V)	MEASURED INPUT VOLTAGE (V)	EXPECTED OUTPUT VOLTAGE (mV)	MEASURED OUTPUT VOLTAGE (mV)	ERROR
5%	15	15.0017	71.109	70.6986	0.05%
10%	30	30.0019	142.211	141.314	0.00%
51%	150	150.005	711.035	706.737	0.02%
102%	300	300.014	1422.089	1414.53	0.10%
122%	360	360.023	1706.536	1697.02	0.07%

The gain factor for this voltage channel W is 1.0063.

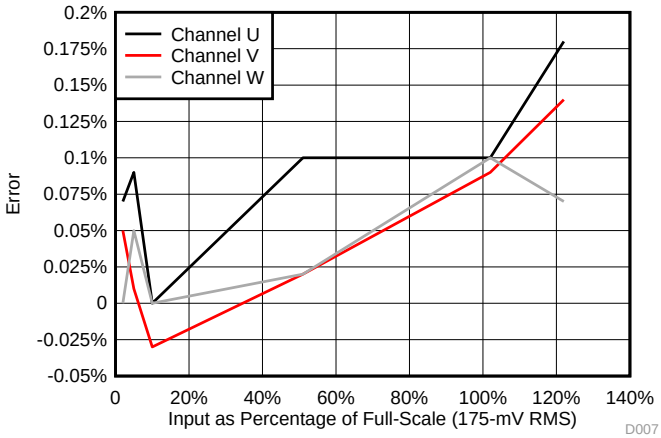


Figure 30. Voltage Measurement Error for U, V, and W Channels

7.2.5.2 *Accuracy Testing at DC Input*

Table 39, Table 40, and Table 41 show the measured accuracy of three voltage channels tested with a DC input. Figure 31 shows a plot of the voltage channel accuracy with a DC input. The DC input accuracy testing is performed with the AMC1100 device interfaced to the ADS131E08 EVM.

Table 39. Voltage Channel U

AC INPUT VOLTAGE ADJUSTED AS % OF FULL SCALE (100% = 250 mV)	APPLIED INPUT VOLTAGE (V)	MEASURED INPUT VOLTAGE (V)	EXPECTED OUTPUT VOLTAGE (mV)	MEASURED OUTPUT VOLTAGE (mV)	ERROR
5%	21	21.084	99.940	101.2081	0.02%
10%	42	42.234	200.192	200.8917	–0.02%
50%	211	210.98	1000.061	996.4314	–0.04%
80%	338	337.54	1599.965	1593.628	–0.01%

The gain factor for this voltage channel U is 1.005 and the offset voltage is 1.75 mV.

Table 40. Voltage Channel V

AC INPUT VOLTAGE ADJUSTED AS % OF FULL SCALE (100% = 250 mV)	APPLIED INPUT VOLTAGE (V)	MEASURED INPUT VOLTAGE (V)	EXPECTED OUTPUT VOLTAGE (mV)	MEASURED OUTPUT VOLTAGE (mV)	ERROR
5%	21	21.084	99.940	99.91066	–0.03%
10%	42	42.234	200.192	199.5849	–0.05%
50%	211	210.98	1000.061	995.1494	–0.04%
80%	338	337.54	1599.965	1592.601	0.01%

The gain factor for this voltage channel V is 1.005 and the offset voltage is 0.5 mV.

Table 41. Voltage Channel W

AC INPUT VOLTAGE ADJUSTED AS % OF FULL SCALE (100% = 250 mV)	APPLIED INPUT VOLTAGE (V)	MEASURED INPUT VOLTAGE (V)	EXPECTED OUTPUT VOLTAGE (mV)	MEASURED OUTPUT VOLTAGE (mV)	ERROR
5%	21	21.084	99.940	101.5924	0.01%
10%	42	42.234	200.192	201.3196	–0.01%
50%	211	210.98	1000.061	997.2441	0.00%
80%	338	337.54	1599.965	1594.77	0.04%

The gain factor for this voltage channel W is 1.005 and the offset voltage is 2.15 mV.

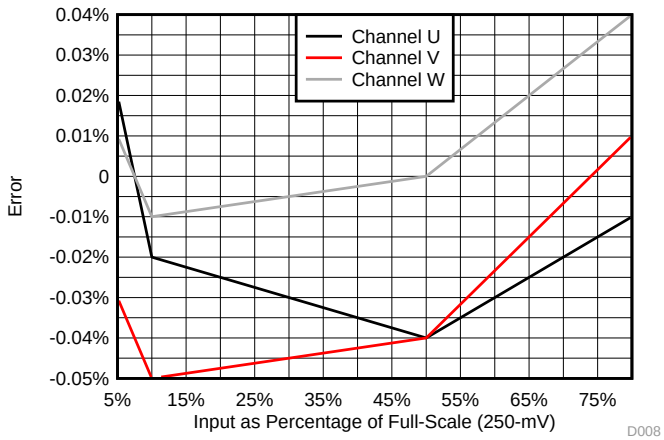


Figure 31. Voltage Measurement Error for U, V, and W Channels

Table 42 shows the measured accuracy of a current channel tested with a DC input. Figure 32 shows a plot of the current channel accuracy with a DC input. The DC input accuracy testing is performed with the AMC1100 device interfaced to the ADS131E08 EVM.

Table 42. Current Channel U

AC INPUT CURRENT ADJUSTED AS % OF FULL SCALE (100% = 250 mV)	INPUT CURRENT (A)	MEASURED INPUT CURRENT (A)	MEASURED OUTPUT VOLTAGE (mV)	GUI READING (mV)	ERROR
4%	3	3.00131	72.031	74.46	0.00%
7%	6	6.00173	144.042	146.43	–0.03%
11%	9	9.00309	216.074	218.58	0.04%

The gain factor for this current channel U is 1 and the offset voltage is 2.42856 mV.

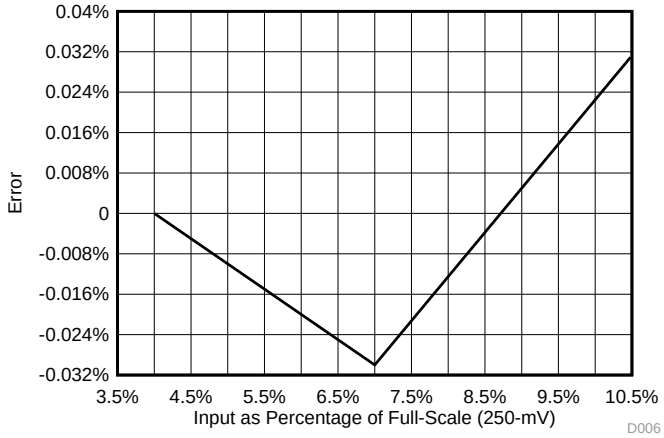


Figure 32. Current Measurement Error for U Channel

NOTE: The DC current measurements have been taken up to 9 A only because of the current source availability.

7.3 Test Results Summary

As Table 43 shows, the TIDA-00555 design meets the goal of < ±0.5% accuracy for 5% to 100% of the AMC1100 full-scale input.

Table 43. Summary of Test Results

SERIAL NUMBER	PARAMETERS	OBSERVATION
1	Isolated power supply output: +5 V, –5 V	Ok
2	Non-isolated power supply output: +3.3 V	Ok
3	Voltage measurement accuracy: 50 Hz, 60 Hz	Ok
4	Current measurement accuracy: 50 Hz, 60 Hz	Ok
5	Voltage measurement accuracy: DC, 400 Hz	Ok
6	Current measurement accuracy: DC, 400 Hz	Ok
7	ADS131E08EVM-PDK interface and measurement accuracy	Ok
8	MSP430FR5869 interface and measurement accuracy	Ok

8 Design Files

8.1 Schematics

To download the schematics for each board, see the design files at TIDA-00555.

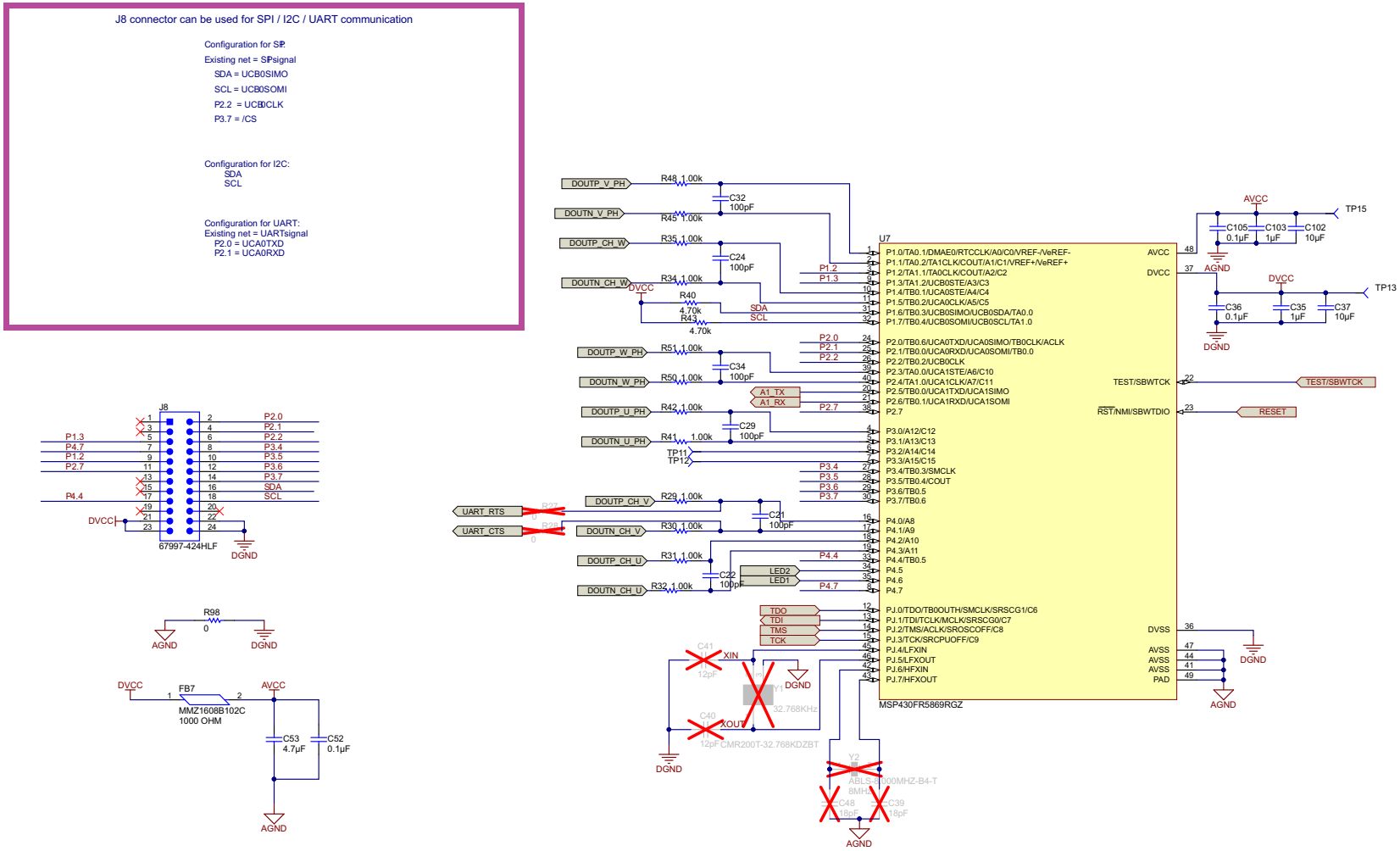


Figure 33. TIDA-00555 Schematic—MCU

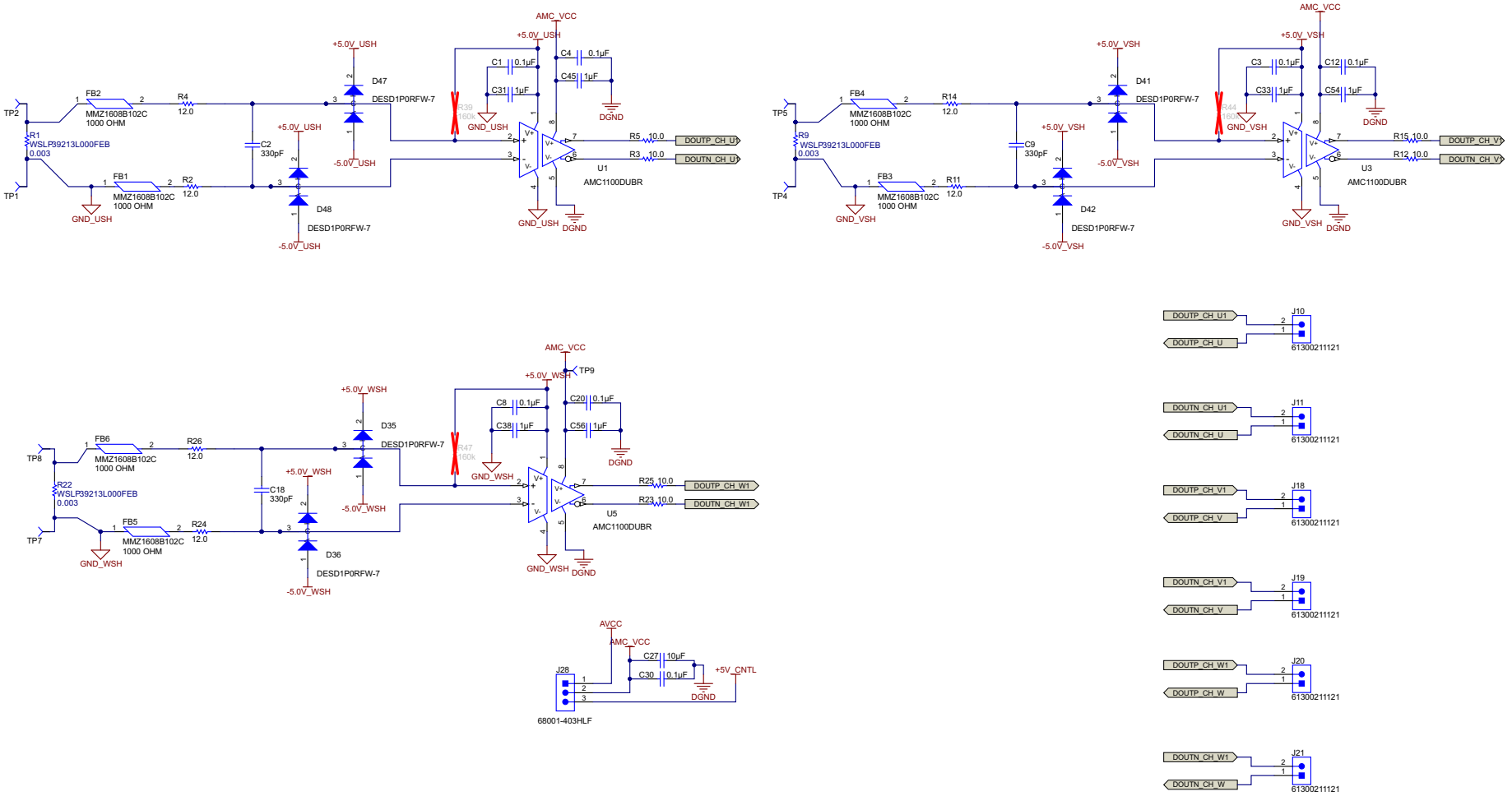


Figure 34. TIDA-00555 Schematic—Current Inputs

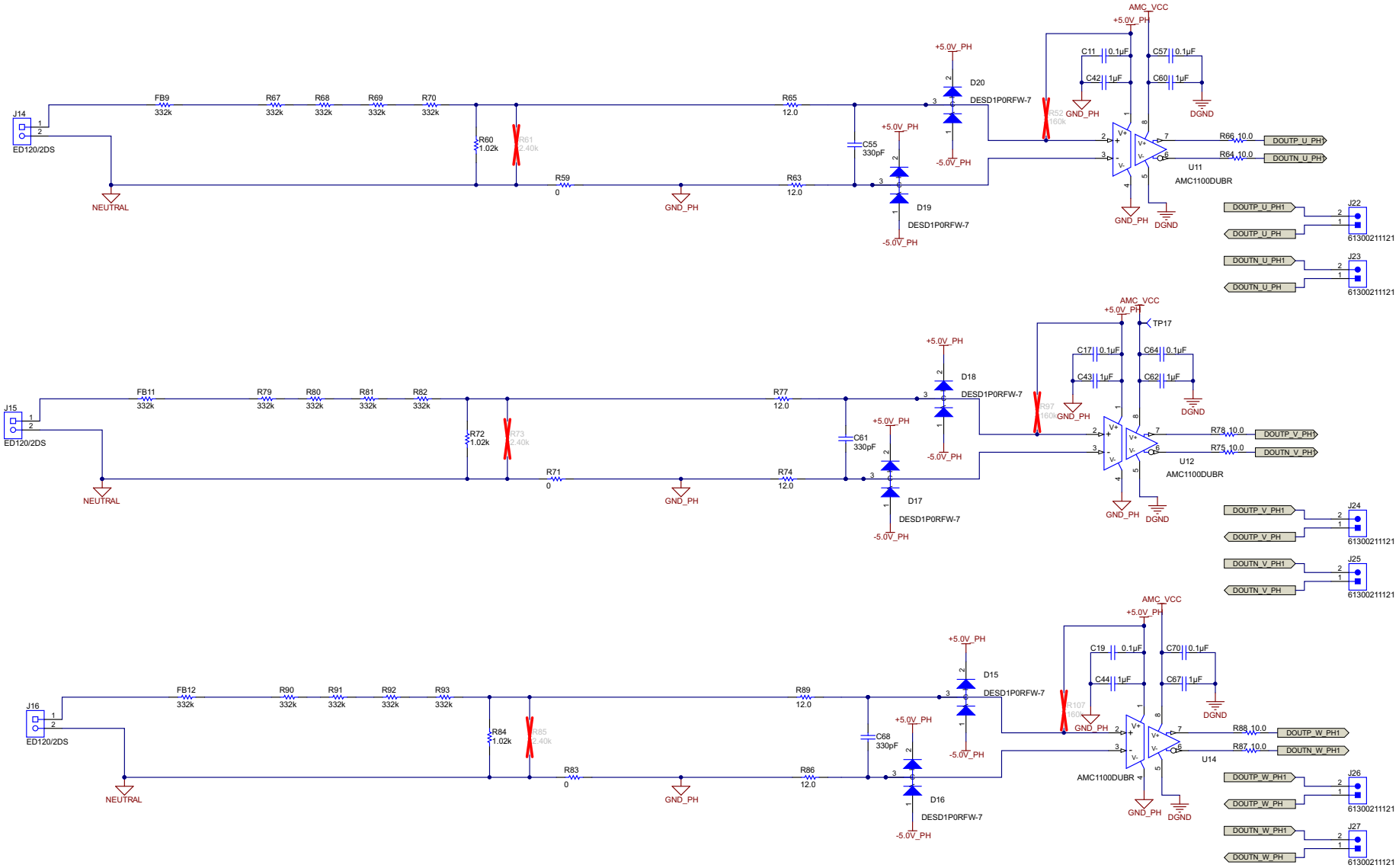


Figure 35. TIDA-00555 Schematic—Voltage Inputs

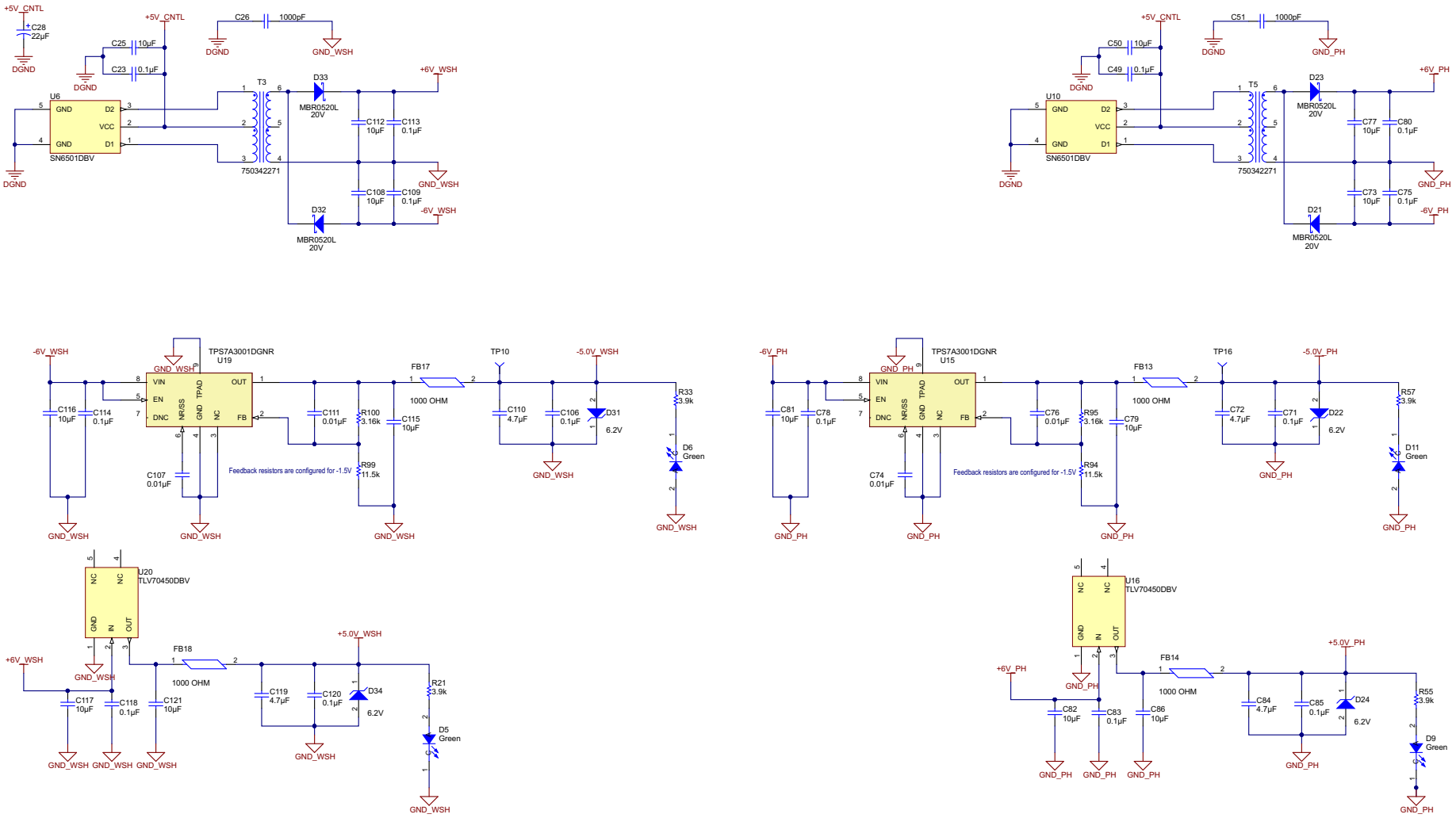


Figure 36. TIDA-00555 Schematic—Regulators

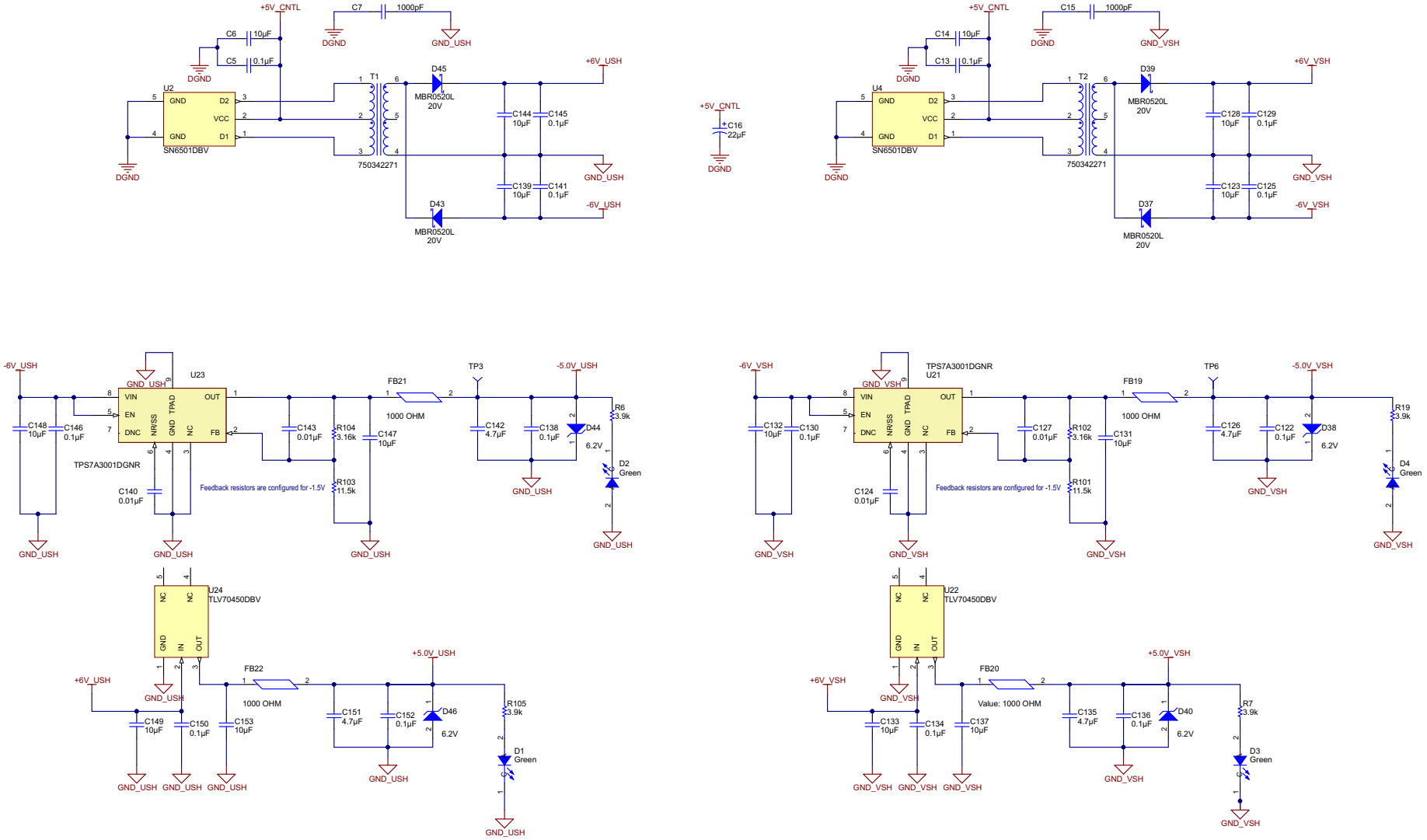


Figure 37. TIDA-00555 Schematic—Regulators

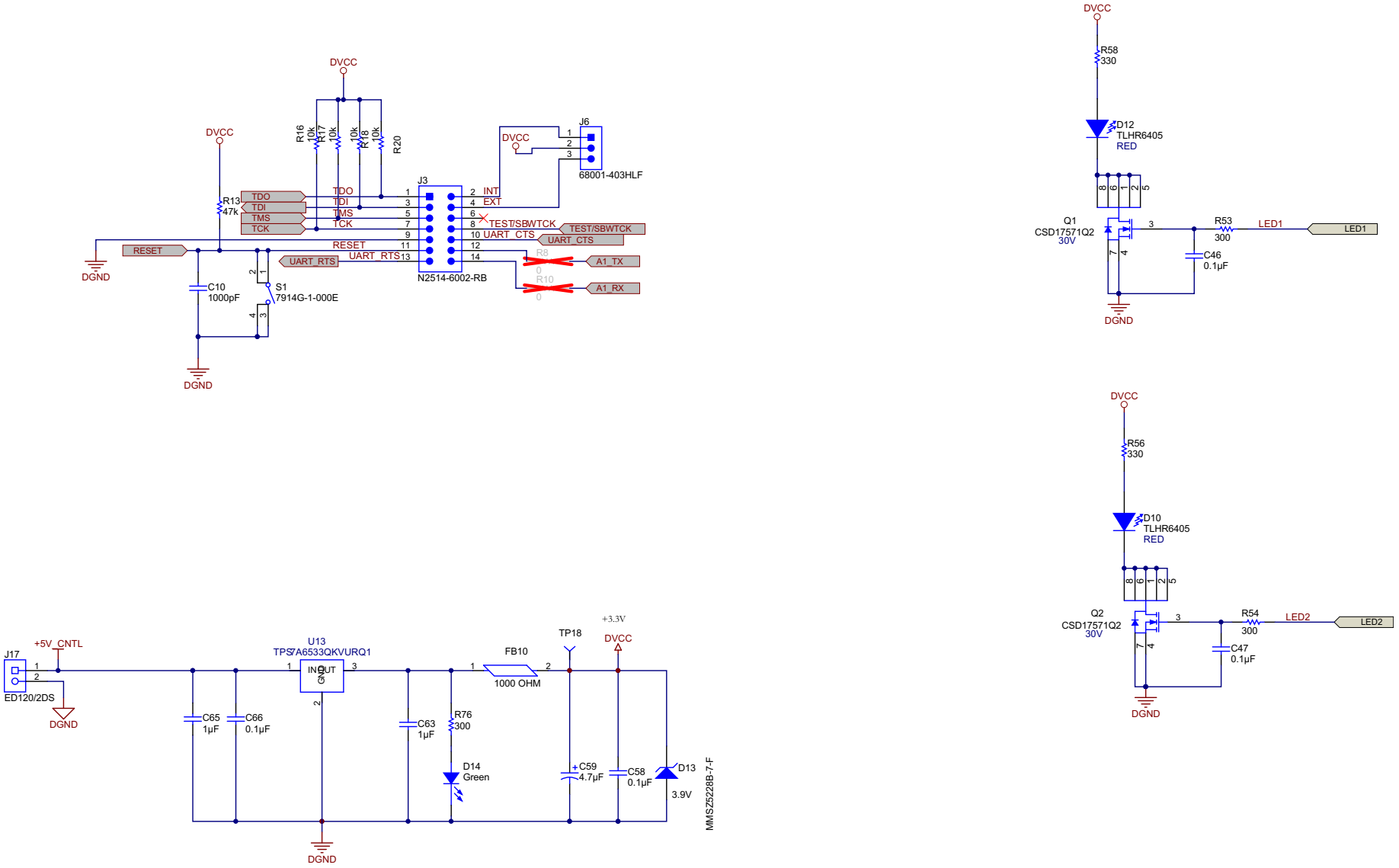


Figure 38. TIDA-00555 Schematic Page 6

8.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00555.

8.3 PCB Layout Prints

To download the layer plots, see the design files at TIDA-00555.

8.4 Altium Project

To download the Altium project files, see the design files at TIDA-00555.

8.5 PCB Routing Guidelines

8.5.1 Shunt PCB Guideline

The shunt must be placed as close together as possible to establish a direct connection between the current input trace. The shunt etch must be sized to the maximum current requirement. The sense etch should be connected between the resistor bond pads and function as a differential pair to the next stage of the isolated amplifier. With this layout, the sense voltage is measured directly across the sense and is not subject to the influence of other circuit board etch. Figure 39 shows the implemented Kelvin connection. Ensure that the shunt layout meets the expectations of this guideline to avoid compromising the accuracy of the shunt resistor measurement.

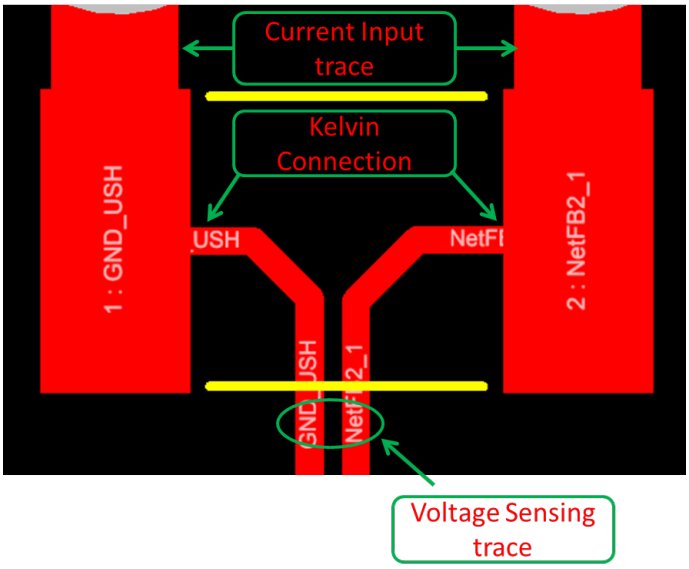


Figure 39. TIDA-00555 Shunt Layout

8.6 Gerber Files

To download the Gerber files, see the design files at TIDA-00555.

8.7 Assembly Drawings

To download the Assembly Drawings for each board, see the design files at TIDA-00555.

9 References

1. Texas Instruments, *Isolated Current (Shunt-Based) and Voltage Sensing for Smart Grid Applications*, TIDA-00080 User's Guide (TIDU429)
2. Texas Instruments, *Performance Demonstration Kit for the ADS131E08*, ADS131E08 User's Guide (SBAU200)

10 Terminology

RTU— Remote terminal unit

IED— Intelligent electronic device

CT— Current transformer

EVM— Evaluation module

ESR— Equivalent series resistance

RISC —Reduced Instruction set computing

ULP— Ultra-low power

ADC— Analog-to-digital converter

LCD— Liquid-crystal display

SVS— Supply voltage supervisor

UART— Universal asynchronous receiver/transmitter

SPI— Serial Peripheral interface

11 About the Author

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