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Rail Cleaner With Adjustable Output Voltage Drop and Soft-Start Capabilities

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TIDA-00533	Design Folder
LP38798	Product Folder

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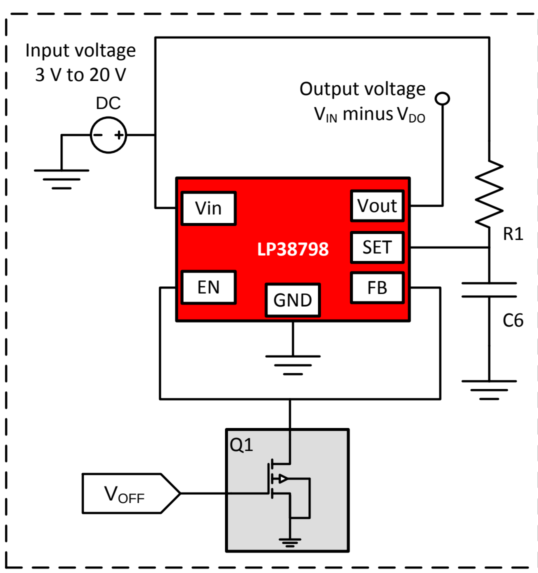
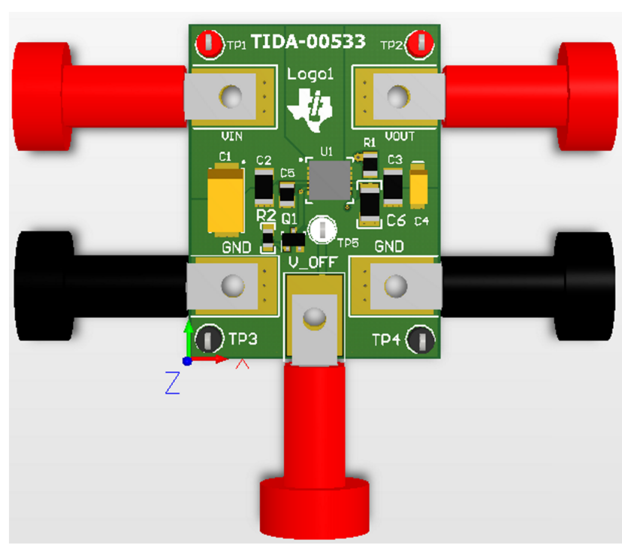
Design Features

- Low-Noise Post-Regulation Rail Ripple Cleaner
- Adjustable Output Voltage Dropout
- Output Voltage Disabled Feature
- Adjustable Soft-Startup
- Small Footprint

Featured Applications

- Personal Electronics: Set-Top Box, Audio, Portable Devices
- Communication Equipment: Audio RF, VCO Power, Wireless LAN Devices, Wireless Cable Modems, Servers





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1 Key System Specifications

Table 1. Key System Specifications

PARAMETER	SPECIFICATION	DETAILS
Voltage drop	Adjustable output voltage drop	See Section 4.1 and Section 6.3
Safety features	Current limiting Undervoltage lockout (UVLO) Thermal shutdown	See Section 4.2
Soft start	Adjustable soft start	See Section 4.3 and Section 6.4
Shut off	Output voltage disable feature with fast start after exiting the disable mode	See Section 4.4 and Section 6.5

2 System Description

The TIDA-00533 reference design features a post regulation voltage follower and rail cleaner for noise sensitive applications, with adjustable output voltage drop, adjustable soft-start, and output disable features.

These additional safety features make this solution more beneficial than a discrete rail cleaner:

- Output current limiting
- Over temperature protection
- Undervoltage lockout (UVLO)

Design characteristics:

- Minimum operating input voltage: 3 V
- Maximum operating input voltage: 20.0 V
- Output voltage: $V_{IN} - V_{DO}$
- Adjustable output voltage drop (V_{DO}): 500 mV to 1 V
- Maximum operating output current: 800 mA

3 Block Diagram

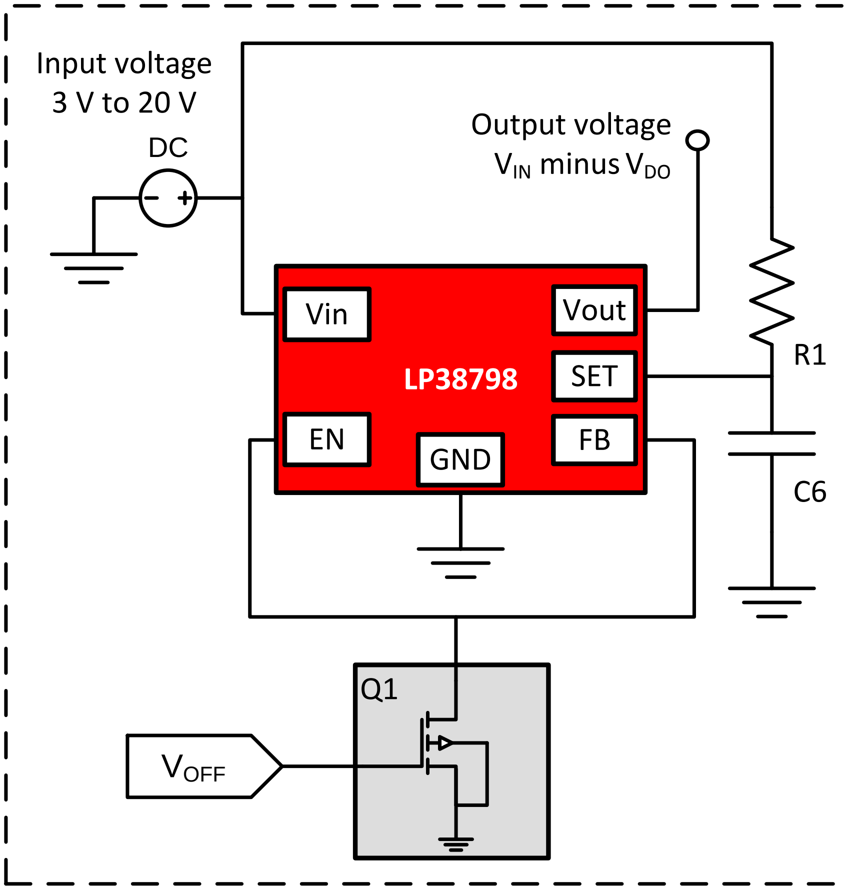

Figure 1. TIDA-00533 Block Diagram

3.1 Highlighted Devices

3.1.1 LP38798-ADJ

The LP38798-ADJ is a high-performance linear regulator capable of supplying 800 mA output current. Designed to meet the requirements of sensitive RF/Analog circuitry, the LP38798-ADJ implements a novel linear topology on an advanced CMOS process to deliver ultra-low output noise and high PSRR at switching power supply frequencies. The LP38798SD-ADJ is stable with both ceramic and tantalum output capacitors and requires a minimum output capacitance of only 1 μF for stability.

4 System Design Theory

The blue line and red line in Figure 2 represent two connections that must be made to enable the LP38798-ADJ as a voltage follower. The blue connection disables Comparator 1 by connecting the comparator's negative feedback (FB) input to the higher potential of the Enable pin (EN). The red connection sets the required voltage drop (V_{DROP}) for the rail cleaner; V_{DROP} is a function of I_{SET} and R1. Section 4.1 explains how to set the V_{DROP}.

The rail cleaner does a great job of minimizing the input noise. Any noise at the LP38798-ADJ SET pin is reduced by an internal first-order low-pass RC filter before it is passed to the output buffer stage. The low-pass filter has a –3-dB cut-off frequency of approximately 0.08 Hz. The noise introduced in the IN pins will be minimized by the Active Ripple Rejection block.

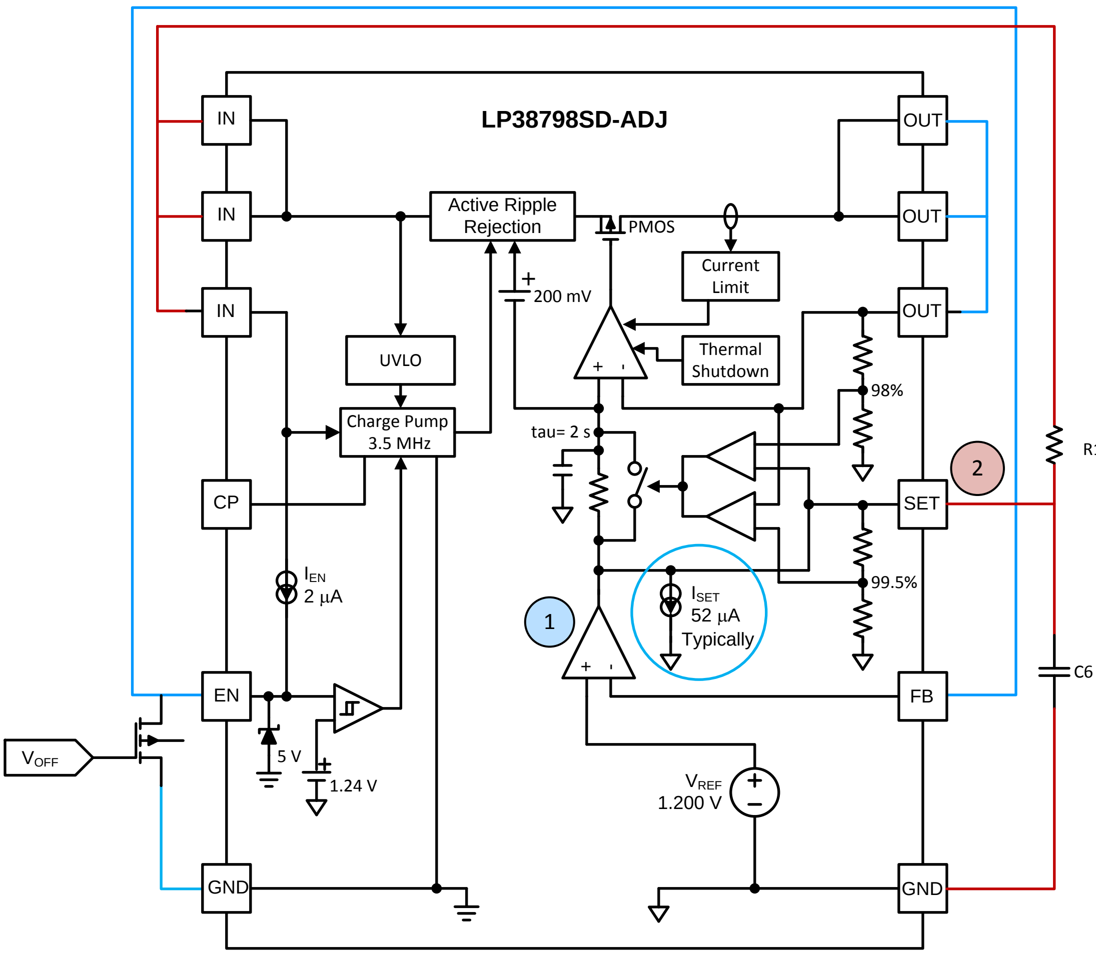

Figure 2. LP38798SD-ADJ Functional Block Diagram

4.1 Voltage Drop Setup

The input-to-output voltage drop must be at least the sum of the dropout voltage at the rated current plus the peak-to-peak ripple. Failure to set the input-to-output voltage drop to an adequate value will result in an inferior performance. The resistor R1 may be adjusted as needed to achieve the desired output voltage drop. Equation 1 determines the output voltage:

$$V_{OUT} = V_{IN} - \left(R1 \times I_{SET}\right) \tag{1}$$

Alternately, Equation 2 can determine the appropriate R1 value for a given V_{DROP}:

$$R1 = \left(\frac{V_{DROP}}{I_{SET}}\right) \tag{2}$$

The current source from the I_{SET} pin varies depending on the input voltage. An output voltage tolerance of ±5% across the input voltage range is expected if the typical I_{SET} current of 52 µA is used to calculate the voltage drop. If the application requires a more accurate output voltage at a certain input voltage range, I_{SET} can be calculated using Equation 3; however, there will be a compromise in the output voltage accuracy at lower input voltages as shown in Section 6.3.

The XY plot on Figure 3 was made using the typical I_{SET} values from the LP38798-ADJ datasheet (SNOSCT6). The plot shows a projection of the I_{SET} current at various input voltages.

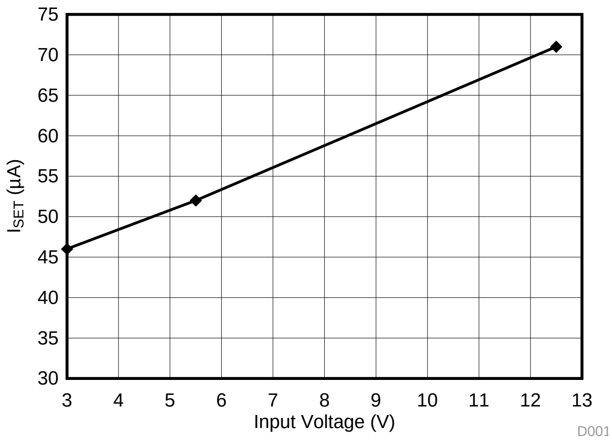

Figure 3. I_{SET} versus Input Voltage

Equation 3 was obtained from the trend line of Figure 3, which gives an approximation of the I_{SET} current at various input voltages.

$$I_{SET} = 0.0331 \times \left(V_{IN}\right)^2 + 2.1188 \times \left(V_{IN}\right) + 39.349 \tag{3}$$

4.2 Safety Features

4.2.1 Current Limiting

The LP38798-ADJ incorporates active output current limiting. The threshold for the output current limiting is set well above the ensured output operating current such that it does not interfere with normal operation.

NOTE: Output current limiting is provided as a safety feature and is outside the recommended operating conditions. Operation at the current limit is not recommended as the device junction temperature (T_J) will rise rapidly and operation will likely cross into thermal shutdown behavior.

4.2.2 UVLO

The LP38798-ADJ incorporates UVLO. The UVLO circuit monitors the input voltage and keeps the LP38798-ADJ disabled while a rising V_{IN} is less than 2.65 V (typical). The rising UVLO threshold is approximately 350 mV below the recommended minimum operating V_{IN} of 3 V.

4.2.3 Thermal Shutdown

The LP38798-ADJ includes thermal protection that will shut off the output current when activated by excessive device dissipation. Thermal shutdown (T_{SD}) occurs when the junction temperature has risen to 170°C. The junction temperature must fall typically 12°C from the shutdown temperature for the output current to be restored. Junction temperature is calculated from the formula in Equation 4:

$$T_J = T_A + \left(P_D \times R_{\theta JA}\right) \quad (4)$$

The power being dissipated, P_D, is defined by Equation 5:

$$P_D = \left(V_{IN} - V_{OUT}\right) \times I_{OUT} \quad (5)$$

NOTE: Thermal shutdown is provided as a safety feature and is outside the specified operating ratings temperature range. Operation with a junction temperature (T_J) above 125°C is not recommended as the device behavior is not specified.

4.3 Soft Start

The programmable soft-start function limits the inrush current to the device being powered and controls the output voltage raise time during power-up. When the LP38789-ADJ is disabled through a high logic signal at the V_{OFF} pin, the device will have a fast start-up independent of the soft-start settings.

The resistive-capacitive (R1 × C6) circuit at the SET pin defines the time constant of the output slew rate. Note that the soft-start function only works when the LDO is powered from 0 V_{IN}, not when the shut-off or output-disabling function is used.

4.4 Disable Output Voltage Feature

Using the output voltage disable or shut-off feature minimizes the power drain to meet the requirements of portable battery operated systems while providing a fast start-up after exiting the shut-off mode.

The Enable pin in the LP38798-ADJ is internally pulled high by a 2-µA current. Q1 is used to pull the EN pin low. The gate of Q1 has a pull-down resistor that keeps Q1 inactive by default by pulling the V_{OFF} pin high either by connecting to a voltage greater than 2.5 V (typical) or by connecting directly to the input voltage, which will activate Q1 and will disable the LP38798-ADJ output.

5 Getting Started: Hardware

Before applying power to the TIDA-00533 rail cleaner board, verify all external connections. The external power supply must be turned off before being connected. Confirm proper polarity to the V_{IN} and GND terminals before turning the external power supply on. Connect an appropriate load between the V_{OUT} and GND terminals. Under basic evaluation conditions, all of the test points can be left open. The evaluation board will be in the normal operating mode when input power is applied.

6 Test Data

6.1 Test Equipment

Table 2. Test Equipment

TEST EQUIPMENT	PART NUMBER
Oscilloscope	Agilent MSO7034B
Voltage supply	Agilent E6131A
Network analyzer	Agilent E5061B
Digital multimeter	Agilent 34401A

6.2 Power Supply Ripple Rejection

The output voltage ripple rejection ratio was calculated by comparing the regulated output ripple to the input voltage ripple of 50 mV over a frequency range of 10 Hz to 10 MHz.

Input voltage = 5.5 V + 50 mV Cos (ωt)

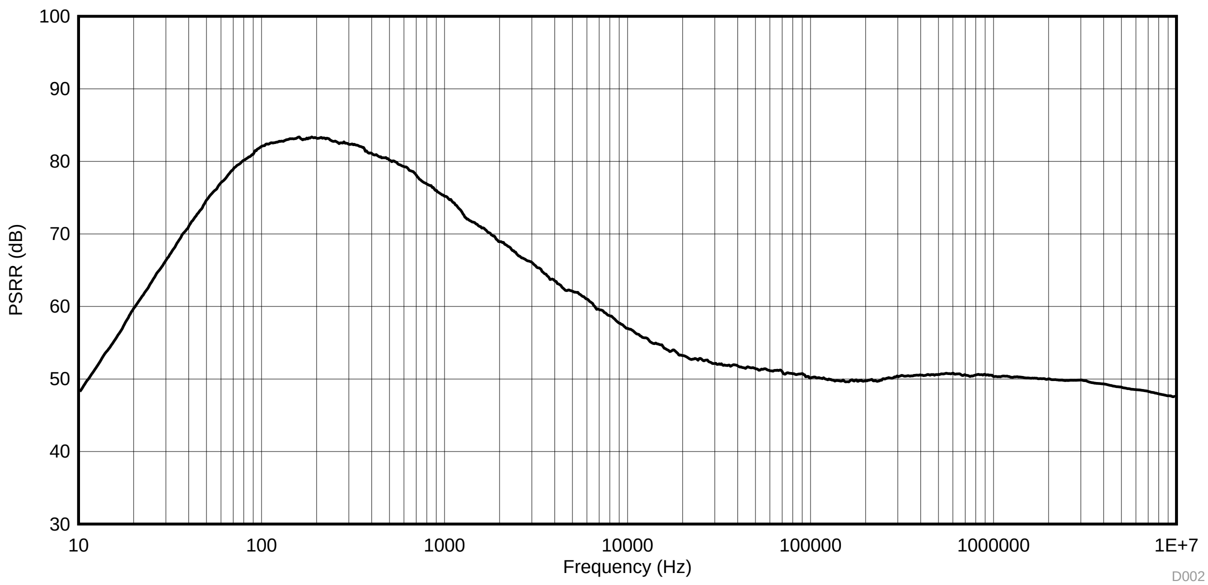

Figure 4. Frequency versus PSRR

6.3 Voltage Drop Setup

The output voltage drop is a function of I_{SET} and R1. I_{SET} varies with the input voltage. The higher the voltage drop, the higher the V_{OUT} tolerance.

When the typical I_{SET} current of 52 µA at 5.5 V_{IN} is used to calculate the output voltage drop, a maximum output voltage tolerance of ±5% is expected over the full range of the operating voltage at room temperature 23°C. The blue line in Figure 5 shows the V_{OUT} tolerance at 500 mV_{DROP}. The blue line in Figure 6 shows the V_{OUT} tolerance at 1 mV_{DROP}. The V_{OUT} tolerance is lower at the lower V_{DROP} setup.

If the application requires a higher output voltage accuracy at a higher input voltage range, the V_{OUT} tolerance can be optimized by calculating the I_{SET} current using Equation 2 from Section 4.1 and then with the resulting current value calculate R1 using Equation 3. The green and red lines in Figure 5 and Figure 6 show a lower V_{OUT} tolerance at higher V_{IN}.

Table 3. Voltage Drop Test Conditions

PARAMETER	VALUE
Load resistance	3.3 kΩ
V_{IN}	3.5 to 20.5 V

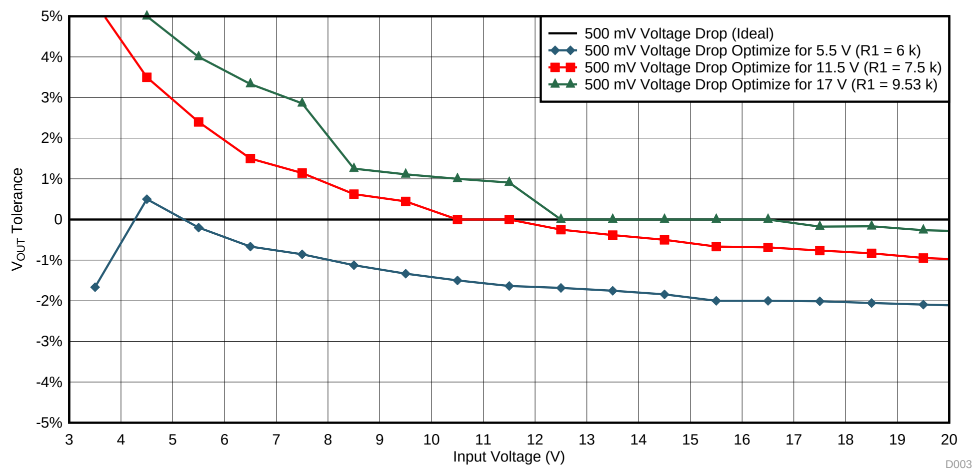

Figure 5. Output Voltage Tolerance at 500 mV_{DROP} versus Input Voltage

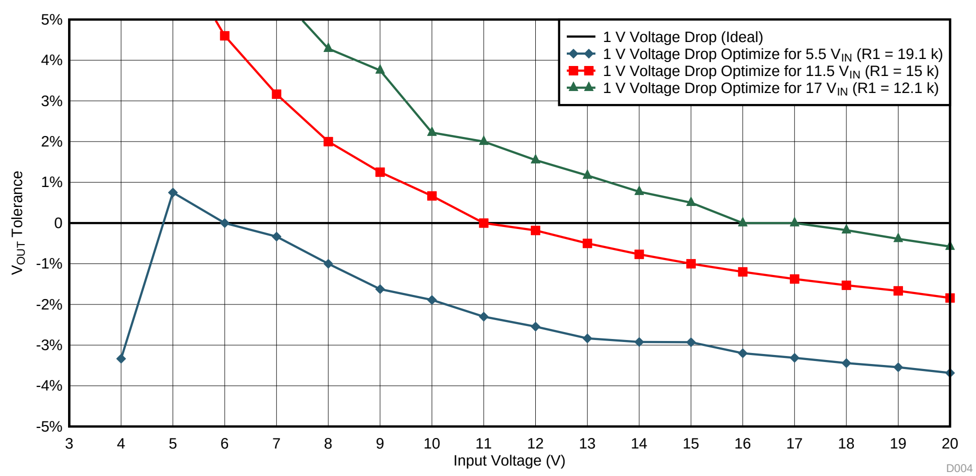

Figure 6. Output Voltage Tolerance at 1 V_{DROP} versus Input Voltage

6.4 Soft Start

The soft-start function was evaluated by shutting down the LP38798-ADJ completely and applying 5.5 V at the V_{IN} pin.

Table 4. Soft Start Test Conditions

PARAMETER	VALUE
Load resistance	3.3 kΩ
V_{IN}	3.5 to 20.5 V

R1 and C6 form the RC time constant (Tau), which contributes to the output voltage rise time (T_{RISE}). Figure 7 shows the relationship of Tau and T_{RISE}.

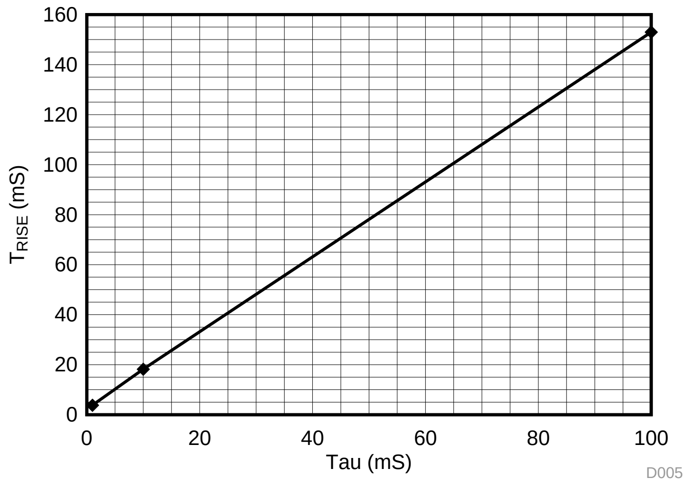

Figure 7. Output Voltage Rise Time (T_{RISE}) versus RC Time Constant (Tau)

Equation 6 gives a close approximation of the time that the output voltage takes from 10% V_{OUT_MAX} to reach 90% V_{OUT_MAX}.

$$T_{RISE} = -0.001 \times Tau^2 + 1.6114 \times Tau + 2.1897 \quad (6)$$

Table 5 compares the discrepancy between the computed T_{RISE} using Equation 6 and the measured T_{RISE} at different time constants settings.

Table 5. Measured T_{RISE} versus Computed T_{RISE}

Tau (ms)	COMPUTED T_{RISE} (ms)	MEASURED (ms)	DISCREPANCY (%)
1	3.8	3.8	0
10	18.2	18.2	0
35.2	57.7	56	3
56.9	90.6	94	4
70.5	110.8	106	5
90.2	139.5	146	4
94	144.8	154	6
100	153	153	0

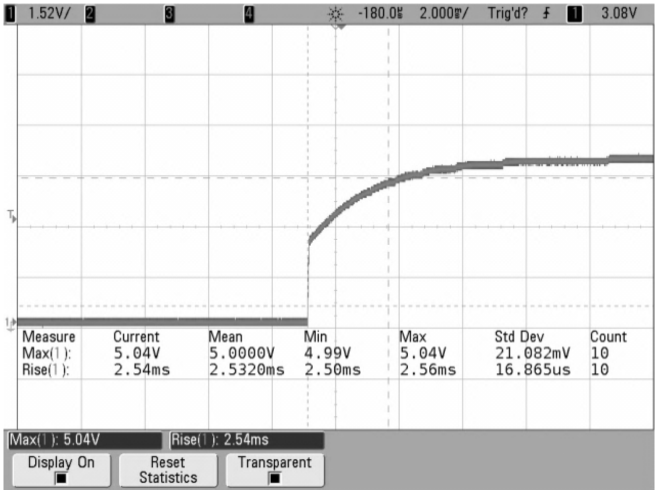

Figure 8. No Capacitor C6; Tau = N/A; Measured T_{RISE} = 2.54 ms

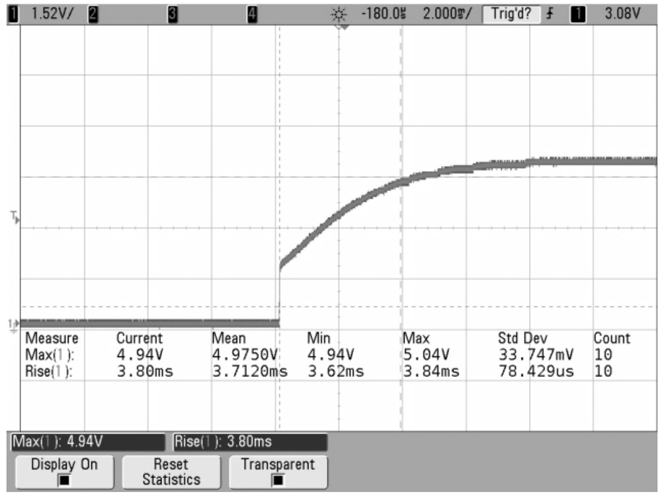

Figure 9. Tau = 1 ms; Measured T_{RISE} = 3.80 ms

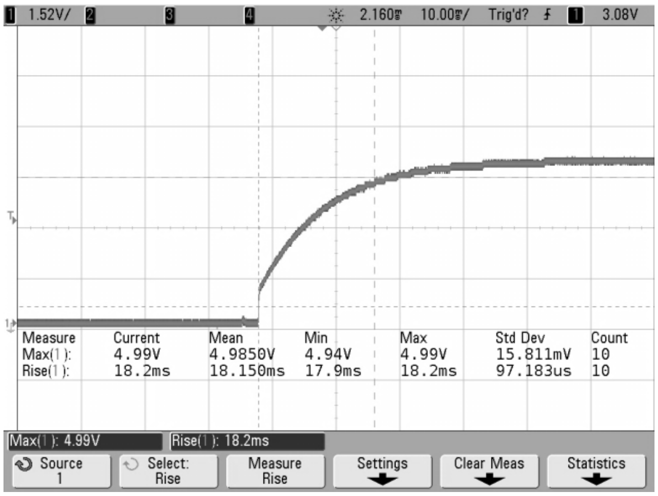

Figure 10. Tau = 10 ms; Measured T_{RISE} = 18.2 ms

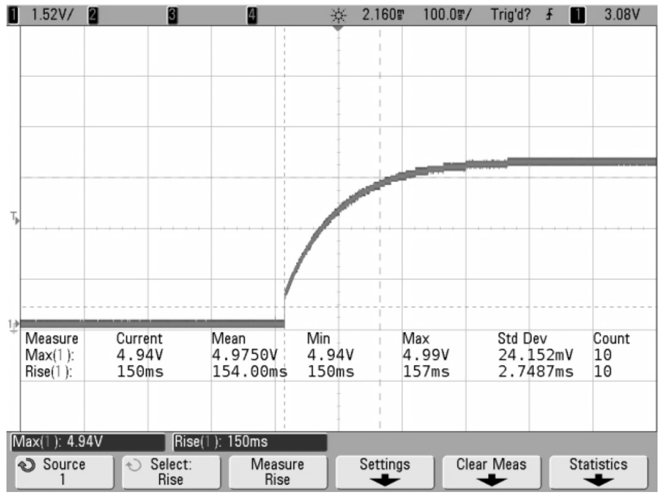

Figure 11. Tau = 100 ms; Measured T_{RISE} = 153 ms

6.5 Disable Output Voltage and Fast Startup

This test was accomplished by applying 2.5 V at the V_{OFF} pin to disable the output voltage and then removing the 2.5 V at the V_{OFF} pin to enable the output voltage again.

Table 6. Disable Output Voltage Test Conditions

PARAMETER	VALUE
V_{IN}	5.5 V
I_{OUT}	383 mA
V_{OFF}	2.5 V
Load resistance	13 Ω
C3	10-µF ceramic
C4	10-µF tantalum

When 2.5 V is applied to the V_{OFF} pin under the specified conditions, the output voltage takes approximately 1 ms to fall from 5 to 0 V_{OUT}.

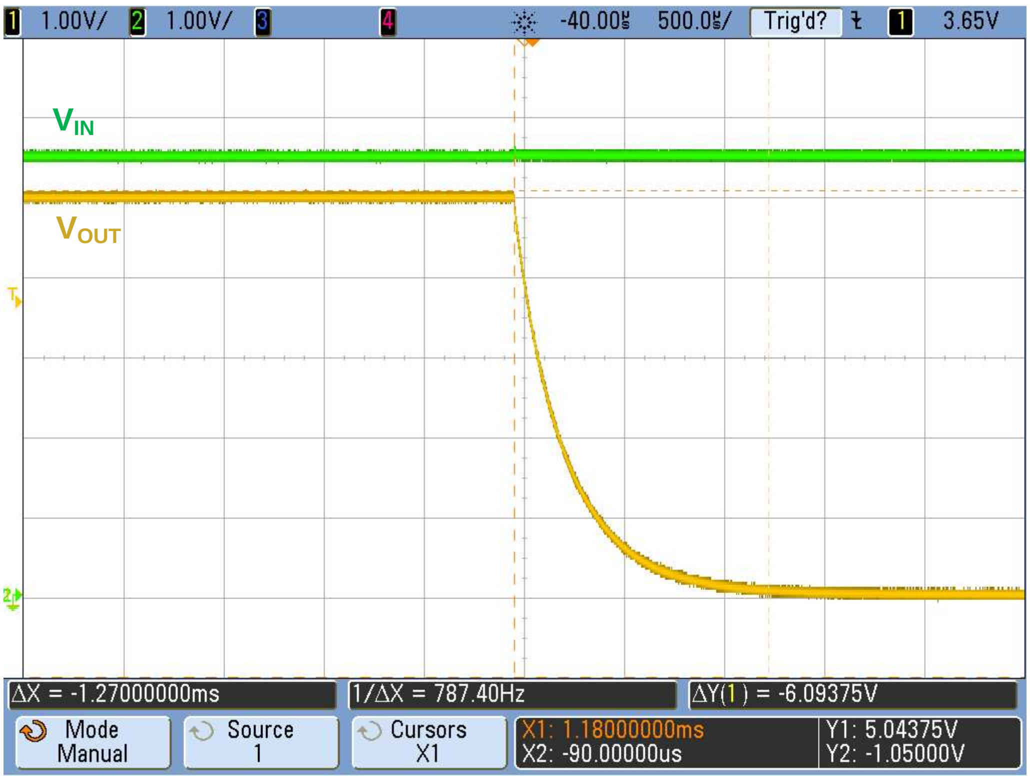

Figure 12. V_{OFF} from Low to High

When 2.5 V is removed from the V_{OFF} pin, the device exits the shut-off mode and the output voltage rises from 0 V_{OUT} to 5 V_{OUT} in approximately 40 µs as shown in Figure 13.

Figure 13. V_{OFF} from High to Low

7 Design Files

7.1 Schematics

To download the schematics, see the design files at TIDA-00533.

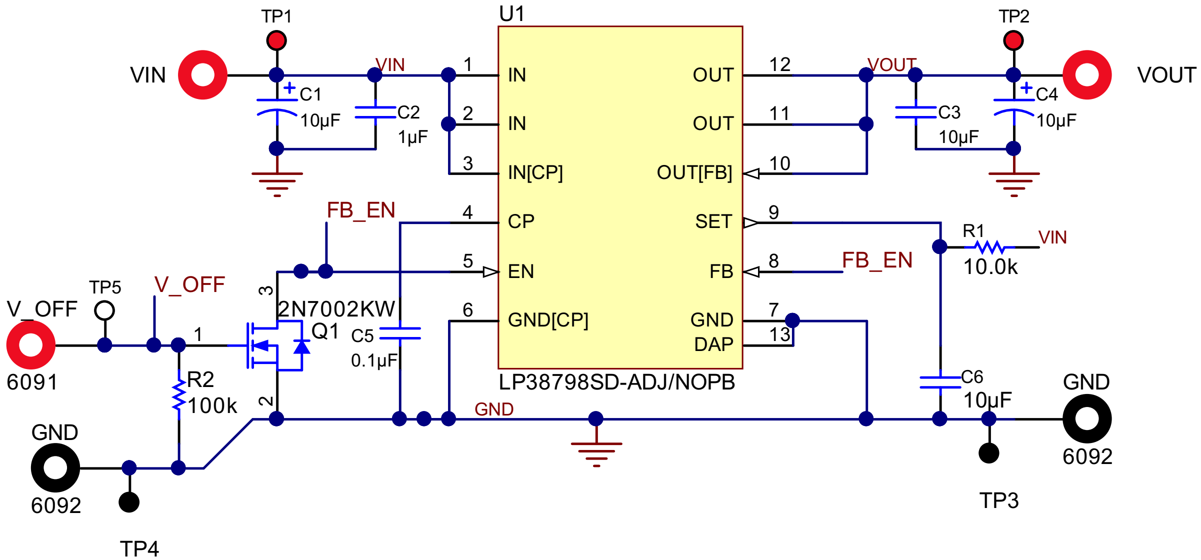

Figure 14. TIDA-00533 Schematic

7.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00533.

7.3 PCB Layout Recommendations

The dynamic performance of the LP38798 is dependant on the layout of the PCB. PCB layout practices that are adequate for typical LDOs may degrade the PSRR, noise, or transient performance of the LP38798.

Best performance is achieved by placing all of the components on the same side of the PCB as the LP38798, and as close as is practical to the LP38798 package. All component ground connections should be back to the LP38798 analog ground connection using as wide, and as short, of a copper trace as is practical. The datasheet recommends a short connection between the FB pin and V_{SET}; in this case, the FB trace length will not be as critical.

Connections using long trace lengths, narrow trace widths, and connections through vias should be avoided. These connections will add parasitic inductances and resistance that results in an inferior performance, especially during transient conditions.

A ground plane, either on the opposite side of a two-layer PCB or embedded in a multi-layer PCB, is strongly recommended. This ground plane serves two purposes:

1. Provides a circuit reference plane to assure accuracy
2. Provides a thermal plane to remove heat from the LP38798 through thermal vias under the package DAP

7.3.1 Layer Plots

To download the layer plots, see the design files at TIDA-00533.

7.4 Altium Project

To download the Altium project files, see the design files at TIDA-00533.

7.5 Gerber Files

To download the Gerber files, see the design files at TIDA-00533.

7.6 Assembly Drawings

To download the assembly drawings for each board, see the design files at TIDA-00533.

8 References

1. Texas Instruments, *Soft-start circuits for LDO linear regulators*, Analog and Mixed-Signal Products Technical Brief (SLYT096).

9 About the Author

ANTONY PIERRE CARVAJALES is an applications engineer on the mobile power devices RF power group at Texas Instruments. Antony has worked in various business units expanding his knowledge in analog circuitry design to help customers solve their design challenges using TI technologies. Antony earned his bachelors of science in electrical engineering from Florida International University, FL.

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