Eugenio Mejia

TI Designs – Precision: Verified Design
Low-noise Precision Variable Reference

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Design Resources

TIPD194	All Design files
TINA-TI™	SPICE Simulator
DAC8820	Product Folder
OPA227	Product Folder
TPS71750	Product Folder
REF5010	Product Folder

Circuit Description

A precision dynamic reference source that is able to supply a voltage range from of ±10 V with a 16-bit resolution focusing on initial accuracy and low noise.

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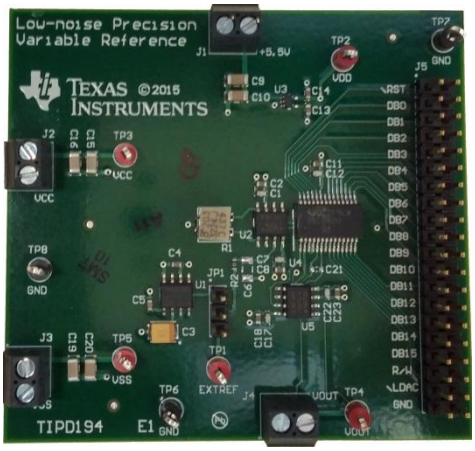

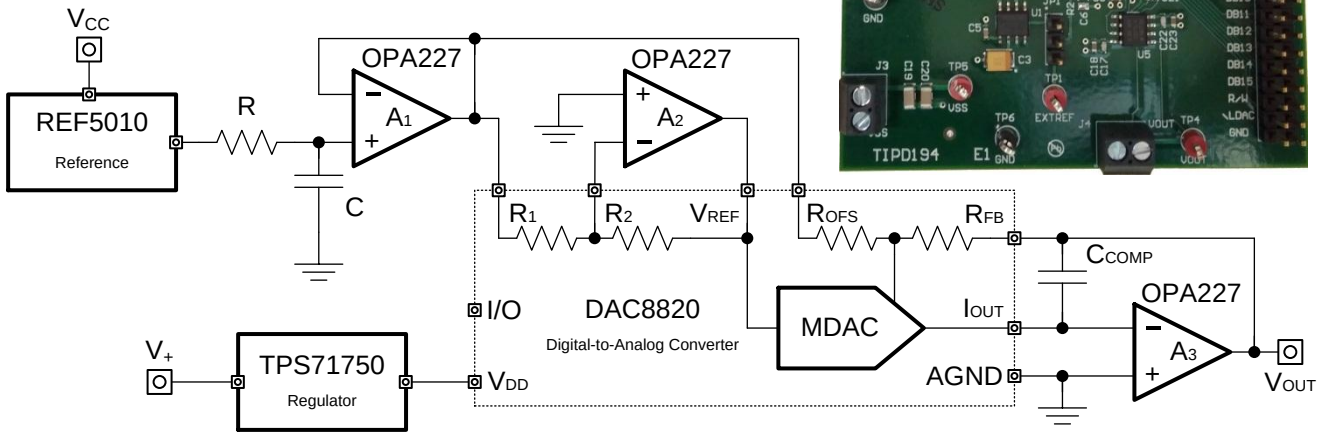

1 Design Summary

The design requirements are as follows:

- DAC Supply Voltage: +5 V
- Output Stage Supply Voltage: ±15 V
- Input: +10 V
- Output: ±10 V

The design goals and performance are summarized in Table 1. Figure 1 depicts the measured transfer function of the design.

Table 1. Comparison of Design Goals, Simulation, and Measured Performance

	Goal	Simulated	Measured
Initial Accuracy (%FSR Max.)	0.03	0.0245	0.013

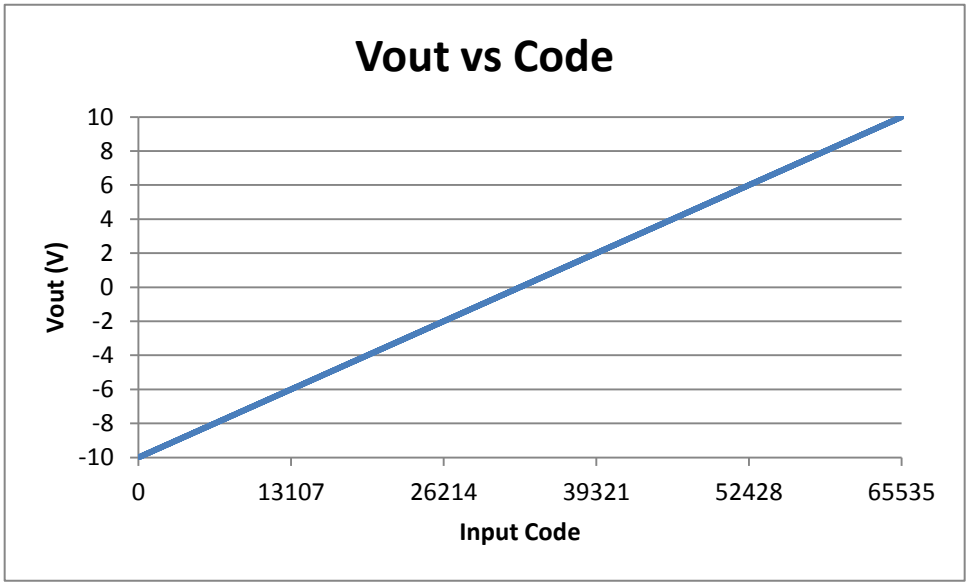

Figure 1: Measured Transfer Function

2 Theory of Operation

The variable precision reference design consists of one Low-Drop Out Regulator (LDO), one Precision Voltage Reference (REF), one Digital-to-Analog Converter (DAC) and three Operational Amplifiers (OPA).

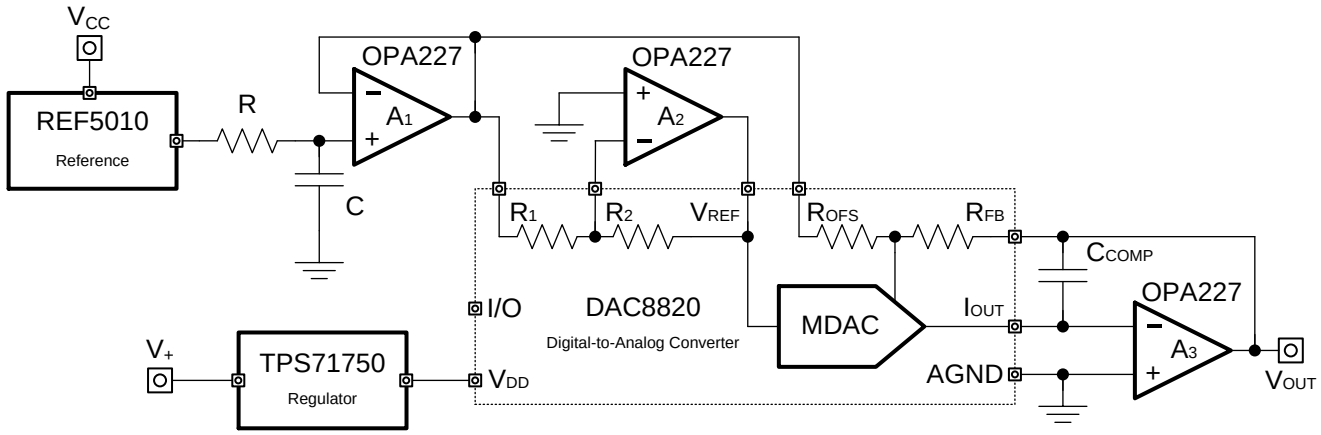

Figure 2: Detailed block diagram

2.1 Operation

2.1.1 Inverting reference stage

The inverting reference stage consists of a precision reference (REF5010), two amplifiers (A_1 & A_2), an RC network and two resistors. The reference generates a positive +10 V output which is followed by an RC filter that is in place to limit the high frequency noise contribution from the reference to the rest of the system. The cutoff frequency of the filter is shown in Equation (**1**).

$$f_{-3dB} = \frac{1}{2 \cdot \pi \cdot R \cdot C} \quad (1)$$

A_1 is responsible for buffering the reference output, which is required with larger filter capacitors. The buffer prevents the RC filter from being loaded by the feedback network of A_2. The A_2 amplifier inverts the +10 V output of the buffer resulting in -10V at the DAC VREF pin. The inverting network of A_2 is comprised by the internal resistors of the DAC. The matching and tracking of internal resistors is much better than most external resistors, but using external resistors is still a viable solution if using a different DAC or if a different gain is desired. Please refer to Section 3.5.2 for help picking external resistors. If you want to set your own gain by emulating this circuit using external resistors, you can use Equation (**2**) to obtain the resistor values.

$$V_{-REF} = -\frac{R_2}{R_1} \cdot V_{+REF} \quad (2)$$

2.1.2 Summing stage

The summing stage sums the output of the MDAC with a dc offset as shown by Equation (**3**). The voltage conversion of the output current of the DAC can be interpreted as a variable resistor (R_{DAC}) as shown in Equation (**4**). Combining Equations (**3**) & (**4**) will result in the output transfer function described by Equation (**5**).

$$V_{OUT} = -\frac{R_{FB}}{R_{OFS}} \cdot V_{+REF} - \frac{R_{FB}}{R_{DAC}} \cdot V_{-REF} \quad (3)$$

$$R_{DAC} = 2 \cdot R_{FB} \cdot \frac{2^{16}}{CODE} \quad (4)$$

$$V_{OUT} = V_{+REF} \cdot \left[2 \cdot \frac{CODE}{2^{16}} \cdot \frac{R_2}{R_1} - \frac{R_{FB}}{R_{OFS}} \right] \quad (5)$$

2.2 Noise Analysis

For the noise analysis of an MDAC, it is necessary to take into consideration that the voltage noise of the output transimpedance amplifier will be modulated due to the internals of an MDAC. The modulation amplitude depends on the output code and it is directly related to the input offset voltage modulation mentioned in Section 3.3. The voltage noise can be modeled in the same position as the input offset voltage (non-inverting node of the amplifier). In short, this means that the noise gain will be equal to the 2.4 V/V. For more information regarding the specifics of the modulation please refer to another MDAC TI Design (TIPD137) which explains in detail the interaction between the MDAC and the output transimpedance amplifier.

The reference noise attenuation is also an important aspect of working with an MDAC. Since the MDAC works as an attenuator, the input reference to the MDAC is attenuated depending on the output code as is the reference noise. Assuming a 16-bit DAC the greatest attenuation happens at Code 0, and the least attenuation at Code 65535.

After understanding these two aspects of MDAC noise, the calculation and simulation of the MDAC system noise becomes a standard amplifier noise calculation which requires the understanding of 3 different noise contributors: resistor thermal noise, 1/f noise and broadband noise.

2.2.1 Resistor thermal noise

The noise contribution from the resistors is referred to as thermal noise (en_R). Equation (6) describes the spectral noise contribution of the resistors. The variables are as follows: k is Boltzmann constant, T is the temperature of the environment, R is the equivalent resistance and f is the noise frequency. The designer will have the most control over the size of the equivalent resistance. Picking smaller resistors will reduce the overall noise introduced into the system. For this design the resistor size is set by the DAC internal resistors.

$$en_R = \sqrt{4 \cdot k \cdot T \cdot R \cdot f} \quad (6)$$

2.2.2 1/f noise

The low frequency noise is referred as the 1/f noise or flicker noise ($e_{1/f}$). This noise, as the name suggests, has a noise response inversely proportional to frequency. The operational amplifiers in this design will be the largest contributors of noise. The datasheets of OPAs will include this specification in the electrical characteristics table as well as a graph vs frequency. In the electrical characteristics table it is usually listed as the spectral noise from 1 to 10 Hz. Although the 1/f noise is most prevalent at the lower frequencies, it is only limited by the noise bandwidth of the stage. It is easiest to use the spectral noise at 1 Hz to calculate the peak-to-peak noise ($en_{1/f}$), but some datasheets may not include the measurement at 1 Hz. Use Equation (7) to extrapolate the 1/f noise at 1Hz from the 1/f noise at frequency f_X. After normalizing the 1/f noise, the peak to peak voltage can be calculated using Equation (8) where f_{HIGH} is the noise bandwidth and f_{LOW} is the lowest frequency of interest.

$$e_{1/f}\Big|_{1Hz} = e_{1/f}\Big|_{f_x} \cdot \sqrt{f_x} \quad (7)$$

$$en_{1/f} = e_{1/f}\Big|_{1Hz} \cdot \sqrt{\ln\left(\frac{f_{HIGH}}{f_{LOW}}\right)} \quad (8)$$

2.2.3 Broadband noise

The high frequency noise is referred to as broadband noise (e_{BB}). The operational amplifiers in this design will also be the largest contributors of noise. The datasheet of OPAs will include this specification in the electrical characteristics table as well as a graph vs frequency. In the electrical characteristics table it is usually listed as the spectral noise from 1 to 100 kHz. The broadband noise is limited by the noise bandwidth of the stage. To calculate the broadband peak-to-peak noise use Equation (**9**), where f_{HIGH} is the noise bandwidth.

$$en_{BB} = e_{BB} \cdot \sqrt{f_{HIGH}} \quad (9)$$

2.2.4 Noise addition

Noise is not added linearly; instead a root sum square approach is used as shown in Equation (**10**).

$$en_{TOTAL} = \sqrt{en_R^2 + en_{1/f}^2 + en_{BB}^2} \quad (10)$$

2.2.5 RC Buffer stage noise

The noise calculation in this stage includes the noise from:

- The REF5010 (en_{REF})
- The RC filter (en_{RC})
- The OPA227 A_1 1/f noise ($en_{1/f}$) as well as the broadband noise (en_{BB})

$$en_1 = \sqrt{en_{REF}^2 + en_R^2 + en_{1/f}^2 + en_{BB}^2} \quad (11)$$

2.2.6 Inverting reference stage noise

The noise calculation in this stage includes the noise from:

- The RC buffer stage (en_1)
- The two internal resistors R_1 and R_2 of the DAC8820 (en_{REQ1})
- The OPA227 A_2 1/f noise ($en_{1/f}$) as well as the broadband noise (en_{BB})

$$en_2 = \sqrt{en_1^2 + en_{REQ1}^2 + en_{1/f}^2 + en_{BB}^2} \quad (12)$$

2.2.7 Summing stage noise

The noise calculation in this stage includes the noise from:

- The RC buffer stage (en_1) with gain of R_{FB}/R_{OFS}
- The inverting reference stage (en_2)

- Two internal resistors R_{FB} and R_{OFS} of the DAC8820 (en_{REQ2})
- The output of the DAC (en_{DAC}) with a gain of 2.4 V/V
- The OPA227 A_1 1/f noise ($en_{1/f}$) as well as the broadband noise (en_{BB}) with a gain of 2.4 V/V

$$en_3 = \sqrt{\left(en_1 \cdot \frac{R_{FB}}{R_{OFS}}\right)^2 + \left(en_{REQ2}^2 + en_{1/f}^2 + en_{BB}^2\right) \cdot (2.4)^2} \quad (13)$$

3 Component Selection

3.1 Digital-to-Analog Converter (DAC)

The DAC8820 has high linearity, low gain error and low output noise. In addition the DAC includes internally matched resistors that will contribute to low system gain and offset erros as well as good tracking over temperature in contrast to external passive components.

The parallel interface of the DAC8820 can be easily replaced by an SPI interface. Usually parallel interfaces are used to provide extremely fast communication between the master and the slave devices. In this design the parallel interface is showcased because it allows the designer to power-on the DAC to a set voltage determined by permanently connected the data pins to GND or VDD, if necessary.

3.2 Regulator (LDO)

The TPS71750 is a 5.0 V output low drop-out regulator (LDO) is a candidate for regulating the DAC power supply. DACs tend to have high power-supply rejection ratio (PSRR), but using a regulator can increase the PSRR, improving the performance of the system. The DAC draws minimal current so it feasible to share the LDO from a different part in the system.

3.3 Amplifier (OPA)

The OPA227 is a high precision amplifier with low typical offset voltage of 5 µV, with a noise density of 3 nV/√Hz at 1 kHz.In addition the OPA227 is unity gain stable. The flexibility of this amplifier allows for the same part to be used in three distinct roles within this design: a non-inverting buffer, a non-inverting buffer and a transimpedance amplifier.

Low input offset voltage (V_{OS}) is a core specification of the OPA227 that is important in all stages of this design, but it is particularly important in the output transimpedance stage. V_{OS} must be low in the output stage of an MDAC because the I_{OUT} will modulate the input offset voltage into a linearity error multiplied by a factor of 2.4. This means that the output linearity error will increase by V_{OS}*2.4. If you want to know more details about the conditions that cause this behavior please refer to another of our MDAC TI Designs (TIPD137) in Section 9 which explains this information about MDACs and their output stage in detail.

One key thing to notice in this design is that the noise from the REF5010 and the DAC8820 are both significantly larger than the noise of the OPA227. Noise sources are summed in a root-sum square approach which causes the larger noise contributors to drown-out the lower noise sources. In short, even though it would be possible to use an even lower noise amplifier than the OPA227 it would be a waste of resources since the performance of the system with not noticeably increase.

3.4 Reference (REF)

The REF5050 is a low-drift low-noise precision voltage +10 V reference with an initial accuracy of 0.05 %, accuracy over temperature of 0.03 % and low output voltage noise.

3.5 Passive Components

There are four groups of passive components in this design that should be discussed independently.

3.5.1 RC Pair

The RC pair that follows the output of the REF5010 is in place to limit the bandwidth of the noise introduced by the REF5010. If higher noise references must are used or lower noise is required, an RC filter can be used to limit the bandwidth to close to dc with a large capacitor. The RC will also slow down the response of the reference at start-up therefore it is important to find a good balance between the two.

3.5.2 Inverting and bipolar stage resistors

There are no discrete resistors on the inverting and bipolar stages of this design thanks to the matched ,integrated resistors of the DAC8820. For the transfer function shown in Equation (**5**), the absolute size of these resistors is not important, the matching of these resistors is important. The DAC8820 trimming scheme makes sure that these resistors are matched very closely in order to provide excellent performance. Take a look at Table 2 for the nominal resistor values inside the DAC8820.

Table 2: DAC8820 resistor sizes

Resistors	Value
R1	12 kΩ ± 20%
R2	12 kΩ ± 20%
RFB	12 kΩ ± 20%
ROFS	12 kΩ ± 20%
RDAC	6 kΩ ± 20%

However, if a different device that does not have these internal resistors is used, it would be important to pick resistors that have a tolerance of at least 0.1% for 16-bit resolution. Matching the resistors will minimize the offset and gain errors introduced into the system.

It is also important to have a balanced resistors size. Smaller resistors will introduce the least noise, but will increase the current consumption. The compromises between current consumption and noise performance will vary on the application.

3.5.3 Input and output capacitors

The TPS71750 and the REF5010 have suggested best practice input and output capacitors in their datasheets. These best practice input and output capacitors are implemented in the design. Please refer to the datasheets of these devices to obtain a full description of the effects these input and output capacitors have on the performance of each device.

3.5.4 Bypass Capacitors

Bypass capacitors are used at the inputs of the board supplies and supply pins. These bypass capacitors can aid to smooth out the supply rails, improving the performance of the devices under supply transients. Using a combination of large and small capacitors can reduce the self-resonance effects of each individual capacitor at different frequencies. A combination of 10 µF to 100 pF capacitors is recommended. The smaller capacitors should be placed closer to the device as possible in order to minimize the effect of any transients.

4 Simulation

Figure 3 shows the realization of the circuit using MDAC DAC8820. The desired output waveform is generated by the “Ideal Output Waveform” and an ideal ADC is used to generate the input codes for the DAC. The simulation includes all of the components except the TPS71750 which, as of the time of this writing, has no available TINA model. The TPS71750 will have negligible impact on the simulation results under normal conditions, since the TPS71750 is in place to minimize the supply transients that may come from outside of the system. The models use typical specifications by default, but some specifications can be modified to use maximum values.

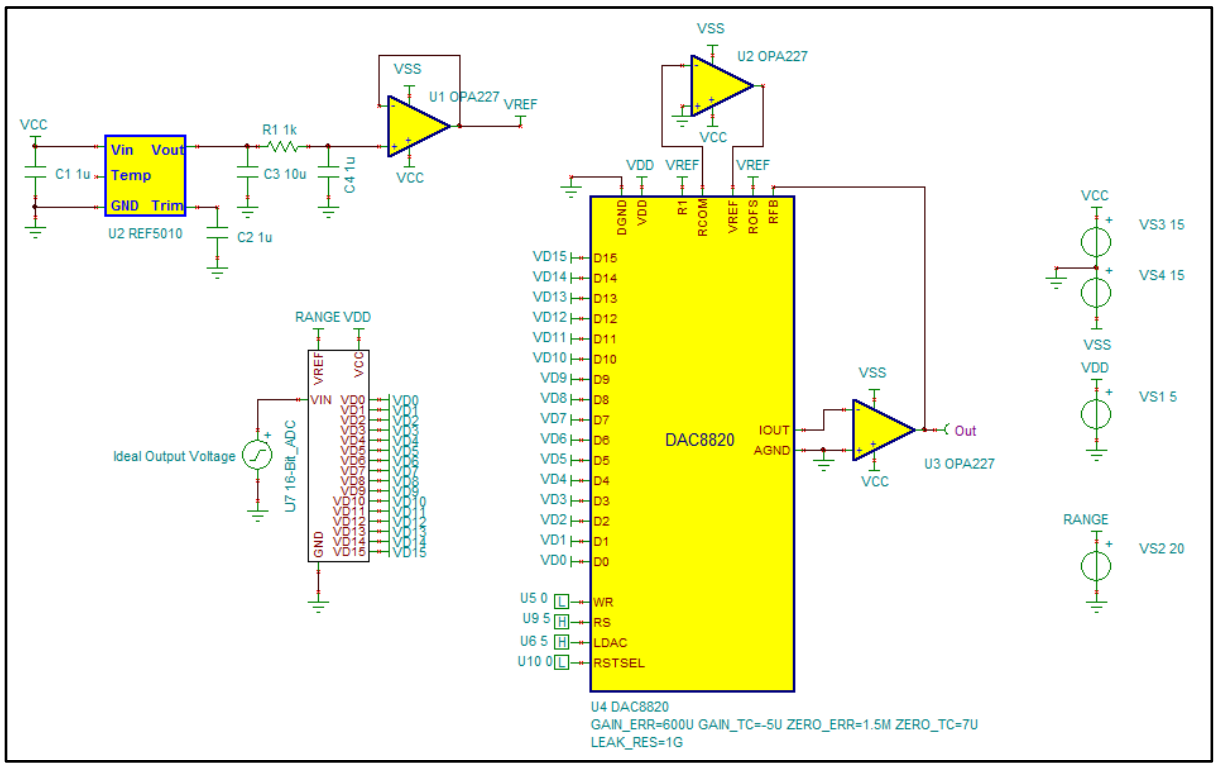

Figure 3: TINA Simulation

4.1 Simulated Transfer Function

The transfer function is shown in Figure 4.

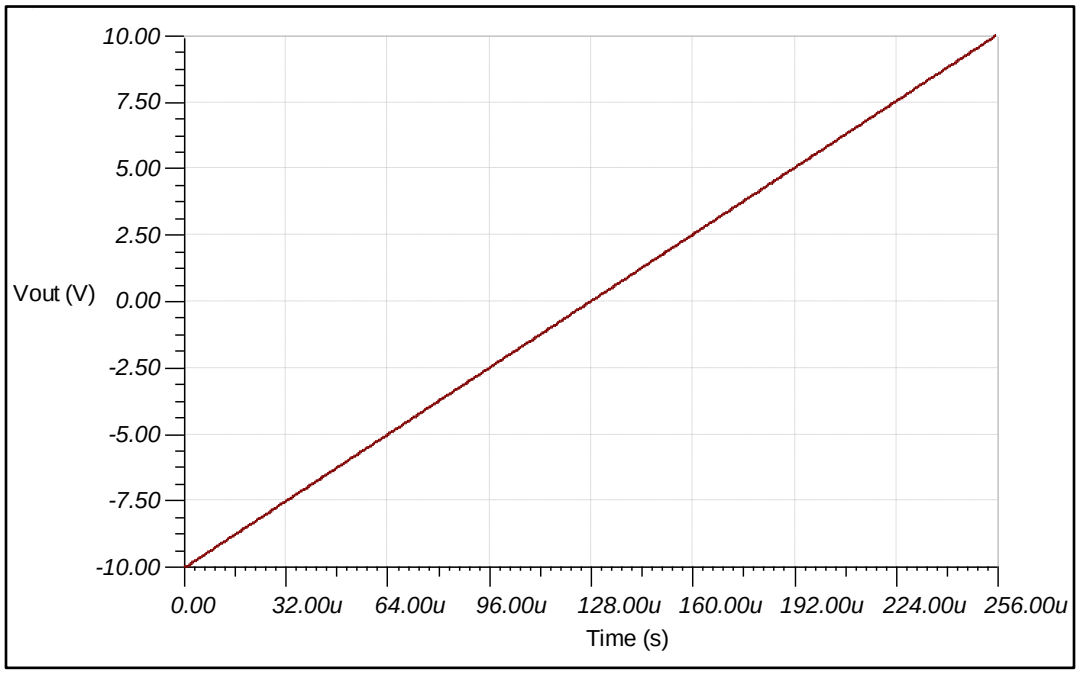

Figure 4: Simulated transfer function

Table 3: Simulated results

Errors	Typ.	Typ. Over Temp	Max.	Max. Over Temp
INL	± 1 LSB	± 1 LSB	± 1 LSB	± 1 LSB
Offset	403 µV	645 µV	403 µV	645 µV
Gain	0.0031 %FSR	0.0116 %FSR	0.0244 %FSR	0.0414 %FSR
TUE	0.0039 %FSR	0.0121 %FSR	0.0245 %FSR	0.0416 %FSR

5 PCB Design

In most cases data converter PCB layout focuses on maintaining the digital traces separate from the analog traces. For this application it is not as essential since the digital lines will not be toggling during normal operation, only during the setup procedure. Even so the layout of the device pins allow for easy routing of the analog traces avoiding any crossover with digital traces.

When laying out reference sources it is important to use large widths on the analog traces in order to reduce any potential voltage drops across the line and maintain the integrity of our output reference voltage.

5.1 PCB Layout

Figure 5 shows the layout for this design. For a more detailed inspection look at the design archive that goes along with this document.

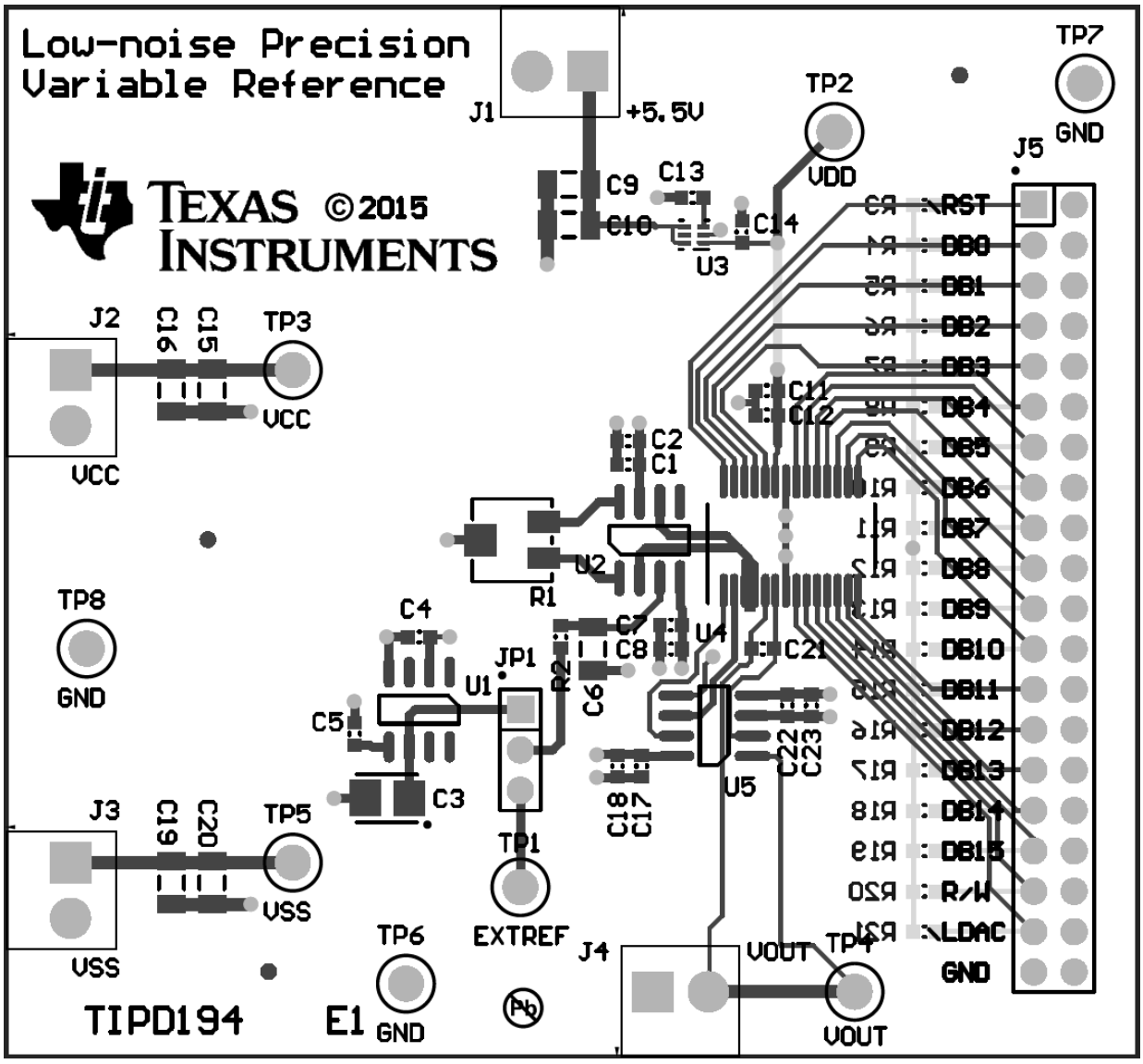

Figure 5: PCB Layout

6 Verification & Measured Performance

6.1 Transfer function

The transfer function is Equation (**14**), which uses Equation (**5**) with the values from Table 2 to generate the transfer function of the circuit designed in this document. The number of codes range from Code 0, to Code 65535. The ideal output range will be from -10 V, to +9.999695 V in steps of 305 µV. This allows the designer to use this output voltage as a precise reference source for another circuit or as a precision bias voltage.

$$V_{OUT} = 10 \cdot \left(2 \cdot \frac{CODE}{2^{16}} \cdot 1 - 1 \right) [V] \quad (14)$$

6.2 Results

The results on Table 4 show the initial accuracy of this design. The Total Unadjusted Error (TUE) stays below 0.02 %FSR at room temperature. With this design it is possible to calibrate the offset and gain error of the circuit which will minimize the TUE of the output. Calibration will reduce the error of the system to ideally only the INL error.

Table 4: Results

Errors	Typ.	Typ. Over Temp*	Max.	Max. Over Temp*
INL	0.56 LSB	0.68 LSB	0.56 LSB	0.68 LSB
Offset	571 µV	880 µV	695 µV	920 µV
Gain	0.0097 %FSR	0.0187 %FSR	0.0130 %FSR	0.0201 %FSR
TUE	0.0101 %FSR	0.0192 %FSR	0.0133 %FSR	0.0207 %FSR

* The temperature range tested is determined by the DAC8820 datasheet range from -40°C to +85°C.

7 Modifications

7.1 Alternate devices

Depending on the design requirement other multiplying DACs can be used in this design. DAC8820 was selected for its parallel interface, high resolution, and multiplying bandwidth. Table 5 shows other MDAC options for application that may not require high resolution or that may require a parallel interface. Table 6 shows alternative amplifiers that can be used in this design for larger bandwidth or minimal input bias current.

Table 5. Alternative MDACs

MDAC	Resolution	Channel Count	Interface	Reference multiplying bandwidth
DAC8820	16 bits	1	Parallel	10 MHz
DAC8811	16 bits	1	Serial	10 MHz
DAC8812	16 bits	2	Serial	10 MHz
DAC8822	16 bits	2	Parallel	10 MHz
DAC8801	14 bits	1	Serial	10 MHz
DAC8806	14 bits	1	Parallel	10 MHz
DAC7821	12 bits	1	Parallel	10 MHz

Table 6. Alternative operational amplifiers

Amplifier	Supply	Bandwidth	Input bias current (Typ.)
OPA277	±18 V	1 MHz	±500 nA
OPA188	±18 V	2 MHz	±160 pA
OPA170	±18 V	1.2 MHz	±8 pA

7.2 Optimization

The design used in this document uses a very flexible topology with an extremely accurate 16-bit output voltage. The specifications of each component will depend on the specific application. The critical specifications of each component are discussed in Section 3.

The number of components in the design is heavily influenced by the desired output voltage range and the performance required. For example: a unipolar output stage does not require the use of the inverting amplifier. This will not only reduce the amplifier count by one, but will also reduce the noise introduced by using the resistors in this stage. Figure 6 shows a unipolar implementation that eliminates the reference buffer OPA, the inverting OPA and the regulator.

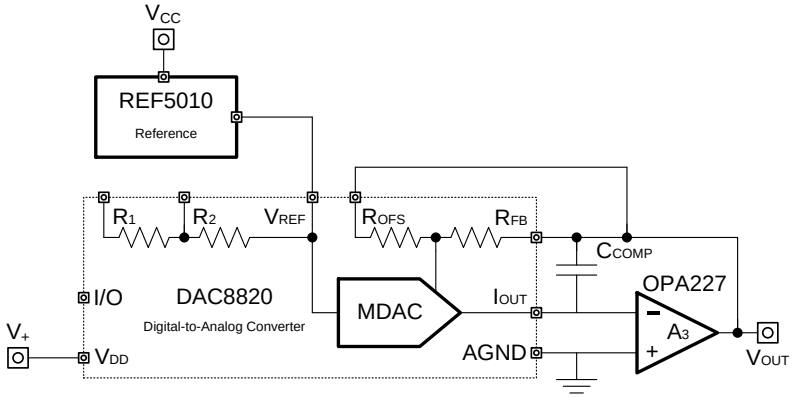

Figure 6: Unipolar implementation

If you have any questions regarding the design and optimization of a precision variable reference please feel free to post in the TI E2E Forums for Precision Data Converters. One of our applications will assist you with your questions.

8 About the Author

Eugenio Mejia is an applications engineer in the precision digital to analog converters group at Texas Instruments. Eugenio received his Bachelors of Science in Electrical Engineering from Texas A&M University.

9 Acknowledgements & References

1. *Engineer It, What is a multiplying DAC (MDAC)? (Video)*
2. *TIPD137, ±10V 4-Quadrant Multiplying DAC (TIDU031)*

Appendix A.

A.1 Electrical Schematic

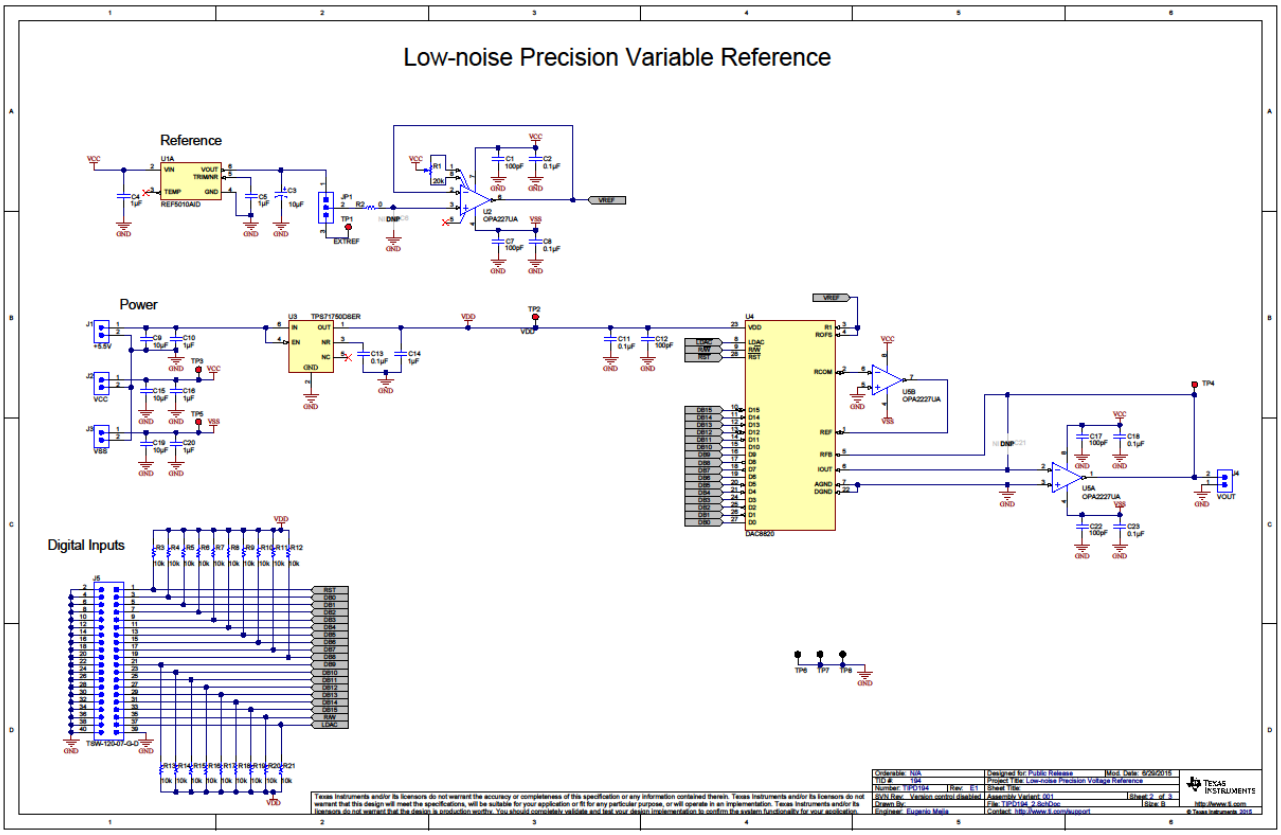

Figure A-1: Electrical Schematic

A.2 Bill of Materials

Texas Instruments

Bill of Materials

TI DESIGNS
TIPD194: Low-noise Precision Variable Reference

Item	Quantity	Designator	Description	Manufacturer	Part Number
1	5	C1, C7, C12, C17, C22	CAP, CERM, 100 pF, 50 V, +/- 5%, C0G/NP0, 0603	AVX	06035A101JAT2A
2	6	C2, C8, C11, C13, C18, C23	CAP, CERM, 0.1 µF, 50 V, +/- 10%, X7R, 0603	MuRata	GCM188R71H104KA57D
3	1	C3	CAP, TA, 10 µF, 16 V, +/- 10%, 0.5 ohm, SMD	AVX	TPSB106K016R0500
4	3	C4, C5, C14	CAP, CERM, 1uF, 25V, +/-10%, X5R, 0603	TDK	C1608X5R1E105K080AC
5	3	C9, C15, C19	CAP, CERM, 10uF, 25V, +/-10%, X5R, 1206	MuRata	GRM31CR61E106KA12L
6	3	C10, C16, C20	CAP, CERM, 1uF, 25V, +/-10%, X7R, 1206	AVX	12063C105KAT2A
7	4	J1, J2, J3, J4	Terminal Block, 6A, 3.5mm Pitch, 2-Pos, TH	On-Shore Technology, Inc.	ED555/2DS
8	1	J5	Header, 100mil, 20x2, Gold, TH	Samtec	TSW-120-07-G-D
9	1	JP1	Header, 100mil, 3x1, Gold, TH	Samtec	TSW-103-07-G-S
10	1	R1	TRIMMER, 20K, 0.25W, SMD	Bourns	3224J-1-203 E
11	1	R2	RES, 0, 5%, 0.1 W, 0603	Yageo America	RC0603JR-070RL
12	19	R3, R4, R5, R6, R7, R8, R9, R10, R11, R12, R13, R14, R15, R16, R17, R18, R19, R20, R21	RES, 10.0 k, 1%, 0.1 W, 0603	Yageo America	RC0603FR-0710KL
13	4	TP1, TP3, TP4, TP5	Test Point, Multipurpose, Red, TH	Keystone	5010
14	1	TP2	Test Point, Compact, Red, TH	Keystone	5005
15	3	TP6, TP7, TP8	Test Point, Multipurpose, Black, TH	Keystone	5011
16	1	U1	Low Noise, Very Low Drift, Precision Voltage Reference, -40 to 125 degC, 8-pin SOIC(D), Green (RoHS & no Sb/Br)	Texas Instruments	REF5010AID
17	1	U2	High Precision, Low Noise Operational Amplifier, 5 to 36 V, -55 to 125 degC, 8-pin SOIC (D0008A), Green (RoHS & no Sb/Br)	Texas Instruments	OPA227UA
18	1	U3	Single Output High PSRR LDO, 150 mA, Fixed 5 V Output, 2.5 to 6.5 V Input, with Low IQ, 6-pin WSON (DSE), -40 to 125 degC, Green (RoHS & no Sb/Br)	Texas Instruments	TPS71750DSER
19	1	U4	24-BIT, 192-KHZ SAMPLING, ADVANCED SEGMENT, AUDIO STEREO DIGITAL-TO-ANALOG CONVERTER, DB0028A	Texas Instruments	DAC8820
20	1	U5	High Precision, Low Noise Operational Amplifier, 5 to 36 V, -40 to 85 degC, 8-pin SOIC (D0008A), Green (RoHS & no Sb/Br)	Texas Instruments	OPA2227UA

Figure A-2: Bill of Materials

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