

TI Designs

Linear Regulator as a Dynamic Voltage Scaling Power Supply



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Design Resources

[TIDA-00531](#)
[LP3878-ADJ](#)
[TPL0401A](#)

Tool Folder Containing Design Files
 Product Folder
 Product Folder



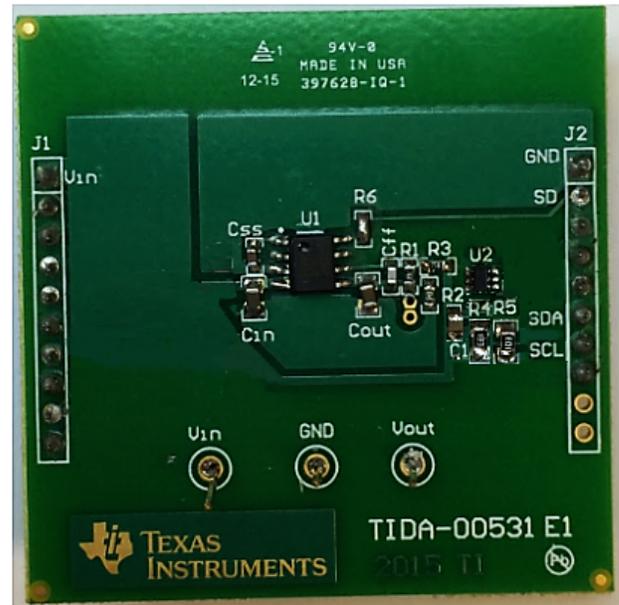
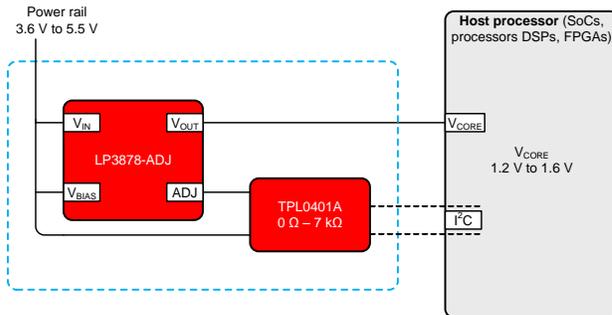
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Design Features

- Output Voltage Ranges from 1.2 V to 1.6 V With 90 Steps in Between
- Output Voltage Adjustable Through I²C Interface
- Up to 800-mA Output Current
- Output Voltage Enable and Disable

Featured Applications

- PDAs
- Wearables
- MP3 Players
- Battery Operated Devices



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1 System Description

The TIDA-00531 reference design features dynamic voltage scaling (DVS) as a power management solution to prolong the battery operation of portable devices. By pairing a linear regulator with a digital potentiometer, the user can adjust the supply voltage based on the need of the processor to save power.

In this design the output voltage is adjustable from 1.2 V to 1.6 V through the I²C interface. The TMS320VC5509A is a general example of a digital signal processor that has core voltages between 1.2 V up to 1.6 V depending on the processor clock frequency that is being used.

Table 1. TMS320VC5509A DSP Recommended Core Voltage

CORE SPEED	MIN	NOM	MAX
108 MHz	1.14 V	1.2 V	1.26 V
144 MHz	1.28 V	1.35 V	1.42 V
200 MHz	1.55 V	1.6 V	1.65 V

1.1 TI Design Overview

The current market trend is moving toward wearables and portable devices. As applications become more complex, the systems require more processing power, which increases the power consumption and leads to a decreased battery life.

Most applications only require a high performance from a processor for a fraction of the time, while at longer periods of time; a lower performance can satisfy the application. Because most systems have CMOS logic architecture and knowing that the energy dissipated per cycle with CMOS circuitry scales dramatically with respect to the supply voltage, the user can reduce the power consumption by implementing DVS.

The DVS method is widely used to reduce the average power consumption in embedded systems. Some examples where DVS is widely used are application specific integrated circuits (ASICs), system on a chip (SoC), processors, digital signal processors (DSPs), and field-programmable gate arrays (FPGAs). Lower the average power consumption by reducing the switching losses of the system, which is accomplished by selectively reducing the core voltage based on the requirements of the system. For instance, if the clock frequency in the processor is reduced the propagation delay is longer; as a result, the processor consumes more power unless the core voltage is reduced as well.

This TI design details a method to implement DVS using a low-dropout linear regulator (LDO), enabling all of the benefits of an LDO, such as a high power supply rejection ratio (PSRR), small footprint, economical value, and ease of implementation. This reference design also provides all of the applicable design files such as schematic images, Gerber files, and test data.

Table 2. Design Parameters

DESIGN PARAMETERS	VALUE
Input voltage	3.6 V to 5.5 V
Output voltage	1.2 V to 1.6 V
Maximum output current	800 mA

2 Block Diagram

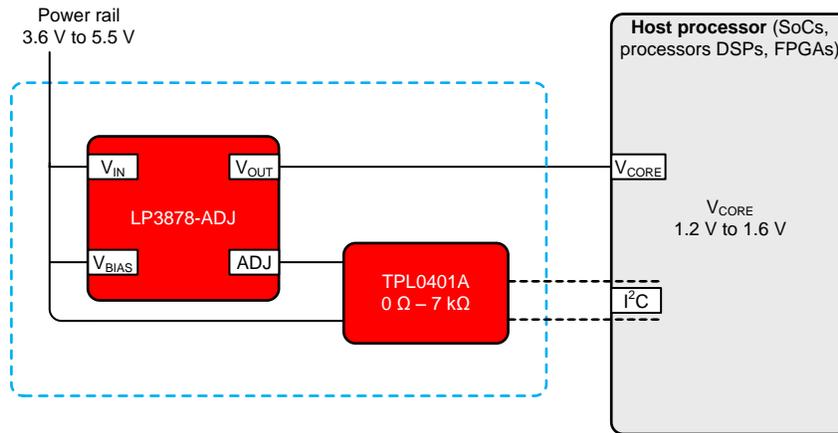


Figure 1. TIDA-00531 Comprehensive Block Diagram

3 Component Selection

The TIDA-00531 design guide features the following devices:

LDO: The LP3878-ADJ is a micropower, 800-mA low-noise, “ceramic stable” adjustable voltage regulator. For further details regarding the LP3878-ADJ device, see [Section 3.1](#).

Consider the following parameters when selecting the LDO:

- Adjustable output by resistor divider
- Maximum constant output current 800 mA
- Low IQ at shutdown

The alternative parts must have an adjustable pin:

- LP38851 has similar functionality at lower output voltages (0.8 V)
- LP38853 has similar functionality at a higher output current (3 A)

Digital potentiometer: The TPL0401A-10 is a 128 TAPS digital potentiometer with an I²C interface in a small SC-70 package. For further details regarding the TPL0401A-10 device, see [Section 3.2](#).

Consider the following parameters when selecting the digital potentiometer:

- Standard I²C interface
- Typical end-to-end resistance of 10 kΩ
- 128 wiper positions

The following lists alternative parts with similar functionality:

- TPL0401B-10 featuring a different I²C Interface
- TPL0501-100 uses a serial peripheral interface (SPI) interface
- TPL0102-100 uses non-volatile memory

3.1 LP3878-ADJ

The LP3878-ADJ is an 800-mA, adjustable output, voltage regulator designed to provide high performance and low noise in applications requiring output voltages as low as 1 V.

Using an optimized vertically integrated (VIP) PNP transistor, the LP3878-ADJ delivers superior performance:

- Ground pin current: Typically 5.5 mA at an 800-mA load and 180 μA at a 100-μA load.
- Low power shutdown: The LP3878-ADJ draws less than 10-μA quiescent current when the SHUTDOWN pin is pulled low.
- Precision output: The ensured output voltage accuracy is 1% at room temperature.
- Low noise: The broadband output noise is only 18 μV (typical) with a 10-nF bypass capacitor.

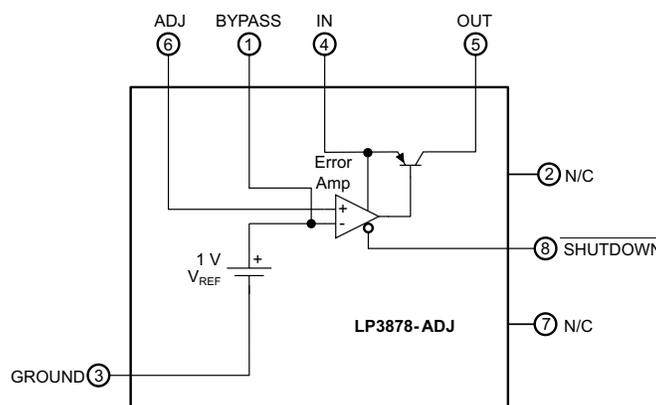


Figure 2. LP3878-ADJ Functional Block Diagram

3.2 TPL0401A-10

The TPL0401A is a single channel, linear-taper digital potentiometer with 128 wiper positions. The TPL0401A-10 has the low terminal internal and connected to GND. The position of the wiper can be adjusted using an I²C interface. The part has a 10 k end-to-end resistance and can operate with a supply voltage range of 2.7 V to 5.5 V.

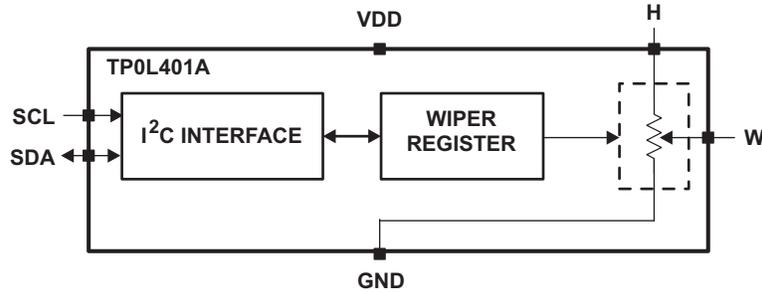


Figure 3. TP0L401A Functional Block Diagram

4 System Design and Component Selection

The following system considerations apply only for the conditions of this design. Verifying the ratings and operating conditions for the parts used in this design is essential. Find this information in the respective datasheets. If the parameters do not fit the application, consider one of the alternative parts from [Section 3](#) or perform an easy parametric search at <http://www.ti.com/ldo>.

4.1 Input Voltage Consideration

The input voltage of the LP3878-ADJ must be 2 V higher than the expected output voltage; in this case, the minimum input voltage must remain above 3.6 V for a stable output voltage of 1.6 V.

To eliminate high frequency noise and for stability, low equivalent series resistance (ESR) X7R ceramic capacitors are placed as close as possible to the input and output pin.

$$V_{IN} = V_{OUT_MAX} + 2\text{ V} = 1.6\text{ V} + 2\text{ V} = 3.6\text{ V} \quad (1)$$

The digital potentiometer TPL0401A-10 has an input voltage range from 2.7 V to 5.5 V. Because the D-potentiometer and the LDO share the same power rail, the input range of this system is from 3.6 V to 5.5 V.

If using an independent power rail to power the D-potentiometer, then the input voltage supply of the LDO can be as high as 16 V, allowing an input voltage range from 3.6 V to 16 V.

4.2 Capacitor Selection Consideration

4.2.1 Noise Bypass Capacitor

A 10-nF bypass capacitor reduces noise on the regulator output and is required for loop stability. The following recommendation must be taken into account:

- The bypass capacitor leakage must never exceed 100 nA.
- High-quality ceramic capacitors with either an NP0 or COG dielectric typically have very low leakage.
- 10-nF polypropylene and polycarbonate film capacitors typically have an extremely low leakage current.

4.2.2 Feedforward Capacitor

The feedforward capacitor (C_{FF}) is required to increase phase margin, ensure loop stability, and improve transient response.

The C_{FF} forms both a pole and zero in the loop gain. The zero provides a beneficial phase lead (which increases phase margin), and the pole adds an undesirable phase lag that must be minimized.

The zero frequency is determined by the values of C_{FF} and $R1$:

$$F_z = \frac{1}{2\pi C_{FF} \times R1} \quad (2)$$

The pole frequency is determined by the value of C_{FF} and the parallel combination of $R1$ and $R2$:

$$F_p = \frac{1}{2\pi C_{FF} \times \frac{R1 \times R2}{R1 + R2}} \quad (3)$$

For $V_{OUT} \leq 2.5\text{ V}$, C_{FF} must be selected to set the zero frequency in the range of about 50 KHz to 200 KHz.

The following [Equation 4](#) is used to calculate C_{FF} . The zero frequency is set to 52 KHz.

$$C_{FF} = \frac{1}{2\pi F_z R1} = \frac{1}{2\pi \times 52\text{ KHz} \times 604\pi} = 0.005\text{ }\mu\text{F} = 5\text{ nF} \quad (4)$$

4.2.3 Input and Output Capacitors

Input and output capacitors eliminate high frequency noise and are necessary for loop stability. Consider the following recommendations:

- Utilize X7R or X5R ceramic capacitors to minimize tolerance and variation with temperature
- Capacitance ESR in the 50- to 200-KHz range must not exceed 25 mΩ
- Input and output caps must be located less than 1 inch from the input and output pins
- Input minimum capacitance of 4.7 μF
- Output minimum capacitance of 10 μF
- Minimum of ± 20% capacitance tolerance

4.3 Output Voltage Configuration

The output voltage on this LDO in a typical application is determined by an external resistor divider R1 (upper-side resistor) and R2 (lower-side resistor).

$$V_{OUT} = V_{REF} \left(1 + \frac{R1}{R2} \right) \tag{5}$$

The LP3878-ADJ datasheet specifies that V_{REF} is typically 1 V at the adjustable pin.

In the TIDA-00531 reference design a digital potentiometer is placed across R2 with a series resistor. By adjusting the resistance of the potentiometer through the I²C interface, the resistor divider ratio changes accordingly, thus changing the output voltage.

4.3.1 Resistors Values Selection

TI recommends selecting resistor values of a high quality and tight tolerance. Figure 5 represents the components that define the output voltage. To ensure loop stability the lower-side resistance (R_{LS}) must not exceed 5 kΩ.

Figure 4 shows the implemented digital potentiometer configuration. The R_{HW} is the adjustable resistance between R3 and ground. Calculate R_{HW} using Equation 6:

$$R_{HW} = R_{TOT} \times \left(1 - \left(\frac{\text{Decimal value of step code}}{128} \right) \right) \tag{6}$$

RHEOSTAT MODE B

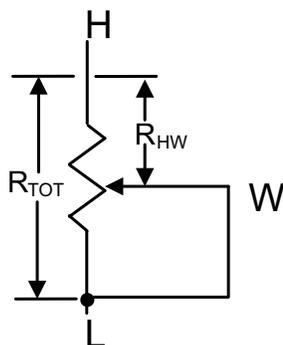


Figure 4. TPL0401A Configuration

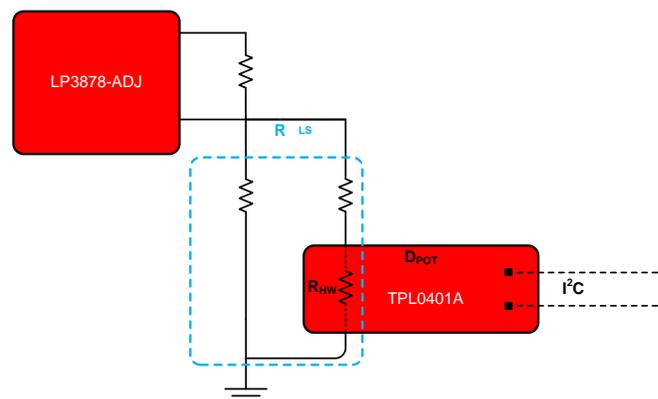


Figure 5. Resistor Divider

The TPL0401A-10 datasheet specifies that its typical maximum resistance is 10 kΩ with a tolerance of ±20%; meaning that the maximum value could be from 8 kΩ to 12 kΩ. To address these tolerances and maintain the maximum output voltage to no higher than 1.6 V, use the digital potentiometer within a range of 0 Ω (R_{HW_MIN}) to 7 kΩ (R_{HW_MAX}). This range allows for 90 steps of resolution in a typical D-potentiometer.

To be compliant with the 5-kΩ rule, 3 kΩ was chosen for the R_{LS} maximum value. Because 3 kΩ is the highest value for the equivalent lower resistance, this setting yields the lowest expected voltage of 1.2 V.

Calculate R1 using Equation 7:

$$R1 = R_{LS_MAX} \times \left(\frac{V_{OUT}}{V_{REF}} - 1 \right) = 3 \text{ k}\Omega \times \left(\frac{1.2 \text{ V}}{1 \text{ V}} - 1 \right) = 600 \text{ }\Omega \quad (7)$$

Calculate the minimum equivalent lower resistance R_{LS} using Equation 8.

$$R_{LS_MIN} = \frac{R1}{V_{MAX} - 1} = \frac{600 \text{ }\Omega}{1.6 \text{ V} - 1} = 1000 \text{ }\Omega \quad (8)$$

Resistor R3 is essential to avoid a short path to ground when the D-potentiometer is set to 0 Ω . A value of 1.2 k Ω is selected for R3. Calculate the parallel resistance R2 using Equation 9.

$$R2 = \frac{(D_{POT_MAX} + R2) \times R_{LS_MAX}}{(D_{POT_MAX} + R2) - R_{LS_MAX}} = \frac{(7 \text{ k}\Omega + 1.2 \text{ k}\Omega) \times 3 \text{ k}\Omega}{(7 \text{ k}\Omega + 1.2 \text{ k}\Omega) - 3 \text{ k}\Omega} \quad (9)$$

4.4 Final Component Selection

Table 3 shows the components selected in order to be compliant with the SMT 0603 1% standard.

Table 3. SMT 0603 1% Resistors

RESISTOR	COMPUTED VALUES	0603 SMT 1% STANDARD
R1	600 Ω	604 Ω
R2	4730.8 Ω	4,750 Ω
R3	1200 Ω	1,200 Ω

Table 4 shows the final capacitor values used in the design.

Table 4. Capacitors

CAPACITORS	INDICATOR	VALUE
Input capacitor	C_{IN}	4.7 μF
Output capacitor	C_{OUT}	10 μF
Bypass capacitor	C_{SS}	0.01 μF
Feedforward capacitor	C_{FF}	0.005 μF

5 I²C Interface Details

The resistance of the TPL0401A-10 can be configured by transmitting a seven-bit address through a standard I²C interface. The communication maximum frequency is 400 KHz.

The bidirectional I²C bus consists of the serial clock (SCL) and serial data (SDA) lines. Both lines must be connected to a positive supply through a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

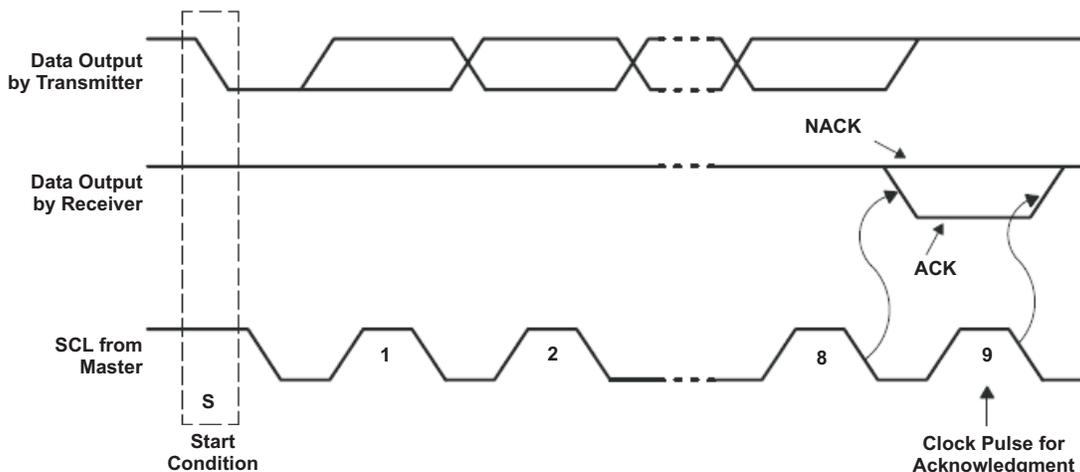


Figure 6. Data Transfer Digital Sequence

I²C communication with this device is initiated by the master sending the start condition, a high-to-low transition on the SDA output while the SCL is held high.

After the start condition, the device address byte is sent (0x2E), which is the most significant bit and it contains the data direction bit (R/W). The TPL0401A-10 device does not respond to the general call address. After receiving the valid address byte, this device responds with an ACK signal, which is a low on the SDA input or output during the high of the ACK-related clock pulse.

The stop condition is a low-to-high transition on the SDA output while the SCL input is held high. [Figure 7](#) is a graphical representation of the I²C interface sequence.

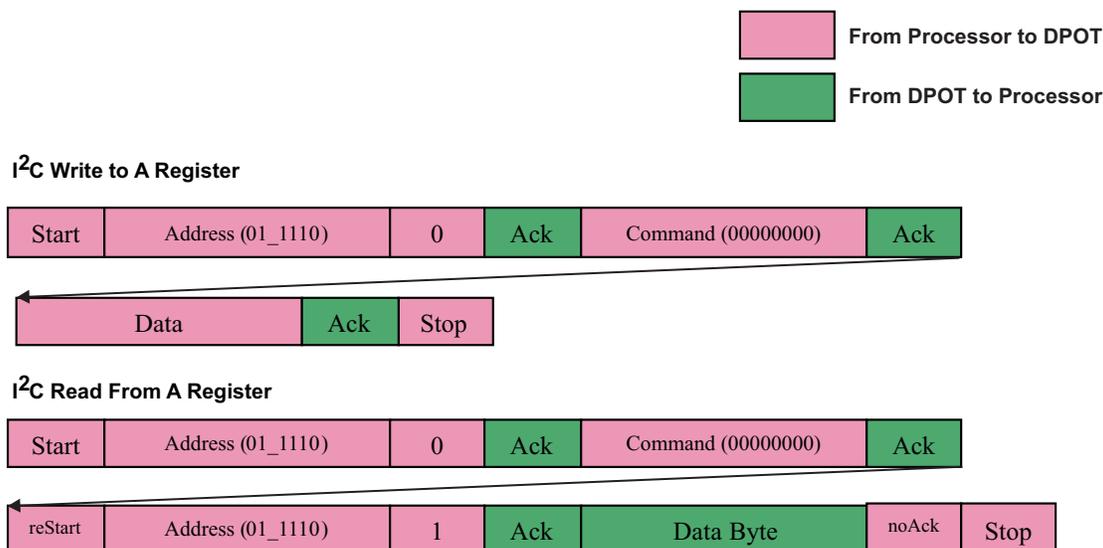


Figure 7. I²C Interface Details

For further information and details about the I²C interface, please refer to the [TPL0401A-10](#) datasheet.

5.1 Pull-Up Resistors

If the master microcontroller (MCU) or CPU has open-collector SDA and SCL lines, they must be connected to the supply voltage using pull-up resistors. Pulling the line up is necessary when the I²C lines are not driven low by the open-collector interface.

Selecting the correct resistor value is crucial because a small pull-up resistor can prevent the I²C lines from driving low enough to cross the logic low threshold. Conversely, a high resistor value may not allow the signal to rise to the logic high threshold before the digital signal is pulled low again.

The minimum pull-up resistance is a function of supply voltage (V_{DD}), max output low voltage (V_{OL}), and sink current (I_{OL}).

$$R_{P_MIN} = \frac{V_{CC} - V_{OL_MAX}}{I_{OL}} \quad (10)$$

The maximum pull-up resistance is limited by the capacitance in bus C_B , the bus capacitance is determined by the collective capacitance of all the pins and wire connections. The C_B and pull-up resistor form a resistor-capacitor (RC) circuit, which increases the slew rate of the digital signal due to the RC time constant. The maximum resistance can be determined by calculating the rising time constant using the input high voltage (V_{IH}), input low voltage (V_{IL}), and solving for the R_p equation and bus capacitance.

The following [Equation 11](#) is for the charging capacitor:

$$V_T = V_{CC} \times \left(1 - e^{-\frac{t}{R_P \times C_B}} \right)$$

where

- solving for $V_{IH} = V_{CC} \times 0.7 \geq T_1 = 1.203970 \times RC$
- solving for $V_{IL} = V_{CC} \times 0.3 \geq T_2 = 0.3556675 \times RC$

The rising time of the I²C bus can be written as:

$$T_R = T_2 - T_1 = 0.847298 \times R_P \times C_B \quad (12)$$

Solve for R_p to find the maximum pull-up resistance, as [Equation 13](#) shows.

$$R_{P_MAX} = \frac{T_R}{0.8473 \times C_B} \quad (13)$$

Select a pull-up resistor in the middle of the range to provide as much guard bandwidth as possible.

$$\frac{V_{CC} - V_{OL_MAX}}{I_{OL}} \leq R_P \leq \frac{T_R}{0.8473 \times C_B} \quad (14)$$

For more detailed information and parameters about the I²C interface, please refer to the [SLVA689](#) application note.

6 Layout Guidelines

Be sure to use the proper printed circuit board (PCB) layout procedures to avoid instability caused by ground loops and voltage drops. The input and output capacitors must be directly connected to the input, output, and ground pins of the regulator using traces which do not have other currents flowing throughout (Kelvin connect).

The best way to make this connection is to lay C_{IN} and C_{OUT} near the device with short traces to the V_{IN} , V_{OUT} , and ground pins. The regulator ground pin must be connected to the external circuit ground so that the regulator and its capacitors have a single point to ground.

Note that some stability problems have been seen in applications where using vias to an internal ground plane at the ground points of the IC, input capacitors, and output capacitors. This instability is caused by varying ground potentials at these nodes as a result of the current flowing through the ground plane. Using a single-point ground technique for the regulator and the capacitors fixes the problem. Because a high current flows through the traces going into V_{IN} and coming from V_{OUT} , TI recommends to use a four-terminal connection or “Kelvin connection” for the capacitor leads to these pins to prevent a voltage drop in series with the input and output capacitors.

7 Test Results

7.1 Equipment Used

Table 5 is a list of the test equipment used in the previous sections.

Table 5. Test Equipment

TEST EQUIPMENT	PART NUMBER
Oscilloscope	Agilent MSO7034B
Voltage supply	Agilent E61A
Network analyzer	Agilent E5061B

7.2 Default Output Voltage at Start-Up

Table 6 shows the start-up default settings of the system. The default start-up resistance value of TPL0401A-10 is typically at a mid-scale value (5 k Ω).

Table 6. Default Output Voltage Settings

HEX D _{POT} STEP	R _{HW} (Ω)	R _{HW} + R3	(R _{HW} + R3) R2	V _{OUT}
0x3F	5080 Ω	6280 Ω	2704.4 Ω	1.23 V

7.3 Power Output Settings

To simplify the evaluation procedure, the PCB was designed as a BoosterPack evaluation module (EVM), which fits on a variety of low-cost LaunchPads. The [MSP-EXP430FR5969™](#) LaunchPad was used to set the wiper values of the digital potentiometer. Access the sample I²C source code online at the following link: <http://dev.ti.com/tirex/#/DevTool/MSP-EXP430FR5969/Package/MSPWare>.

As Figure 8 shows, the connections between TIDA-00531 and LaunchPad must align. P1.6 and P1.7 are the I²C channels of the LaunchPad used in this evaluation. The GPIO signal must be high between 1.4 V and V_{IN} to enable the LP3878 device.

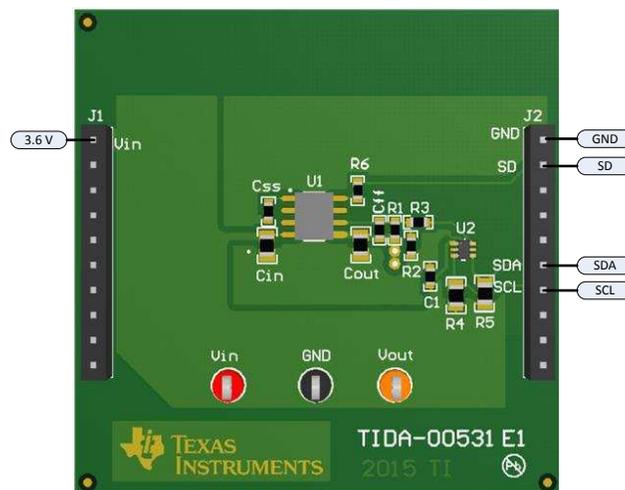


Figure 8. TIDA-00531 Connections With LaunchPad

Table 7 shows the output voltage settings at the output voltage of interest in the TIDA-00531 reference design.

Table 7. Output Voltage Settings

HEX D _{POT} STEP	R _{HW} (Ω)	R _{HW} + R3	(R _{HW} + R3) R2	V _{OUT}
0x7F	80 Ω	1280 Ω	1008 Ω	1.60 V
0x6C	1560 Ω	2760 Ω	1745.7 Ω	1.35 V
0x26	7030 Ω	8230 Ω	3011.7 Ω	1.20 V

7.4 Input Voltage Versus Output Voltage

The regulated output voltage remains stable at various input voltage levels. Figure 9 shows the system output voltage at various input voltage levels.

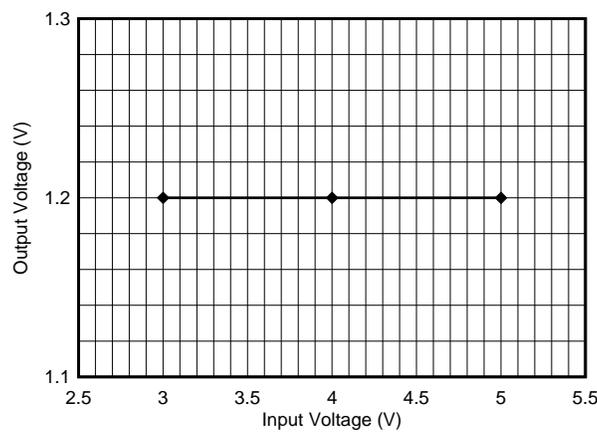


Figure 9. Output Voltage Versus Input Voltage

7.5 Power Supply Rejection Ratio

The output voltage ripple rejection ratio was calculated by comparing the regulated output voltage ripple to the input voltage ripple of 50 mV over a frequency range of 10 Hz to 10 MHz.

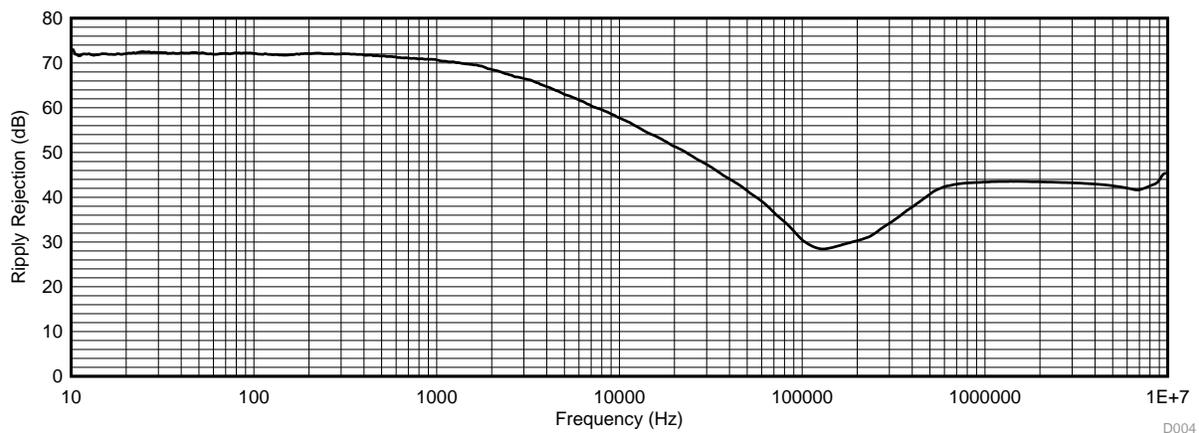


Figure 10. Ripple Rejection

7.6 Start-Up and Shut Down Transition

This test was done by removing or applying 3.6 V at the input voltage and measuring the transients at the output voltage pin. The voltage output was left in the default start-up state. The rising time from 0 V to 1.23 V took approximately 16 μ s. The falling time from 1.23 V to 0 V took an approximate 53 ms with a 10- μ F cap at the output pin to ground. [Figure 11](#) and [Figure 12](#) are scope shots of the output voltage during start-up and shut down.

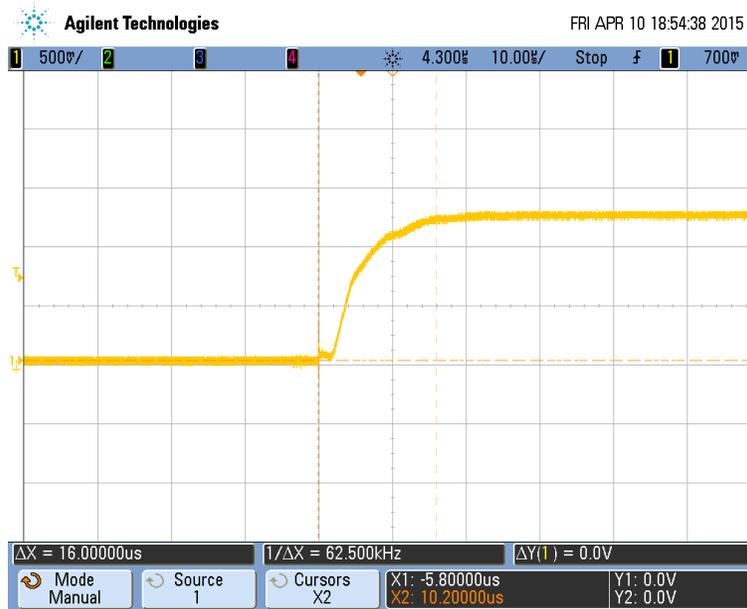


Figure 11. Start-Up Output Voltage Transient

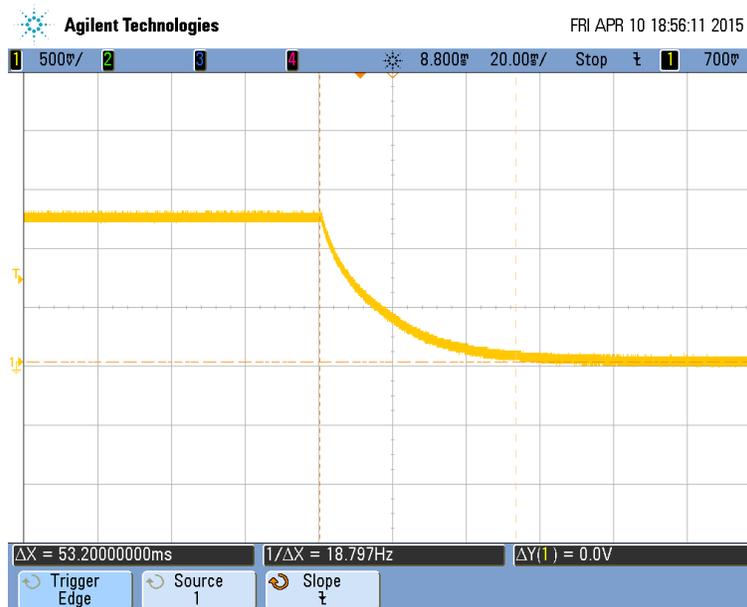


Figure 12. Shut Down Output Voltage Transient

7.7 Voltage Steps Resolution

Figure 13 shows a graph of the computational results of the output voltage versus the R_{HW} resistance of the digital potentiometer.

The user can expect to have a resolution of 90 steps with a typical digital potentiometer .

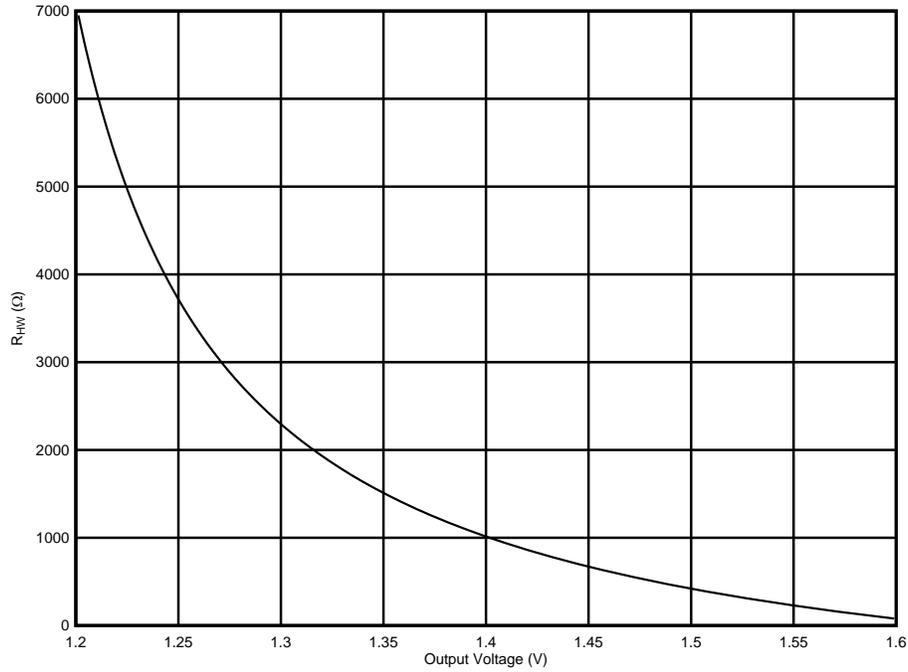


Figure 13. Digital Potentiometer Resistance Versus Output Voltage

8 Design Files

8.1 Schematics

To download the schematics, see the design files at [TIDA-00531](#).

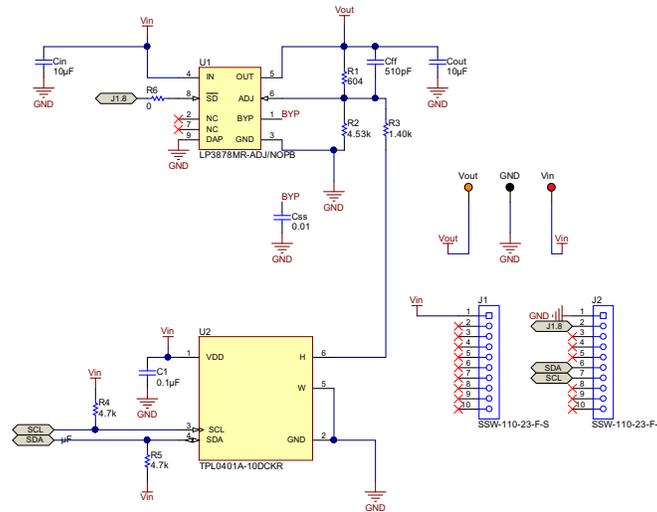


Figure 14. TIDA-00531 Schematic

8.2 Bill of Materials

To download the bill of materials (BOM), see the design files at [TIDA-00531](#).

8.3 Layout Prints

To download the layout prints, see the design files at [TIDA-00531](#).

8.4 Layout Guidelines

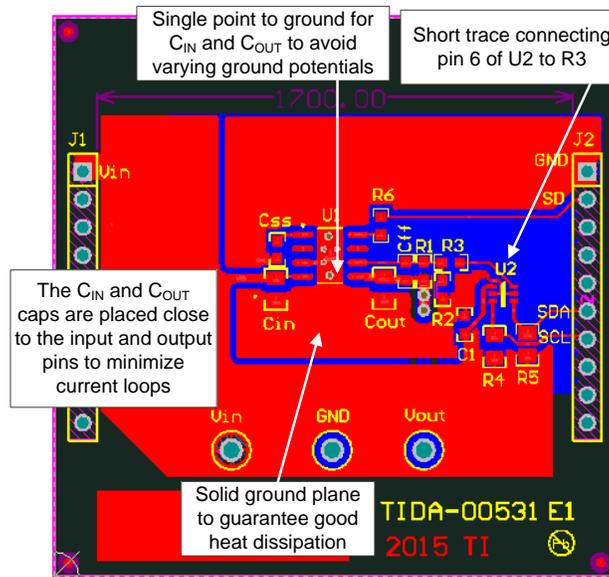


Figure 15. Layout Guidelines

8.5 Gerber Files

To download the Gerber files, see the design files at [TIDA-00531](#).

9 References

1. Texas Instruments; Lestor, Scot; *System Power Savings Using Dynamic Voltage Scaling*, TI Developer Conference: March 2014, ([SPRP571](#))
2. Texas Instruments; *Adaptive (Dynamic) Voltage (Frequency) Scaling — Motivation and Implementation*, Application Report, ([SLVA646](#))
3. ACM Digital Library; Pouwelse, Johan; Langendoen, Koen; Sips, Henk; *Dynamic voltage scaling on a low-power microprocessor*, Article, <http://dl.acm.org/citation.cfm?id=381701>
4. IEEE Xplore® Digital Library; Bai, Ying-Wen; *Using the load current of the CPU to dynamically control the voltage and reduce the power consumption of PC systems*, Article, http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=6229211&tag=1

10 About the Author

ANTONY PIERRE CARVAJALES is an Applications Engineer on the mobile power devices RF power group at Texas Instruments; Antony has worked in various business units expanding his knowledge in analog circuitry design to help customers solve their design challenges using TI technologies. Antony earned his Bachelors of Science in Electrical Engineering from Florida International University; FL.

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