PMP10630
Test Report
03/31/2015

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I. Overview

The PMP10630 reference design is a complete high density power solution for Xilinx® Kintex® UltraScale™ XCKU040 FPGA. This design uses an optimal combination of SIMPLE SWITCHER® modules and LDOs to provide all the necessary voltage rails in a small solution size of 36 x 43 mm (1.4 x 1.7 inch). The design includes the LMZ31704 LMZ3 series module to power the core rail and three LMZ21700/1 Nano series modules. The design manages the proper power sequencing using LM3880 sequencer, and it also has an optional DDR3 memory power supply featuring the LP2998 DDR termination regulator. The reference design takes 12V DC input voltage, and the total output power is 6W. The power block diagram is shown in Figure 1.

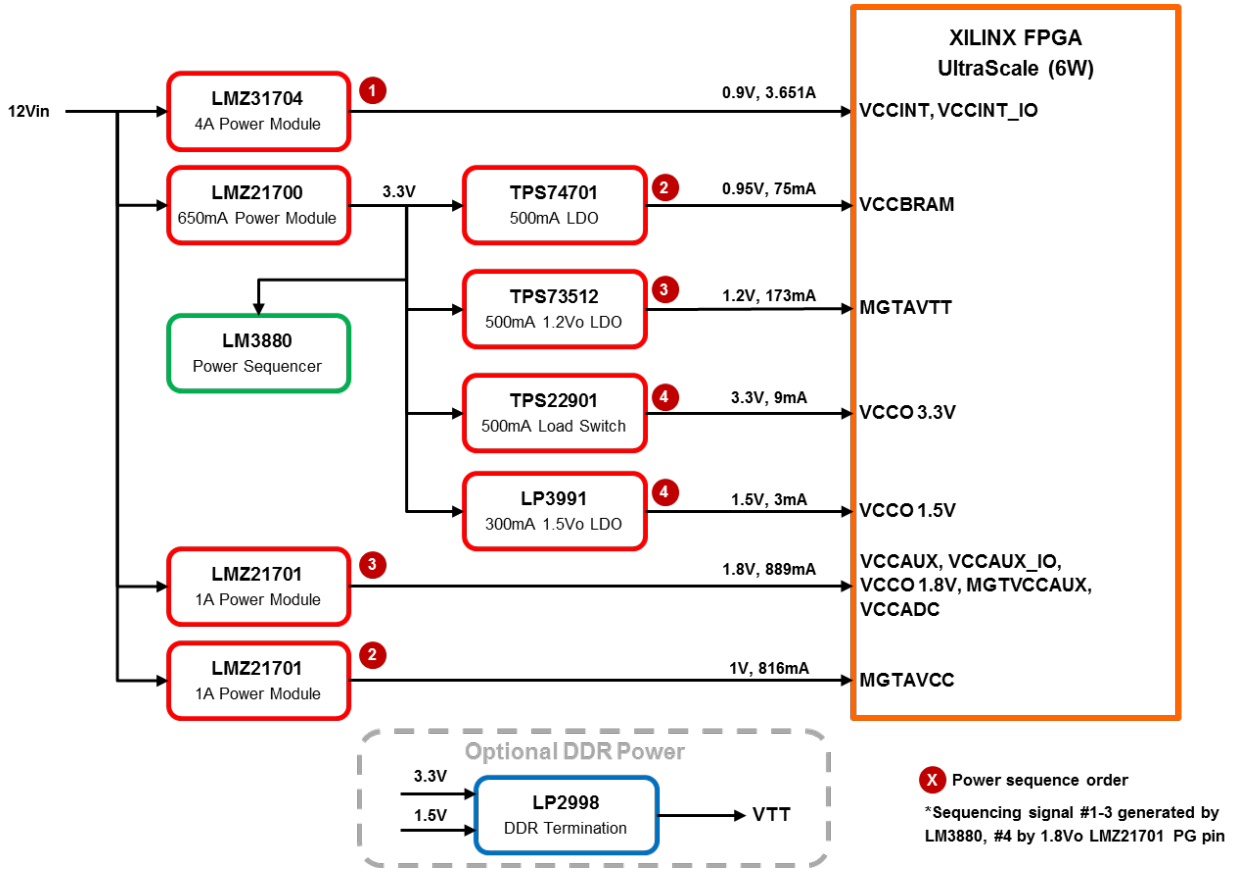

Figure 1 Power supply block diagram

II. Power Specification

Input Voltage: 12V

Outputs (in power sequence order):

1. VCCINT, VCCINT_IO, 0.9V @ 3.651A
2. VCCBRAM, 0.95V @ 75mA
   MGTAVCC, 1V @ 816mA
3. MGTAVTT, 1.2V @173mA
   VCCAUX, VCCAUX_IO, VCCO 1.8V, MGTVCCAUX, VCCADC, 1.8V @ 889mA
4. VCCO 3.3V, 3.3V @ 9mA
   VCCO 1.5V, 1.5V @ 3mA

Total output power: 6W

III. Reference Board

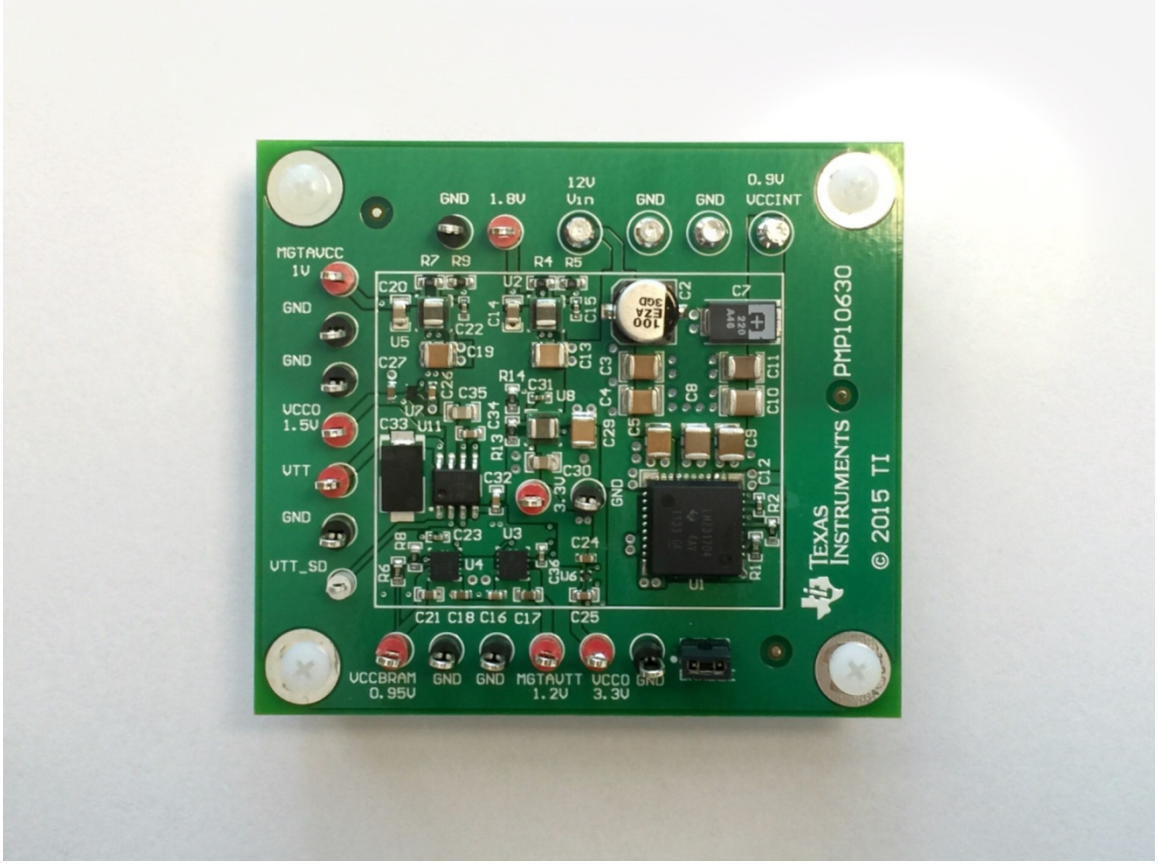

Figure 2 Reference board top view

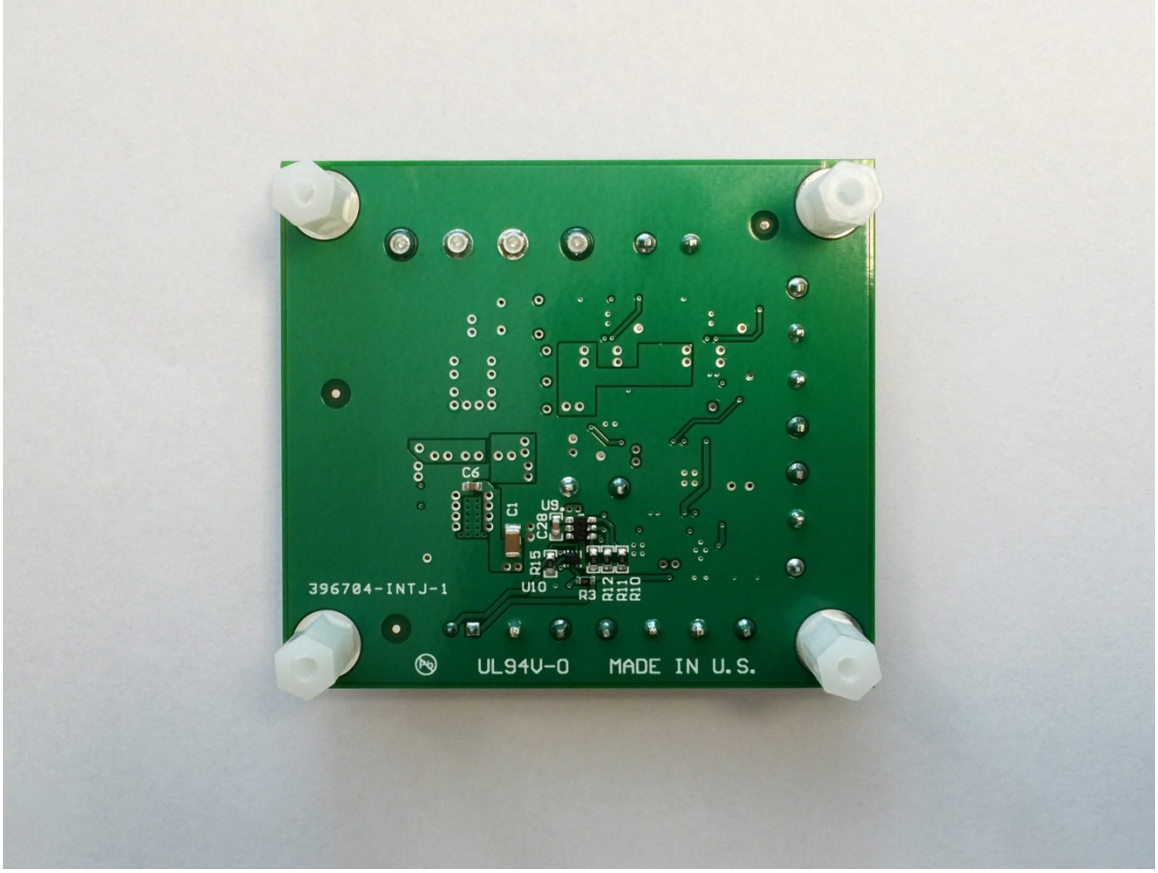

Figure 3 Reference board bottom view

The board size is 61 x 69 mm (2.4 x 2.7 inch).

The component area is 36 x 43 mm (1.4 x 1.7 inch).

IV. Power Sequencing

In order to achieve minimum current draw, the recommended power up sequence of the UltraScale™ FPGA is as follows:

VCCINT/VCCINT_IO => VCCBRAM => VCCAUX/VCCAUX_IO => VCCO
VCCINT => MGTAVCC => MGTAVTT
No recommended sequencing for MGTAVCCAUX
If the voltage levels are the same for some of the rails, they can be powered up simultaneously.

The power down sequence is recommended as the reverse of the power up.

To implement this power sequence, the reference design group the voltage rails into 4 sequencing order (see Figure 1). Since the LM3880 sequencer has 3 enable signal outputs, the 4th enable signal is generated from the logic AND signal of the system enable and the PG signal of the LMZ21701, which is the power module for the 3rd power-up rail VCCAUX 1.8V. The LM3880 has the reverse sequence for power down, so the recommended power down sequence is also ensured. The sequencing circuit is shown in Figure 4. The system enable is the “ENABLE” jumper header on the reference board.

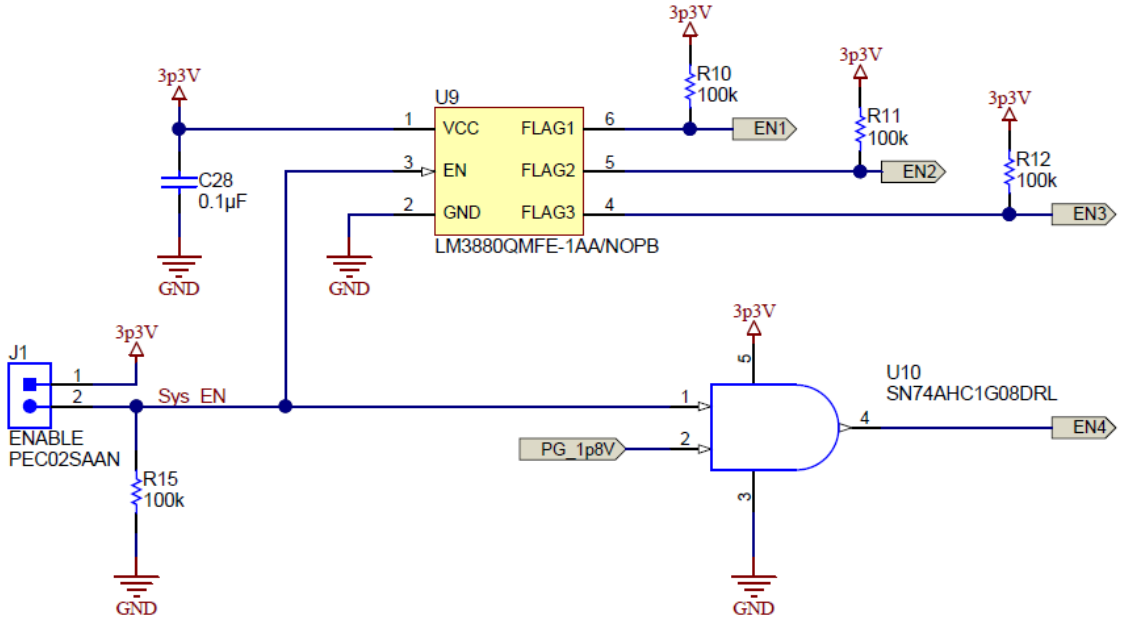

Figure 4 Power sequencing circuit

Figure 5 and Figure 6 shows the power up and down sequence of 4 voltage rails. It was tested by toggling the ENABLE jumper. Ch1 (yellow) is the VCCINT 0.9V voltage, Ch2 (green) is the MGTAVCC 1V voltage, Ch3 (purple) is the MGTAVTT 1.2V voltage, and Ch4 (magenta) is the VCCO 3.3V voltage.

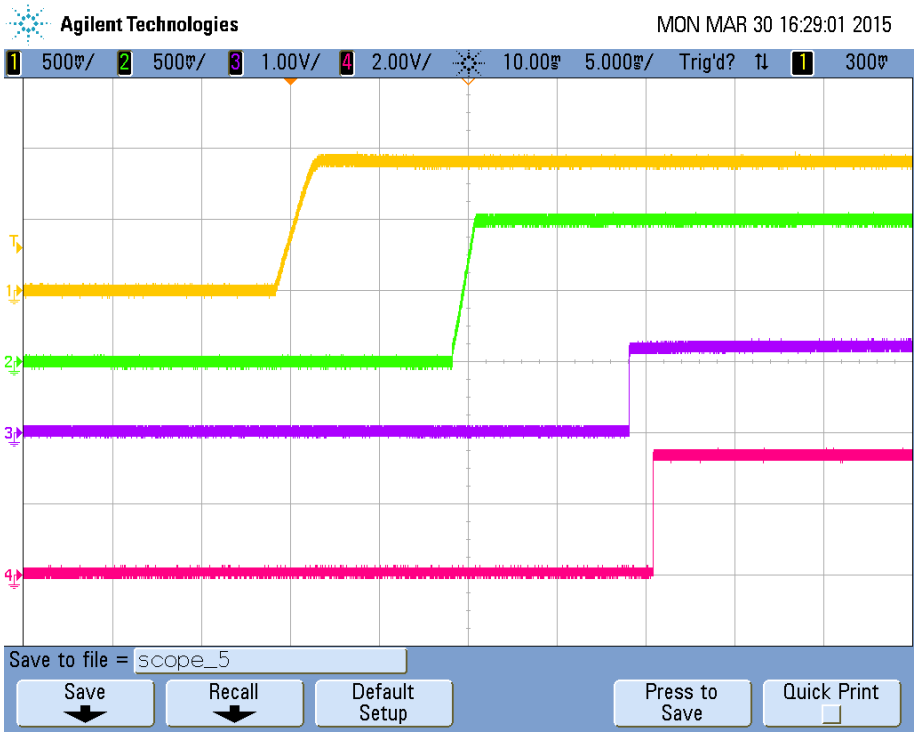

Figure 5 Power up sequence of VCCINT 0.9V, MGTAVCC 1V, MGTAVTT 1.2V, VCCO 3.3V

Figure 6 Power down sequence of VCCINT 0.9V, MGTAVCC 1V, MGTAVTT 1.2V, VCCO 3.3V

The power up timing for the input voltage and all the rails are shown in Figure 7 - Figure 10. It was tested by turning on the 12V input with ENABLE jumper already shorted.

1. Ch1 (yellow) is the 12V input voltage, Ch2 (green) is the VCCINT 0.9V voltage, Ch3 (purple) is the VCCBRAM 0.95V voltage, and Ch4 (magenta) is the MGTAVCC 1V voltage.

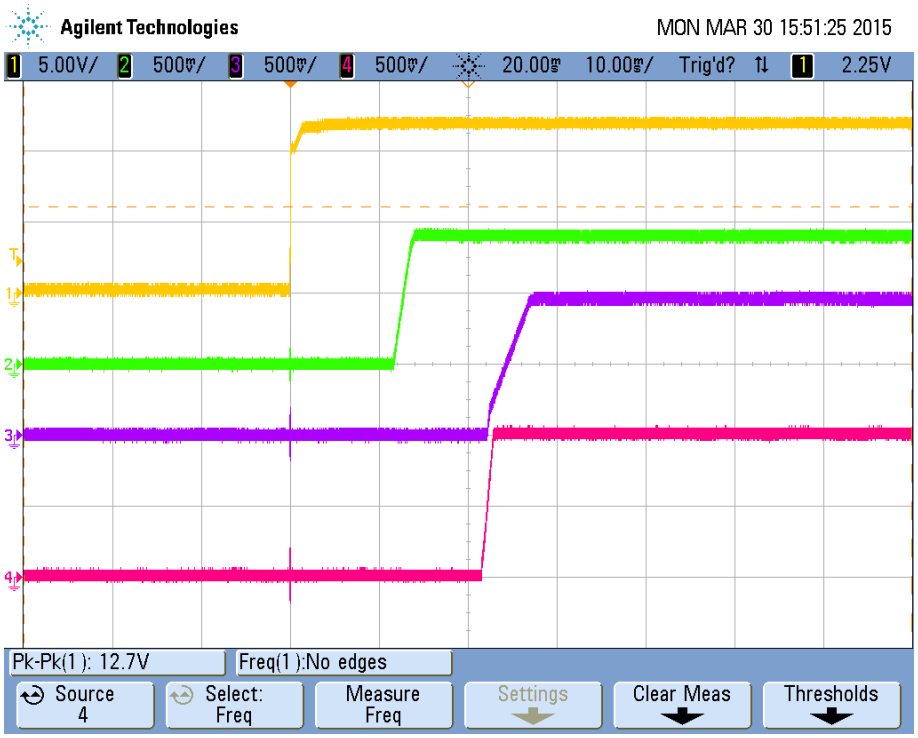

Figure 7 Power up timing of Vin 12V, VCCINT 0.9V, VCCBRAM 0.95V, MGTAVCC 1V

2. Ch1 (yellow) is the 12V input voltage, Ch2 (green) is the MGTAVTT 1.2V voltage, Ch3 (purple) is the VCCAUX 1.8V voltage, and Ch4 (magenta) is the VCCO 3.3V voltage.

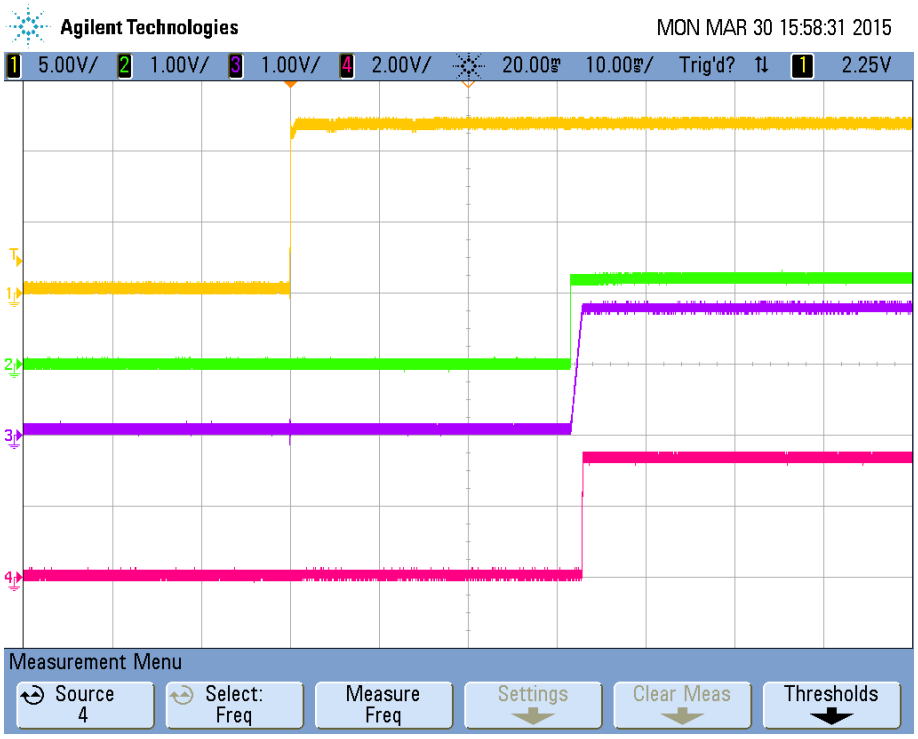

Figure 8 Power up timing of Vin 12V, MGTAVTT 1.2V, VCCAUX 1.8V, VCCO 3.3V

3. Ch1 (yellow) is the 12V input voltage, Ch2 (green) is the MGTAVTT 1.2V voltage, Ch3 (purple) is the VCCO 1.5V voltage, and Ch4 (magenta) is the VCCO 3.3V voltage.

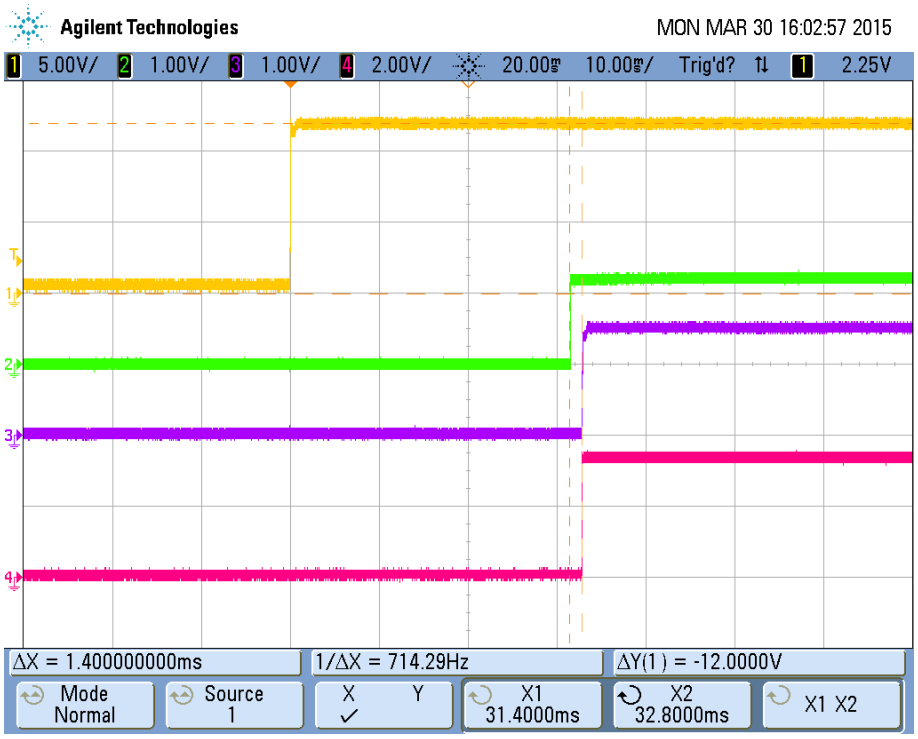

Figure 9 Power up timing of Vin 12V, MGTAVTT 1.2V, VCCO 1.5V, VCCO 3.3V

4. Ch1 (yellow) is the 12V input voltage, Ch2 (green) is the system aux supply 3.3V voltage, Ch3 (purple) is the VCCO 1.5V voltage, and Ch4 (magenta) is the VTT 0.75V voltage from the LP2998.

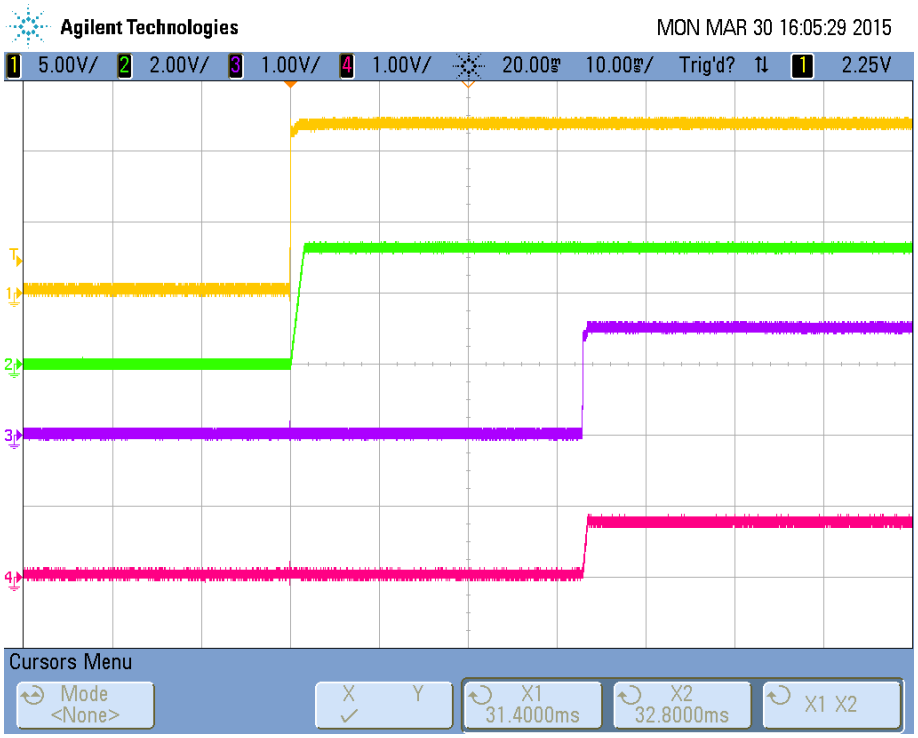

Figure 10 Power up timing of Vin 12V, VAUX 3.3V, VCCO 1.5V, VTT 0.75V

V. Efficiency

The efficiency was measured at full load for all the rails, and the efficiency for each power module was also measured separately. All tests were taken at 12V input.

Full load efficiency data:

Outputs	Vo (V)	Io (A)	Po (W)
VCCINT 0.9V	0.891	3.651	3.252
VCCBRAM 0.95V	0.950	0.095	0.090
MGTAVTT 1.2V	1.181	0.236	0.279
VCCO 3.3V	3.315	0.010	0.033
VCCO 1.5V	1.500	0.003	0.005
VCCAUX 1.8V	1.777	0.890	1.582
MGTAVCC 1V	0.988	0.833	0.823
		Total Po	6.064
Input	**Vin(V)**	**Iin (A)**	**Pin (W)**
	12.045	0.692	8.334
		Efficiency	**72.8%**

Note that some of the loads were a little higher than the max current in the full load condition. It is because some of the load resistor used didn't match the exact full load.

The efficiency data of three power modules were measured separately. They are the LMZ31704 module for VCCINT 0.9V and two LMZ21701 modules for MGTAVCC 1V and VCCAUX 1.8V, which cover all the relatively high current rails in the design. When one module's efficiency was measured, the other unconcerned enable signals were disabled by connecting the sequencer outputs to GND and removing the pull-up resistors. The efficiency plots are shown in Figure 11 - Figure 13, the test data can be found in the Appendix .

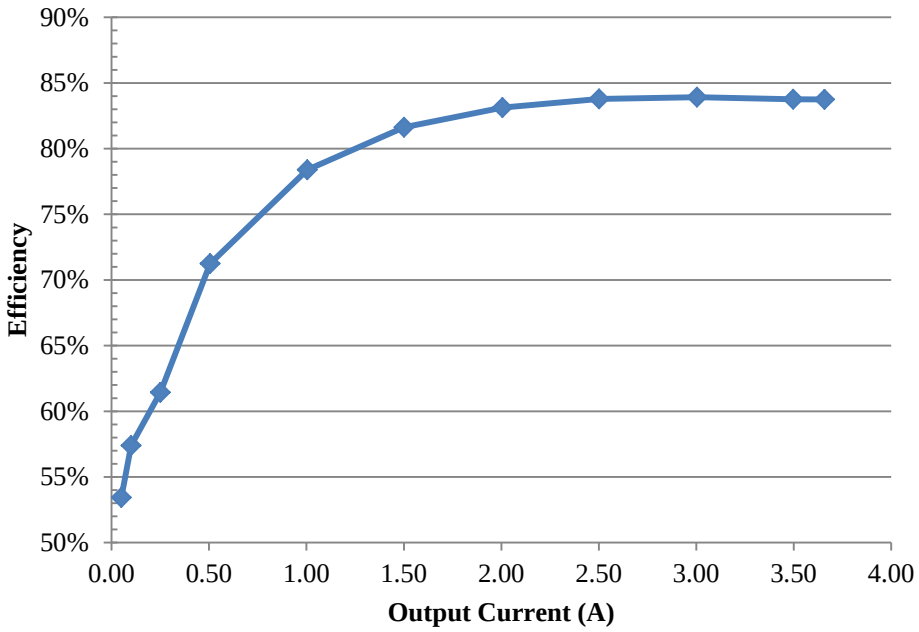

Figure 11 Power efficiency of VCCINT 0.9V output

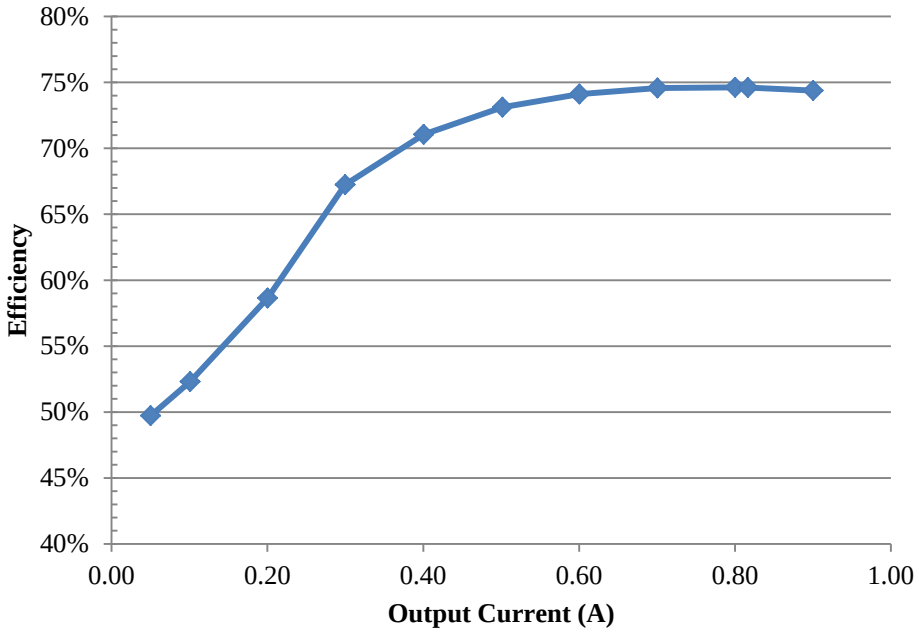

Figure 12 Power efficiency of MGTAVCC 1V output

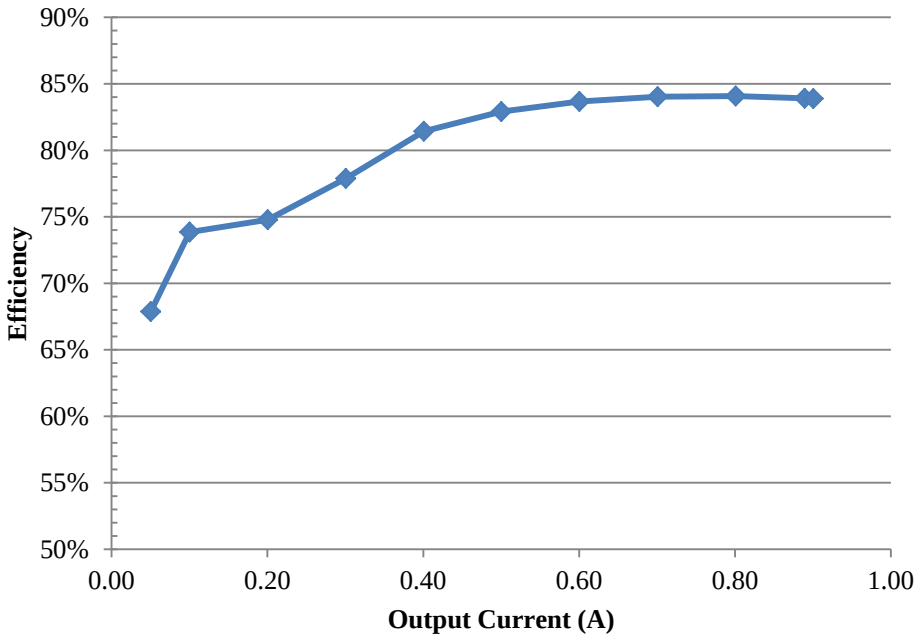

Figure 13 Power efficiency of VCCAUX 1.8V output

Since the LMZ21700 for the 3.3V system aux supply and the LM3880 sequencer were not disabled, the measured efficiency for each module is slightly lower than the actual number. The system aux supply and sequencer consumed power was measured by disabling all enable signal, and the reading is as follows: Vin=12.045V, Iin= 0.225mA, Paux=2.7mW. Subtracting this power from the input power can get a better estimate to the actual efficiency.

VI. Thermal

The thermal image was taken at 23°C room temperature, no air flow. The board was operating at 12V input, full load on all outputs (same condition as in the full load efficiency test).

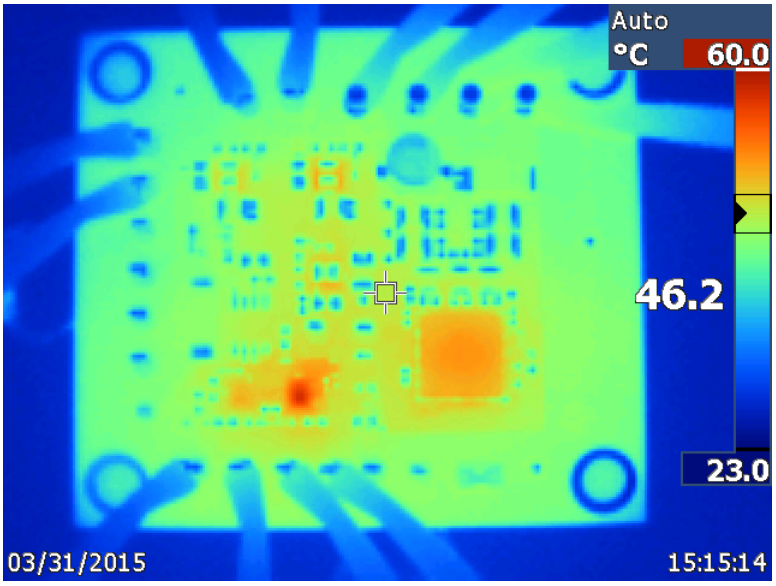

Figure 14 Thermal image from top view

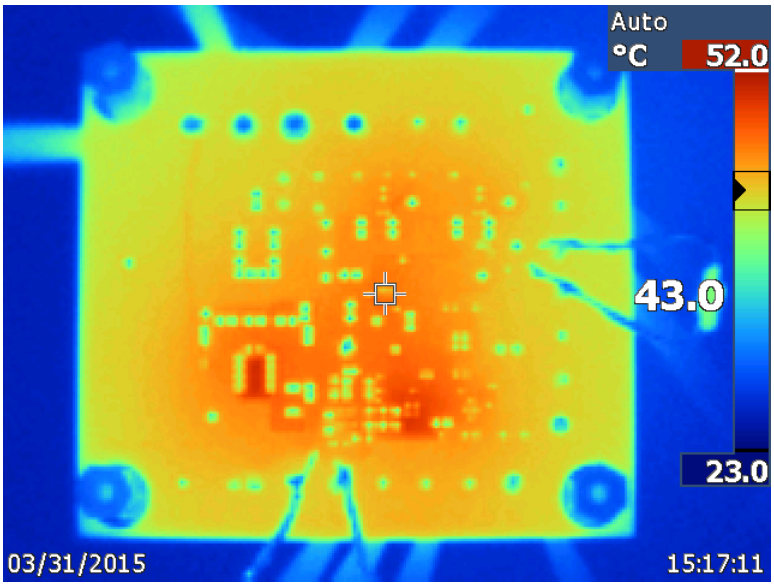

Figure 15 Thermal image from bottom view

VII. Regulation

The regulation was measured on three power module outputs, VCCINT 0.9V, MGTAVCC 1V and VCCAUX 1.8V.

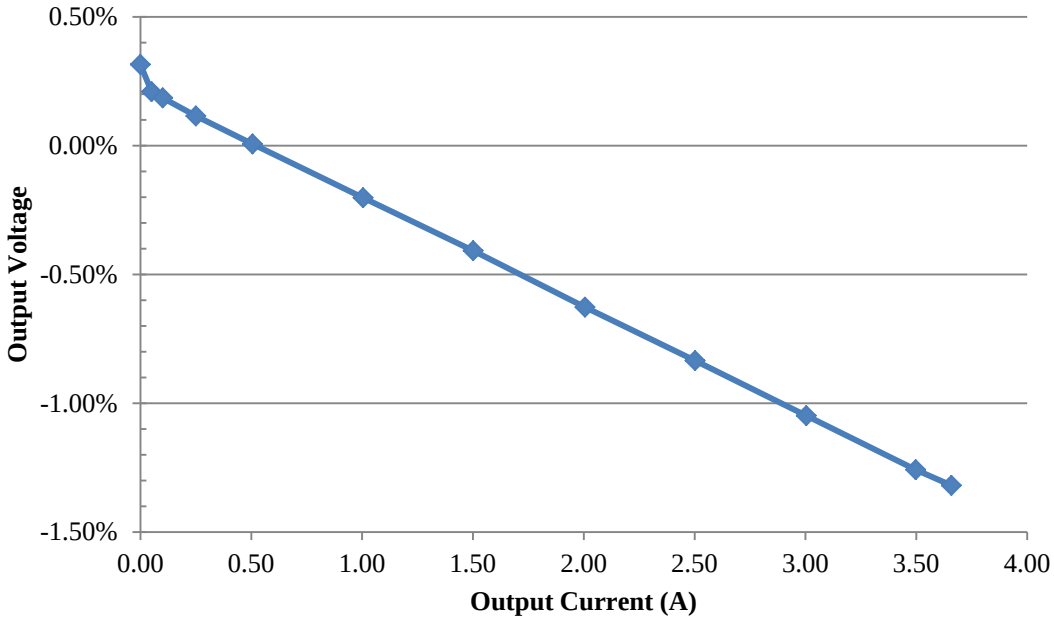

Figure 16 Output regulation of VCCINT 0.9V output

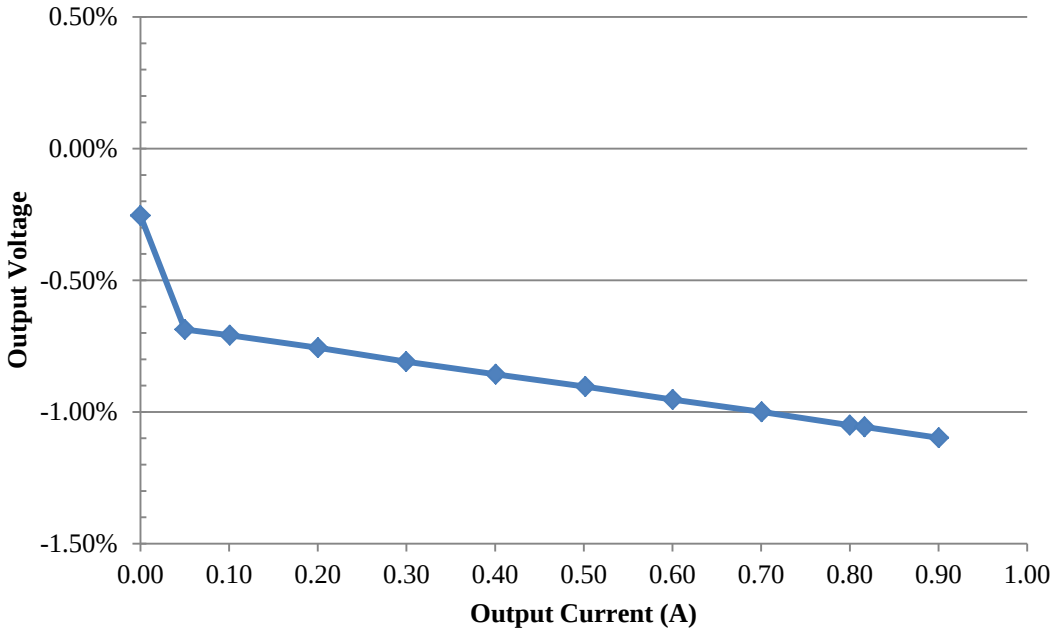

Figure 17 Output regulation of MGTAVCC 1V output

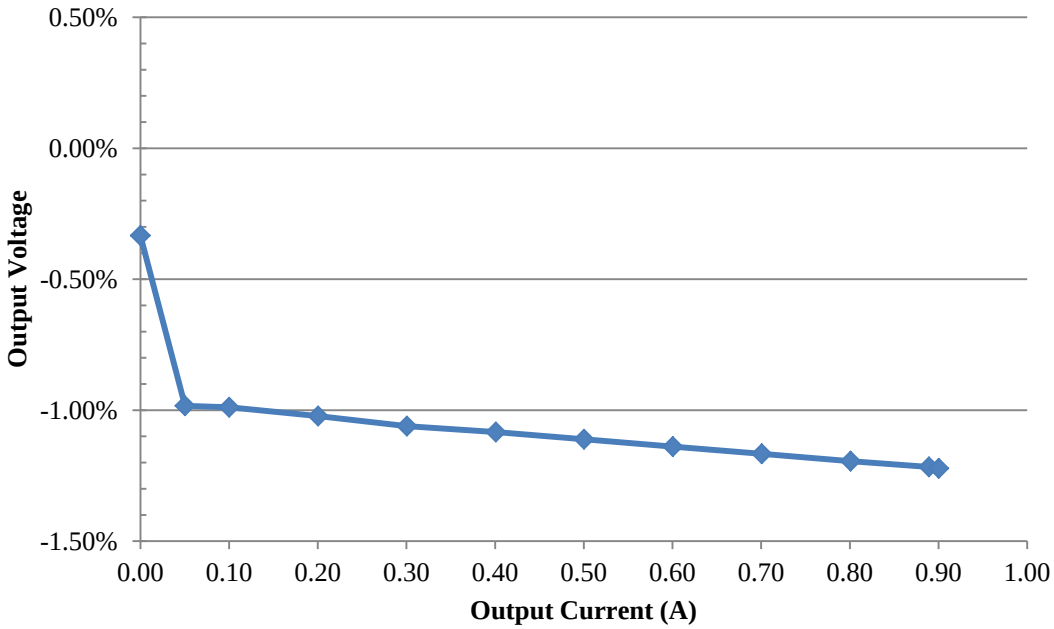

Figure 18 Output regulation of VCCAUX 1.8V output

VIII. Load Transients

The load transient response was tested by applying load steps from 0 to 50% on three power module outputs, VCCINT 0.9V, MGTAVCC 1V and VCCAUX 1.8V at 12V input. Ch1 (yellow) is the output voltage in AC mode, and Ch4 (magenta) is the output current.

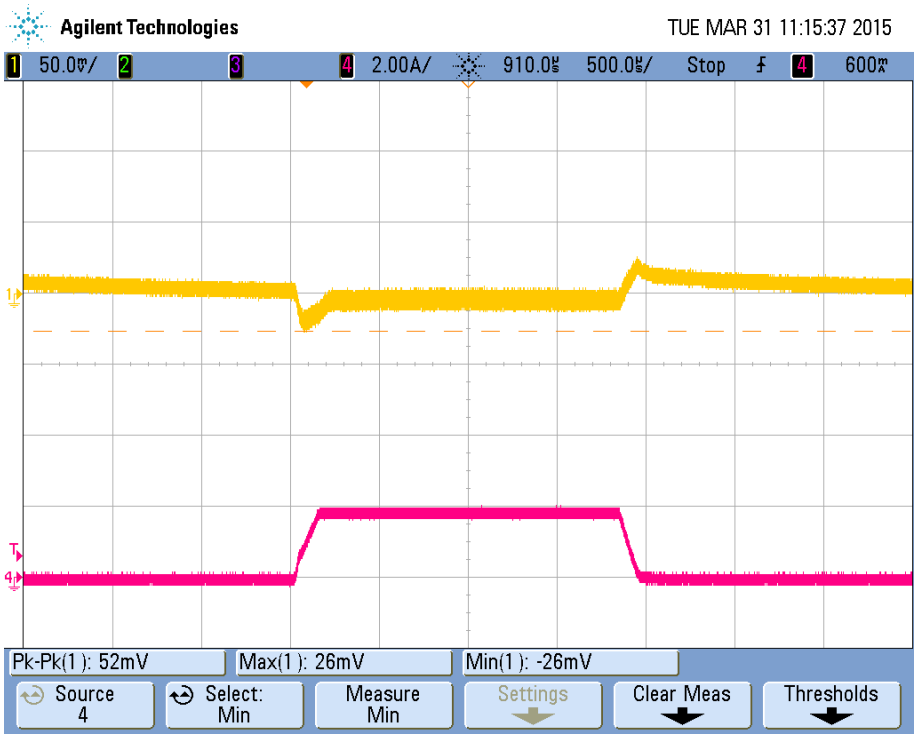

Figure 19 Output load transient of VCCINT 0.9V output

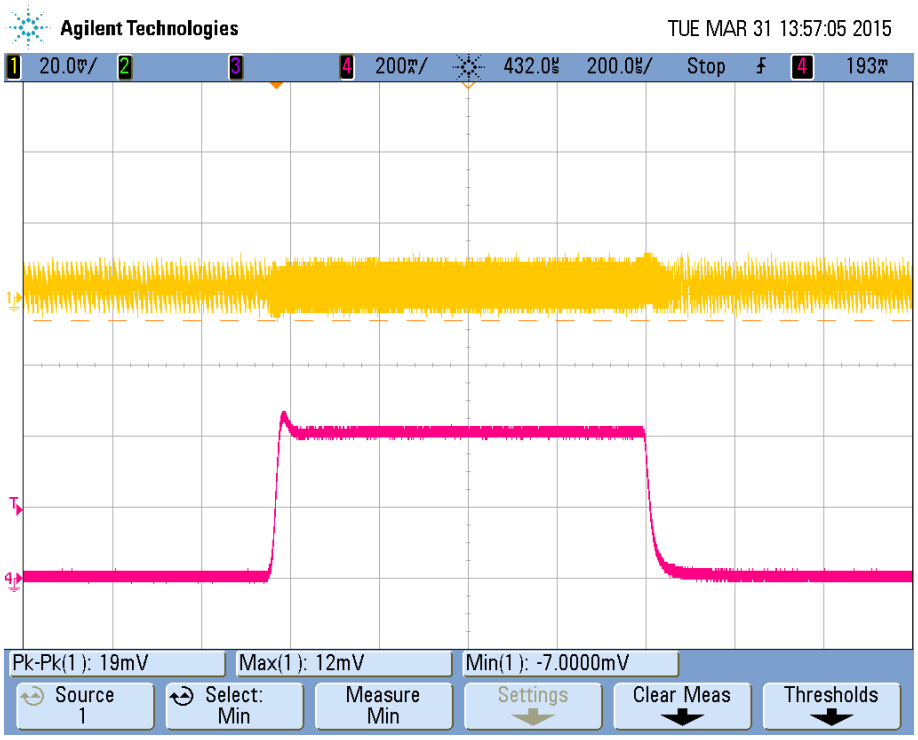

Figure 20 Output load transient of MGTAVCC 1V output

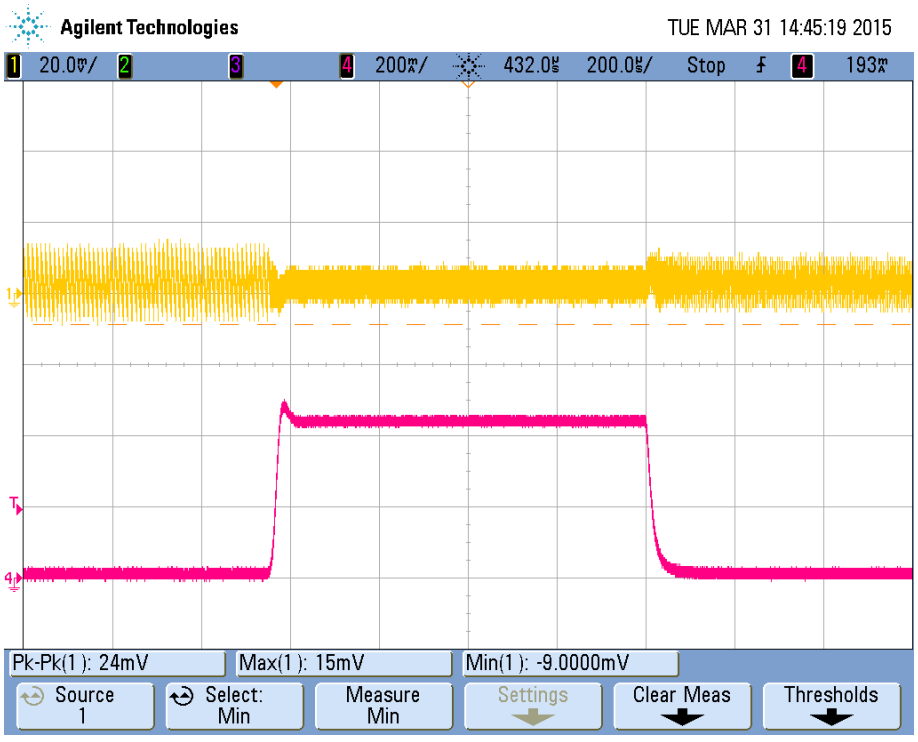

Figure 21 Output load transient of VCCAUX 1.8V output

IX. Output Voltage Ripples

The output ripples were measured directly at the output capacitors. Three power module outputs, VCCINT 0.9V, MGTAVCC 1V and VCCAUX 1.8V, were measured. Ch1 (yellow) is the output voltage ripple in AC mode.

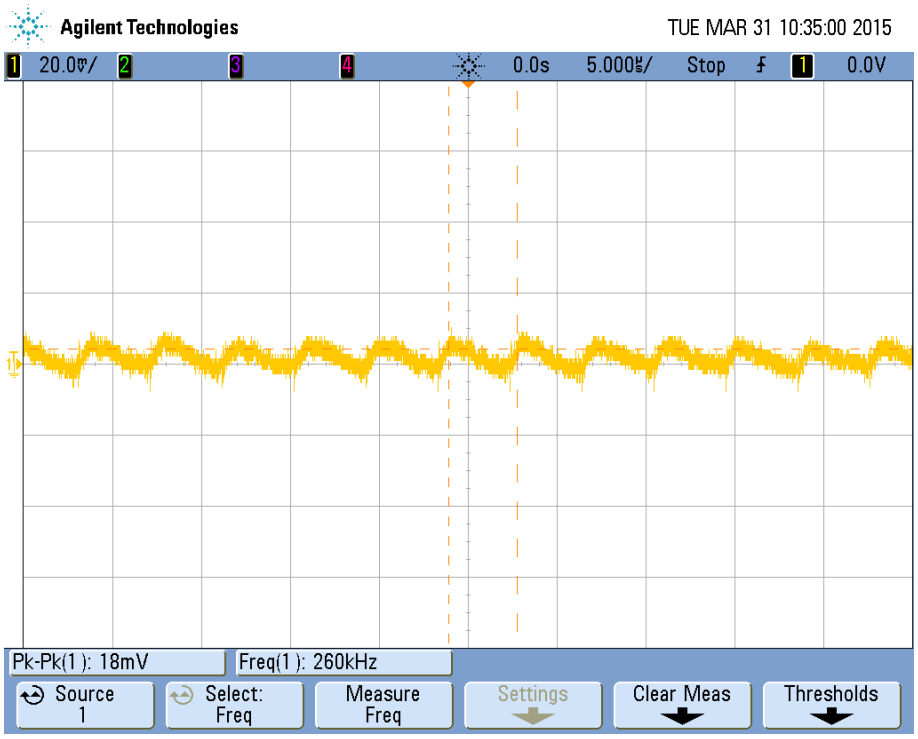

Figure 22 Output ripple of VCCINT 0.9V output at full load, 12Vin

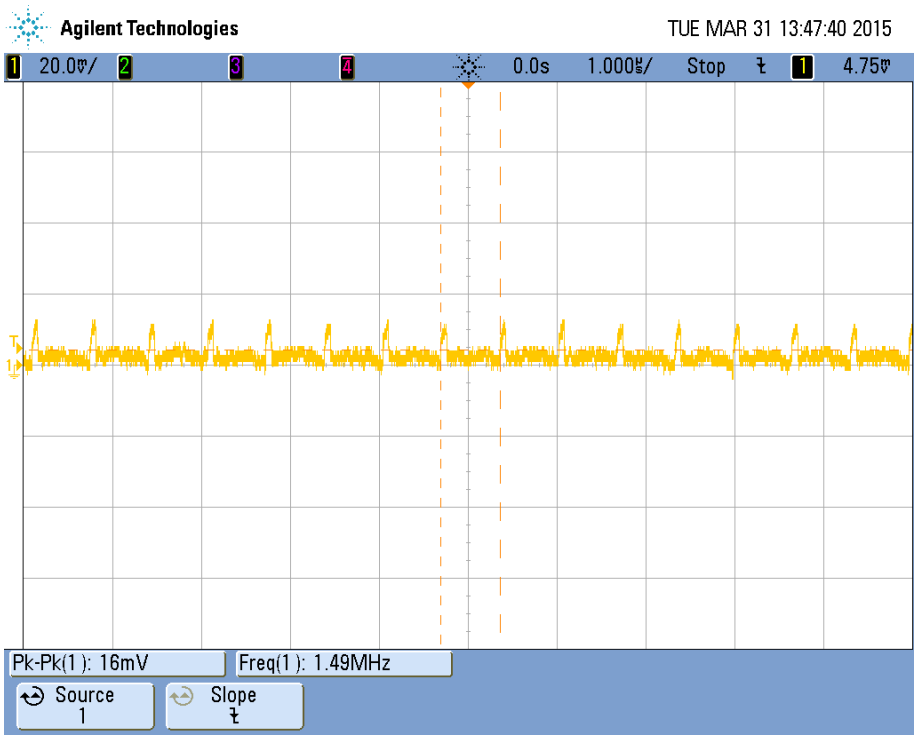

Figure 23 Output ripple of MGTAVCC 1V output at full load, 12Vin

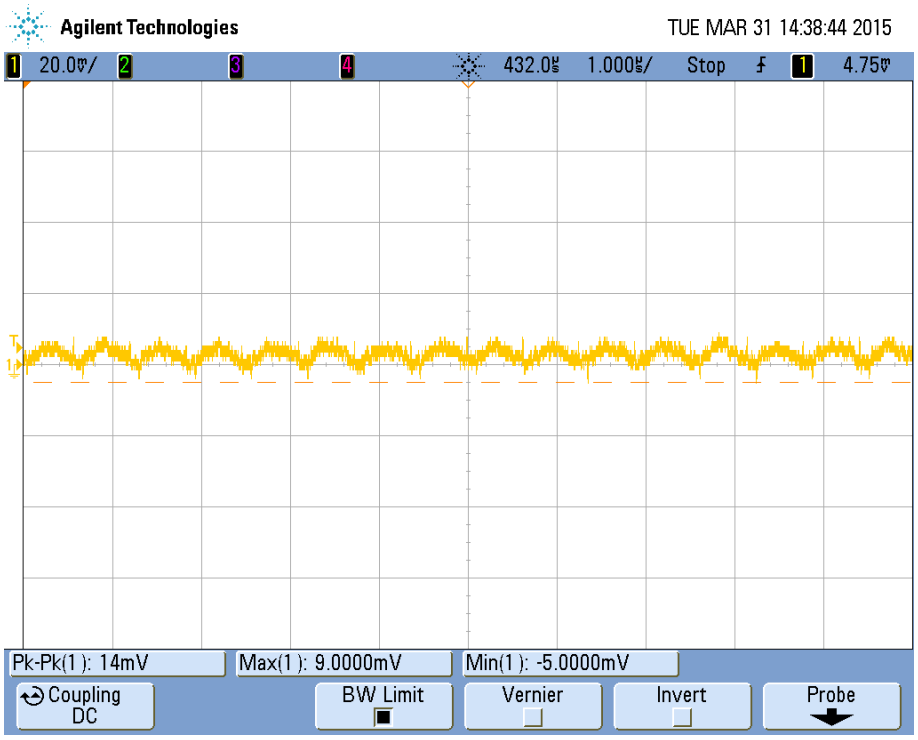

Figure 24 Output ripple of VCCAUX 1.8V output at full load, 12Vin

Appendix: Efficiency and Regulation Test Data

VCCINT 0.9V (EN2, EN3, EN4 disabled)

Vin(V)	Iin(A)	Vout(V)	Iout(A)	Efficiency (%)
11.996	8.54E-04	0.903	0.000	0.0%
12.011	7.06E-03	0.902	0.050	53.4%
12.077	0.013	0.902	0.101	57.4%
12.081	0.030	0.901	0.250	61.4%
12.055	0.053	0.900	0.506	71.2%
12.017	0.096	0.898	1.004	78.4%
12.023	0.137	0.896	1.501	81.6%
12.099	0.178	0.894	2.005	83.1%
12.075	0.221	0.892	2.502	83.8%
12.050	0.265	0.891	3.004	83.9%
12.025	0.309	0.889	3.498	83.8%
12.017	0.323	0.888	3.658	83.7%

MGTAVCC 1V (EN1, EN3, EN4 disabled)

Vin(V)	Iin(A)	Vout(V)	Iout(A)	Efficiency (%)
12.046	6.70E-04	0.997	0.000	0.0%
12.003	8.34E-03	0.993	0.050	49.7%
12.062	0.016	0.993	0.101	52.3%
11.992	0.028	0.992	0.200	58.6%
12.004	0.037	0.992	0.300	67.2%
12.010	0.047	0.991	0.401	71.1%
12.004	0.057	0.991	0.502	73.1%
12.028	0.067	0.990	0.600	74.1%
12.007	0.077	0.990	0.701	74.6%
11.997	0.088	0.990	0.800	74.6%
11.986	0.090	0.989	0.817	74.6%
12.004	0.100	0.989	0.900	74.4%

VCCAUX 1.8V (EN1, EN2, EN4 disabled)

Vin(V)	Iin(A)	Vout(V)	Iout(A)	Efficiency (%)
12.009	2.73E-04	1.794	0.000	0.0%
12.019	1.10E-02	1.782	0.050	67.9%
12.069	0.020	1.782	0.100	73.8%
12.019	0.040	1.782	0.200	74.8%
12.022	0.057	1.781	0.301	77.9%
12.034	0.073	1.781	0.401	81.4%
12.044	0.089	1.780	0.500	82.9%
12.049	0.106	1.780	0.600	83.7%

12.070	0.123	1.779	0.701	84.0%
12.060	0.140	1.779	0.801	84.1%
12.051	0.156	1.778	0.889	83.9%
12.050	0.158	1.778	0.900	83.9%

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