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TI High Speed Designs: Verified Design
Clocking Solution for GSPS ADCs

TEXAS INSTRUMENTS

TI High Speed Designs

TI High Speed Designs are analog solutions created by TI's analog experts. Verified Designs offer the theory, component selection, simulation, complete PCB schematic & layout, bill of materials, and measured performance of useful circuits. Circuit modifications that help to meet alternate design goals are also discussed.

Circuit Description

The ADC12J4000EVM from Texas Instruments offers an example of a clocking solution for a Giga-sampling ADC. The ADC on this EVM can operate at a maximum sample rate of 4GHz, which is not easily generated by an IC with the required phase noise to show the true performance of this Giga sampling ADC.

This type of circuit may be used in wireless infrastructure, RF-sampling Software Defined Radio, Radar and LIDAR, Military Communications, and Test Equipment applications. The synthesizer circuit implemented on this EVM has programmable output dividers that can enable continuous frequency coverage from 300 MHz to 4.8 GHz.

Design Resources

ADC12J4000EVM	Product Folder
TRF3765EVM	Product Folder
ADC12Jxx00 Design Package	EVM Design Package
TRF3765 Design Package	EVM Design Package

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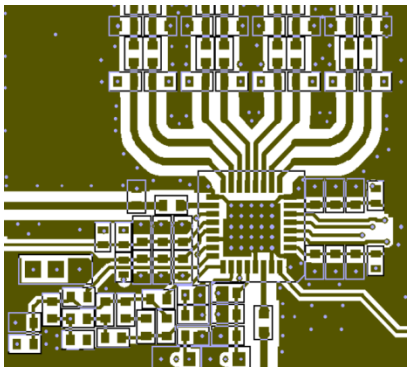

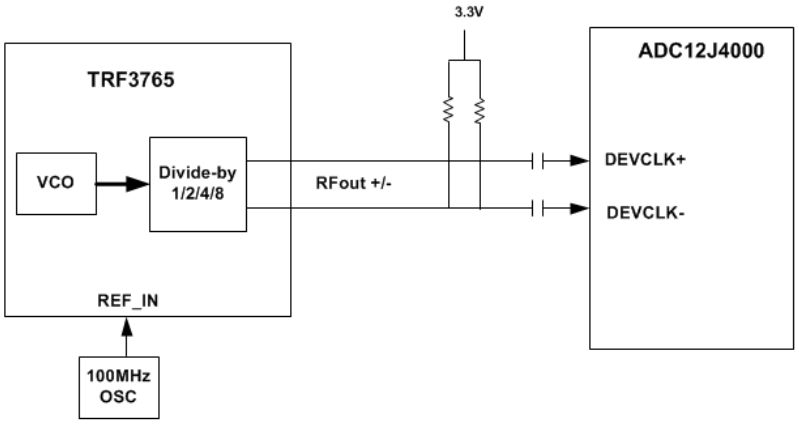

1 Introduction

High speed data converters are sampling faster than ever before. One problem that arises from this is finding a suitable clock source that meets not only the sampling speed of these devices but offers very low jitter (phase noise) which will maximize the performance of the converter.

The ADC12J4000EVM is an evaluation module that allows for the evaluation of Texas Instruments' ADC12J4000. The ADC12J4000 is a low power, 12-bit, 4-GSPS RF-sampling analog to digital converter (ADC) with a buffered analog input, integrated Digital Down Converter with programmable NCO and Decimation settings (including un-decimated 12 bit ADC output) and features a JESD204B interface. A TRF3765 clock synthesizer is included on the EVM and can be configured to provide an ultra-low-jitter ADC clocking solution.

The TRF3765 is a wideband Integer-N/Fractional-N frequency synthesizer with an integrated, wideband voltage-controlled oscillator (VCO). Programmable output dividers enable continuous frequency coverage from 300 MHz to 4.8 GHz.

2 TRF3765 Features

The TRF3765 has four separate differential, open-collector RF outputs to allow multiple devices to be driven in parallel without the need of external splitters. In the case of the ADC12J4000 EVM, one output is used to drive the differential sampling clock inputs of the ADC.

Key features of the TRF3765 include:

- Output Frequencies: 300 MHz to 4.8 GHz
- Low-Noise VCO: –133 dBc/Hz
  (1-MHz Offset, f_{OUT} = 2.65 GHz)
- 13-/16-Bit Reference/Feedback Divider
- 25-Bit Fractional-N and Integer-N PLL
- Low RMS Jitter: 0.35 ps
- Input Reference Frequency Range:
  0.5 MHz to 350 MHz
- Programmable Output Divide-by-1/-2/-4/-8
- Four Differential LO Outputs
- External VCO Input with Programmable VCO On/Off Control

3 TRF3765 interface to the ADC12J4000

The TRF3765 clock output interface to the ADC12J4000 is shown in Figure 1.

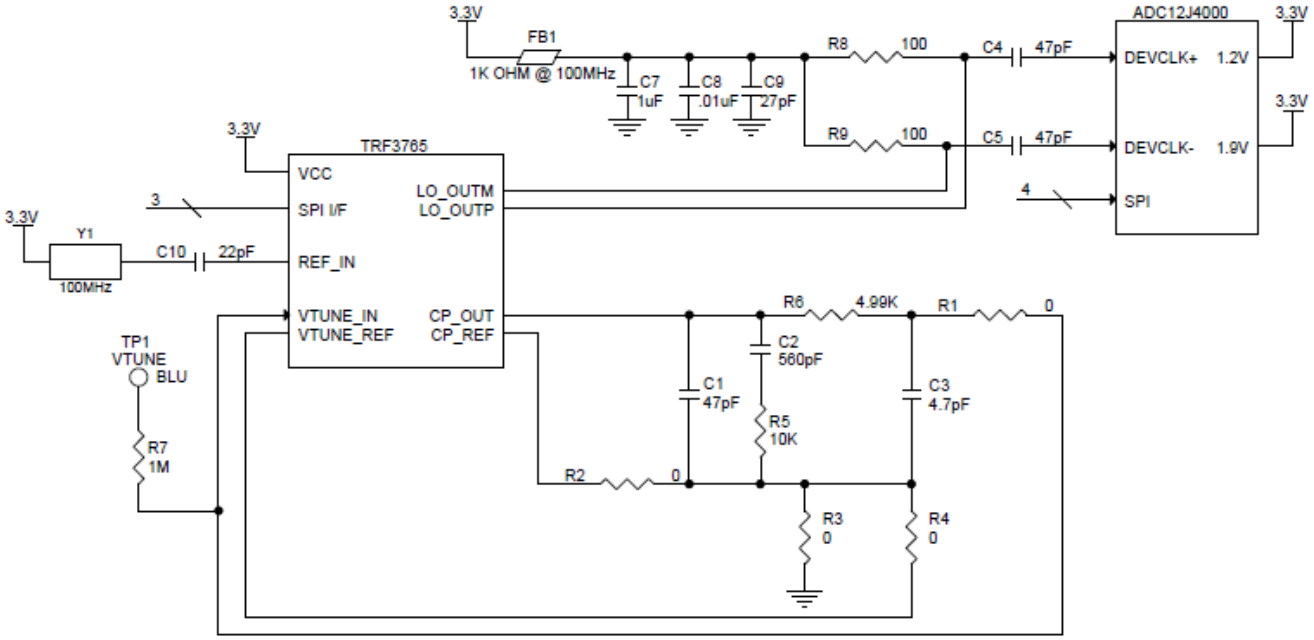

Figure 1. TRF3765 interface circuit to ADC12J4000

The TRF3765 output buffers are open collector so external biasing is required. This is accomplished using pullup resistors to 3.3 volts. Capacitors and a ferrite bead are used to isolate the high speed clock lines from the 3.3 Volt power. The bypass caps and ferrite bead are chosen at a suitable value to provide isolation at the frequency of interest.

The 100 Ohm resistors are used to set the impedance to the device. In this reference design, the traces between the TRF3765 and the ADC are routed as100 Ohm differential impedance. The resistors and associated circuitry should be placed as close as possible to the TRF3765. More information regarding output termination can be found on the TI application note called “TRF3765 Output Terminations (SLWA070)”.

Layout of the application board significantly impacts the analog performance of the TRF3765 device. Noise and high-speed signals should be prevented from leaking onto power-supply pins or analog signals. Follow these recommendations:

1. Place supply decoupling capacitors physically close to the device, on the same side of the board. Each supply pin should be isolated with a ferrite bead.
2. Maintain a continuous ground plane in the vicinity of the device and as return paths for all high-speed signal lines. Place reference plane vias or decoupling capacitors near any signal line reference transition.
3. The pad on the bottom of the device must be electrically grounded. Connect GND pins directly to the pad on the surface layer. Connect the GND pins and pad directly to surface ground where possible.
4. Power planes should not overlap each other or high-speed signal lines.
5. Isolate REF_IN routing from loop filter lines, control lines, and other high-speed lines.

The ADC input sampling clock must always be AC-coupled, so the only consideration here is the value of capacitor. The sampling clock is terminated by 100-Ω differential impedance, so the choice of capacitor determines the highpass cutoff frequency:

$fc = 1 / (2 \times \pi \times R \times CFCLK)$

where:

- R = 50 Ω
- CFCLK = the capacitor value chosen

The example from the ADC12J4000EVM uses 4.7-nF caps, which results in a highpass fc = 677 kHz. Chose another value as long as it does not interfere with the sample clock frequency.

On the ADC12J4000EVM, theTRF3765 uses an external 100MHz oscillator as the input reference source. More information regarding the use of the reference input can be found in the TI application note called “TRF3765 REF_IN Impedance Application note (SLWA067)”.

In cases where a single-ended clock is required, converting the signal to differential is necessary. TI recommends the Anaren B0430J50100AHF which covers 400 MHz to3000 MHz. When using a balun, the AC-coupling caps and balun should be placed as close as possible to the ADC.
Similar to the analog inputs, these clock signals are sensitive, high-speed signal and special care must be taken in order to avoid coupling the analog inputs or power planes into the sampling clock. One method of isolating the clock from the analog input is to place the clock driver as far away as possible from the analog input traces. On the ADC12J4000EVM, this is accomplished by placing the TRF3765 on the top side of the PCB and the ADC and the analog input traces on the bottom side.

4 TRF3765 Power

A clean power supply is critical to optimal phase noise performance of the synthesizer. The impact of the power supply is discussed in detail in the application report *Supply Noise Effect on Oscillator Phase Noise* (SLWA066). Linear power supplies(LDO’s) are the best sources available. Switching power supplies degrade inband phase noise by 10 dB compared to linear laboratory supplies. LDO regulators, such as the TI ultra-clean TPS74201, which are used on the TRF3765EVM, provide excellent performance.

5 Loop Filter Component Selection

The TRF3765 requires an external loop filter for proper operation. The loop filter design is critical for achieving low closed-loop phase noise. For this design the synthesizer is operating in Fractional-N mode with a PFD (phase frequency detector) frequency of TBD. The charge pump current is set to 1.95 mA to minimize noise. The loop filter component values are given in Table 1, referenced to designators in Figure 1.

Fpfd (MHz)	C1	C2	R5	C3	R6
1.6	47 pF	560 pF	10K	4.7 pF	4.99K

Table 1. TRF3765 loop filter components

If there is a need to modify the PFD frequency or operational mode, then the loop filter may need to be modified. The Loop_Filter-CALC program available on the TI web can assist in determining the proper loop filter component values.

6 TRF3765 Performance at 4GHz

SPI communication is required for configuring the TRF3765 device. TI provides a Graphical User Interface (GUI) software program that allows the user to configure the TRF3765. To program the TRF3765 to generate a 4GHz output for the LO1 outputs, load the device registers shown below with the following settings:

0x9 0x3C1800A
0xB 0x0000000
0xC 0x0400300
0xD 0x0EC74B4
0xE 0x2A38880
0xA 0x44500C8

With the TRF3765 configured with the register settings above and using external loop filter values per Table 1, the device provides a very low jitter output. Figure 2 is a phase noise plot from a TRF3765EVM with the register settings above and the loop filter configured per Table 1.

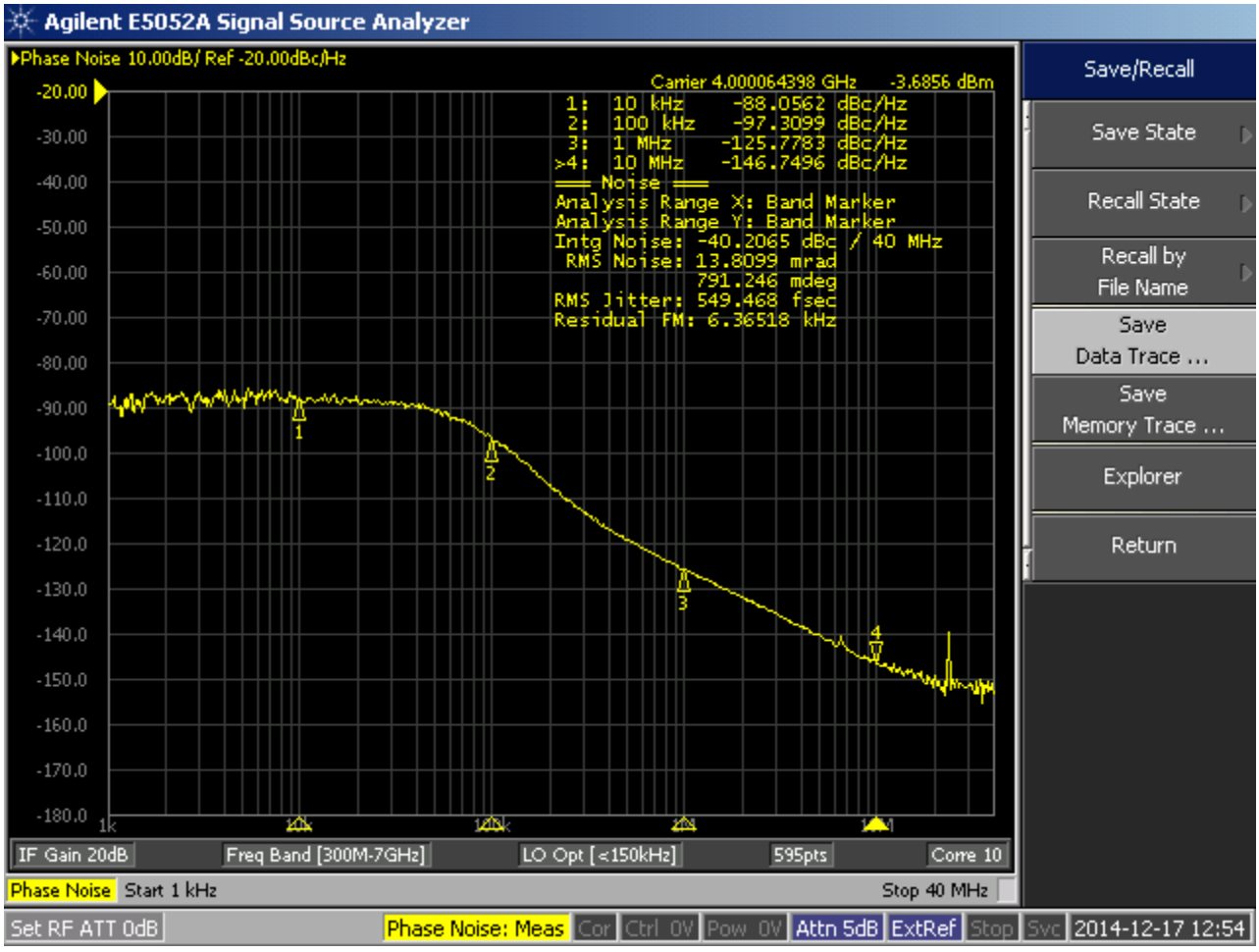

Figure 1. TRF3765 Output Phase Noise Plot

7 Results on TRF3765 clocking the ADC12J4000

The implementation of the TRF3765 clocking the ADC12J4000 at 4 GSPS shows nearly datasheet performance.. In a simple test where a clean, filtered 350 MHz IF signal is fed into the ADC, the SNR showed ~54.7 dBFs, which is only a slight degradation from the 55 dBFs of the ADC12J4000 data sheet value using an ultra low noise signal generator for the clock. The SFDR is at 67.42 dBFs which matches the typical data sheet value of 67.4 dBFs.

In summary a very clean clock interface can be implemented using the TRF3765 to drive the device clock of a GSPS ADC.

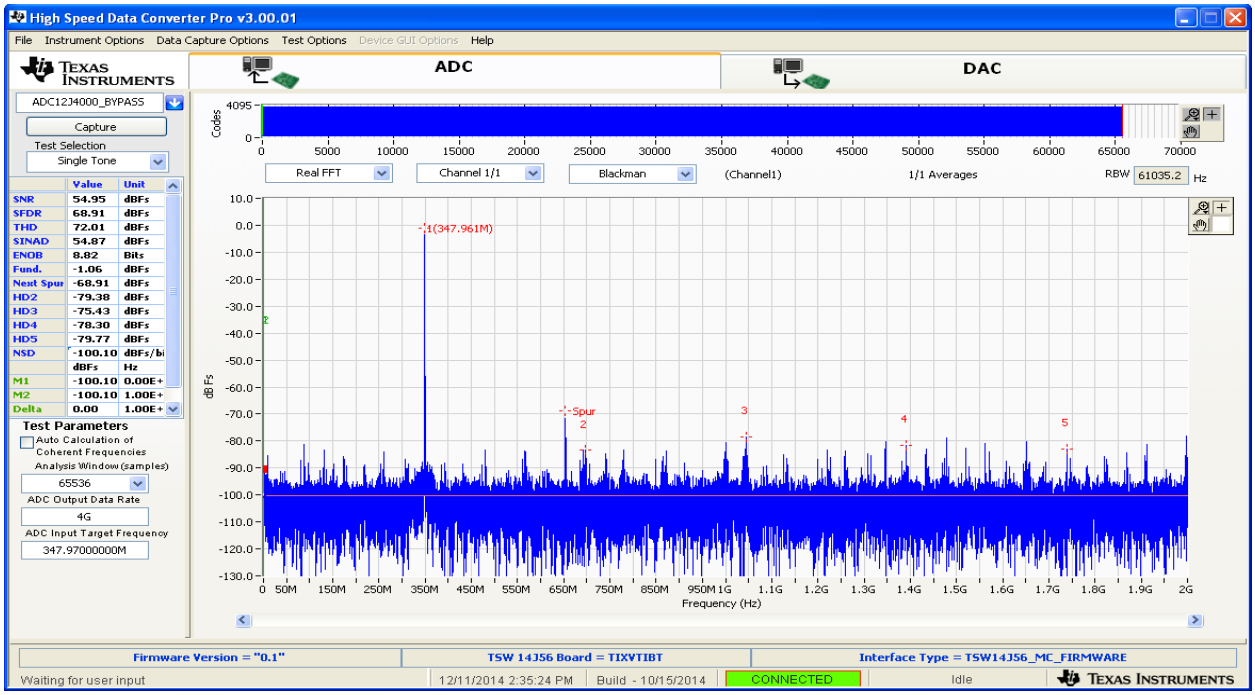

Figure 2. FFT performance of the ADC12J4000 with TRF3765 clock interface

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