TI Designs
Generic Energy Harvesting Adapter Module for TEG

TEXAS INSTRUMENTS

TI Designs

TI Designs provide the foundation that you need including methodology, testing and design files to quickly evaluate and customize the system. TI Designs help *you* accelerate your time to market.

Design Resources

|	
TIDA-00246	Design Folder
BQ25570	Product Folder
TPL5100	Product Folder
TLV3691	Product Folder
CSD13202Q2	Product Folder
CSD17483F4T	Product Folder

TI E2E™ Community

ASK Our E2E Experts
WEBENCH® Calculator Tools

Design Features

- II-VI Marlow EverGen® Power Strap Thermal Harvester Source
- Withstands Negative Temperature Gradients
- Optimized for Low-Temperature Gradients (Ultra-Low-Power)
- 60-nA Full System Consumption (Power + MCU + Logic) in Lowest Power Mode of State Machine
- BoosterPack™ for MSP430FR5969 LaunchPad™

Featured Applications

- Oil and Gas Process Control (Flow, Pressure, Temp Transmitters)
- Factory Automation
- Building Automation
- Sensors and Field Transmitters
- Portable Instrumentation
- Autonomous Wireless HART (WHART) Nodes
- GEHAM (VDE2185)
- ISA100.18
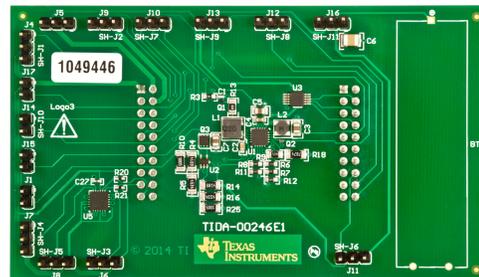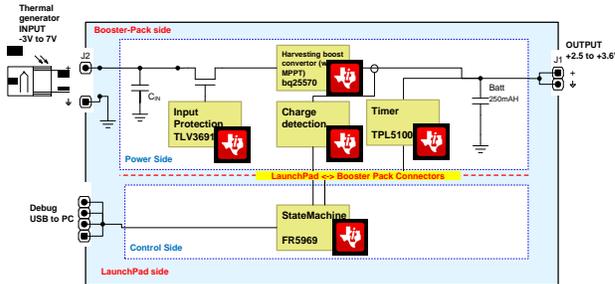
An IMPORTANT NOTICE at the end of this TI reference design addresses authorized use, intellectual property matters and other important disclaimers and information.

All trademarks are the property of their respective owners.

Copyright © 2015, Texas Instruments Incorporated

1 System Overview

The system described in this TI Design aims at solving the following challenges:

Table 1. TIDA-00246 Solutions

INDUSTRY CHALLENGE	TIDA-00246 SOLUTION
Diversity of harvesters types and performances	GEHAM electronic reference design
Energy harvesting designs requires full system power optimizations	Full system (power, MCU with state machine, signal chain) optimized to achieve power consumption as low as 130 nA
Thermoelectricity projects require multi-physics domain collaboration	Reference design including thermal, mechanics and electronics aspects

1.1 Key System Parameters

Table 2. Key System Parameters

PARAMETER	SPECIFICATION	VALUE	DETAILS
II-VI Marlow EverGen PowerStrap spec	80°C pipe, 20°C ambient — matched load power is 350 mW	30 mW	Section 3.1
II-VI Marlow EverGen PowerStrap spec	120°C pipe, 20°C ambient — matched load power is 870 mW	90 mW	Section 3.1
ΔT_{min_OP}	Min temp delta between cold and hot side for positive energy generation	4 K (TBC)	Section 3.1
$\Delta T_{min\_Protection}$	Max negative temperature gradient where system is protected	100 k	Section 3.4
ΔT_{max}	Max temperature gradient where energy is harvested	130 k	Section 3.4
P_{OUT}	Average P generated	$> P_{WHART\_node}$	Section 2.4 Section 5.2
Autonomy	WHART capabilities from fully charged batter, without any harvesting	8 days	Section 2.4 Section 3.6
I_{DEEP_SLEEP}	Battery current drain when Vbat < UVLO (including wake-up every 17 mn for sensing if input power is restored)	60 nA	Section 3.2

2   Theory of Operation

While thermal energy harvesting has been known for decades, applications beyond space exploration have started deployments only in the last decade. One area where this technology is of most practical application is the oil and gas industry, especially in the case of heavy crude oils (API gravity < 10), where steam can be injected to reduce viscosity and facilitate flows. As the steam is injected, it increases significantly the gradient temperature, making energy harvesting possible.

This section will provide the following generic background information to facilitate the understanding of this TI Design:

*   Thermoelectricity
*   Energy harvesting
*   Ultra-low-power design guidelines
*   Recent industry standards released to facilitate adoption of energy harvesting

2.1   Thermoelectricity

2.1.1   History

Thermal energy harvesting is based on the physical phenomenon known as the Seebeck effect. The Seebeck effect, which was discovered in 1821 by T.J. Seebeck, is the physical effect by which some materials under the effect of heat flux will generate free electrons (n-type) or absorb free electrons (p-type). When n-types and p-types are connected, an electrical current is generated that is proportional to the temperature difference between the hot side and the cold side.

> **NOTE:**   A pair of n-type and p-type makes a thermo-generator element. Thermo-generators can be associated in series (to increase voltage) or parallel (to increase current).

Seebeck elements have been characterized as a function of their figure of merit: zT. zT is a dimensionless measure of the efficiency of the material to convert heat flux to electricity and is defined in relation to the efficiency of the thermogenerator: While there is no theoretical limit to zT, no known material of zT > 3 are known and known with zT > 2 are in production.

While research for different materials with higher zT has been active since the discovery of thermoelectricity, the most recent focus has been on improving the industrial process of connecting single elements in different ways to improve the voltages and current capabilities of those thermogenerators. As of today, three generations of thermogenerators are being discussed:

*   Bulk (first generation): Multiple elements of typical sizes are approximately 1 mm and already in production for decades based on material with zT ~ 0.9 (Bi_2Te_3). The assembly is automated.
*   Thin-films (second generation): Elements are assembled using a semiconductor-related process, allowing a much smaller size of elements (~10 s of µm). The materials are similar to first generation. The first pre-series production started after 2010. Thin films usually put more elements in series and hence generate higher output voltages but with a higher series resistance.
*   Nanostructures (third generation): At the time of writing in 2014, this is still in the research phase but focuses on bringing zT towards 3. This level of performances being enabled by a combination of new materials and new structures (quantum dots, nanowires, lattices, and so on). This technology can be considered as having a TRL between 5 and 7.

> **NOTE:**   For practical projects, the choice of the first two generations and the design decision is guided by a compromise between cost and desired output voltage.

2.1.2 Physics

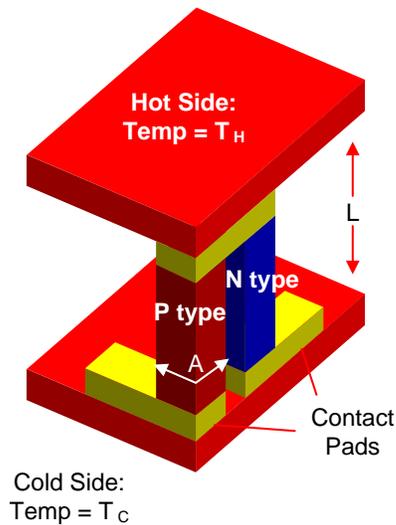Consider a thermogenerator with M pairs of P-N elements in series as described by Figure 1 and Figure 2:
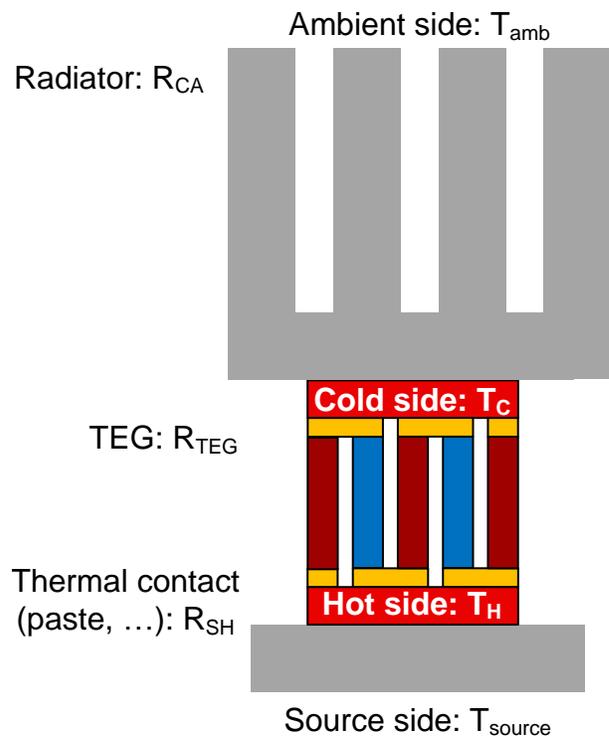

Figure 1. View of the TEG

Figure 2. View of the TEG in System With the Different Thermal Resistances Highlighted

Each p-type and n-type material has a Seebeck coefficient (α_p and α_n, respectively,) and thermal coefficient (k_p and k_n) and resistivity ($Þ_p$ and $Þ_n$), and each element has a length L and cross section area A ($\lambda = L / A$).

Define the average Seebeck coefficient:

$$\bar{\alpha} = \alpha_p - \alpha_n$$

(1)

The electrical resistance of the thermoelectric generator (TEG) R_{el-TEG} made of an assembly of M pairs of material, with contact pads is

$$R_{el-TEG} = M \times \left[(\rho_p + \rho_n) \times \frac{L}{A} + R_C \right] = M \times \left[\lambda \times (\rho_p + \rho_n) + R_C \right]$$

where

- R_c is the resistance of the contact pads

(2)

In the following equations, this parameter will be neglected.

The open circuit output voltage is:

$$Voc = M \times \bar{\alpha} \times \Delta T$$

where

- Voc is the open circuit (in absence of load) voltage
- ΔT is the temperature difference between the hot side and the cold side of the TEG

(3)

NOTE: The unloaded TEG output voltage varies linearly with the temperature difference.

The current flowing through a load R_{load} is

$$I = \frac{\overline{\alpha}}{R} \times \frac{\Delta T}{1 + \frac{1}{u}}$$

where

- R is the electrical resistance of a single pair of n-type and p-type

- u is the ratio between the TEG internal impedance and the load: $u = \frac{R_{load}}{R_{TEG}}$ (4)

This theoretical analysis does not consider the case where TEGs are set in parallel to increase the output current. In that case, the previous equations need to be scaled by P, the number of parallel TEG.

While ΔT is TH-TC, TH and TC are not necessarily the temperature of the physical elements to which the TEG is attached as the thermal resistance of the TEG needs to be taken into account.

> **NOTE:** More specifically, in most cases a heat sink needs to ensure the temperature gradient across the actual Seebeck material stays as high as possible.

While it would go beyond the scope of this introduction, those equations (except Equation 4) are valid only under open circuit conditions. As soon as the current is allowed to flow from the TEG, the heat flow through the TEG increases. For more details, refer to *Energy harvesting for wireless sensors, Synergistic analysis of thermoelectric devices, heat sinks and associated electronics for optimized energy harvesting systems* [2].

2.1.3 Theoretical Maximum TEG Efficiency

> **NOTE:** A frequent topic of discussion is whether the efficiency of a TEG is "sufficient". This topic has specifically not discussed as the only design criteria for this design is whether the TEG produces enough energy for the system to be operated and whether this is done at an economical point.

The maximum efficiency is a function of the Carnot efficiency (thermodynamic limit):

$$\eta_{max} = \frac{\Delta T}{T_H} \times \frac{\sqrt{1 + zT} - 1}{\sqrt{1 + zT} + \frac{T_C}{T_H}}$$

$$zT = \text{Thermoelectric figure of merit (dimensionless)} = \frac{\alpha^2 T}{\rho \kappa}$$

$$\frac{\Delta T}{T_H} = \text{Carnot efficiency (maximum possible theoretically)}$$

(5)

The simplifications to obtain this equation, which are also its limit of validity, are relatively small delta of temperature. Under industrial operating conditions, this will always be the case.

2.1.4 Maximizing System Efficiency

If a TEG is shorted, it will generate the maximum amount of current, but as no voltage will be on its output, no power is available. Reciprocally, if the TEG is left open, the highest possible voltage will be available, but as no current flows, no power is available.

The electrically available output power P_{ELEC} can be written as:

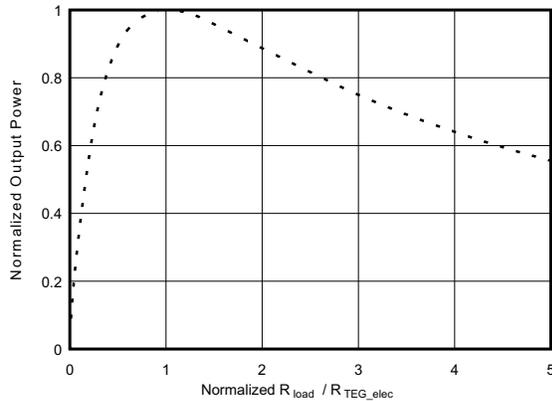$$P_{ELEC} = \frac{V_{OC}^2}{R_{TEG}} \times \frac{u}{(1+u)^2}$$

(6)

Figure 3. Normalized P$_{OUT}$ Versus P$_{OUT\_MAX}$
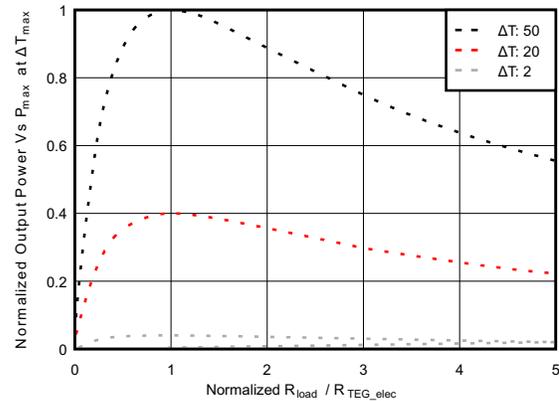
Figure 4. Normalized P$_{OUT}$ Versus P$_{OUT\_MAX}$ at ΔT$_{MAX}$

Solving it numerically yields a maximum for u = 1, which can be expected when matching the internal resistance with the load.

> **NOTE:** To extract the maximum amount of energy, the load should be kept at the same value as the TEG internal impedance (which can be difficult for reusing across multiple projects) or the TEG output voltage should be kept at 50% of its open circuit voltage. Keeping V_{TEG} at 50% of V_{TEG-OC} is much more easily achieved.

> **NOTE:** The system achieves maximum efficiency when thermal impedances are matched. Refer to *Energy harvesting for wireless sensors, Synergistic analysis of thermoelectric devices, heat sinks and associated electronics for optimized energy harvesting systems* for more details [2].

2.1.5 Negative Voltage Generation

Following Equation 3, if there is a negative temperature gradient (for example, if the side defined as "cold side" becomes hotter than the side named "hot side") the TEG element will generated a negative voltage.

> **NOTE:** In applications where negative temperature gradients can occur, few integrated circuits for power management can withstand negative input voltages.

As such a case is industry dependent, protection against negative voltages is dependent on the target end-application as the protection in itself would draw current and could reduce the overall efficiency of the system without gains if this use case never occurs (controlled process environment with known temperature side on the process side and controlled room temperature).

However, given the focus of this design for the oil and gas industry and because the steam used to reduce the viscosity of some heavy oils can under some extreme cases be released at or near the radiator of the harvester, a negative temperature gradient could be generated. Therefore, a protection circuitry will be part of the design.

2.2 Impedance Matching (MPPT)

Impedance matching is also referred to in the literature as MPPT. Both aim at extracting the maximum amount of energy from the source which has a varying impedance dependent on physical parameter changes (ambient temperature change, delta temperature change, and so on).

The difference, which is often made explicit, is that impedance matching is more a static process while MPPT is often used for a fast response loop (mostly for PV inverters).

The proper selection of an MPPT strategy must be correlated tightly to the speed of variations of the impedance of the TEG and with the cost (in silicon as well as in power) associated with higher speed of reactions to changes from the MPPT algorithms. A detailed study, which goes beyond the scope of this paper, can be found in *Energy comparison of MPPT techniques for PV Systems*.

The most effective method for µW and mW power levels is dynamic tracking of fractional voltage method.

2.3 Efficiency Optimization

A key aspect of energy harvesting systems is that by nature the power source is a stochastic process. While the average value can be well characterized and so its distribution over time, the instant value cannot be predicted.

Resultantly, the following are the key parameters that should be determined by design:

- The average harvesting power *must* match or exceed the average system power
- System autonomy *must* be designed to address the time when the harvested energy is less than the used one (either low input energy or no input energy)

NOTE: Take special attention to the corner case where no energy is available at the input to ensure that the energy used by the power management is minimized until the input power source is available again.

Assuming the TEG impedance is matched, a more visual way to see this is to write:

$$P_{system} = P_{TEG} - \left(P_{dyn} + P_{stat}\right) = \eta \times \alpha \times \frac{\Delta T}{4} \times R_{TEG} - \left(C \times V^2 \times f \times V \times I_{leak}\right)$$

where

- P_{system} is the total power of the system (including power devices, microcontroller, logics, and so on)
- η is the efficiency of the power conversion and for first order approximation we can lump the leakage current of the power conversion with the leakage current of the digital logic
- $CV2$ is the dynamic power, which scales squarely with the supply voltage
- $V \times I_{leak}$ is the static power dissipation, which shows that the static power is proportional to the supply voltage   (7)

Therefore, optimizing the system power leads to:

1. Reducing the supply voltage to the minimum needed to get the processing performances
2. Removing the leakage current of unneeded peripherals (load switch either integrated or discrete)

While scaling dynamically the voltage to the computing performances might be still unrealistic for low-power systems, an often overlooked and easily achieved optimization is to add a power regulation between the storage element and the microcontroller to reduce the power dissipation. The application note *Using power solutions to extend battery life in MSP430 applications* details the reasons for which an extra power stage will decrease the overall power consumption, which can be summarized with Equation 8:

$$V_{supply} \times I_{MCU} > V_{supply} \times I_{q\_LDO} + \left(V_{supply} - V_{out\_LDO}\right) \times I_{MCU} + V_{out\_LDO} \times I_{MCU}$$ (8)

Given the range of power consumption from systems in a few hundreds of µA for active MCU, and recent introduction of DC-DC the above can be further optimized with usage of DC-DC with ultra-low leakage current, which becomes

$$V_{supply} \times I_{MCU} > V_{supply} \times I_{q\_DCDC} + V_{out\_DCDC} \times I_{MCU}$$ (9)

2.4 WHART Power Needs

There are multiple ways to determine WHART network power consumption needs. One could look at the physical network setup, the frequency of update, or the depth of the network (between the deepest sensor and the gateway), which was done extensively in *A Simulation Model for the Performance Evaluation of WirelessHART TDMA Protocol* [17]; however, it still remains difficult to model actual network conditions.

Alternatively, look at existing products guaranteed lifetime and the battery they embed. Looking at existing products on the market [9] [10] [11], they have a 19-Ah battery for an average of operation time of five years. A simple calculation gives that an average WHART node consumes: P_{WHART_node} ~ 3 mW

This average power consumption is also the target for the ISA100.18 working group [1].

2.5 GEHAM – VDE2185

Wir verbinden Kompetenz is the standard from the German industry specifying "requirements and specifications for power supply solutions based on batteries and energy harvesting" for industrial systems [16].

The standard specifies requirements for battery (primary or rechargeable) powered radio-communicating systems but also for a "Generic Energy Harvesting Adapter Module" (GEHAM).

The standard specifies that the GEHAM should be mechanically compatible with existing batteries as well as electrically compatible (3.6 or 7.2 V).

The GEHAM is a system made of harvesters, batteries, electronics, and mechanics that abstract the variability of harvester to provide a common interface to the electronics (similar to classical batteries).
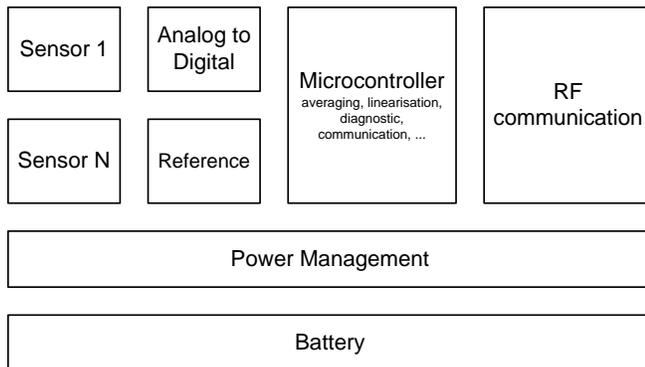
| Figure 5. Traditional Wireless Sensor Transmitter Used in the Industry | Figure 6. Sensor Transmitter With GEHAM as Defined by VDE2185 |
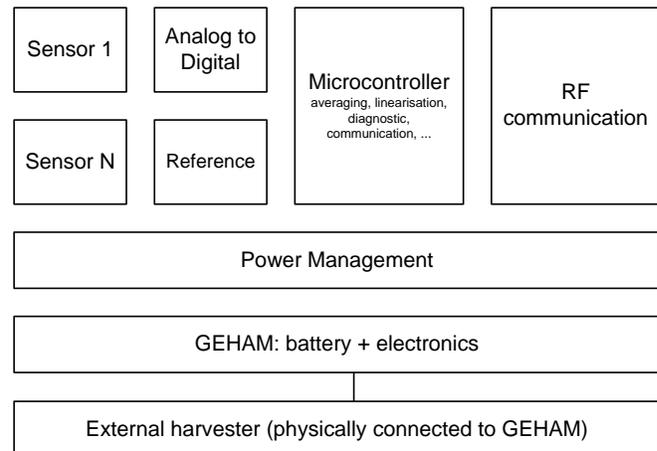
2.6 Symbol for TEG

While TEG has been around for long time, they have rarely made it to schematics, so few tools and electronic engineers are aware of the TEG symbol defined by EN60617:
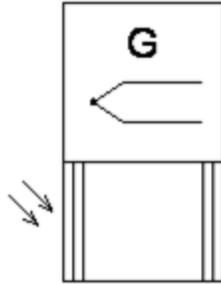

Figure 7. TEG Symbol

To connect this symbol to the electronics, the author modified the symbol to expose connections, the resulting symbol is:
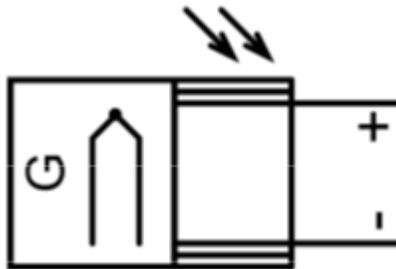

Figure 8. TEG Symbol With Connections

3 Design

3.1 Harvester Selection

Given the multiple aspects listed in Section 2, the TEG harvester for a GEHAM reference design for oil and gas industry needed to have the following specification:

- Required:
  - First generation (bulk type) for reliability (with historical data) and broad availability
  - Strong mechanical and thermal design to help the design to focus on electronics
- Recommended:
  - Existing field testing results giving average and standard deviation temperature gradients

Given this criteria, only one harvester was found, the II-IV Marlow EverGen PowerStrap, with the following characteristics:

- Renewable power source addresses costs, maintenance, and disposal associated with battery replacement of wireless sensors
- Five-minute installation
  - Single bolt tightening
- Electrical storage as safe (or safer) as most existing batteries
  - Actually classified as safer for transportation — not subject to DGR shipping requirements
  - Long operating lifetime, long shelf life, extremely high cycling capability
- Operational in all geographic locations (pervasive)
- Harvester storage capable of operating transmission for more than two weeks with zero ΔT at eight-second update rate. Storage capacity may be scaled up for longer holdup
- Low and high voltage protection circuitry
- Regulated voltage output to protect the sensor and transmitter
- Configurable for vertical and horizontal pipes of all standard pipe diameters
- High volume manufacturing by II-VI Marlow in Vietnam
  - Designed for economical manufacturing
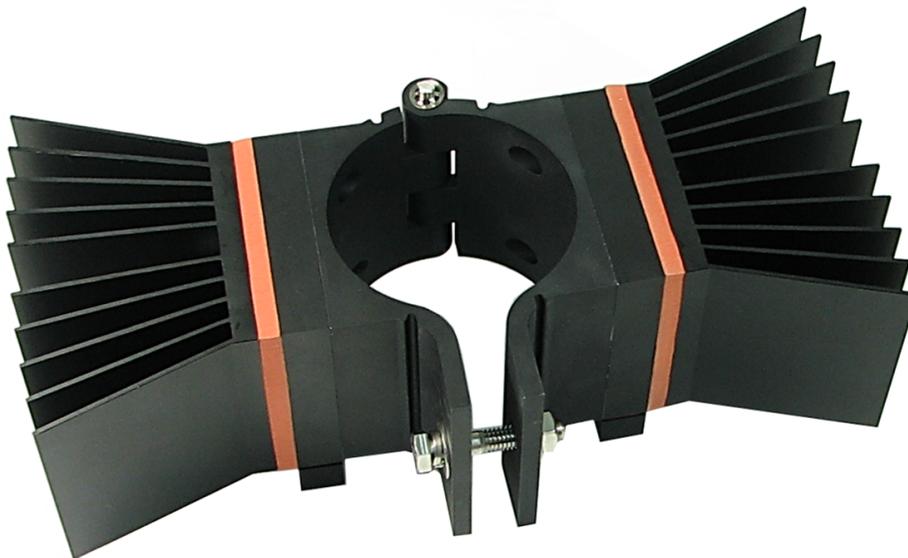
Figure 9. II-VI Marlow EverGen PowerStrap

3.2 Integrated Circuits Selection

For the power management, the bq25570 was selected as it addresses the following needs, which were highlighted in Section 2:

Table 3. Selection Criteria for Power Management IC

CRITERIA	bq25570 VALUES
High-efficiency at input power between 100 nW and > 100 mW	Up to 90% Higher than 70% from 60-µW input power
MPPT (while achieving the above target)	YES
Low input voltage (compatible with TEG voltages)	Input voltage as low as 100 mV
Buck conversion to address the need for limiting the operating voltage to the minimum needed	YES
Low quiescent current when not active	5 nA in ship mode at 25°C < 30 nA over full temperature range

Addressing the need for ultra-low leakage current in standby mode, the two industry leading devices were selected:

Table 4. Selection Criteria for Digital

CRITERIA	VALUES
MSP430FR5969 in LPM4.5 (can be woken-up from asynchronous interrupts)	80 nA at 85°C (20 nA at 60°C)
TPL5100	30 nA

The decision to go to the lowest power mode Deep_Sleep is taken when there is no more input power (no temperature gradient) and when the battery is too low.

Because the input voltage can go negative, a load switch is built to protect the input of the power management. To minimize the power taken by this load with the following goals are set:

- Built with discrete to minimize power consumption
- Designed to be a "normally open" switch (selection of NFET low RDS(on) and low threshold voltage (VGS(th)): selected CSD13202Q2 which has VGS(th) of 0.8 V and RDS(on) of 9.1 mΩ (at VGS of 2.5 V)
- Power can be removed when not needed (to optimize power consumption)
- Uses best in class comparators for power consumption: TLV3691 (I_q: 75 nA)

To be able to take the decision to switch the different power rails on or off based on the input power, two options are possible:

1. Monitor the input voltage
2. Monitor the charge of the battery

Given the fact that the input voltage could be negative and that offsetting the voltage would burn power, the monitoring of the battery charging was decided. For this, a low gate charge transistor was selected and used in a "pulse stretching" topology to enable the detection of the pulse by the MSP430.

3.3 Design Overview

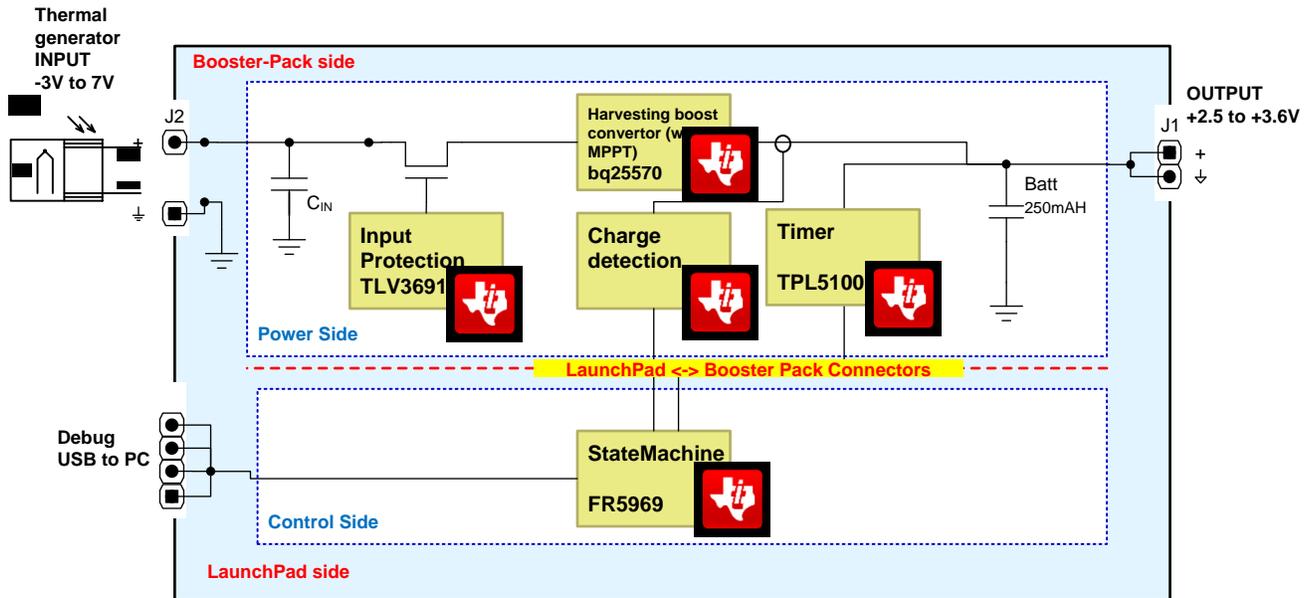Figure 10 through Figure 12 describe the design:

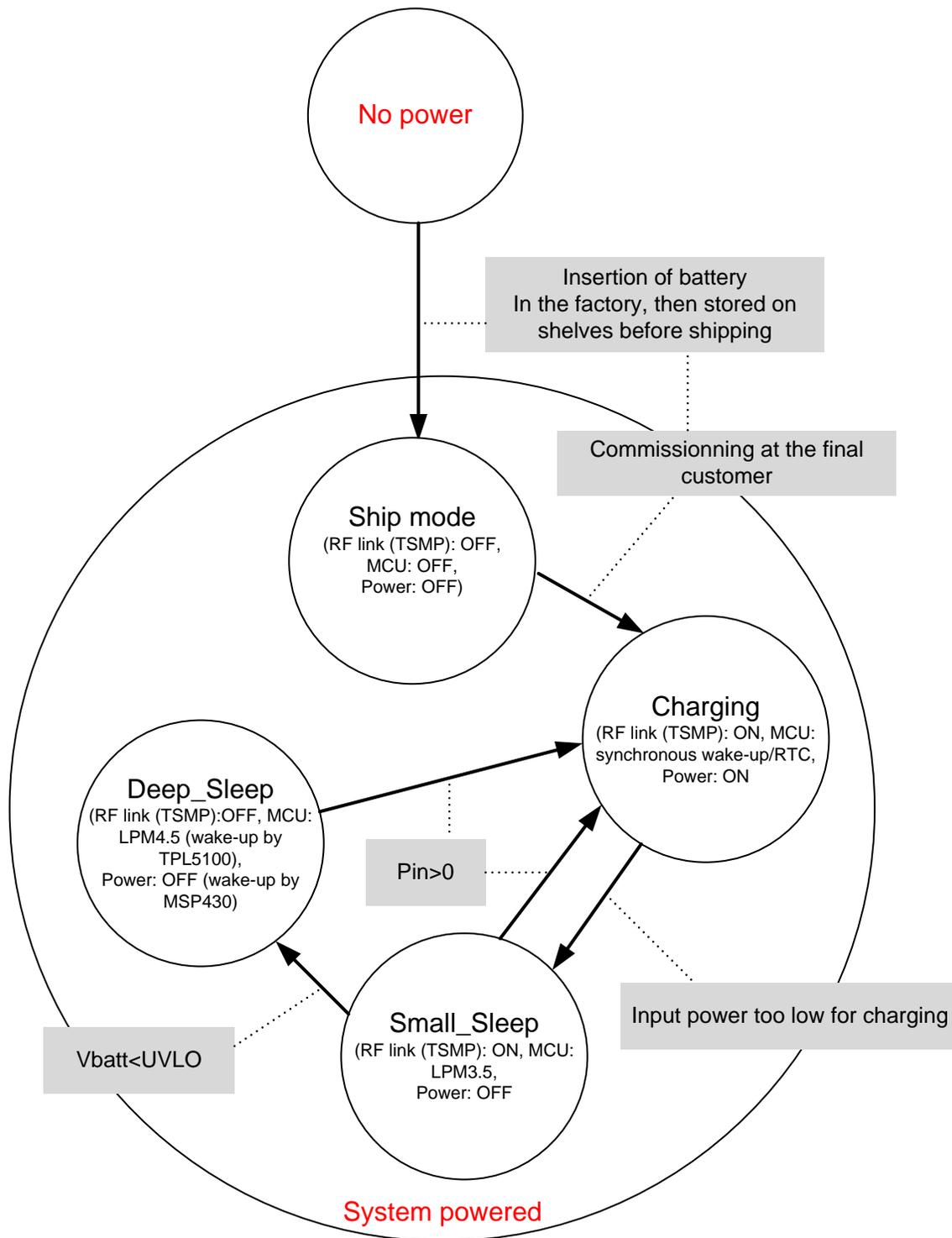**Figure 10. Overview of GEHAM for II-VI Marlow TEG Reference Circuit**

Copyright © 2015, Texas Instruments Incorporated

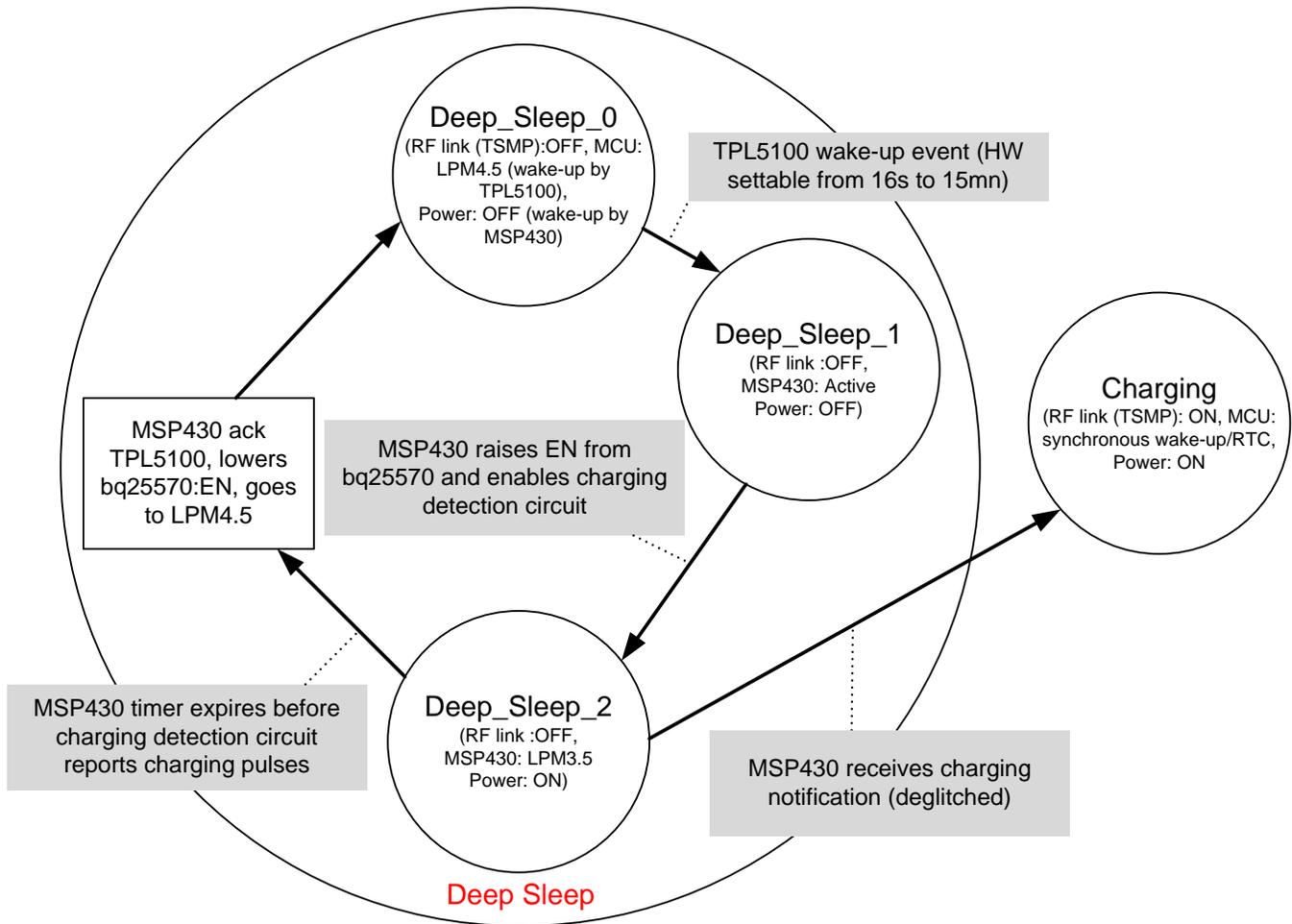**Figure 11. Overview of Different States from TIDA-00246**

Figure 12. Details of the Deep_Sleep State of TIDA-00246

The system is considered to have three main states:

- Active
  - In this state, the bq25570 charges the battery and the full system makes regular measurement and reporting values over WHART as its configuration demands.
- Small_Sleep (shorter name for Active and Not_Charging)
  - In this state, the system is also making measures and radio communication but the battery is not charging. Because the battery is not charging, the bq25570 is disabled to allow reducing even further the drain from the battery (from the range of 445 to 900 nA down to 1 to 30 nA)

Table 5. bq25570 Quiescent Current in Different Modes

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_Q	$\overline{EN}$ = 0, VOUT_EN = 1 - Full operating mode	VIN_DC = 0 V; VSTOR = 2.1 V; T_J = 25°C		488	700	nA
		VIN_DC = 0 V; VSTOR = 2.1 V; −40°C < T_J < 85°C			900	
	$\overline{EN}$ = 0, VOUT_EN = 0 - Partial standby mode	VIN_DC = 0 V; VSTOR = 2.1 V; T_J = 25°C		445	615	
		VIN_DC = 0 V; VSTOR = 2.1 V; −40°C < T_J < 85°C			615	
	$\overline{EN}$ = 1, VOUT_EN = × - Ship mode	VBAT = 2.1 V; T_J = 25°C; VSTOR = VIN_DC = 0 V		1	5	
		VBAT = 2.1 V; −40°C < T_J < 85°C; VSTOR = VIN_DC = 0 V			30	

- Deep_Sleep
  - In this state, the battery is below the UVLO and the system is not measuring nor communicating through radio. It has entered the state of lowest power consumption with MSP430FR5969 in LPM4.5, and the MSP430 is woken-up by the TPL5100 every 1024 seconds (which is 17 minutes).
  - Also in this state, all components other than MSP430FR5969 and TPL5100 are disabled leading to a battery current drain of 130 nA where the MSP430FR5969 will monitor conditions at the input of the bq25570 (enabling briefly the bq25570, the AFE circuitry and the sensing). If the battery is charging, it will let the system try to recover. If the battery is not charging, it will set the entire system back to sleep and wait for another 17 minutes to do the same procedure.
    - 80 nA (MSP430FR5969_LPM4.5_SVSOFF) + 50 nA (TPL5100)

Table 6. MSP430 Lowest Power Consumption

PARAMETER		V_{CC}	–40°C		25°C		60°		85°C		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
$I_{LPM4.5}$	Low-power mode 4.5, excludes SVS[1]	2.2 V	0.02		0.02		0.02		0.08		
		3.0 V	0.02		0.02		0.02		0.08	0.35	µA

[1]   Low-power mode 4.5, excludes SVS test conditions:
      Current for brownout is included. SVS is disabled (SVSHE = 0). Core regulator is disabled.
      PMMREGOFF = 1, CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 1 (LPMx.5),
      f_{XT1} = 0 Hz, f_{ACLK} = 0 Hz, f_{MCLK} = f_{SMCLK} = 0 MHz

Table 7. TPL5100 Power Consumption

SYMBOL	PARAMETER	CONDITIONS	MIN[1]	TYP[2]	MAX[1]	UNIT
IVDD	Supply current[3]	PGOOD=VDD		30	50	nA
		PGOOD=GND		12		nA

[1]   Limits are specified by testing, design, or statistical analysis at 25°C. Limits over the operating temperature range are specified through correlations using statistical quality control (SQC) method.

[2]   Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.

[3]   Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.

3.4 bq25570 Overview

3.4.1 Features

- Ultra-low power DC-DC boost charger
  - Cold-start voltage: VIN ≥ 330 mV
  - Continuous energy harvesting from VIN as low as 100 mV
  - Input voltage regulation prevents collapsing high impedance input sources
  - Full operating quiescent current of 488 nA (typical)
  - Ship mode with < 5 nA from battery
- Energy storage
  - Energy can be stored to re-chargeable li-ion batteries, thin-film batteries, super-capacitors, or conventional capacitors
- Battery charging and protection
  - Internally set undervoltage level
  - User programmable overvoltage levels
- Battery good output flag
  - Programmable threshold and hysteresis
  - Warn attached microcontrollers of pending loss of power
  - Can be used to enable or disable system loads
- Programmable step down regulated output (buck)
  - High Efficiency up to 93%
  - Supports peak output current up to 110 mA (typical)
- Programmable maximum power point tracking (MPPT)
  - Provides optimal energy extraction from a variety of energy harvesters including solar panels, thermal and piezo electric generators

3.4.2 Applications

- Energy harvesting
- Solar chargers
- TEG harvesting
- Wireless sensor networks (WSN)
- Low-power wireless monitoring
- Environmental monitoring
- Bridge and structural health monitoring (SHM)
- Smart building controls
- Portable and wearable health devices
- Entertainment system remote controls

Table 8. Device Information[(1)]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
bq25570	VQFN (20)	3.50 × 3.50 mm

[(1)] For all available packages, see the orderable addendum at the end of the datasheet.

Typical Application Schematic
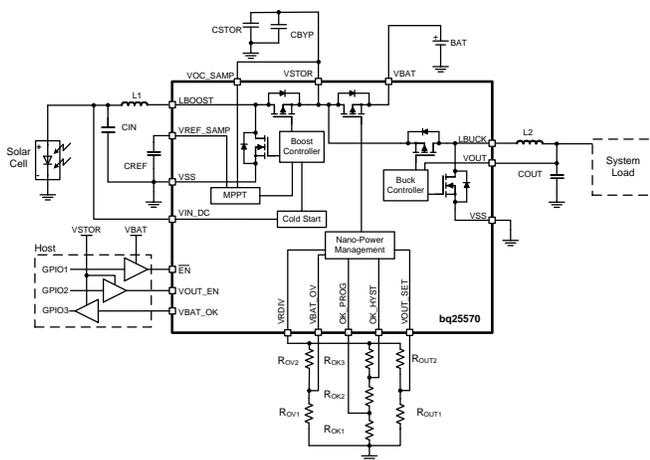
Charger Efficiency versus Input Voltage
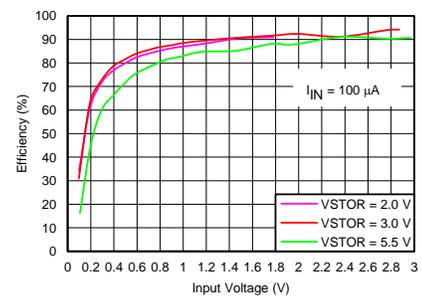
3.4.3 Description

The bq25570 device is specifically designed to efficiently extract microwatts (µW) to milliwatts (mW) of power generated from a variety of high output impedance DC sources like photovoltaic (solar) or TEGs without collapsing those sources. The battery management features ensure that a rechargeable battery is not overcharged by this extracted power, with voltage boosted, or depleted beyond safe limits by a system load. In addition to the highly efficient boosting charger, the bq25570 integrates a highly efficient, nano-power buck converter for providing a second power rail to systems such as WSNs, which have stringent power and operational demands. All the capabilities of bq25570 are packed into a small foot-print 20-lead 3.5×3.5-mm QFN package (RGR).

3.4.4   bq25570 MPPT Scheme

The bq25570 employs an MPPT known as the dynamic tracking of fractional voltage method. Dynamic means that the open circuit voltage is regularly sampled (16 seconds for the bq25570) and the input current is limited to ensure the input voltage of bq25570 stays above the defined fraction of the open circuit voltage (50% in the case of TEG).

The bq25570 provides a predefined setting for TEG, allowing the VOC_SAMP to be grounded to reduce the component count and set the ratio to 50%.

Table 9. Bias and MPPT Control Stage Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VOC_SAMPLE	Time period between two MPPT samples			16		s
VOC_STLG	Setting time for MPPT sample measurement of VIN_DC open circuit voltage	Device not switching		256		ms

Table 10. VOC_SAMP Pin Function

PIN		I/O	DESCRIPTION
NAME	NO.		
VOC_SAMP	3	1	Sampling pin for MPPT network. Connect to VSTOR to sample at 80% of input source open circuit voltage. Connect to GND for 50% or connect to the mid-point of external resistor divider between VIN_DC and GND.

3.4.5   bq25570 State Machine

The state machine of the bq25570 with respect to battery protection and usage of VBAT_OK is best explained in the bq25570 user's guide [8]:

> "To further assist users in the strict management of their energy budgets, the bq25570 toggles a user programmable battery good flag (VBAT_OK), checked every 64 ms, to signal the microprocessor when the voltage on an energy storage element or capacitor has risen above (OK_HYST threshold) or dropped below (OK_PROG threshold) a pre-set critical level. To prevent the system from entering an undervoltage condition or if starting up into a depleted storage element, it is highly recommended to isolate the system load from VSTOR by 1) setting VBAT_OK equal to the buck converter's enable signal VOUT_EN and 2) using an NFET to invert the BAT_OK signal so that it drives the gate of PFET, which isolates the system load from VSTOR."

The scope of this design is to further enhance the capabilities of the bq25570 state machine and system level efficiencies by allowing the system to reduce its battery drain when the battery is not charging by disabling the bq25570. To allow the system to still be operational the control logic has to be powered directly on the VBAT node and draw current in the order of magnitude of the self-discharge of the battery since the UVLO protection of the bq25570 cannot operate on loads connected in parallel to the battery. Those details are explained in Section 3.3.

3.4.6   bq25570 PCB Settings

To facilitate the PCB design of the bq25570, a configuration tool [7] has been made available to identify the different resistance sets needed to configure the bq25570.

Given the objectives VBAT_OV = 3.7 V:
VBAT_OK = 2.5 V, VBAT_OK_HYST = 2.6, VOUT = 2 V

The excel sheet with all values is also available as a collateral and can be downloaded as "TIDA-00246_collateral_bq25570Configurator.xls" found at TIDA-00246.

3.5 Front-End Protection

Figure 13. Front-End Protection Schematic

When it comes to reverse polarity protection, there are a few possible options:

- Passive full-wave rectifier
- Active full-wave rectifier
- Bi-stable relays
- Switch

The key parameters to consider when designing the protection are:

- How much above and below the max ratings of the selected IC is the input voltage going
- How fast the input voltage is going above the max ratings
- How often the input voltage is going beyond the max ratings of the IC

In this case, given the forward voltage, the diodes introduced in the option of the passive full-wave rectifier would significantly impact the energy harvested as it would reduce the ΔT from which energy would be harvested and would also reduce the total efficiency.

On the other hand, active rectification would add quiescent current, which would overall also reduce the system efficiency.

Bi-stable relays are also a technical option for connecting the TEG to the input of the bq25570 but are often considered cost prohibitive, so the relays were not designed in.

Given the thermal inertia of the radiator and more generally of any thermal system, the voltage would not change "fast" to go out of range. Fast being much lower than say 10 kHz was the reason why an ultra-low-power comparator like TLV3691 was selected.

For the switch, there are two options: series switch and shunt switch. A shunt switch is preferred when the input voltage raises too high for the monitoring circuit. Given the system specs (7 V_{OC_MAX}), a series switch was selected as it is easier to protect against negative voltages.

3.6 *Charging Detection*

According to Section 2, when there is no energy coming in the system, it is preferred to switch the harvesting IC "OFF" to reduce the leakage. To this end, the MCU should be notified when energy is flowing into the storage element to enable or disable the charging circuit.

3.6.1 Considered Options

To detect that the bq25570 is charging the battery, there are multiple options:

- Monitor the VSTOR voltage; however, this was dismissed as the battery could be charging yet have a higher load and lead to wrong decisions.
- Monitor the input voltage; however, given the possibility of a negative voltage this option is dismissed for this design. Also, because the design goal is to have a generic solution, voltage monitoring can be misleading for photovoltaics harvester. The two reasons (negative voltage, low accuracy for photovoltaics) being the reasons for not selecting this method for charging detection.
- Monitor the switch node and compare to the input voltage.
- Monitor the switch node and compare to the ground.

The key aspects when monitoring the switch node are:

- To remember that a boost convertor software node will be switching between GND (when the low side switch is ON) and OUT (when the low side switch is OFF but the high-side is ON) see Figure 14.
- Also parasitic capacitance should be reduced to minimum.
- Comparators should be selected with high-bandwidth to ensure the minimum pulse width.
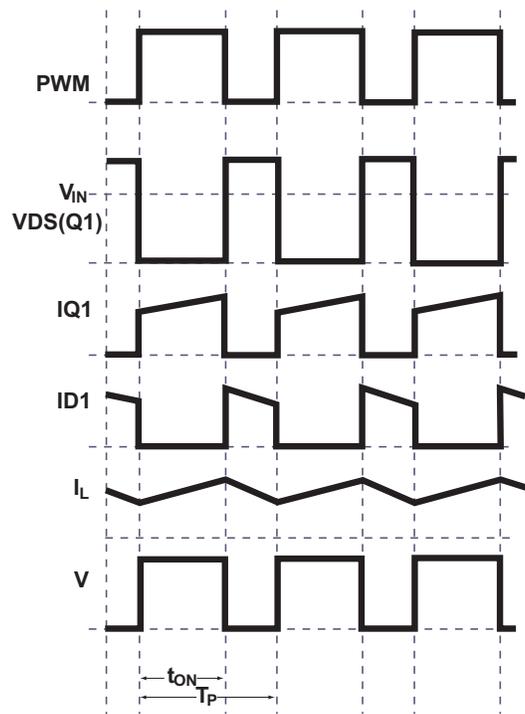
Figure 14. Boost – Voltage and Current Waveforms

A quick calculation to estimate the pulse width leads to

$$V_{out} / V_{in} = \frac{1}{1-D} \Leftrightarrow 1-D = V_{in} / V_{out} \geq \frac{1}{Fs} \times (1-D_{max}) = V_{in\_min} / V_{out\_max}$$

(10)

This leads to the small burst width is 18 ns (F_s = 1 MHz, V_{in_min} = 100 mV, V_{out_max} = 5.5 V)

Considering that a GPIO from MSP430FR5969 can only see a pulse of 20-ns wide (see the MSP430FR59xx datasheet [19]), a pulse stretcher topology was used, which offers the additional advantage of significantly reducing the parasitic capacitance added to the software node, and given bandwidth of pulse stretcher no further comparators are needed, the output is fed directly to the MSP430FR5969.

Another parameter for such a pulse stretcher is to ensure that the additional power consumption is kept low. To this effect, two things were done:

- The power of the pulse stretcher is taken from a GPIO to ensure that one the function is not needed, no current will be drawn
- The R and C were designed to achieve minimum power consumption when running.

It was decided that the function when running should not take more than 300 nA when VBATT is at its lowest (as higher power when the battery is charged is not so critical and also the circuit can be controlled by MSP430 GPIO so integral power consumption is small).

Given I = CDV / DT , I = 300 nA, and DVmax = 2.5 and DT = 1/1 MHz

$$\Leftrightarrow C = 300\,nA \times 1\,\mu S\,/\,2.5\,V = 0.12\,pF \tag{11}$$

To ensure that in steady state the voltage is settled, set 7 t = 7 × R × C = 1 μs

R ~ 1 MΩ

The FET was then selected to have the lowest gate charge.

3.6.2 Charge Detection Notification (Pulse Stretcher)
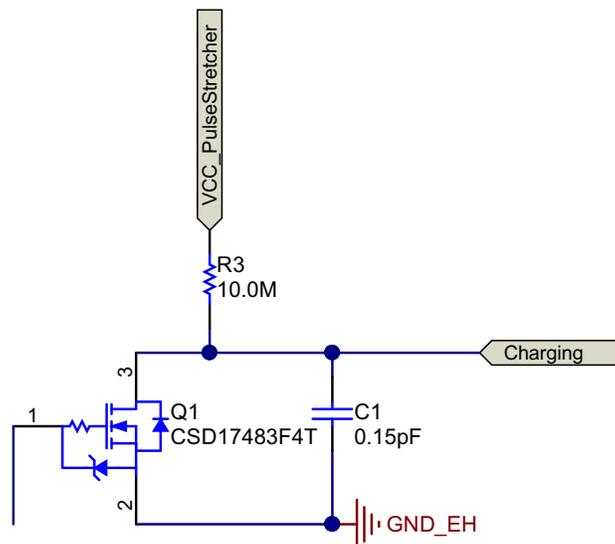
Figure 15. Charge_DETECT Schematic

3.7   *GEHAM and Selected Battery*

Given the requirements for 3.6- or 7.2-V output, this design is set on a 3.6-V output.

Given the objective to provide a generic energy harvesting adapter module, the system should provide voltages compatible with lithium-thionyle voltages. A lithium-thionyle battery typically operates in the 2.5- to 3.7-V range so the same is targeted for this design.

The bq25570 was selected as it allows an additional rail to power low-power devices. For low-power evaluations, a 2-V rail can be provided to facilitate evaluations of the most effective system setup, which depends on application needs (either running more effectively from a 2-V rail the MCU and rest of system but adding the quiescent of a 300-nA buck, or running from 3-V rail without the quiescent current of a buck.

To this end, the HLC-1550A battery was selected. Its features include:

- Capacity when charge to 3.67 V, 560 A
- Discharge end voltage 2.5 V (discharge below 2.5 V at RT may increase the HLC internal impedance)
- Nominal capacity 560 As (155 mAh) at 3.6 V

Given an average power consumption of 3 mW, the autonomy of the system is:

$$\frac{3.6\ V \times 155\ mAh}{13\ mW} \approx 8\ days \tag{12}$$

3.8 *Design for Test*

To facilitate the test and characterization, the following features were added to the core functionality of the design.

3.8.1 Design Identification

For forward compatibility, U5 is added to allow automatic identification of the BoosterPack added on top of a launchpad. The MCU on the BoosterPack can read through I^{2}C, the values of GPIO connected on the U5 circuit, and know the unique ID of the design as well as the revision.

3.8.2 Signal Monitoring

The following headers are added to facilitate signal monitoring and configuration of the design:

- J1: Input voltage for the TEG
- J2: Interface to the LaunchPad
- J3: Interface to the LaunchPad
- J4: Power the LaunchPad from the BoosterPack (intended functionality)

NOTE: In this configuration, the LaunchPad power must be removed. Refer to the respective LaunchPad documentation for removing appropriate jumpers.

- J5: Power the launchpad from 5 V.
  This function is only provided for forward compatibility and not intended to be used on this version
- J6, J7, J8: I^{2}C address settings for U5
- J9: Control of the bq25570 enable signal either through hardware (connect J9:2 to J9:1 to enable) or through GPIO from the LaunchPad (connect J9:2 and J9:3)
- J10: Control of the buck integrated in the bq25770 either through jumpers or through GPIO from the LaunchPad
- J11: Jumpers to control the FE
- J12: Jumpers enabling loads to be disconnected from the battery when the battery falls below the UVLO level. To enable this functionality, connect a load ground to J12:2.
  This jumper is in association to Q2, which will disconnect loads when VBATT_OK goes "LOW", when VBATT_OK goes "HIGH" its RDS(on) is specified as 240 mΩ (under VGS = 2.5 V)
- J13: Control of the charge detect functionality.
  Connecting J13:2 with J13:1 allows the software to control if the function draws current or not (and resultantly if the MSP430 will get interrupts when the bq25570 is charging the battery).
- J14: Jumpers to connect or disconnect the charge notification to the MCU. This jumper can also be used to monitor the signal "CHARGING"
- J15: Jumpers to by-pass the front-end protection
- J16: Jumpers to select the power source or power reserve of the system:
  - If a power source is connected to J16:2, it can be used to control the system power consumption
  - If J16:2 and J16:3 are connected together, the system is running from the battery
  - if J16:2 and J16:1 are connected together, the system is running from the 10 µF (which allows to see faster voltage changes than with the default 250-mAh battery).
- J17: Allows to connect VSTOR to the 3.3-V rail from the rest of the system

3.8.3 BoosterPack Setup

To allow rapid prototyping, the reference design is made to follow the electrical convention of BoosterPacks, which allows different MCU (on the LaunchPad) to be tested.

For more details on BoosterPack, LaunchPad and Energia, TI rapid prototyping environment refer to:

- http://www.ti.com/tool/Energia
- http://www.ti.com/ww/en/launchpad/boosterpacks.html
- http://www.ti.com/ww/en/launchpad/launchpad.html

4 Layout Considerations

The reference design features the following devices.

4.1 bq25570

For layout of the bq25570, follow the guidelines from the [bq25570 datasheet](#).

4.2 TPL5100

For layout of the TPL5100, follow the guidelines from the [TPL5100 datasheet](#).

4.3 MSP430FR5969

Pay special attention to the power supply decoupling and bulk capacitors recommendations from the [MSP430FR5969 datasheet](#).

4.4 TLV3691

For layout of the TLV3691, follow the guidelines from the [TLV3691 datasheet](#).

5   Verification and Characterization

5.1   Test Setup

5.1.1   Measuring TEG Impedance for Startup-Voltage Characterization

As detailed in Section 2.1, the impedance of the TEG is a key electrical characteristics. For a test setup to characterize electrical performances, it is important to get a realistic figure for this impedance.

However, because Ohm meters usually inject a small amount of current in the load to measure the voltage drop generated (or a small voltage and measuring the current) [18], this current will create a small ΔT across the TEG, which will induce a small emf and cause bad readings.

To measure the R_{TEG-el}, the following procedure is recommended by II-VI Marlow:

*   Do not measure impedance with a DC resistance meter, you must use an AC resistance meter
*   There should be no ΔT across the TEG (that is, heat source should be turned off); otherwise, the output of the TEG will impact the resistance reading

Using an LCR Meter 4270, the electrical resistance of the II-VI Marlow TEG was measured at 10 Ω, which is the expected value given the two elements in series each having a 5-Ω internal impedance.

5.1.2   Deep_Sleep Testing Jumpers Configuration

To test the Deep_Sleep enter and exit sequence, the following jumper configurations are needed:

To measure the system current consumption, the jumper settings are as follow (counter-clockwise from the top right corner of the PCB):

*   J16:2 (VBATT)→Connected to PSU to measure the current, emulate a battery being connected to the system when no power is available at the input
*   J12:3 (GND_EH)→Connect to the PSU to measure the current
*   J13:1↔J13:2 to ensure that the "Charge Detection" is disabled through software

> **NOTE:** J13:1 --- J3:20 --- BP11 - P1.3 - GPIO drive low.

*   J10:1 and J10:2 are connected to ensure bq25570 DC/DC is disabled (to reduce power), controlled by GPIO. J10:1 = J2-9 = BP8 = P3.5, which is set high by software

Table 11. bq25570 Logic Level: VOUT_EN

PIN		I/O	DESCRIPTION
NAME	NO.		
VOUT_EN	6	I	Active high digital programming input for enabling and disabling the buck converter. Connect to VSTOR to enable the buck converter.

*   J9:2 and J9:3 are connected to ensure the bq25570 charging is disabled (to reduce power). J2:9 = BP5 = P4.3 is set high by software

Table 12. bq25570 Logic Level: $\overline{EN}$

PIN		I/O	DESCRIPTION
NAME	NO.		
$\overline{EN}$	5	I	Active low digital programming input for enabling and disabling the IC. Connect to GND to enable the IC.

- J5: Do not connect (not used with MSP-EXP430FR5969 as the board does not have a 5-V supply→J5 is left open)
- J4:3 and J4:2 must be connected so the LaunchPad is powered from the BoosterPack VBATT node

---

CAUTION

The MSP430FR5969 on the LaunchPad is by default powered from the USB. In this test setup, the device will be powered by the TIDA-00246 BoosterPack. Carefully follow instructions from the *MSP-EXP430FR5969 LaunchPad User's Guide* (SLAU535) on jumper settings needed for this configuration (see Figure 16 for guidance).

Note that only removing the V+ and GND is not enough to isolate the target from the eZ-FET section as the debug signals are driven from the eZ-FET section and thus the source power to the target.
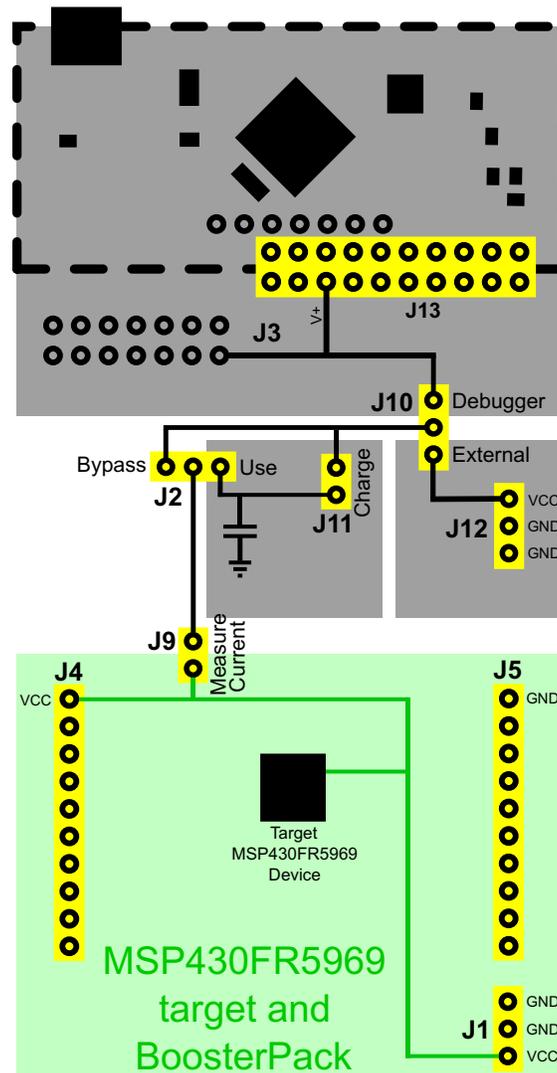
Figure 16. LaunchPad Jumper Configurations

- J17: VSTOR; To be connected to 3V3 from PSU (for testing purposes only): J17:1 ↔ J17:2
- Connect J14:1 and J14:2 (charge detect functionality; connect to avoid floating input on MSP430 as J14:1 – J3:18 – BP12 – P1.4; input pull-down low)
- J15: Front-end bypass; do not connect
- J1: TEG input; do not connect as in Deep_Sleep. Do not have any TEG voltage present
- J6, J7, J8: TIDA-identification. Do not leave floating → connect to GND
- J11: Front-end; do not connect

CAUTION

If in possession of an E1 hardware, cut the traces from 3V3 to U5 to avoid the U5 IC current consumption to be taken into account when measuring the Deep_Sleep current consumption. Also, connect through the blue wire the GND_EH and GND traces.

NOTE: To obtain representative numbers, do not connect scope probes to the PCB.

5.1.3 Board Enter and Exit Deep_Sleep – Test Code Validation – LaunchPad Only
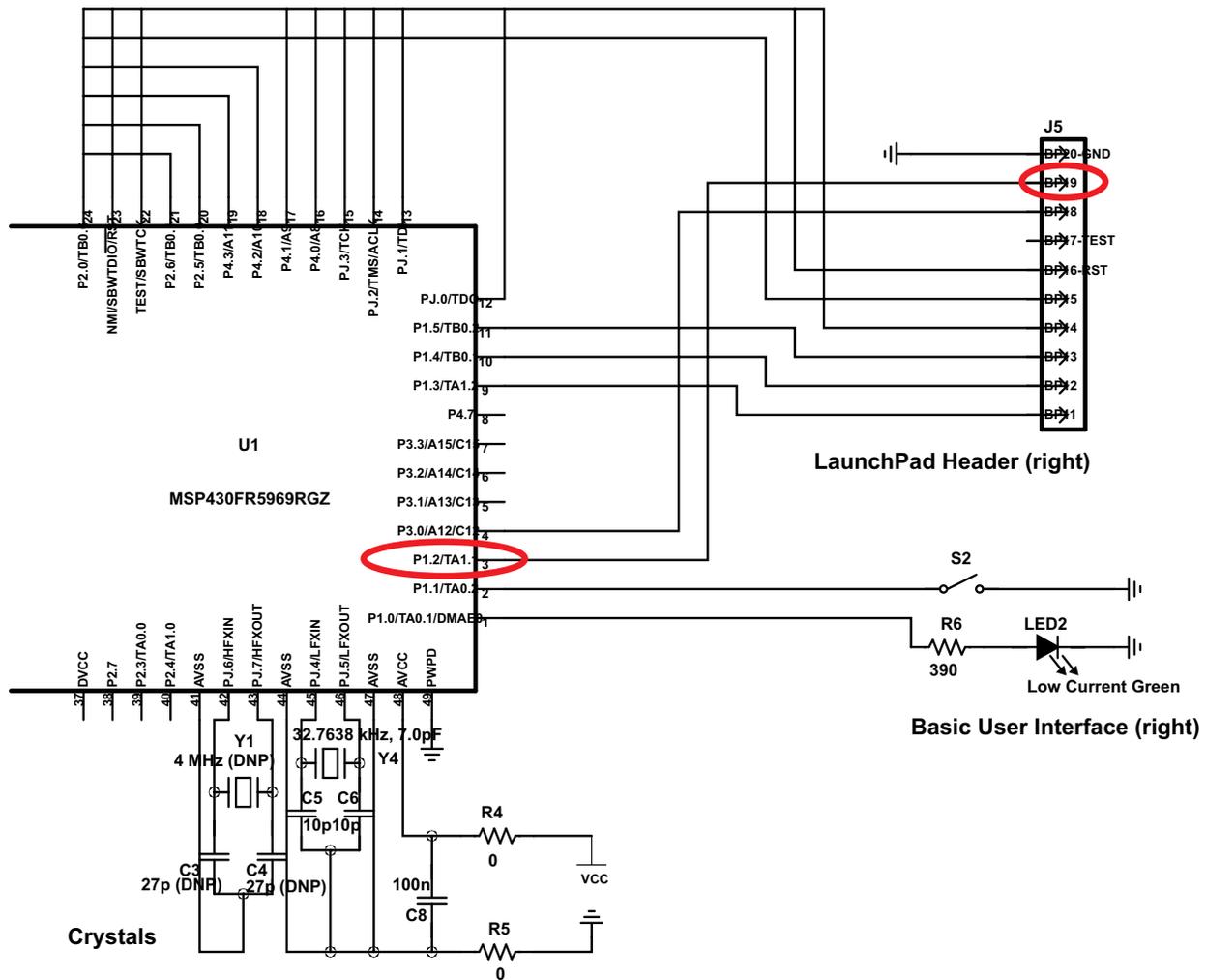
Figure 17. MSP-EXP430FR5969 Schematic Highlighting P1.2 and BP19

Testing of the functionality can be first tested on a LaunchPad only by slightly modifying one of the MSP430FR5969 code example:

1. Open the "msp430fr59xx_lpm4-5_02.c" from the project named "Entering and waking up from LPM4.5 via P1.1 interrupt with SVS disabled"

   Applying following software patch at
   1) diff -r .\msp430fr59xx_lpm4-5_02\msp430fr59xx_lpm4-5_02.c .\TIDA-00246_GoBackToDeepSleepTest.c
   46c46,50
   > // Credits: based on the LPM4.5 code demo from William Goh / Andreas Dannenberg
   > //
   > // TIDA-00246 DEMO - Entering and waking up from LPM4.5
   > // via P1.1 interrupt (Launchpad S2)
   > // or via P1.2 interrupt (WAKEUP from TIDA-00246)
   50,51c54,57
   > // LPM4.5 is correctly entered. Use a button S2 (or P1.1) on the
   > // EXP board to wake the device up from LPM4.5. This will enable
   - - -
   > // LPM4.5 is correctly entered.
   > // Use a button S2 (or P1.1) on the EXP board
   > // or wait for WAKEUP (P1.2) from the booster pack
   > // to wake the device up from LPM4.5. This will enable
   63c69,71
   < // | P4.6|---> LED1 (MSP-EXP430FR5969)
   - - -
   > // | |
   > // | | ___ J6
   > // | P4.6|--| |-> LED1 (MSP-EXP430FR5969)
   65a74,80
   > // | P1.2|<--- J5.19 = WAKEUP from BoosterPack (TIDA-00246BP)
   > // | P1.3|---> BP11 = Charge Detect Enable (drive 'LOW' for DeepSleep)
   > // | P1.4|<--- B12 = Charge Notification (no pull-down)
   > // | P4.3|---> BP5 -> /EN bq25570 (drive 'HIGH' to disable bq25570
   > // | P3.4|---> BP8 -> VOUTEN bq25570 (drive 'HIGH' to disable bq25570 buck DCDC)
   > // | PJ.0|---> NOT CONNECTED ON PCB !?!?!!!!!!! -> BP17 >-J3:8------>DONE (tpl5100)
   > // | P1.6|--->
   -> BP15->J3:12---blue wire -> J3:8^
   67c82
   < // William Goh / Andreas Danneberg
   - - -
   > // M. Chevrier
   69c84
   < // June 2014
   - - -
   > // 2015/Feb/28
   73a89,92
   > #define TIDA00246 1 //we differentiate the case with TIDA-00246 BoosterPack
   > #ifndef TIDA00246
   > #define EXPMSP430FR5969 1 //from the case without TIDA-00246 as the MSP430 input need pull-up / pull-down to not be floating
   > #endif
   74a94
   >
   75a96,98
   > int i;
   > int LPM45;
   >
   78,80c101,106
   < // Configure GPIO
   < P1OUT = 0; // Pull-up resistor on P1.1

```
< P1DIR = 0xFF; // Set all but P1.1 to output direction
- - -
>
>
> // Determine cause for entering main()
> if (SYSRSTIV == SYSRSTIV_LPM5WU) {
> //we came here from LPM4.5
>
82,83c108,176
< P2OUT = 0;
< P2DIR = 0xFF;
- - -
>
>
> // PJSEL0 = BIT4; // For XT1
> //
> // // Clock System Setup
> // CSCTL0_H = CSKEY >> 8; // Unlock CS registers
> // CSCTL1 = DCOFSEL_0; // Set DCO to 1MHz
> // CSCTL2 = SELA__LFXTCLK | SELS__DCOCLK | SELM__DCOCLK;
> // CSCTL3 = DIVA__1 | DIVS__1 | DIVM__1; // Set all dividers
> // CSCTL4 &= ~LFXTOFF;
>
>
> // Disable the GPIO power-on default high-impedance mode to activate
> // previously configured port settings. The oscillator should now start...
> // PM5CTL0 &= ~LOCKLPM5;
> LPM45=1;
>
> }
> else {
> LPM45=0;
> }
> /*
> After the wake-up from LPM4.5 the state of the I/Os are locked and remain unchanged until you clear the
> LOCKLPM5 bit in the PM5CTL0 register.
> Do the following steps after a wake-up from LPM4.5:
> 1. Initialize the port registers exactly the same way as they were configured before the device entered
> LPM4.5 but do not enable port interrupts.
> 2. Clear the LOCKLPM5 bit in the PM5CTL0 register.
> 3. Enable port interrupts as necessary.
> 4. After enabling the port interrupts the wake-up interrupt will be serviced as a normal interrupt.
> If a crystal oscillator is needed after a wake-up from LPM4.5 then configure the corresponding pins and
> start the oscillator after you cleared the LOCKLPM5 bit.
> */
>
>
>
>
> // | P1.0|---> LED2 (MSP-EXP430FR5969
> // | |
> // | |___ J6
> // | P4.6|--| |-> LED1 (MSP-EXP430FR5969)
> // | |
> // | | P1.1|<--- S2 push-button (MSP-EXP430FR5969)-interrupt MUST be enabled to wake-up from LMP4.5
> // | P1.3|---> BP11 = Charge Detect Enable (drive 'LOW' for DeepSleep)
```

```
> // | P1.4|---> BP12 = Charge Notification (no pull-down)
> // | P4.3|---> BP5 -> /EN bq25570 ( drive 'HIGH' to disable bq25570
> // | P3.4|---> BP8 -> VOUTEN bq25570 ( drive 'HIGH' to disable bq25570 buck DCDC)
> // | PJ.0|---> NOT CONNECTED ON PCB !?!?!!!!!!! -> BP17 >-J3:8------>DONE (tpl5100)
> // | P1.6|---> -> BP15->J3:12---blue wire -> J3:8^
>
>
>
> // P1.2 does not need a pull-up or pull-down as it is driven actively by TPL5100
> //below two lines not needed for application but added for testing to ensure the LaunchPad does not
have floating pins when measuring consumption of LP only before connecting BP
>
>
> // Configure GPIO, by default output low
> P1DIR = 0xFF ^ (BIT1|BIT2|BIT4); // Set all to output except P1.1, P1.2 P1.4
> P1OUT = (BIT1 |BIT2); // Set all GPIO to low except P1.1 and P1.2
> #ifdef TIDA00246
> P1REN = ( BIT1 | BIT4); // Enable pull for P1.1 and P1.4
> #endif
> #ifdef EXPMSP430FR5969
> P1REN = ( BIT1 | BIT4 | BIT2); // Enable pull for P1.1 and P1.4
> #endif
>
> P2OUT = 0;
> P2DIR = 0xFF;
85,96c178,186
< P3OUT = 0;
< P3DIR = 0xFF;
<
< P4OUT = 0;
< P4DIR = 0xFF;
<
< PJOUT = BIT4; // Set PJ.4 / LFXTIN to high
<
< // Determine whether we are coming out of an LPMx.5 or a regular RESET.
< if (SYSRSTIV == SYSRSTIV_LMP5WU) {
< PJSEL0 = BIT4; // For XT1
- - -
> P3DIR = 0xFF; // all output
> P3OUT = BIT4; // all all low except P3.4, must be 'high' for bq25570 buck
>
> P4DIR = 0xFF; // all output
> P4OUT = BIT3; // all all low except P4.3, must be 'high' for bq25570 charger
> // P4OUT &= ~BIT6;
>
> PJDIR = 0xFFFF;
> PJOUT = 0; // keep xal 32k off
98,110c188,190
< // Clock System Setup
< CSCTL0_H = CSKEY >> 8; // Unlock CS registers
< CSCTL1 = DCOFSEL_0; // Set DCO to 1MHz
< CSCTL2 = SELA__LFXTCLK | SELS__DCOCLK | SELM__DCOCLK;
< CSCTL3 = DIVA__1 | DIVS__1 | DIVM__1; // Set all dividers
< CSCTL4 &= ~LFXTOFF;
<
< // Configure LED pin for output
< P1DIR |= BIT0;
<
< // Disable the GPIO power-on default high-importance mode to activate
< // previously configured port settings. The oscillator should now start...
```

```
< PM5CTL0 &= ~LOCKLPM5;
- - -
> // Disable the GPIO power-on default high-impedance mode to activate
> // previously configured port settings
> PM5CTL0 &= ~LOCKLPM5;
112,132c192,236
< do {
< CSCTL5 &= ~LFXTOFFG; // Clear XT1 fault flag
< SFRIFG1 &= ~OFIFG;
< } while (SFRIFG1 & OFIFG); // Test oscillator fault flag
< }
< else {
< // Configure P1.1 Interrupt
< P1OUT |= BIT1; // Pull-up resistor on P1.1
< P1REN |= BIT1; // Select pull-up mode for P1.1
< P1DIR = 0xFF ^ BIT1; // Set all but P1.1 to output direction
< P1IES |= BIT1; // P1.1 Hi/Lo edge
< P1IFG = 0; // Clear all P1 interrupt flags
< P1IE |= BIT1; // P1.1 interrupt enabled
<
< P4OUT |= BIT6; // Turn on P4.6 (LED1) on EXP board
< // to indicate we are about to enter
< // LPM4.5
<
< // Disable the GPIO power-on default high-impedance mode to activate
< // previously configured port settings
< PM5CTL0 &= ~LOCKLPM5;
- - -
> P1IES |= (BIT1|BIT2); // P1.1 and P1.2 Hi/Lo edge
> P1IFG = 0; // Clear all P1 interrupt flags
> P1IE |= (BIT1|BIT2); // P1.1 and P1.2 interrupt enabled
>
>
>
> // // Clock System Setup
> // CSCTL0_H = CSKEY >> 8; // Unlock CS registers
> // CSCTL1 = DCOFSEL_0; // Set DCO to 1MHz
> // CSCTL2 = SELA__LFXTCLK | SELS__DCOCLK | SELM__DCOCLK;
> // CSCTL3 = DIVA__1 | DIVS__1 | DIVM__1; // Set all dividers
> // CSCTL4 &= ~LFXTOFF;
>
>
>
> // do {
> // CSCTL5 &= ~LFXTOFFG; // Clear XT1 fault flag
> // SFRIFG1 &= ~OFIFG;
> // } while (SFRIFG1 & OFIFG); // Test oscillator fault flag
>
>
> if (LPM45==1){
> //we enter here because we exited LPM4.5: either SW2 or WAKE signal from TPL5100
> //so we toggle P1.6 = DONE signal to clear the TPL5100
> P1OUT |= BIT6;
> // P1OUT |=BIT6;
> // __delay_cycles(1);
> P1OUT &= ~BIT6; //we toggle P1.7 to indicate TPL5100 we are 'done'
> P4OUT |= BIT6; //we toggle P4.6 to indicate LPM4.5
>
> //
> // for (i=20;i>0;i--){
```

```
> // P4OUT ^= BIT6; // P4.6 = toggle to show we woke-up from lpm4.5
> // __delay_cycles(1);
> // }
> }
> else{
> for (i=20;i>0;i--){
> P1OUT ^= BIT0; // P1.0 = toggle and
> P4OUT ^= BIT6; // P4.6 = toggle to show we just powered-up
> __delay_cycles(100000);
> }
> }
>
>
135,138c239,242
< PMMCTL0_H = PMMPW_H; // Open PMM Registers for write
< PMMCTL0_L &= ~(SVSHE); // Disable high-side SVS
< PMMCTL0_L |= PMMREGOFF; // and set PMMREGOFF
< PMMCTL0_H = 0; // Lock PMM Registers
- - -
> PMMCTL0_H = PMMPW_H; // Open PMM Registers for write
> PMMCTL0_L &= ~(SVSHE); // Disable high-side SVS
> PMMCTL0_L |= PMMREGOFF; // and set PMMREGOFF
> PMMCTL0_H = 0; // Lock PMM Registers
140,147c244,248
< // Enter LPM4 Note that this operation does not return. The LPM4.5
< // will exit through a RESET event, resulting in a re-start
< // of the code.
< __bis_SR_register(LPM4_bits);
<
< // Should never get here...
< while (1);
< }
- - -
> // Enter LPM4 Note that this operation does not return. The LPM4.5
> // will exit through a RESET event, resulting in a re-start
> // of the code.
> __bis_SR_register(LPM4_bits);
> }
149,154d249
< // Now blink the LED in an endless loop.
< while (1) {
< P1OUT ^= BIT0; // P1.0 = toggle
< __delay_cycles(100000);
< }
```

2. Use a wire to connect BP19 to VCC (BP1).
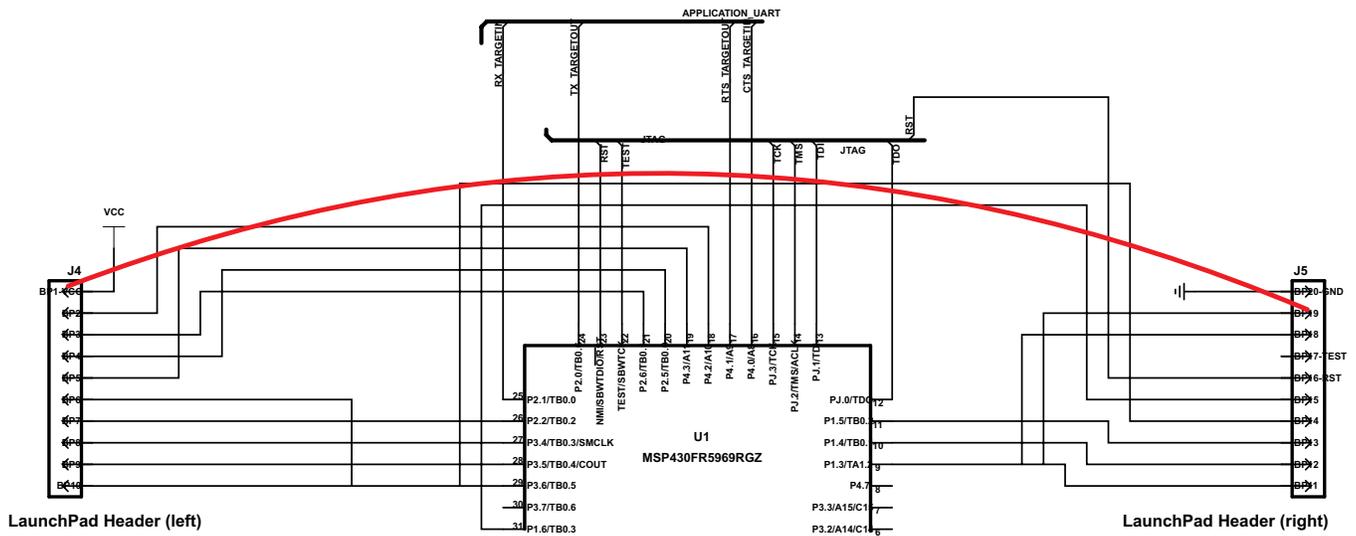
Figure 18. LaunchPad Connectors and Connections Highlighted

3. Disconnect the cable between BP19 and BP1 and connect it to BP20 (that is, simulating a high-to-low transition on P1.2).

4. The LED1 will start blinking RED.

5.1.4 Measuring Power Consumption of Boards for Currents < 100 nA

Given the challenge to find test equipment which measures current below 100 nA, the following setup is used:

- A PSU (E3631A) supplies 3.3 V.
- A resistor measured to be at 1 MΩ is put in series with V+.
- A HP34401A measures across the resistor the voltage drop.

NOTE: A wire is used to short the resistor to allow the system to power-up properly before the current is measured.
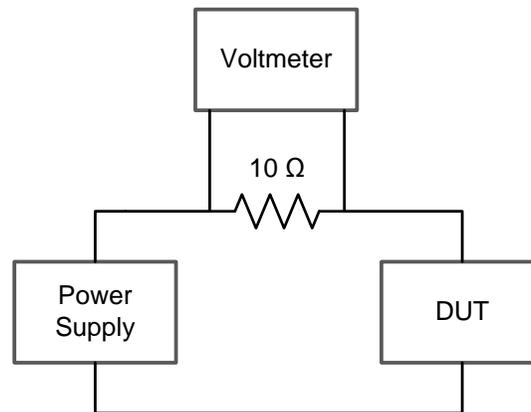
Figure 19. Setup Used to Measure Current Below 100 nA

The test procedure is as follows:

1. Set power supply unit (PSU) to target voltage: 2.5 V.
2. Enable PSU outputs:
   (a) Check that voltmeter has a reading < 1 mV (to ensure that the 1 MΩ is shorted so the inrush current from all parasitic caps supply the board properly (to ensure the MSP430 boots properly)
   (b) If the voltmeter was not shorted, set PSU voltage to 0, wait for 10 seconds (to ensure all parasitic capacitors are discharge), and start again from Step 1.
3. Wait for one minute. To ensure that the inrush current is over, see Section 5.1.
4. Remove short from the voltmeter to be able to read voltage.
5. Read voltage from the voltmeter. Read multiple times to assess the noise in measurement.
6. Go back to Step 1 and increase the PSU voltage by 100 mV from the previous value.

5.1.5 Startup Voltage

When testing the startup voltage of the TIDA-00246, remember the system is designed to handle power sources with limited capabilities.

CAUTION

If V_{IN_DC} is higher than VSTOR and VSTOR is equal to VBAT_OV, the input V_{IN_DC} is pulled to ground through a small resistance to stop further charging of the attached battery or capacitor. It is critical that if this case is expected, the impedance of the source attached to V_{IN_DC} be higher than 20 Ω and not a low impedance source.

To have more representative results, an impedance in series with the power supply of value equivalent to the impedance of the harvester should be placed.

For TEG, the impedance of the TEG should be measured as described in Section 5.1.1.

Should the impedance of the TEG be less than the recommended impedance, the maximum rating of the bq25570 for input power is 510 mW, which must under no condition be exceeded.

		MIN	MAX	UNIT
Input voltage	VIN_DC, VOC_SAMP, VREF_SAMP, VBAT_OV, VRDIV, OK_HYST, OK_PROG, VBAT_OK, VBAT, VSTOR, LBOOST, EN, VOUT_EN, VOUT_SET, LBUCK, VOUT[2]	−0.3	5.5	V
Peak Input Power, PIN_PK			510	mW
Operating junction temperature, T_J		−40	125	°C
Storage temperature, T_{stg}		−65	150	°C

Figure 20. Absolute Maximum Ratings

5.1.6 Active Mode

The setup to measure the active mode is the same as the Deep_Sleep mode except that the software is changed to enable the different functions.

- P1.3 drives the "Charge Detection Enable" is configured as output high\
- P1.4 is the input for the charge detect notification is configured as "INPUT" without pull-down or pull-up as the signal is driven by the charge detect circuit
- P1.6 is by default output low and generates the "DONE" signal to acknowledge the "WAKE" signal from TPL5100
- P3.4 is output "LOW" to enable the bq25570 charge functionality
- P4.3 is output "LOW" to enable the bq25570 DC/DC buck functionality
- The jumpers are set (order anti-clockwise on the PCB):
- VBATT supplied on J16:2 (3.3 V)
- GND on J12:3
- J13:2 and J13:1 are connected together to enable the control by the GPIO from MSP430
- J10:2 and J10:1 are connected together to enable the control by the GPIO from the MSP430 of the bq25570 buck
- J9:2 and J19:1 are connected together to enable the control by the GPIO from the MSP430 of the charging by the bq25570
- J5 is not connected
- J4 is not connected
- J17:1 and J17:2 are connected
- J14:1 and J14:2 are connected to allow the GPIO from MSP430 to be biased
- J15:1 and J15:2 are connected to by-pass the front-end
- J1:2 is connected to the TEG V+
- J1:1 is connected to the TEG V– (which is also connected to PSU GND)

5.2   Thermal Test Results

5.2.1   TEG Load Matching and Impedance Measurements

Figure 21 shows the theoretical values and the measured values for output voltage and output power.
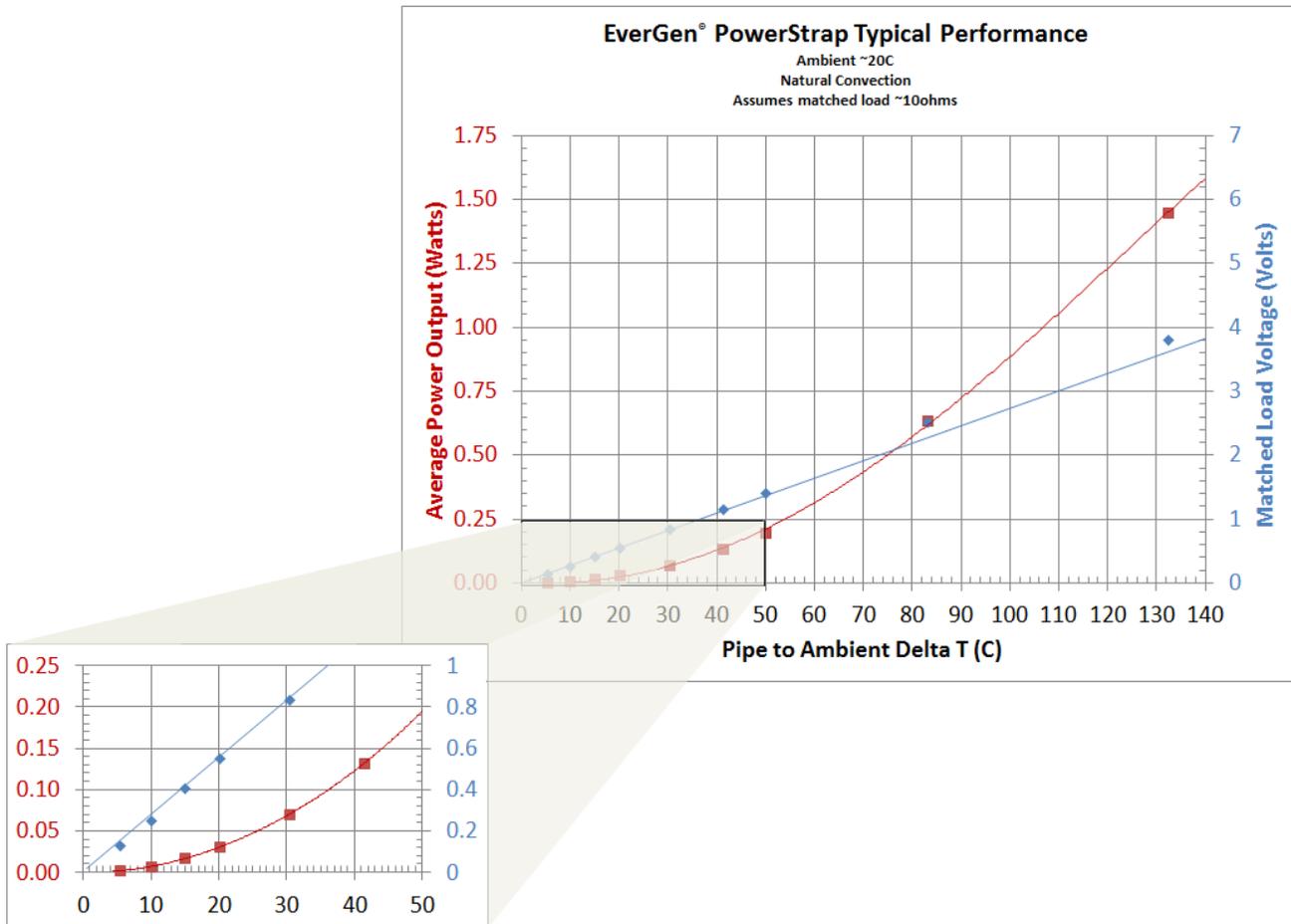
Figure 21. TEG_Vout_Pout

5.2.2   Thermal Data from II-VI Marlow
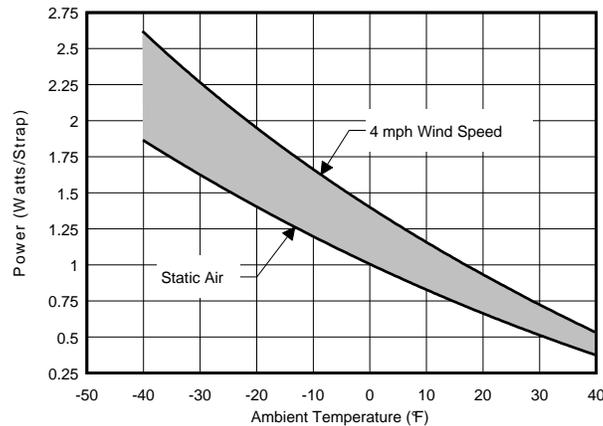
Figure 22. Power Generation With Wind Speed

5.2.3   Field Measures from II-VI Marlow

Figure 23 is an extra month of characterization in open air conditions ran by II-VI Marlow showing that in the hottest month of the year (when the ΔT is the smallest) an overall net increase of the power going into the battery. The small dips are during the hottest hours of the day when the battery is supplying more power than it is receiving. Nonetheless, it shows the total viability of a system that has a positive energy balance even in worst case conditions in the field.
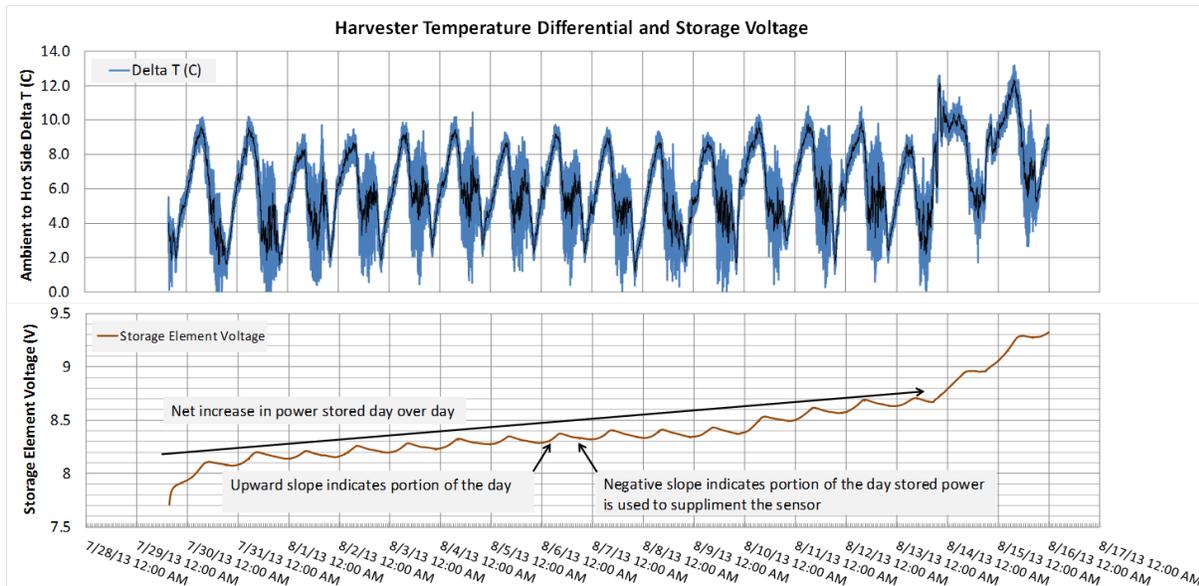
Figure 23. II-VI Marlow Field Testing

6   Test Results

6.1   *Board Boot Timing Diagram*

Figure 24 is one example of how the current varies over time, showing that every time the supply is varied a long time needs to be waited for taking a representative measurement of the current consumption.
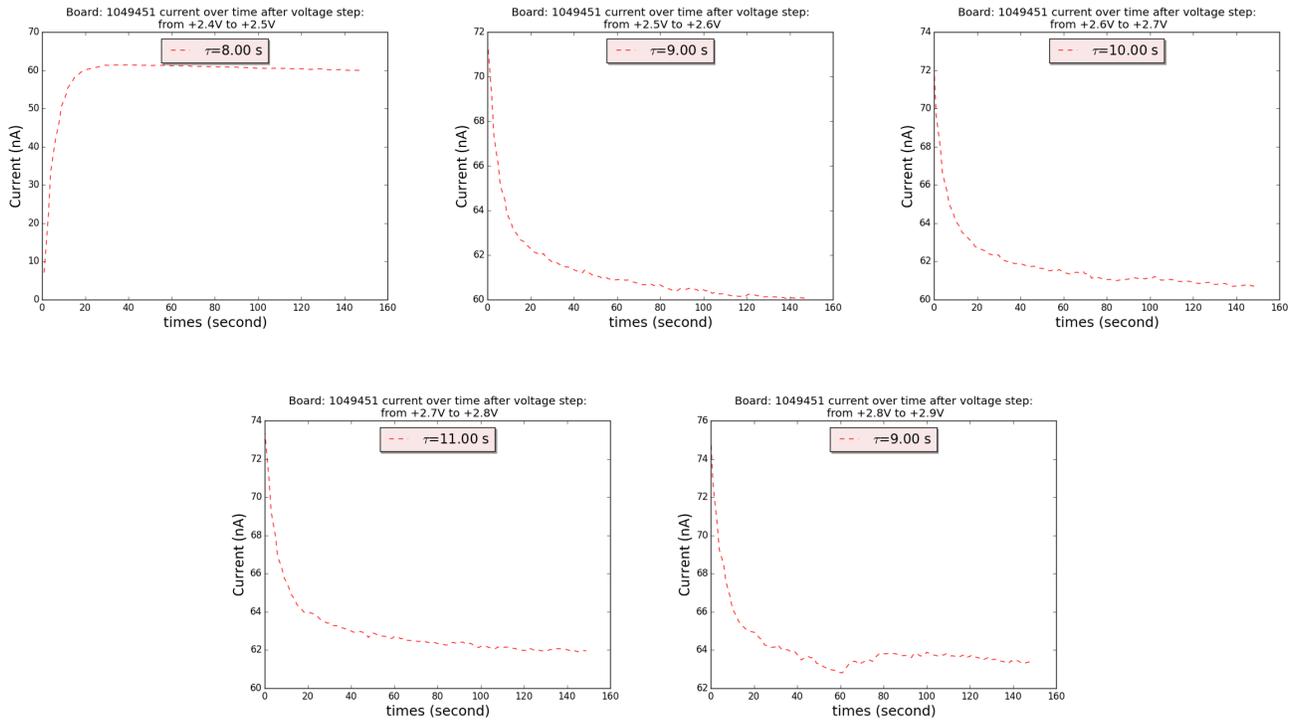
Figure 24. Current Response to 100-mV Step

As seen in the above plots, the current will slowly decay to its final value. This behavior is totally normal but needs to be taken into consideration during any test procedure that uses the setup described in Section 5.1.4.

The reason for this behavior is simply that there is a 1-MΩ resistor, which makes a RC circuit with the 10-µF capacitor mounted on the PCB of TIDA-00246 (C1 on top-right corner)
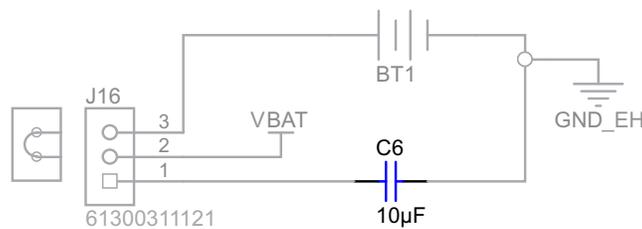
Figure 25. Schematic Extract Showing 10-µF Capacitor

6.2   LaunchPad Only Power Consumption Measurement
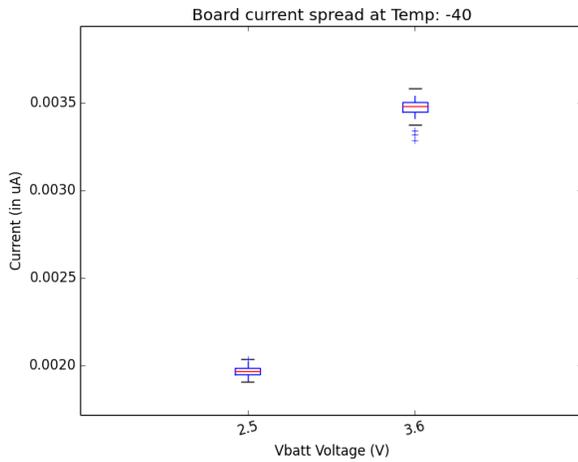
Figure 26. Current Measurement for the LaunchPad at –40°C With 2.5 and 3.6 V on 3.3-V Rail
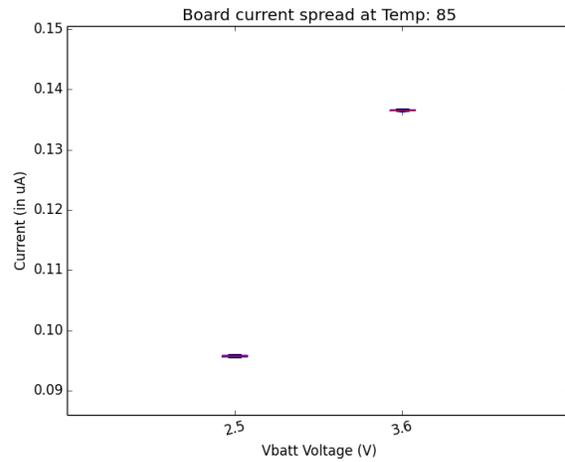
Figure 27. Current Measurement for the LaunchPad at 85°C With 2.5 and 3.6 V on 3.3-V Rail

6.3   Power Consumption TIDA-00246 Booster Pack + MSP-EXP430FR5969

Following the setup in Section 5.1 and with a resistor measured at 0.917 MΩ, a voltage drop of 65 mV is measured in series with the power supply.

Leading to an equivalent power consumption from the system in deep sleep of 76 nA at room temperature.

Section 6.5 gives more statistical information about current consumption as a function of temperature and voltage.

6.4 Scope Plot of System Exiting and Going Back to Deep_Sleep

When the system wake-up needs to be tested, the switch S2 can be used.
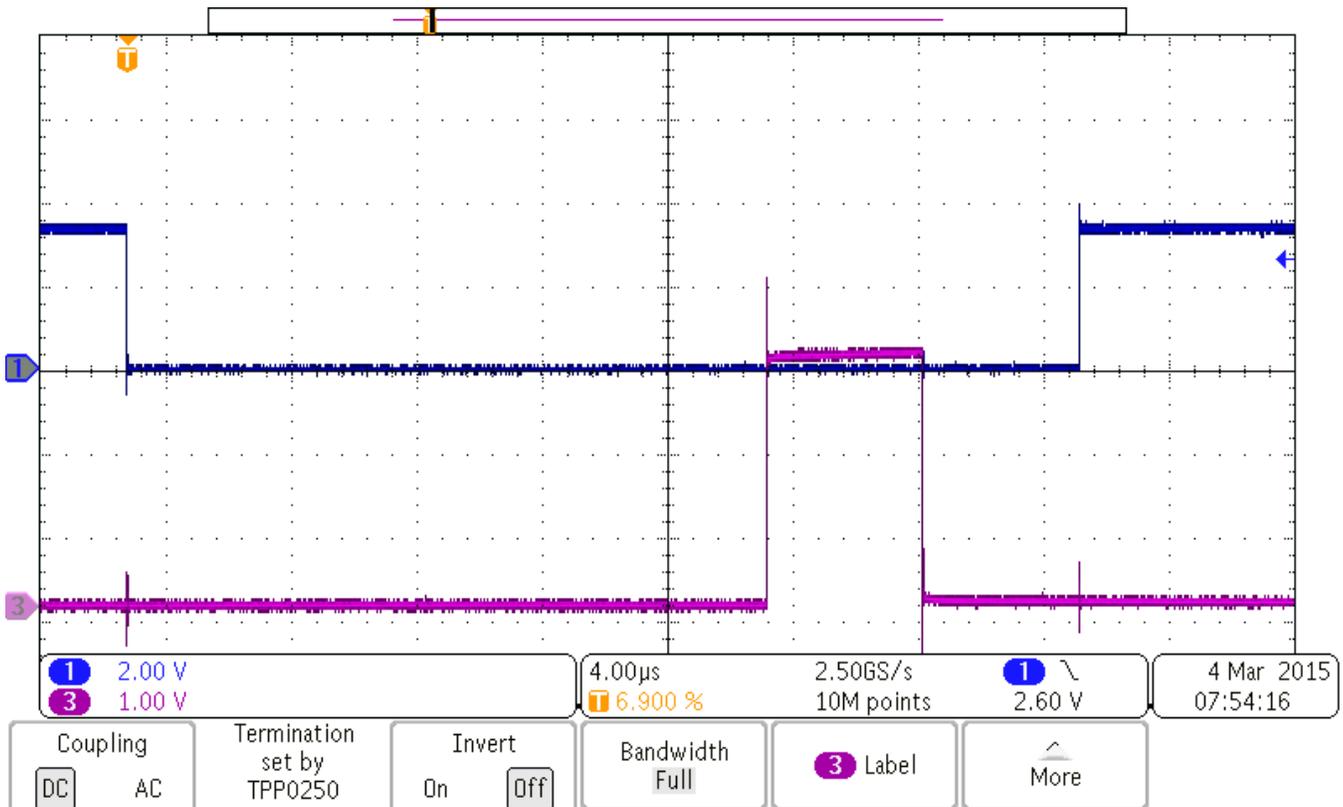
Figure 28. TIDA-00246 + MSP-EXP430FR5969, Exiting and Re-Entering Deep_Sleep

NOTE: Ch1: P4.6 (set to 'LOW' when exiting LPM4.5 and 'HIGH' just before entering LPM4.5)
CH3: P1.6 (DONE signal from MSP340 back to TPL5100)
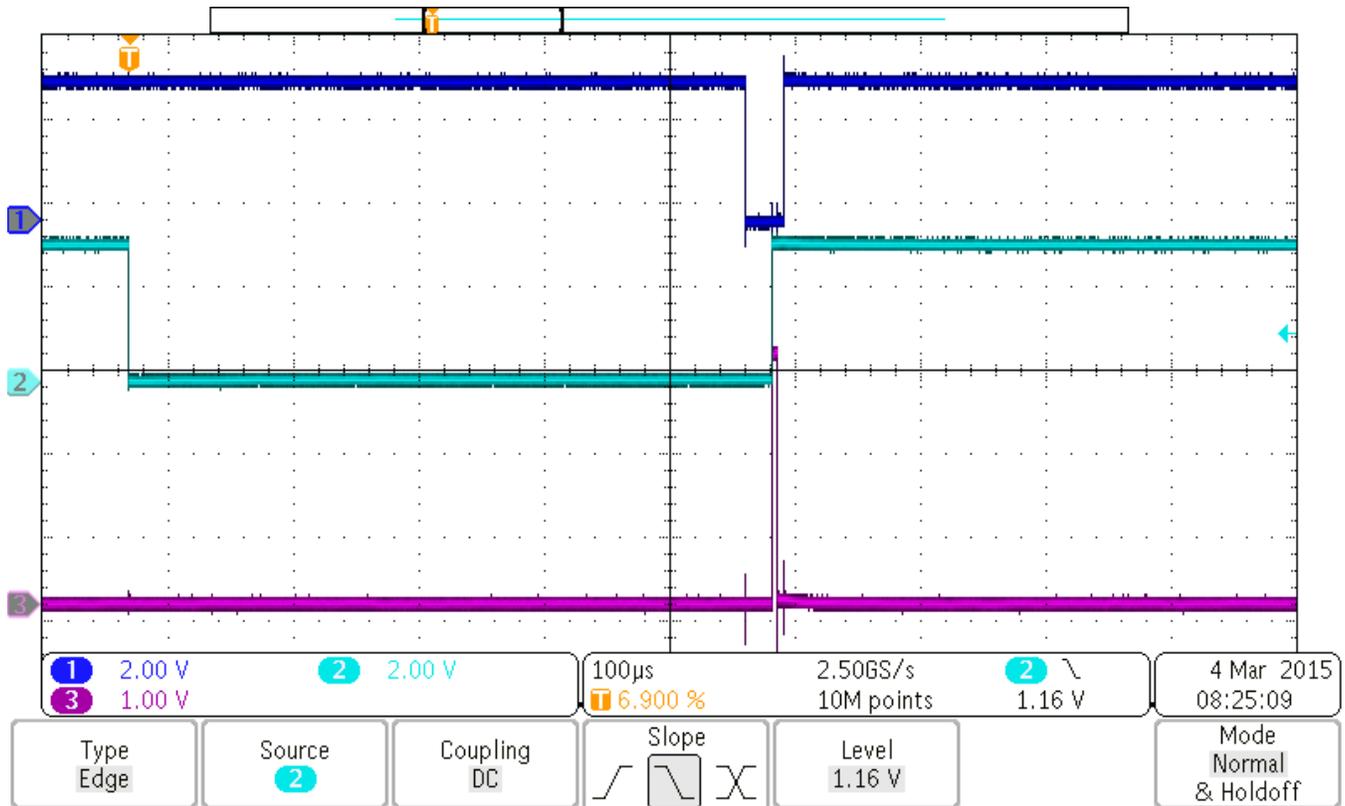
Figure 29. Complete Timing Diagram of Deep_Sleep Exit and Re-Entry

---

NOTE: Ch1: P4.6 (set to 'LOW' when exiting LPM4.5 and 'HIGH' just before entering LPM4.5)
Ch2: WAKE signal from TPL5100 (pin MOS_DRV)
CH3: P1.6 (DONE signal from MSP340 back to TPL5100)

Ch1 will go low after a few instructions of code. Using the cursors, the signal WAKE is low for 512 µs.

6.5 Current Consumption of System

This section gives an indication on eight boards of the current consumption of the system over temperature and voltage supply.

The information is displayed using boxplot diagram, using the following convention:

IQR: inner quartile range

The box represents the first and third quartiles, with the red line the median (second quartile)

The whiskers are at 1.5 IQR

Any data not within the whiskers are plotted as individual dots.
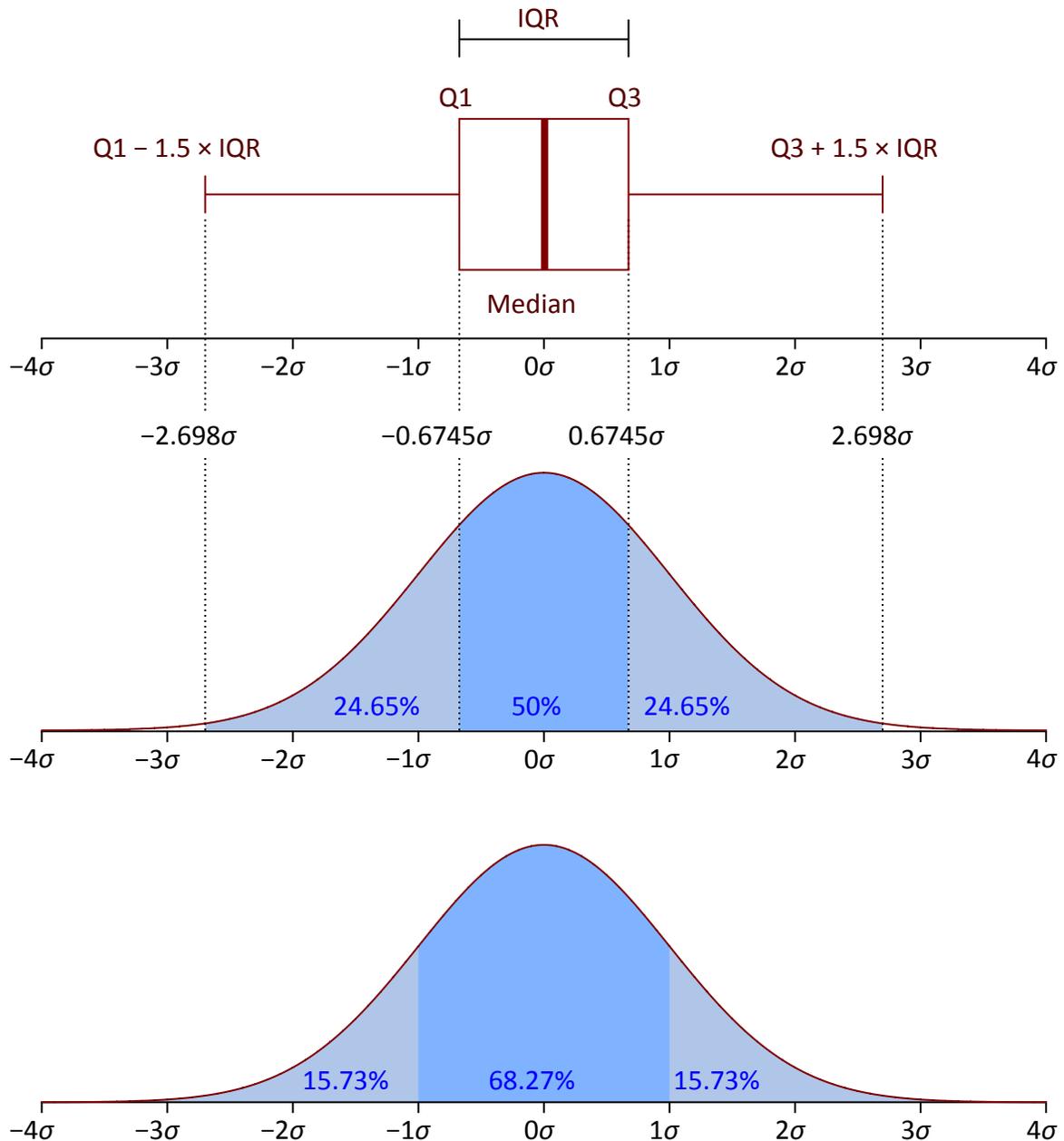
Figure 30. Visual Explanation of Whiskers in Relation to Statistical Distribution

6.5.1 At –40°C
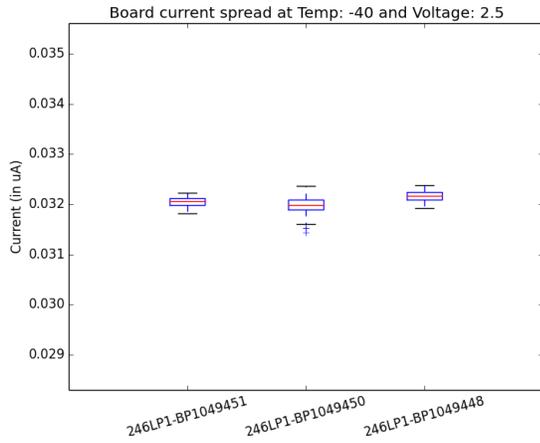
Figure 31. Board Current Spread at –40°C and 2.5 V
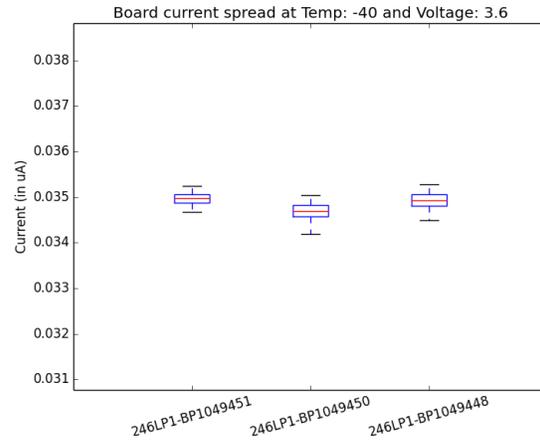
Figure 32. Board Current Spread at –40°C and 3.6 V

6.5.2 At 25°C
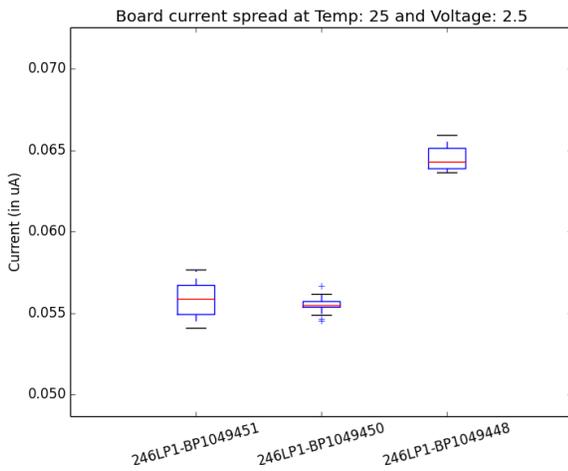
Figure 33. Board Current Spread at 25°C and 2.5 V
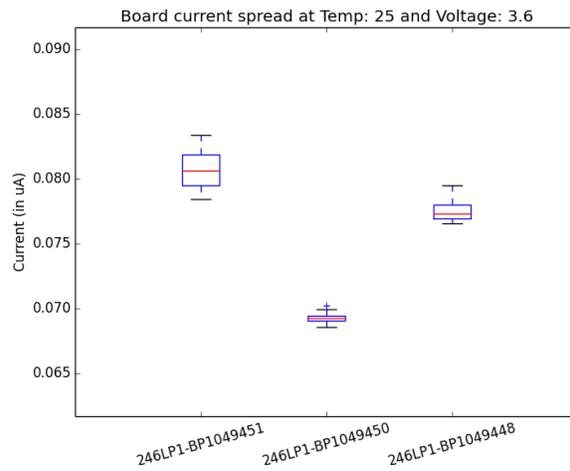
Figure 34. Board Current Spread at 25°C and 3.6 V

6.5.3   At 85°C
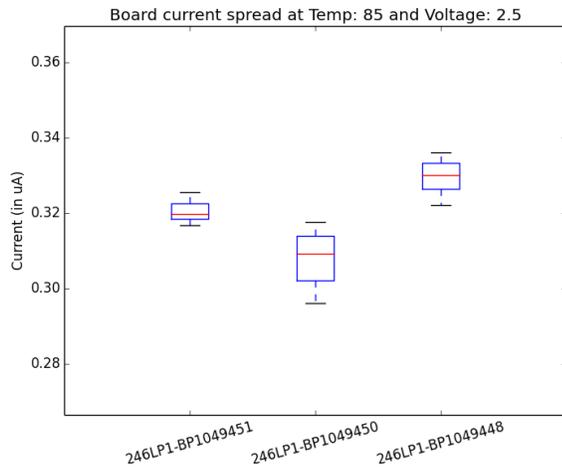
Figure 35. Board Current Spread at 85°C and 2.5 V
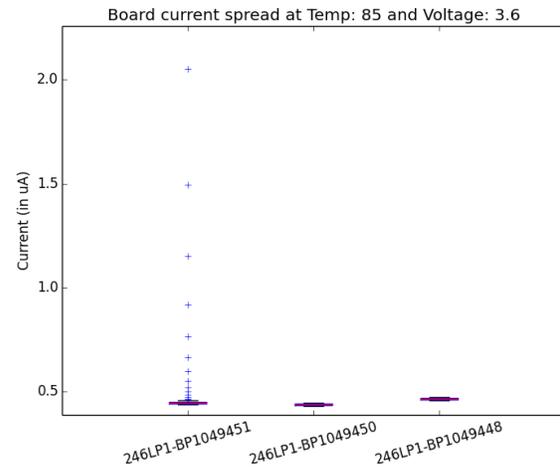
Figure 36. Board Current Spread at 85°C and 3.6 V

The high number of outlier on the board 246LP1-BP109451 is due to the initial characterization software not taking into account the current response to step voltage (see Section 6.1).

Because the average value was well inline with the other boards characterized, this data set was maintained.

6.5.4   Summary

From the above characterization, it is clear that as expected while the voltage influences the leakage, the dominant factor is temperature.

Assuming that the electronics for the GEHAM are not located on the pipe like the TEG, it is assumed that the ambient temperature can estimated to 25°C and hence the average power consumption of the GEHAM to be 70 nA.

6.6   Charging Detection Function

Figure 37 is a plot made at J14:on the jumper between J14:1 and J14:2.

NOTE: Because the probe used at a 10-MΩ impedance, the amplitude is 50% of the amplitude on the PCB (given that R3 is a 10-MΩ resistor).

From Figure 37, it is clear that the MCU can see the signal and can react accordingly.
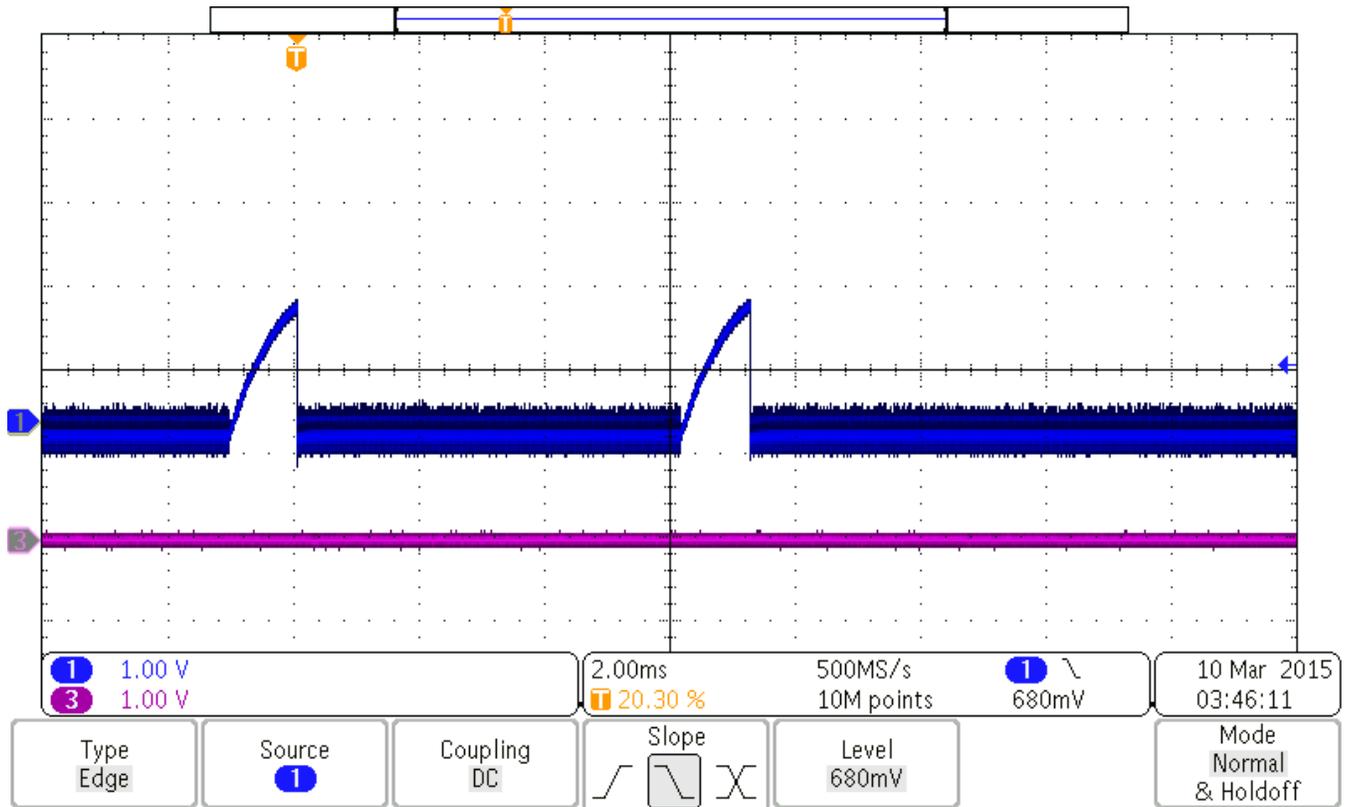
Figure 37. Snapshot of Charging Signal

6.7   Startup Voltage of Circuit

By monitoring the ChargeDetect signal and slowly increasing the V_{TEG} voltage, the startup voltage is measured at 75 mV.

7   Design Files

7.1   Schematics

To download the most recent schematics, see the design files at TIDA-00246.

7.2   Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00246.

7.3   Layer Plots

To download the layer plots, see the design files at TIDA-00246.

7.4   Altium Project

To download the Altium project files, see the design files at TIDA-00246.

7.5   Gerber Files

To download the Gerber files, see the design files at TIDA-00246.

8   Lexicon

Seebeck coefficient: The physical measure of the magnitude of the voltage induced by a temperature gradient.

Thermoelectric generator (TEG): The physical artifact made from the assembly of multiple pairs of p-type and n-type thermo-elements with the aim to provide power to a sub-system from an existing temperature gradient.

Technology readiness level (TRL): A scale used to estimate the maturity of a technology and its applicability for industrial projects. The scale starts at 1 with basic research and ends at 9 when being used in systems being mass produced.

9 References

1. ISA, Roy Freeland, *Practical Power Solutions for Wireless Sensing* ([PDF](#))

2. *Energy harvesting for wireless sensors, Synergistic analysis of thermoelectric devices, heat sinks and associated electronics for optimized energy harvesting systems*, Robin McCarty, II-VI Marlow White paper

3. IEEE, Hal Edwards, Jeff Debord, Toan Tran, Dave Freeman, and Ken Maggio, *Performance metrics for thermoelectric energy harvesting studied using a novel planar 65 nm silicon CMOS-based thermopile*, SENSORS, 2013 IEEE; 3–6 Nov. 2013 (http://ieeexplore.ieee.org/xpls/icp.jsp?arnumber=6688611)

4. Marlow Industries, Joshua Moczygemba, *Energy harvesting TEG Power Strap for Industrial, Chemical, Oil and Gas Applications* ([PDF](#))

5. Marlow Industries, Joshua Moczygemba, *Converting waste heat into electrical energy* ([PDF](#))

6. IEEE, Jim Bierschenk, *Optimized Thermoelectrics for Energy Harvesting Applications* ([PDF](#))

7. bq25505 and bq25570 Design Files ([SLUC484](#))

8. Texas Instruments, *User's Guide for bq25570 Battery Charger Evaluation Module for Energy Harvesting*, bq25570 User's Guide ([SLUUAA7](#))

9. Emerson Process Management, *SmartPower™ Solutions*, Quick Start Guide ([PDF](#))

10. Pepperl+Fuchs, *W-BAT-B2-Li Battery* ([PDF](#))

11. Endress+Hauser, *WirelessHART Adapter SWA70 Technical Information* ([PDF](#))

12. IEEE, J. Rodriguez, K. Remack, J. Gertas, L. Wang, C. Zhou, K. Boku, J. Rodriguez-Latorre, *Reliability of Ferroelectric Random Access memory embedded within 130nm CMOS*, Reliability Physics Symposium (IRPS), 2010 IEEE International, Vol. May 2010, pp.750–758 (http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=5488738)

13. WSEAS Transactions On Power Systems, *Energy comparison of MPPT techniques for PV Systems*, Roberto Faranda, Sonia Leva, Issue 6, Vol. 3, June 2008 ([PDF](#))

14. EU PVSEC, *A Study Of Dye Sensitized Solar Cells under Indoor and Low Level Outdoor Lighting: Comparison to Organic and Inorganic Thin Film Solar Cells and Methods to Address Maximum Power Point Tracking*, Nagarajan Sridhar1 and Dave Freeman, EU PVSEC Proceedings 2011, (http://www.eupvsec-proceedings.com/proceedings?paper=13959)

15. Texas Instruments, Michael Day, *Using power solutions to extend battery life in MSP430 applications*, Technical Brief ([SLYT356](#))

16. VDI The Association of German Engineers ([www.vdi.eu/2185](#))

17. *A Simulation Model for the Performance Evaluation of WirelessHART TDMA Protocol*, Osama Khader, Andreas Willig, and Adam Wolisz, Technical University Berlin, Telecommunication Networks Group, Berlin May 2011 ([PDF](#))

18. Keithley, *Low Level Measurements Handbook: Precision DC Current, Voltage, and Resistance Measuments*, 7th edition ([PDF](#))

19. Texas Instruments, *MSP430FR59xx Mixed-Signal Microcontrollers*, MSP430FR59xx Datasheet ([SLAS704](#))

10 About the Author

MATTHIEU CHEVRIER is a systems architect at Texas Instruments, where he is responsible for defining and developing reference design solutions for the industrial segment. Matthieu brings to this role his extensive experience in embedded system designs in both hardware (power management, mixed signal, and so on) and software (such as low level drivers, RTOS, and compilers). Matthieu earned his master of science in electrical engineering (MSEE) from Supélec, an Ivy League university in France. Matthieu holds patents from IPO, EPO, and USPTO.

IMPORTANT NOTICE FOR TI REFERENCE DESIGNS