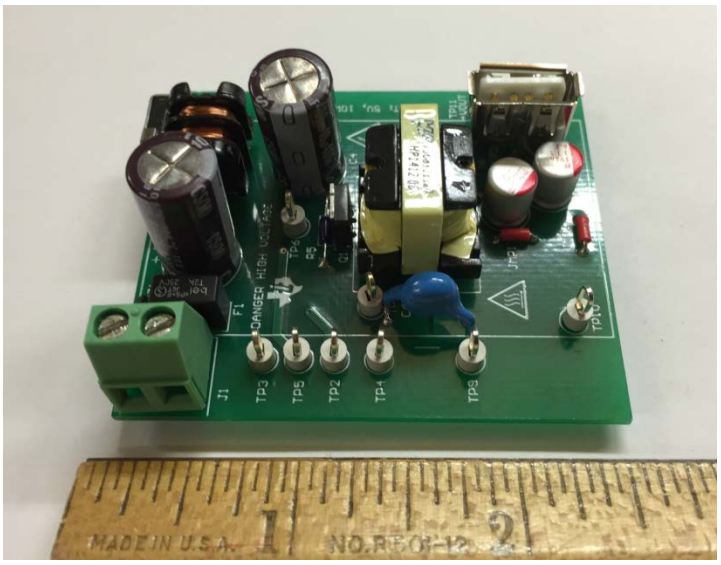
PMP9561 Rev. A Test Results

1. PHOTO OF THE PROTOTYPE:



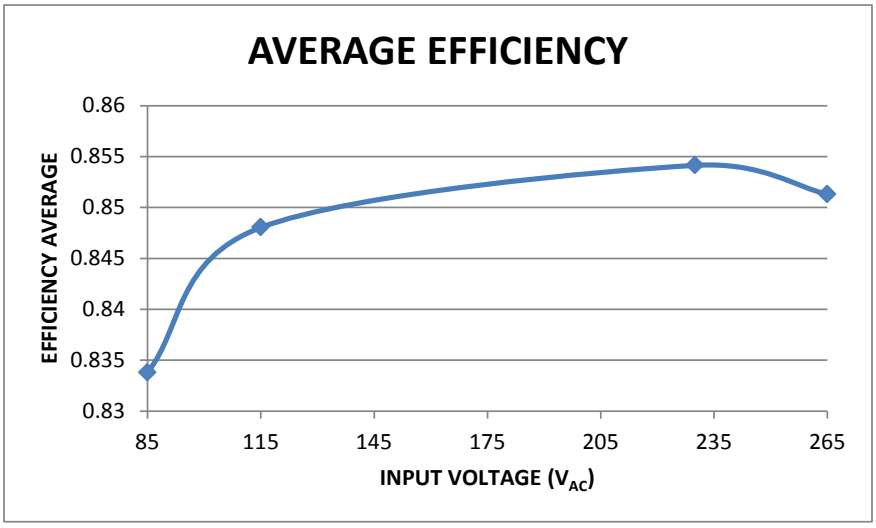
The PMP9561 is a 10-W off-line discontinuous mode (DCM) flyback converter that provides constant-voltage (CV) and constant-current (CC) output regulation without the use of an optical coupler. The controller uses primary side regulation (PSR) and detects a wake-up signal from the UCC24650 secondary-side voltage-droop monitor for improved transient response to large load steps. The UCC24610 is used to drive the 60V CSD18534Q5A synchronous rectifier and demonstrates the ENS function of the UCC24650 Wake-up monitor. This reference design shows how the UCC28730 can provide ultra-low standby power without sacrificing start-up time or output transient response with an internal 700-V start-up switch, dynamically controlled operating states, and a tailored modulation profile. The UCC28730 uses frequency modulation, peak primary current modulation, valley switching and valley skipping in its control algorithm in order to maximize efficiency over the entire operating range. The PMP9561 reference design exceeds Level VI and CoC Tier 2 specifications, effective 2016, for average efficiency, 10% load efficiency, and no-load stand-by power. **Note that this reference design is not an orderable device from TI, but shows the performance of a UCC28730/UCC24650 in a constant voltage/ constant current controller in a typical 10-W USB adapter application.**

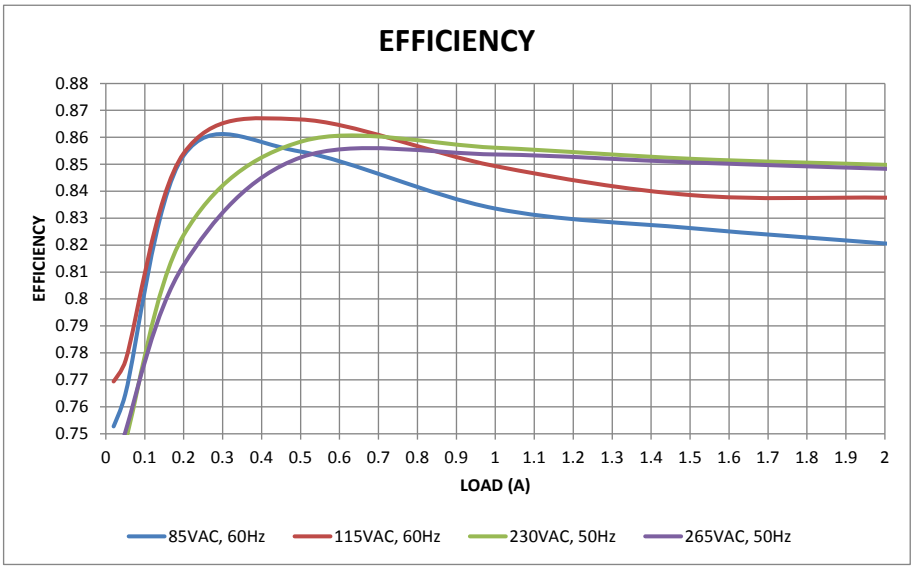
2. Electrical Performance Specifications

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNITS
Input Characteristics					
Voltage range, V_{IN}		85	115/230	265	V_{RMS}
Maximum input current	$V_{IN} = V_{INmin}$, $I_{OUT} = I_{OUTmax}$			0.250	A_{RMS}
Line frequency		47	60/50	63	Hz
No-load power consumption	$V_{INmin} \le V_{IN} \le V_{INmax}$, $I_{OUT} = 0A$			5	mW
Output Characteristics					
Output voltage, CV mode, V_{OUT}	$V_{INmin} \le V_{IN} \le V_{INmax}$, $0A \le I_{OUT} \le I_{OUTmax}$	4.75	5	5.25	V
Output load current, CV mode, I_{OUTmax}	$V_{INmin} \le V_{IN} \le V_{INmax}$	1.9	2.0	2.1	A
Output voltage regulation	Line Regulation: $V_{INmin} \le V_{IN} \le V_{INmax}$, $I_{OUT} = I_{OUTmax}$			5	%
	Load Regulation: $0A \le I_{OUT} \le I_{OUTmax}$			5	%
Output voltage ripple	$V_{INmin} \le V_{IN} \le V_{INmax}$, $0A \le I_{OUT} \le I_{OUTmax}$			80	mVpp
Output over current, I_{OCC}	$V_{INmin} \le V_{IN} \le V_{INmax}$			2.15	A
Minimum output voltage, CC mode	$V_{INmin} \le V_{IN} \le V_{INmax}$, $I_{OUT} = I_{OCC}$		1.4	2	V
Brown-out protection	$I_{OUT} = I_{OUTmax}$		62		V_{RMS}
	$I_{OUT} = 10\%\ I_{OUTmax}$		34		
Systems Characteristics					
Switching frequency, f_{SW}		0.05		50	kHz
Average efficiency	25%, 50%, 75%, 100% load average at nominal input voltages	84	85		%
Operating temperature			25		ºC

3. Efficiency

V_{IN} V_{RMS}	P_{IN} W	V_{OUT} V	I_{OUT} A	P_{OUT}	EFFFICIENCY
85V, 60Hz	1.1736	5.007	0.200	10%	0.8533
	2.909	4.993	0.498	25%	0.8547
	5.963	4.986	0.997	50%	0.8336
	9.1	4.996	1.505	75%	0.8263
	12.319	5.021	2.013	100%	0.8205
115V, 60Hz	1.1725	5.007	0.2	10%	0.8541
	2.872	4.998	0.498	25%	0.8666
	5.862	4.989	0.998	50%	0.8494
	8.959	4.995	1.504	75%	0.8385
	12.043	5.016	2.011	100%	0.8376
230V, 50Hz	1.2161	5.009	0.200	10%	0.8238
	2.96	5.013	0.507	25%	0.8586
	5.839	4.999	1	50%	0.8561
	8.838	5	1.506	75%	0.8520
	11.848	5.019	2.006	100%	0.8498
265V, 50Hz	1.2342	5.015	0.200	10%	0.8127
	2.954	5.027	0.501	25%	0.8526
	5.869	5.005	1.001	50%	0.8536
	8.865	5.004	1.507	75%	0.8506
	11.884	5.023	2.007	100%	0.8483

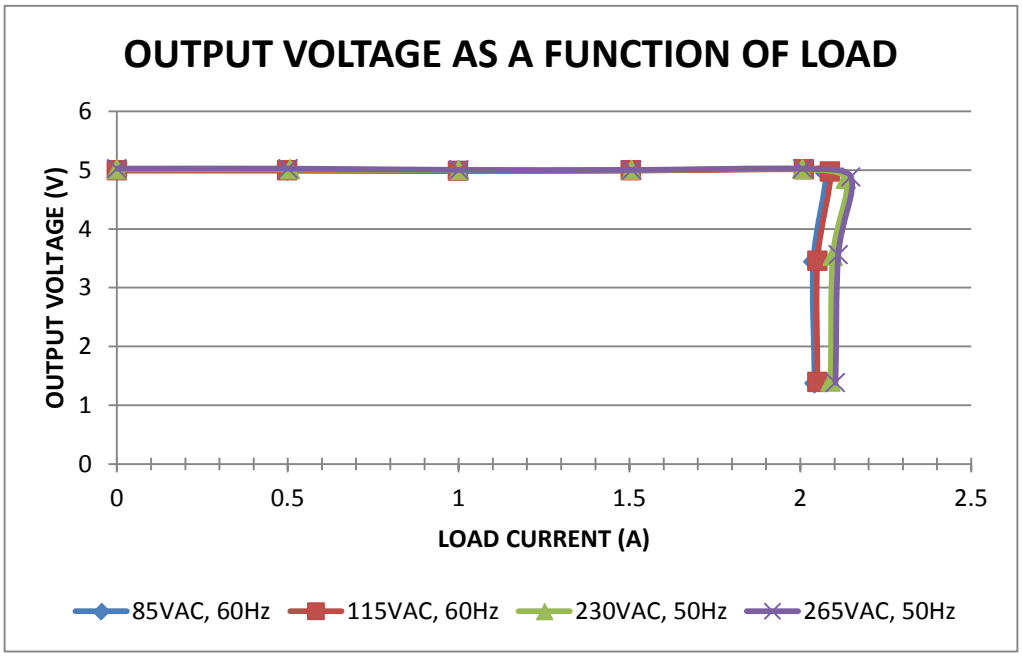




4. No-Load Power Consumption

INPUT VOLTAGE	INPUT POWER
85 VRMS, 60Hz	2.401 mW
115 VRMS, 60Hz	2.565 mW
230 VRMS, 50Hz	3.119 mW
265 VRMS, 50Hz	3.408 mW

5. Output Voltage vs Output Current



The converter is in constant-voltage operating mode from 0 A load up to approximately 2.05 A. Once reaching this output over-current threshold, the converter transitions into constant-current mode where the load current remains constant until the output voltge falls below 2 V, at which point the converter enters shutdown/restart. If the load demand is decreased to the constant current operating region, the converter will automatically re-start.

6. Transient Response and WAKE Function

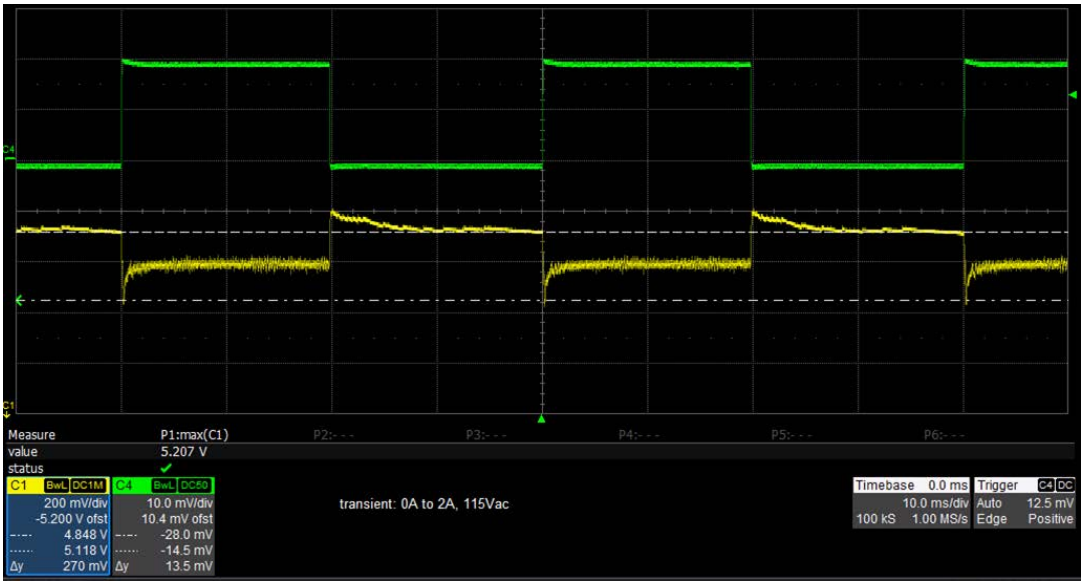


Figure 1. Load transient from No-Load to Full-Load

The transient response shown was taken with a 115 VAC, 60 Hz input voltage and a load transition from 0 A to full load. Channel 4 is the load current on a scale of 1 A per division, channel 1 is the output voltage on a scale of 200 mV per division, offset from the center line by -5.20 V. The cursors show the undershoot from the regulated output voltage, under full load transient conditions. Output voltage undershoot may vary dependent upon the specific time the transient occurs during the switching cycle.

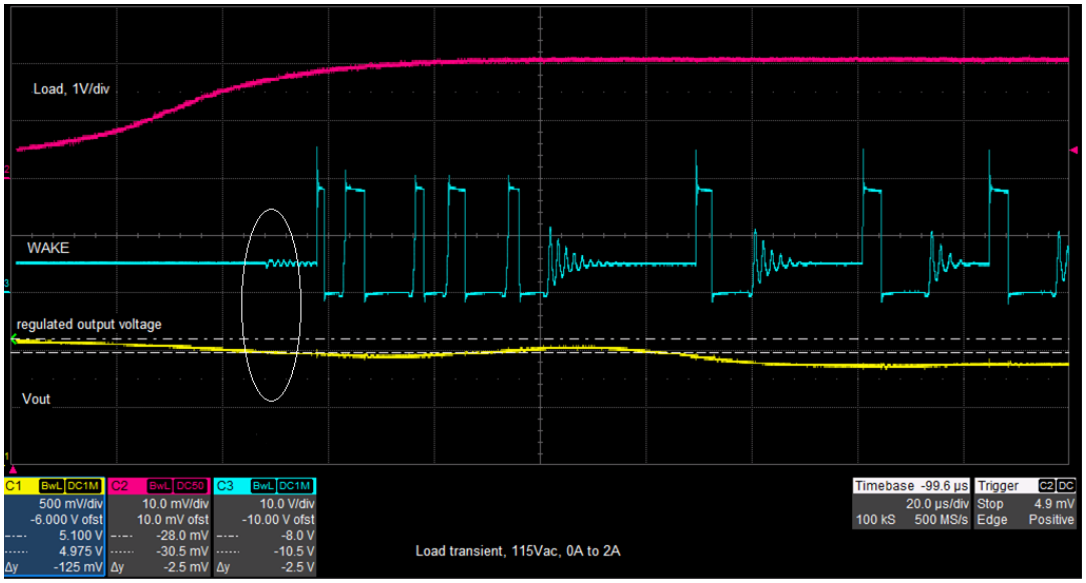


Figure 2. WAKE Signal During Load Transient

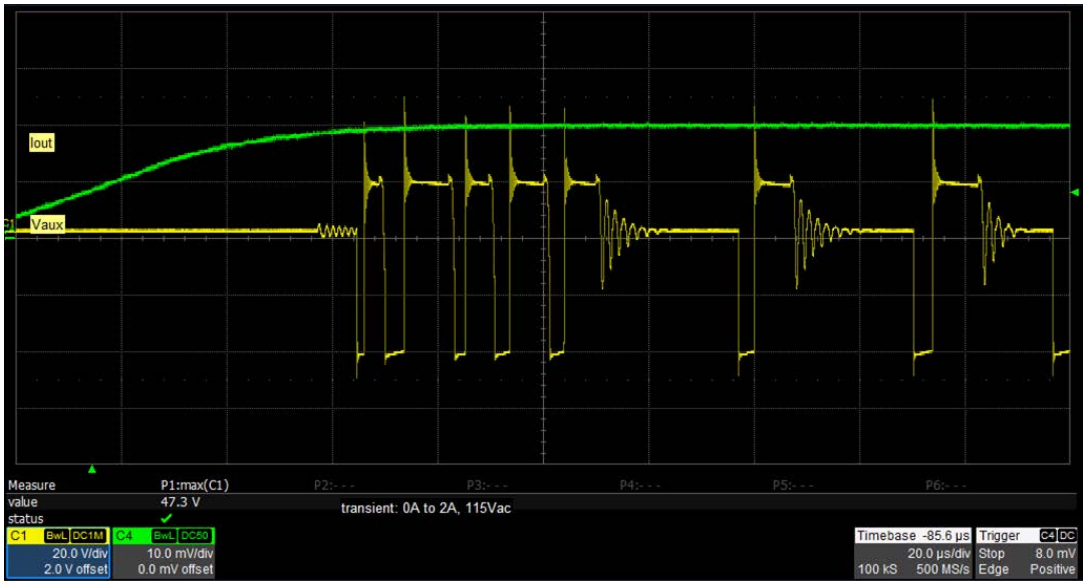


Figure 3. WAKE Signal Transmitted to the AUX Winding

Figure 2 shows the WAKE signal from the UCC24650 Wake-Up Monitor activating when the output voltage falls below approximately 3% of its regulated value. Figure 3 shows the wake-up alert signal transmitted to the PSR controller on the AUX winding.

7. Output Ripple

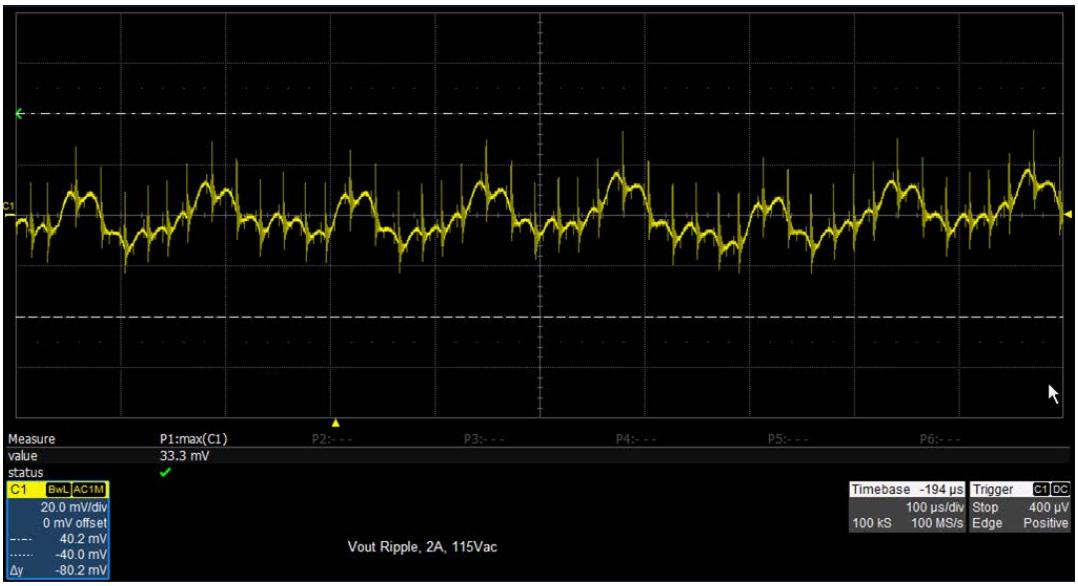


Figure 4. Output Ripple at Full-Load, 115Vin

Figure 4 shows the output voltage ripple taken at full load with an input voltage of 115 VAC, 60 Hz and the waveform is AC coupled, with 20 MHz bandwidth limit. The cursor indicates the maximum peak to peak limit of 80 mV permitted for the design. The ripple pattern seen is characteristic of the EMI dithering method used by the UCC28730 controller.

8. Turn On Waveform

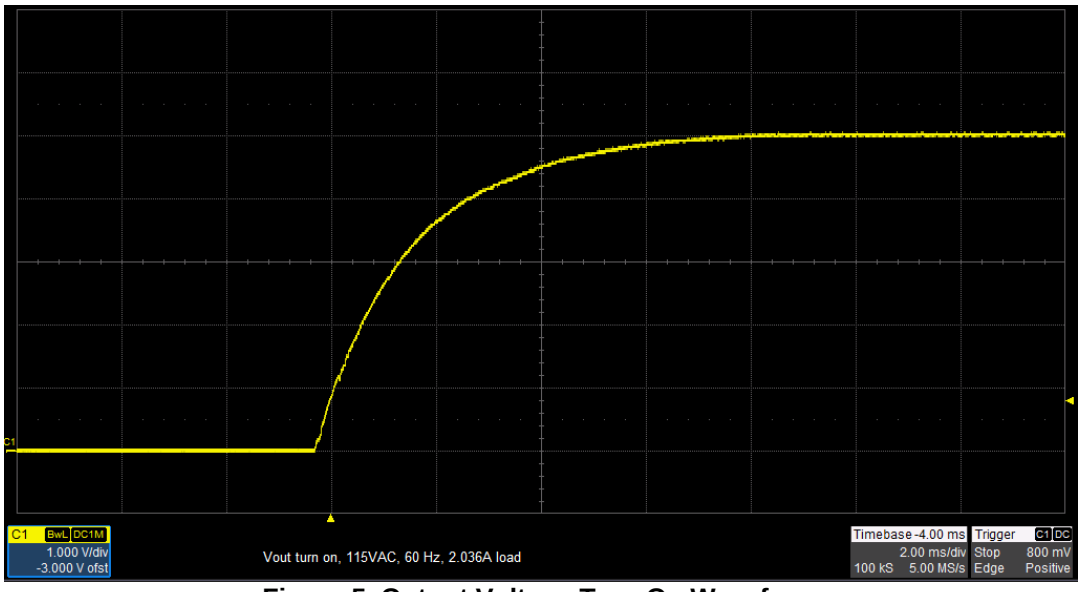


Figure 5. Output Voltage Turn On Waveform

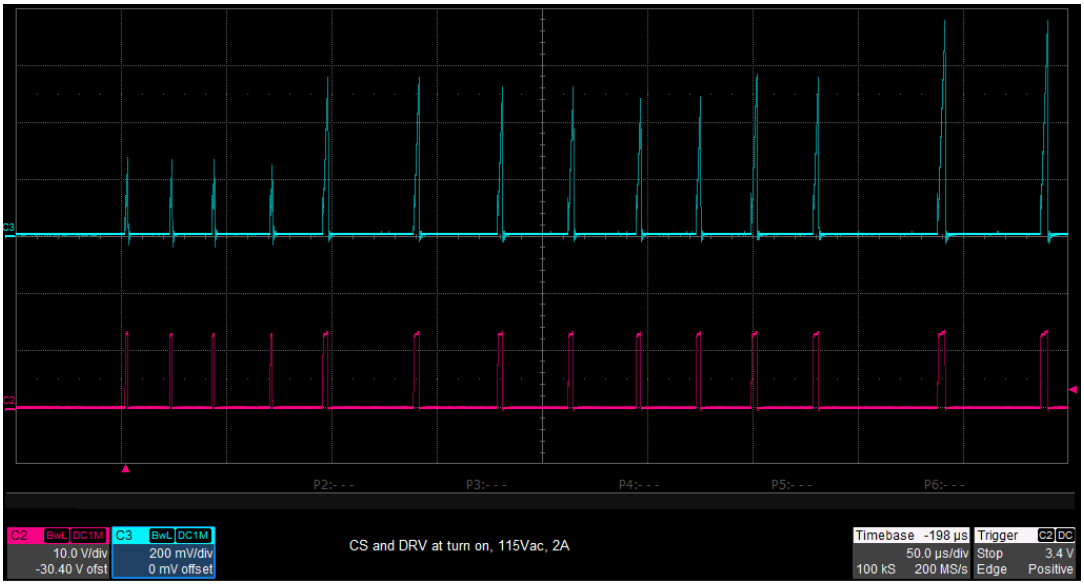


Figure 6. CS and DRV at Turn On

Figure 6 shows how the UCC28730 limits the first four switching-cycle current peaks to IPP(min) in order to monitor for any initial input or output faults with limited power delivery. After these initial four pulses, the controller will limit the amplitude of the peak primary current to approximately 0.67 x $I_{PP(max)}$. Modifications are also made to D_{MAGCC}, increasing it from 0.432 to 0.650. These modifications during startup allow high frequency charge-up of the output capacitor to avoid audible noise. Once the VS signal is greater than 1.36 V (approximately 1.45 V on the output), D_{MAGCC} is restored to its normal value and the peak primary current resumes at $I_{PP(max)}$.

9. Switching Waveform

Figure 7. Primary Side Switching Waveform

The typical switching waveform can be seen in Figure 7. Channel 1 shows the MOSFET drain to source voltage at 100 V per division, channel 2 shows the AUX winding at 50 V per division, channel 3 is the CS waveform at 500 mV per division, and channel 4 shows the gate drive at 10 V per division. The scan was taken at 2 A load, 115 V_{AC}, 60 Hz input voltage. At this operating point, the switching frequency is dithering between 48 kHz and 40 kHz due to valley skipping.

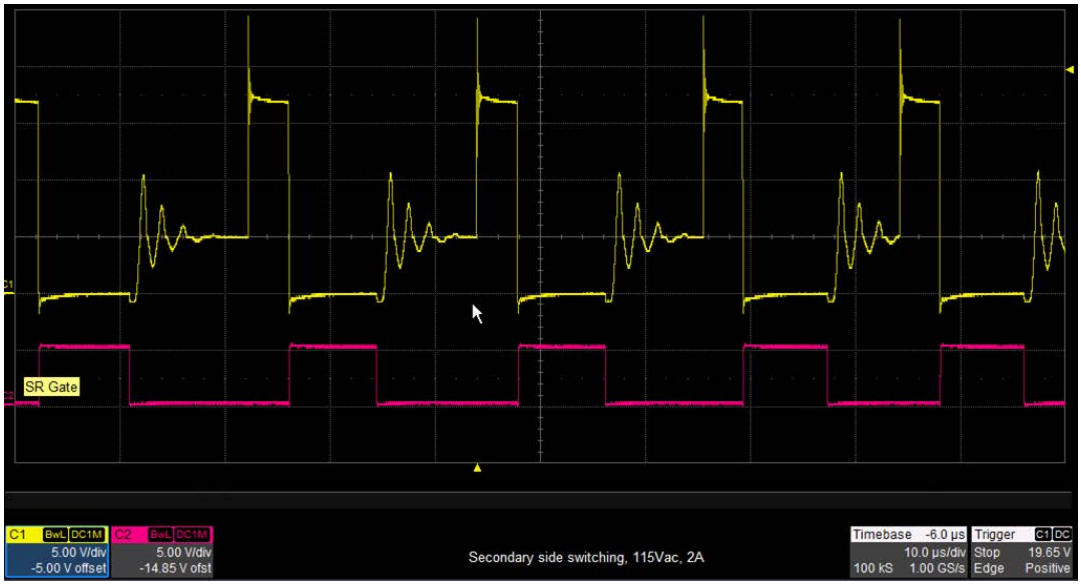


Figure 8. Secondary Side Switching Waveform

Figure 8 shows the switching waveforms on the secondary side, channel 1 is the SW node and channel 2 shows the UCC24610 gate drive for the secondary side synchronous rectifier.

10. ENS

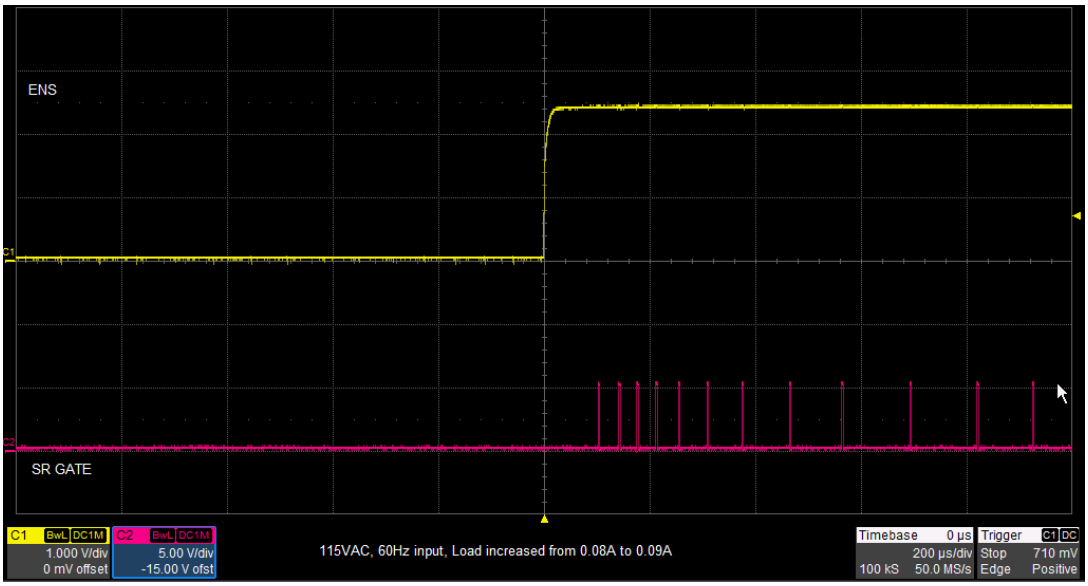


Figure 9. ENS and SR Gate as Load Decreases

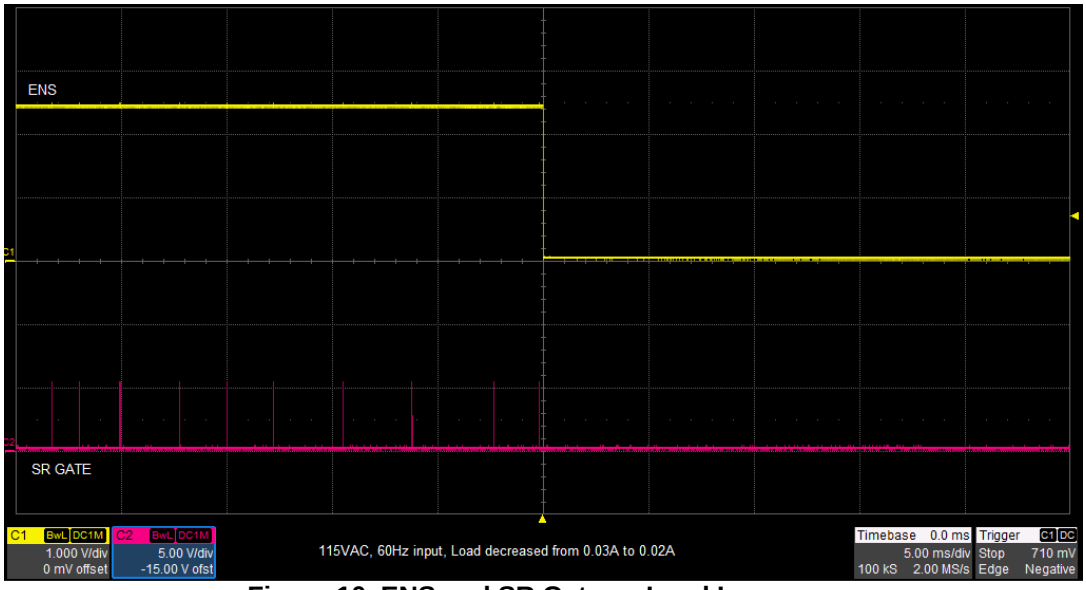
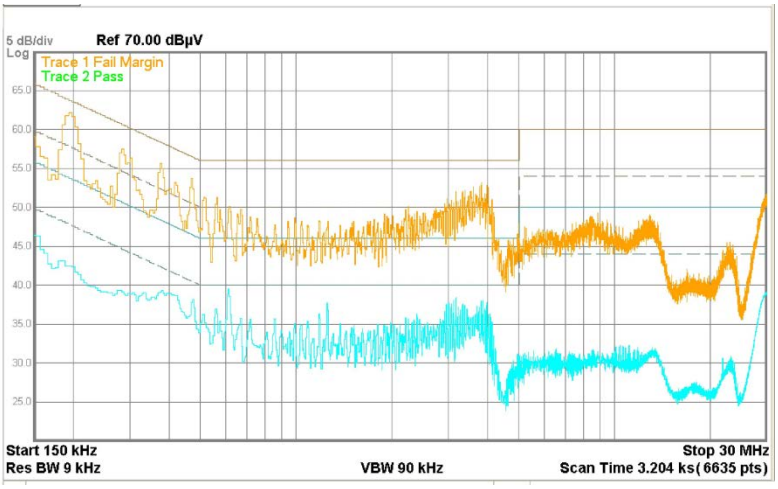


Figure 10. ENS and SR Gate as Load Increases

The ENS open-drain MOSFET output of the UCC24650 Wake-Up Monitor will disable the UCC24610 Synchronous Rectifier Driver when the load decreases below 0.03 A, as shown in Figure 9. The ENS re-enables the UCC24610 when the load increases above 0.09 A. as shown in Figure 10. Controlling the secondary-side circuitduring no-load and light-load conditions helps to reduce stand-by and light-load power loss.

11. EMI

Note that this reference design does pass EMI but fails margin. It is recommended that the transformer be redesigned with a more appropriately placed shield winding for better EMI performance.



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