TI Designs

700–2700-MHz Dual-Channel Receiver With 16-Bit ADC and 100 MHz of IF Bandwidth

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TI Designs provide the foundation that you need including methodology, testing, and design files to quickly evaluate and customize the system. TI Designs help *you* accelerate your time to market.

Design Resources

TIDA-00360	Tool Folder Containing Design Files
TSW16DX370EVM	Product Folder
TRF37B32	Product Folder
LMH6521	Product Folder
ADC16DX370	Product Folder
LMK04828	Product Folder
LMX2581	Product Folder

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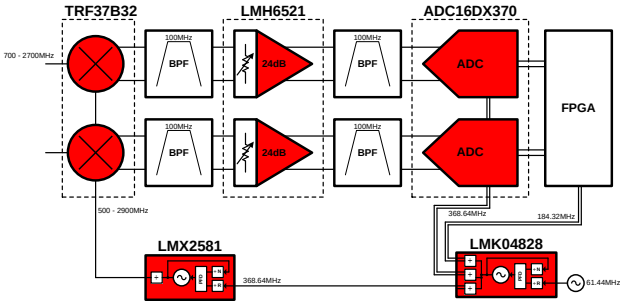
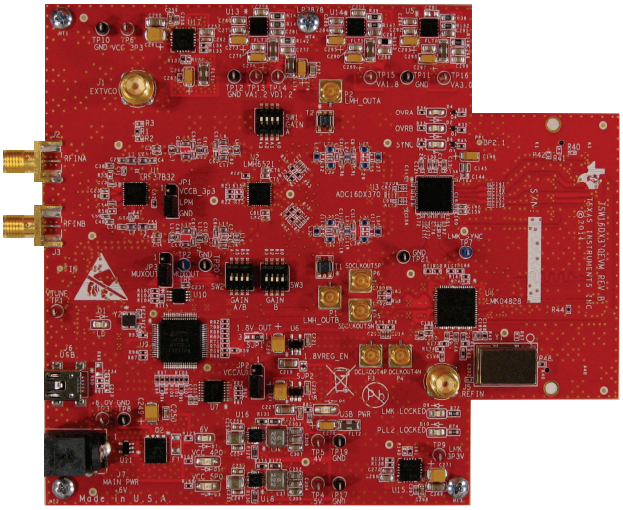
Design Features

- Implements a RF Super-Heterodyne Receiver Subsystem with 700–2700-MHz Input Range, Wide 100-MHz IF Bandwidth and 16-Bit ADC
- Evaluate this Reference Design Effortlessly With Supported Data Capture and Analysis Tools
- This Reference Design is Tested and Includes an Evaluation Module (EVM), Configuration Software, and User's Guide

Featured Applications

- Accelerate the Design Time of a Wireless Communications, Software-Defined Radio, Military, or Test and Measurement Application With a Proven IF Signal Chain





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1 Introduction

The increasing demand on wireless networks to provide faster data links to customers has driven transceiver hardware to increasingly demanding performance with enough bandwidth to support the largest standardized multi-carrier frequency bands (with band aggregation in some cases) and enough receiver sensitivity and dynamic range to function in the presence of the strong blocking signals common in busy environments.

Receivers in these difficult applications have pushed beyond the 75-MHz node and are on to 100-MHz nodes and beyond. The large bandwidth demands frequency-flexible mixers, high sampling rates, and good distortion performance through the whole signal chain up to higher intermediate frequencies (IF). Increased data rate also requires a standard serialized data interface to minimize the data bus real estate.

This TI Design describes a RF receiver subsystem reference design (TSW16DX370EVM) including a down-converting mixer, digitally-controlled variable gain amplifier (DVGA), high speed pipelined analog-to-digital converter (ADC), Local Oscillator (LO) RF synthesizer, and jitter-cleaning clock generator. The dual-signal path subsystem also connects to a field programmable gate array (FPGA) across a JESD204B standard interface. The frequency plan of the design accommodates a wide RF input range from 700–2700-MHz and more than 100-MHz of bandwidth with an intermediate frequency of 276-MHz. Figure 1 shows the block diagram.

2 Block Diagram

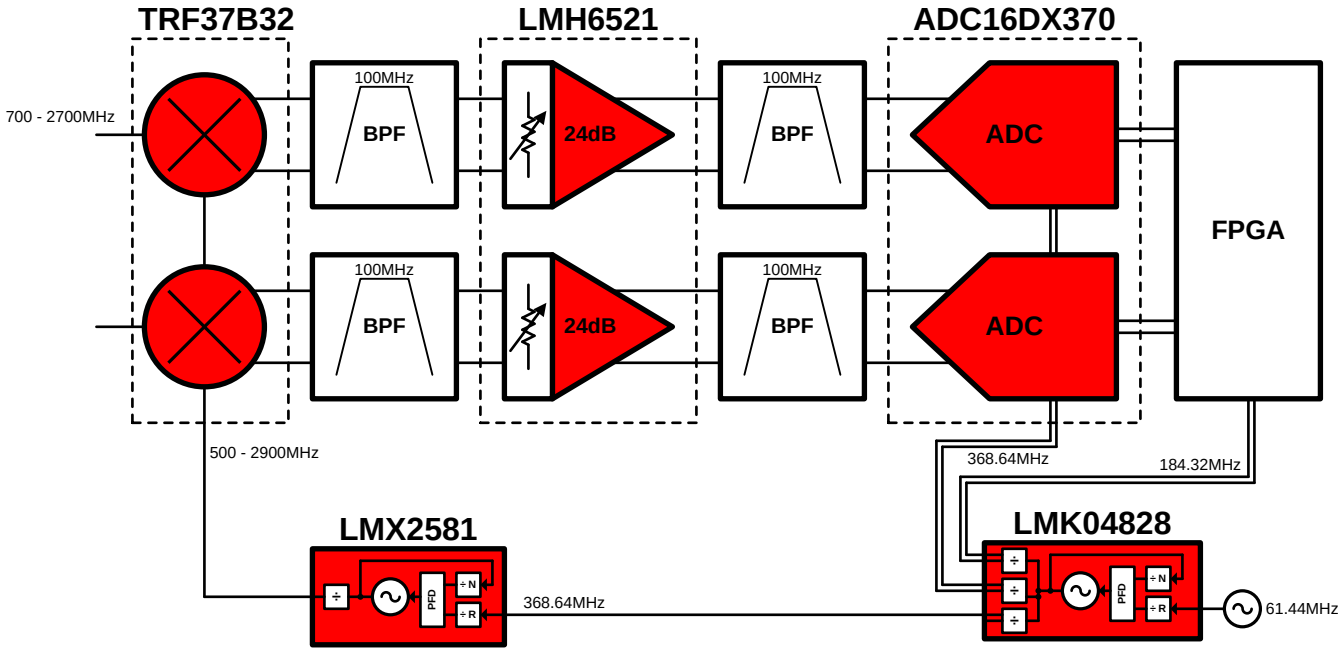

Figure 1. TSW16DX370EVM Block Diagram

3 Block Descriptions

The TRF37B32 is a dual-channel, down convert receive mixer. It provides high-linearity over wide RF and IF bandwidths while also consuming low power. The device covers an extremely wide frequency band and can operate with either low side injection (LSI) or high side injection (HSI). The device consists of a passive mixer core buffered by an LO amplifier and a high-linearity IF amplifier. There is an on-chip LDO to regulate VCC to the voltages required for the small-geometry SiGe BiCMOS components. The single-ended RF and LO inputs each have a wideband internal balun. Table 1 shows the performance metrics for this device.

Table 1. TRF37B32 Device Performance

BLOCK	FEATURE	VALUE	CONDITIONS
Down-conversion mixer (TRF37B32)	Gain	10 dB	RF Input = 1800 MHz
	NF	9.5 dB	
	IIP3	34 dBm	
	P1dB	10.5 dB	
	RF input frequency range	700–2700 MHz	
	LO input frequency range	500–2900 MHz	
	IF output frequency range	30–600 MHz	
	Input and output impedance	50 Ω and 200 Ω	

The LMH6521 is a dual, digitally-controlled variable gain amplifier (DVGA) designed for narrowband or wideband, intermediate-frequency sampling applications. The LMH6521 is optimized for accurate 0.5-dB gain steps with exceptional gain and phase matching between channels combined with low distortion products. The gain matching error is less than ±0.05 dB and the phase matching error is less than ±0.5 degrees over the entire attenuation range. The LMH6521 is ideal for driving ADC converters where high linearity is necessary. Table 2 shows the performance metrics for this device.

Table 2. LMH6521 Device Performance

BLOCK	FEATURE	VALUE	CONDITIONS
DVGA (LMH6521)	Max voltage gain	24 dB	
	Min voltage gain	–7.5 dB	
	Gain step	0.5 dB	
	NF	7.3 dB	Attenuation = 0 dB 200-Ω source
	OIP3	43 dBm	Input frequency = 276 MHz Input power = 4 dBm/tone Attenuation = 16 dB
	P1dB	17 dBm	
	Input and output impedance	200 Ω and 20 Ω	Low impedance output

The ADC16DX370 device is a monolithic, dual-channel, high performance ADC converter capable of converting analog input signals into 16-bit digital words with a sampling rate of 370-million samples per second (MSPS). This converter uses a differential pipelined architecture with integrated input buffer to provide excellent dynamic performance while maintaining low power consumption. The output digital data is provided through a JESD204B subclass 1 interface at up to 7.4 Gb/s. Table 3 shows the performance metrics for this device.

Table 3. ADC16DX370 Device Performance

BLOCK	FEATURE	VALUE	CONDITIONS
ADC (ADC16DX370)	Sampling rate	368.64 MSPS	
	Input BW	> 800 MHz	
	Noise spectral density	–152.7 dBFS/Hz	Small signal
		–151.7 dBFS/Hz	Input = –3 dBFS, 325 MHz
	SFDR	–85 dBFS	Input = –3 dBFS, 325 MHz
	IMD3	–92 dBc	Input = –10 dBFS/tone, 145/155 MHz
	Input impedance	100 Ω	Includes external 200-Ω termination
	Output data lane rate	7.4 Gb/s	One lane per channel

The LMK04828 is a dual phase-locked loop (PLL) clock conditioner, multiplier, and distributer with JEDEC JESD204B support. The 14 clock outputs can be configured to drive seven JESD204B converters or other logic devices using device and SYSREF clocks. The high phase noise performance combined with features like the ability to trade off between power or performance, dual VCOs, dynamic digital delay, holdover, and glitch-less analog delay make the LMK04828 ideal for providing flexible high performance clocking trees. Table 4 shows the performance metrics for this device.

Table 4. LMK04828 Device Performance

BLOCK	FEATURE	VALUE	CONDITIONS
System clock PLL (LMK04828)	Input reference frequency	61.44 MHz	
	Clock output phase noise		LVPECL16, 240 Ω, VCO0 Freq = 245.76 MHz (example) Offset:
		–124.3 dBc/Hz	1 kHz
		–134.7 dBc/Hz	10 kHz
		–136.5 dBc/Hz	100 kHz
		–148.4 dBc/Hz	1 MHz
		–160.8 dBc/Hz	10 MHz
	Total jitter, ADC sampling clock	93 fs	LVPECL16, BW = 12 kHz to 20 MHz

The LMX2581 is a low noise wideband frequency synthesizer that integrates a delta-sigma fractional N PLL, multiple core VCO, programmable output divider, and two different output buffers. The VCO frequency range is from 1880 through 3760 MHz and can be sent directly to the output buffers or divided down by even values from 2 to 38. Each buffer is capable of output power from –3- to 12-dBm at 2700 MHz. Integrated LDOs are used for superior noise immunity and consistent performance. Table 5 shows the performance metrics for this device.

Table 5. LMX2581 Device Performance

BLOCK	FEATURE	VALUE	CONDITIONS
Fractional-N synthesizer (LMX2581)	Input reference frequency	368.64 MHz	
	Internal VCO phase noise		Freq = 2.7 GHz
		–81.7 dBc/Hz	10 kHz
		–112.2 dBc/Hz	100 kHz
		–136.0 dBc/Hz	1 MHz
		–153.1 dBc/Hz	10 MHz

The two IF Bandpass Filters are 10-pole, maximally flat designs with a standard LC architecture. Both filters target a –1-dB, 100-MHz bandwidth centered at 276 MHz. The first filter in the signal path is designed for a 200-Ω source and load, whereas the second filter is designed for 100 Ω. The filter footprint is designed to be compact and flexible to support custom filter designs. Table 6 shows the performance metrics for these filters.

Table 6. IF Bandpass Filter Performance

BLOCK	FEATURE	VALUE	CONDITIONS
IF bandpass filter	Bandwidth	100 MHz	
	Passband flatness	1 dB	
	Center frequency	276 MHz	
	Stopband attenuation	< –22 dBc	Input = 450 MHz

4 Frequency Plan

The sub-system is synchronous to a 61.44-MHz crystal oscillator module reference clock provided on the board. From the reference clock, the LMK04828 generates the 368.64-MHz ADC sampling clock, 184.32-MHz reference for the FPGA, 11.52-MHz SYSREF clock for the FPGA, and 368.64-MHz reference for the LMX2581. The LMX2581 then uses the reference to generate a flexible LO frequency from 500 to 2600 MHz.

Table 7. Frequency Plan Summary

REFERENCE	FREQUENCY	NOTES
System reference	61.44 MHz	Onboard XO
ADC conversion clock frequency	368.64 MHz	Equal to sampling rate
FPGA SERDES reference clock	184.32 MHz	Must be ≤ 250 MHz
FPGA SYSREF clock	11.52 MHz	Equal to 368.64 / 32
LO reference clock	368.64 MHz	Equal to ADC sampling rate to prevent system spurs
LO frequency	500–3800 MHz	Generated by Fractional-N synthesizer

The 368.64-MSPS ADC sampling clock provides 184.32 MHz of un-aliased bandwidth, which can support up to an approximate 130 MHz of signal bandwidth depending on the desired system performance and IF filter complexity. This design utilizes LC bandpass filters (BPF) centered in the middle of the second Nyquist zone at 276 MHz that have a 100-MHz, –1-dB bandwidth. Figure 2 shows an example where the receiver is mixing the standard cellular 3GPP band 40 from 2300–2400 MHz down to the intermediate frequency with an LO frequency of 2073.55 MHz.

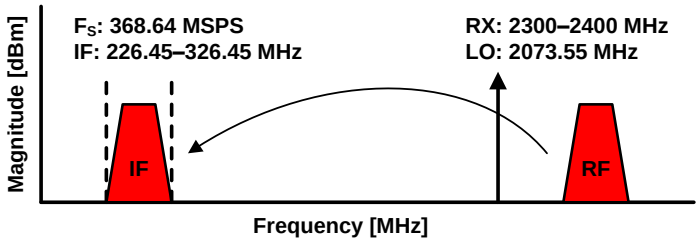

Figure 2. Frequency Plan for 3GPP Band 40

This centering of the IF frequency in the second Nyquist zone allows simple IF to complex digital baseband conversion. The signal band occupies most of the Nyquist zone, so frequency planning around harmonics is not an option. The super-heterodyne architecture does allow for the filtering of harmonics and IMD2 products created by the device prior to the ADC. This filtering is in contrast to a direct conversion (zero IF) receiver, which cannot filter out harmonic content before sampling.

5 Measured Signal Path Performance

5.1 Bench Measurement Setup

Figure 3 shows how the reference design was evaluated in the bench setup. A low-noise spectrum analyzer is used to generate a 1-tone or 2-tone signal (using a second generator and power combiner in the latter case). A signal path filter is optional for signal generators with good noise performance because the reference design achieves enough anti-aliasing protection to eliminate signal generator harmonics. A small signal path attenuator is used to improve the gain flatness across the frequency when connecting the input cable transmission line to the input of the TRF37B32 device. No additional clock sources are required for testing because the EVM has an onboard reference clock.

The TSW16DX370EVM connects to the TSW14J56EVM data capture platform and uploads data to a computer that is running the High Speed Data Converter Pro Software (1), which analyzes the data.

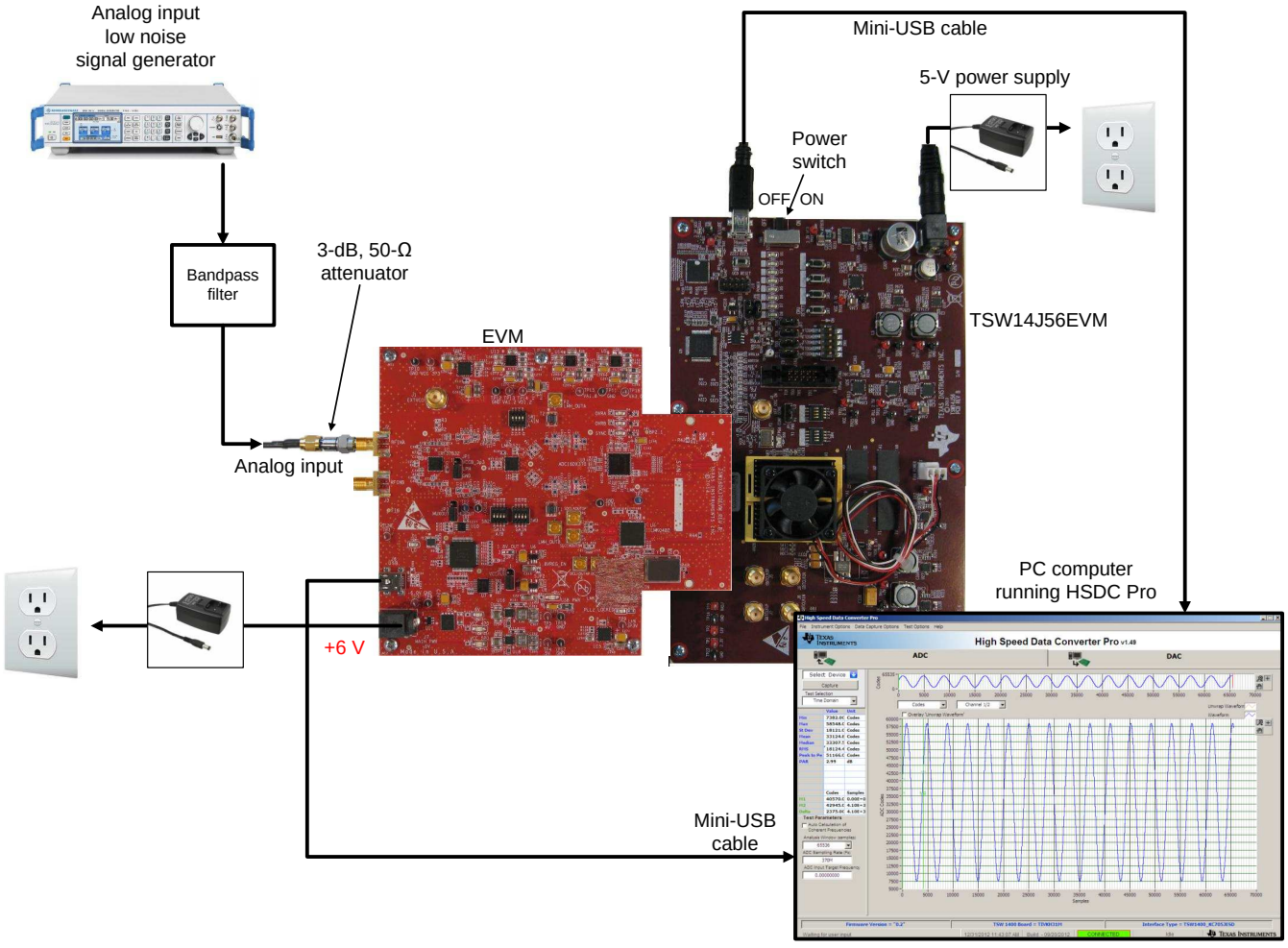

Figure 3. Bench Evaluation Setup

5.2 Noise and Distortion

The noise and distortion performance closely matches the expected signal path performance. Table 8 shows the summary of measured performance.

Table 8. System Performance Summary

PARAMETER	CONDITION	RESULT	NOTES
Gain	DVGA att. 0 dB	28.7 dB	
	DVGA att. 24 dB	4.7 dB	
OIP3	Fin = 1710/1700, –9 dBFS/tone, DVGA att. 0 dB	36.1 dBm	IMD = –79 dBc, IIP3 = 7.4 dBm
	Fin = 1710/1700, –9 dBFS/tone, DVGA att. 24 dB	30 dBm	IMD = –66.7 dBc, IIP3 approx. 25.3 dBm
	Fin = 1790/1800, –9 dBFS/tone, DVGA att. 0 dB	35.2 dBm	IMD = –77.4 dBc, IIP3 approx. 5.5 dBm
	Fin = 1790/1800, –9 dBFS/tone, DVGA att. 24 dB	27.3 dBm	IMD = –61.4 dBc, IIP3 approx. 22.6 dBm
NF	DVGA att. 0 dB	11 dB	
	DVGA att. 24 dB	25.9 dB	
Phase noise	100 kHz	–114.4 dBc/Hz	DVGA att. 24 dB. frequencies above 1 MHz influenced significantly by broadband noise of ADC and LMH.
	200 kHz	–121.4 dBc/Hz	
	500 kHz	–128.9 dBc/Hz	
	1 MHz	–136.4 dBc/Hz	
	2 MHz	–140.4 dBc/Hz	
	5 MHz	–143.4 dBc/Hz	
	10 MHz	–144.4 dBc/Hz	

5.3 Selectivity

The selectivity of the sub-system is set by two 10-pole LC bandpass filters, one filter following the mixer and the other filter following the DVGA while acting as the noise anti-aliasing filter. The first filter is designed for a 200-Ω source and load. The second filter is designed for a 100-Ω source and load, too; however, both filters are designed for a similar frequency response. Figure 4 shows the measured composite total sensitivity of both filters.

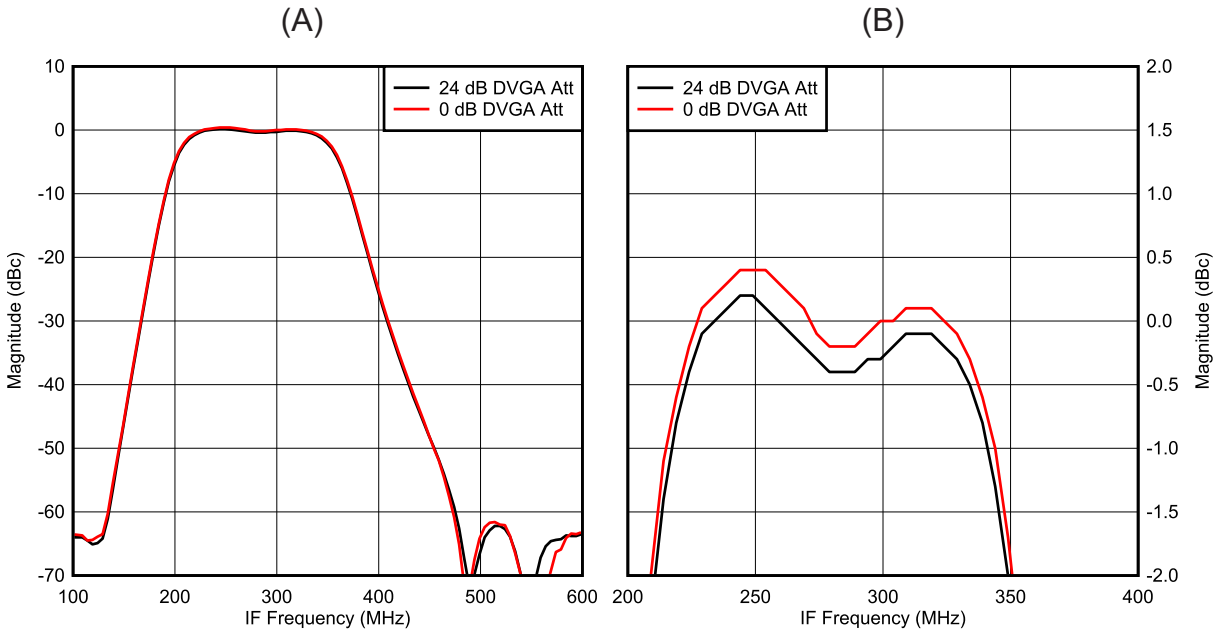

Figure 4. TSW16DX370EVM Selectivity Ch.A—Total Selectivity of IF Sub-System (A) and (B)

6 Design Files

6.1 Schematics

To download the schematics, see the design files at TIDA-00360.

6.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00360.

6.3 Layer Plots

To download the layer plots, see the design files at TIDA-00360.

6.4 Cadence/Allegro Files

To download the Cadence/Allegro files, see the design files at TIDA-00360.

6.5 Gerber Files

To download the Gerber files, see the design files at TIDA-00360.

6.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-00360.

6.7 Software Files

To download the software files, visit the TSW16DX370EVM product page and the High Speed Data Converter Pro Software product page.

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