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8-Ch Parallel 0.5-A Low-Side Digital Output Module for Programmable Logic Controllers (PLCs)

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TIDA-00236	Design Folder
Beaglebone Black	Community
DRV8803	Product Folder
ISO7140CC	Product Folder
ISO7142CC	Product Folder
SM72485	Product Folder

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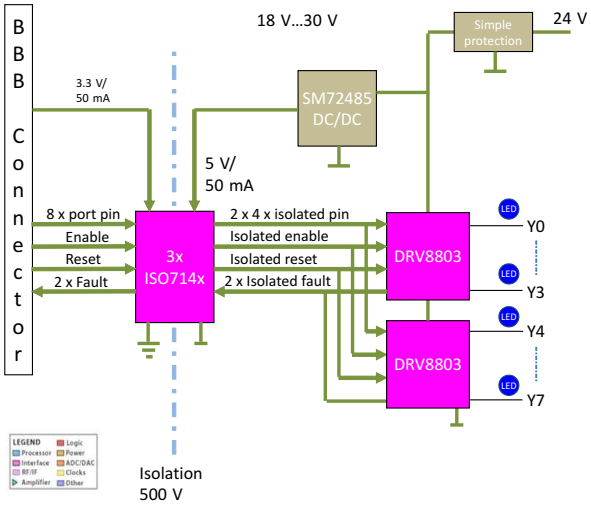
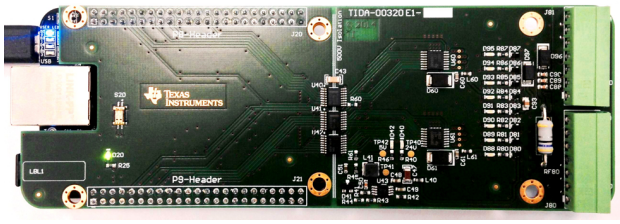
Design Features

- High-density 8-Ch, 24-V Low-Side Digital Output
- 500 mA/Ch Unregulated (20%), 2-A Peak
- Parallel Control for Simple MCU Interface
- Capable of Switching Inductive Loads
- LED to Indicate Output State
- Beaglebone Black Cape Form Factor for Easy Evaluation

Featured Applications

- PLC, DCS, and PAC
  - Digital Output
  - CPU (PLC)
- Motor Control I/O Modules
- Sensor Concentrators





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1 Key System Specifications

Table 1. Key System Specifications

SYMBOL	PARAMETER	CONDITIONS	SPECIFICATION			UNIT
			MIN	TYP	MAX	
V_{IN}	Input voltage	Normal operation	10	24	33	V
I_{IN}	Input current	Normal operation	—	15	50	mA
V_{LOAD}	Load supply voltage	Normal operation	0	24	44	V
I_{LOAD}	Load current	Per channel T_A = 85°C	—	500	600	mA
		Per channel T_A = 25°C	—	700	1000	mA
		Single channel per driver, T_A = 25°C	—	—	2000	mA
P_{LOSS}	Power loss per channel	R_L = 48 Ω, V_{LOAD} = 24 V, T_A = 25°C	—	200	—	mW
f_{SW}	Switching frequency	Resistive load		1000		Hz
		Inductive load, 0.1 H, all channels		10		Hz
t_{RISE}	Load voltage rise time 10% .. 90%	R_L = 48 Ω, V_{LOAD} = 24 V, T_A = 25°C	—	600	—	ns
t_{PDHL}	Propagation Delay Input L→H, output H→L (<90%)	R_L = 50 Ω, V_{LOAD} = 24 V, T_A = 25°C	—	440	—	ns
t_{FALL}	Load voltage fall time 90% .. 10%	R_L = 48 Ω, V_{LOAD} = 24 V, T_A = 25°C	—	140	—	ns
t_{PDLH}	Propagation Delay Input H→L, output L→H (> 10%)	R_L = 50 Ω, V_{LOAD} = 24 V, T_A = 25°C	—	540	—	ns
I_{PEAK}	Peak current (1 ms)		2.3		3.8	A
P_{IND}	Inductive power for each group of channels(1)				0.5	J/s

(1) Outputs Y0 to Y3 are one group, and outputs Y4 to Y7 are another group.

2 System Description

A digital output (DO) module is a standard module in a PLC or DCS system. The DO module is used to permanently turn on and off resistive, capacitive, or inductive loads or control them with pulse width modulation (PWM).

A DO with a MOSFET can be realized as a high-side or low-side switch. This design uses the low-side switch principal, which means that the load connected to the output between the 24-V supply and the output of the module. Therefore, the switch is below the load seen from the 24-V DC supply.

The advantage with this principle is its lower cost of the switching MOSFETs as they can be of NMOS type. These MOSFETs are about 2.5 times smaller compared to a PMOS FET with the same $R_{ds(on)}$. A gate voltage of 10 V above GND is sufficient to keep these FETs in the saturated region. This gate voltage also saves level shifters and charge pumps. A low-side configuration is on the other hand more sensitive to corrosion as the load is permanently connected to a 24-V supply even when switched off. This configuration also means that a short to ground turns on the load unintentionally.

The TIDA-00320 is designed as a Beaglebone Black Cape form factor. The microprocessor (MPU) on the Beaglebone Black can be used to control the outputs or the board can be used stand alone or any other MCU with 3.3-V GPIOs.

In most cases, the digital outputs are galvanic isolated from the control of the outputs. This design uses low-power digital isolators to separate the 24-V field side from the driving logic implemented by the Beaglebone Black. Even a lightning strike on the field side with ground shifts of 500 V and more will preserve the operation of the MPU.

3 Block Diagram

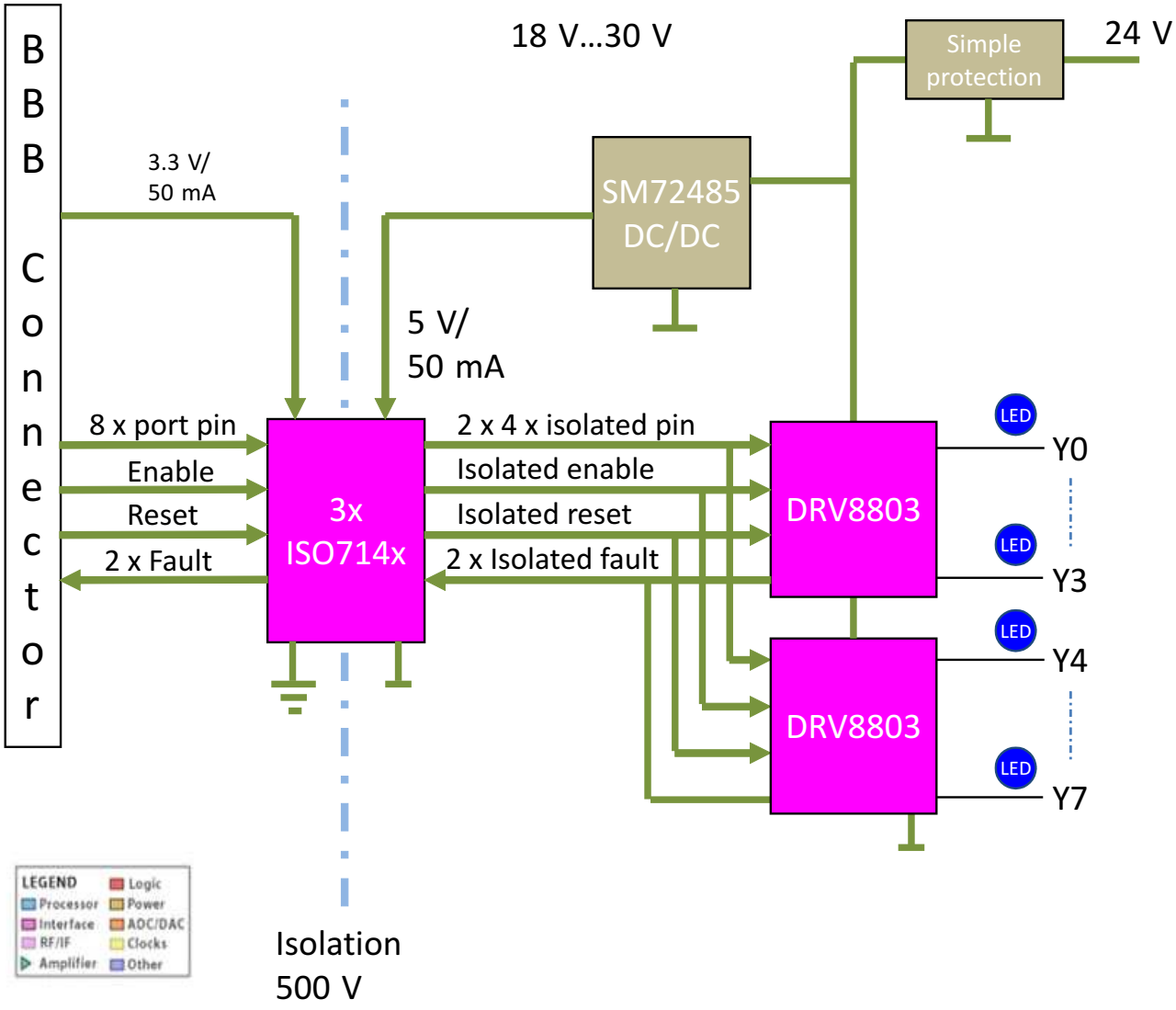

Figure 1. TIDA-00320 Block Diagram

3.1 Highlighted Products

The TIDA-00320 has eight DOs configured as low-side drivers. The design uses two DRV8803 with four protected low-side drivers integrated in each device. The ISO7140 provides galvanic isolation for the SPI channel. Each DRV8803 also has a global fault pin, which indicates fault on any of the four output channels. Those signals are connected to the ISO7140, which galvanic isolate the signals. The SM72485 is used in a low-cost buck configuration to provide 5 V for powering the secondary side of the ISO7140 and ISO7142. Eight status LEDs are connected to the outputs of the DRV8803s and indicate the physical status of the output.

3.1.1 DRV8803

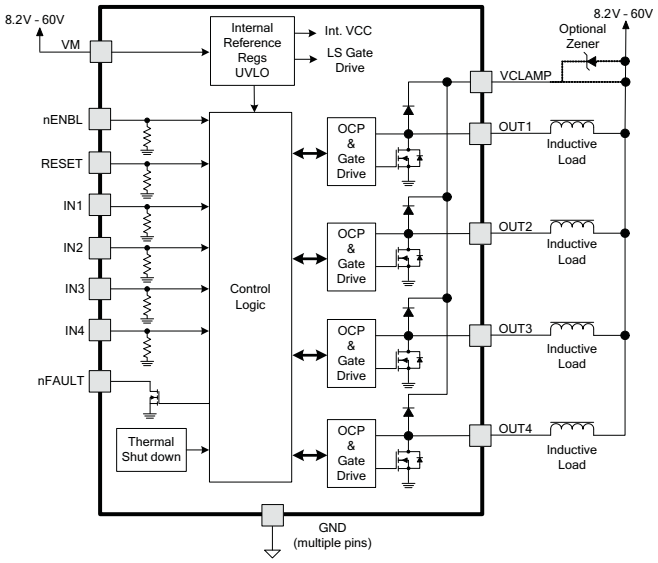

Figure 2. DRV8803 Block Diagram

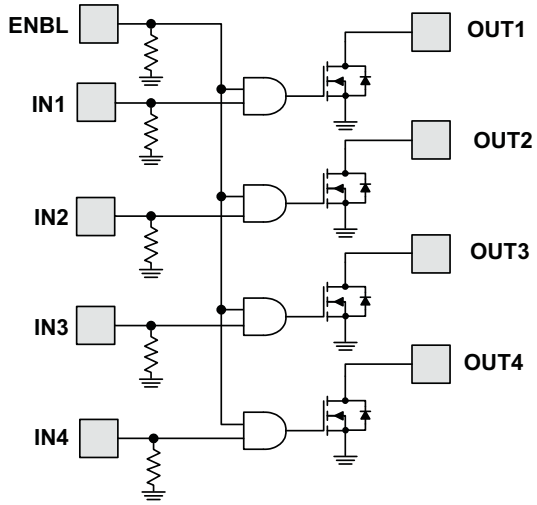

Figure 3. DRV8803 Simplified Diagram

3.1.2 ISO7140

The design uses eight Beaglebone Black signals for the outputs Y0 to Y7. Two additional signals are driving RESET and nENBL of the DRV8803s. The two signals /FAULT0 and /FAULT1 from the two DRV8803s are fed back to the Beaglebone Black to indicate error conditions. These ten forward and two backward signals are distributed over three isolator devices with four channels each. Two of the isolators are of an ISO7140 type with four channels in one direction and one isolator is of an ISO7142 type with two channels in each direction. The ISO714x family provides galvanic isolation at 2500 V_{RMS} for one minute per UL or 4242 V_{PK} per VDE. The selected isolators support up to 50 Mbps, which is well above the communication speed used in the design.

3.1.3 SM72485

The SM72485 is a wide input step down non-synchronous converter with integrated FET. In the design, this device provides a 5-V regulated output from the 24-V field connector to supply the isolator devices.

4 System Design Theory

4.1 Low-Side Driver Selection

To demonstrate the small form factor, this design uses two DRV8803. These devices integrate four power outputs in a PWP package at 5×7-mm board space and are capable of simultaneously driving 0.5 A at each output with only PCB cooling. An area of about 15 cm^2 per DRV8803 would suffice to operate at ambient temperatures of 85°C and the design provides around 22-cm^2 copper per device. The DRV8803s have internal diodes to a common clamping pin. This pin allows setting a clamping voltage different from the operating voltage for fast inductive discharge. The discharge then happens in an external Zener diode (D57 and D58). The power capability of the zener diodes defines the quantity of inductive discharge the module can handle and can be set application specific. The TIDA-00320 uses a clamp of 48 V and the Zener diodes have a 3-W power capability each. Thus, a maximum inductive discharge of 750 mJ can occur once each second for each output. The designer must take care of thermal management. In this design, the TVS cooling is sufficient for 500 mW, limiting the discharge to 125 mJ per second. The design considerations are also elaborated in Section 4.3.

Unlike the application circuit in the DRV8803 datasheet (SLVSAW5), the Zener diodes are connected between the clamping point and ground. This connection guarantees independence of the 24-V supply and the clamping voltage. Otherwise the 24-V supply voltage might creep up from inductive discharge until the clamping point voltage exceeds the absolute maximum voltage. Also, it is easier from a layout point of view to keep the current into ground close together during inductive switching, thus preventing noise from injecting into the ground.

4.2 Thermal Management

The thermal management budget has been calculated based on the following design considerations:

- The junction temperature should not surpass 150°C.
- The thermal resistance of the package is 2.3°K/W junction to bottom plate.
- The thermal vias have an inner diameter of 8 mm and a thermal resistance of 170°K/W.
- The board space provides thermal resistance to air of around 900°K/W per cm^2 (see formula 23 in Reference 2).

The $R_{DS(on)}$ of the DRV8803 is max 0.8 Ω, and with four outputs turned on at 0.5 A, the total power dissipation is 0.8 W per device ($4 \times 0.5^2 \times 0.8$). For an ambient temperature of 85°C, the junction temperature may increase 65°K. Therefore TIDA-00320 has 5 thermal vias per device, which results in 34°K/W resistance. The pad is also connected on the top side of the PCB with about the same thermal resistance of 34°K/W. The total connection resistance then is 17°K/W corresponding to a 14°K increase on top of the 1.8°K junction case rise. As a consequence, the copper area may only have a temperature increase of 49°K. The copper area therefore needs a thermal resistance to air of less than 61°K/W, which is equivalent to 15 cm^2. The TIDA-00320 has approximately 22 cm^2 available per DRV8803, so an ambient temperature of 85°C is safe to operate.

If an ambient temperature beyond 85°C is desired, the thermal management could be further optimized by using a four-layer board with thicker copper. While the inner layers cannot radiate the heat, they could still provide for better heat distribution and prevent the outer layers from being split by traces. Therefore, the active cooling area could be increased.

4.3 Switch off an Inductive Load

The TIDA-00320 can be used to switch off inductive loads like motors, valves, and so on. An inductive load has the property that it stores energy. When the switch wants to turn, the inductive load off this energy is released. The inductor tries to keep the current flowing, which could result in a high voltage spike at the output of the switch. Typical methods to prevent the occurrence of spikes are freewheeling diodes. These diodes limit the voltage at the inductor so that the diode does not exceed the typical diode forward voltage of 0.7 V. The resulting voltage at the output of the switch would be 24.7 V, assuming a power supply of 24 V. The method is simple, but it has the disadvantage the current keeps flowing for some period of time. The time is reverse proportional to the freewheeling voltage. For high speed actuators like injection valves in process control systems, this is not desired. The preferred method is to use a Zener diode so that the freewheeling voltage can be higher. In this reference design, the freewheeling voltage is clamped to 48 V. At a 24-V supply, this voltage will result in a freewheeling voltage of 24 V and a much faster decay of the inductor current. Therefore, this reference design is best suited for direct control of stepper motors or injection valves.

The DRV8803 has protected the low-side switches with one integrated clamping diode per each output. All clamping diodes are fed to one pin for an external Zener diode. This diode will clamp the voltage to 48 V.

The external Zener diodes in the TIDA-00320 (D57 and D58) is a 3-W TVS diode with cooling calculated for 500 mW; therefore, all outputs of one DRV8803 can absorb 0.5 J/s of energy. An inductive load of 100 mH can store around 12.5 mJ ($E = ½ \times L \times I^2$) at a current of 0.5 A. The diode could therefore switch at a rate of 40 Hz for one output or 10 Hz if all four outputs are loaded and switched.

4.4 Switching Light Bulbs

The TIDA-00320 can be used to switch conventional light bulbs. Such a load has a very low cold resistance so that the initial current can be as much as 10 times higher than the continuous current. A 24-V, 5-W light bulb has an in-rush current of 2 A, which is within the operating range of the DRV8803. Larger light bulbs would trigger the overcurrent protection without harming the DRV8803, but the light bulb might not turn on as desired.

5 Getting Started Hardware

The TIDA-00320 can be used either as cape with the Beaglebone Black evaluation platform or as a standalone card with any processor capable of handling parallel GPIO communication. For the connection to the Beaglebone Black connector, J20 and J21 will handle the communication.

5.1 Pin Assignment

Table 2. Pin Assignment

TIDA-00320 FUNCTION	TIDA-00320 HEADER	BBB HEADER	SOFTWARE	DIRECTION
Y0	J20, PIN 8	P8_8	TIMER7	OUT
Y1	J21, PIN 12	P9_12	GPIO1_28	OUT
Y2	J21, PIN 23	P9_23	GPIO1_17	OUT
Y3	J21, PIN 22	P9_22	UART2_RXD	OUT
Y4	J20, PIN 9	P8_9	TIMER5	OUT
Y5	J20, PIN 10	P8_10	TIMER6	OUT
Y6	J20, PIN 14	P8_14	GPIO0_26	OUT
Y7	J20, PIN 17	P8_17	GPIO0_27	OUT
nENBL	J21, PIN 15	P9_15	GPIO1_16	OUT
RESET	J21, PIN 21	P9_21	UART2_TXD	OUT
/FAULT0(Y0..Y3)	J20, PIN 26	P8_26	GPIO1_29	IN
/FAULT1(Y4..Y7)	J20, PIN 18	P8_18	GPIO2_1	IN

5.2 Initialization and Control

During the start-up phase, the Beaglebone Black I/O pins might be floating. The selected isolator type ISO7140CC drives in this case its outputs high. These levels will keep RESET and nENBL high, which deactivates the DRV8803 outputs and prevents undesired switching. The following initialization sequence will help to activate outputs only after the control code is up and running:

1. Configure P9_15 as output.
2. Set nENBL high (P9_15).
3. Configure P9_21 as output.
4. Set RESET high (P9_21).
5. Set In_Y0 – In_Y7 low: Y0 to Y7 = P8_8, P9_12, P9_23, P9_22, P8_9, P8_10, P8_14, P8_17
6. Set RESET low. 7. Set nENBL low.

The TIDA-00320 is now active. The following sequence should be part of the control loop:

1. Set In_x high for any output to activate: Y0 to Y7 = P8_8, P9_12, P9_23, P9_22, P8_9, P8_10, P8_14, P8_17
2. Set In_x low for any output to deactivate.
3. Monitor input /FAULT0 for Y0 to Y3 (BBB pin P8_26) and display error condition (error: /FAULT0 = low) in conjunction with group Y0 to Y3.
4. Monitor input /FAULT1 for Y4 to Y7 (BBB pin P8_18) and display error condition (error: /FAULT0 = low) in conjunction with group Y4 to Y7.

5.3 Fault Signal

The /XFAULT0 signal on pin 26 of J20 is a global fault signal for any of the four outputs Y0 to Y3. /XFAULT1 provides the same function for outputs Y4 to Y7. The pin will be driven low in the case of an overcurrent in any of the DRV8803. At the same time, the corresponding output driver will be turned off. After 1.2 ms, THE OUTPUT DRIVER will retry to drive the output and clear the fault signal if the overcurrent situation is gone. /XFAULT will also be cleared if the XRST pin is activated or the 24-V field supply is removed (J61 or J62).

If the die temperature in the DRV8803s exceeds safe limits, all outputs will be switched off and the /XFAULT of that DRV8803 will be driven low. The operation will resume when the temperature falls under the limit.

5.4 Power Supply

The board is connected to a 24-V field supply. The 5 V for the isolators are coming from this supply as well as the voltage VM for the DRV parts. A combination of a fusible resistor and a 33-V TVS diode is used as protection against surge pulses of 500 V. For faster transients like ESD strikes, a filter based on the fusible resistor and three low ESR capacitors is formed. Reverse polarity protection follows after this surge protection and is implemented as simple diode.

EMI protection is implemented using the series resistor RF80 and set of PI-filters for the DC/DC converter and each of the DRV8804 driver ICs. The PI-filter for the DC/DC converter consists of C93, C94, L40, C47, and C48. The filter has the –3-dB point at 600 kHz and a steepness of 18 dB per octave. The filter for the DRVs consists of C93, C94, and L80/C80 for U60 and L81/C81 for U61. Below 600 kHz, the capacitive behavior of the PI-filter creates a low pass with RF80 with its –3-dB point at 30 kHz and a steepness of 6 dB per octave. This low pass leads to a damping factor of –30 dB at 600 kHz for both DRV8803 parts and –50 dB for the SM72485. At 1.2 MHz, these factors are already –64 dB for the DRVs and –84 dB for the SM72485.

The spice simulation model for the set of filters is shown in Figure 4 and the corresponding AC simulation plot in Figure 5.

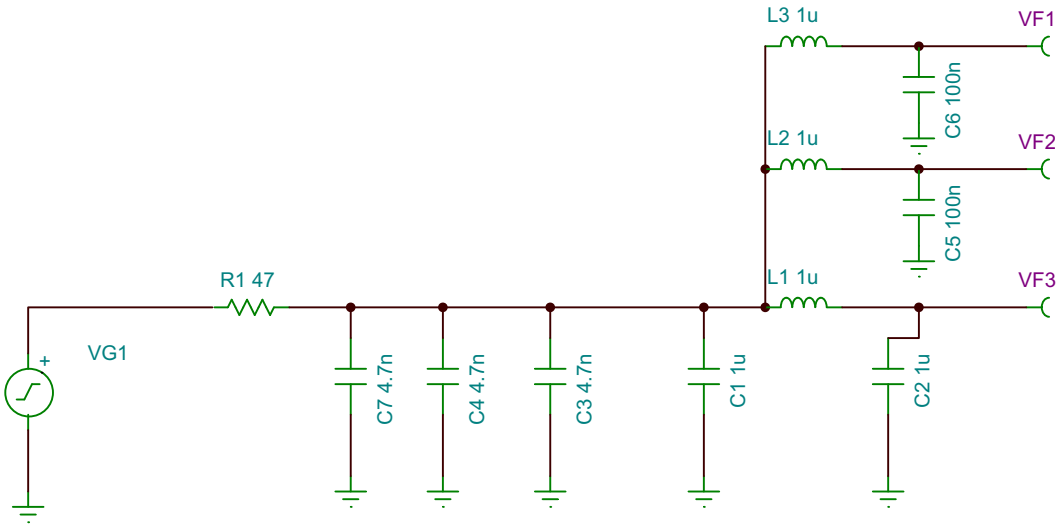

Figure 4. EMI Filter Simulation Model

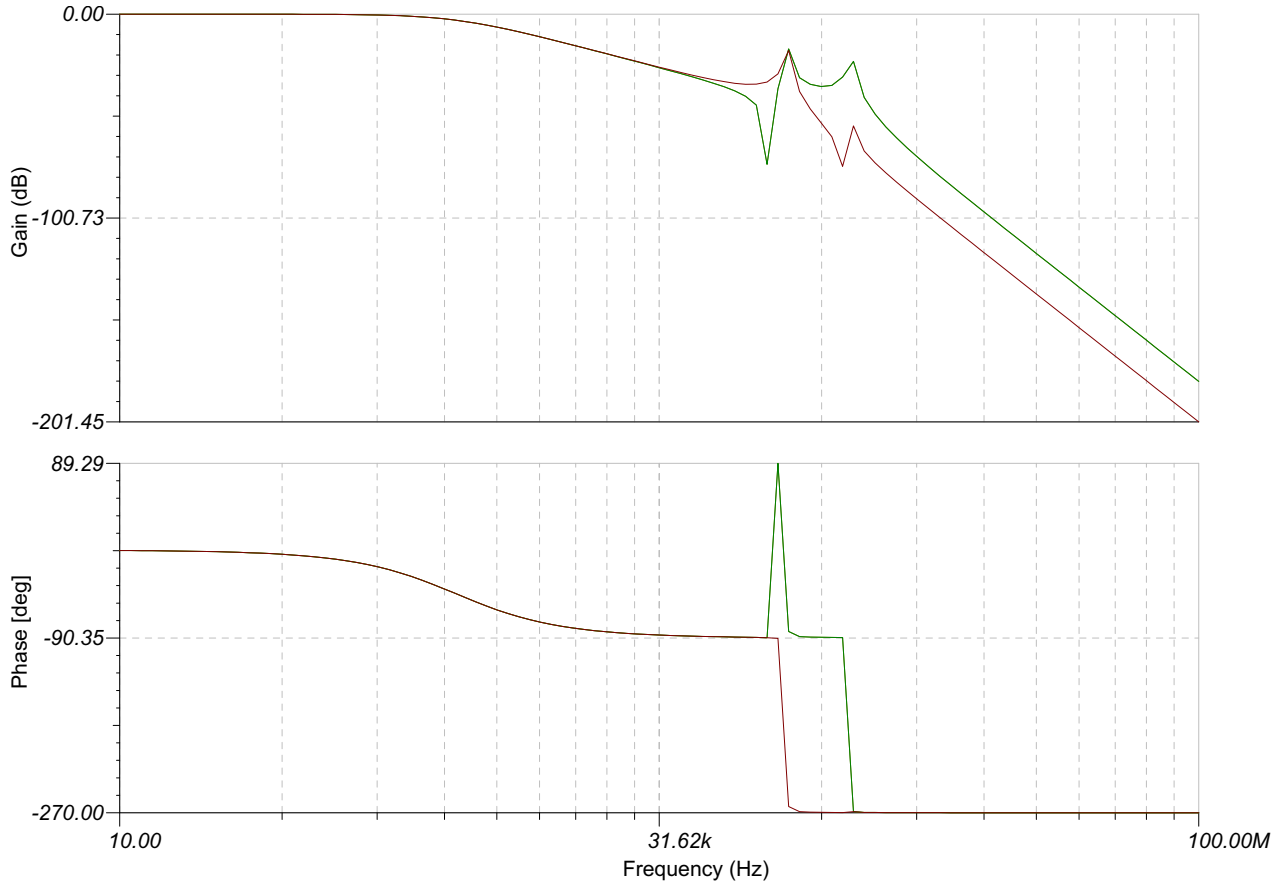

Figure 5. AC Simulation Plot

5.5 Output and Field Power Connector

All DRV8803 outputs are connected to blue LEDs. The LED current is set to around 2 mA. Additional diodes are in series with the LEDs to eliminate reverse currents from inductive switching. Close to each output connector pin is a 10-nF capacitor to reduce ESD sensitivity and reduce EMI. The board connector is a low-profile type so that it is possible to stack capes and still have access to each of the boards.

6 Test Setup

6.1 Output Current Capability

Setup for testing the output current capability:

- Power supply: GW inSTEK GPS-4303 quad output DC power supply 2 × 0 to 30 V, 3 A and 8 to 15 V, 1 A and 2.2 to 5.5 V, 1 A
- Thermo scan: Fluke Ti40FT 160×120, calibrated from –20°C to 350°C

The correctness of the thermal management is verified by connecting the output Y7 through an electronic load to the 24 V of the power supply. GND and Earth are connected to 0 V of the power supply. The output is programmed to turn on. The current from the power supply into the electronic load is set to the level required to achieve an approximate 0.8-W power loss in the DRV8803, which is the equivalent power loss as if all outputs carry 0.5 A each. The value will be close to 1.15 A, causing a drop voltage of 0.72 V. The temperature of the driving switch is observed using the thermo scan. The temperature is expected to settle at around 65˚C at a room temperature of 25˚C. The typical drop voltage over the switch at room temperature and at the nominal current of 500 mA is expected to be 250 mV.

6.2 Rise, Fall, and Propagation Delay Times

Setup for testing the rise, fall, and propagation delay times:

- Power supply: GW inSTEK GPS-4303 quad output DC power supply 2 × 0 to 30 V, 3 A and 8 to 15 V, 1 A and 2.2 to 5.5 V, 1 A
- Oscilloscope: Tektronix TDS 3034

All four outputs of one group (Y4 to Y7) are connected through individual 48-Ω, 12-W resistors to 24 V of the power supply. GND and Earth are connected to 0 V of the power supply. The oscilloscope is connected to the latch input on the host side with channel one and to output Y7 with channel two. It is set to normal trigger rising edge with the trigger coming from channel one. Trigger level is 1 V. Then, all outputs are programmed to turn on. The oscilloscope will capture a falling edge on Y7. Thereafter, all outputs are programmed to turn off and the oscilloscope will capture a rising edge on Y7. The measurement is repeated with the other three outputs of the same group. Then, the resistors are connected to the second group of outputs (Y0 to Y3) and the measurement continues on these.

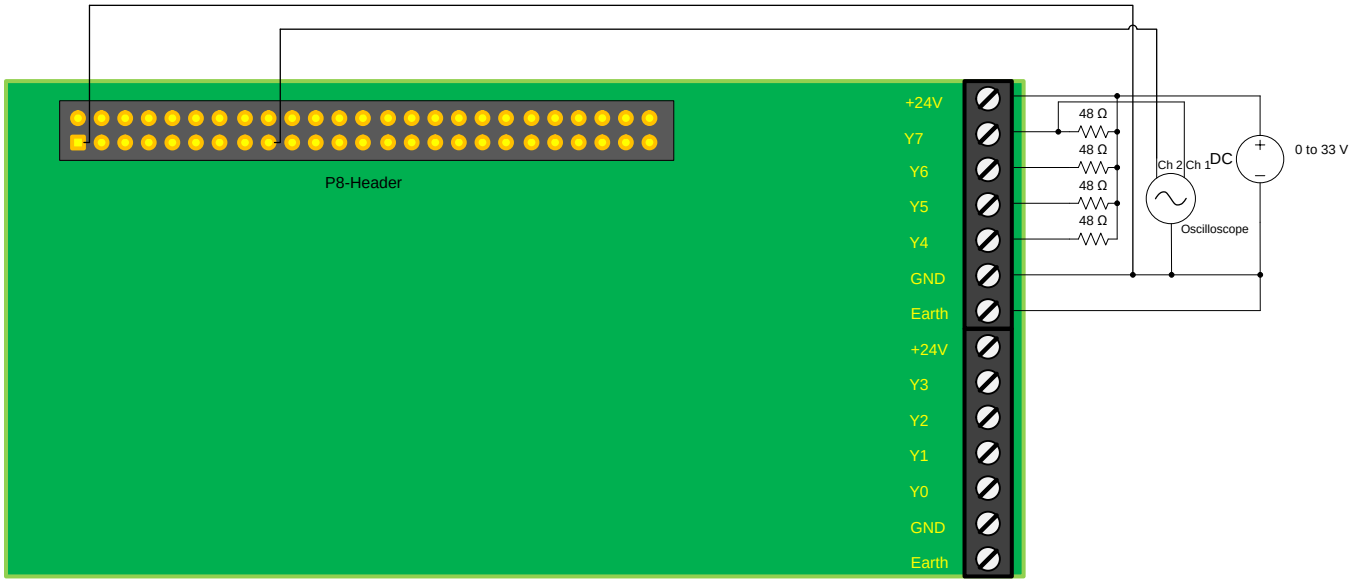

Figure 6. Measurement Setup for Rise, Fall, and Propagation Delay Times

7 Test Data

Table 3. Test Results

SYMBOL	PARAMETER	CONDITIONS	SPECIFICATION			MEAS.	UNIT
			MIN	TYP	MAX		
V_{IN}	Input voltage	Normal operation	10	24	33	24.5	V
I_{IN}	Input current	Normal operation	—	15	50(1)	14	mA
V_{LOAD}	Load supply voltage	Normal operation	0	24	44	24.5	V
I_{LOAD}	Load current	Per channel T_A = 60°C	—	500	600	—(2)	mA
		Per channel TA = 25°C	—	700	1000	—(2)	mA
P_{LOSS}	Power loss per channel	R_L = 48 Ω, V_{LOAD} = 24 V, T_A = 25°C	—	200	—	—(2)	mW
f_{SW}	Switching frequency	Resistive load		1000		1000	Hz
		Inductive load, 0.1 H all channels		10		—(2)	Hz
t_{RISE}	Load voltage rise time (10% to 90%)	R_L = 48 Ω, V_{LOAD} = 24 V, T_A = 25°C	—	600	—	550	ns
t_{FALL}	Load voltage fall time (90% to 10%)	R_L = 48 Ω, V_{LOAD} = 24 V, T_A = 25°C	—	120	—	125	ns
t_{PD}	Propagation Delay (latch to output change)	R_L = 50 Ω, V_{LOAD} = 24 V, T_A = 25°C	60	150	200	165	ns
I_{PEAK}	Peak current (1 ms)		2.3		3.8	—(2)	A
P_{IND}	Inductive power for each group of channels(3)				0.5	—(2)	J/s

(1) Depends on number of LEDs on and communication activity.
(2) Based on calculations derived from DRV8803 datasheet.
(3) Outputs Y0 to Y3 are one group, and outputs Y4 to Y7 are another group.

In Figure 7, channel 2 (red) is connected to the In0 signal of the host connector and triggers on rising edge. This edge causes the data to transfer to the output Y0 in the form of a high to low transition and is therefore suited to capture this output transition on channel 1 (blue) and the timing for the $t_{pd(HL)}$ propagation delay measurement. The fall time is dominated by the switching speed of the output transistor in the driver. Due to the open drain configuration, the rise time results from the RC combination formed by the 10-nF capacitor connected to the switch output in the reference design, the driver output capacitance, and the 48-Ω load resistor at the output.

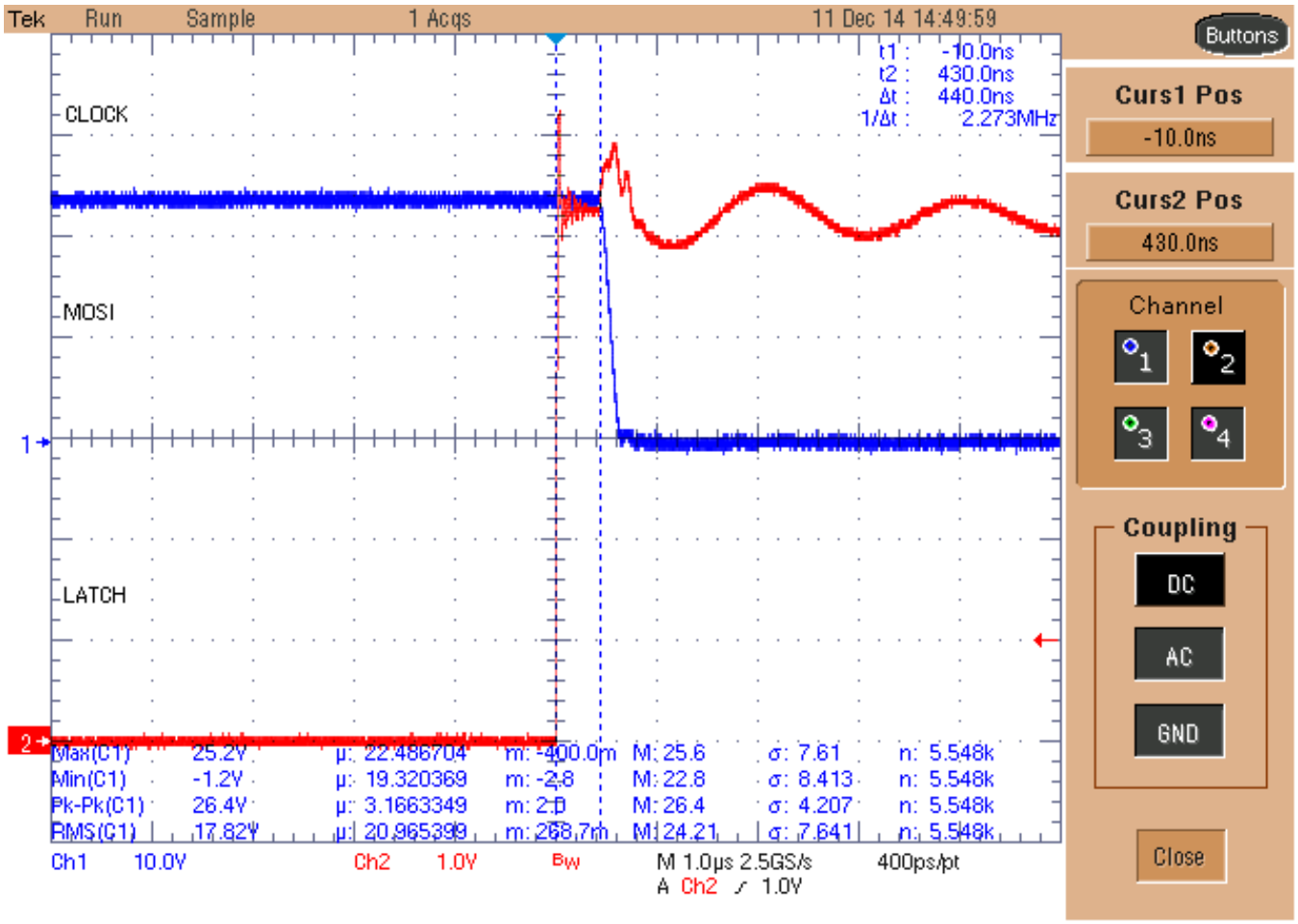

Figure 7. Fall Time and Propagation Delay

In Figure 8, channel 2 (red) is still connected to the In0 signal of the host connector and triggers now on the falling edge. This edge causes the data to transfer to the output Y0 in form of a low to high transition and is therefore suited to capture this output transition on channel 1 (blue) and the timing for the $t_{pd(LH)}$ propagation delay measurement. Due to the open drain configuration, the rise time results from the RC combination formed by the 10-nF capacitor connected to the switch output in the reference design, the driver output capacitance, and the 48-Ω load resistor at the output.

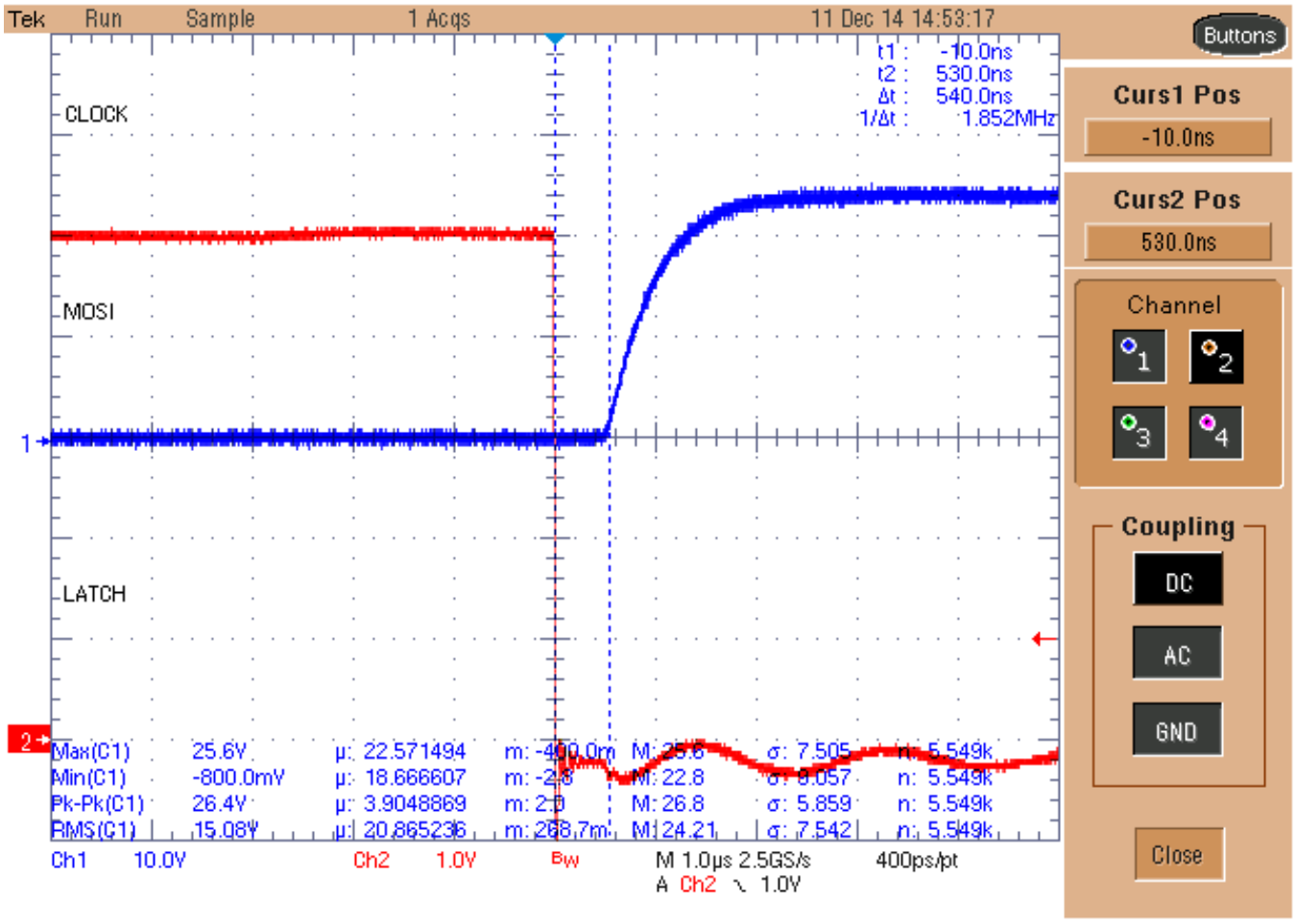

Figure 8. Rise Time and Propagation Delay

The result of the heat management verification is visible in Figure 9 for the bottom of the PCB and in Figure 10 for the top of PCB. The bottom side reaches round 50°C under the DRV8803, and the top side peaks at 65°C on the top surface of the IC. These peaks correspond to a temperature rise of 35°K to 40°K in the silicon above the ambient temperature. Based on the heat distribution on thermal images with both DRV8803 active, the temperature rise would be 10°K higher. Assuming a maximum silicon temperature of 150°C, an ambient temperature of 100°C would be absolute maximum. 85°C would leave sufficient guard band for safe operation under all conditions.

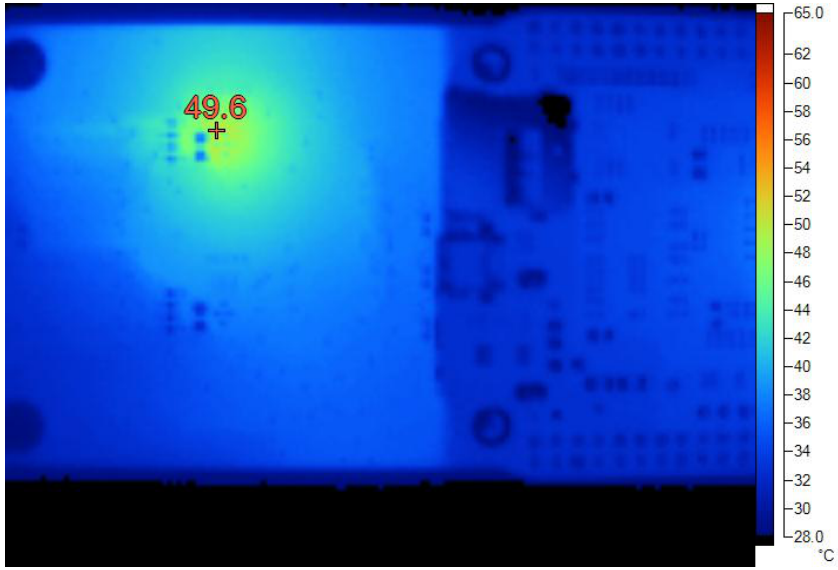

Figure 9. Thermal Scan of PCB Bottom Under Load

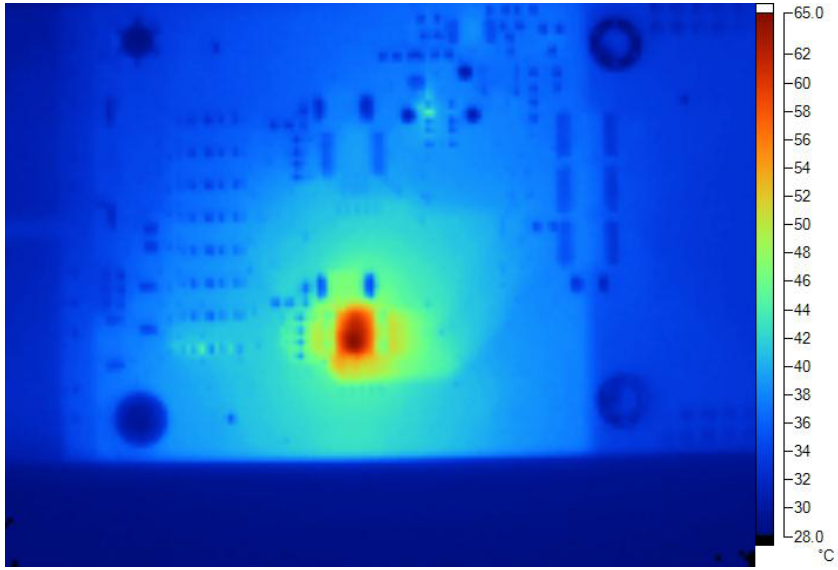

Figure 10. Thermal Scan of PCB Top Under Load

8 Design Files

8.1 Schematics

To download the schematics, see the design files at TIDA-00320.

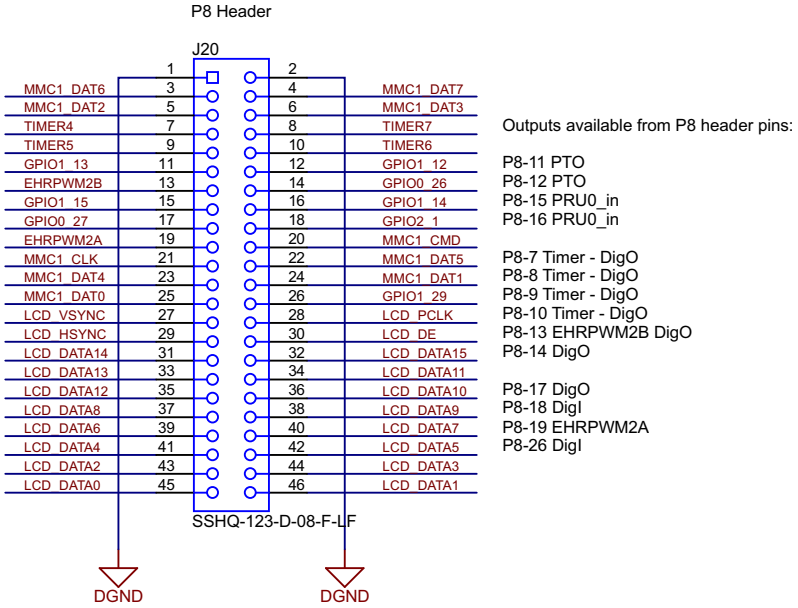

Figure 11. Beaglebone Connector and ID Prom1

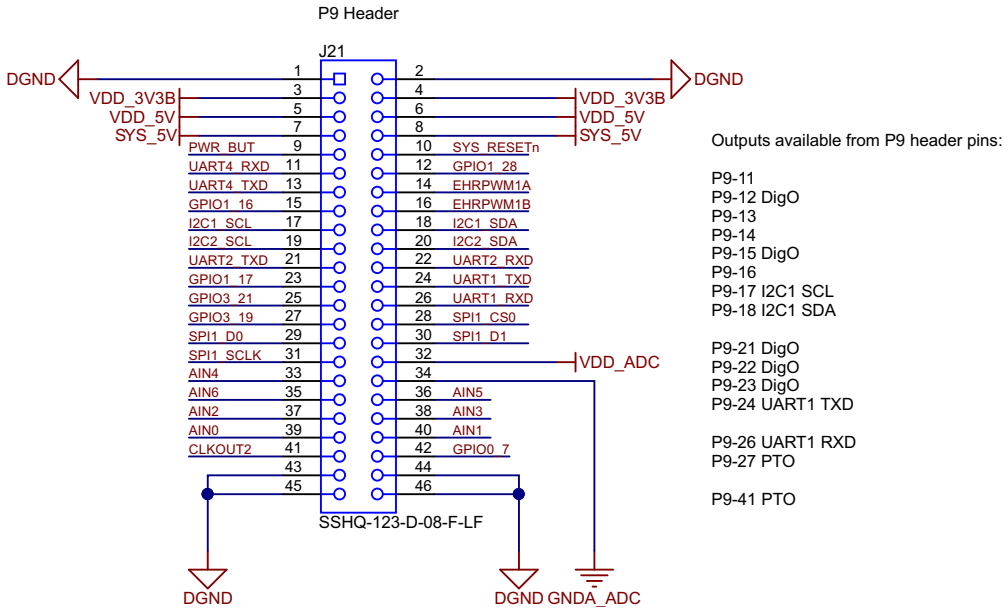

Figure 12. Beaglebone Connector and ID Prom2

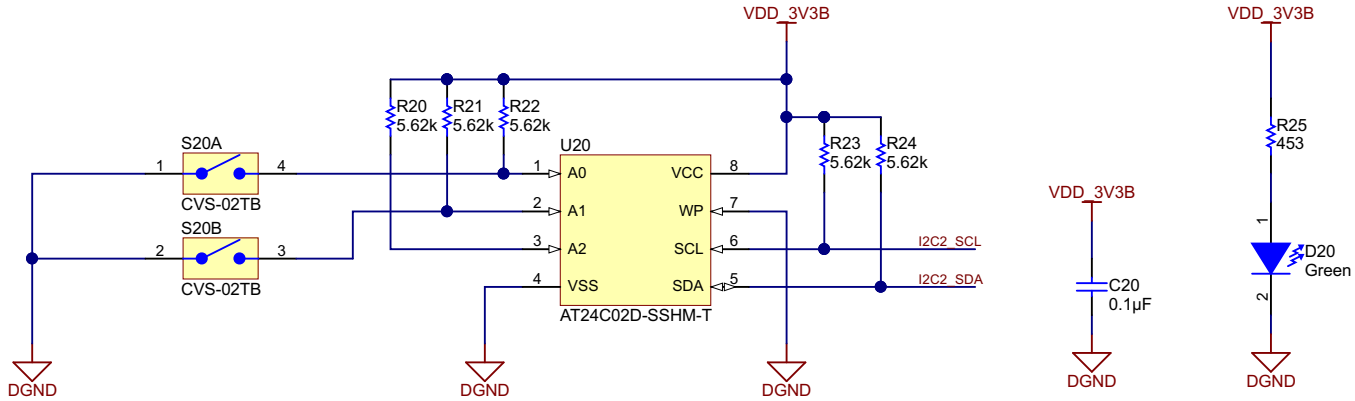

Figure 13. Beaglebone Connector and ID Prom3

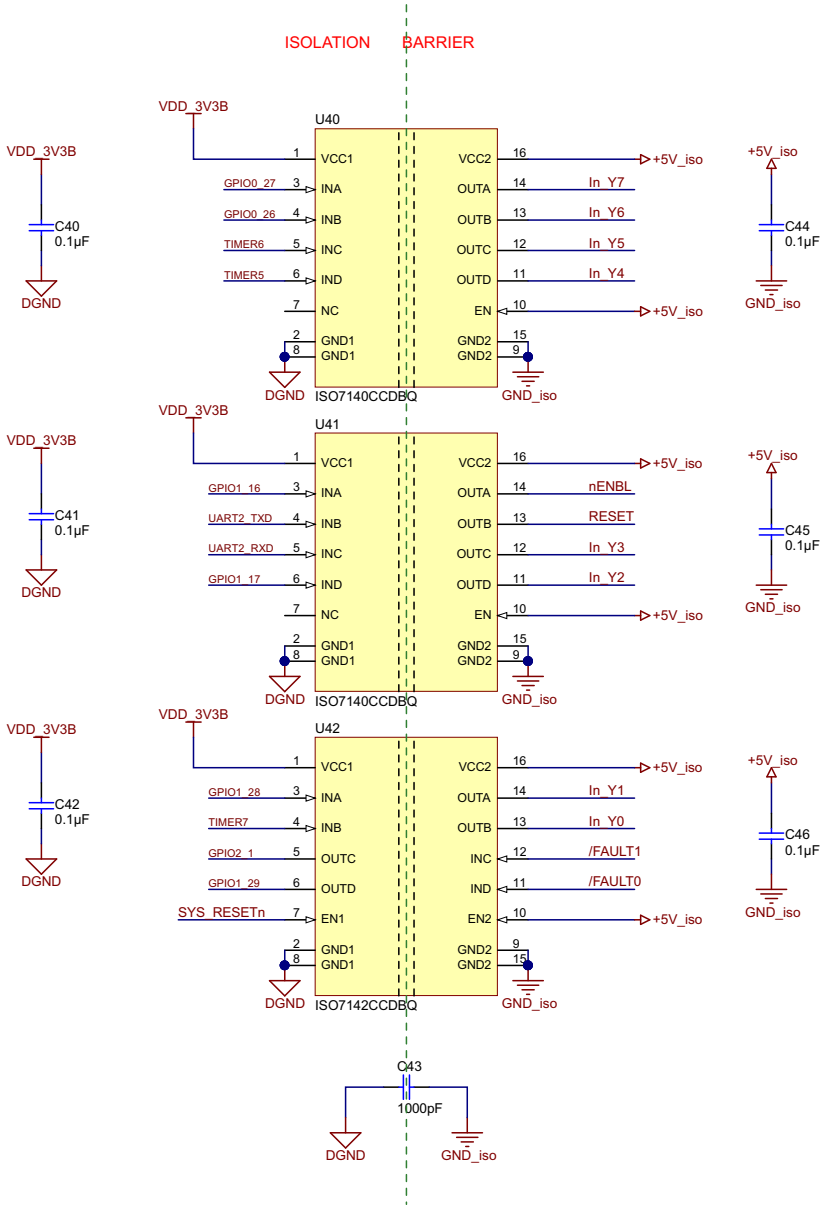

Figure 14. Digital Isolators and Field Power Supply1

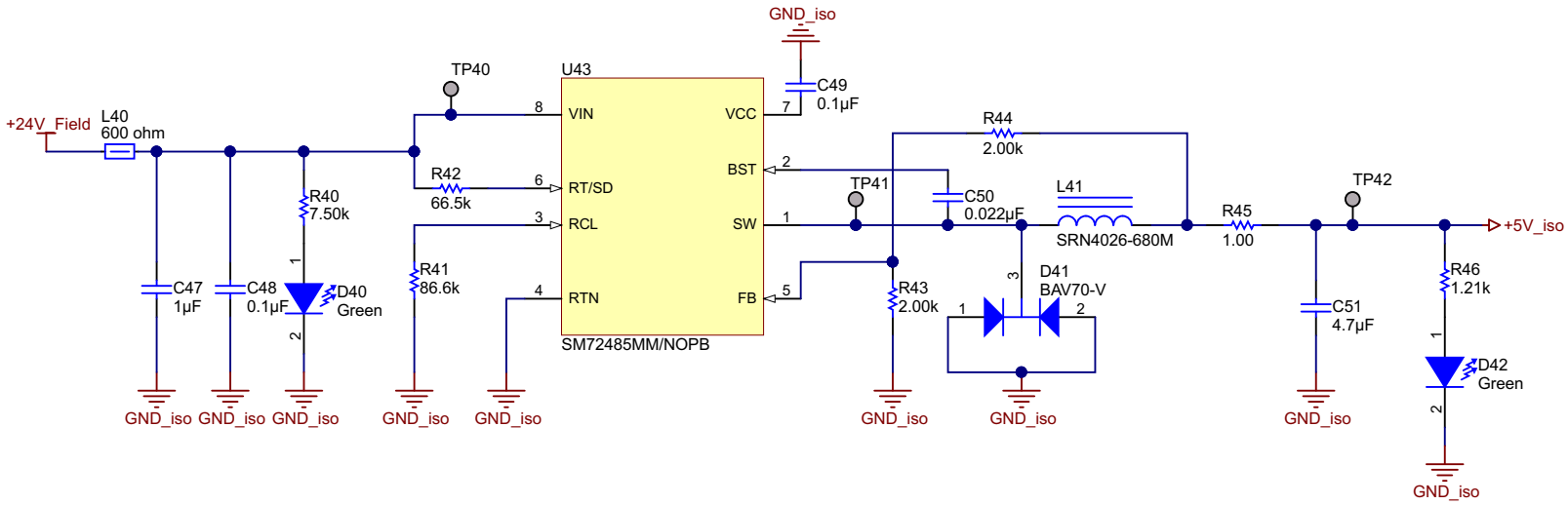

Figure 15. Digital Isolators and Field Power Supply2

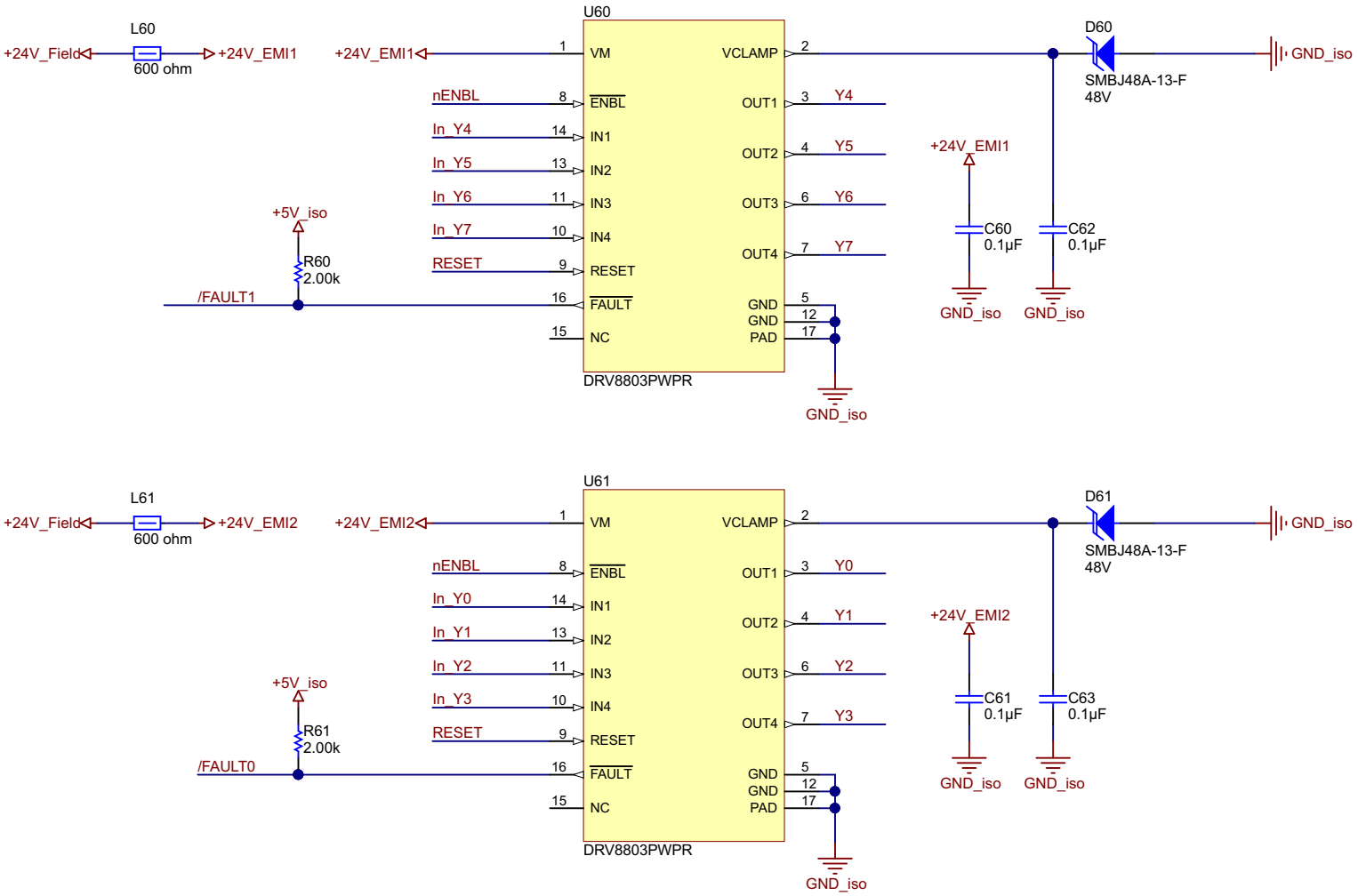

Figure 16. Digital Output Stage

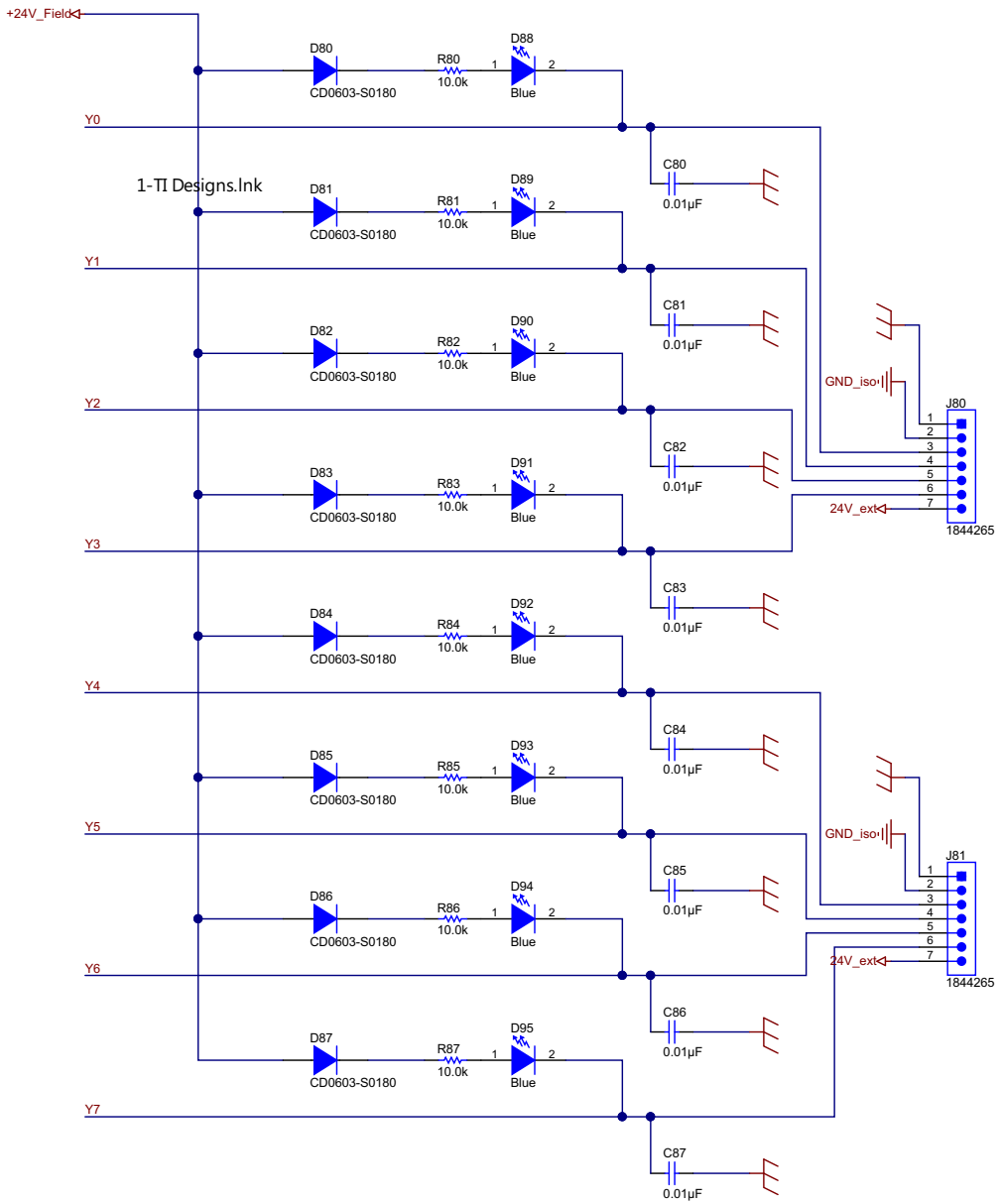

Figure 17. Output Connectors and Surge Protection1

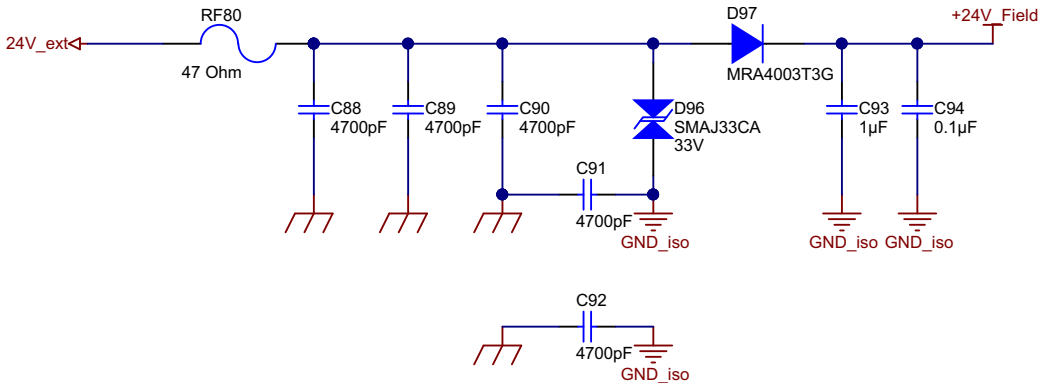

Figure 18. Output Connectors and Surge Protection2

8.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00320.

Table 4. BOM

ITEM #	DESIGNATOR	QTY	VALUE	PARTNUMBER	MANUFACTURER	DESCRIPTION	PACKAGE REFERENCE
1	!PCB1	1		TIDA-00320	Any	Printed Circuit Board	
2	C20, C40, C41, C42, C44, C45, C46, C49, C60, C61	10	0.1 µF	C0603C104K5RACTU	Kemet	CAP, CERM, 0.1 µF, 50 V, ±10%, X7R, 0603	0603
3	C43	1	1000 pF	202R18W102KV4E	Johanson Dielectrics Inc	CAP, CERM, 1000 pF, 2 KV 10% X7R 1206	1206
4	C47	1	1 µF	C3216X7R1H105K	TDK	CAP, CERM, 1 µF, 50 V, ±10%, X7R, 1206	1206
5	C48, C94	2	0.1 µF	C0603C104K5RACTU	Kemet	CAP, CERM, 0.1 µF, 50 V, ±10%, X7R, 0603	0603
6	C50	1	0.022 µF	C0603C223K5RACTU	Kemet	CAP, CERM, 0.022 µF, 50 V, ±10%, X7R, 0603	0603
7	C51	1	4.7 µF	C0603C475K8PACTU	Kemet	CAP, CERM, 4.7 µF, 10 V, ±10%, X5R, 0603	0603
8	C62, C63	2	0.1 µF	CL21B104KCFSFNE	Samsung	CAP, CERM, 0.1 µF, 100 V, ±10%, X7R, 0805	0805
9	C80, C81, C82, C83, C84, C85, C86, C87	8	0.01 µF	C1608X7R2A103M	TDK	CAP, CERM, 0.01 µF, 100 V, ±20%, X7R, 0603	0603
10	C88, C89, C90, C91, C92	5	4700 pF	C1608X8R2A472K	TDK	CAP, CERM, 4700 pF, 100 V, ±10%, X8R, 0603	0603
11	C93	1	1 µF	CL21B105KBFNNNE	Samsung	CAP, CERM, 1 µF, 50 V, ±10%, X7R, 0805	0805
12	D20, D40, D42	3	Green	LTST-C190KGKT	Lite-On	LED, Green, SMD	1.6 × 0.8 × 0.8 mm
13	D41	1	70 V	BAV70-V	Vishay-Semiconductor	Diode, Switching, 70 V, 0.25 A, SOT-23	SOT-23
14	D60, D61	2	48 V	SMBJ48A-13-F	Diodes Inc.	Diode, TVS, Uni, 48 V, 600 W, SMB	SMB
15	D80, D81, D82, D83, D84, D85, D86, D87	8	90 V	CD0603-S0180	Bourns	Diode, Switching, 90 V, 0.1 A, 0603 Diode	0603 Diode
16	D88, D89, D90, D91, D92, D93, D94, D95	8	Blue	LB Q39G-L2N2-35-1	OSRAM	LED, Blue, SMD	BLUE 0603 LED
17	D96	1	33 V	SMAJ33CA	Littelfuse	Diode, TVS, Bi, 33 V, 400 W, SMA	SMA
18	D97	1	300 V	MRA4003T3G	ON Semiconductor	Diode, Standard Recovery Rectifier, 300 V, 1 A, SMA	SMA

Table 4. BOM (continued)

ITEM #	DESIGNATOR	QTY	VALUE	PARTNUMBER	MANUFACTURER	DESCRIPTION	PACKAGE REFERENCE
19	FID1, FID2, FID3, FID4, FID5	5		N/A	N/A	Fiducial mark. There is nothing to buy or mount.	Fiducial
20	J20, J21	2		SSHQ-123-D-08-F-LF	Major League Electronics	Female Connector, 2.54 mm, 23×2, TH	Female Connector, 2.54 mm, 23×2, TH
21	J80, J81	2		1844265	Phoenix Contact	Header (Shrouded), 3.5 mm, 7×1, R/A, TH	TH, 7-Leads, Body 9.2 × 25.9, Pitch 3.5 mm
22	L40, L60, L61	3	600 Ω	BLM18KG601SN1D	MuRata	Ferrite Bead, 600 Ω @ 100 MHz, 1.3 A, 0603	0603
23	L41	1	68 µH	SRN4026-680M	Bourns	Inductor, Wirewound, Ferrite, 68 µH, 0.35 A, 0.852 Ω, SMD	SMD, 2-Leads, Body 4.2×4.2 mm
24	LBL1	1		THT-14-423-10	Brady	Thermal Transfer Printable Labels, 0.650" W × 0.200" H - 10,000 per roll	PCB Label 0.650"H × 0.200"W
25	R20, R21, R22, R23, R24	5	5.62 k	CRCW06035K62FKEA	Vishay-Dale	RES, 5.62 k, 1%, 0.1 W, 0603	0603
26	R25	1	453	CRCW0603453RFKEA	Vishay-Dale	RES, 453, 1%, 0.1 W, 0603	0603
27	R40	1	7.50 k	CRCW06037K50FKEA	Vishay-Dale	RES, 7.50 k, 1%, 0.1 W, 0603	0603
28	R41	1	86.6 k	CRCW060386K6FKEA	Vishay-Dale	RES, 86.6 kΩ, 1%, 0.1 W, 0603	0603
29	R42	1	66.5 k	CRCW060366K5FKEA	Vishay-Dale	RES, 66.5 kΩ, 1%, 0.1 W, 0603	0603
30	R43, R44, R60, R61	4	2.00 k	CRCW06032K00FKEA	Vishay-Dale	RES, 2.00 k, 1%, 0.1 W, 0603	0603
31	R45	1	1.00	CRCW06031R00FKEA	Vishay-Dale	RES, 1.00, 1%, 0.1 W, 0603	0603
32	R46	1	1.21 k	CRCW06031K21FKEA	Vishay-Dale	RES, 1.21 k, 1%, 0.1 W, 0603	0603
33	R80, R81, R82, R83, R84, R85, R86, R87	8	10.0 k	CRCW060310K0FKEA	Vishay-Dale	RES, 10.0 kΩ, 1%, 0.1W, 0603	0603
34	RF80	1	47	EMC2-47RKI	TT Electronics/IRC	RES, 47 Ω, 10%, 2 W, Fusible, TH	Axial resistor
35	S20	1		CVS-02TB	Copal Electronics	DIP Switch, SPST, 2Pos, Slide, SMT	SW, 4.7 × 1.45 × 3 mm
36	U20	1		AT24C02D-SSHM-T	Atmel	I2C-Compatible (2-wire) Serial EEPROM 2-Kbit (256 × 8), SOIC-8	SOIC-8
37	U40, U41	2		ISO7140CCDBQ	Texas Instruments	4242-V_{PK} Small-Footprint and Low-Power Quad Channels Digital Isolators, DBQ0016A	DBQ0016A
38	U42	1		ISO7142CCDBQ	Texas Instruments	4242-V_{PK} Small-Footprint and Low-Power Quad Channel Digital Isolator, DBQ0016A	DBQ0016A

Table 4. BOM (continued)

ITEM #	DESIGNATOR	QTY	VALUE	PARTNUMBER	MANUFACTURER	DESCRIPTION	PACKAGE REFERENCE
39	U43	1		SM72485MM/NOPB	Texas Instruments	SolarMagic 100 V, 150 mA Constant On-Time Buck Switching Regulator, DGK0008A	DGK0008A
40	U60, U61	2		DRV8803PWPR	Texas Instruments	Quad Low-Side Driver IC, PWP0016D	PWP0016D

8.3 PCB Layout Recommendations and Guidelines

Sufficient cooling of the DRV8803s is critical to the design and requires thermal vias under the devices and contiguous copper area. In this design, thermal vias are also used to transfer the heat between the layers if traces break the cooling area. The goal was to have sufficient cooling and still maintain a two-layer design. The red circle in Figure 19 shows an area where heat is blocked by a trace. A number of vias around the trace will lead the heat to the bottom layer under the trace and back to the top layer beyond the trace. Figure 20 shows contiguous copper for that part of the PCB. All together, this design practice effectively increasing the active copper area by around 50%. The result and effectiveness of this practice can be seen in Figure 9 and Figure 10 where heat is transferred beyond the trace on the top layer.

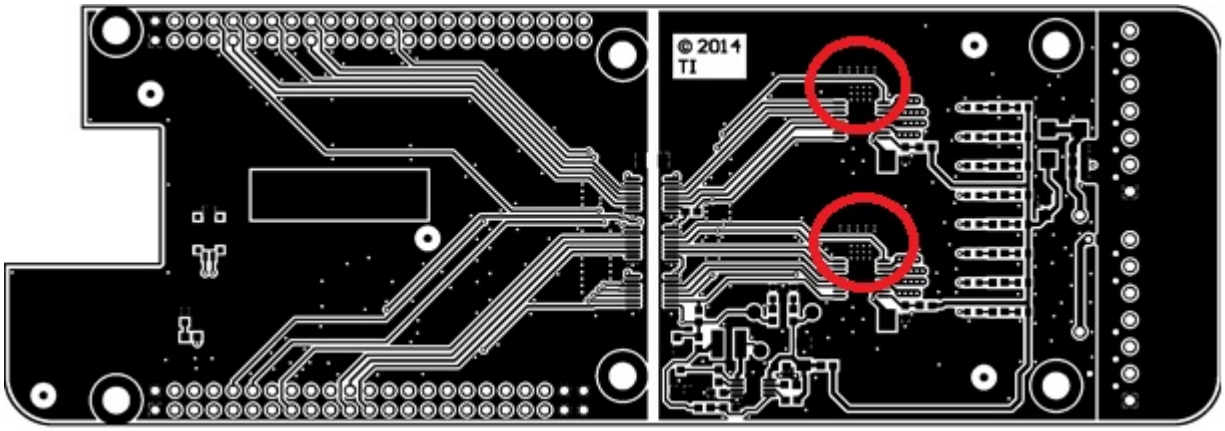

Figure 19. Top View

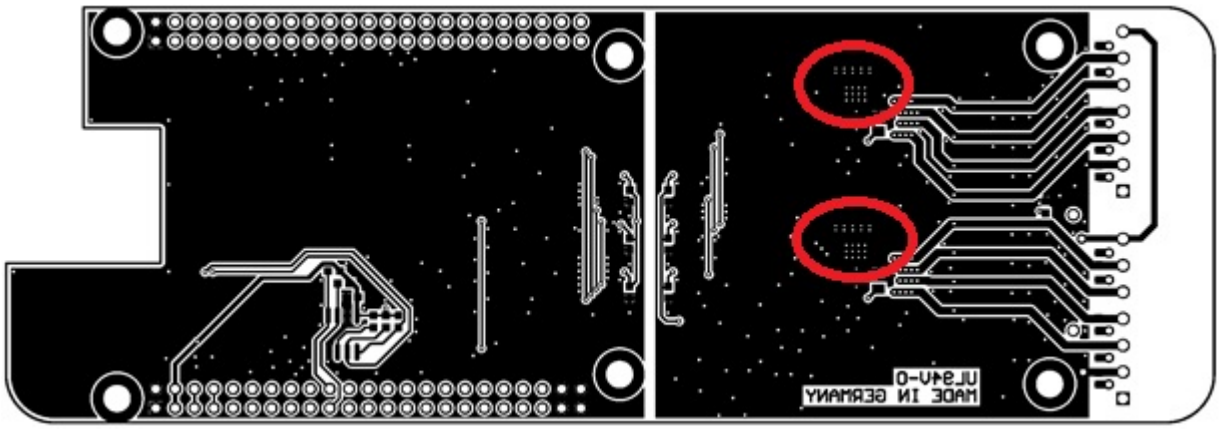

Figure 20. Bottom View

8.3.1 Layer Plots

To download the layer plots, see the design files at TIDA-00320.

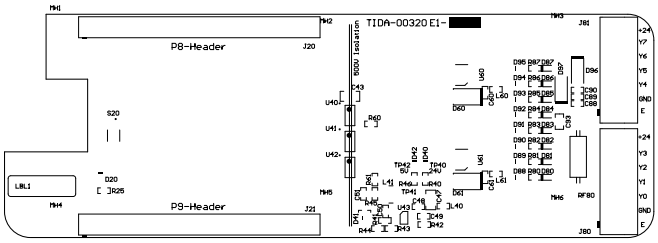

Figure 21. Top Silkscreen

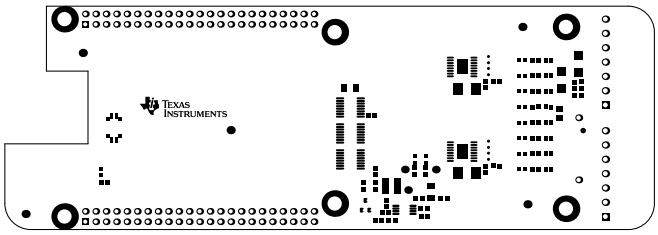

Figure 22. Top Solder Mask

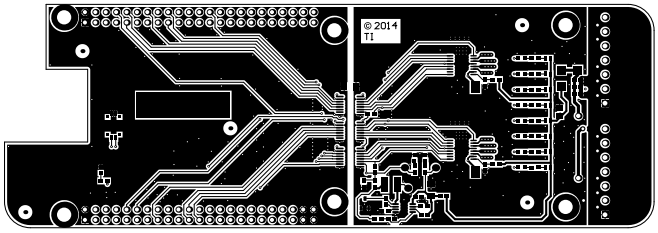

Figure 23. Top Layer

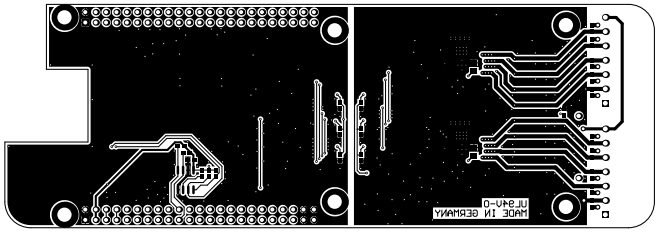

Figure 24. Bottom Layer

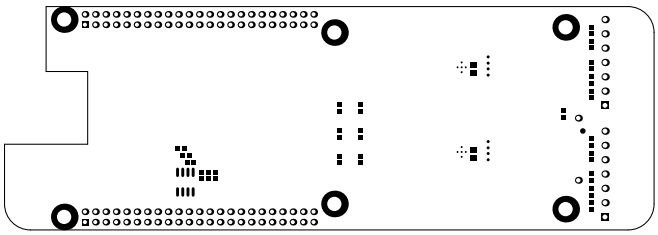

Figure 25. Bottom Solder Mask

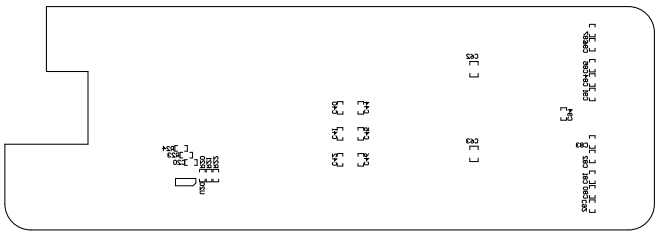

Figure 26. Bottom Silkscreen

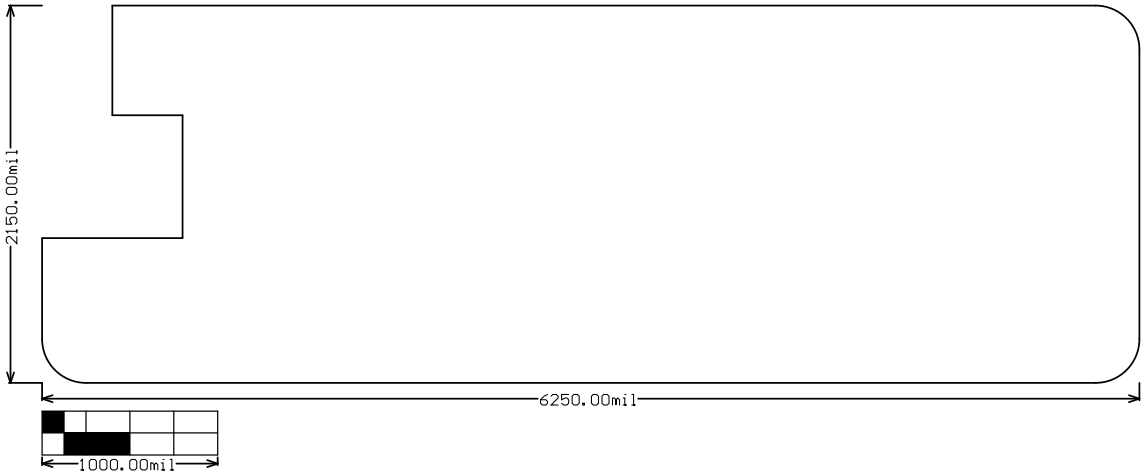

Figure 27. Mechanical Dimensions

8.4 Altium Project

To download the Altium project files, see the design files at TIDA-00320.

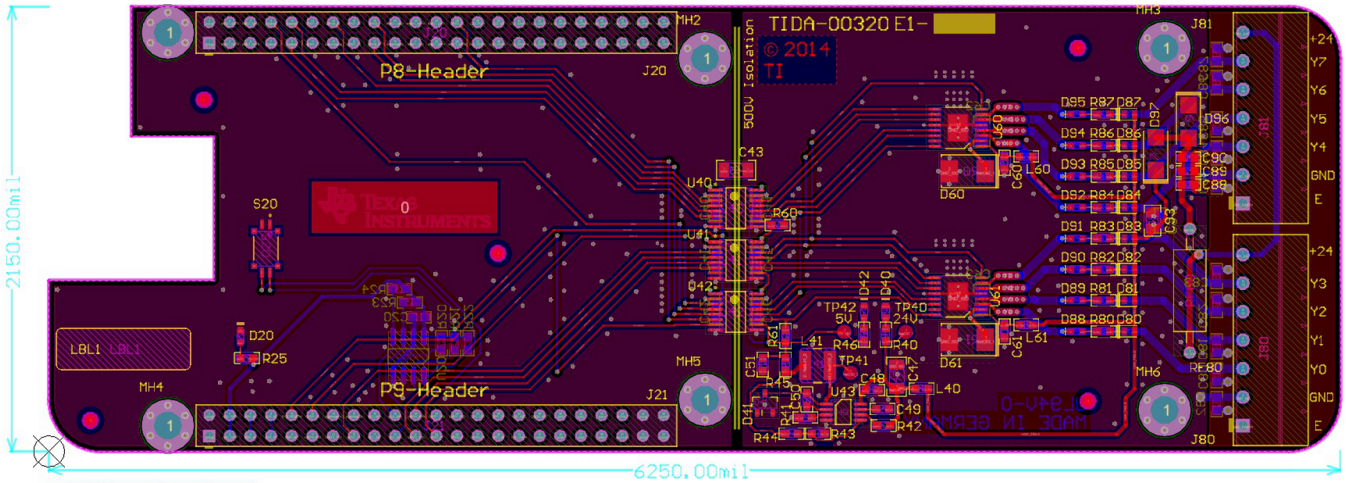

Figure 28. Multilayer Composite Print

8.5 Gerber Files

To download the Gerber files, see the design files at TIDA-00320.

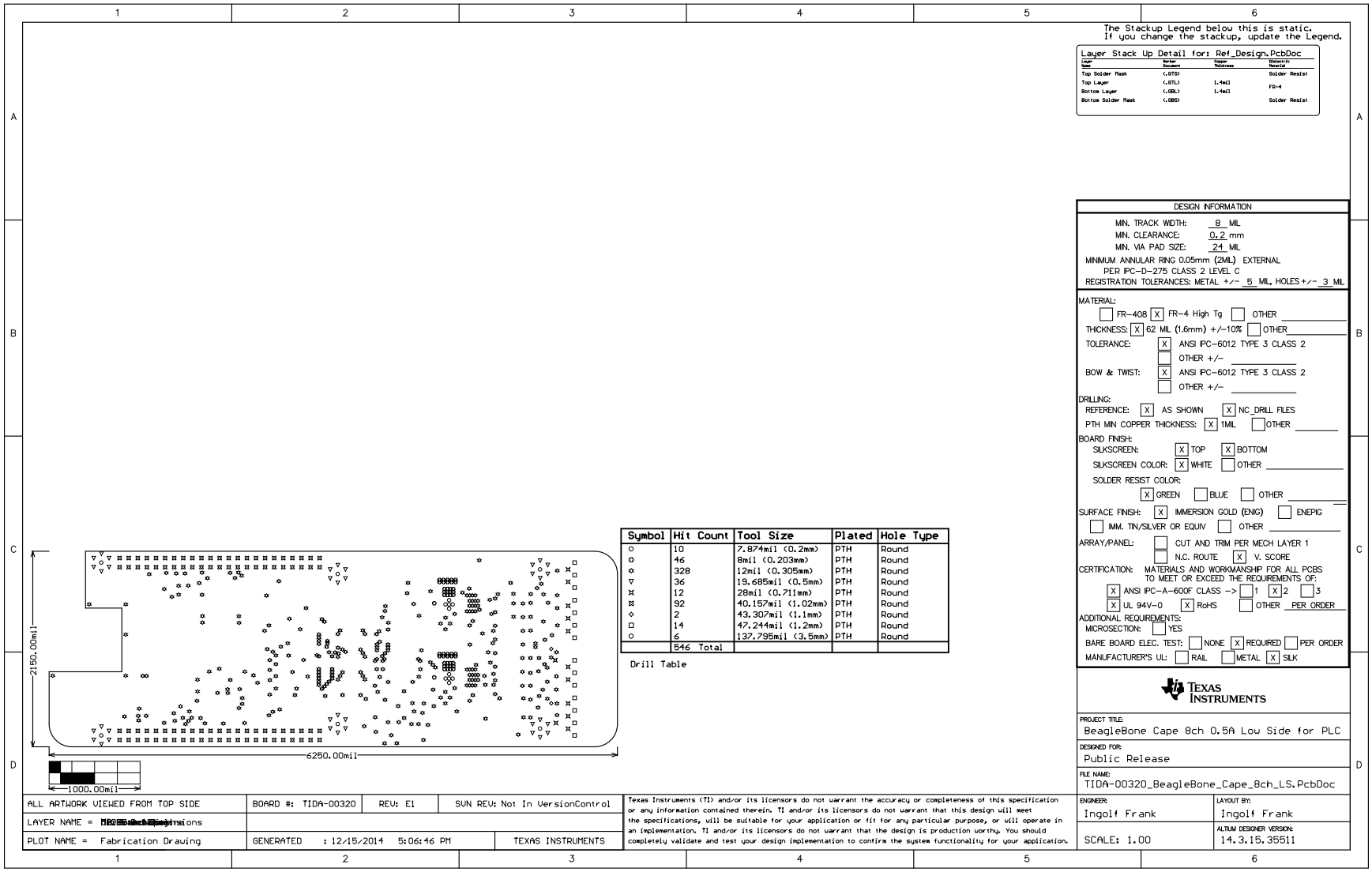

Figure 29. Fabrication Drawing

8.6 Assembly Drawings

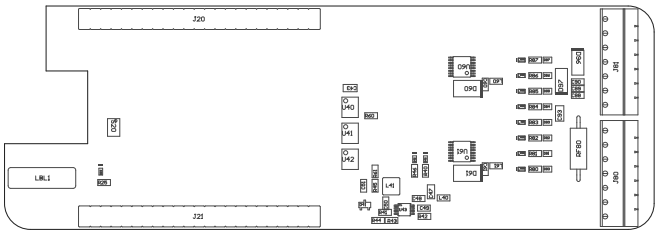

Figure 30. Top Assembly Drawing

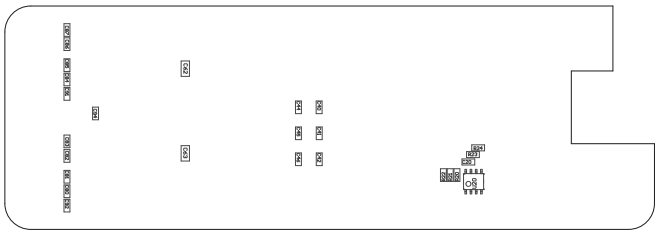

Figure 31. Bottom Assembly Drawing

8.7 Software Files

To download the software files, see the design files at TIDA-00320.

9 References

1. Texas Instruments, *Low Side 0.5-A, 8-Ch Digital Output Module for PLC*, TIDA-00236 Design Guide (TIDU470)
2. Charles Mauney, Texas Instruments, *Thermal Considerations for Surface Mount Layouts* (PDF)

10 About the Author

INGOLF FRANK is a systems engineer in the Texas Instruments Factory Automation and Control team, focusing on PLC I/O modules. Ingolf works across multiple product families and technologies to leverage the best solutions possible for system-level application designs. Ingolf earned his electrical engineering degree (Dipl. Ing. (FH)) in the field of information technology at the University of Applied Sciences Bielefeld, Germany in 1991.

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Revision History

Changes from Original (January 2015) to A Revision	Page
• Changed preview page to completed design guide	1

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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