Test Data
For PMP10531
11/20/2014

Overview

The PMP10531 reference design is an 8-output isolated Fly-Buck power supply for IGBT gate driver in motor drive or high voltage inverter applications.

It takes 24V nominal input and provides 4 isolated sets of (+15V, -8V) bias voltage. The board is designed to provide driver bias power for 6 IGBTs in 3-phase configuration: 3 sets of outputs for the 3 top side IGBTs with 100mA output current, and 1 set of 300mA outputs for all the bottom IGBTs. Each set of the positive and negative rails is generated from one single transformer winding using the voltage split circuit formed by a Zener diode and a resistor. With the voltage split circuit, the transformer size and pin count are minimized, and a compact solution size is achieved (62x62mm). The positive rail clamped by the Zener has tight regulation tolerance, which ensures the fast turn on of the IGBT. The negative rail helps securing the IGBT turn-off by holding the gate-emitter voltage to a negative potential. It prevents spurious turn-on induced by the high voltage/current swing in high power motor drive applications. An example block diagram of the system configuration can be seen in Figure 1.

The design features the LM5160 synchronous buck converter configured as a Fly-Buck regulator. With the benefit of primary side regulation, the supply has the outputs regulated without the opto-coupler or additional transformer winding. The LM5160 has a wide Vin range of 4.5V to 65V and 1.5A output current capability with integrated switch FETs. The input voltage to the reference design can be loosely regulated, and the prototype board is tested at an input range of 20V to 30V.

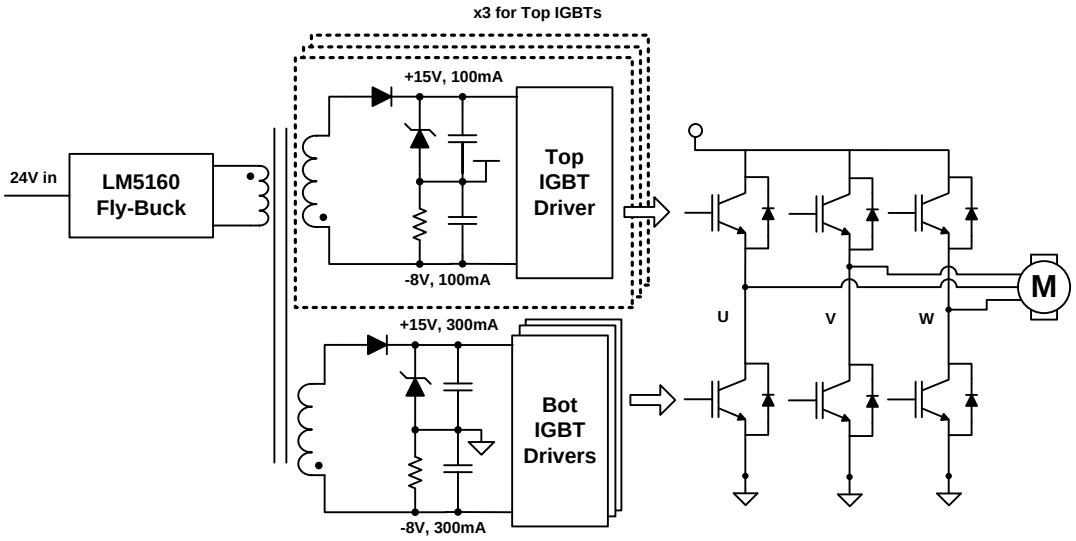

Figure 1 The Fly-Buck gate driver bias in 3-phase motor drive

Power Specification

Nominal Vin:	24V
Vin Range:	20V – 30V
Outputs:	3 sets of (+15V, -8V) @ 100mA
	1 set of (+15V, -8V) @ 300mA,
	Each output set is isolated from each other
Output Power:	13.8W max
Switching Frequency:	250 kHz

Power Supply Board

The photos of the board are shown in below. The board size is 62x62mm. The 8 outputs are grouped in positive/negative sets, and are designated to bias the IGBT gate driver circuits in 3-phase (U, V, W phase) configuration. They are configured as follows: the Vcc_U_T and Vee_U_T are the +15V and -8V, 100mA for the top side IGBT in U phase, and they can be accessed from connector JUT on the board; the Vcc_V_T and Vee_V_T are for top IGBT in V phase from JVT; the Vcc_W_T and Vee_W_T are for top IGBT in W phase from JWT. The Vcc_B and Vee_B are the 300mA outputs for the bottom IGBTs of all 3 phases, which share the common ground, and they are from connector JB.

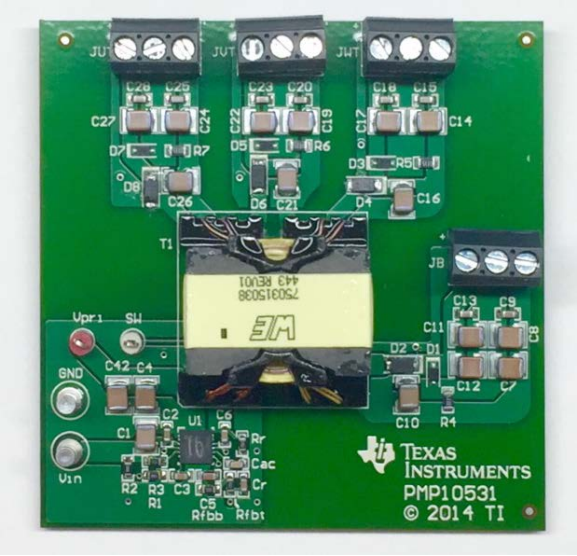

Figure 2 Board front

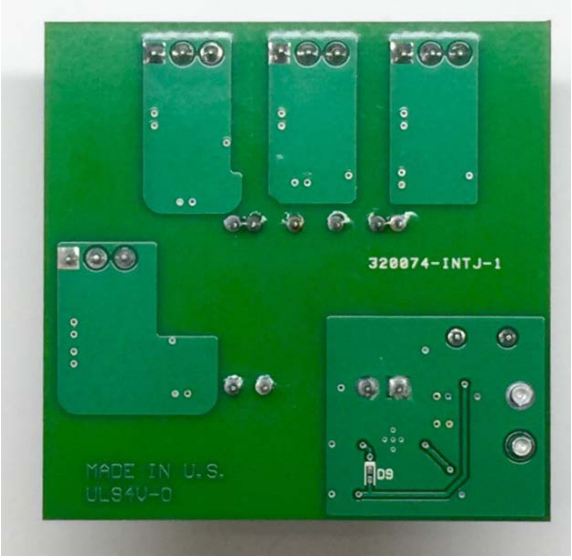

Figure 3 Board back

Efficiency

The efficiency measurement was taken as all outputs are loaded at the same percentage current in respect of their full load. The peak efficiency is about 82% occurred at full load.

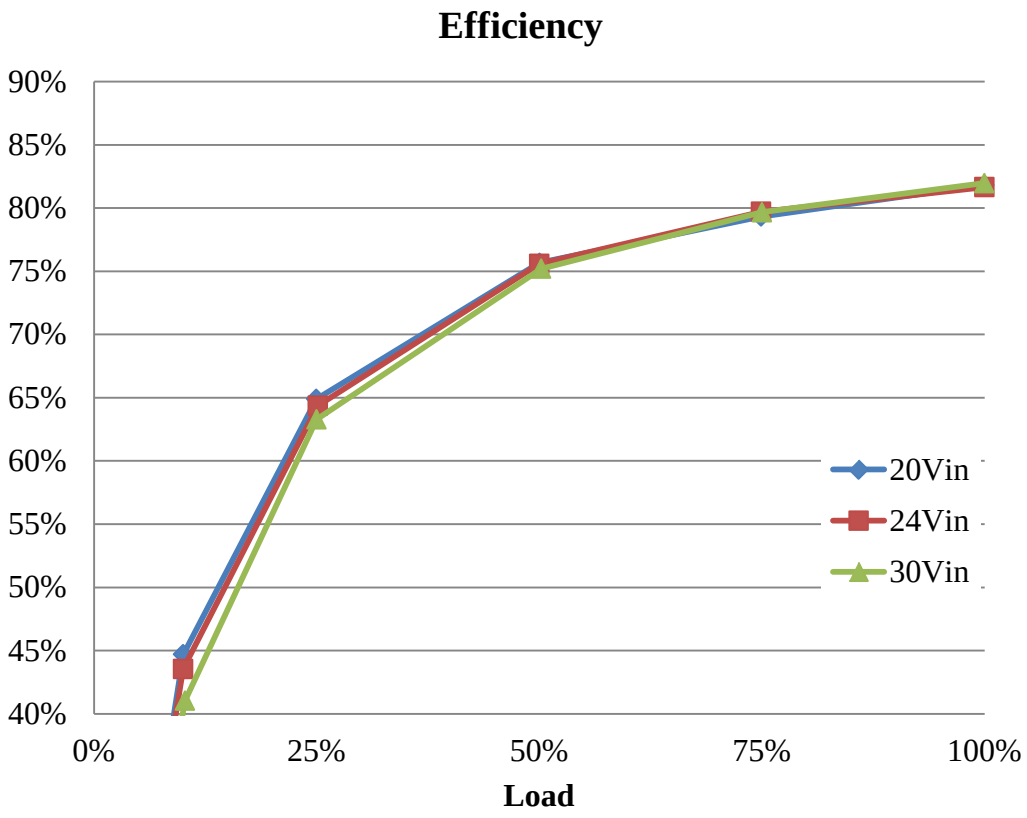

Figure 4 Total efficiency under balanced load

Cross Regulation

The regulation under balanced load condition was tested as all outputs were loaded with the same percentage of current in respect of their full load at different input voltage conditions. Since the U_T/V_T/W_T set of outputs is symmetrical to each other, only the U_T outputs are shown.

The voltage between Vcc and Vee were measured as a 23V output, as it is from one single transformer winding. As seen in Figure 5, the worst case variation on the 23V output under line/load change is about 1.69V (7.4%). The Vcc (+15V) outputs are clamped by a 15V Zener diode, and therefore the voltage level is fairly stable under all conditions (Figure 6). On the other hand, the Vee (-8V) outputs endures all the

deviation from the total 23V output, but the voltage level still holds acceptable level below -6.6V (Figure 7).

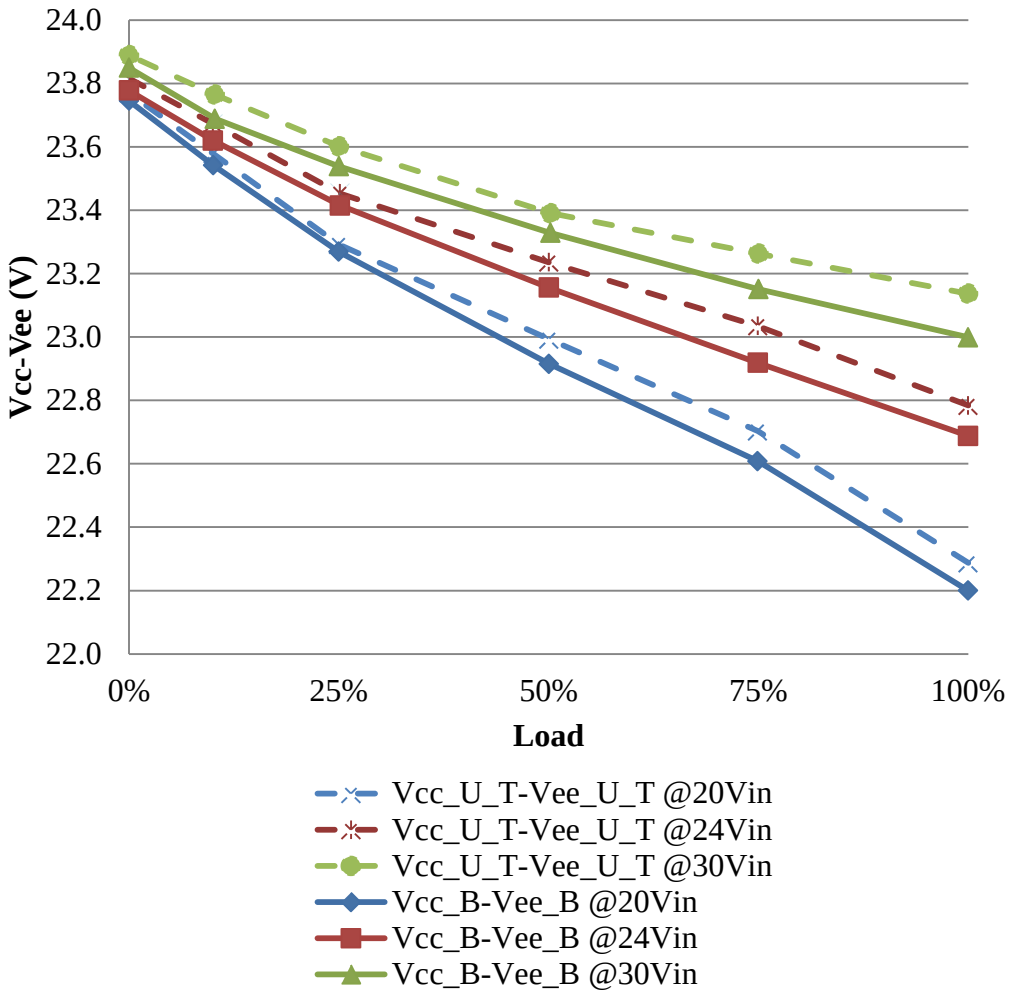

Figure 5 Vcc-Vee output regulation under balanced load

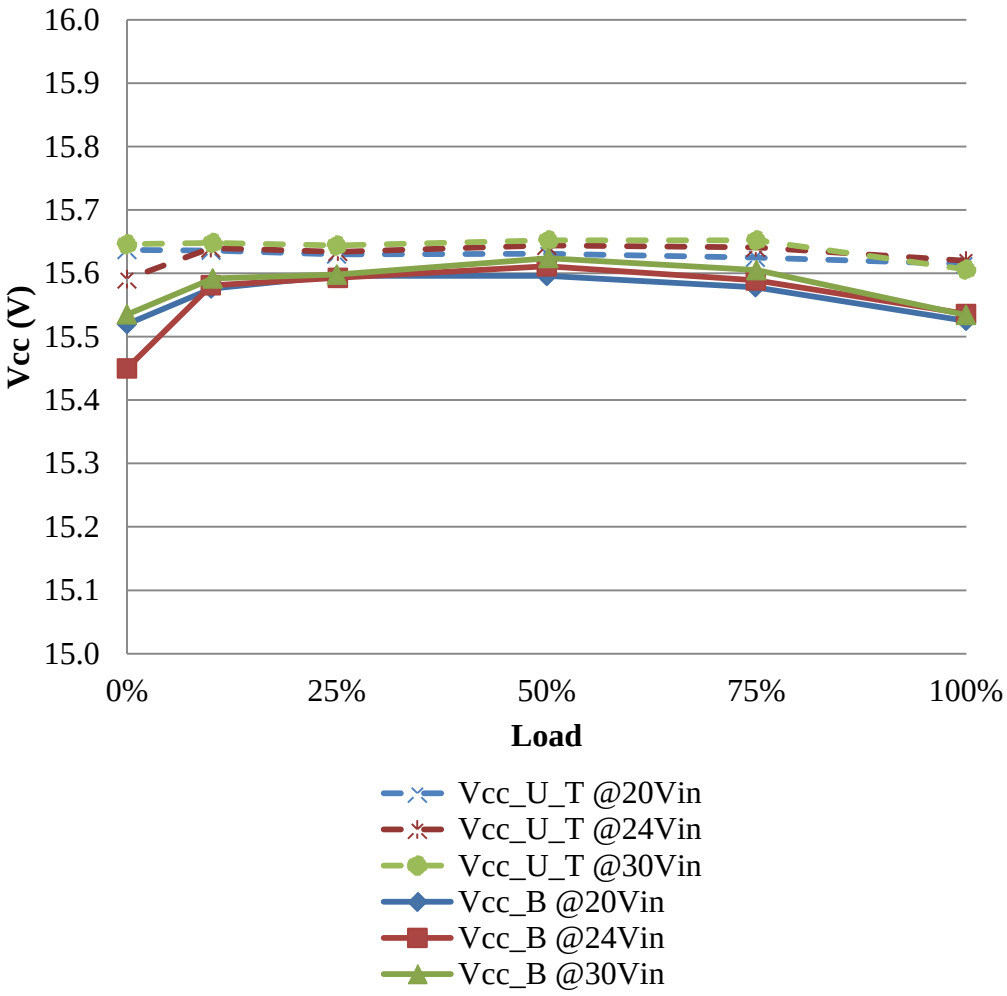

Figure 6 Vcc output regulation under balanced load

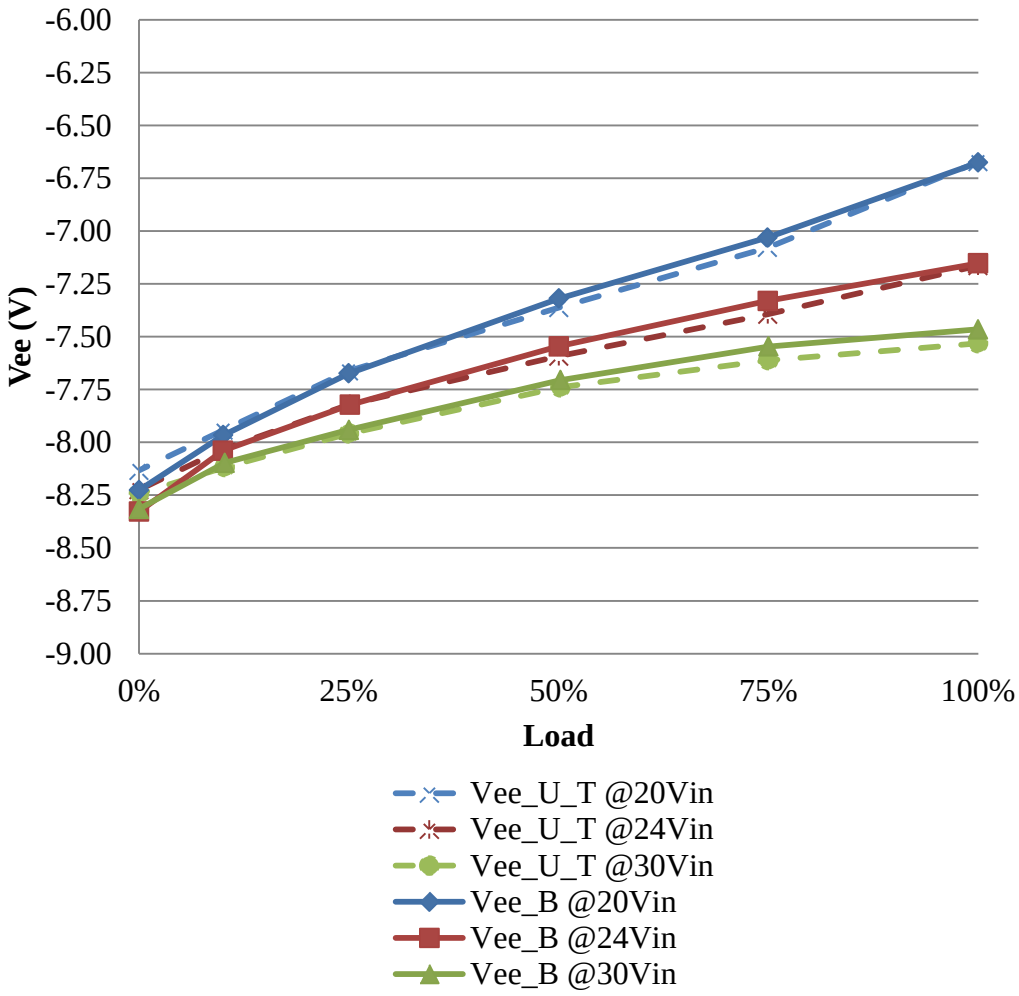

Figure 7 Vee output regulation under unbalanced load

Start Up

The board was tested under no load and full load at 24V input. The four sets of output were monitored, and they ramped up in the same matching pace. Thus, only VCC_B/VEE_B and VCC_U_T/VEE_U_T are shown here. Ch1 (yellow) is the input voltage, Ch2 (green) is the total voltage from VCC_B to VEE_B, Ch3 (purple) is the total voltage from VCC_U_T to VEE_U_T.

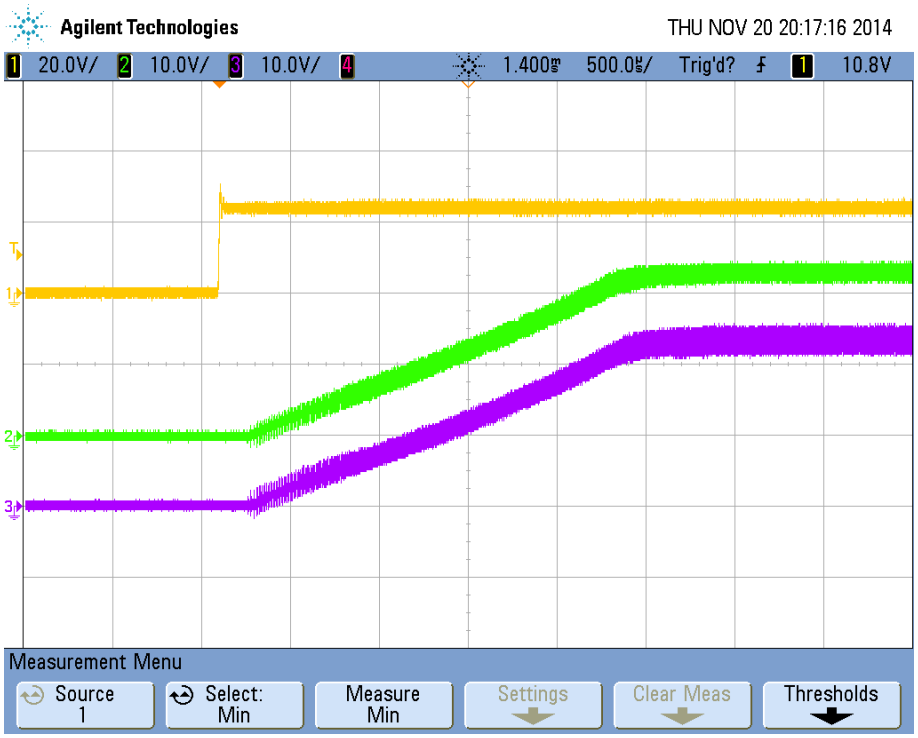

Figure 8 Start up into full load at 24Vin

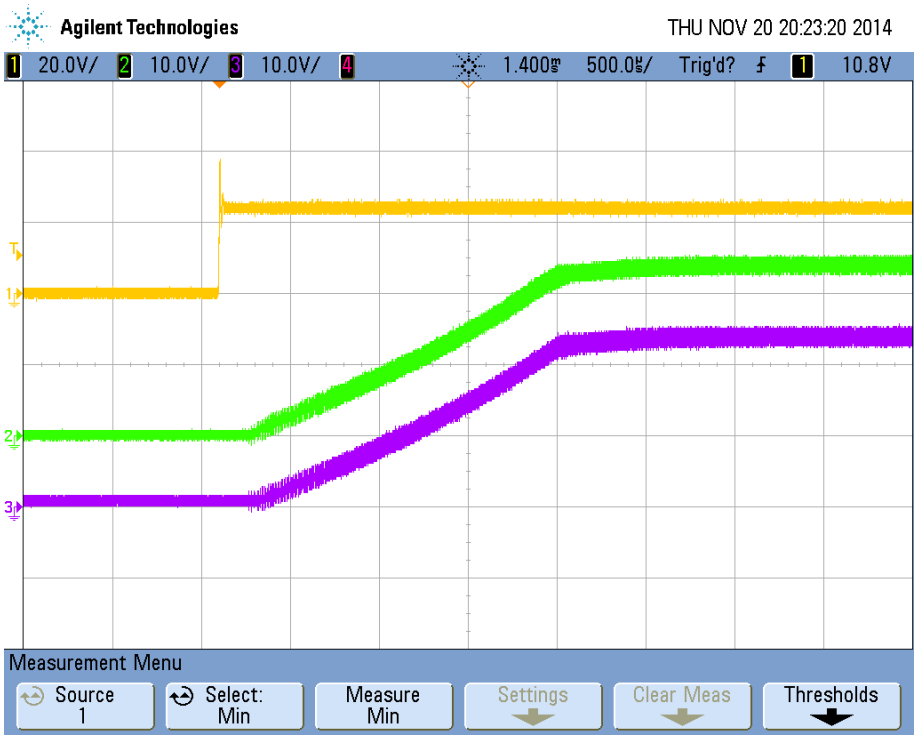

Figure 9 Start up into no load at 24Vin

In below, the waveforms show how the positive and negative rails ramp up during star-up. Ch1 (yellow) is the input voltage, Ch2 (green) is the VCC_B +15V rail, and Ch3 (purple) is the VEE_B -8V rail.

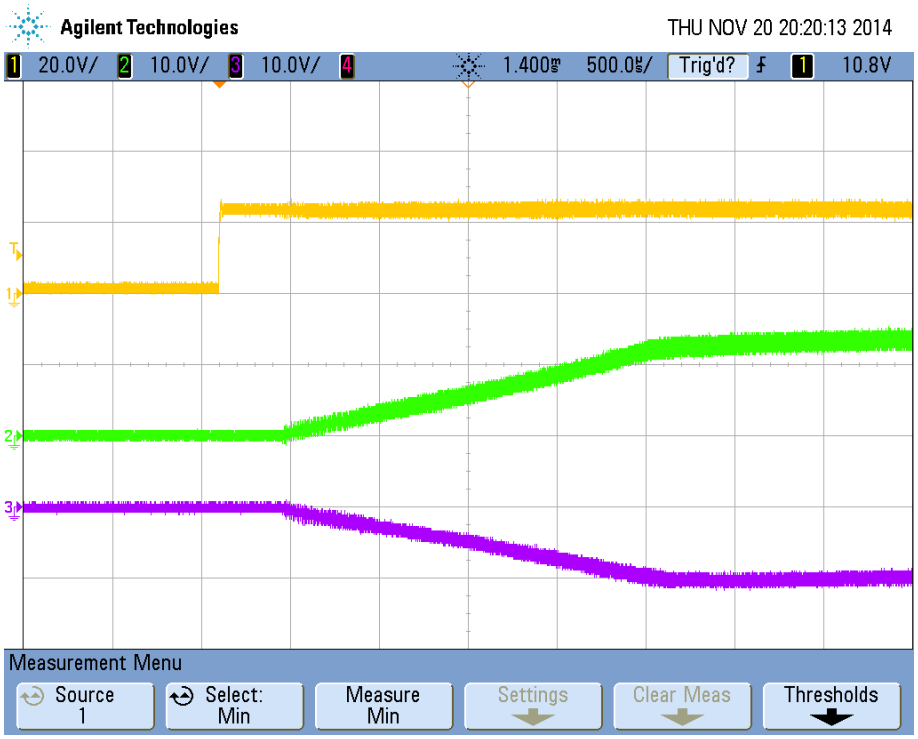

Figure 10 VCC_B and VEE_B start up into full load at 24Vin

Figure 11 VCC_B and VEE_B start up into no load at 24Vin

Switching Waveforms

The primary side switch node voltage was measured at no load and full load condition at 24V input. Ch1 (yellow) is the switch node voltage.

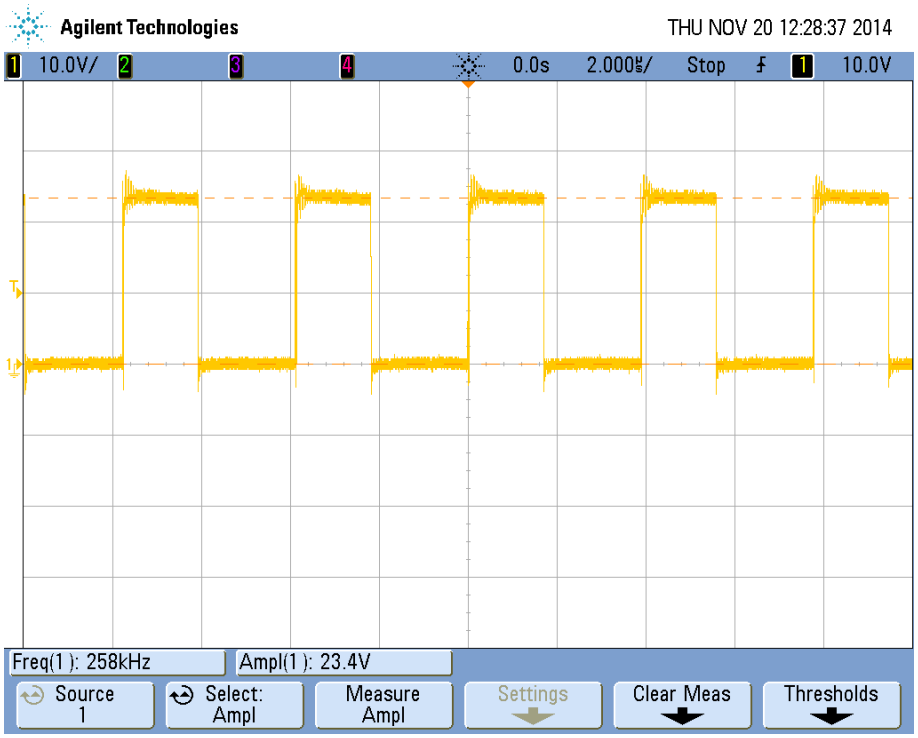

Figure 12 Switching waveform at full load, 24Vin

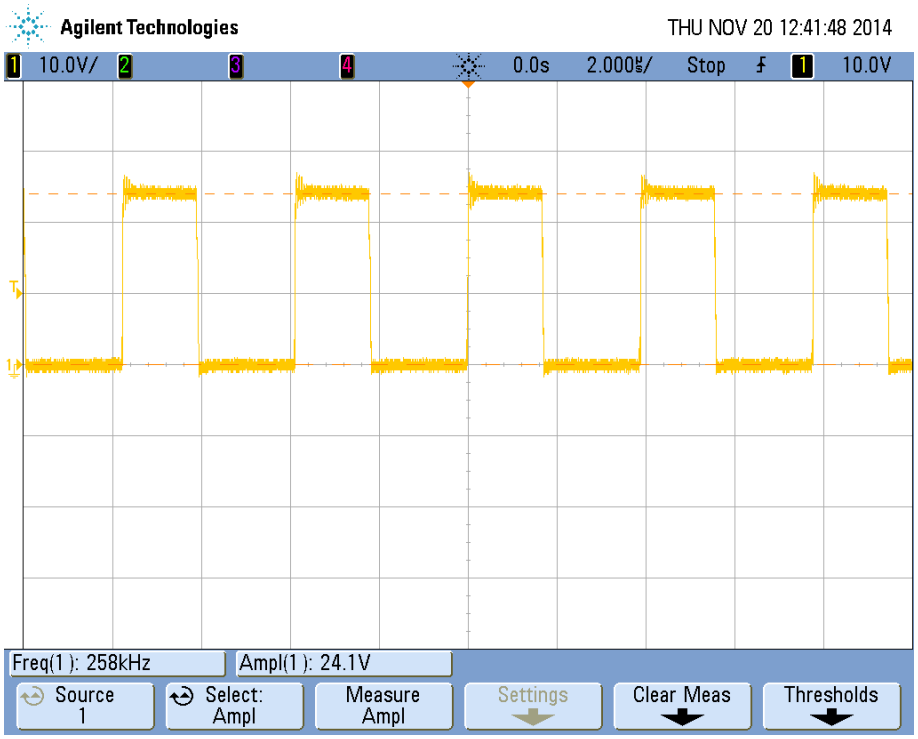

Figure 13 Switching waveform at no load, 24Vin

The secondary side diode voltage stress was checked at full load and 30V input, and they were all below the diode's 200V blocking voltage rating. The diodes of U_T, V_T and W_T output share the same test result, and only the U_T diode's is displayed. Ch1 (yellow) shows the voltage across the diode.

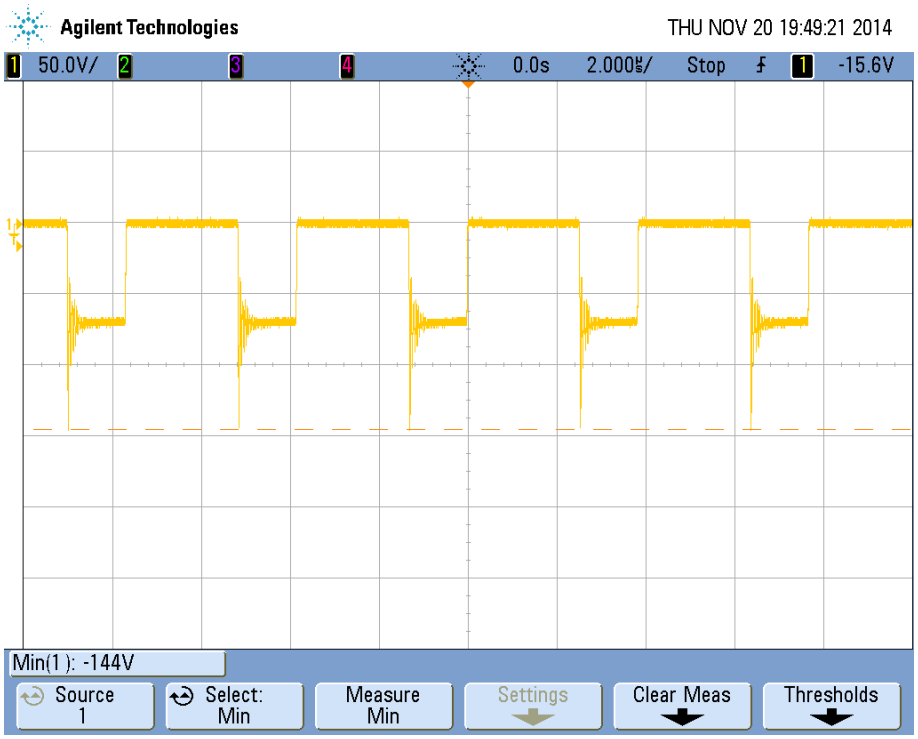

Figure 14 VCC_B and VEE_B output diode anode (+) to cathode (-) voltage at full load, 30Vin

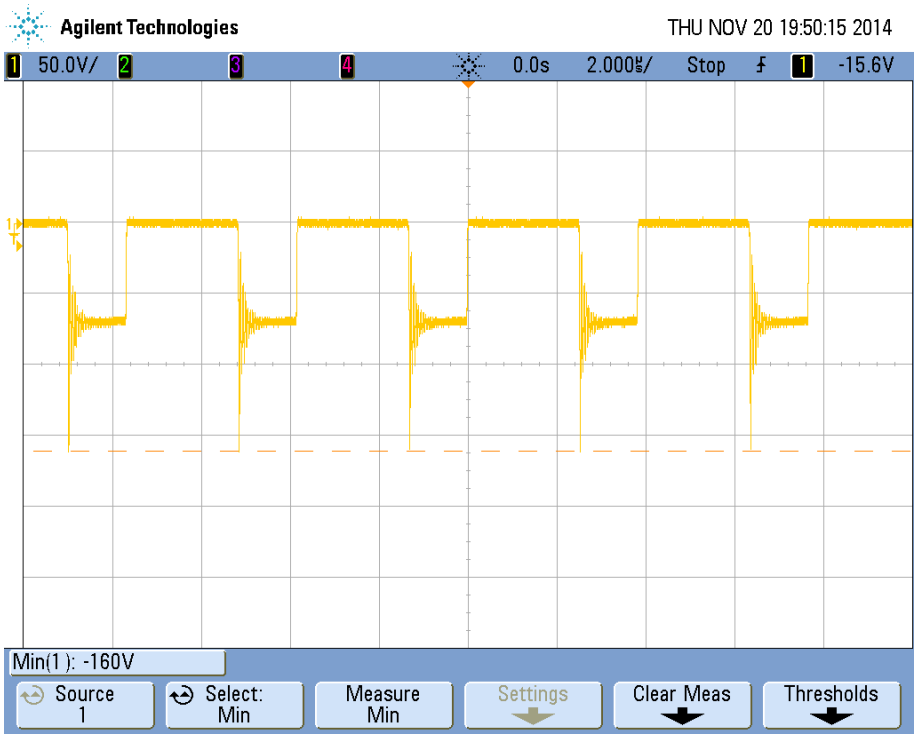

Figure 15 VCC_U_T and VEE_U_T output diode anode (+) to cathode (-) voltage at full load, 30Vin

Load Transients

The load transient response was tested by adding load step on the positive and negative output pair, treating it as one output, and the other outputs have no load. The VCC_B/VEE_B and the rest U_T, V_T and W_T outputs are tested separately. Only VCC_B/VEE_B and VCC_U_T/VEE_U_T are shown here. The Vin was set at 24V. Ch1 (yellow) is the output voltage in AC mode, and Ch4 (magenta) is the output current.

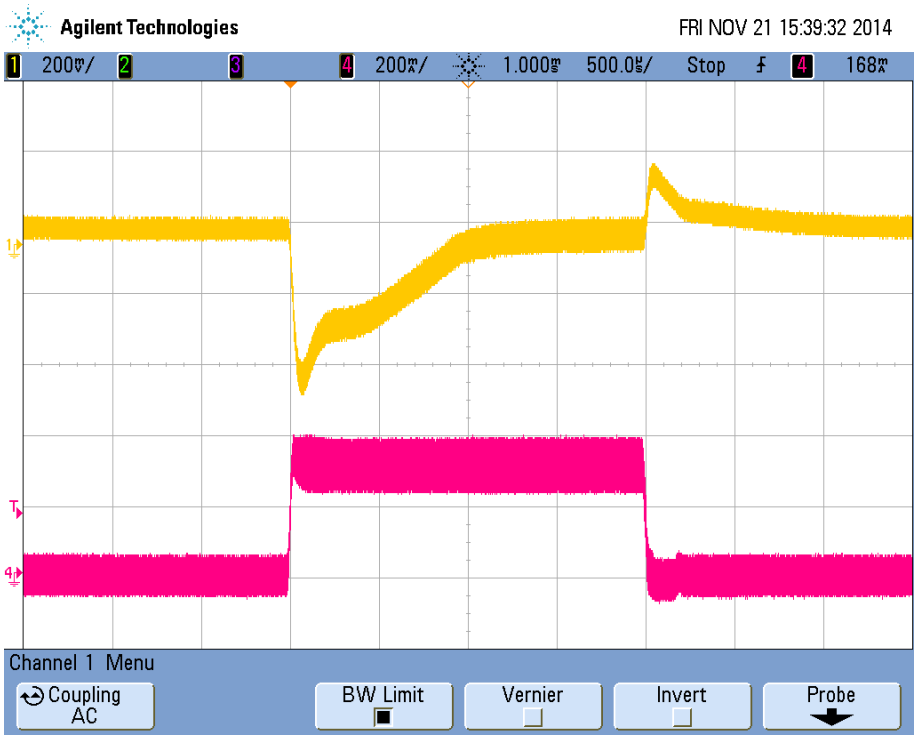

Figure 16 VCC_B output load transient

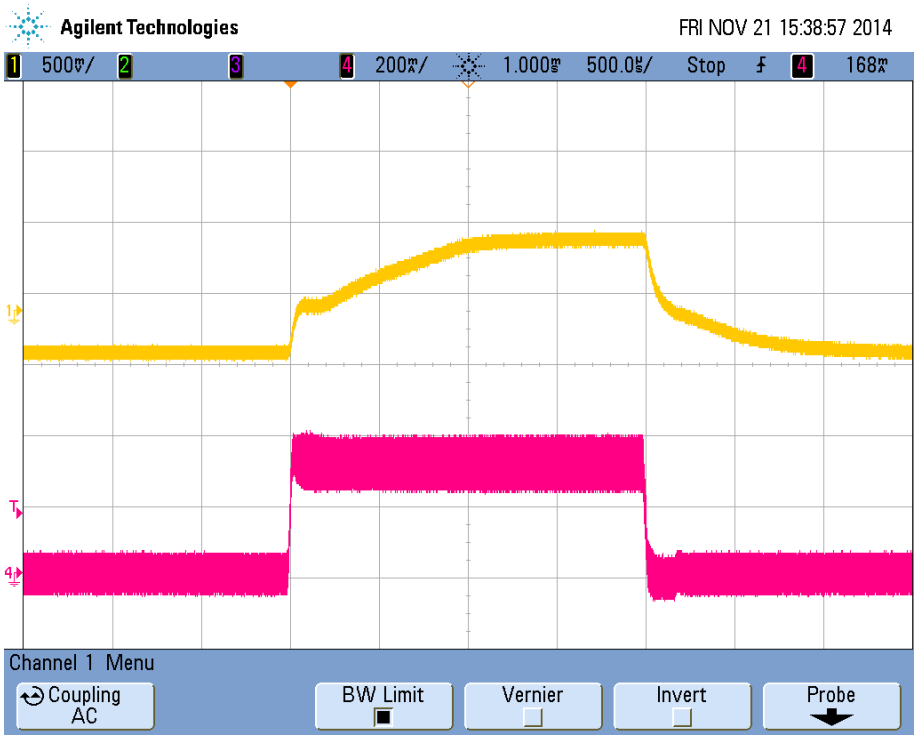

Figure 17 VEE_B output load transient

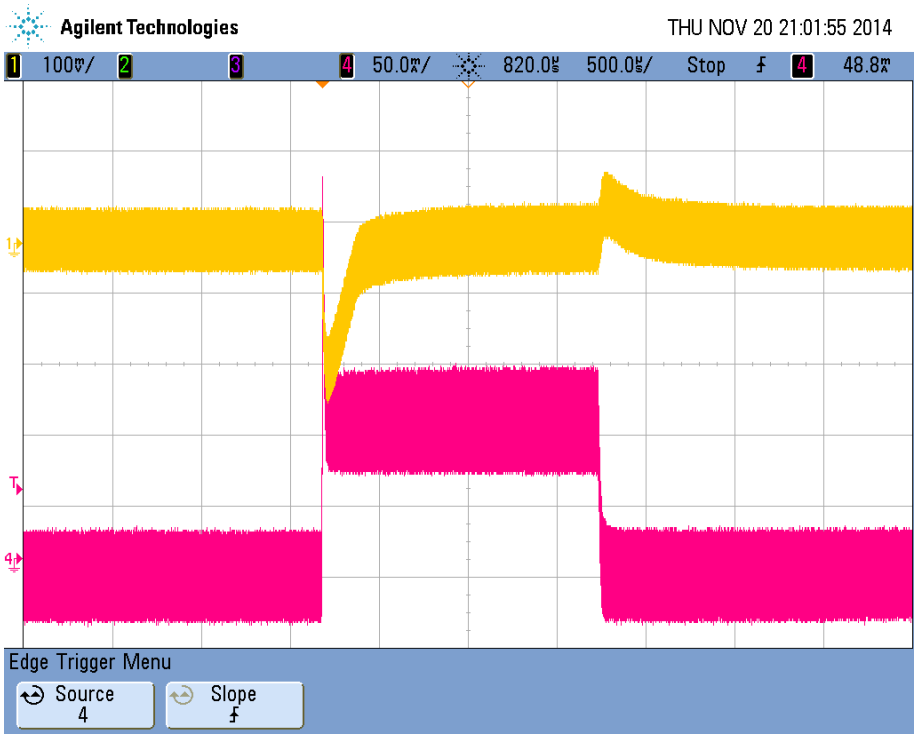

Figure 18 VCC_U_T output load transient

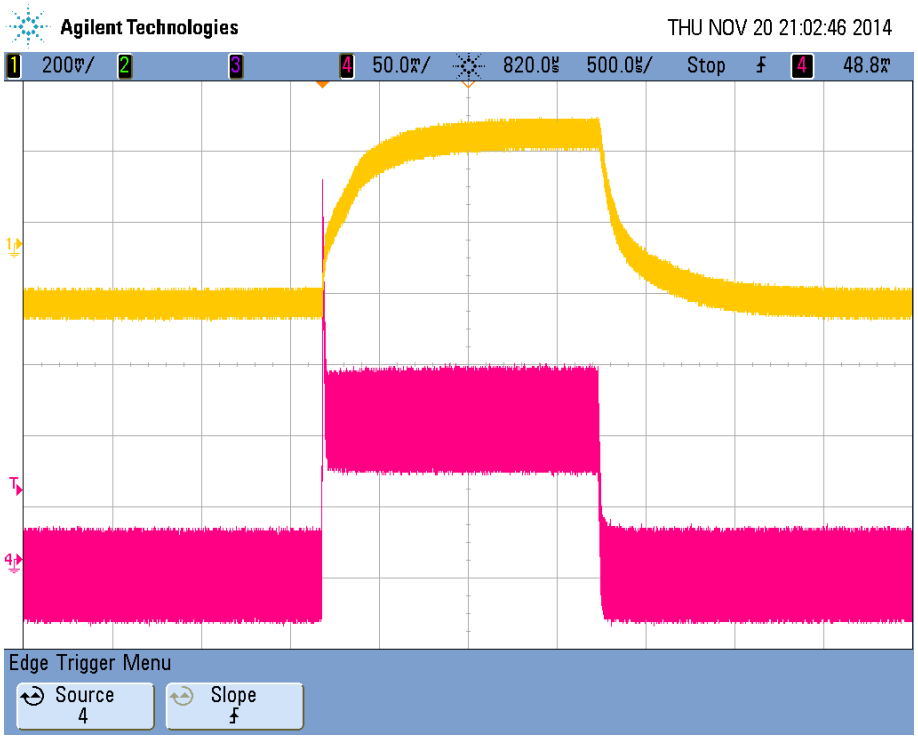

Figure 19 VEE_U _T output load transient

Output Voltage Ripples

The output ripples were measured directly at the output capacitors, when all outputs were fully loaded. The input voltage was at 24V. The U_T/V_T/W_T outputs have matching ripple results due to the symmetrical structure, and only U_T is shown. In the scope shots, Ch1 (yellow) is the correspondent output ripple in AC mode.

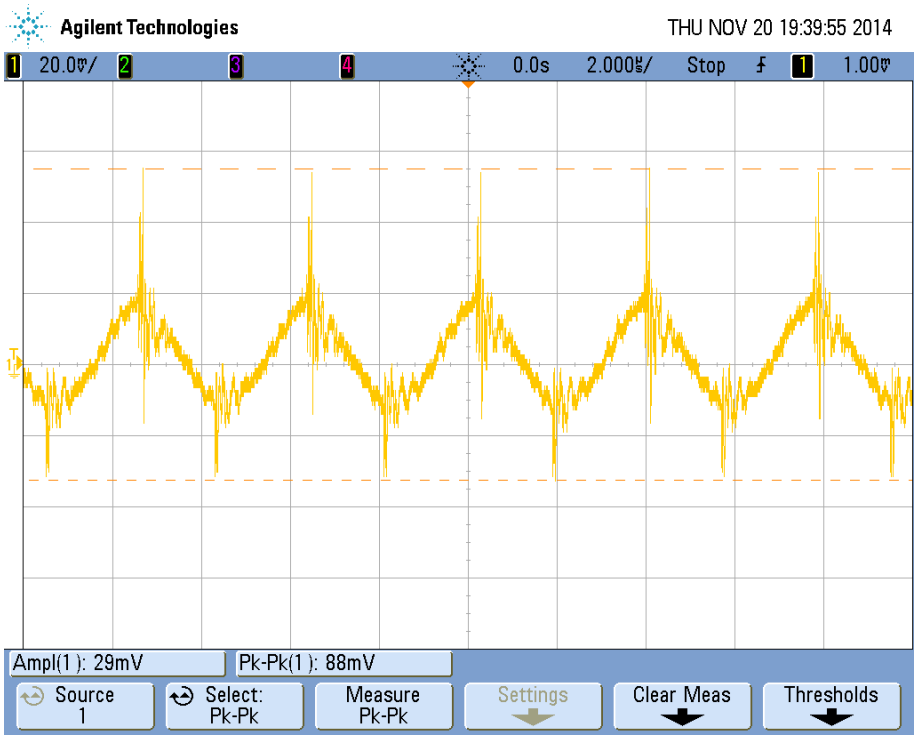

Figure 20 VCC_B output ripple at full load, 24Vin

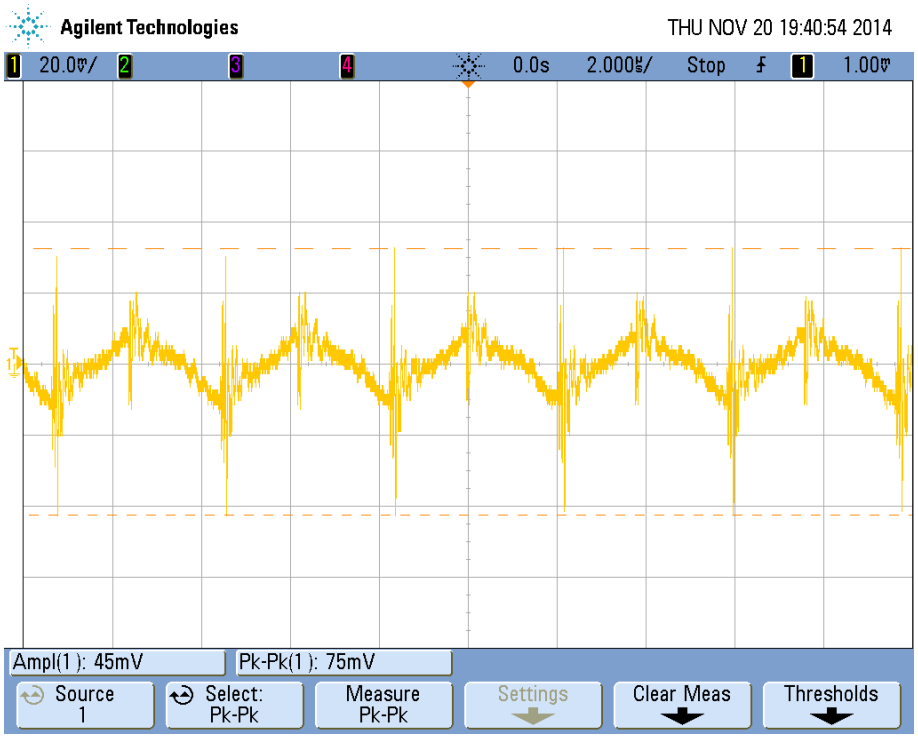

Figure 21 VEE_B output ripples at full load, 24Vin

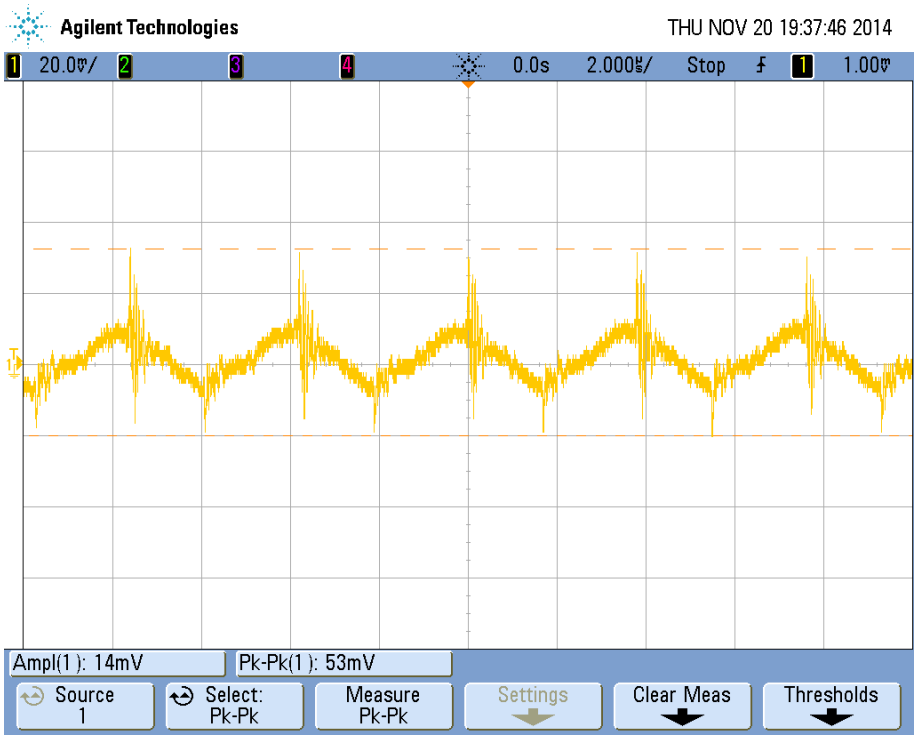

Figure 22 VCC_U_T output ripple at full load, 24Vin

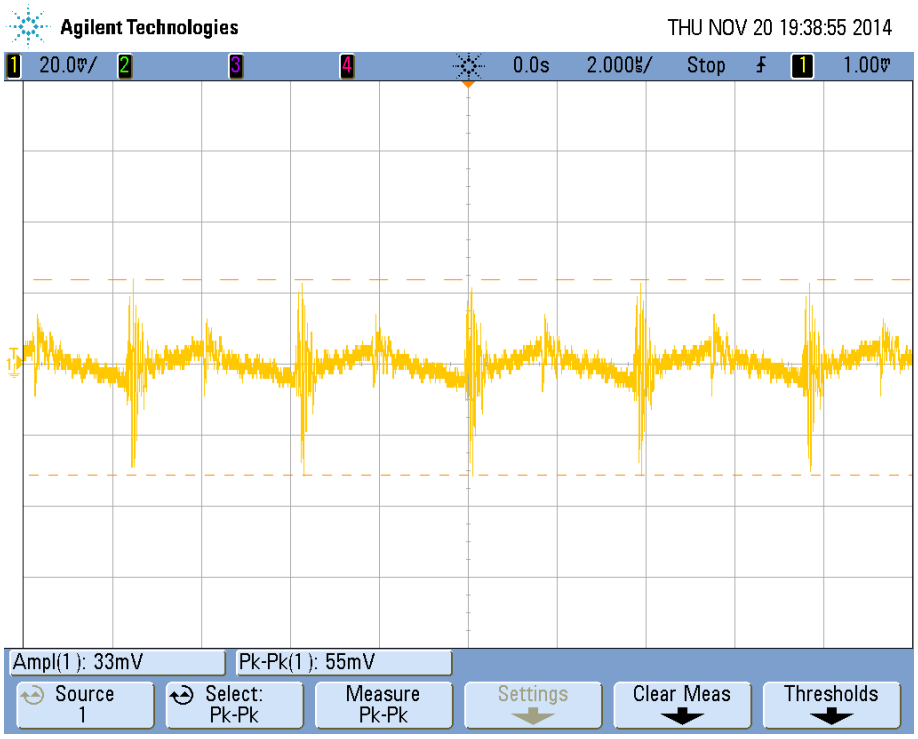

Figure 23 VEE_U_T output ripples at full load, 24Vin

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