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Wide-Input Isolated IGBT Gate-Drive Fly-Buck™ Power Supply for Three-Phase Inverters

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Design Resources

TIDA-00199	Design Page
LM5160	Product Folder
ISO5500EVM	Tool Folder
C2000 Piccolo LaunchPAD™	Tool Folder

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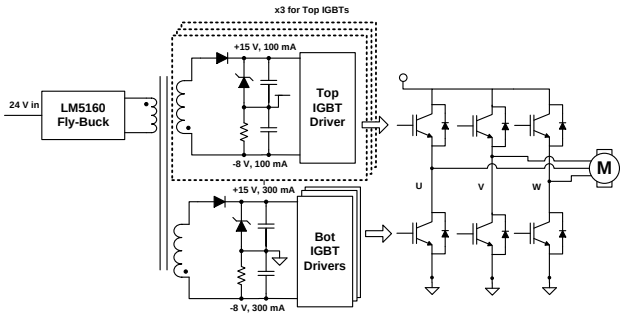
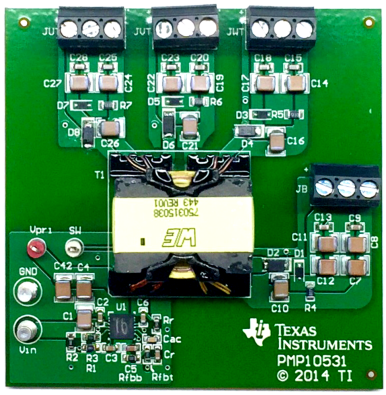
Design Features

- Isolated Power Supply for Insulated-Gate Bipolar Transistor (IGBT) Gate Drive
- Supports Six IGBT Gate Drivers for 3-Phase Inverter (Each Arm in Half-Bridge Configuration)
- Positive and Negative, Low-Ripple (< 200 mV) Bias Outputs for Each IGBT of Three-Phase Inverter: 15 V and –8 V
- Operates With 24-V ±20% Input Range
- Fly-Buck Topology Provides Easy-to-Design Multi-Output Isolated Power Supply Solution With Primary Side Regulation
- Output Power: 2.3 W Per IGBT
- Peak Efficiency of 82% at Balanced Full-Load
- Output Capacitors Rated to Support Up to 6-A Peak Gate Drive Currents
- Design Validated With TI's Isolated Gate-Driver ISO5500 Driving IGBTs

Featured Applications

- Variable Speed AC and DC Drives
- Industrial Inverters and Solar Inverters
- UPS Systems
- Servo Drives
- IGBT Based High-Voltage DC (HVDC) Systems





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1 System Description

The TIDA-00199 reference design provides positive and negative voltage rails required for insulated-gate bipolar transistor (IGBT) gate drivers. IGBTs are used in three phase inverters for variable-frequency drives to control the speed of AC motors. This reference design uses a Fly-Buck topology and is intended to operate from an unregulated 24-V DC input. The Fly-Buck converter circuit can be deemed a combination of a buck converter on the primary side and a flyback-like secondary side. The isolated outputs generate through the coupled windings of the transformer. The Fly-Buck has a primary side regulation and can achieve a good cross regulation without opto-coupler feedback or auxiliary winding. This reference design is implemented with LM5160, awide-input constant on-time (COT) synchronous buck regulator. This reference design is capable of operating from a loosely regulated 24-V DC input and generates four pairs of 15-V and –8-V outputs suitable for powering six IGBT gate drivers.

This reference design uses a single transformer for generating power rails for all three arms of the 3-phase inverter. The voltage rails for all the TOP IGBTs are isolated, whereas the voltage rails for all bottom IGBTs are combined together.

Three-phase inverters function as variable-frequency drives to control the speed of AC motors and for high power applications such as HVDC power transmissions. The typical application of a three-phase inverter using six isolated gate drivers is shown in Figure 1. Note that each phase uses a high-side and a low-side IGBT switch to apply positive and negative high-voltage DC pulses to the motor coils in an alternating mode. High-power IGBTs require isolated gate drivers to control their operations. Each IGBT is driven by a single isolated gate driver that galvanically isolates the high-voltage output from the low-voltage controlled inputs. The emitter of the top IGBT floats, which makes the use of an isolated gate-driver necessary. To isolate the high-voltage circuit with a low-voltage control circuit, isolated gate-drivers are used to control the bottom IGBTs.

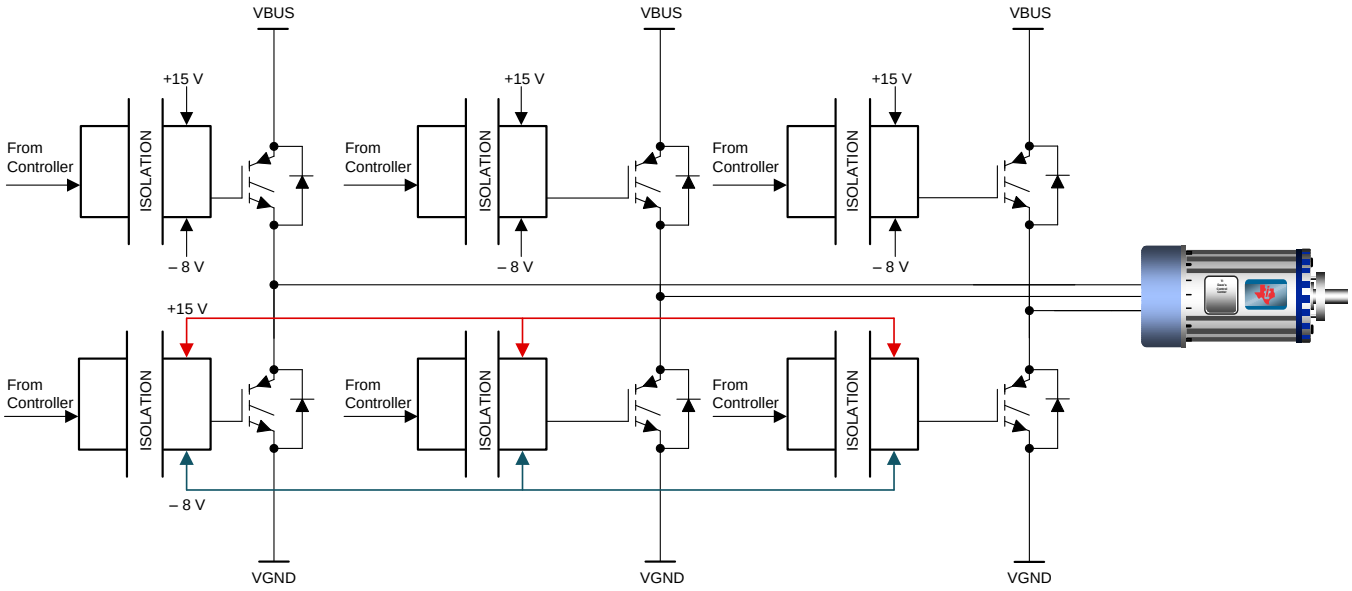

Figure 1. 3-Phase Inverter With Isolated Gate-drive

1.1 Gate-Drive Supply Requirements

To reduce conduction losses, the gates of the IGBTs are supplied with a much higher voltage than the actual gate-threshold voltages. Typically, 15 V to 18 V is applied at the gate to reduce the $V_{CE(on)}$.

The IGBT is a minority-carrier device with high-input impedance and the capacity to carry a large, bipolar current-carrying capability. The switching characteristics of an IGBT are quite similar to that of a power MOSFET. Assuming identical conditions, IGBTs and MOSFETs function identically when turned on and both have similar current rise and voltage fall times. However, the waveforms of the switched current are different at turn-off.

At the end of the switching event, the IGBT has a tail current, which does not exist for the MOSFET. This tail is caused by minority carriers trapped in the base of the bipolar output section of the IGBT, which causes the device to remain turned on. Unlike a bipolar transistor, it is not possible to extract these carriers to speed up the switching, as there is no external connection to the base; so the device remains turned on until the carriers recombine.

This tail current increases the turn-off losses and requires an increase in the dead time between the conduction of two devices in a half-bridge circuit. To reduce the turn-off time, it is helpful to have a negative voltage (–5 V to –10 V) at the gate.

When an IGBT is turned on, some voltage spikes are generated on the gate terminal due to the high dv/dt and parasitic capacitance between the gate and emitter. The voltage spikes can trigger a false turn-on of the bottom IGBT. A negative voltage at the gate helps to avoid this false turn-on trigger.

Deciding on the power requirement to drive the IGBT is important. The calculation of the gate-drive power requirement for different power ratings of variable speed drives is explained in Equation 1.

As noted earlier, an isolated gate driver is used to turn the IGBT on and off. In this process, power is dissipated by the driver IC, IGBT gate, and by any RC circuits in the gate drive path. Refer to Figure 2.

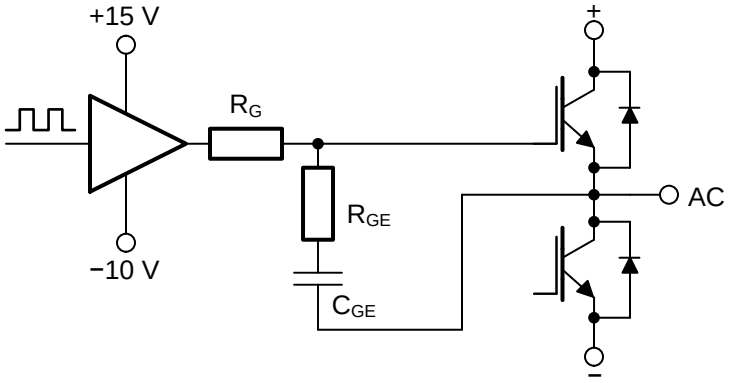

Figure 2. IGBTs With Gate Drive Circuitry for Gate Power Calculation

Equation 1 calculates the total gate power dissipation:

$$P_{gate} = P_{driver} + (Q_{gate} \times f_{sw} \times \Delta V_{gate}) + (C_{ge} \times f_{sw} \times \Delta V_{gate}^{2}) \quad (1)$$

where

- Q_{gate} = Total gate charge.
- F_{sw} = Switching frequency.
- ΔV_{gate} = Gate driver output voltage swing.
- C_{ge} = External gate-to-emitter capacitance.
- P_{driver} = Gate-driver total power consumption.

Note that the second term in Equation 1 reflects the power requirement for IGBT gate capacitance and the third term reflects the power requirement for an additional external capacitance, as Figure 2 shows.

Consider the following example:

- An IGBT module with a 1200-V, 200-A capacity (applicable for < 100-kW drives) with Q_{gate} = 1.65 µC
- Switching frequency of 16 kHz, which is on the higher side for typical high power drives
- A gate voltage, swinging from –15 V to +15 V (values are a worst-case scenario because IGBTs are typically driven with 15 V and either –5 V or –8 V)
- C_{ge} = 20 nF (typical value ranges between 1 nF and 20 nF)
- P_{driver} = approximately 600 mW (estimated using the typical data sheet of an isolated IGBT gate-driver)

Using the values above:

$$P_{gate} = 0.6\ W + 0.792\ W + 0.288\ W = 1.68\ W \quad (2)$$

Considering the de-rating, the power in Equation 2 must be rounded up to 2 W / IGBT.

2 Design Features

The primary objective of this design is to provide an isolated power supply that can operate from an unregulated input supply. The design provides four isolated sets of (15 V, –8 V) bias voltage. The board is designed to provide driver bias power for six IGBTs in three-phase configurations: three sets of outputs for the three top side IGBTs with 100-mA output currents, and one set of 300-mA outputs for all of the bottom IGBTs. Each set of the positive and negative outputs are generated from a voltage split circuit of the Zener diode and a resistor from one single transformer winding with a 23-V voltage output. With the voltage split circuit, the transformer size and pin count are minimized, and a compact solution size is achieved (62 x 62 mm). The positive rail clamped by the Zener has a tight regulation tolerance, which ensures the fast turn-on of the IGBT. The negative rail helps to secure the IGBT turn-off by holding the gate-emitter voltage to a negative potential. The negative rail prevents spurious turn-ons induced by the high-voltage current swing in the high-power motor drive. The design features the LM5160 synchronous-buck converter configured as a Fly-Buck regulator. With the benefit of primary side regulation, the supply regulates the outputs without the opto-coupler or additional transformer winding. The LM5160 device has a wide V_{IN} range of 4.5 V to 65 V and a 1.5-A output-current capability with integrated high-side and low-side MOSFETs. The input voltage of the design can be loosely regulated and the design is tested at an input range of 20 V to 30 V.

2.1 Design Requirements

The system-level requirements for this design include:

- A pulse-width modulation (PWM) controller and a topology that can work with a dc input voltage that is loosely regulated and helps to scale the output power, while driving high power IGBTs
- Isolated positive and negative rails that must be 15 V and –8 V to power the isolated gate driver and the gates of the IGBTs
- Continuous output power of at least 2 W to drive each IGBT
- Support of up to 6-A peak currents with an output voltage ripple of less than 200 mV

2.2 Topology Selection

The traditional isolated switched power topologies such as push-pull, flyback, and forward converters are widely used for the gate drive bias supply. The output regulation of these solutions often relies on either open-loop, fixed-duty cycle switching or a closed-loop control for the auxiliary winding feedback. The disadvantages of using an open-loop control are that the line and load transient responses are poor and the open-loop control requires the input DC voltage to be tightly regulated (or needs post-regulation, low drop-out voltages (LDOs)). For the auxiliary winding feedback method, the cross regulation between multiple outputs is not optimal; however, the Fly-Buck topology has the inherent primary-side regulation feature and can achieve isolated output regulation effortlessly. The cross-regulation performance is better overall between outputs. There are also benefits from a cost perspective to having one transformer generate all of the isolated rails to feed the gate driver. The requirements of the PWM controller and transformer are listed in Section 2.2.1 and Section 2.2.2.

2.2.1 PWM Controller Requirements

The PWM controller requires the following:

- Support for Fly-Buck topology
- Support for primary-side regulation
- Operation from a 24-V supply

2.2.2 Transformer Specifications (as per IEC61800-5-1)

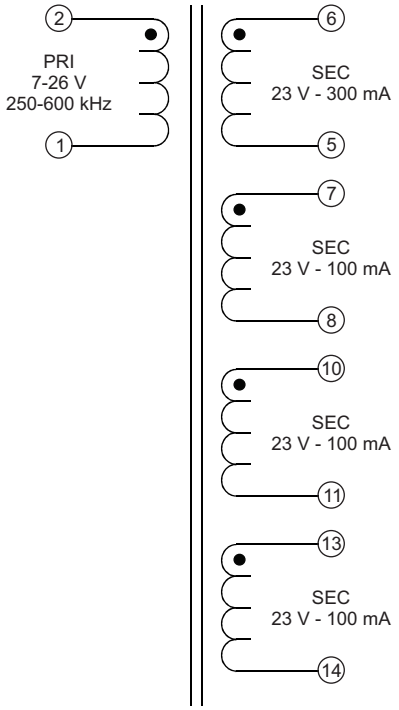

Figure 3. Fly-Buck Transformer Symbol for TIDA-00199

The transformer requires the following:

- Four 23-V isolated outputs: one with 300 mA and three with 100 mA each
- Switching frequency = 250 kHz
- Isolation voltage:
  - Primary to secondary, 3600-V AC for 5 seconds
  - Secondary to secondary, 1800-V AC for 5 seconds
- Spacings:
  - Primary to secondary clearance = 8 mm
  - Secondary to secondary clearance = 5 mm
  - Creepage distance = 4 mm
- Basic insulation between windings

The above spacing, creepage, and impulse test voltages are determined by considering the basic isolation. If the drive architecture requires only functional isolation, the transformer can be redesigned. Lower levels of spacing and creepage values significantly reduce the size of the transformer.

3 Block Diagram

This reference design is intended for motor control, industrial inverters, and many other applications where IGBT drivers are used and should significantly help to reduce design time while meeting all of the design requirements. The design files include schematics, Bill of Materials (BOM), layer plots, Altium files, Gerber Files, and test results. The block diagram is shown in Figure 4.

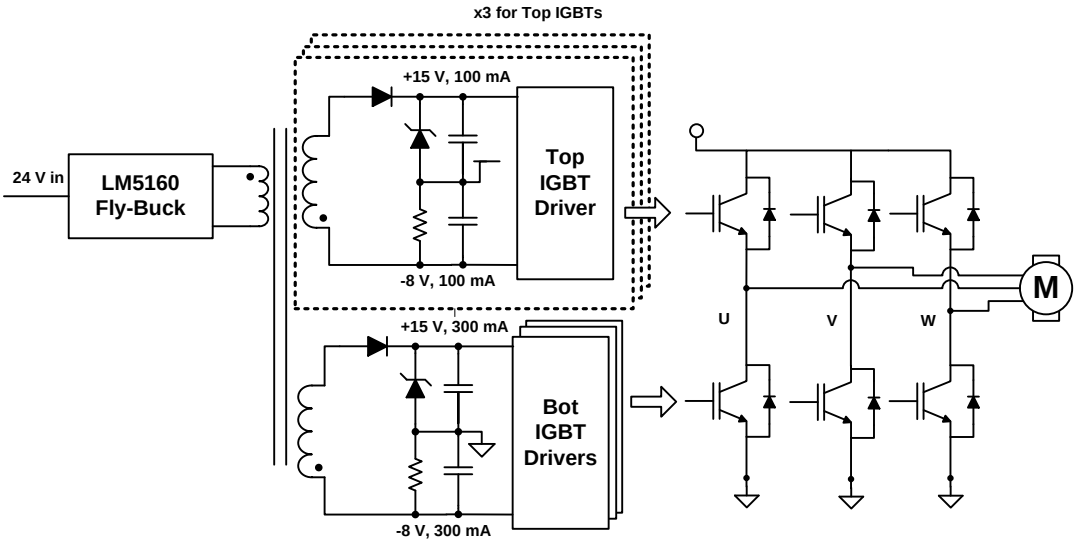

Figure 4. System Block Diagram

4 Highlighted Products

This reference design features the LM5160 device (a wide input 65-V, 1.5-A synchronous buck and Fly-Buck converter), which is selected based on the design requirements and device specifications. For more information, view the product folder LM5160.

4.1 Component Selection

The LM5160 is a 65-V, 1.5-A synchronous step-down converter with integrated high-side and low-side MOSFETs. The constant-on-time control scheme does not require loop compensation and supports high step-down ratios with a fast transient response. An internal feedback amplifier maintains ±1% of output voltage regulation over the entire operating temperature range. The on-time varies inversely with input voltage resulting in a nearly constant switching frequency.

4.2 Fly-Buck Converter Operation

The primary goal of this design is to provide a high-performance, cost-effective, and easy-to-design isolated power supply solution for the IGBT gate drive bias power. The Fly-Buck is basically a buck regulator with couple windings added to the inductor. The coupled windings can generate isolated outputs. The physical appearance of the Fly-Buck resembles a combination of a buck and flyback converter, hence the name Fly-Buck (Figure 5). The operation on the primary side is similar to the buck, while the secondary side output is clamped by the primary output. The Fly-Buck operation in a switching cycle can be divided into on-time and off-time, as Figure 6 illustrates.

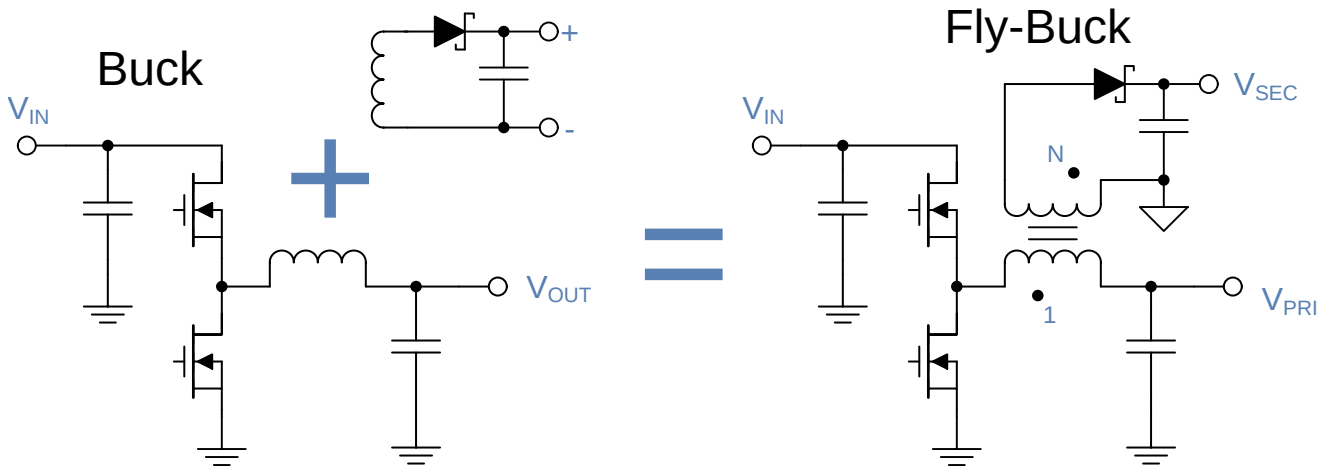

Figure 5. From Buck to Fly-Buck

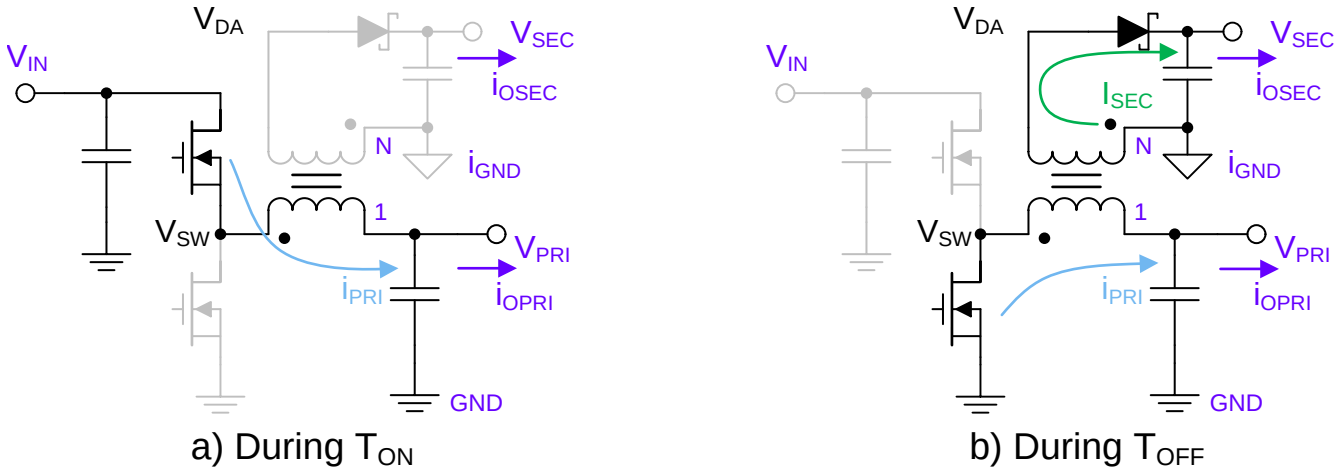

Figure 6. The Fly-Buck in ON and OFF time

During T_{ON}, the rectifier diode is in reverse bias, so the secondary side is cut off from the primary. The primary side operates similarly as it does in a buck regulator; the transformer primary current rises linearly. The primary output voltage is $V_{pri} = D \times V_{in}$. During T_{OFF}, the diode is forward biased and conducts. The current can flow in the primary and secondary side simultaneously; however, the magnetizing current in the transformer is still in the triangle waveform, which can be calculated as the combination of the primary and secondary winding current as defined by Equation 3:

$$i_m = i_{pri} + N \times i_{sec} \quad (3)$$

The primary side output clamps the secondary output voltage, $V_{SEC} = N \times V_{PRI}$. View the steady-state operation waveforms of a Fly-Buck in Figure 7.

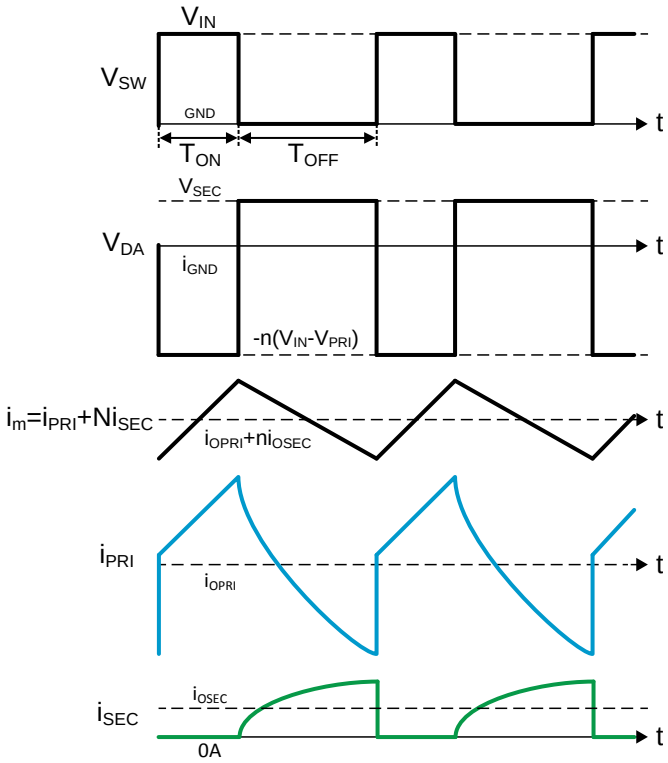

Figure 7. Fly-Buck Operation Waveform

From the above analysis, the magnetizing current ripple can be derived as Equation 4:

$$\Delta i_m = \frac{V_{pri}}{L_{pri}} \times \frac{1 - D}{f_{sw}} \quad (4)$$

where

- L_{pri} = Primary inductance.
- $D = T_{ON} / (T_{ON} + T_{OFF})$ = Duty cycle.
- f_{sw} = Switching frequency.

Equation 5 calculates the peak current of the primary side as:

$$i_{m(peak)} = i_m + \tfrac{1}{2}\Delta i_m = i_{opri} + (N \times i_{osec}) + \tfrac{1}{2}\Delta i_m \quad (5)$$

where

- i_{opri} = Average primary output current.
- i_{osec} = Average secondary output current.

If multiple outputs are involved, each secondary output must be converted to the primary side by multiplying the corresponding turns ratio—Equation 5 is still applicable.

4.3 Circuit Design

4.3.1 Setting Primary Side Output Voltage

Figure 8 shows that the primary-side regulation (PSR) of the Fly-Buck topology is realized through the coupled winding of the transformer, as the primary output clamps the secondary outputs during duty off time. Setting the primary output is the first step in a Fly-Buck converter design. Having the duty cycle below 50% is optimal because the Fly-Buck secondary outputs transfer the energy in off-time; and having a duty cycle too high affects the energy flow. Based on $V_{PRI} = D \times V_{IN}$, the primary side output is initially set at 10 V, which gives 50% of D at the minimum of V_{IN} = 20 V. Then the secondary-to-primary turns ratio of the transformer can be estimated as $N = V_{SEC} / V_{PRI} = 2.3$, and the primary-side average current at full-load is roughly $6 \times (N \times i_{osec}) = 1.38$ A, accounting for a 100-mA bias current each for a total of six IGBT drivers. Establishing these preliminary parameters provides a starting point and helps to guide through the sequential steps of the design. These parameters must be tuned and adjusted during the design process. In the final design, the primary output voltage is settled at 10.5 V as Figure 8 illustrates.

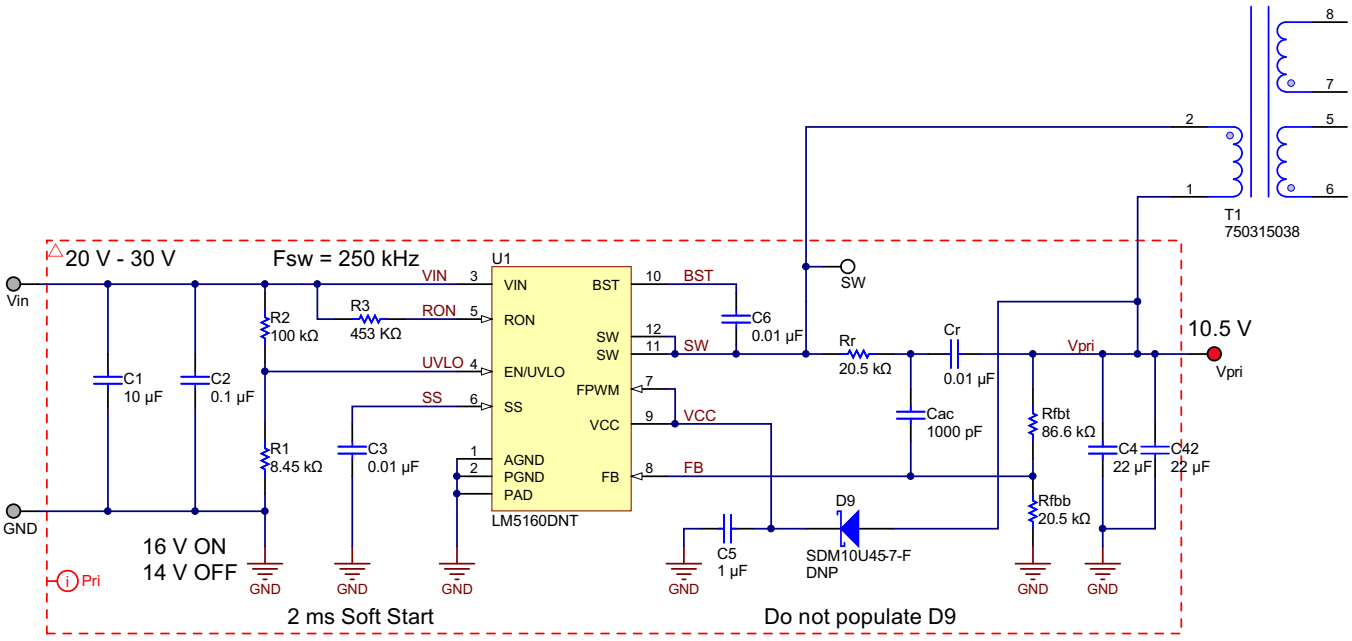

Figure 8. Primary Section of Schematic Showing LM5160

4.3.2 Transformer Design

The desirable transformer turns ratio is calculated based on the secondary-to-primary output ratio, which is 2.3:1. The rectifier diode forward voltage and winding data capture record (DCR) drop must be taken into account; therefore, the turns ratio is slightly higher than 2.3. The turns ratio also has a certain granularity limit subject to the actual winding turn count. To accommodate that granularity limit, adjust the primary output voltage accordingly.

The primary side inductance determines the current ripple in the transformer. The LM5160 device limits the peak current to approximately 2.1 A, and from the estimated 1.38-A average current level, there is plenty of ripple margin. The ripple must usually be limited to less than 60% of the average current. Equation 4 calculates the minimum required inductance at the max V_{IN} condition, which gives $L_{pri} > 32$ µH.

The transformer used in this design is built with a PQ2020-core through-hole package by Wurth Elektronik, and the part number is 750315038. The transformer specification has a secondary-to-primary turns ratio of 2.33:1, and all four secondary windings have the same turn count. The primary inductance is 36.5 µH. Upon checking, the peak current is approximately 1.74 A (given by Equation 5) below the 2.1-A current limit.

4.3.3 Shutdown Function

The LM5160 has an under-voltage lock out (UVLO) pin for the low-voltage shutdown, which can be utilized as an enable function pin. External circuitry can be used to pull the UVLO pin to ground to shut down the operation of the power supply.

4.3.4 Generating Positive and Negative Bias for Gate-Driver

A single transformer winding in the design generates the positive and negative bias voltage rails. The total output voltage from the secondary winding is 23 V, and the 15 V and –8 V is obtained through a Zener diode and a resistor voltage split circuit. The 15-V Zener clamps the positive output from 15 V to the common ground. The resistor limits the current through the Zener from the ground to the –8-V rail. The split circuit requires balanced load currents to both outputs; otherwise, the output with a heavier load collapses. The static current in the resistor is the additional budget current that allow supply to the positive output, as the 15 V requires a few mA more of supply current to power the driver IC. This reference design uses a 511-Ω resistor, which gives the 15-V rail approximately 15-mA more current capacity than the –8-V rail.

The voltage split circuit is a compromise between the solution size and regulation. Using a separate winding for each output results in the best regulation and efficiency, but increases the size and pin count of the transformer. For the centralized-driver bias supply design, it is impractical to have eight windings for all eight outputs given the requirements of high-voltage insulation spacing. With the Zener diode, the 15-V rail can have a stable output with a tight regulation tolerance, which is important for the turn-on speed of high power IGBTs. For –8 V, using the resistor provides a larger variation margin, but the negative bias is less critical in terms of the level of accuracy. The purpose of the negative bias is to prevent a high dv/dt-induced false turn-on of the IGBT in motor drive and high-voltage inverter applications. As long as the negative bias has low enough potential, it can maintain the secure turn-off of an IGBT. Another benefit of the voltage split scheme is the flexibility of setting the positive and negative voltage levels. Unlike the separate winding method, the voltage split scheme does not restrain to the transformer turns ratio. The total winding voltage can be adjusted by changing the primary output, and a different combination of Zener and resistor can be used.

Figure 9 shows the secondary section of the schematic.

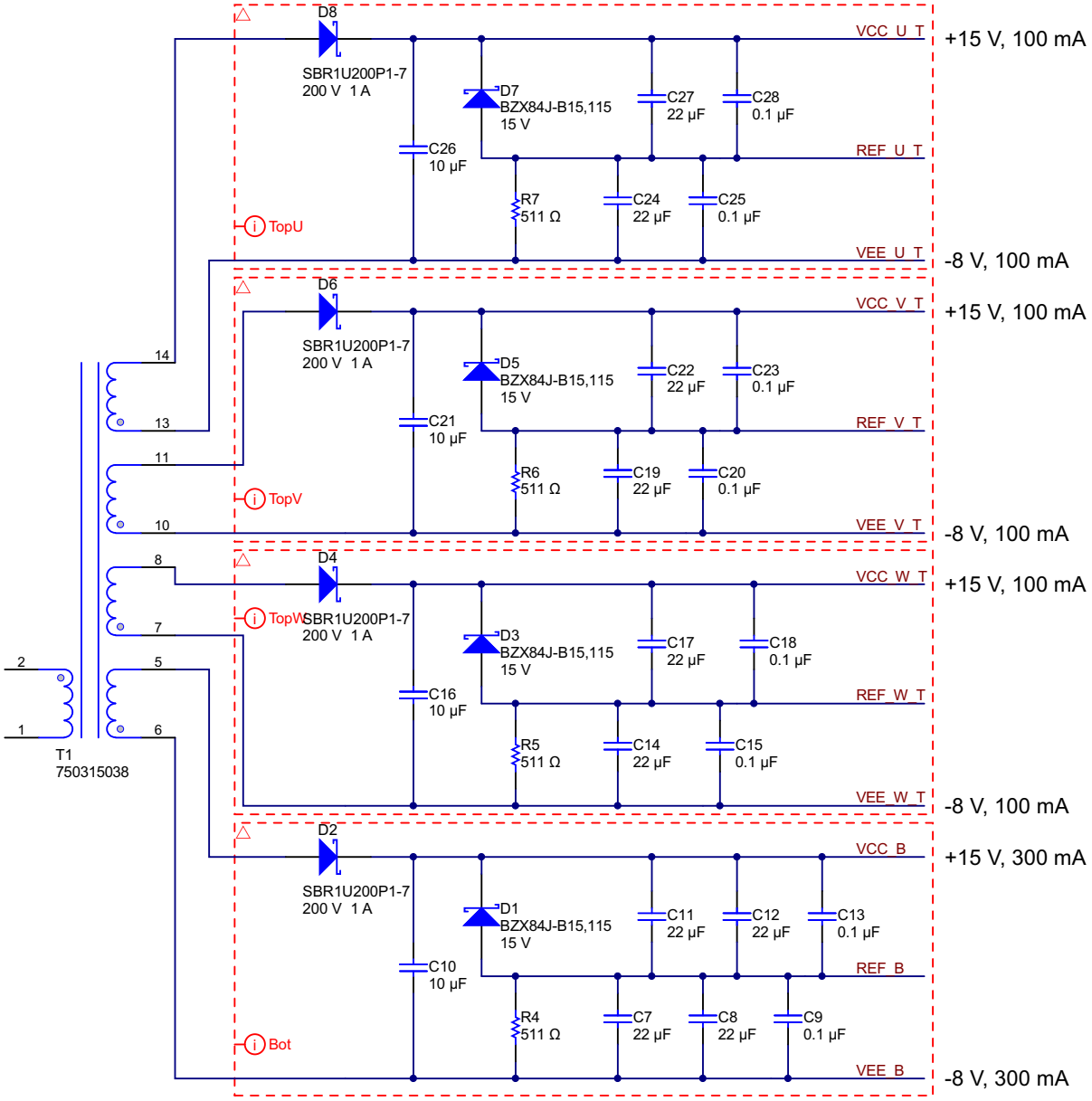

Figure 9. Secondary Section of the Schematic

4.3.5 Single Transformer for Powering All Three IGBT Arms

The Fly-Buck design uses only one transformer to power all three arms (U, V, and W) of the three-phase inverter. Each top-side IGBT requires an isolated bias supply for the driver, while the three bottom IGBTs can share the same bias, as these have common ground potential. Therefore, there are four pairs of positive and negative rails, (eight outputs in total), required to power the six IGBTs in three-phase bridge arms. Table 1 shows the configuration of the outputs.

Table 1. Outputs for Top and Bottom IGBTs (for all three arms)

PHASE	FOR TOP IGBT	FOR BOTTOM IGBT
U	VCC_U_T	VCC_B
	VEE_U_T	VEE_B
	REF_U_T	REF_B
V	VCC_V_T	VCC_B
	VEE_V_T	VEE_B
	REF_V_T	REF_B
W	VCC_W_T	VCC_B
	VEE_W_T	VEE_B
	REF_W_T	REF_B

5 Test Setup and Test Results

5.1 Start-Up Waveforms

The board is tested at both no-load and full-load conditions at a 24-V input. The four sets of outputs were monitored and ramped up at the same matching pace— for this reason, only VCC_B to VEE_B and VCC_U_T to VEE_U_T are shown here. In Figure 10, channel 3 (C3) in blue is the total voltage from VCC_B to VEE_B and channel 4 (C4) in green is the total voltage from VCC_U_T to VEE_U_T.

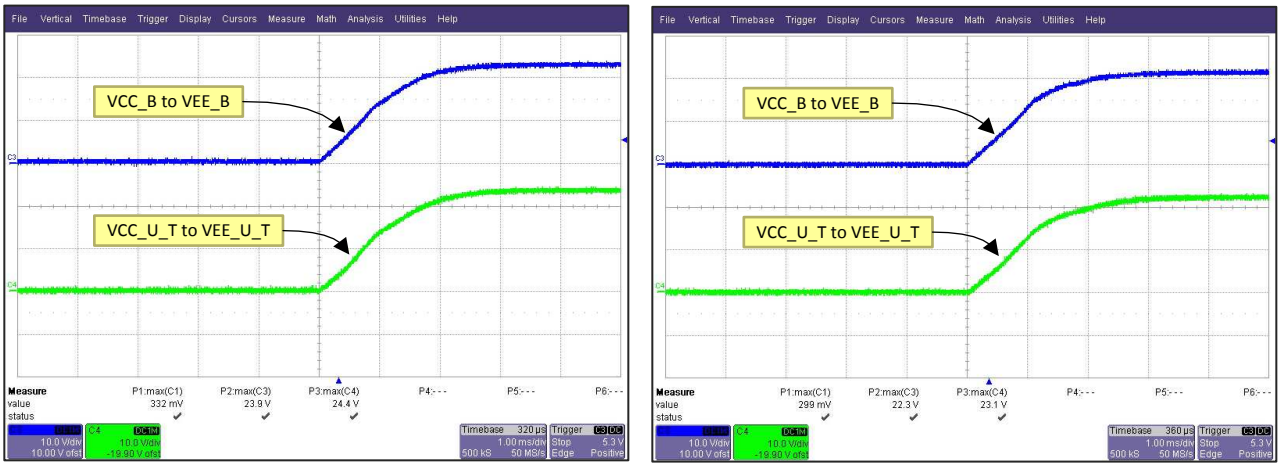

Figure 10. Start-Up into (Left) No Load at 24 V_{IN} and (Right) Full Load at 24-V_{IN}

The waveforms in Figure 11 show how the positive and negative rails ramp up during star-up. C3 (blue) is the VCC_B (15-V rail), and C4 (green) is the VEE_B (–8 V rail).

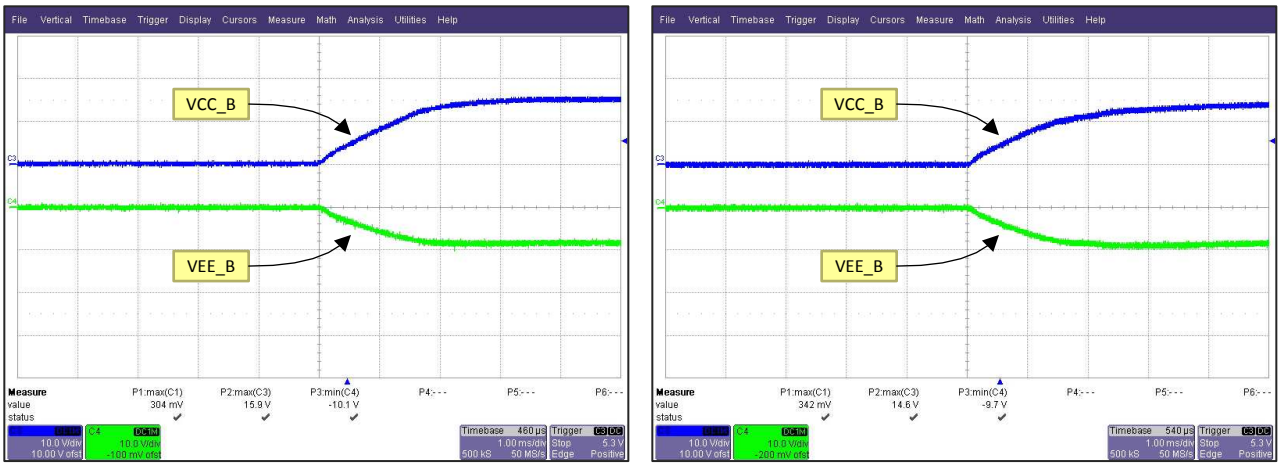

Figure 11. VCC_B and VEE_B Start-Up into (Left) No Load at 24-V_{IN} and (Right) Full Load at 24-V_{IN}

5.2 Switching Waveforms

The switch node voltage on the primary side is measured at no-load and full-load conditions at a 24-V input. Figure 12 shows the switching waveforms at no-load and full-load conditions.

Figure 12. Switching Waveform at (Left) No Load at 24-V_{IN} and (Right) Full Load at 24-V_{IN}

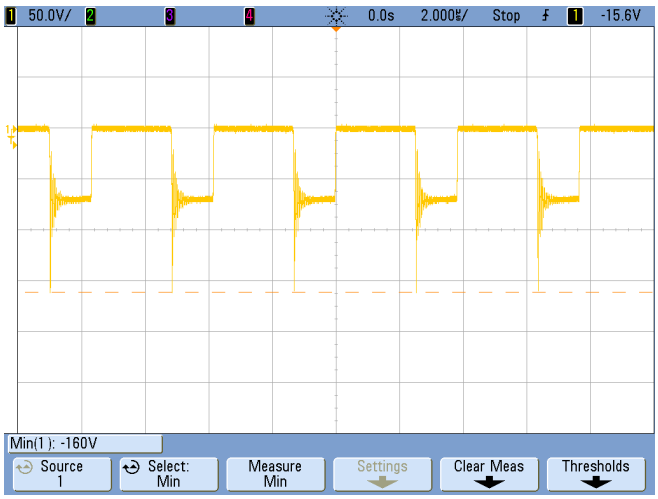

Figure 13. U_T Output Diode Voltage at Full load at 30-V_{IN}

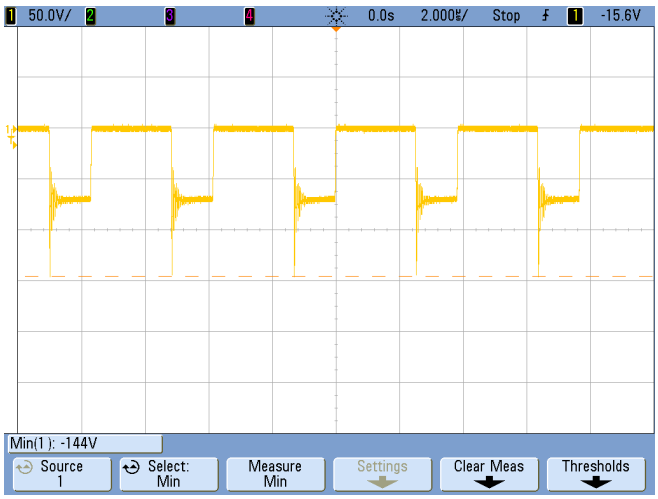

Figure 14. Bottom Output Diode Voltage at Full Load at 30-V_{IN}

5.3 Efficiency

The efficiency measurement was taken when all of the outputs were loaded at the same percentage current with respect to their full load. As Figure 15 shows, the peak efficiency reaches approximately 82% at full load.

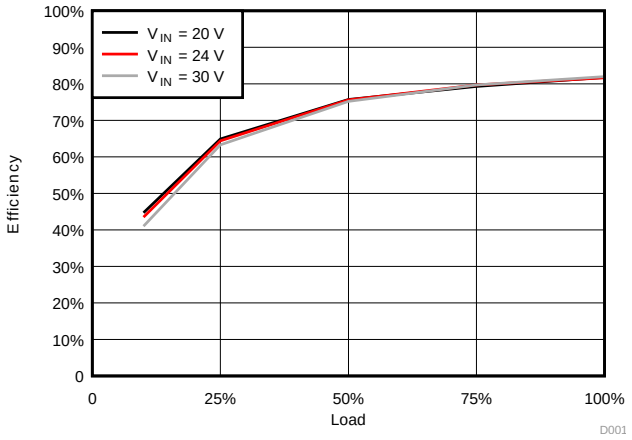

Figure 15. Total Efficiency Under Balanced Load

5.4 Regulation and Cross-Regulation

The regulation under balanced load conditions was tested when all of the outputs were loaded with the same percentage of current with respect to their full load at different input voltage conditions. Because the U_T, V_T, and W_T set of outputs is symmetrical to each other, only the U_T output regulation is displayed.

The voltage between V_{CC} and V_{EE} was measured as a 23-V output, as the two outputs are from one single transformer winding. Figure 16 shows that the worst-case variation on the 23-V output under line and load change is below ±4%. A 15-V Zener diode clamps the V_{CC} (15 V) outputs; therefore, the voltage level is fairly stable under all conditions. Alternatively, the V_{EE} (–8 V) outputs endures all of the deviation from the total 23-V output, while still holding acceptable levels.

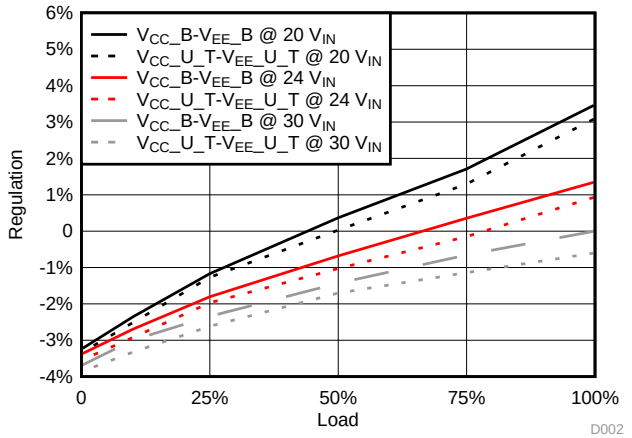

Figure 16. V_{CC} to V_{EE} Output Regulation Under Balanced Load

5.5 Output Voltage Ripples

The output ripples were measured directly at the output capacitors when all outputs were fully loaded. The input voltage was at 24 V. The U_T, V_T, and W_T outputs have matching ripple results due to their symmetrical structure, and only U_T is displayed. The scope shots in Figure 17, Figure 18, Figure 19, and Figure 20 are the corresponding output ripple waveforms in AC mode.

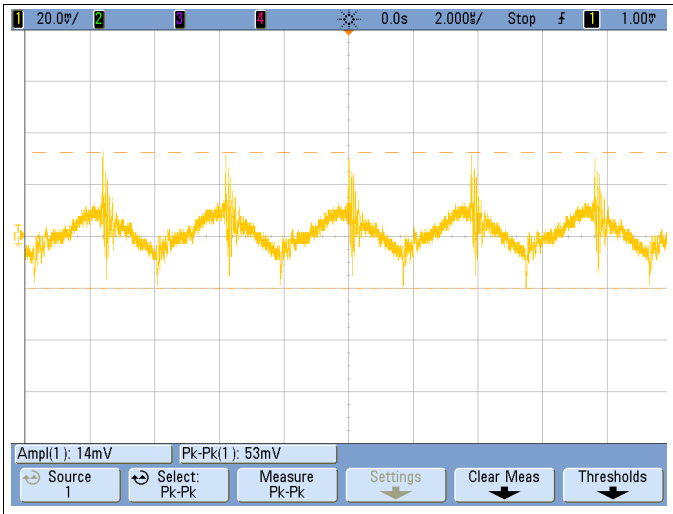

Figure 17. VCC_U_T Output Ripple at Full Load at 24-V_{IN}

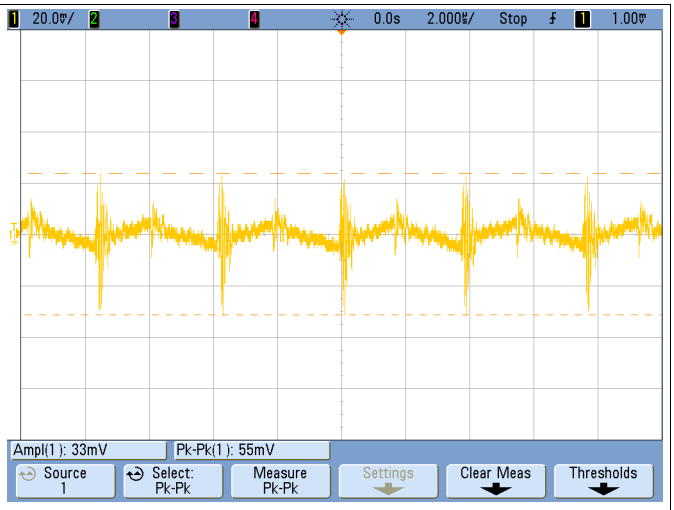

Figure 18. VEE_U_T Output Ripple at Full Load at 24-V_{IN}

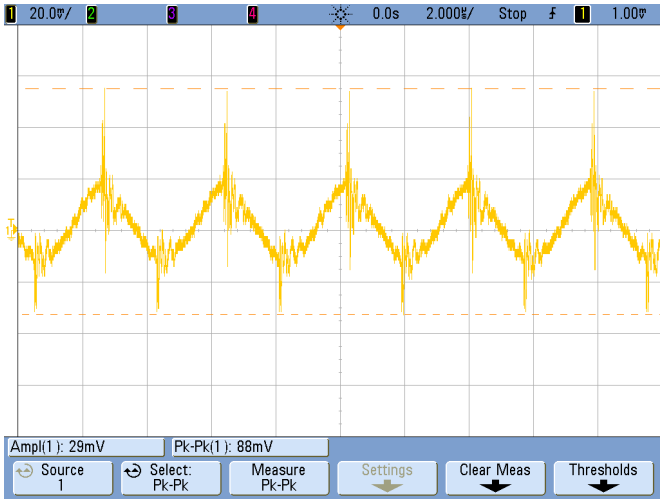

Figure 19. VCC_B Output Ripple at Full Load at 24-V_{IN}

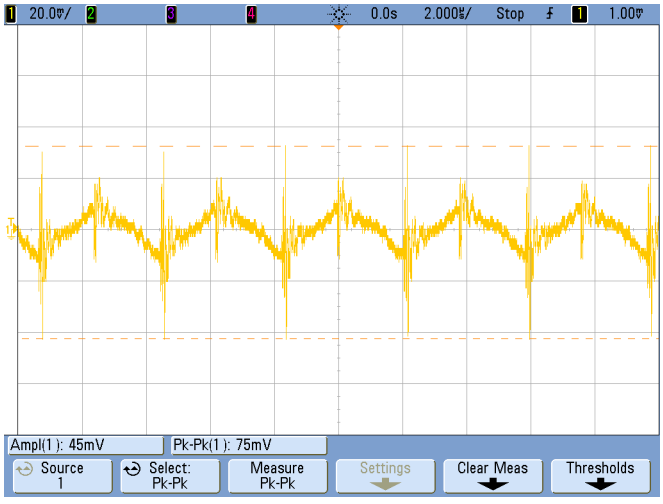

Figure 20. VEE_B Output Ripples at Full Load at 24-V_{IN}

5.6 Testing With ISO5500 and IGBTs

To emulate the actual drive testing, this reference design is tested with TI's ISO5500 evaluation modules (EVMs) along with 1200-V IGBTs. Six 16-kHz complementary PWM signals for IGBT gate driving are generated using the Piccolo LaunchPAD™ from TI. These PWM signals are fed to six ISO5500s (each connected to one 1200-V IGBT). Figure 21 shows that the IGBTs are connected in half-bridge form with a 1-kΩ load connected at the output. Figure 22 shows an image of the setup with all of the boards.

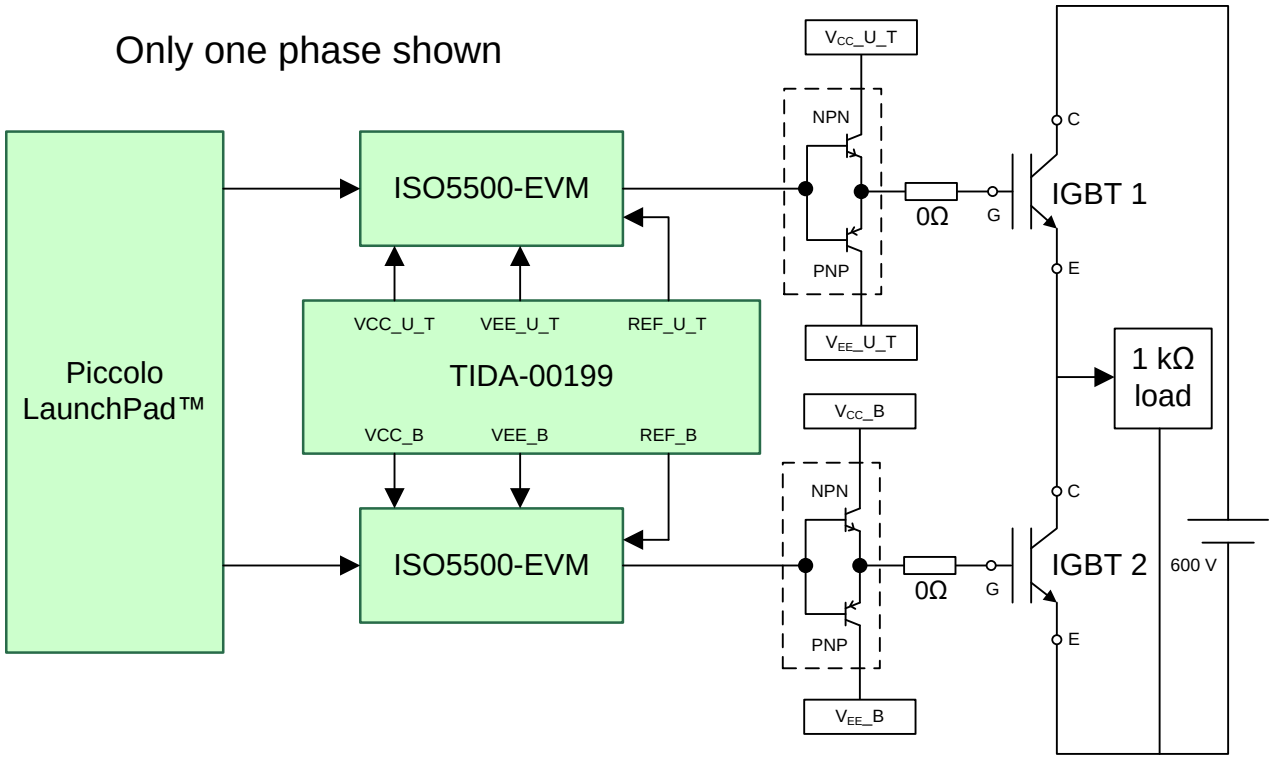

Figure 21. Setup for Testing TIDA-00199 Design With TI's ISO5500 and IGBTs

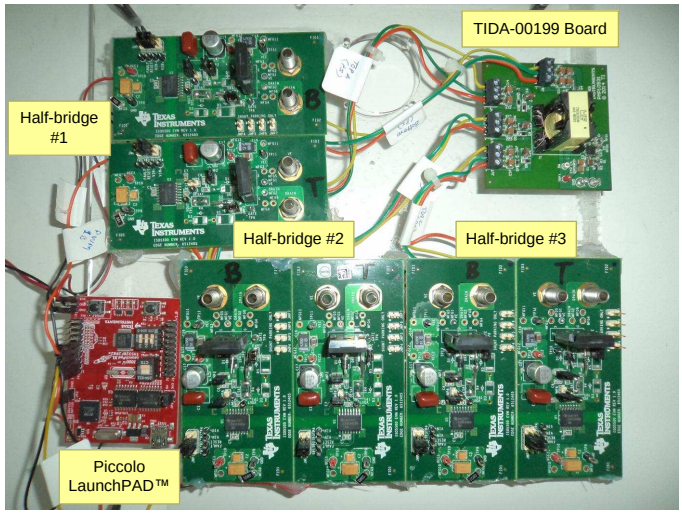

Figure 22. Board Setup Image

The voltage ripple was measured when a 600-V voltage was applied to the IGBT arms and the ISO5500 boards were powered by this reference design board. Figure 23 and Figure 24 show the output ripple-voltage waveforms that meet the specifications of the reference design.

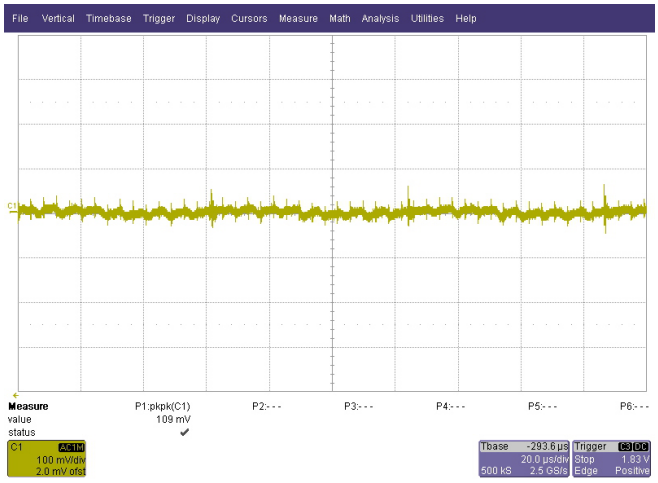

Figure 23. Ripple on 15-V Output (for dv/dt = 5.6 × E9 V/s on the Output Load)

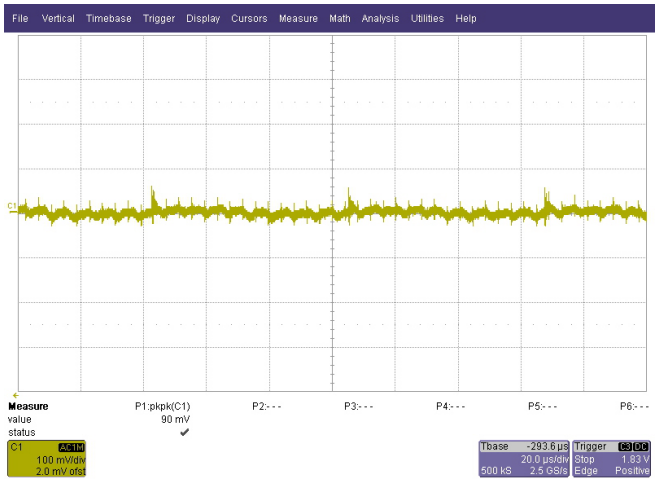

Figure 24. Ripple on –8-V Output (for dv/dt = 5.6 × E9 V/s on the Output Load)

The current boost transistors (NPN and PNP) are used to boost the output current of the ISO5500 to drive the IGBTs. With a 6-A peak current while charging the internal capacitance of the IGBTs, the ripple on the V_{CC} and V_{EE} outputs of power supply are also measured. Figure 25 and Figure 26 show the same ripple on the outputs.

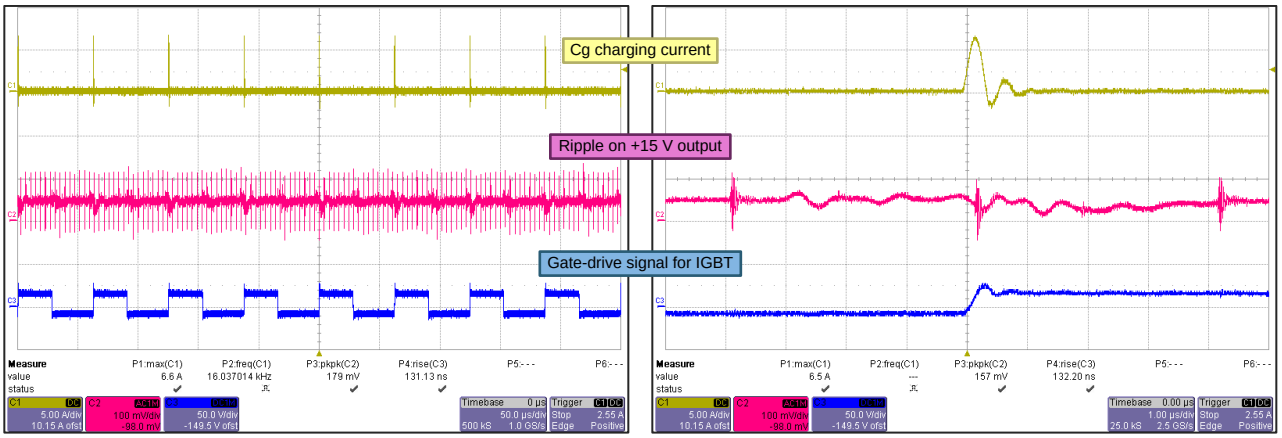

Figure 25. (A) Ripple on 15-V Output for 6-A Peak Load Current With IGBTs (B) Zoomed Waveforms

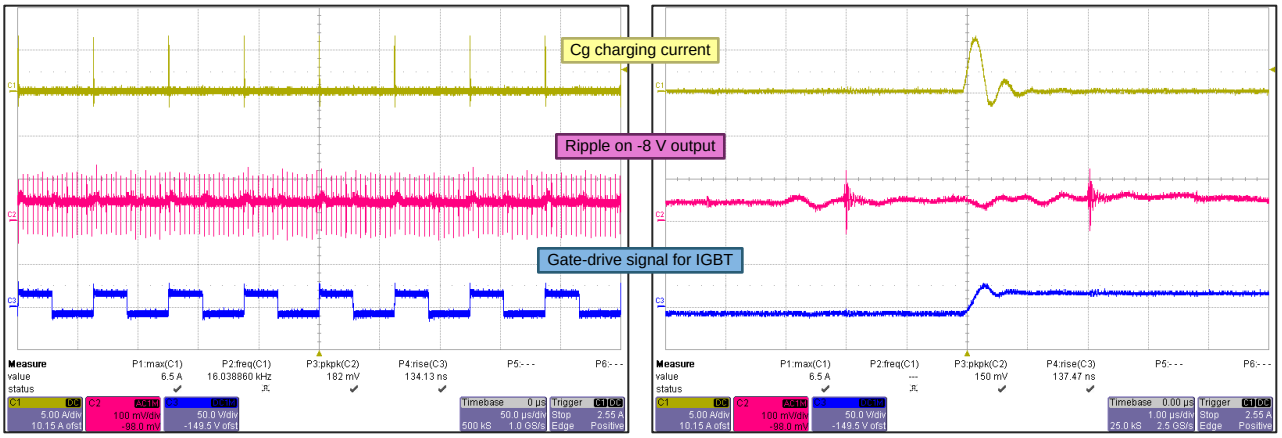

Figure 26. (A) Ripple on –8-V Output for 6-A Peak Load Current With IGBTs (B) Zoomed Waveforms

6 Design Files

6.1 Schematics

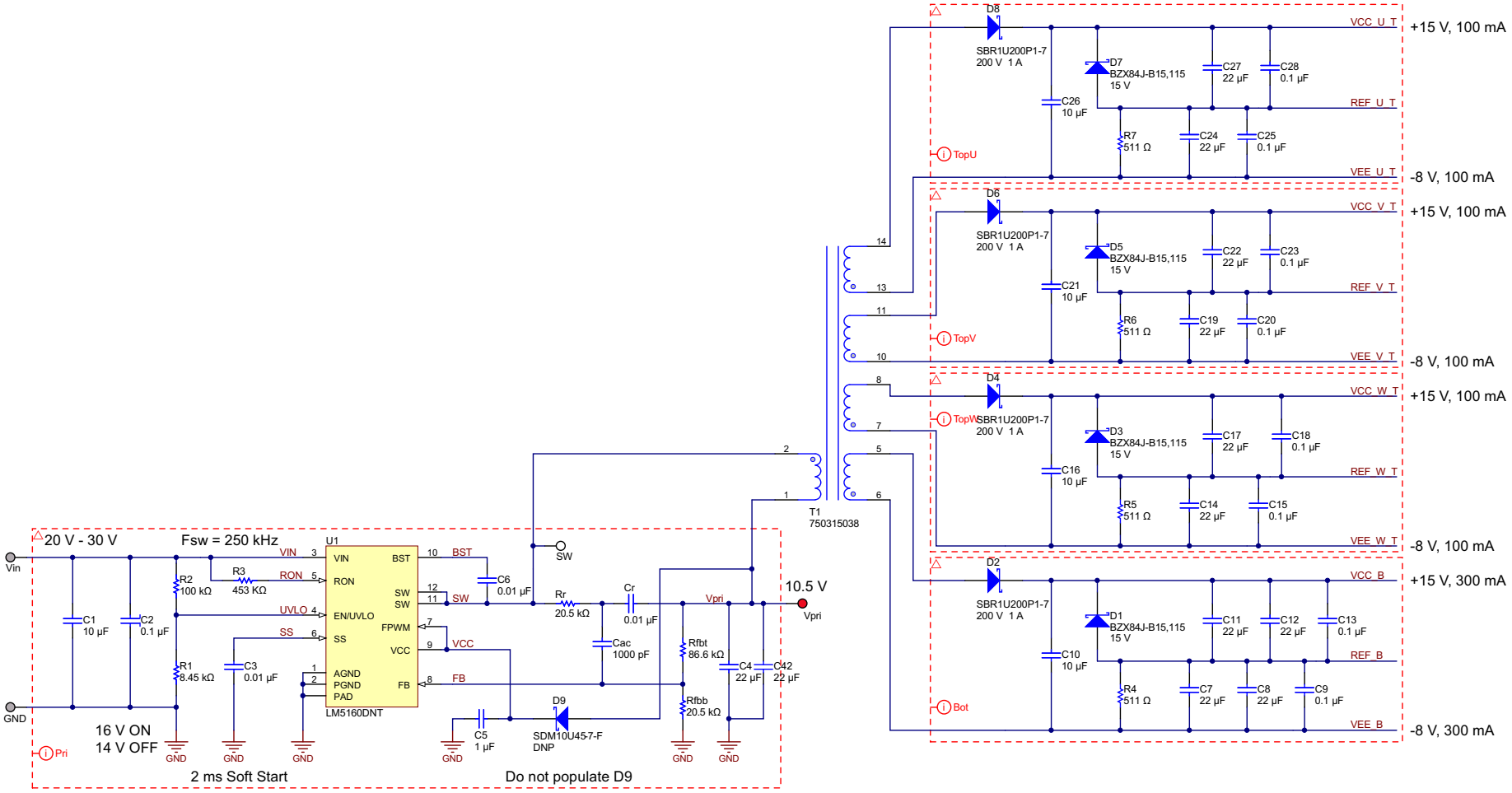

Figure 27. TIDA-00199 Schematic

6.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00199.

Table 2. BOM

QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER	MANUFACTURER PART NUMBER	PCB FOOTPRINT	NOTE
1	!PCB1	Printed Circuit Board	Any	TIDA-00199		Fitted
5	C1, C10, C16, C21, C26	CAP, CERM, 10 µF, 50 V, ±10%, X7R, 1210	MuRata	GRM32ER71H106KA12L	1210	Fitted
9	C2, C9, C13, C15, C18, C20, C23, C25, C28	CAP, CERM, 0.1µF, 50V, ±10%, X7R, 0603	TDK	C1608X7R1H104K	0603	Fitted
2	C3, C6	CAP, CERM, 0.01 µF, 50 V, ±10%, X7R, 0603	TDK	C1608X7R1H103K	0603	Fitted
12	C4, C7, C8, C11, C12, C14, C17, C19, C22, C24, C27, C42	CAP, CERM, 22 µF, 25 V, ±10%, X7R, 1210	MuRata	GRM32ER71E226KE15L	1210	Fitted
1	C5	CAP, CERM, 1 µF, 25 V, ±10%, X7R, 0603	TDK	C1608X7R1E105K080AB	0603	Fitted
1	Cac	CAP, CERM, 1000 pF, 50 V, ±10%, X7R, 0603	TDK	C1608X7R1H102K	0603	Fitted
1	Cr	CAP, CERM, 0.01 µF, 50 V, ±10%, X7R, 0603	MuRata	GRM188R71H103KA01D	0603	Fitted
4	D1, D3, D5, D7	DIODE ZENER 15 V 550 mW SOD323F	NXP Semiconductors	BZX84J-B15,115	SOD-323F	Fitted
4	D2, D4, D6, D8	DIODE SBR 200 V 1 A POWERDI123	Diodes Incorporated	SBR1U200P1-7	powerDI123	Fitted
1	D9	Diode, Schottky, 45 V, 0.1 A, SOD-523	Diodes Inc.	SDM10U45-7-F	SOD-523	Fitted
2	GND2, Vin	Terminal, Turret, TH, Double	Keystone	1502-2	Keystone1502-2	Fitted
4	JB, JUT, JVT, JWT	Terminal Block, 6A, 3.5 mm Pitch, 3-Pos, TH	On-Shore Technology	ED555/3DS	TERM_BLK_ED555-3DS	Fitted
1	R1	RES, 8.45 kΩ, 1%, 0.1 W, 0603	Vishay-Dale	CRCW06038K45FKEA	0603	Fitted
1	R2	RES, 100 kΩ, 1%, 0.1 W, 0603	Vishay-Dale	CRCW0603100KFKEA	0603	Fitted
1	R3	RES 453 kΩ 1/10 W 1% 0603 SMD	Panasonic Electronic Components	ERJ-3EKF4533V	0603	Fitted
4	R4, R5, R6, R7	RES, 511 Ω, 1%, 0.125 W, 0805	Vishay-Dale	CRCW0805511RFKEA	0805_HV	Fitted
2	Rfbb, Rr	RES, 20.5 kΩ, 1%, 0.1 W, 0603	Vishay-Dale	CRCW060320K5FKEA	0603	Fitted

Table 2. BOM (continued)

QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER	MANUFACTURER PART NUMBER	PCB FOOTPRINT	NOTE
1	Rfbt	RES, 86.6 kΩ, 1%, 0.1 W, 0603	Vishay-Dale	CRCW060386K6FKEA	0603	Fitted
1	SW	Test Point, Miniature, White, TH	Keystone	5002	Keystone5002	Fitted
1	T1	Transformer, Thru-Hole, 36.5 µH, 1:2.33:2.33:2.33:2.33	Wurth Electronics Midcom	750315038	WURTH_750315038	Fitted
1	U1	Wide Input 65 V, 1.5 A Synchronous Step-Down DC-DC Converter, DNT0012B	Texas Instruments	LM5160DNT	DNT0012B	Fitted
1	Vpri	Test Point, TH, Miniature, Red	Keystone	5000	Keystone5000	Fitted
0	FID1, FID2, FID3	Fiducial mark. There is nothing to buy or mount.	N/A	N/A	Fiducial10-20	Not Fitted

6.3 Layout Guidelines for LM5160

A proper layout is essential for optimum performance of the circuit. In particular, the following guidelines must be observed:

- The loop consisting of the input capacitor, V_{IN} pin, and P_{GND} pin carries the switching current. Therefore, the input capacitor must be placed close to the IC, directly across the V_{IN} and P_{GND} pins. The connections to these two pins must be direct to minimize the loop area. In general, it is not possible to place all of the input capacitances near the IC. A good practice is to use a 0.1 µF to 0.47 µF capacitor directly across the V_{IN} and P_{GND} pins as close as possible to the IC with the remaining bulk capacitor.
- The V_{CC} and bootstrap (BST) bypass capacitors supply switching currents to the high and low-side gate drivers. These two capacitors must also be placed as close to the IC as possible, and the connecting trace length and loop area must be minimized.
- The feedback trace carries the output voltage information and a small ripple component that is necessary for proper operation of the LM5160 device. Therefore, take care while routing the feedback trace to avoid coupling any noise into the feedback (FB) pin. In particular, the feedback trace must not run close to magnetic components, or parallel to any other switching trace.
- SW trace: The SW node switches rapidly between V_{IN} and GND every cycle and is therefore a source of noise. The SW node area must be minimized. In particular, the SW node must not be inadvertently connected to a copper plane or pour.

6.4 PCB Layout

Note that the total dimension of the board is 62 mm x 55 mm.

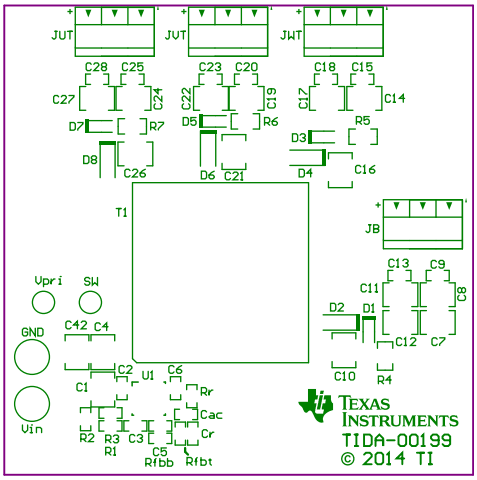

Figure 28. Top Overlay

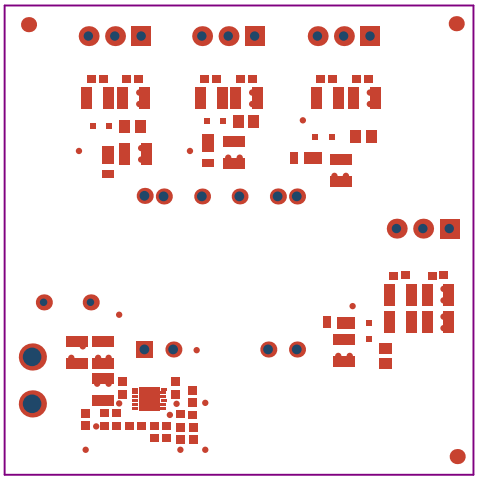

Figure 29. Top Solder Mask

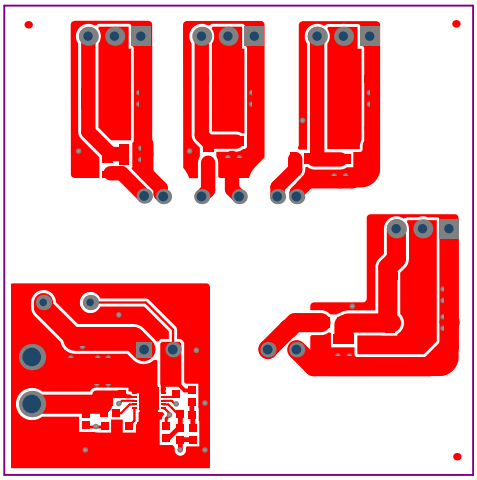

Figure 30. Top Layer

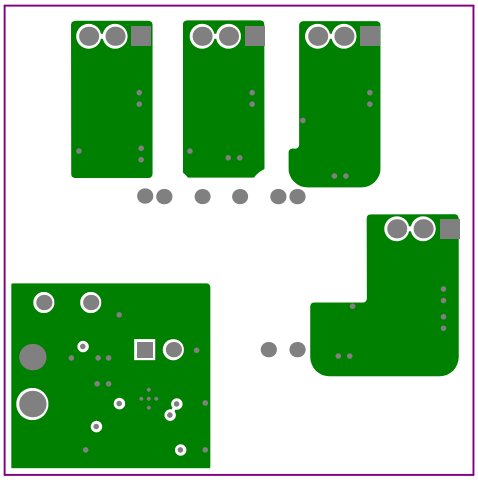

Figure 31. Midlayer 1

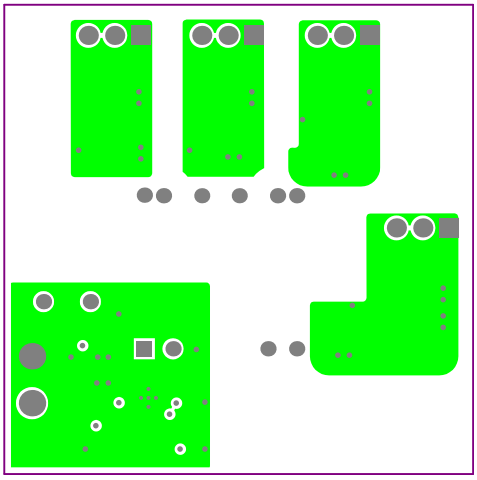

Figure 32. Midlayer 2

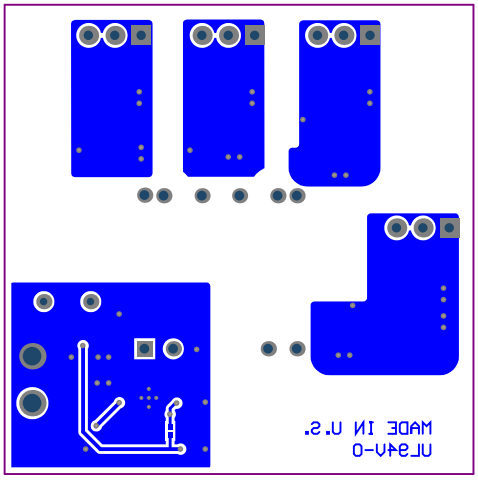

Figure 33. Bottom Layer

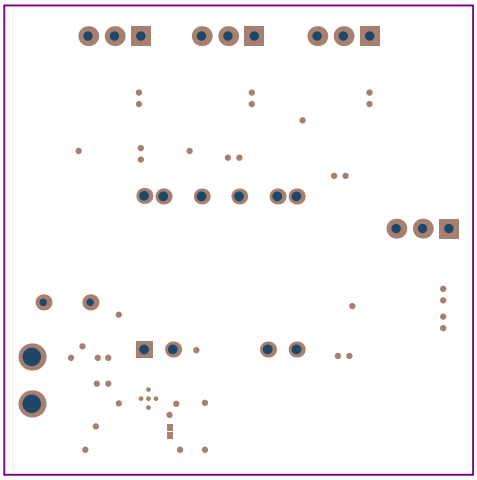

Figure 34. Bottom Solder Mask

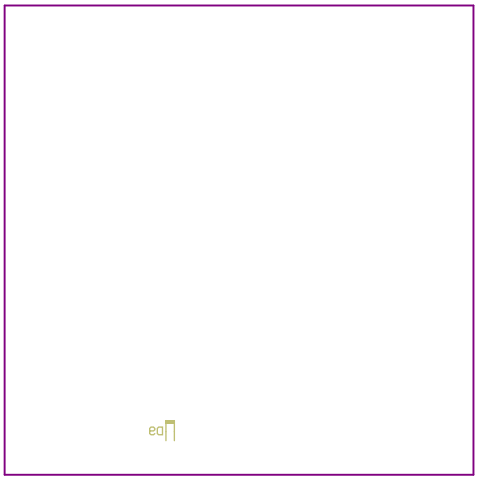

Figure 35. Bottom Overlay

6.5 Altium Project Files

To download the Altium project files, see the design files at TIDA-00199.

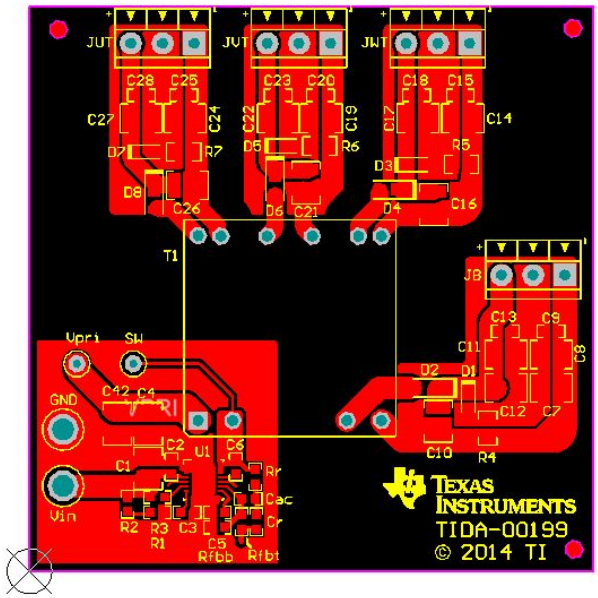

Figure 36. Top Layer

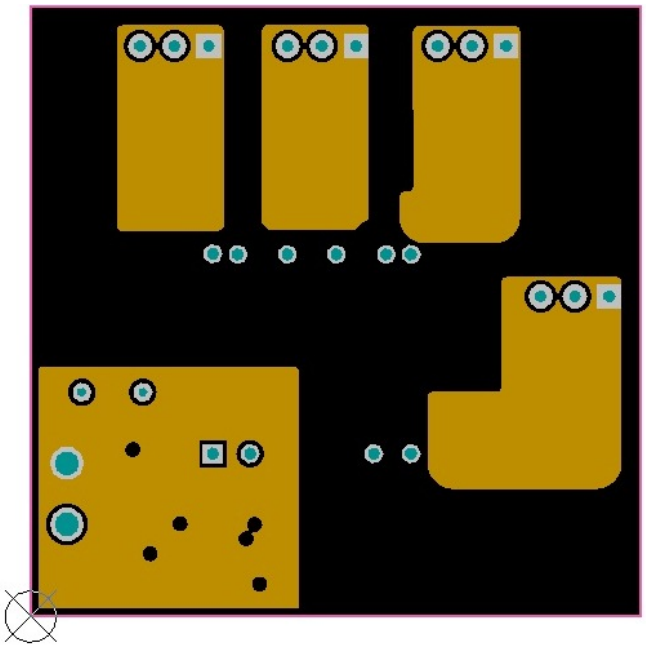

Figure 37. Midlayer 1

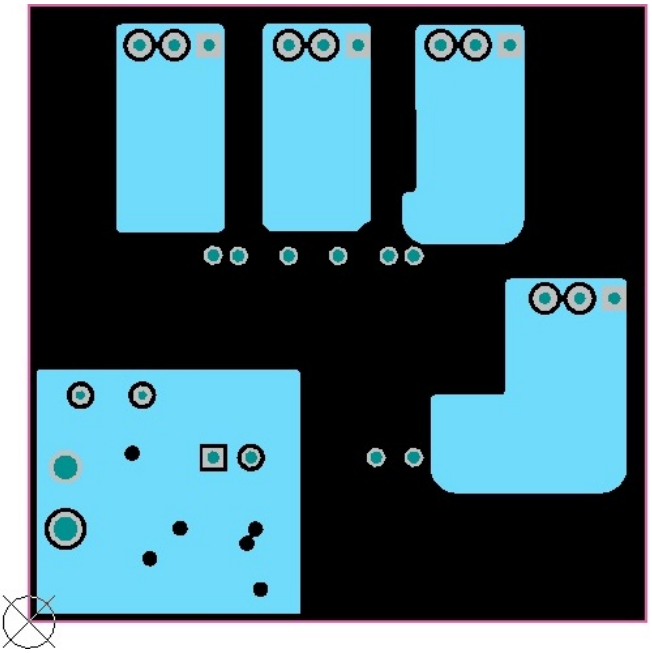

Figure 38. Midlayer 2

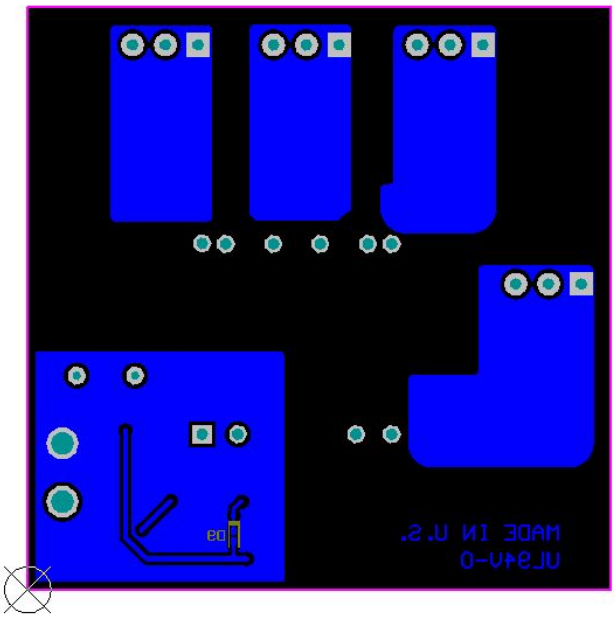

Figure 39. Bottom Layer

6.6 Gerber Files

To download the Gerber files, see the design files at TIDA-00199

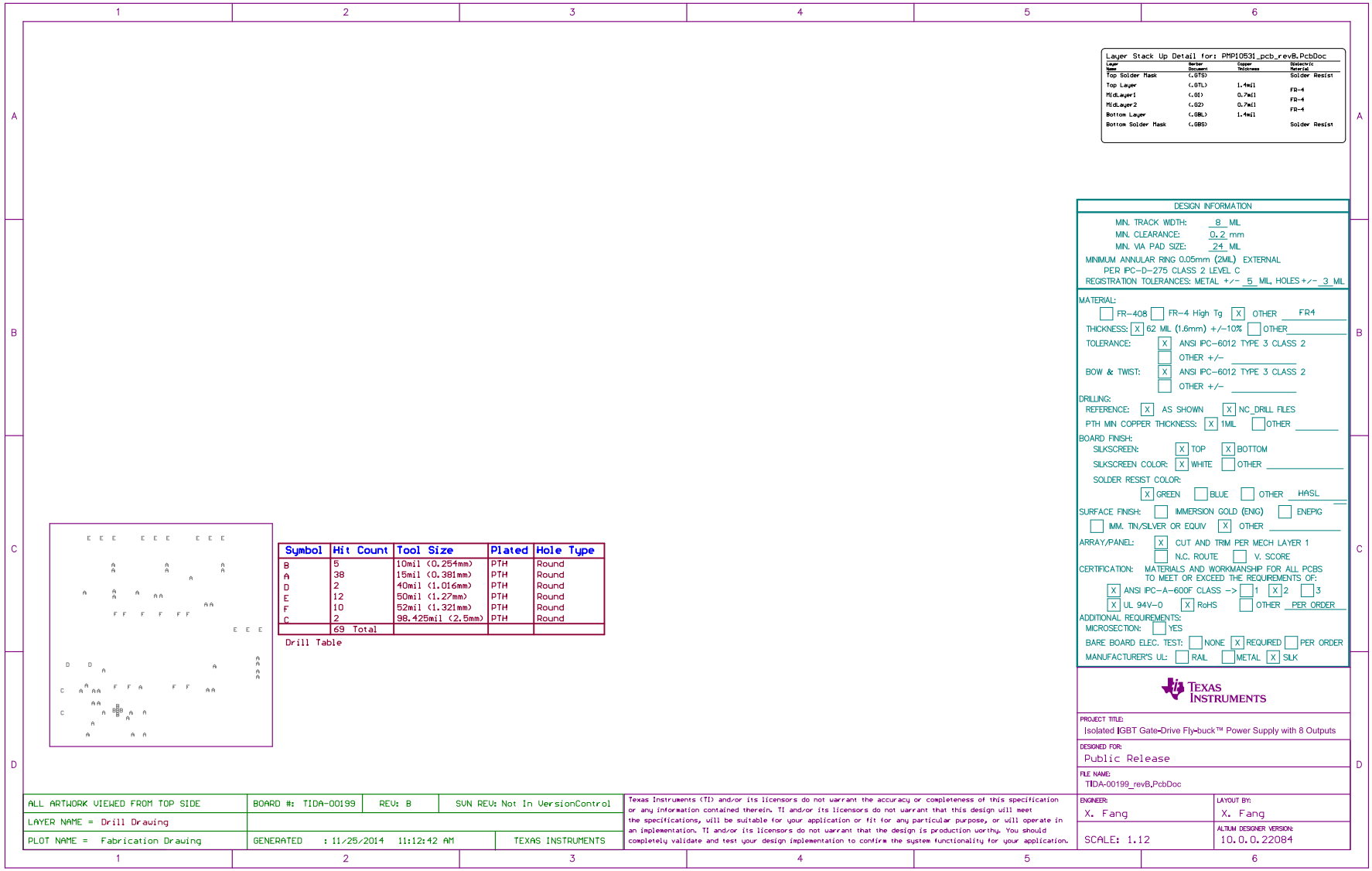

Figure 40. Fabrication Drawing

6.7 Assembly Drawings

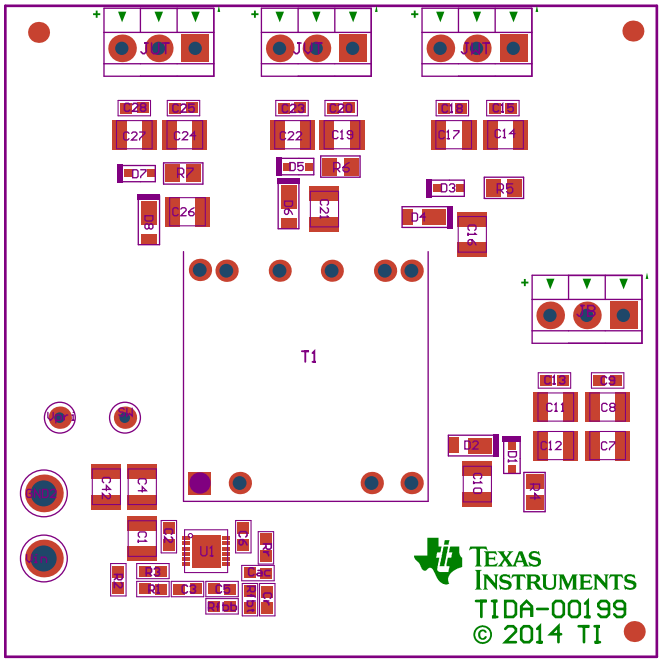

Figure 41. Top Assembly Drawing

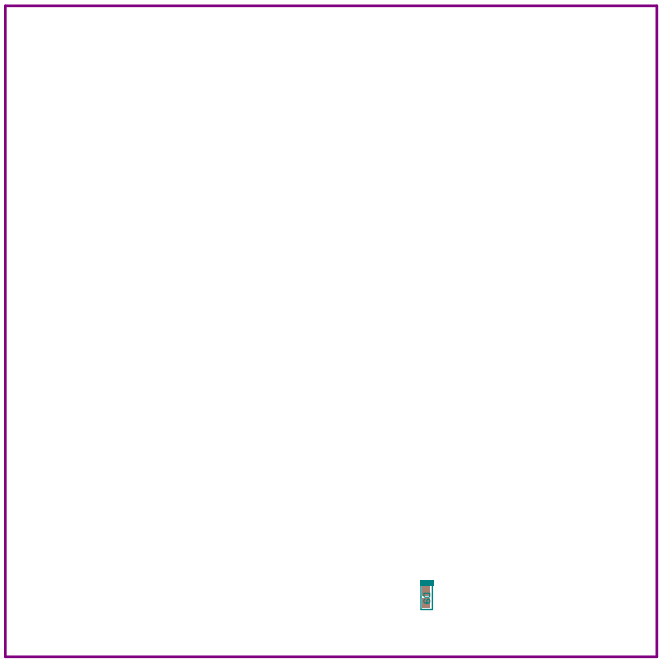

Figure 42. Bottom Assembly Drawing

7 References

1. EE Times, *Power Tip #6: Accurately Measuring Power Supply Ripple*, http://www.eetimes.com/document.asp?doc_id=1273282.
2. Texas Instruments, *LM5160 Buck EVM User's Guide*, (SNVU441).
3. Texas Instruments, *ISO5500EVM*, User's Guide (SLLU136).
4. Texas Instruments, *C2000 Piccolo LaunchPad*, (Tool Folder).
5. Texas Instruments, *Isolated IGBT Gate - Drive Fly-Buck™ Power Supply with 4 Outputs*, Reference Guide (TIDU478).
6. Texas Instruments, *Reinforced Isolated IGBT Gate-Drive Flyback Power Supply With Eight Outputs*, Reference Guide (TIDU411).

8 About the Author

XIANG FANG is an Applications Engineer at Texas Instruments where he is responsible for developing power solutions and reference designs. Xiang has been with TI since 2012 and has been involved in designing products for industrial and automotive applications. Xiang earned his PhD in Power Electronics at University of Central Florida in 2012.

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Revision History

Changes from Original (December 2014) to A Revision	Page
• Changed reference from Equation 1	9
• Changed reference from Equation 2	9

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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