Dennis Hudgins
Aaron Paxton

TI Designs
Dynamic Voltage Scaling with a Dual LDO

TI Designs

TI Designs provide the foundation that you need including methodology, testing and design files to quickly evaluate and customize the system. TI Designs help you accelerate your time to market.

Design Resources

TIDA-00387	Design Page
TLV7101828	Product Folder

Featured Applications

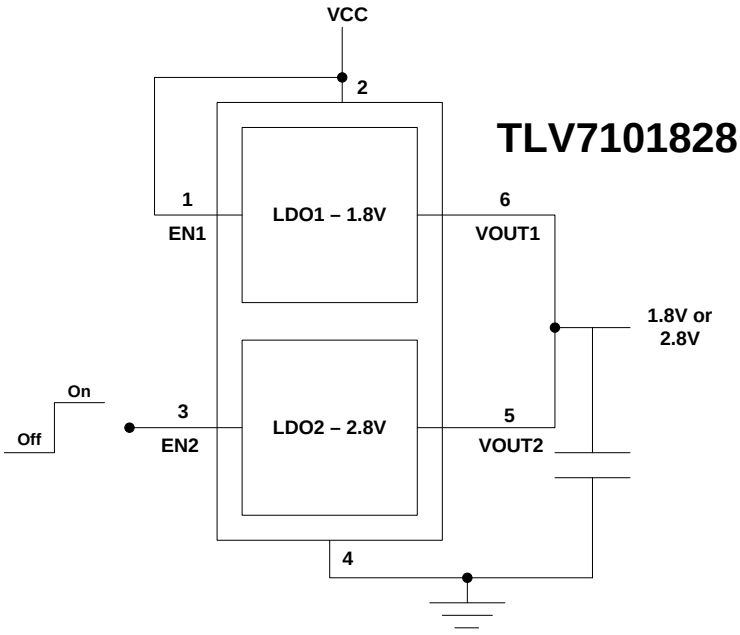
- Powering Microcontrollers
- Portable and Battery-Powered Applications
- Radio Applications

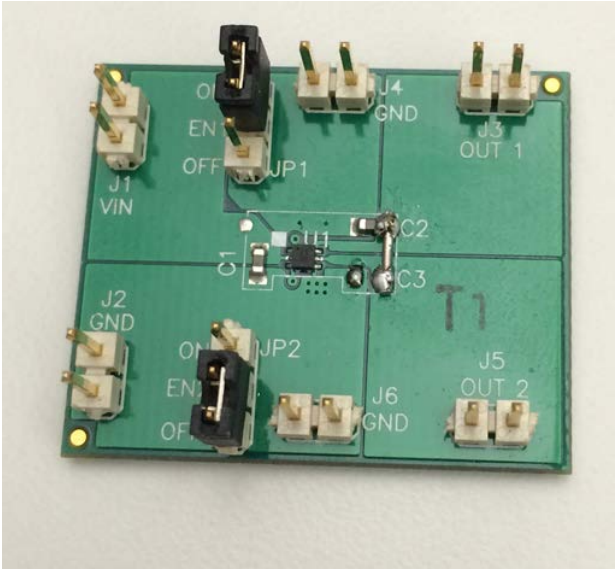
Circuit Description

This application solution details how a dual-channel LDO may be used to provide a dynamic voltage scaling output. This functionality is of particular interest when powering microcontrollers that have a wide operating voltage range: it is advantageous, when possible, to lower the operating voltage of the MCU in order to achieve lower power consumption.

TI E2E™ Community

Ask The Analog Experts
WEBENCH® Design Center
TI Precision Designs Library





1 Design Summary

The design requirements are as follows:

- Supply Voltage: 3.3 V
- Output Current: up to 200mA
- Load Transient Response: ≤ 70mV spike, 100µs recovery time
- Voltage Transition time: ≤ 200µs
- Quiescent Current: ≤ 35µA when the high channel is disabled
- Monotonic rise

The design goals and performance are summarized in Table 1.

Table 1. Comparison of Design Goals, Simulation, and Measured Performance

	Goal	Measured
Load Transient Spike	≤ 70mV	25mV
Load Transient Response time	≤ 100µs	100µs
Voltage transition time	≤ 200µs	200µs, 158µs
Quiescent Current	≤ 35µA (1.8V channel)	28.7µA

1.1 Equations

Power dissipation in a linear regulator is expressed as follows:

$$P_{LOSS} = (\frac{V_{IN} - V_{OUT}}{V_{IN}} \times I_{OUT}) + (V_{IN} \times I_{GND}) \quad (1)$$

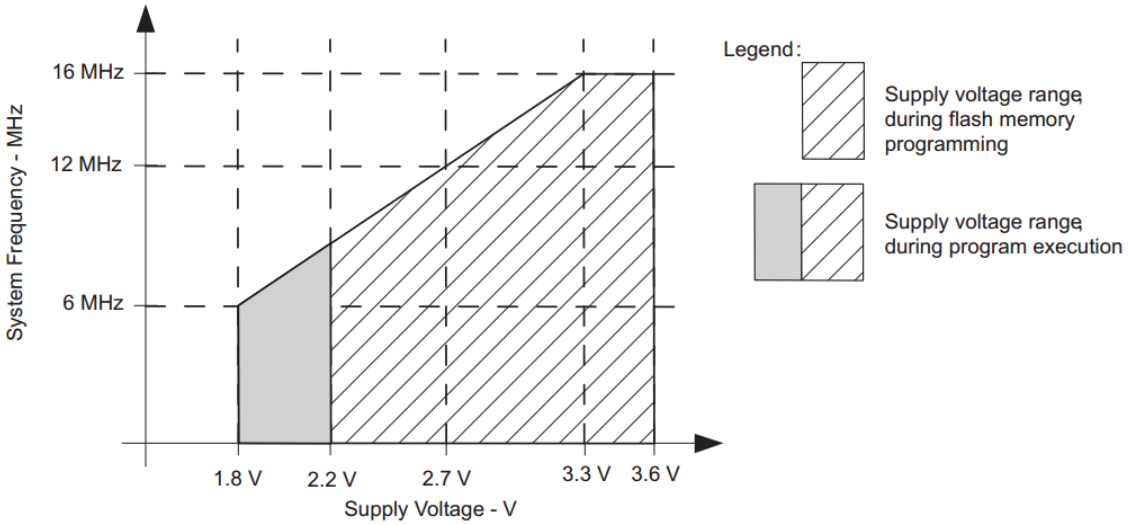
However, if $I_{OUT} \gg I_{GND}$, this equation can be reduced to the following:

$$P_{LOSS} = \frac{V_{IN} - V_{OUT}}{V_{IN}} \times I_{OUT} \quad (2)$$

2 Theory of Operation

Dynamic Voltage Scaling can be an important function when powering a variety of low-power microcontrollers. To see why, it helps to examine the properties of a series of prominent microcontrollers like the MSP430G2x:

The MSP430G2001, for example, has a supply voltage range that varies depending on the system frequency and programming modes. As an example, when the system frequency is 1MHz and flash memory programming is not required, the supply voltage range spans from 1.8V to 3.6V. However, if flash memory programming is required, the supply voltage range contracts to 2.2V to 3.6V. These ranges are illustrated in Figure 1.



Note: Minimum processor frequency is defined by system clock. Flash program or erase operations require a minimum V_{CC} of 2.2 V.

Figure 1: MSP430 Supply Voltage Range vs. System Frequency

Examining this chart might lead one to conclude that it is more advantageous to supply a constant voltage above 2.2V to the microcontroller (assuming the system frequency is 1MHz) in order to accommodate for instances where flash programming might be necessary. However, this wouldn't be the most efficient mode of operation. This is because current consumption also varies with supply voltage.

Fortunately, this behavior is also illustrated within the MSP430 datasheet. Looking at Figure 2, it is apparent that as the supply voltage increases, the Active Mode Current will correspondingly increase:

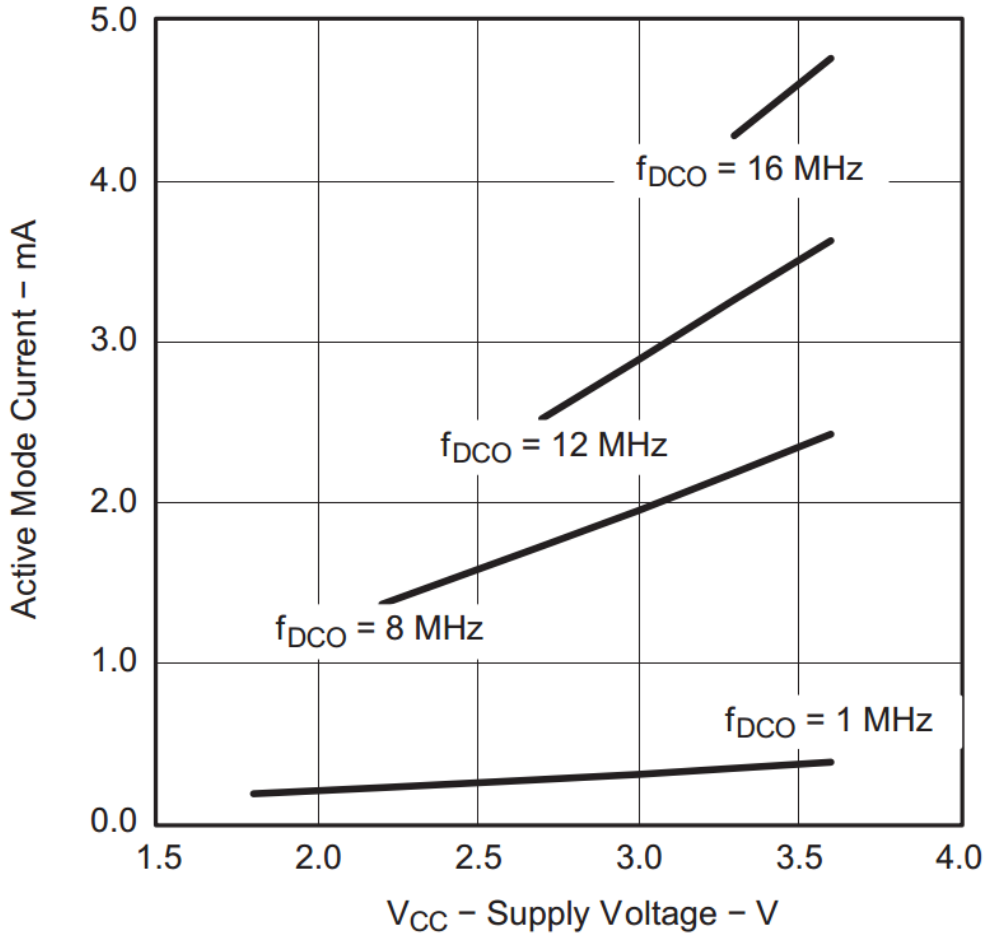


Figure 2: MSP430 Active Mode Current vs. Supply Voltage Range and System Frequency

The implications of this correlation between supply voltage and current consumption are of concern for applications running off of a battery. As the battery has a limited amount of capacity, denoted as mAh, reducing system current consumption is imperative to extending the life of the battery. Low-power microcontrollers, like MSP430, are popular choices for battery-powered applications by virtue of their low-power consumption. However, steps must be taken to ensure that this low-power operation is being taken advantage of.

One way to capitalize on this particularity of low-power microcontrollers is through Dynamic Voltage Scaling. This involves actively scaling the voltage either up or down depending on a particular mode of operation.

In the aforementioned example, a voltage of 2.2V or greater was required to program flash memory. Supplying 2.8V will render an Active Mode Current of 280µA, typically. However, if flash memory is not being programmed, the supply voltage can be dropped to 1.8V. In linear fashion, this will reduce the current consumption to a typical value of 180µA. This yields a 35.7% reduction in current consumption while maintaining the ability for the MCU to program flash memory or operate at a higher system frequency.

(It should be mentioned that the curve associated with a system frequency of 1MHz in Figure 2 has the most gradual slope. As the system frequency increases, the curve becomes steeper and the impact on current consumption becomes more pronounced.)

The correlation between operating voltage and current consumption is not anomalous to Active Mode. In the various Low-Power modes available, current consumption is reduced by lowering the supply voltage as shown in Figure 3:

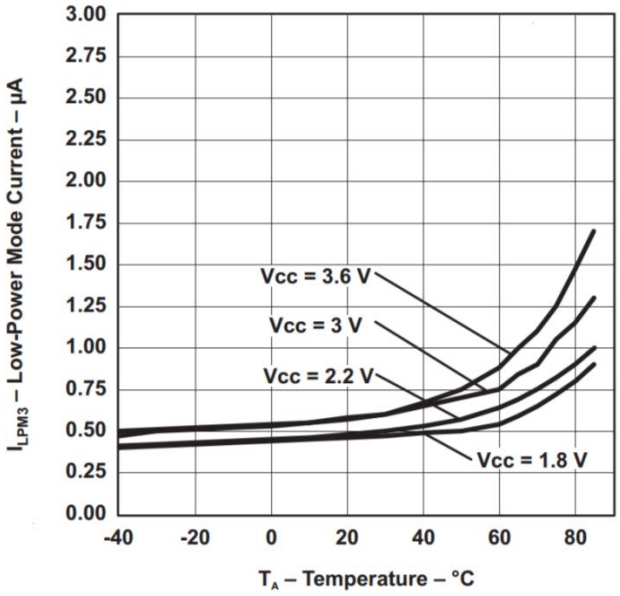


Figure 3: Low-Power Mode Current vs. Supply Voltage and Temperature

Assuming operation at room temperature (25°C) and a supply voltage set at 1.8V, the Low-Power Mode Current (for Low-Power Mode 3) is estimated to be 46µA. Increasing the supply voltage to 3V will result in a Low-Power Mode Current of 60µA. By operating at 1.8V instead of 3V, there is a 23.3% reduction in current consumption.

However, caution must be taken when selecting a regulator for such light loads (≤100µA). Along with the current being sourced to the load, the quiescent current of the voltage regulator must be considered when examining system current consumption. Quiescent current is the current requisite to maintain proper voltage regulation i.e. not being supplied to the load. The quiescent current of the LDO must be sufficiently small to preserve the low-power qualities of this mode. This can be seen via Equation 1 where the ground current contributes a loss comparable the dissipation created source current. Equation 2 is more representative of Active Mode where source current dwarfs ground current and renders it as negligible.

~

One solution for providing this functionality involves using a dual-voltage LDO like TLV7101828. This method requires that each channel has a separate enable pin. To see why, it's helpful to examine the functional diagram in Figure 4:

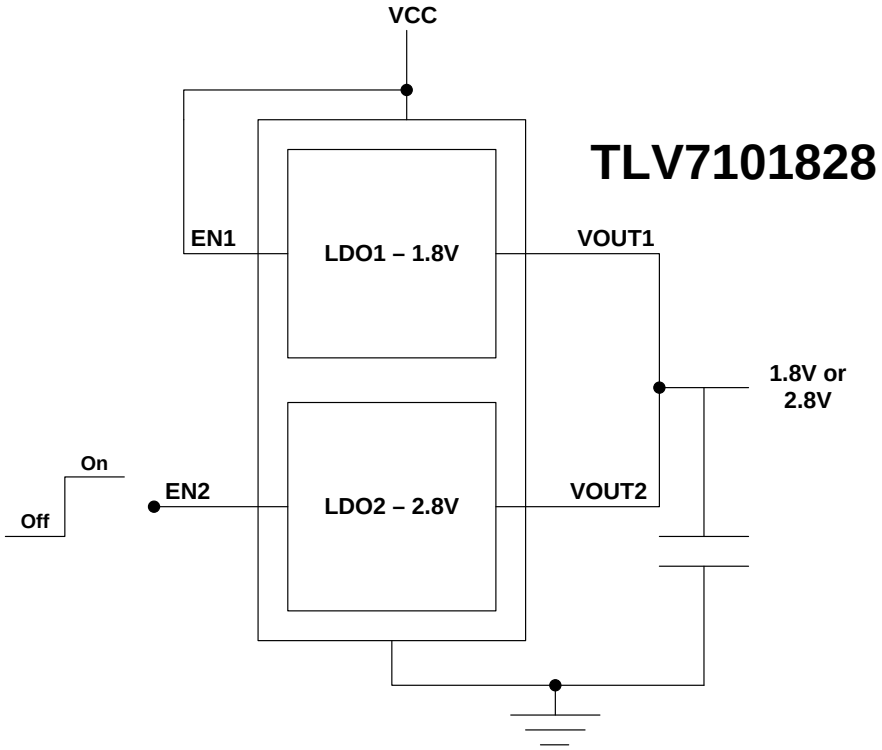


Figure 4: A Functional Representation of a Dynamic Voltage Scaling Dual LDO

As seen above, the dual-channel LDO has two channels: one output is rated 1.8V and the other is rated at 2.8V. The outputs are tied together and share a common output capacitor. The enable pin for the lower voltage channel is tied to the supply, effectively keeping it always enabled. The enable pin for the higher voltage channel, however, can be toggled via an I/O or some other logic.

When the higher voltage channel is disabled, the lower voltage channel regulates like it normally would. As a result, the joint output of the LDO will regulate at the lower voltage. In the case of TLV7101828, the output would be 1.8V.

However, if the higher voltage channel is enabled the output of the lower channel is driven above its 1.8V regulation point and the regulator control loop responds by shutting off the 1.8V internal pass device. At this time the output will regulate to the higher voltage channel of 2.8V.

The transition between the 1.8V and 2.8V levels is controlled by EN2 as shown in Figure 5. Transitions from the 1.8V to the 2.8V operation point are smooth and monotonic and typically occur within 200µs from when EN2 goes high. When EN2 is driven low the output will transition from 2.8V to 1.8V. In this case the transition time will depend on the output capacitance and load current.

3 Component Selection

There are a few considerations to keep in mind when deciding to use a dual LDO as a dynamic voltage scaling LDO.

3.1 LDO

Independent Enable Pins

As mentioned before, in order to properly switch between two different voltage levels, both channels must have independent enable functions. A common enable will not work in this configuration as the common output will always default to the higher voltage when enabled.

Transition time

Given that the many applications will be in Active Mode for a small percentage of the time (i.e. low duty cycle), it is important that the transition between voltage levels is quick enough in order to capitalize on power savings. This is expressed visually in Figure 5:

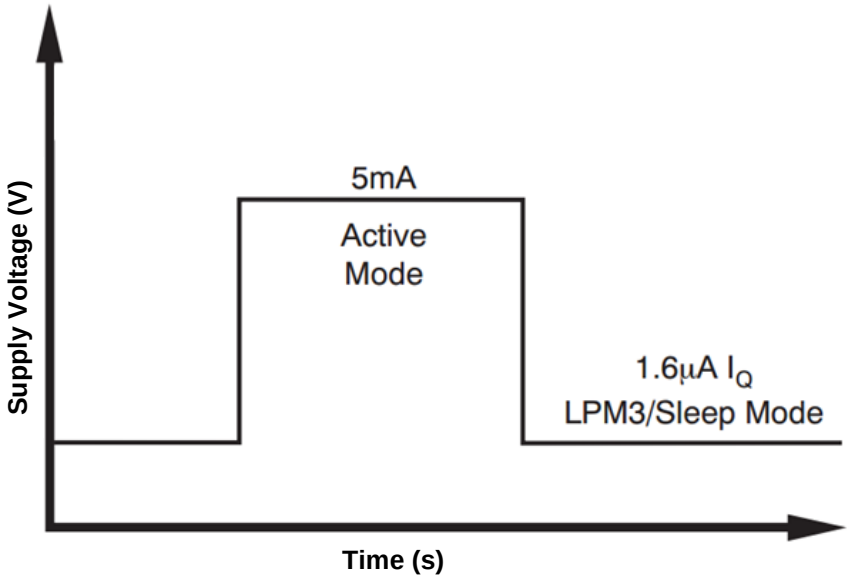


Figure 5: Current Consumption vs. Supply Voltage and Time

The figure shows that the MSP430 in Active Mode consumes considerably more current than in Low-Power Mode 3. Therefore, it is advantageous to spend as little time in Active Mode as possible in order to curb excess consumption. However, if it takes too long to transition the supply voltage from low-to-high or high-to-low, the application will incur higher losses than if the transitions were quick.

Active Output Discharge

Many fixed voltage LDOs are equipped with an Active Output Discharge. This feature allows the LDO output to discharge quickly by means of an internal resistor (usually 120Ω) when the LDO is disabled. This is beneficial in some applications because it leaves the output in a known, grounded state.

However, this feature can cause problems when used in the Dynamic Voltage Scaling configuration. Take a look at Figure 6. TLV7111830 has an Active Output Discharge on both of its channels. As the lower channel (1.8V) is always enabled, the Active Output Discharge function is only engaged when the higher channel (3.0V) is disabled. This turns on a FET that connects 120Ω of resistance to ground. Even without an actual load, the output will source at least 15mA through the resistor in this configuration.

This is problematic because the LDO is burning current unnecessarily. This negates the power savings that Dynamic Voltage Scaling provides.

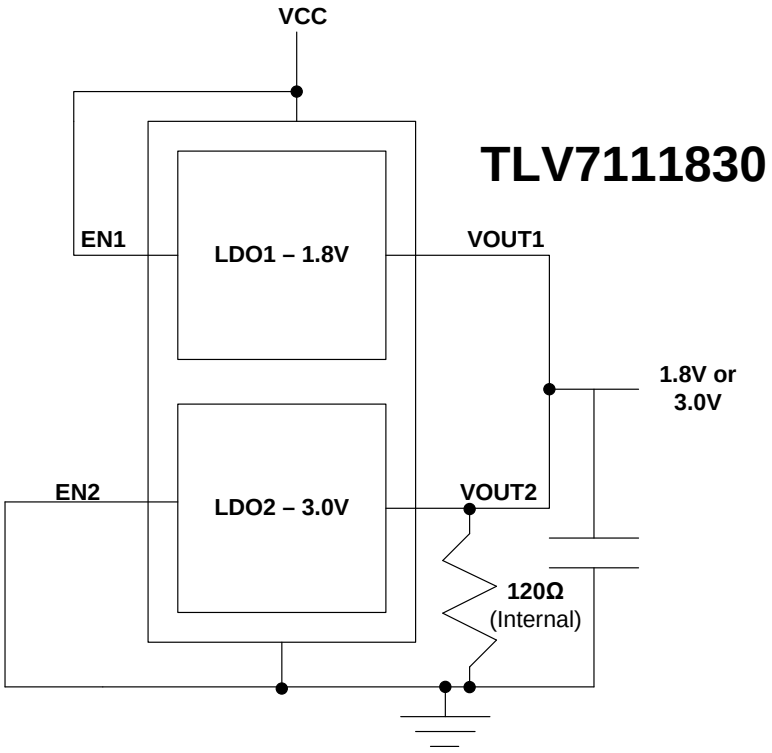


Figure 6: A Functional Representation of a Dynamic Voltage Scaling LDO with Active Output Discharge

Input and Output Capacitors

A common input pin is not required for this application. The supply voltage may be delivered via tied input pins as well (similar to the tying of the output pins). It's important to note that there's no need to bolster capacitance on either the input or output rail once the two channels have been tied together. The input and output capacitance requirements remain the same as if they were operating as two distinct channels.

4 PCB Design

The PCB schematic and bill of materials can be found in the Appendix.

4.1 PCB Layout

Testing of this reference design was done on the existing TLV7101828 evaluation board with the two outputs shorted together.

The PCB layout of the evaluation board used on this design is shown in Figures 7 and 8.

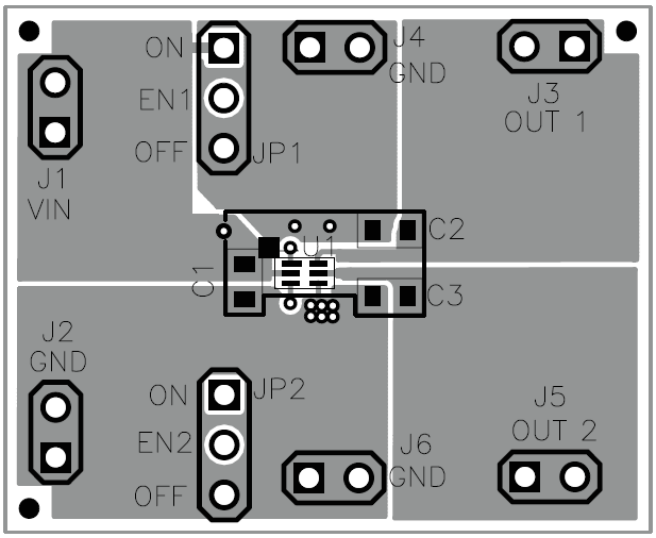


Figure 7: PCB Layout of Test Board (Top Side).

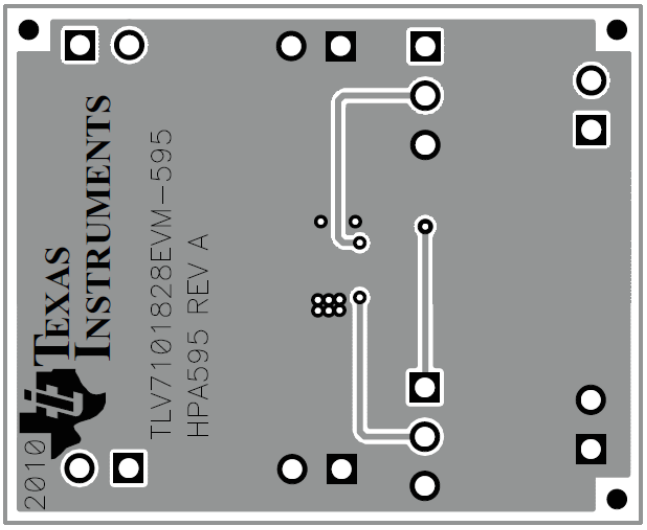


Figure 8: PCB Layout of Test Board (Bottom Side)

5 Verification & Measured Performance

5.1 Power-up, Power-down, and Enable Pulse Response

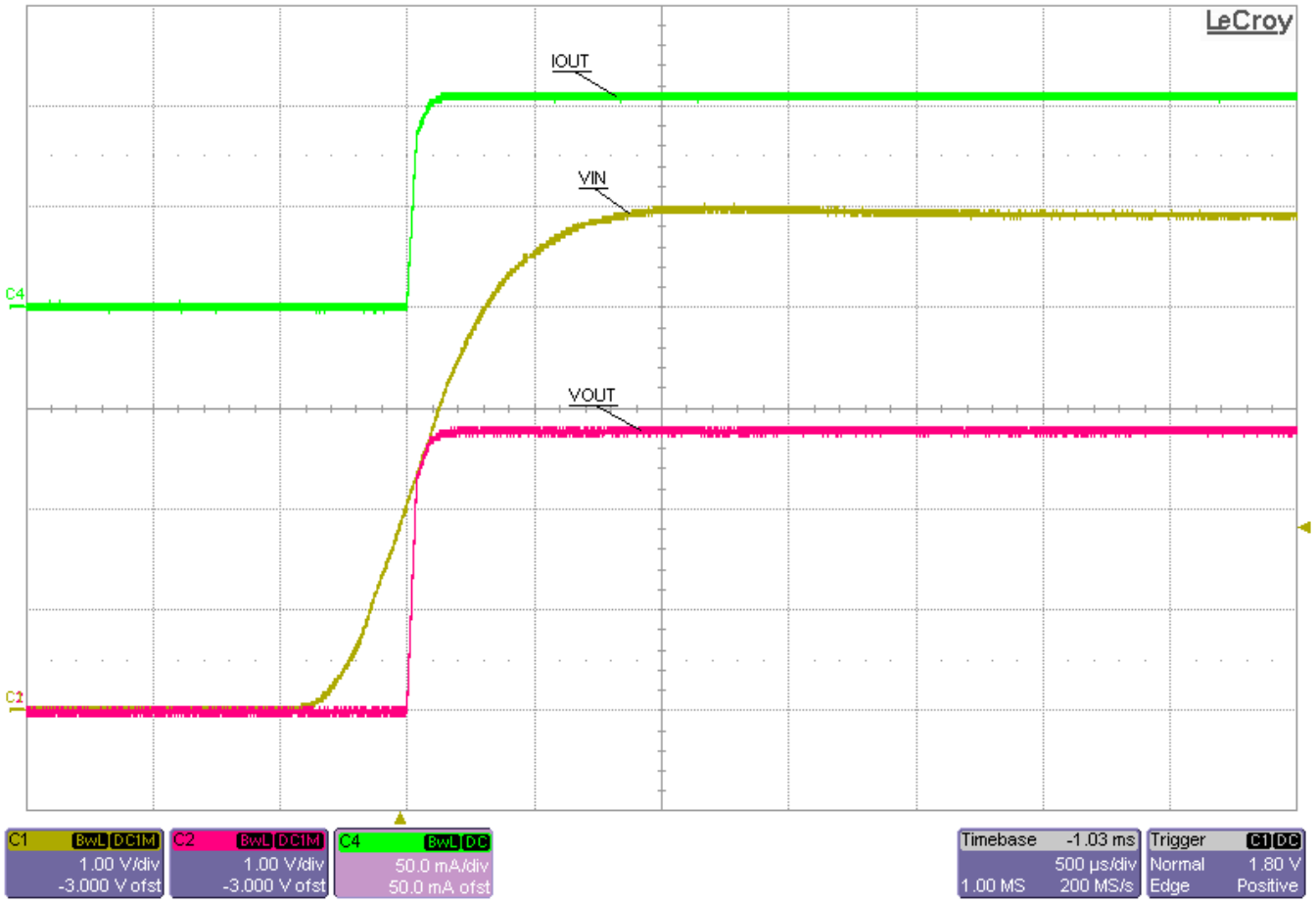


Figure 9: Power-up with the 2.8V channel enabled

With the 2.8V channel enabled, the common output ramps up monotonically to 2.8V during power-up. Monotonicity may be a requirement when powering digital loads.

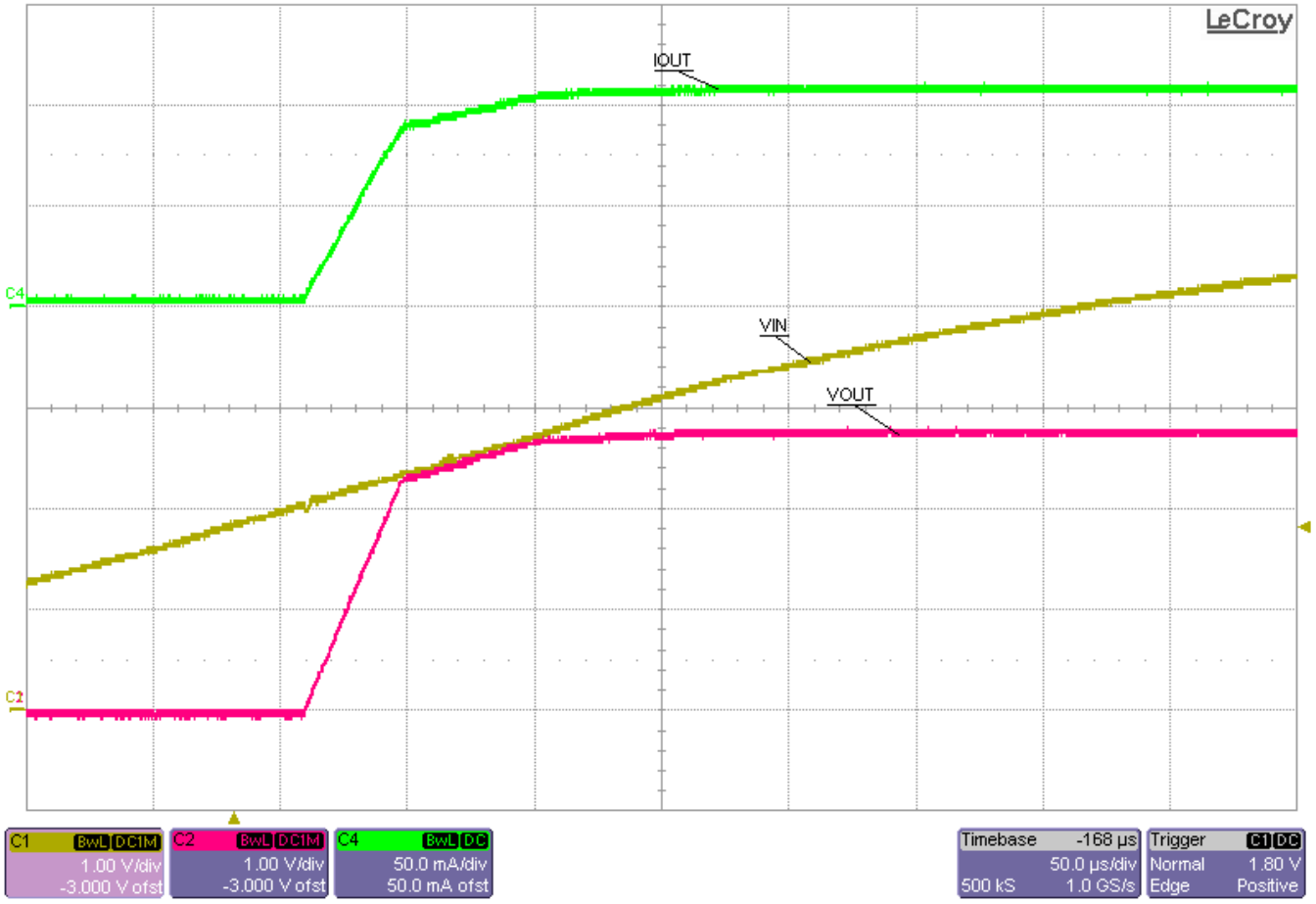


Figure 10: A magnified view of Power-up with the 2.8V channel enabled

This magnified view shows that the output voltage ramps to 2.8V in a steady, controlled fashion.

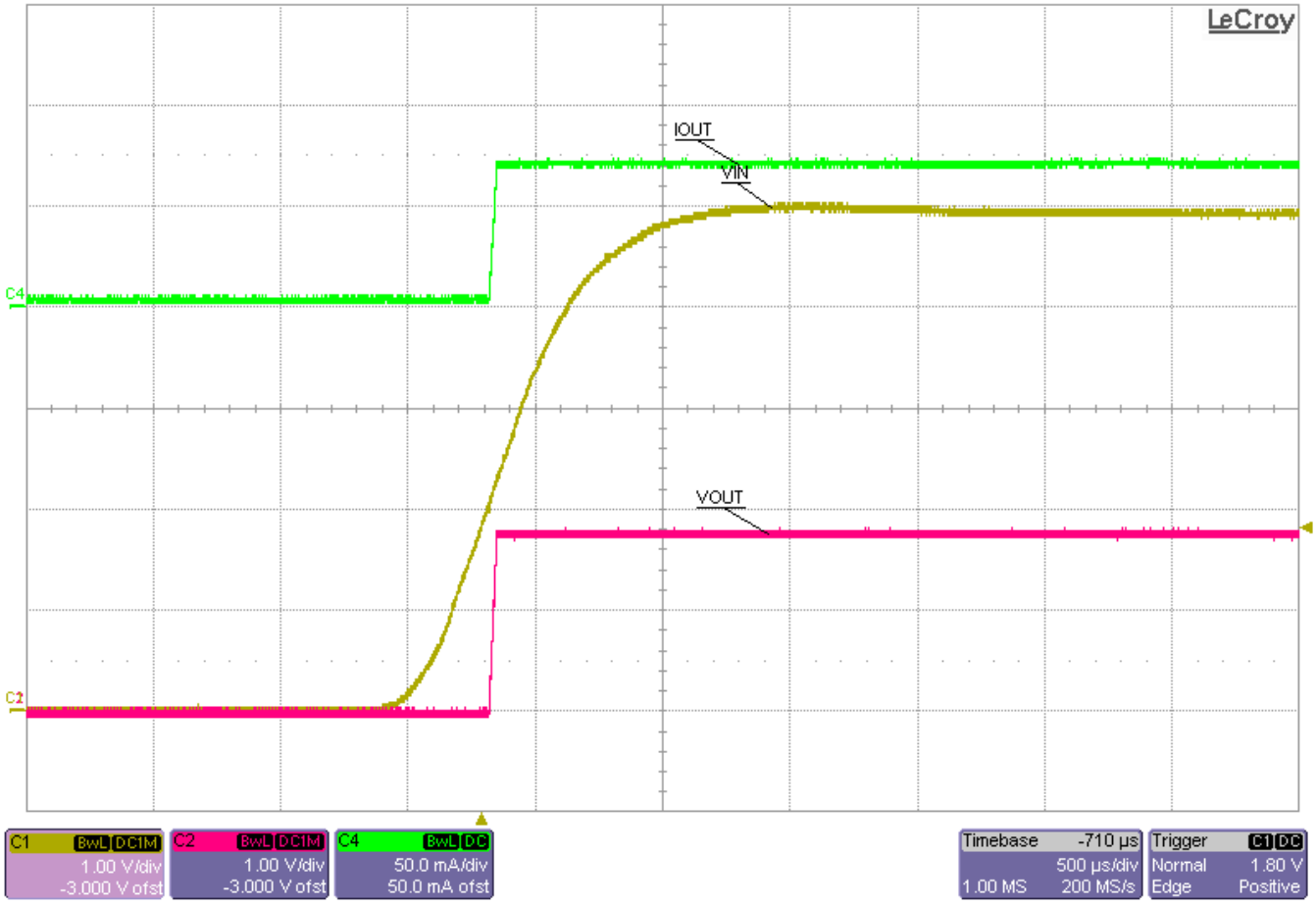


Figure 11: Power-up with the 2.8V channel disabled

Power-up, with the 2.8V channel disabled, similarly shows a smooth, controlled rise of the output voltage to 1.8V.

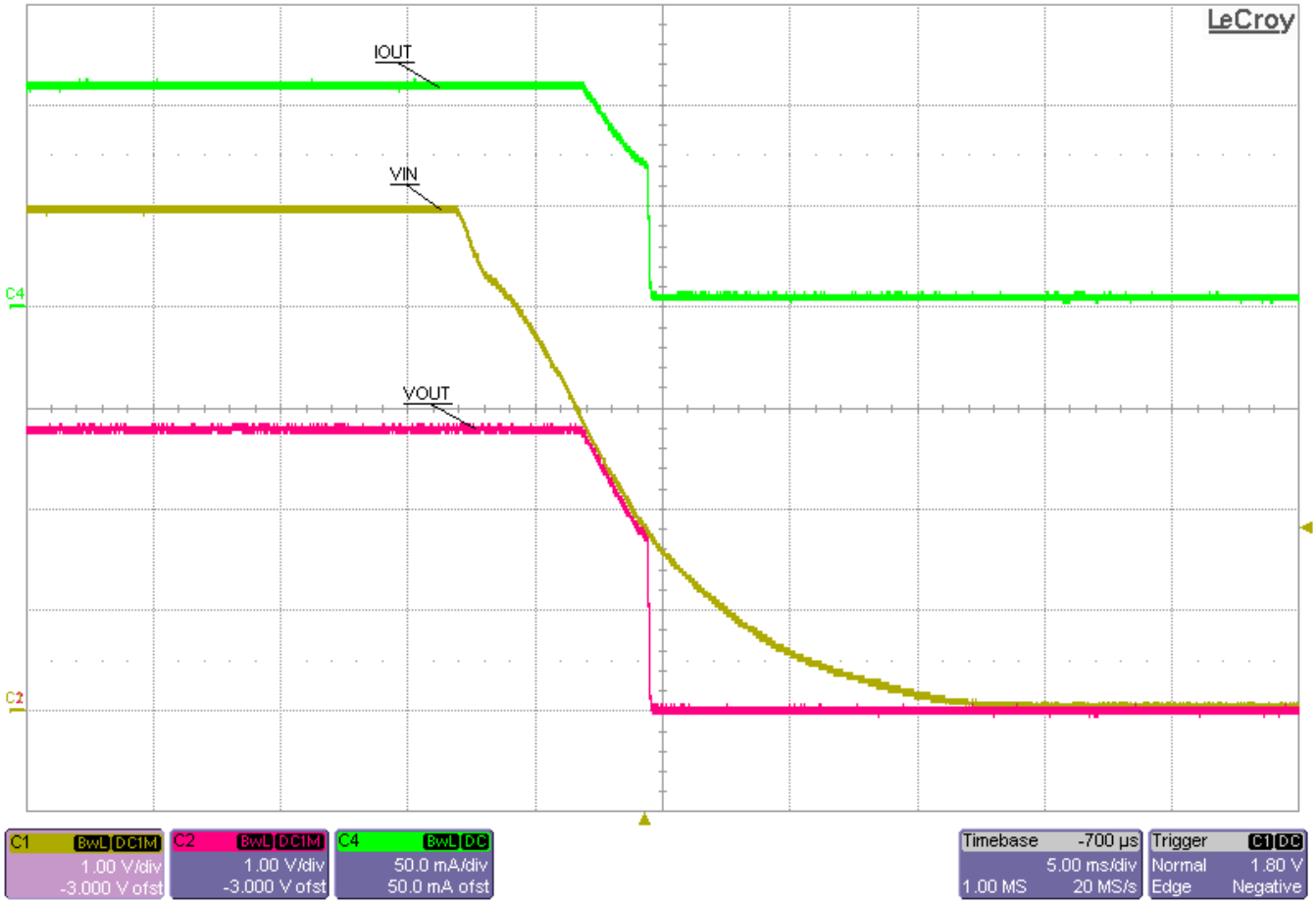


Figure 12: Power-down with the 2.8V channel enabled

The output voltage ramps down monotonically, as well.

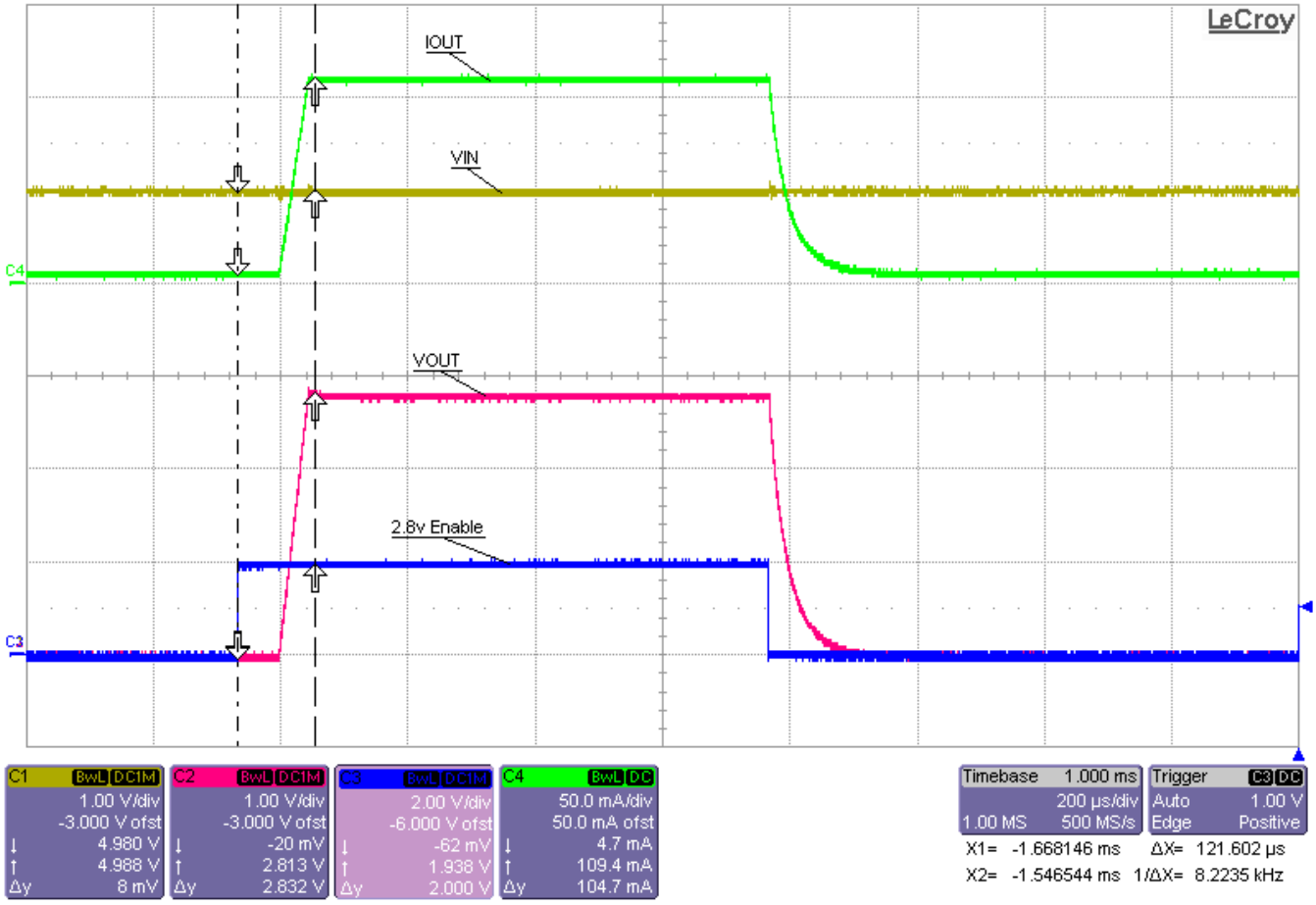


Figure 13: Enable Pulse Response

By tying both enable pins together and toggling them, the output voltage ramps up to and down from 2.8V. The enable pulse response exhibits similar characteristics to the power-up and power-down curves.

5.2 Voltage Scaling Response

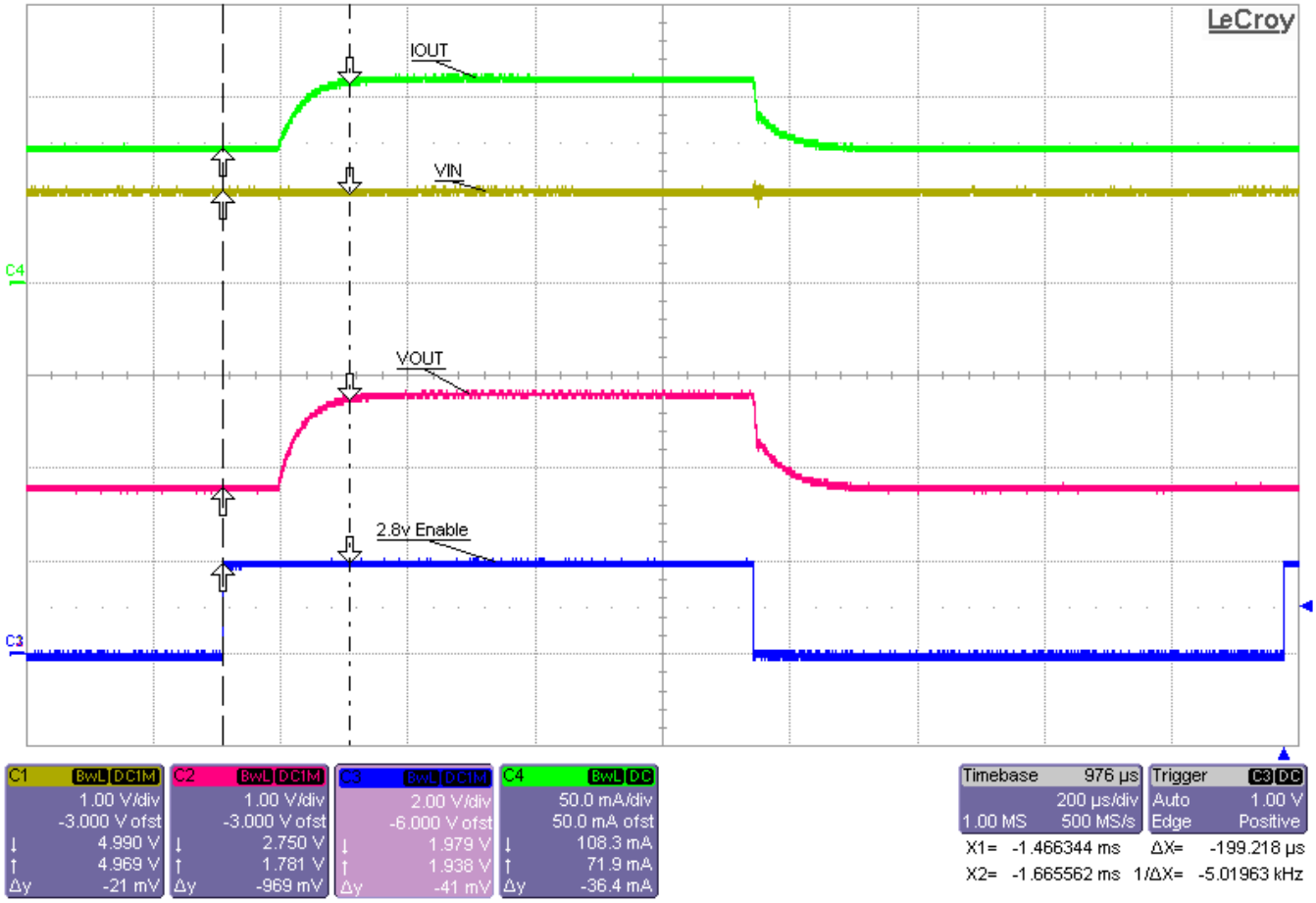


Figure 14: Transitioning the output voltage from 1.8V to 2.8V

When the output is at a steady 1.8V, enabling the 2.8V channel will initiate the output to scale up. There is nearly a 200µs delay associated with scaling up from 1.8V to 2.8V.

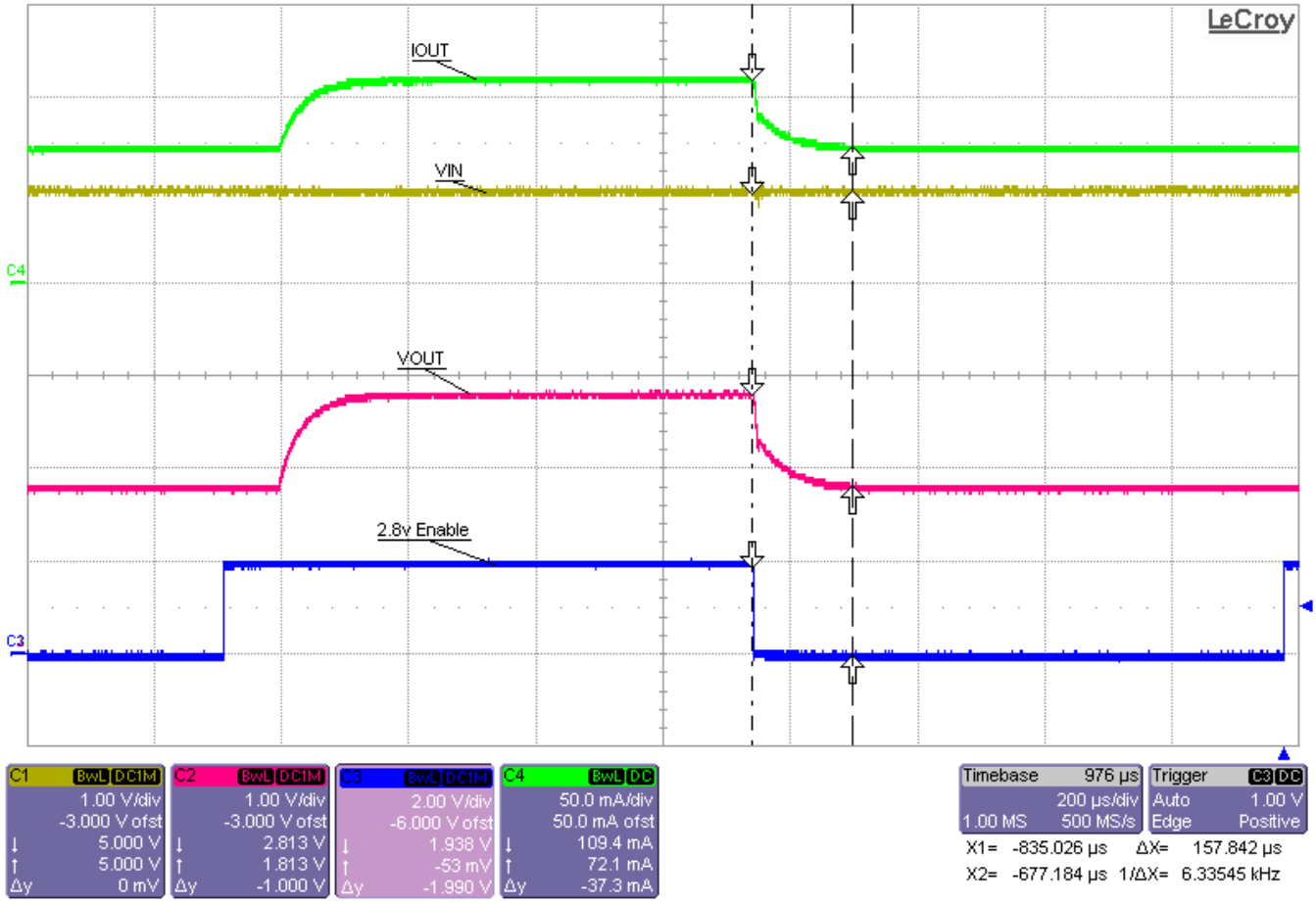


Figure 15: Transitioning the output voltage from 2.8V to 1.8V

Similarly, there is a delay when attempting to scale the output voltage down from 2.8V to 1.8V. This transition time was measured to be nearly 158µs.

5.3 Load Transient Response

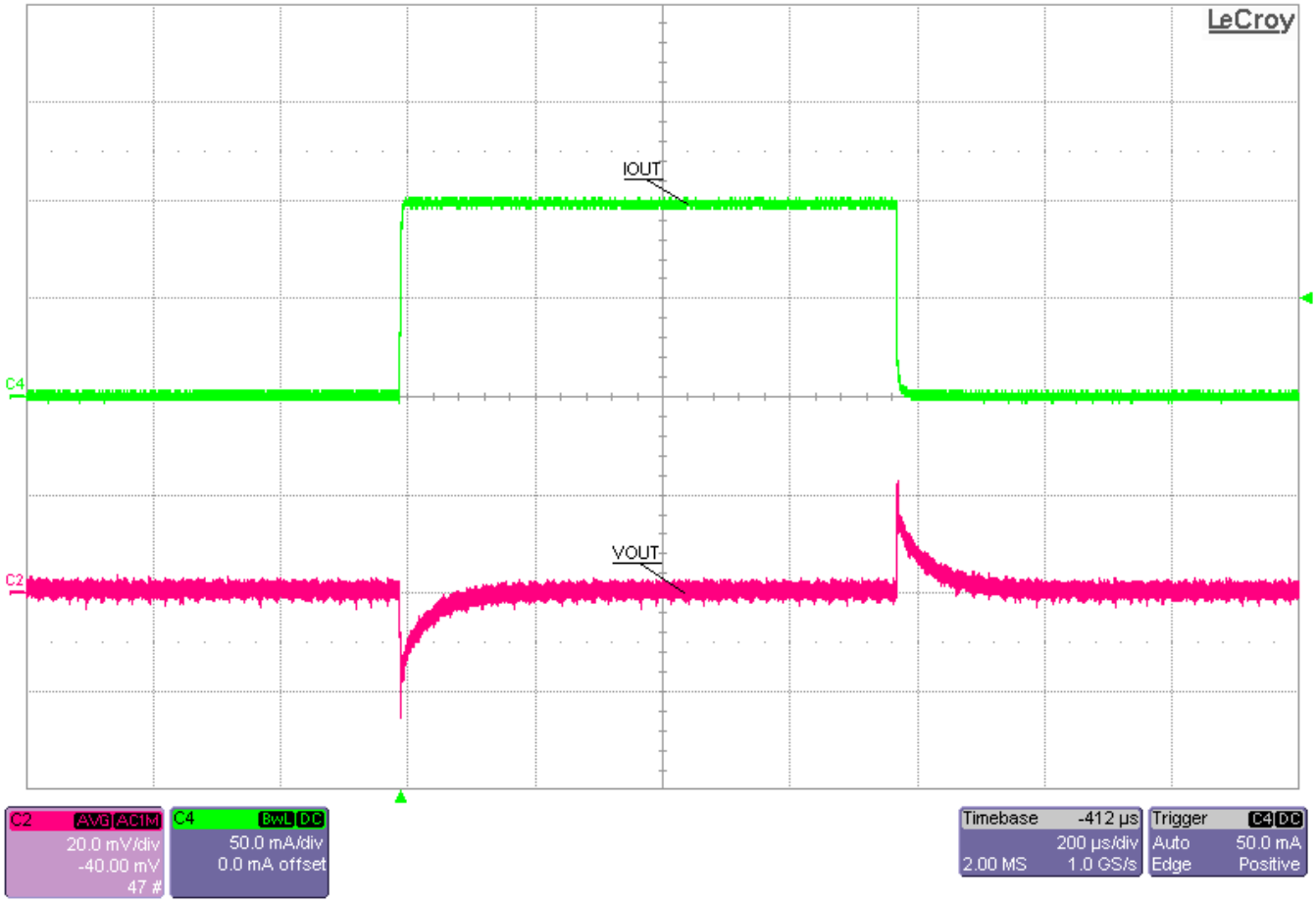


Figure 16: Load Transient Response with the 2.8V channel enabled

The load transient response, with the 2.8V channel enabled, shows very fast settling times (~100µs) and acceptable spikes (~60mV).

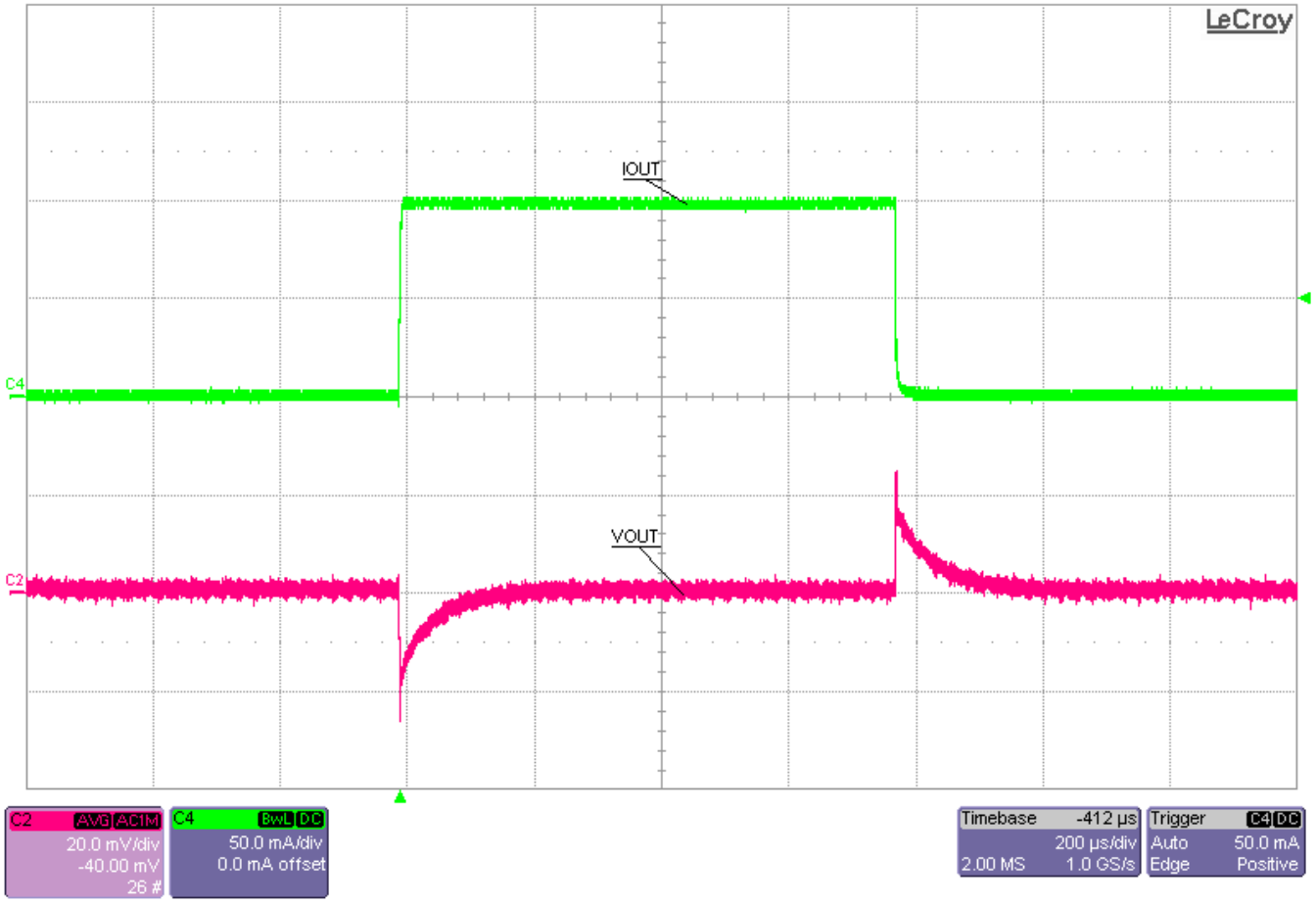


Figure 17: Load Transient Response with the 2.8V channel disabled

The load transient response remains the same even with the 2.8V channel disabled.

6 About the Author

Dennis Hudgins is an applications engineer in the Linear Power business unit. He has worked as an applications manager and applications engineer in various power product lines. Dennis received a BSEE from the Georgia Institute of Technology.

Aaron Paxton is a product marketing engineer in the Linear Power business unit. He received a BAEE/BSEE from the University of San Diego in 2012. He joined TI in 2012.

7 Acknowledgements

A special thanks to John Cummings for proposing this idea.

Appendix A.

A.1 Electrical Schematic

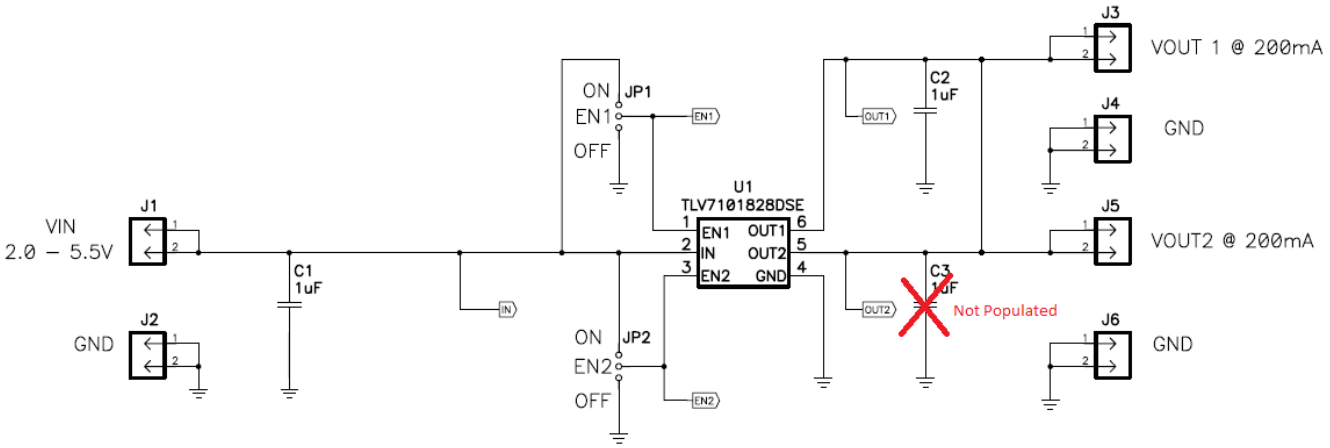


Figure A-1: Electrical Schematic

A.2 Bill of Materials

Texas Instruments

Bill of Materials

TI DESIGNS

TIDA-00387

Item	Qty	Reference	Value	Part Description	Manufacturer	Manufacturer Part Number	Alternate Part	PCB Footprint	Note
1	2	C1, C2	1uF	Capacitor, Ceramic, 6.3V, X5R, 20%	TDK	C1608X5R0J105M	C1608X5R0J105K	603	
2	1	C3	Not populated	-	-	-	-	-	Not Populated
3	6	J1, J2, J3, J4, J5, J6	PEC02SAAN	Header, 2-pin, 100mil spacing	Sullins	PEC02SAAN	-	0.100 inch x 2	
4	2	JP1, JP2	PEC03SAAN	Header, 3-pin, 100mil spacing	Sullins	PEC03SAAN	-	0.100 inch x 3	
5	1	U1	TLV7101828DSE	IC, Dual 200mA, LDO Regulator	TI	TLV7101828DSE	-	SON-6	

Figure A-2: Bill of Materials

IMPORTANT NOTICE FOR TI REFERENCE DESIGNS

Texas Instruments Incorporated ("TI") reference designs are solely intended to assist designers (“Buyers”) who are developing systems that incorporate TI semiconductor products (also referred to herein as “components”). Buyer understands and agrees that Buyer remains responsible for using its independent analysis, evaluation and judgment in designing Buyer’s systems and products.

TI reference designs have been created using standard laboratory conditions and engineering practices. **TI has not conducted any testing other than that specifically described in the published documentation for a particular reference design.** TI may make corrections, enhancements, improvements and other changes to its reference designs.

Buyers are authorized to use TI reference designs with the TI component(s) identified in each particular reference design and to modify the reference design in the development of their end products. HOWEVER, NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY THIRD PARTY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT, IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI REFERENCE DESIGNS ARE PROVIDED "AS IS". TI MAKES NO WARRANTIES OR REPRESENTATIONS WITH REGARD TO THE REFERENCE DESIGNS OR USE OF THE REFERENCE DESIGNS, EXPRESS, IMPLIED OR STATUTORY, INCLUDING ACCURACY OR COMPLETENESS. TI DISCLAIMS ANY WARRANTY OF TITLE AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, QUIET ENJOYMENT, QUIET POSSESSION, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS WITH REGARD TO TI REFERENCE DESIGNS OR USE THEREOF. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY BUYERS AGAINST ANY THIRD PARTY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON A COMBINATION OF COMPONENTS PROVIDED IN A TI REFERENCE DESIGN. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, SPECIAL, INCIDENTAL, CONSEQUENTIAL OR INDIRECT DAMAGES, HOWEVER CAUSED, ON ANY THEORY OF LIABILITY AND WHETHER OR NOT TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES, ARISING IN ANY WAY OUT OF TI REFERENCE DESIGNS OR BUYER’S USE OF TI REFERENCE DESIGNS.

TI reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques for TI components are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

Reproduction of significant portions of TI information in TI data books, data sheets or reference designs is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards that anticipate dangerous failures, monitor failures and their consequences, lessen the likelihood of dangerous failures and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in Buyer’s safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed an agreement specifically governing such use.

Only those TI components that TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components that have ***not*** been so designated is solely at Buyer's risk, and Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265