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Single-Ended Signal Conditioning Circuit for Current and Voltage Measurement Using Fluxgate Sensors

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Design Resources

TIDA-00208	Tool Folder Containing Design Files
OPA4322	Product Folder
ADS7853	Product Folder
ADS7253	Product Folder
TPS7A4700	Product Folder
TLV70033	Product Folder
REF5025	Product Folder
REF2033	Product Folder
TLC372	Product Folder
OPA322	Product Folder
LAUNCHXL-F28027	Tool Folder

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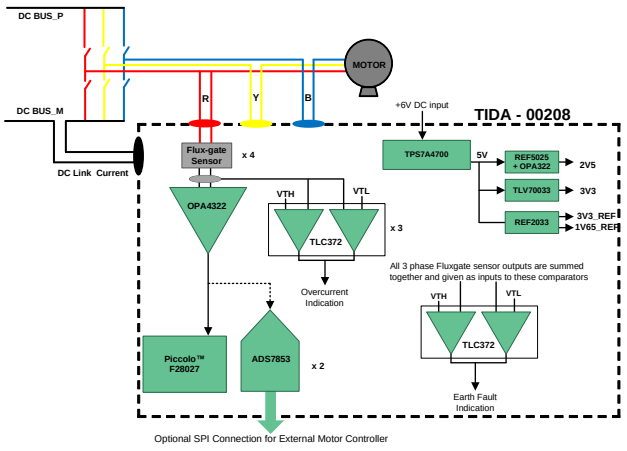
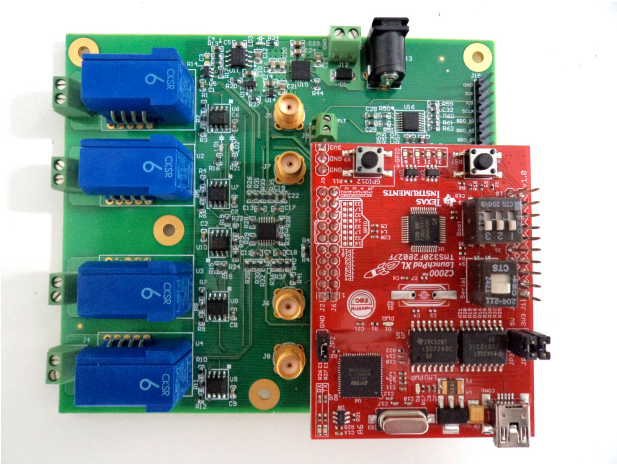
Design Features

- Designed to Measure All 3-Phase Motor Currents Along with DC-Link Current Through 6-A Fluxgate Sensor (Scalable up to 50 A)
- Single-Ended Signal Conditioning Circuit to Interface Fluxgate Sensors With Single-Ended ADCs
- Two Onboard 14-Bit Dual Channel Simultaneous Sampling SAR ADCs With 4-Wire SPI to Interface With External Motor Controllers
- Provision to Measure Current and Voltage Through Internal ADCs of TI's Piccolo™ Controller TMS320F28027
- < 0.1% DC Accuracy of Signal Conditioning Circuit
- Overload and Earth Fault Protections for Each Channels With <100-ns Sensing Delays
- Provision to Interface the Signal Conditioning Circuit With External ADC

Featured Applications

- AC Variable Speed and Servo Motor Drives
- Static Converters
- DC Motor Drives
- UPS Systems
- Solar Inverters
- Power Supplies for Welding Applications





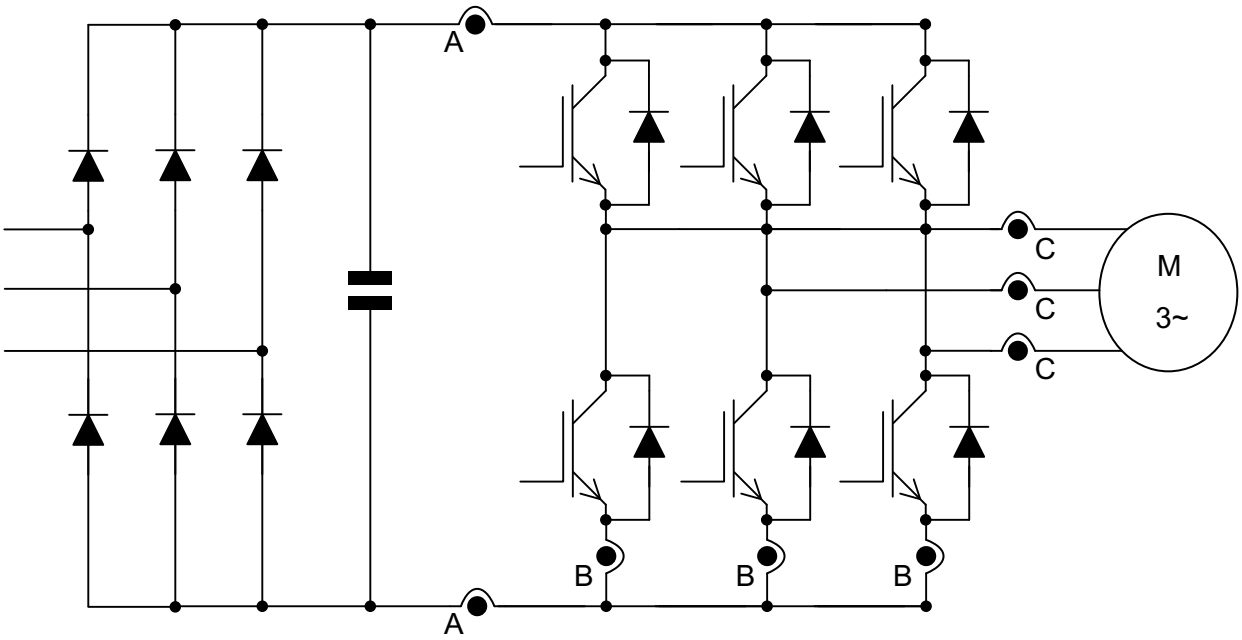
1 System Description

Current measurement is an inherent part of any inverter-driven application. One important reason for measuring the motor current is to control algorithm. Vector control and direct torque control require current sensing for control purposes. Approaches for sensorless control require the motor current measurement to provide accurate control with low cost and complexity. Information of motor parameters is important for several control schemes. Stator current measurement is used for the estimation of these parameters. Motor current information is also required to detect the motor's insulation condition. Electrical insulation is the most critical component for operating electrical motors. Stator insulation failure during motor operation can lead to motor failure, resulting in a costly outage.

Another important phenomenon is protection from hardware overload and earth fault conditions. Typically, these conditions occur when the current exceeds the limit of 200% or 300% of its nominal current. Derating must be taken into account when using the drive in different conditions. Ambient temperature or other environmental conditions such as dust or humidity are unknown, especially when a drive is not installed by the end-user but the machine manufacturer. The end user must identify all derating factors to reach a reliable solution.

Above the drive-designed ambient temperature, drives can usually operate when the maximum output current is derated according to the user's manual of the drive. The switching frequency also plays important role. The higher the switching frequency of the drive is, the more the power semiconductors generate heat losses. Therefore, the drive output current is derated when increasing the switching frequency, which applies to nominal current, overload current, and maximum instantaneous current.

The motor current can be measured at different points in the inverter. Figure 1 shows the overview of usual measurement locations, considering a 3-phase inverter for a motor control application:



A) Current measurement in the DC- and DC+ link
B) Current measurement in the bottom side emitter path of each half-bridge
C) Current measurement in the output phases

Figure 1. Typical Measuring Locations for Current Measurement in Motor Drives

From Figure 1, the least expensive variant of current measurement (*A*) is often used for applications in the lower power range. Typically, the current measurement is done on DC-MINUS bus, because this may be the reference potential of the microcontroller (MCU) and is therefore not necessary to isolate the signal. Another alternative location of current measurement, found particularly in the low-to-medium power range is variant *B*. In this case, the current is measured at the emitter of the bottom IGBT of each arm in a 3-phase inverter. The end user can also dispense with third current measurement as this can be derived by calculation based on the two measured current signals. The advantage of this measurement method is similar to that of variant *a*, in that the negative section of the DC-bus can be taken as the common reference potential. However, the disadvantage is the increased stray inductance. In high dynamic drives and high-power applications, current is usually measured in the output phases of the inverter (variant *C* in Figure 1). The third current sensor is not necessary in this case either.

The design TIDA-00208 is predominantly intended for current measurement using fluxgate sensors in AC motor drives, but the design can also be used for DC drives. The objective of this design is to provide a solution for single-ended signal conditioning circuit along with SAR analog-to-digital converters (ADCs) to measure motor current using fluxgate sensors, typically available from companies like LEM Technologies and VACUUMSCHMELZE. Designs commonly use single-ended ADCs integrated inside the controller for current measurement for industrial motor drives. This design overcomes inaccuracies by using low-cost front-end op-amps with proper filtering. This design also shows the front-end interfacing with the Piccolo series of MCUs (consisting of single-ended input ADCs) from Texas Instruments (TI).

The signal conditioning circuit for fluxgate current sensors is required for the following reasons:

- Fluxgate sensors have inherent noise at 450 kHz / 900kHz because of the internal oscillator and switching, so proper filtering is required.
- Typical fluxgate sensors have a reference signal on REF pin (always at 2.5 V) and signal output available on the OUT pin (±0.625 V riding on a 2.5-V reference). The output voltage of fluxgate sensors may not match the input range of ADCs (external or internal to the controller). In this scenario, level shifting may be required.
- Fluxgate sensors can measure up to 300% of their nominal rating. It is important to detect the overload condition and protect the drive.
- For a fluxgate sensor with nominal current (In) of 6 A with 300% of nominal current rating, the signal strength can vary from 0.625 V [2.5 – (3 × 0.625)] to 4.375 V [2.5 + (3 × 0.625)]. However, the ADCs integrated into microcontrollers can take 0 to 3.3 V, so level shifting is required.
- If using single-ended ADC inside Piccolo controllers, the common-mode voltage needs to be shifted from 2.5 V to 1.65 V, unlike the external ADCs.

2 Design Requirements

- To measure a 3-phase motor current and DC-Link current in a variable speed drive using fluxgate sensor (up to 6 A)
- Signal conditioning circuit with 0.1% accuracy to interface with a single-ended SAR ADC
- Simultaneous sampling of all current channels
- Hardware overload detection within < 100 ns
- Hardware earth fault detection within < 100 ns

3 Block Diagram

The system block diagram is shown in Figure 2. This design uses four fluxgate current sensors: three for the motor phase currents and one for measuring the current flowing through the DC-Link. Each of the sensors is interfaced with the quad low-noise op-amp OPA4322. The four outputs of OPA4322 are:

1. Connected to the onboard 14-bit SAR ADCs (ADS7853), the digital output of which is taken out on a connector to interface with external motor controllers or processors
2. Connected to the 40-pin connector to interface with the internal ADC of Piccolo TMS320F28027

To provide protection against overcurrent fault condition, each of the phases is provided with two fast responding comparators, the TLC372 (one for detection of overcurrent in a positive half-cycle and one for detection of overcurrent in a negative half-cycle). For ground fault detection, the output signals coming from each of the phases are combined together and compared against references using two TLC372s. Both protection circuits have a response time of less than 100 nanoseconds.

The entire board receives power from the 6-V DC power supply available on most of the industrial motor drives. The 6-V DC input is step-downed by a high-precision, low-noise low-dropout regulator (LDO) TPS7A4700 to generate 5 V. (TPS7A4700 has an input voltage range up to 36 V, so it can also be used in case a 15-V or 24-V supply is available). The 5 V is used to power the operational amplifiers (op-amps), onboard ADCs, and the fluxgate current sensors. For a digital supply, the low-cost LDO TLV70033 is used for 5-V to 3.3-V conversion. When used with 5-V ADCs, the output of op-amps should be biased at 2.5 V whereas when used with internal ADC of the Piccolo controller, the output should be biased at 1.65 V. The 2.5-V reference is generated using the REF5025 and OPA322 (used as buffer for reference). The REF2033 is used to generate reference voltage of 1.65 V and 3.3 V.

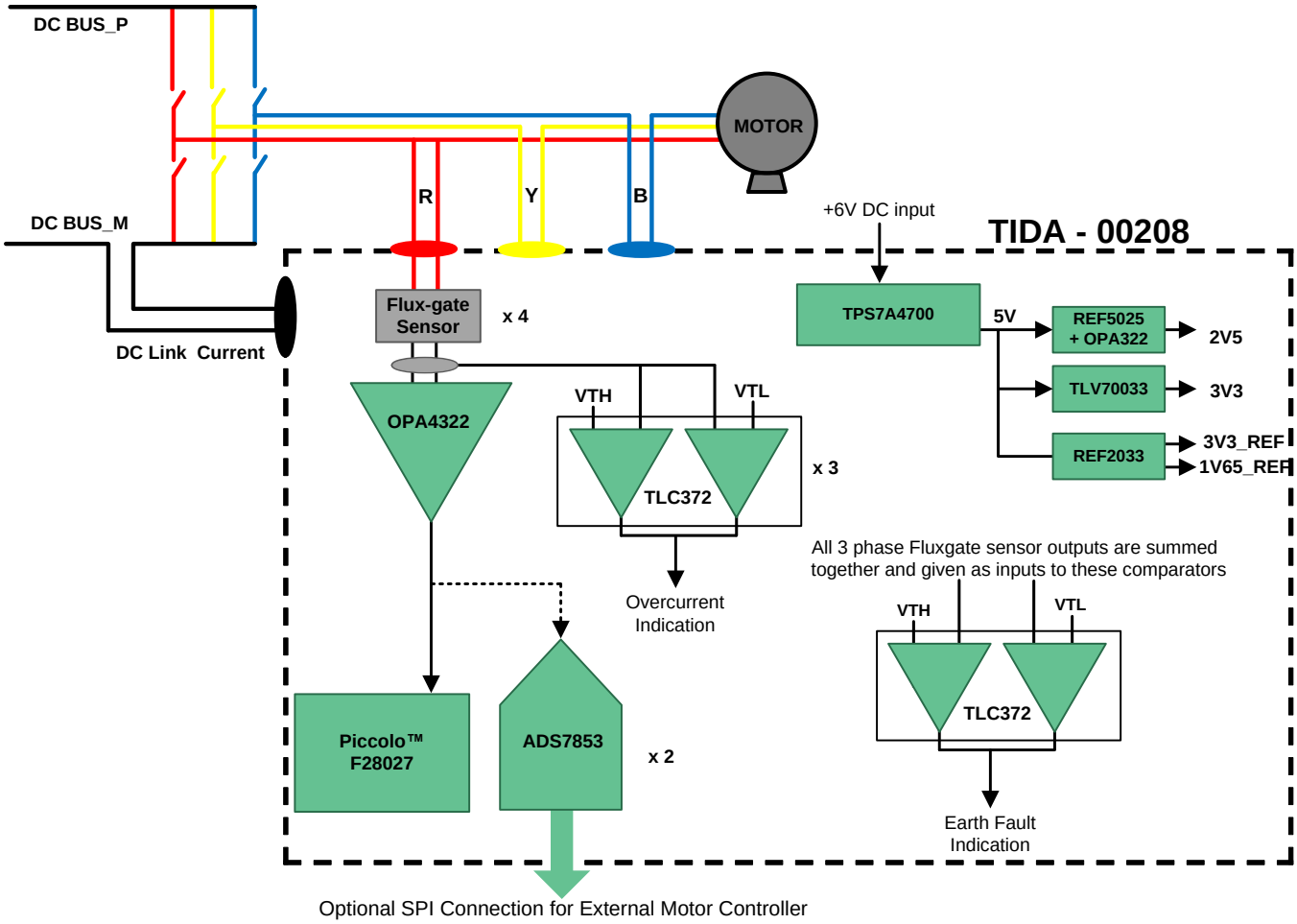


Figure 2. System Block Diagram

4 Highlighted Products

This reference design features the following devices from TI:

- OPA4322: Low-noise, 1.8-V, RRI/O, CMOS op-amp
- ADS7253 and ADS7853: Dual, high-speed, 12-bit and 14-bit, simultaneous-sampling, SAR ADCs
- TPS7A4700: 1-A, low noise (4.17μV_{RMS}), high-voltage LDO
- TLV70033: 200-mA, low IQ, LDO
- REF5025 - Low-noise, very low-drift, precision voltage reference
- OPA322 - Low-noise, 1.8-V RRIO, CMOS om-amp with shutdown
- REF2033: Low-drift, low-power, dual-output VREF and VREF / 2 voltage reference
- TLC372: Dual general purpose LinCMOS™ differential comparator

For more information on each of these devices, see their respective product folders at www.ti.com or click on the links for the product folders in Design Resources.

5 Fluxgate Technology

5.1 Open-Loop and Close-Loop Fluxgate Sensors

The operating principle of open-loop current transducers is shown in Figure 3 (taken from LEM Technologies' voltage transducer catalogue). The magnetic flux created by the primary current IP is concentrated in a magnetic circuit and measured in the air gap using a fluxgate device. The output from the fluxgate device is then signal conditioned to provide an exact representation of the primary current at the output.

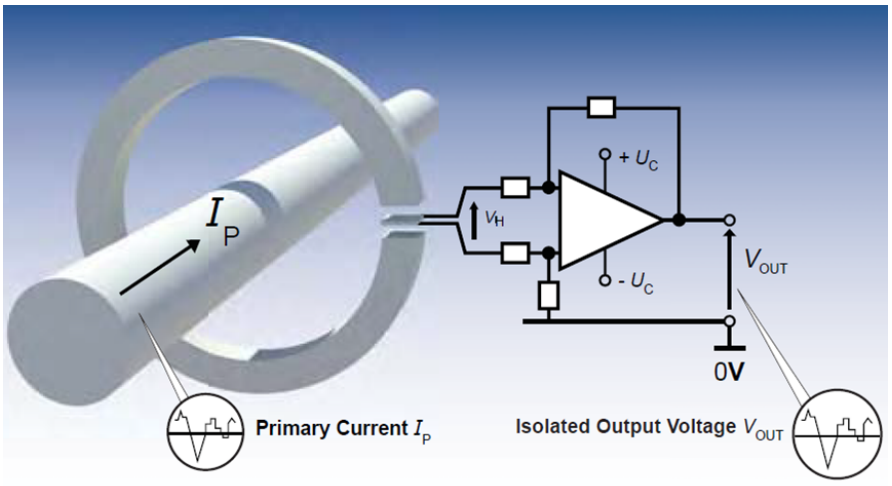


Figure 3. Open-Loop Fluxgate Sensor

On the other hand, the operating principle of a close-loop fluxgate sensor is that of a current transformer equipped with a magnetic sensing element, which senses the flux density in the core. As shown in Figure 4, the output of the field sensing element is used as the error signal in a control loop driving a compensating current through the secondary winding of the transformer. At low frequencies, the control loop maintains the flux through the core near zero. As the frequency rises, an increasingly large fraction of the compensating current is due to the operation in transformer mode. The secondary current is therefore the image of the primary current. In a voltage output transducer, the compensating current is converted to a voltage through a precision resistor and made available at the output of a buffer amplifier.

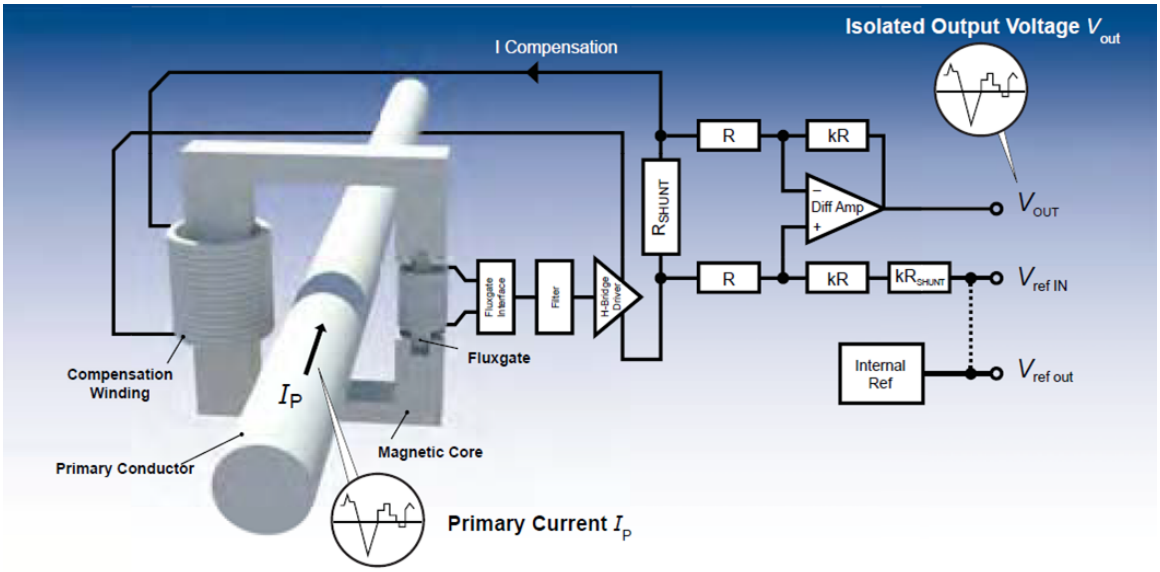


Figure 4. Close-Loop Fluxgate Sensor

5.2 Details of Fluxgate Sensor CKSR 6-NP From LEM Technologies

Selecting the right transducer is often a trade-off between several parameters: accuracy, frequency response, weight, size, costs, and so on. The CKSR 6-NP is a close-loop fluxgate sensor from LEM Technologies. The CKSR 6-NP typically measures current (DC, AC, or pulsed) with galvanic separation between the primary and secondary circuit. The internal structure of CKSR 6-NP is shown in Figure 5.

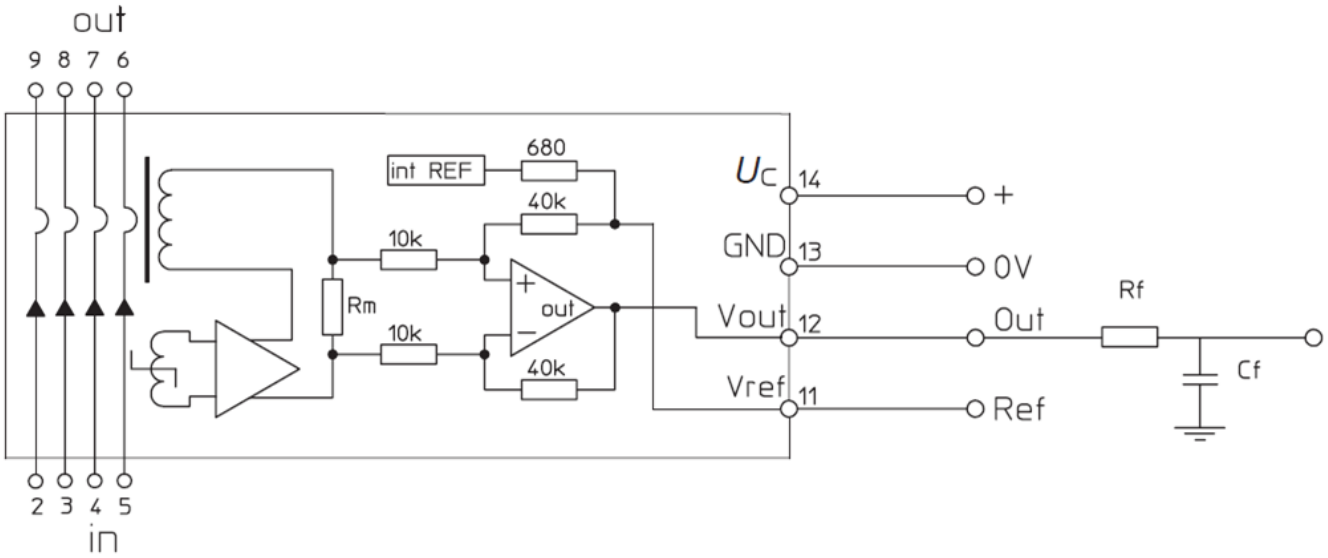


Figure 5. Internal Structure of CKSR 6-NP

The CKSR 6-NP can do bipolar measurements with a single unipolar 5-V power supply. The device can provide its internal voltage reference on an external pin (VREF) or receive an external voltage reference to share it with MCUs or ADCs. The output signal is available on the OUT pin, which is an amplified voltage signal proportional to the primary current. In a single-supply voltage, the output signal varies around a non-zero reference. In CKSR 6-NP, the output signal rides over a 2.5-V reference. The output voltage is proportional to the nominal primary current as shown in Equation 1.

$$VOUT = VREF \pm 0.625 \times \frac{I}{In} \quad (1)$$

where

- VOUT is output voltage
- I is the primary current
- In is nominal primary current (for example, In = 6 A for CKSR 6-NP)

Close-loop fluxgate transducers provide excellent accuracy at 25°C, generally below 1% of the nominal range, and a reduced error over the specified temperature range (–40°C to 105°C). Table 1 shows the accuracy data for CKSR 6-NP (taken from its datasheet).

Table 1. Accuracy of CKSR 6-NP

PARAMETER	SYMBOL	UNIT	MIN	TYP	MAX
Overall accuracy	X_G	% of I_{PN}			1.7
Overall accuracy at T_A = 85°C (105°C)	X_G	% of I_{PN}			2.2 (2.4)
Accuracy	X	% of I_{PN}			0.8
Accuracy at T_A = 85°C (105°C)	X	% of I_{PN}			1.4 (1.6)

6 Overcurrent and Earth Fault Protection

Contemporary state-of-the-art inverters are equipped with full IGBT protection, including overcurrent and earth fault protection. An overcurrent condition is one of the fatal drive faults that could destroy IGBT devices in a motor drive system. IGBT overcurrent conditions fall into three categories: ground fault, line-to-line short, and shoot-through.

Table 2. Overcurrent Conditions and Possible Causes

OVERCURRENT CONDITION	POTENTIAL CAUSE
Ground fault	Motor insulation breakdown to ground
Line-to-line short	Mis-wiring, motor leads short, motor phase-to-phase insulation breakdown
Shoot-through	False IGBT turn-on

Table 2 lists overcurrent conditions and their potential causes. When considering an IGBT overcurrent protection scheme, evaluate two important factors. The first factor is what type of overcurrent protection the system must provide and how the system can shut down. The second factor is the control architecture. Control architecture significantly influences the method and implementation of the overcurrent protection. Protection of IGBT devices is normally implemented in the hardware circuit. However, the circuit implementation and the type of overcurrent-sensing device vary depending on which overcurrent condition is being addressed.

This design implements the overcurrent protection using two comparators for each phase. The two thresholds are derived from the output voltage coming from fluxgate sensors (one for the positive cycle and one for the negative cycle). On the other hand, the earth fault protection is implemented by adding the three signals coming from current sensors connected in each phase and compared against two thresholds (one for the positive cycle and one for the negative cycle).

The total propagation delay of shutdown also is important. The current sensor itself has some delay, which includes delay for the sensing mechanism and its own response time. Therefore, no matter how the protection circuit is implemented, this delay time must be added to the circuit delay to meet the IGBT short-circuit duration time.

7 Component Selection and Circuit Design

7.1 Selection of ADC

- Input voltage range: CKSR 6-NP fluxgate sensor provides a 2.5-V reference output and an output voltage proportional to primary current riding on a 2.5-V reference signal. The output voltage corresponding to the measured current is given by VREF – VOUT. This differential signal can go up to 300% of its nominal output (that is, ±0.625 × 3 = ±1.875 V).
- Number of channels: The three phases (R, Y, and B) and DC-Link current measurement require four channels. It is better to have four ADCs that can be simultaneously sampled.
- Simultaneous sampling: For optimal 3-phase motor control, it is important to take simultaneous current measurements for each of the phases.
- Sampling speed: A typical industrial motor drive application uses a sampling frequency of 100 to 250 kSPS, so the minimum sampling frequency required for the selected ADC is 300 kSPS.
- Number of bits (resolution): Generally, 12 to 14 bits of resolution is enough for an industrial motor drive using fluxgate sensors.
- Supply voltage: Since the CKSR 6-NP has an operating voltage range from 4.75 to 5.25 V, use an ADC with a supply voltage of 5 V.
- Reference requirement: Have internal as well external reference options on hand.

ADS7253 and ADS7853 are suitable devices for the mentioned criteria. The features of ADS7253 and ADS7853 are as follows:

- Pin compatible family: 12 to 14 bits
- Simultaneous sampling of two channels (If the /CS signal of two ADS7x53 devices combine, all four ADCs — two in each ADS7x53 — can be sampled simultaneously).
- Sampling speed: 1 MSPS
- Single-ended and pseudo-differential inputs
- Excellent DC/AC performance
- Dual, programmable, buffered 2.5-V internal reference for gain calibration
- Extended temperature range: –40°C to 125°C

7.2 Selection of Operational Amplifier

The op-amp is a critical piece of the analog signal chain and can often have a dramatic impact on the performance of the entire signal chain. The primary functions of this op-amp are:

1. To buffer the inputs coming from the sensor
2. To amplify the low level input signals coming from the sensor
3. To provide the desired common-mode voltage at the output

Table 3 gives a comprehensive list of the factors that need to be considered in determining the choice of the op-amp.

Table 3. Selection Considerations for the Op-Amp

REQUIREMENT	BENEFIT
High input impedance	Minimizing this reduces input loading on sensor, and minimizes input current offsets on input resistors.
Input current noise	Minimizing this reduces the amount of current noise that becomes converted to voltage noise on input resistors.
Voltage noise	Minimizing this improves the overall signal-to-noise ratio.
CMRR versus frequency	Maximizing this reduces the amount of input offset changes due to high dv/dt at the inverter output.
Voltage offset drift	Minimizing this reduces the amount that the total unadjusted error changes at the output of the op-amp.
Single-supply operation	Designing a single-supply amplifier simplifies the system supply requirements, which usually correlate with a lower power architecture.
Input type	A rail-to-rail input can help to interface sensors that have large input swings.
Output type	With a rail-to-rail output configuration, the amplified input signal can reach the supply voltage and can use the FS range of ADC in a more successful way.

This reference design uses OPA4322 as front-end amplifier for ADC. The OPA4322 is a quad-channel CMOS op-amp featuring low noise and rail-to-rail I/Os optimized for single-supply applications.

7.3 Selection of External Voltage References

TIDA-00208 uses ADS7253, which has an external reference voltage range from 2.4 V to AVDD (or 5 V) as shown in Table 4 (taken from the ADS7253 datasheet).

Table 4. Voltage Reference Input Limits

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VREF reference voltage (input)	±VREF range	2.4	2.5	AVDD	V
	2 × VREF range	2.4	2.5	AVDD / 2	V

The design needs an external reference IC that can provide 2.5 V. The REF5025, selected for this reference, is a low-noise, low-drift, very high-precision voltage reference.

On the other hand, the internal ADC of a controller can take a maximum voltage of 2.5 V on the analog input pins. For signals coming to the inputs of internal ADCs, the common-mode voltages must be at mid-scale to bias the input bipolar signals. The REF2033 can provide two voltages: 1.65 V and 3.3 V.

7.4 Selection of Comparator

A typical industrial drive needs to have overcurrent and earth fault protection to operate within 300 nanoseconds. To reach this goal, the following comparators are compared and TLC372 is selected. The TLC372 has a 200-nanosecond response time. Table 5 shows the comparison chart.

Table 5. Comparison Chart for Comparator Selection

PARAMETER	LM293	LM293A	TLC372	TLV1702	LMV7235	LM6511	TLV1391
No. of Channels	2	2	2	2	1	1	1
Supply voltage (min) in Volts	2	2	3	2.2	2.7	2.5	2
Supply voltage (max) in Volts	36	36	16	36	5.5	30	7
T(RESP) low-to-high (in µS)	1.3	1.3	0.2	0.78	0.075	0.18	0.7
Output type	Open-collector, Open Drain	Open-collector, Open Drain	Open-collector, Open Drain	Open-collector	Open-drain, Push-pull	Open-collector	Open-collector, Open Drain
Input offset voltage (in mV) - Max	5	2	5	0.3	6	8	9
Input offset current (in nA) - Max	50	50	0.001	0.5	200	200	150
Input bias current (in nA) - Max	250	250	0.03	20	400	50	400
Supply current (in mA) - Max	1	1	0.3	??	0.1	5	0.175
Packages available	SOIC-8, VSSOP-8, PDIP-8	SOIC-8, VSSOP-8, PDIP-8	SOIC-8, TSSOP-8, PDIP-8, SO-8	MSOP8-, QFN-8	SOT-23, SC-70	SOIC-8	SOT-23
Temperature (in °C)	–25 to 85	–25 to 85	–40 to 125	–40 to 125	–40 to 85	–40 to 85	–40 to 85

7.5 Selection of Power Devices: Voltage Regulators

The entire board is powered using the 6-V DC power supply available on most of the industrial motor drives. The drive can also have 24-V or 15-V supplies available. To step down the 6-V DC input to generate 5 V, the board requires a high-precision, low-noise LDO. The 5-V is used to power op-amps, onboard ADCs as well as the fluxgate current sensors, so the total current output requirement from the LDO is at least 500 mA.

The TPS7A47 is a family of positive voltage (36 V), ultra low-noise (4 μV_{RMS}) LDOs capable of sourcing a 1-A load. The TPS7A4700 output voltages are user-programmable (up to 20.5 V) using a printed circuit board (PCB) layout without the need of external resistors or feed-forward capacitors, which reduces the overall component count. The TPS7A47 is designed with bipolar technology primarily for high-accuracy, high-precision instrumentation applications where clean voltage rails are critical to maximize system performance. This feature makes the device ideal for powering op-amps, ADCs, digital-to-analog converters (DACs), and other high-performance analog circuitry. (TPS7A4700 has an input voltage range up to 36 V, so the device can also be used in case a 15-V or 24-V supply is available). The digital supply requires a low-cost LDO to convert the 5 V to 3.3 V with a <200-mA output current capability. The TLV70033 is a 3-pin, low-cost LDO that can provide the 200-mA current to convert the 5 V to 3.3 V.

8 Circuit Design

8.1 Decoupling for Fluxgate Current Sensor

As per the CKSR 6-NP datasheet, the internal fluxgate oscillator draws current pulses of up to 30 mA at a rate of 900 kHz. A significant 900-kHz voltage ripple on the supply pin (Vc) can indicate a power supply with high impedance. At these frequencies, the power supply rejection ratio is low, and the ripple may appear on the transducer output Vout and reference Vref. The transducer has internal decoupling capacitors, but in the case of a power supply with high impedance, it is better to use local decoupling (100 nF or more, located close to the transducer).

In this design, the fluxgate sensor is decoupled using the 1-µF ceramic capacitor (as shown in Figure 6). The capacitor is placed very close to the sensor in the layout.

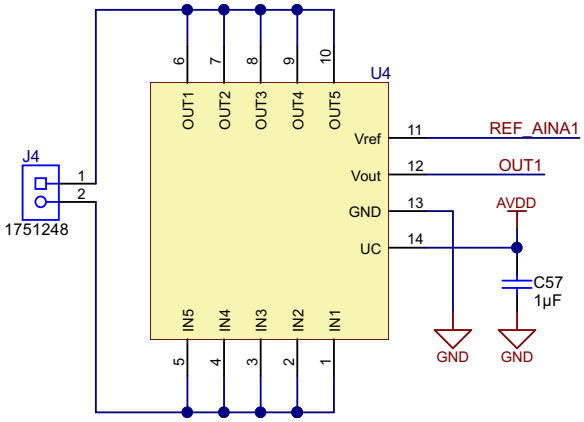


Figure 6. CKSR 6-NP with Capacitor Decoupling on Supply Pin

8.2 Designing the ADC Input Stage

Converting analog-to-digital signals requires sampling an input signal at a constant rate. Any higher frequency content in the input signal beyond half the sampling frequency is digitized and folded back into the low-frequency spectrum. This process is called aliasing. Therefore, an analog anti-aliasing filter must remove the harmonic content from the input signal before being sampled by the ADC. An anti-aliasing filter is designed as a low-pass RC filter, for which the 3-dB bandwidth is optimized based on specific application requirements. A high-bandwidth filter is required to allow accurately settling the signal at the ADC inputs during the small acquisition time window. For AC signals, the filter bandwidth should be kept low to band-limit the noise fed into the ADC input, thereby increasing the signal-to-noise ratio (SNR) of the system. The datasheet of ADS7253 suggests the component values for anti-aliasing filter as shown in Figure 7:

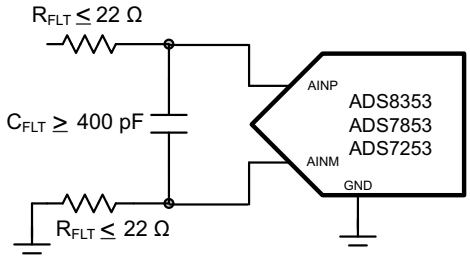


Figure 7. Anti-Aliasing Filter for ADS7x53

The cut-off frequency of anti-aliasing filter is calculated using Equation 2.

$$f_{-3db} = \frac{1}{2\pi \times (R_{FLT} + R_{FLT}) \times C_{FLT}} \quad (2)$$

Designing the input stage is a two-step optimization process:

1. Select a noise rejection input capacitor that charges the sample-hold capacitor (C_{SH}).
2. Identify an op-amp that can consume low power and recharge the input capacitor.

A filter capacitor, C_{FLT}, which connects across the ADC inputs and filters the noise from the front-end drive circuitry, reduces the sampling charge injection and provides a charge bucket to quickly charge the internal sample-and-hold capacitors during the acquisition process. The noise reduction filter block consists of a capacitor, C_{FLT}, which is added between the two input pins as shown in Figure 8. This block helps minimize noise by attenuating the kick-back noise from the ADC and also by band-limiting the broadband noise of the op-amp.

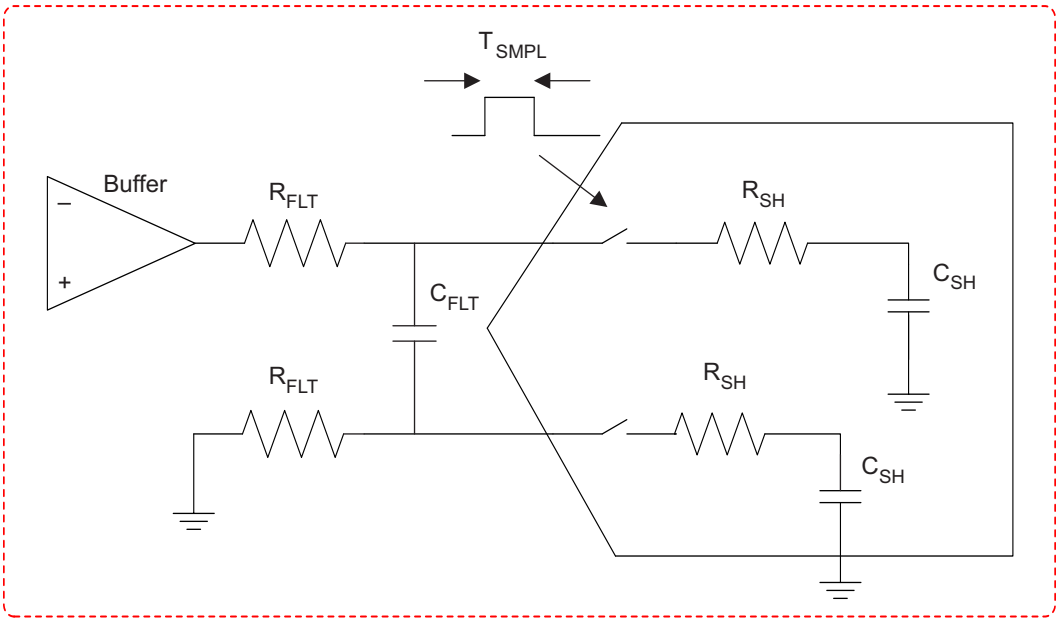


Figure 8. Input Capacitor C_{FLT} for Attenuating Noise

This filter capacitor acts as a charge reservoir by providing the charges to C_{SH} during acquisition time. The op-amp delivers charges to the capacitor to bring it up to the input voltage *V* as shown in Figure 9. This capacitor must be large enough to charge or discharge the sample-hold capacitor during acquisition time and retain 95% of its initial voltage.

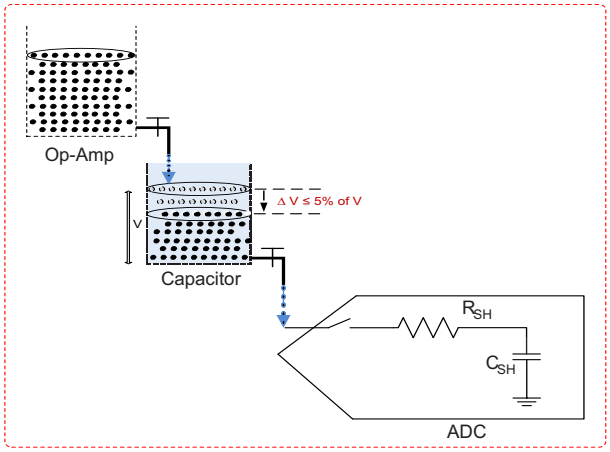


Figure 9. Filter Capacitor Delivering Charges to C_{SH}

The sampling capacitor inside ADS7x53 has a typical value of 40 pF. When the input is at its maximum, C_{SH} has to be charged to 2xVREF during the sampling time. The corresponding charge needed is approximately 200 pC (40 pF × 5 V). While delivering 200 pC to C_{SH}, the voltage across this capacitor should not drop below 5% of its initial voltage, which is VREF to keep the op-amp in its linear operating region (no slew).

As a rule of thumb, the value of this capacitor should be at least 20 times the specified value of the ADC sampling capacitance. For these devices, the input sampling capacitance is equal to 40 pF. Therefore, the value of C_{FLT} should be greater than 800 pF. Note that driving capacitive loads can degrade the phase margin of the input amplifiers, which makes the amplifier marginally unstable. To avoid amplifier stability issues, series isolation resistors (R_{FLT}) are used at the output of the amplifiers. A higher value of R_{FLT} is helpful from the amplifier stability perspective but adds distortion as a result of interactions with the nonlinear input impedance of the ADC. Distortion increases with source impedance, input signal frequency, and input signal amplitude. Therefore, the selection of R_{FLT} requires balancing the stability and distortion of the design. For these devices, TI recommends limiting the value of R_{FLT} to a maximum of 22 Ω to avoid any significant degradation in linearity performance. The tolerance of the selected resistors can be chosen as 1%.

TIDA-00208 uses C_{FLT} = 0.01 µF and R_{FLT} = 10 Ω, with the cut-off frequency of 79.58 kHz.

The flicker and broadband noise introduced by the op-amp (or FDA) can be verified using Equation 3:

$$OPA_{Broadband\_RMS\_Noise} = OPA_{Broadband\_RMS\_Density} \times \sqrt{\frac{\pi}{2} \times \left(\frac{1}{2\pi R_{FLT} C_{FLT}} - 10\,Hz \right)} \quad (3)$$

8.3 Designing the Amplifier Stage

Figure 10 shows the OPA4322 section. As mentioned earlier, TIDA-00208 has four sensors on board, which means the design requires four amplifiers. The OPA4322 is a quad op-amp, and each channel in OPA4322 is used for one fluxgate sensor.

Important observations from Figure 10 are:

- Single-supply operation: The OPA4322 is powered through 5 V coming out of TPS7A4700 (as explained in Section 8.6). One bypass capacitor with a value of 0.1 µF is placed very close to the AVDD pin of OPA4322.
- Output common-mode setting: The non-inverting pin of the op-amp is supplied with 2.5 V (coming from VREF_BUF or the sensor REF output) in case the pin interfaces with an external ADC. But when the internal ADC of the Piccolo controller is used, the common-mode voltage needs to be 1.65 V. In that case, the external voltage on non-inverting pin of op-amp is supplied through 1.65 V (coming from REF2033 REF/2).
- Input signal filtering: The fluxgate sensors have an inherent noise due to their internal structure. Both inputs of OPA4322 use a low-pass filter. The design of filters is explained in Section 8.4.
- Selection of gain:
  - When used with the external ADC, the output can have a common-mode voltage of 2.5 V and the full-scale range of the ADC can be 5 V. The fluxgate sensors can work up to 300% of their nominal current range, which means the signal must have a gain to go from 1.875 to 2.5 V at 300% of the operating current. This signal gives a gain of 1.33.
  - When used with internal ADC of controller, the output can have a common-mode voltage of 1.65 V and the full-scale range of the ADC can be 3.3 V. The fluxgate sensors can work up to 300% of their nominal current range, which means the signal must have a gain to go from 1.875 to 1.65 V at 300% of the operating current. This signal gives a gain of 0.88. If the current measurement requirement is only up to 200% or 250%, a gain of 1 can be used.
- Selection of components: The 0.1-µF caps in the feedback helps to reduce overall noise of the system. One important thing to note that the resistors also have their internal noise. The resistor noise depends on the value of resistor. Select the input and feedback resistor values in some kΩ (preferably < 5 kΩ) to reduce the effect of noise from resistors.

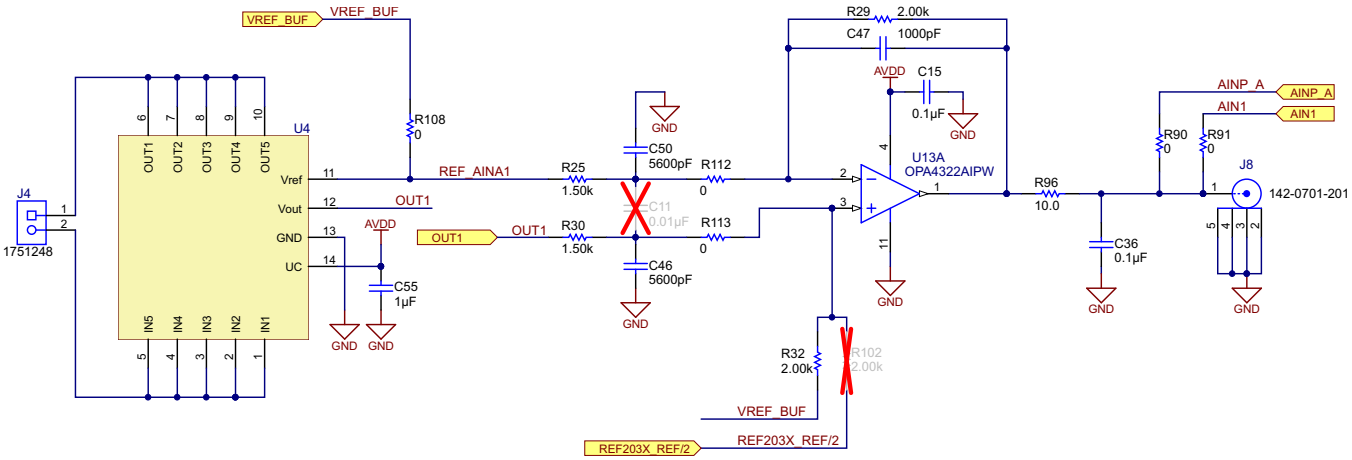


Figure 10. OPA4322 Interface Between Sensor and ADC

8.4 Noise Filtering for Fluxgate Current Sensor

Fluxgates have an inherent noise (450 kHz / 900 kHz) at their output that needs filtering. A low-pass filter is designed with a cut-off frequency of 20 kHz using TI's FilterPro™ software as shown in Figure 11.

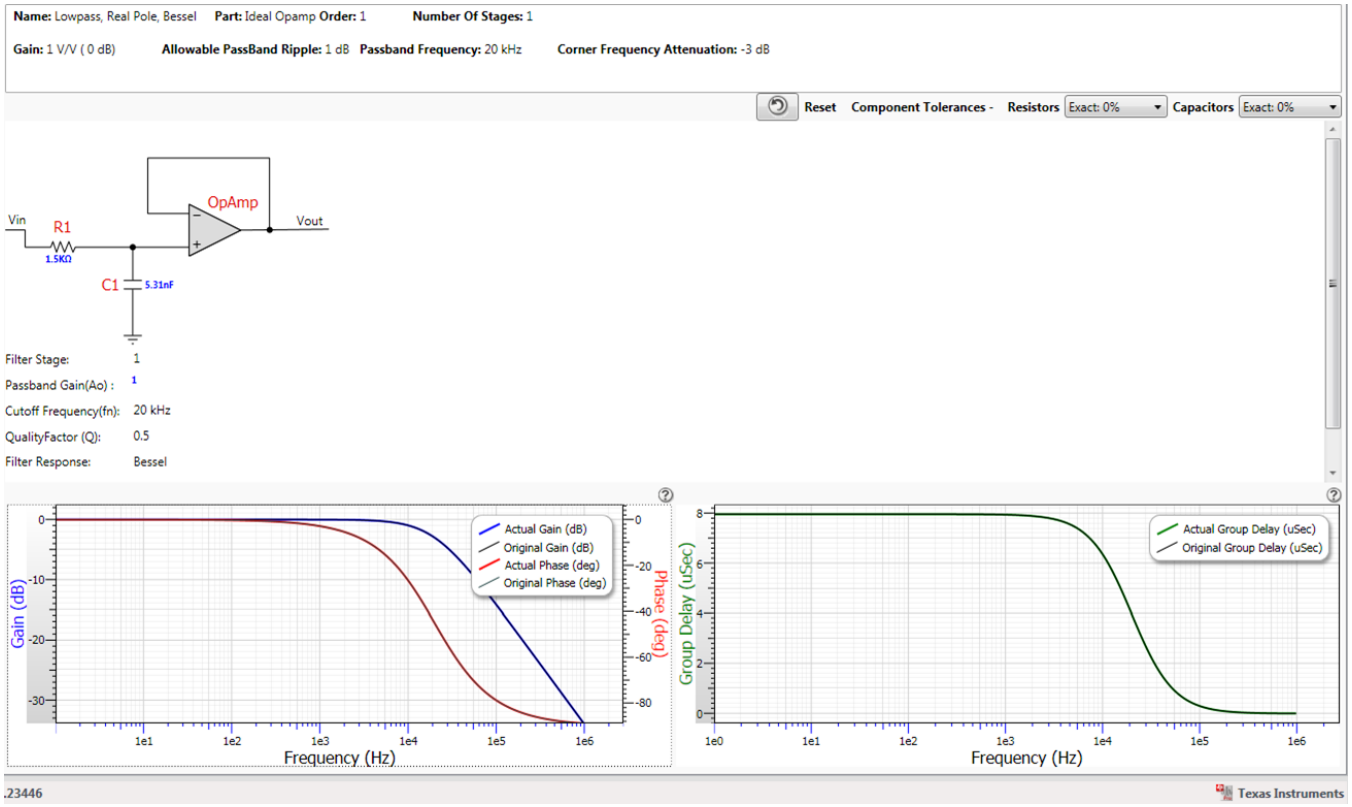


Figure 11. Low-Pass Filter Design Simulation Using FilterPro

8.5 Designing the Reference Circuit for ADC

An ADC is as good as its reference because ADCs compare an input to a known reference and its binary scaled weights to estimate an equivalent digital code. An accurate digital conversion of the input signal requires a highly accurate, low-drift, low-noise reference. The reference should also support the dynamic charge requirements without affecting the noise and linearity performance of the device. An ideal ADC is one that gives the same digital code for a given input. For a capacitor-based ADC reference input, the load at the reference pin spikes out every time a bit value is estimated. Not only does reference current transient multiple times within a conversion cycle, but also the magnitude of the transient current vary between the conversions. A noisy reference shows up as a variation of code out at the output of the ADC for a fixed input. A noisy reference also degrades the linearity, THD, and SNR.

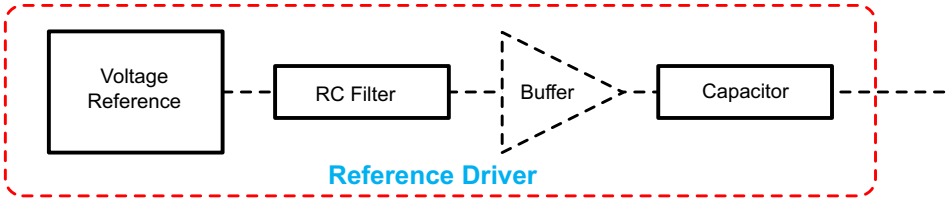


Figure 12. Reference Driver Circuit

As shown in Figure 12, designing the reference drive circuitry is a four-step optimization process that involves

1. identifying a reference that is suitable for the application
2. designing a filter that limits the broadband noise from the reference
3. estimating the capacitor value needed to provide the reference drive current
4. identifying an op-amp that is suitable for low power that can recharge the capacitor

A reference can introduce two types of noise: flicker noise and broadband noise. Flicker noise is the noise dominant at low frequencies and broadband noise dominates at high frequencies. The broadband noise, in particular, can be of the order of hundreds of microvolts and can easily exceed the tens of microvolts of RMS noise of the converter. Typically, flicker noise is specified on the datasheet as peak-to-peak noise up to 10 Hz. This noise has to be scaled down by a factor of 6.6 to convert it into RMS noise. On the other hand, the density of broadband spectral noise may not be specified on the datasheet. For a band-gap reference, the density is 0.1 $\mu V_{RMS}/\sqrt{Hz}$ to 10 $\mu V_{RMS}/\sqrt{Hz}$ in magnitude and is inversely proportional to the square root of the quiescent current of the reference. If the reference is not specified, Equation 4 gives a good approximation:

$$REF_{Broadband\_Noise\_Density} = \frac{10{,}000\ nV}{\sqrt{Hz}} \times \frac{\sqrt{\mu A}}{\sqrt{2 \times IQ\_REF\left(in\ \mu A\right)}} \quad (4)$$

As seen from Figure 13, noise and power are inversely related. A reference with low IQ inherently comes with higher noise.

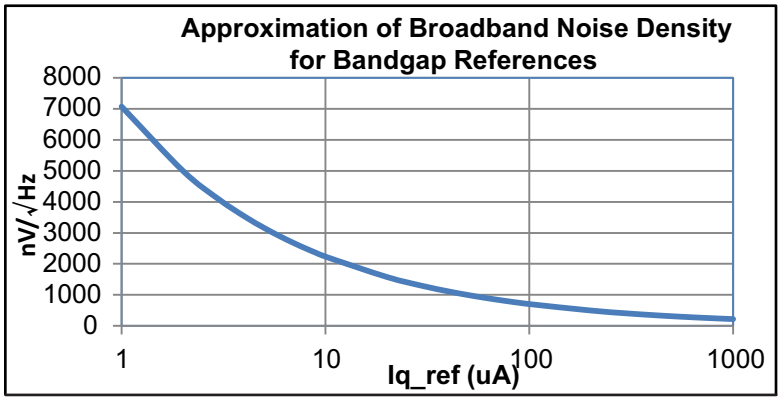


Figure 13. Broadband Noise versus Reference Quiescent Current

For REF5025, I_{Q_REF} = 800 µA, which gives the broadband noise a density equal to 250 nV/√Hz using Figure 13.

Buffer

An op-amp is needed to recharge the capacitor above. Additional noise introduced by the buffer should be minimized while selecting this op-amp. However, this selection is less of a concern because unlike references where output noise density is a few μV/√Hz, the same will be in the range of 10 nV/√Hz to 100 nV/√Hz for op-amps. The broadband noise gets further band-limited by the isolation resistor and the capacitor following the buffer. Flicker and broadband noise introduced by the op-amp should be verified for it to be significantly smaller (less than one-third) than the reference noise before finalizing on the op-amp. Reducing the buffer noise to less than a third of the reference noise makes the op-amp noise term insignificant when it gets added to the reference noise (square root of summation of squares). Flicker noise is specified on the datasheet as peak-to-peak noise up to 10 Hz. This noise has to be scaled down by a factor of 6.6 to convert it into RMS noise. The total noise introduced by the op-amp is the square root of the sum of the squares of the flicker noise and broadband RMS noise. Equation 3 can be used to verify the same.

Note that high resolution converters cause the size of the capacitor in the charge bucket to become too large, causing stability issues in most of the op-amps. This issue can be addressed with a series isolation resistor at the cost of the bandwidth of the op-amp. Choosing the right capacitor, op-amp, and isolation resistor is an iterative process that has to be verified by simulation. During this process the capacitance might require minimal adjustments from the starting value taking stability, voltage drop, and cutoff frequency into consideration.

Reference for External ADC: REF5025 + OPA322

The REF5025 is used as a 2.5-V voltage reference device. Use a supply bypass capacitor ranging between 1 to 10 μF. The REF5025 allows access to the band-gap through the TRIM/NR pin. Placing a capacitor from the TRIM/NR pin to GND in combination with the internal resistors creates a low-pass filter. A capacitance of 1 μF creates a low-pass filter with the corner frequency between 10 and 20 Hz. This filter decreases the overall noise measured on the V_{OUT} pin by half. A higher capacitance results in a lower filter cutoff frequency, further reducing output noise. Note that use of this capacitor increases startup time. Figure 14 shows schematic capture of REF5025 and the OPA322-based buffer connected at the output of the REF5025 so as to recharge the capacitor at the output.

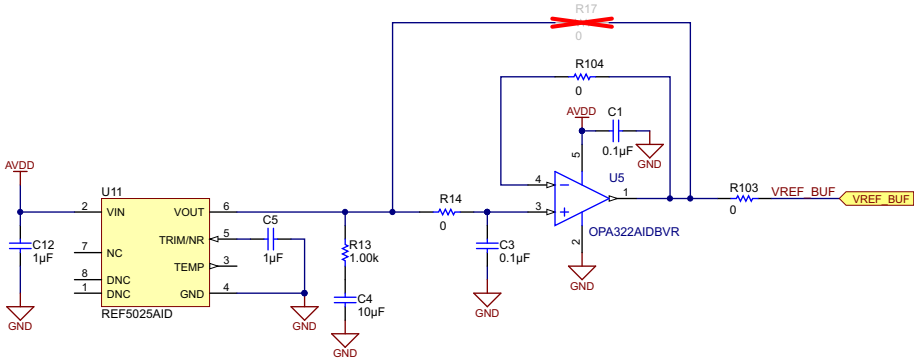


Figure 14. REF5025 + OPA322 Circuit

Reference for Internal ADC of Piccolo TMS320F28027: REF2033

The REF2033 can provide two reference voltages, 1.65 V and 3.3 V. The 3.3 V is given as reference to the integrated ADC, and 1.65 V is used as signal common-mode inputs coming from op-amps. Figure 15 shows the reference circuit using the REF2033.

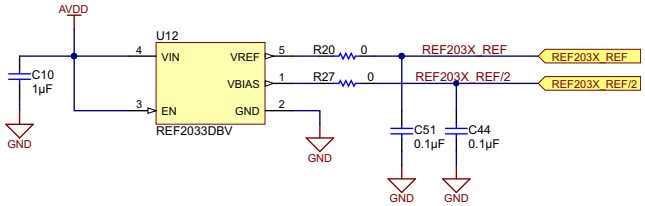


Figure 15. REF2033 Circuit to Provide 1.65 V and 3.3 V as Reference

8.6 Power Supply: 5-V and 3.3-V Generation

The TIDA-00208 board can be powered through connector J12. The input voltage can be 6 V, 15 V, or 24 V based on the availability in the industrial drive. The output voltage for the TPS7A4700 is set by grounding the appropriate control pins. When grounded, all control pins add a specific voltage on top of the internal reference voltage (V_{REF} = 1.4 V). For example, when grounding pins 0P4V and 3P2V, the voltage values 0.4 V and 3.2 V are added to the 1.4-V internal reference voltage for $V_{OUT(NOM)}$ equal to 5.0 V. Figure 16 shows the TPS7A4700 section of the design. One green LED (LD1) is provided to indicate availability of the 5-V output.

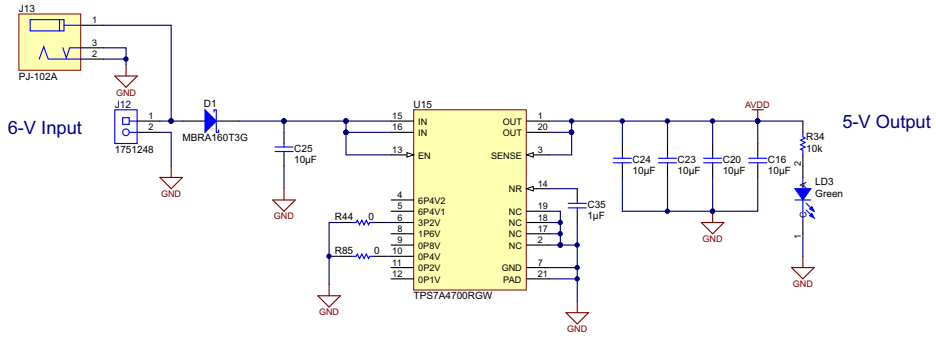


Figure 16. 6- to 5-V Conversion Using TPS7A4700

The TLV70033 converts the 5 V to 3.3 V. Figure 17 shows the schematic for the same.

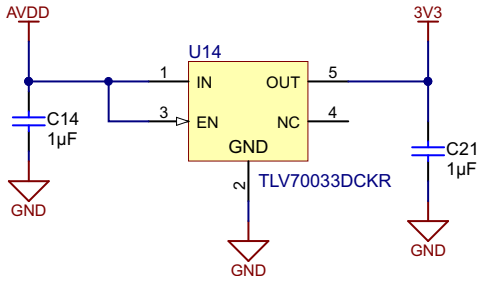


Figure 17. 5- to 3.3-V Conversion Using TLV70033

8.7 Design for Overcurrent and Earth Fault Detection Circuits

Generally, the fluxgate sensors can be operated up to 300% of their nominal current ratings for a shorter duration. If the current goes beyond 300%, enable the protection mechanism. For example, in this design, the thresholds are calculated as follows:

- Nominal current rating (In) = 6 Amperes
  Corresponding fluxgate sensor output voltage = 0.625 Volts
- 300% of the nominal rating = 18 Amperes
  Corresponding fluxgate sensor output voltage at 300% current = 0.625 × 3 = 1.875 Volts

The output of fluxgate sensor always rides on 2.5 V, so the positive and negative values can go up to 4.375 V and 0.625 V, respectively. Considering 50 mV as a buffer, the thresholds are calculated as:

- Threshold for positive cycle = VTH (pos) = 2.5 V + 1.875 V + 0.05 V = 4.38 Volts
- Threshold for negative cycle = VTH (neg) = 2.5 V – 1.875 V – 0.05 V = 0.62 Volts

8.7.1 Overcurrent Protection

The overcurrent protection is implemented as shown in Figure 18. The resistor dividers are calculated for VTH (pos) = 4.38 V and VTH (neg) = 0.62 V. Each channel has individual overcurrent protection. The indication of the overcurrent's condition is shown with an LED at the output.

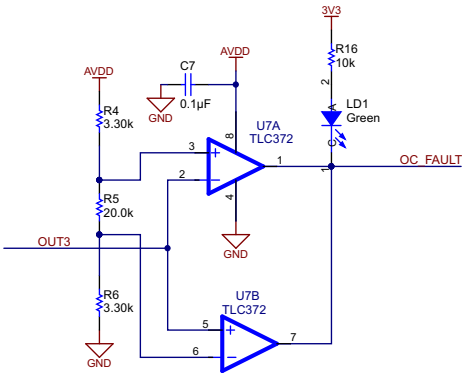


Figure 18. Overcurrent Protection Using TLC372

8.7.2 Earth Fault Protection

The earth fault protection is implemented as shown in Figure 19. The resistor dividers are calculated for VTH (pos) = 4.38 V and VTH (neg) = 0.62 V. The signals coming out from each channel are summed together with resistors. The indication of the overcurrent's condition is shown with an LED at the output. Both OC_FAULT and GND_FAULT are available on connector J9.

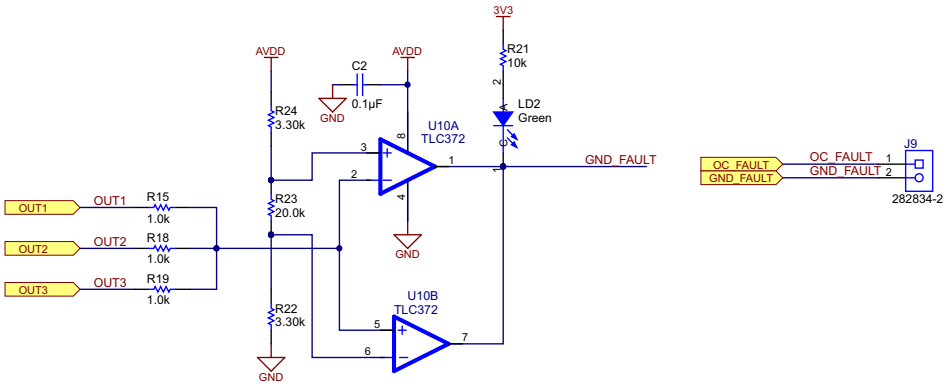


Figure 19. Earth Fault Protection Using TLC372

8.8 Connections to Onboard External ADCs: ADS7853

The ADS7853 belongs to a family of pin-compatible, dual, high-speed, simultaneous-sampling, ADCs that support single-ended and pseudo-differential analog inputs. Each device includes two individually programmable reference sources that can be used for system-level gain calibration. Also, a flexible serial interface that can operate over a wide power-supply range enables easy communication with a large variety of host controllers. The interface is fully specified over the extended industrial temperature range (–40°C to 125°C). Figure 20 shows the schematic for the two ADS7853 devices available on board. The SPI outputs are available on a connector to interface with external motor controller (as shown in Figure 21).

Reference: Both ADCs can use either their internal references or an external reference coming from the REF5025 (VREF_BUF).

Power supply: Both ADCs are powered at AVDD with a 5-V supply voltage coming from the TPS7A4700 with a decoupling cap of 10 µF placed very close to the device. The DVDD supply is given from 3.3 V coming from the TLV70033. DVDD also has a decoupling capacitor of 10 µF placed very close to the device.

Simultaneous sampling of all four ADCs: All four ADCs can sample the input signals simultaneously by connecting the /CS pins together and giving one single /CS signal to the ADCs.

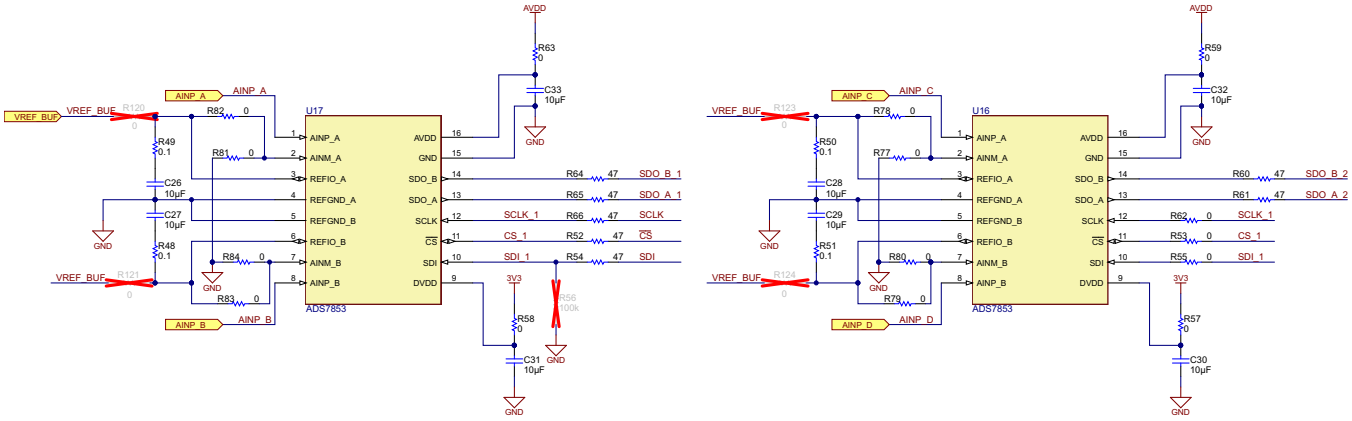


Figure 20. ADS7853 Circuit

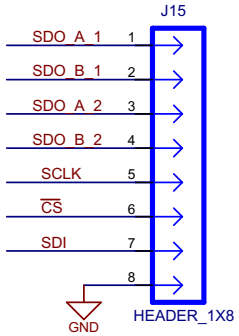


Figure 21. SPI Signals of External ADCs Taken Out on a Connector

8.9 Connections to Piccolo 28027 LaunchPad™

The C2000™ Piccolo LaunchPad LAUNCHXL-F28027 is a complete low-cost experimenter board for the TI Piccolo F2802x devices. The LAUNCHXL-F28027 kit features all the hardware and software necessary to develop applications based on the F2802x microprocessor. The LaunchPad is based on the superset F28027 device and easily allows users to migrate to lower cost F2802x devices once the design needs are known. The device offers an on-board JTAG emulation tool allowing direct interface to a PC for easy programming, debugging, and evaluation. In addition to JTAG emulation, the USB interface provides a UART serial connection from the F2802x device to the host PC.

The LAUNCHXL-F28027 C2000 LaunchPad features include:

- USB debugging and programming interface through a high-speed galvanically isolated XDS100v2 emulator featuring a USB/UART connection
- Superset F28027 device that allows applications to easily migrate to lower cost devices
- Nibble (4-bit) wide LED display
- Two push buttons for user feedback and device reset
- Easily accessible device pins for debugging purposes or as sockets for adding customized extension boards
- Boot selection and USB and UART disconnect switches.

An image of the LaunchPad is shown in Figure 22:

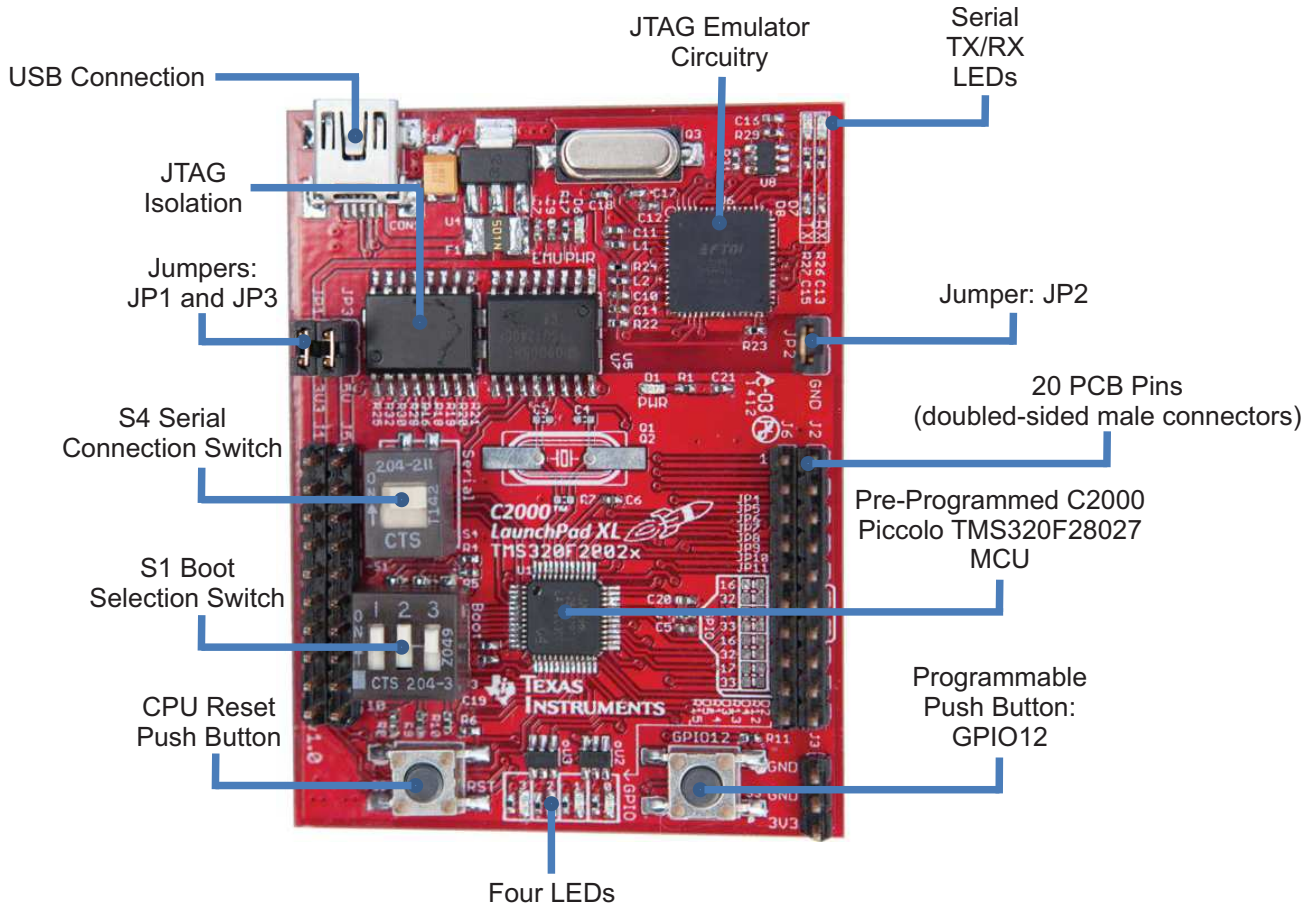


Figure 22. Image of LAUNCHXL-F28027

Table 6 shows the pin-mapping for 40-pin connector available on LAUNCHXL-F28027. The signals are routed as shown in Table 7.

Table 6. C2000 LaunchPad Pin Out and Pin Mux Options

MUX VALUE						MUX VALUE			
3	**2**	**1**	**0**	**J1 Pin**	**J5 Pin**	**0**	**1**	**2**	**3**
			+3.3V	1	1	+5V			
			ADCINA6	2	2	GND			
TZ2	SDAA	SCIRXDA	GPIO28	3	3	ADCINA7			
TZ3	SCLA	SCITXDA	GPIO29	4	4	ADCINA3			
Rsvd	Rsvd	COMP2OUT	GPIO34	5	5	ADCINA1			
			ADCINA4	6	6	ADCINA0			
	SCITXDA	SPICLK	GPIO18	7	7	ADCINB1			
			ADCINA2	8	8	ADCINB3			
			ADCINB2	9	9	ADCINB7			
			ADCINB4	10	10	NC			
3	**2**	**1**	**0**	**J6 Pin**	**J2 Pin**	**0**	**1**	**2**	**3**
Rsvd	Rsvd	EPWM1A	GPIO0	1	1	GND			
COMP1OUT	Rsvd	EPWM1B	GPIO1	2	2	GPIO19	SPISTEA	SCIRXDA	ECAP1
Rsvd	Rsvd	EPWM2A	GPIO2	3	3	GPIO12	TZ1	SCITXDA	Rsvd
COMP2OUT	Rsvd	EPWM2B	GPIO3	4	4	NC			
Rsvd	Rsvd	EPWM3A	GPIO4	5	5	RESET#			
ECAP1	Rsvd	EPWM3B	GPIO5	6	6	GPIO16/32	SPISIMOA/ SDAA	Rsvd/ EPWMSYNCI	TZ2/ ADCSOCA
TZ2/ ADCSOCA	Rsvd/ EPWMSYNCI	SPISIMOA/ SDAA	GPIO16/32	7	7	GPIO17/33	SPISOMIA/ SCLA	Rsvd/ EPWMSYNCO	TZ3/ ADCSOCB
TZ3/ ADCSOCB	Rsvd/ EPWMSYNCO	SPISOMIA/ SCLA	GPIO17/33	8	8	GPIO6	EPWM4A	EPWMSYNCI	EPWMSYNCO
			NC	9	9	GPIO7	EPWM4B	SCIRXDA	Rsvd
			NC	10	10	ADCINB6			

Table 7. Pin-Mapping Details

PIN NUMBER ON LAUNCHPAD	PIN FUNCTIONALITY ON LAUNCHPAD	MAPPING ON TIDA-00208 BOARD (J11 AND J14)
J1- Pin 1	+3.3V	J14 – Pin 20 (+3.3V)
J1- Pin 5	GPIO34	J14 – Pin 12 (/CS)
J1 – Pin 6	ADCINA4	J14 – Pin 10 (AIN2)
J1 – Pin 7	SPICLK	J14 – Pin 8 (SCLK)
J1 – Pin 8	ADCINA2	J14 – Pin 6 (AIN3)
J1 – Pin 9	ADCINB2	J14 – Pin 4 (AIN2)
J1 – Pin 10	ADCINB4	J14 – Pin 2 (AIN1)
J5 – Pin 2	GND	J14 – Pin 17 (GND)
J5 – Pin 3	ADCINA7	J14 – Pin 15 (AIN4)
J5 – Pin 4	ADCINA3	J14 – Pin 13 (AIN1)
J5 – Pin 6	ADCINA0	J14 – Pin 9 (REF203X_REF/2)
J5 – Pin 7	ADCINB1	J14 – Pin 7 (REF203X_REF)
J5 – Pin 8	ADCINB3	J14 – Pin 5 (AIN3)
J5 – Pin 9	ADCINB7	J14 – Pin 3 (AIN1)
J6 – Pin 7	SPISIMOA/SDAA	J11 – Pin 8 (SDI)
J6 – Pin 8	SPISOMIA/SCLA	J11 – Pin 6 (SDO_A_1/SDO_B_1)
J2 – Pin 1	GND	J11 – Pin 19 (GND)
J2 – Pin 7	SPISOMIA/SCLA	J11 – Pin 7 (SDO_A_2/SDO_B_2)

Figure 23 shows the schematic capture for the pin-mapping explained in Table 7. This design also provides an option to mount external clamping diodes for the analog inputs.

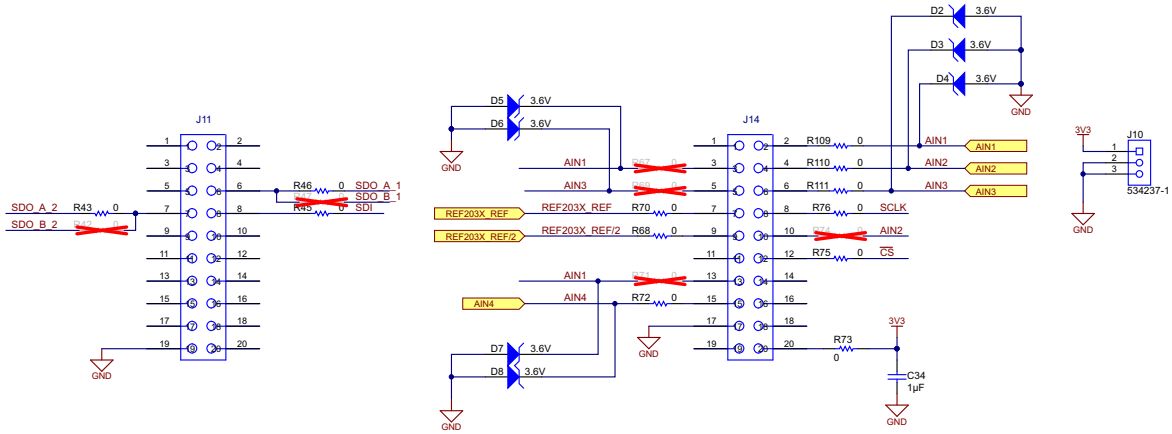


Figure 23. Schematic Capture for J11 and J14 (To Be Connected to 40-Pin Connector on LaunchPad)

9 Test Setup and Test Results

9.1 Noise Filtering for Fluxgate Current Sensor

As explained in Section 8.4, low-pass filters are used to filter out the 450-kHz / 900-kHz noise signal from fluxgate sensors. Figure 24 shows the waveforms before and after the filter. The noise signal on OUT pin of the fluxgate sensor is having frequency of 452.1 kHz, which is same as the internal fluxgate oscillator frequency.

NOTE: The signals captured in Figure 24 also include noise from the oscilloscope itself.

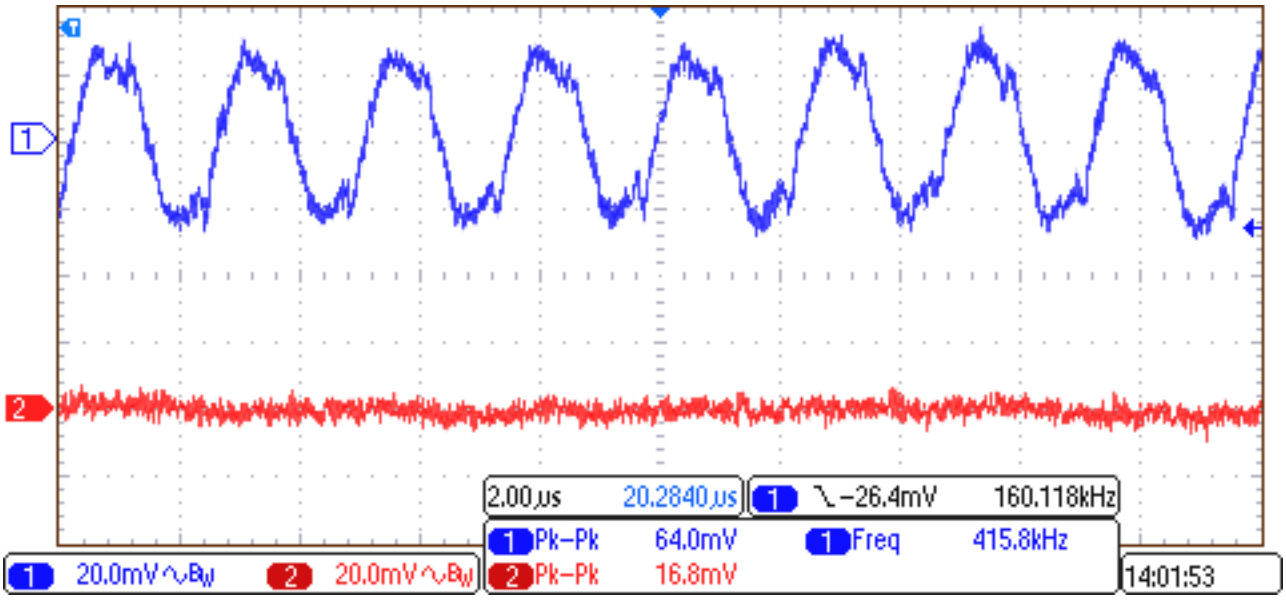


Figure 24. Noise Signal Before and After the Low-Pass Filter

9.2 DC (or Dynamic) Performance of the System Using External ADC ADS7253

All ADC circuits suffer from some amount of inherent broadband noise contributed by the internal resistors, capacitors, and other circuitry, which is referred to the inputs of the ADC. The front-end driver circuit also contributes some noise to the system, which can also be referred to the ADC inputs. The cumulative noise, often called as the input-referred noise of the ADC, has a significant impact on the overall system performance. The most common way to characterize this noise is by using a constant DC voltage as the input signal and collecting a large number of ADC output codes. A histogram can then be plotted to show the distribution of output codes, which can be used to illustrate the impact of noise on the overall system performance. For a theoretically perfect ADC system, the histogram of output codes is a single vertical bar because the ADC output is always the same for a DC input voltage. However, the noise contributions from the ADC and the front-end circuit lead to a distribution of output codes, which provides a measure of the overall system's DC noise. If the output code distribution has large peaks and valleys that make it distinctly non-Gaussian, then the histogram indicates significant DNL errors in the ADC or issues with the system design such as insufficient power supply decoupling, improper ground connections, or other poor PCB layout effects.

The noise-free resolution of an ADC is defined as the number of steady output bits from the converter beyond. The system performance is dominated by noise, and it is not possible to differentiate between individual code transitions. This resolution is an extremely conservative measurement of the ADC's performance because the formula for noise-free resolution is derived from the peak-to-peak code noise, which is extremely dependent on the total number of samples. Do not confuse the effective noise-free resolution and effective number of bits (ENOB) with each other as they are two completely different entities. The ENOB for an ADC is measured with an AC sinusoidal input signal and includes the effects due to quantization noise and distortion terms, which have no impact on a DC measurement.

Figure 25 and Figure 26 show the histogram, noise-free resolution, and the captured data for this design. With a 6-A DC current passing through the fluxgate sensor, the noise-free resolution is 11.90 bits for Channel A and 11.44 bits for Channel B.

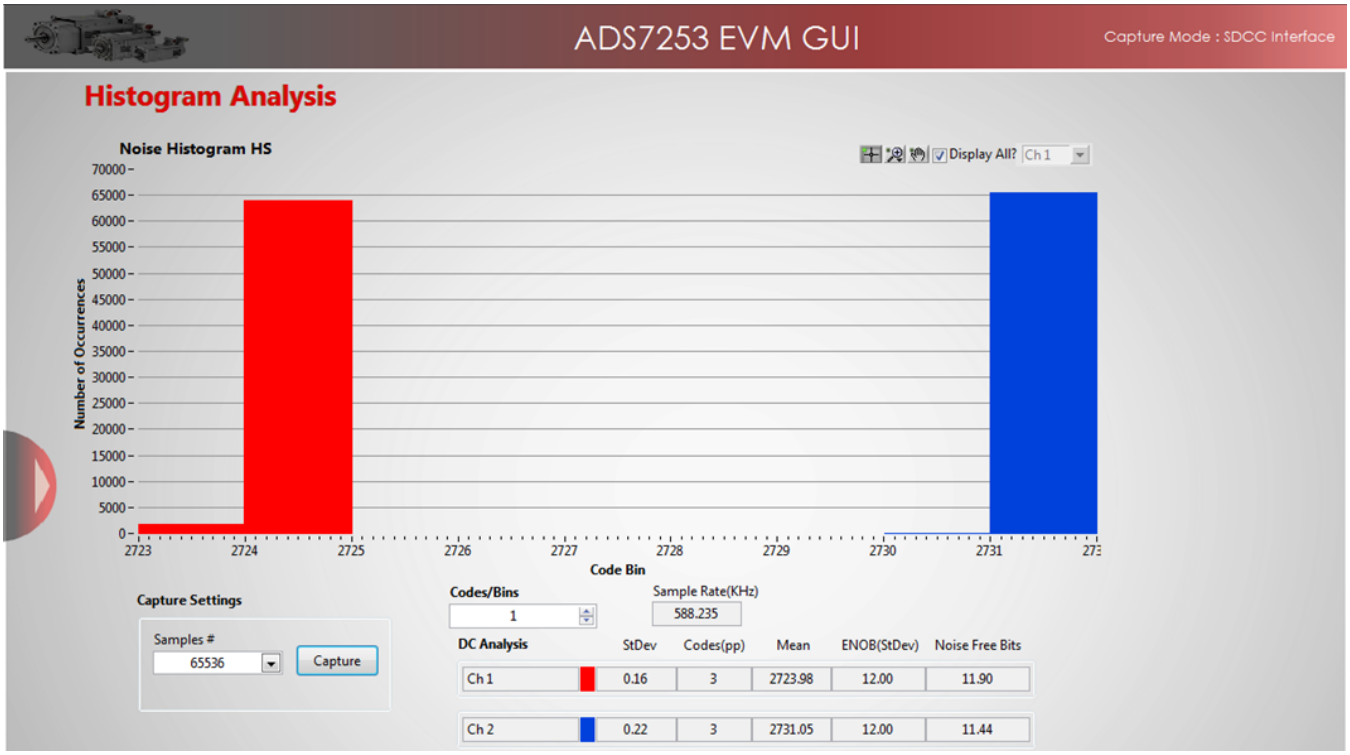


Figure 25. Histogram of Captures for Two Channels Using ADS7253 EVM GUI

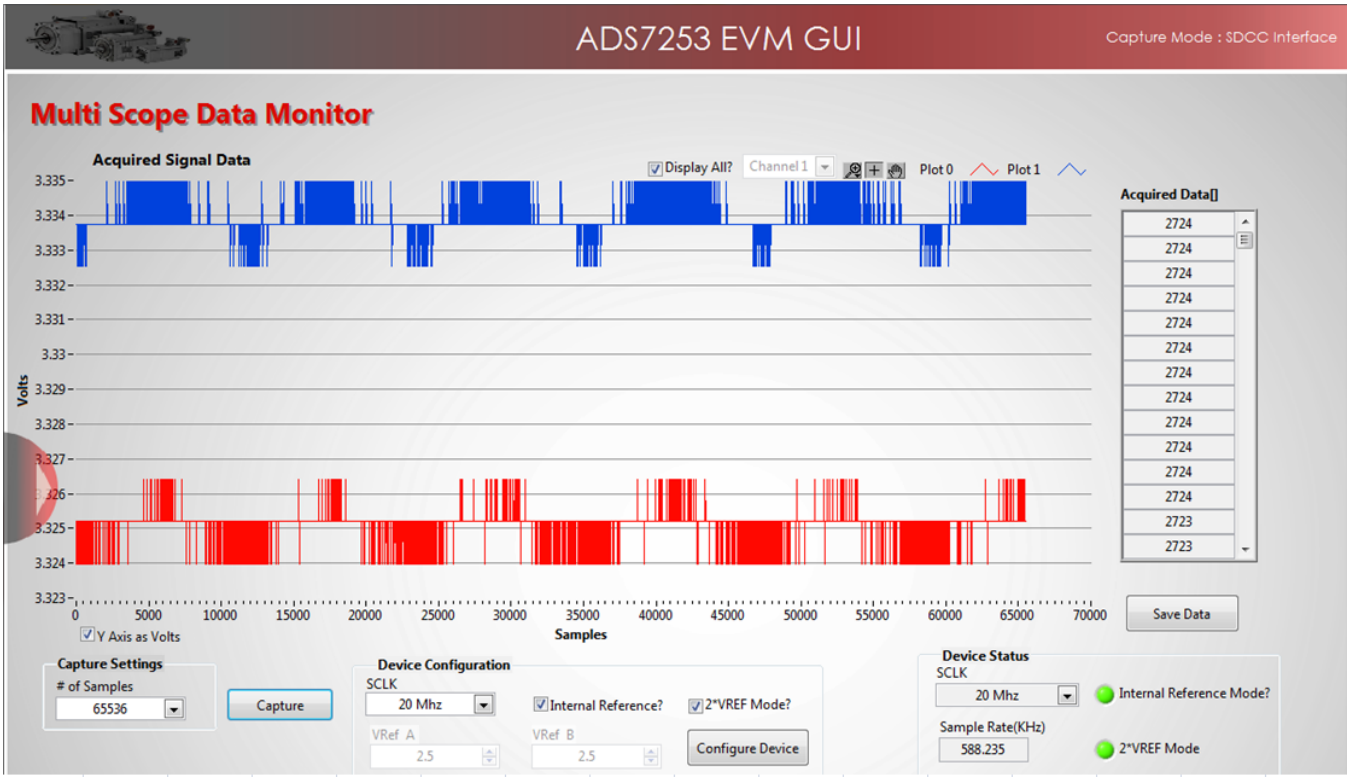


Figure 26. Data Capture for Two Channels Using ADS7253 EVM GUI

9.3 AC (or Static) Performance of the System Using External ADC ADS7253

For any data acquisition system, an important focus is to achieve excellent dynamic performance while minimizing the total power consumption of the system. The main AC specifications to consider are THD, SNR, SINAD, and ENOB. Essentially, these parameters are different ways of quantifying the noise and distortion performance of an ADC based on a fast Fourier transform (FFT) analysis. A typical FFT plot for an ADC is shown in Figure 27.

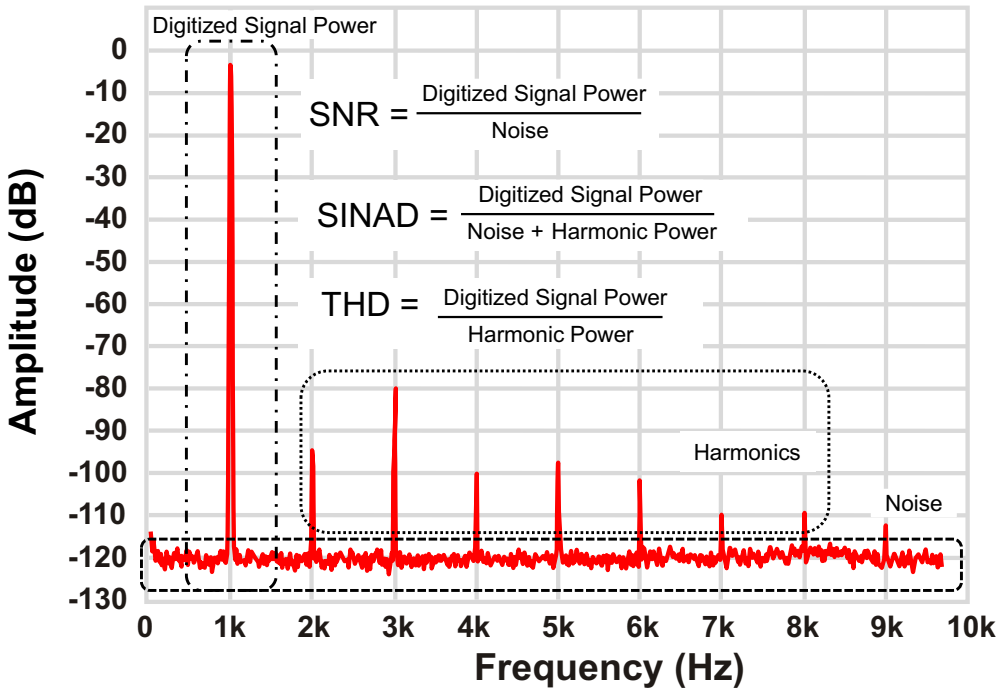


Figure 27. Typical FFT Plot Showing Different Dynamic Parameters

The SNR provides insight into the total noise of the system. The total noise of the data acquisition system is the RSS of the front-end amplifier noise ($V_{n\_AMP\_RMS}$) and the ADC noise ($V_{n\_ADC\_RMS}$). The ADC noise includes the quantization noise as well as the noise contributed by the ADC internal circuitry, or the input-referred noise of the ADC. The total noise contributions from all these sources, denoted as $V_{n\_TOT\_RMS}$, are referred to the input of the ADC to calculate the total SNR of the system (SNR_{SYS}).

$$V_{n\_TOT\_RMS} = \sqrt{V_{n\_AMP\_RMS}^2 + V_{n\_ADC\_RMS}^2}$$

$$SNR_{SYS} = \frac{V_{SIG\_RMS}}{V_{n\_TOT\_RMS}} \quad (5)$$

ENOB is an effective measurement of the quality of a digitized signal from an ADC by specifying the number of bits above the noise floor. For an ideal N-bit ADC with only quantization noise, the SNR (in dB) can be calculated as:

$$SNR = 6.02 \times N + 1.76$$

$$N = \frac{SNR - 1.76}{6.02} \quad (6)$$

While ENOB provides a good summary of the ADC dynamic performance, it does not describe the converter's entire performance over the operating frequency ranges and input signals. Additionally, ENOB does not include the ADC DC specifications such as offset and gain error. Therefore, pay attention to other converter specifications as well depending on the application using the ADC.

For an AC current of 4.5 V_{RMS} at a frequency of 50 Hz, the conditioned voltage signal (at the output of ADS7253) is captured, and the FFT of the system is also taken using the ADS7253EVM and SDCC board. As shown in Figure 28 and Figure 29, the GUI captures show the captured AC signal, the FFT, and other parameters.

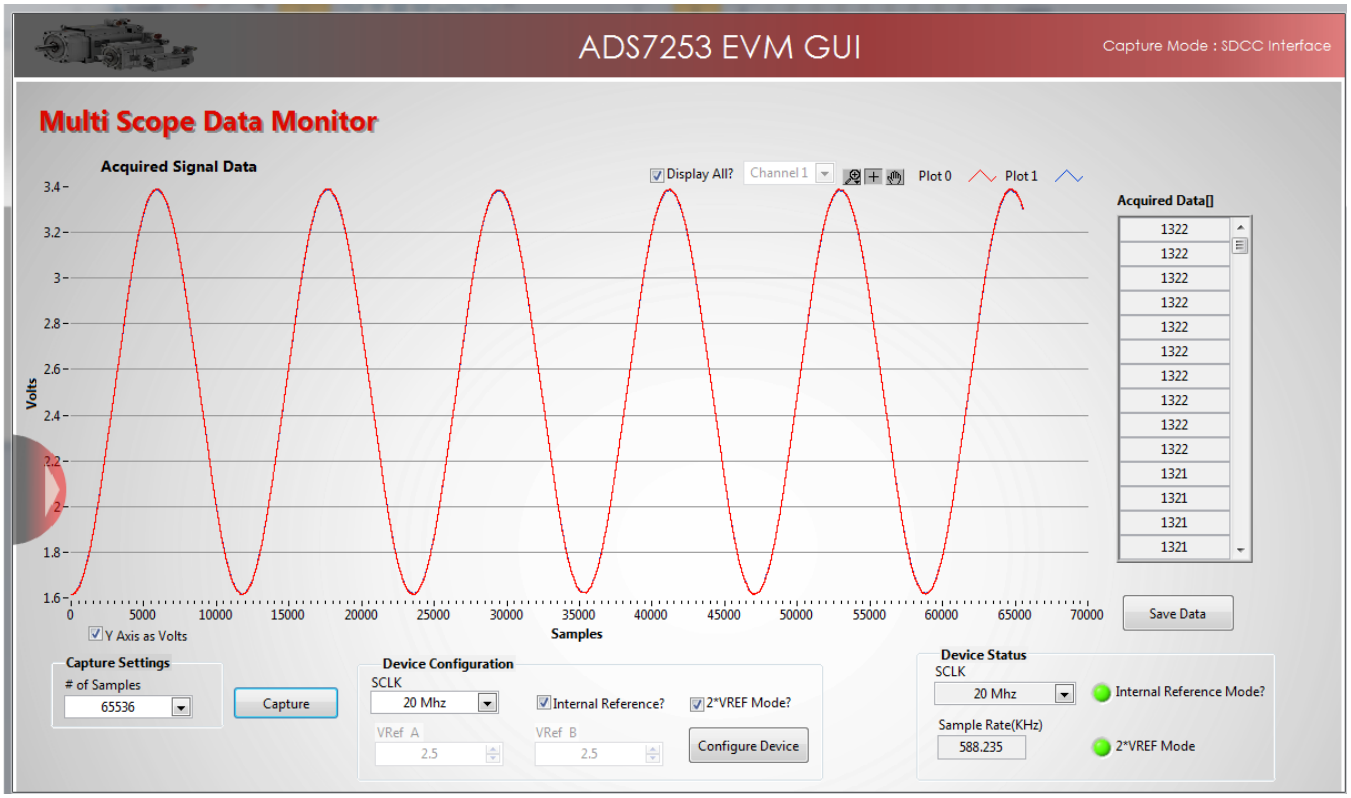


Figure 28. AC Signal Capture for Two Channels Using ADS7253 EVM GUI

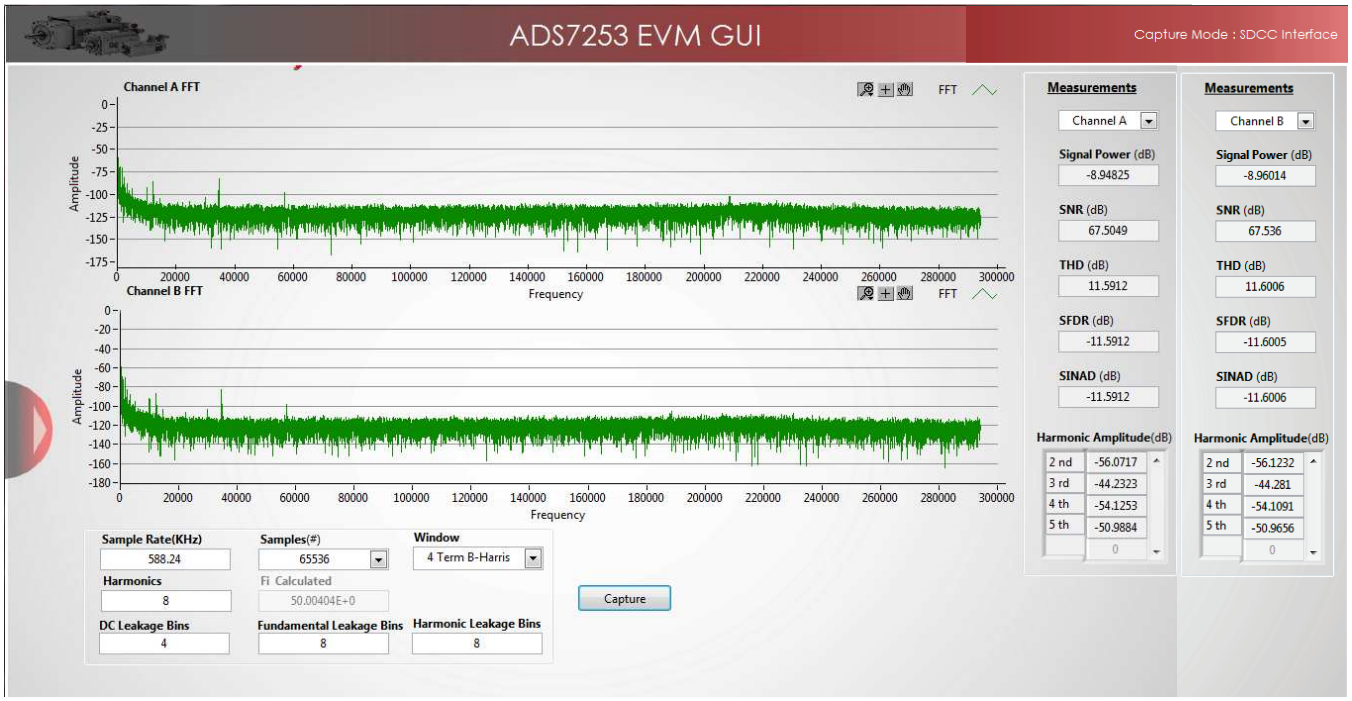


Figure 29. FFT and SNR Shown for Two Channels Using ADS7253 EVM GUI

The FFT for both channels show an SNR of approximately 67.5 dB at a signal amplitude of –8.9 dBFS. This result is just an indication of performance, but the actual SNR can be measured when the device is operated with an input voltage that has reached the full-scale value of the ADC input range. Figure 30 is the setup used to measure the AC and DC performance for this reference design.

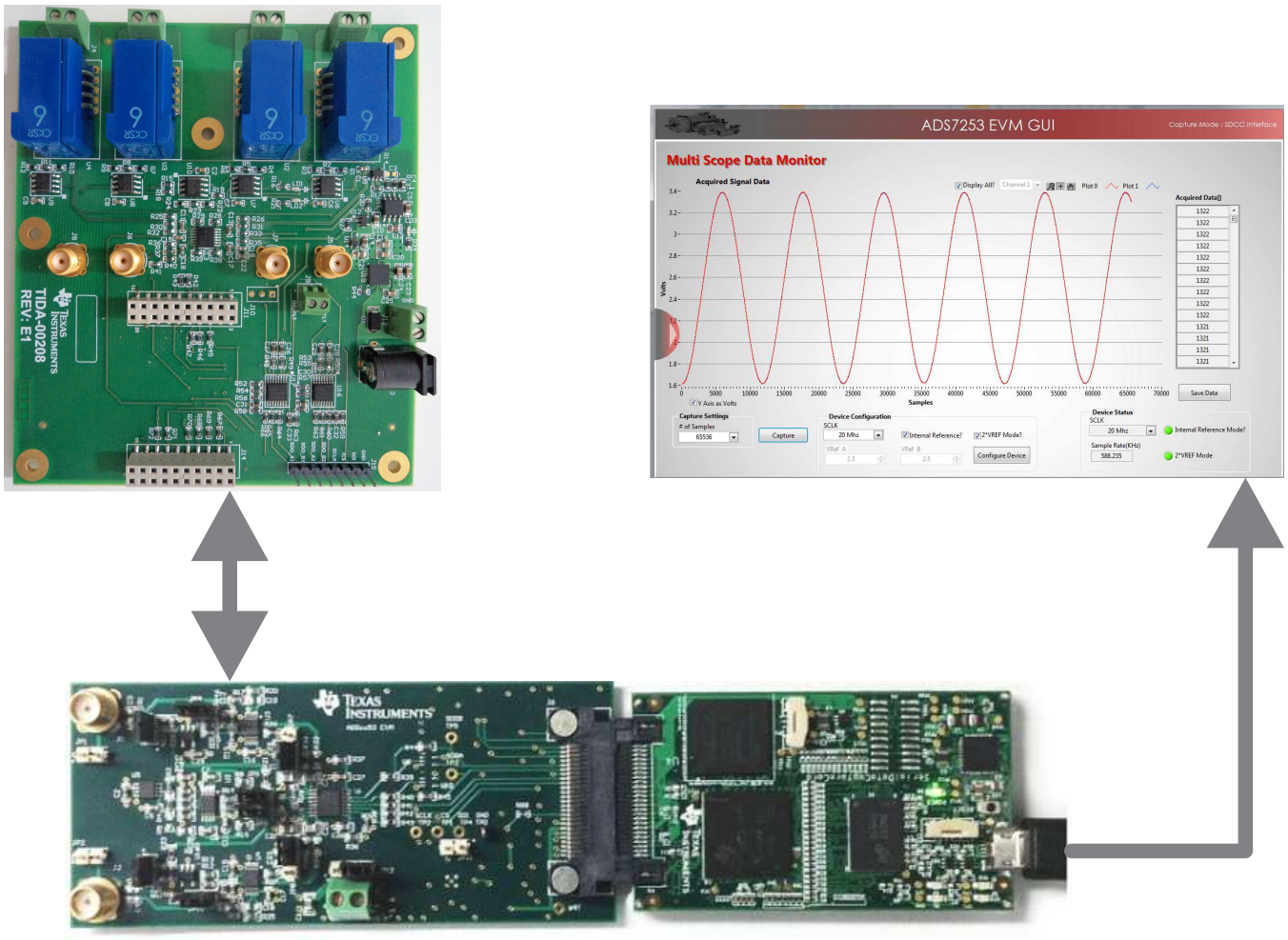


Figure 30. Test Setup for AC and DC Tests for ADS7253

9.4 DC Accuracy Tests (at 25°C and 75°C)

The following figures show the accuracy of the signal at each stage. Figure 31 shows accuracy of signal at the output of THS4531 at 25°C and Figure 32 shows accuracy of signal at 75°C. It includes the offset and gain error compensation along with passive component mismatches in the feedback path of THS4531.

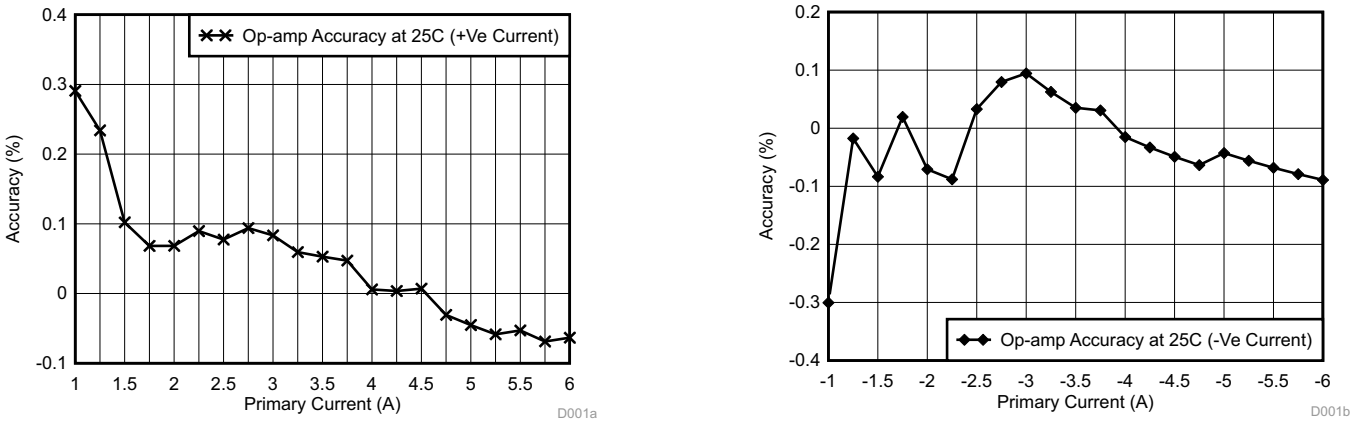


Figure 31. Op-Amp Accuracy at 25°C (Left) for Positive Current (Right) for Negative Current

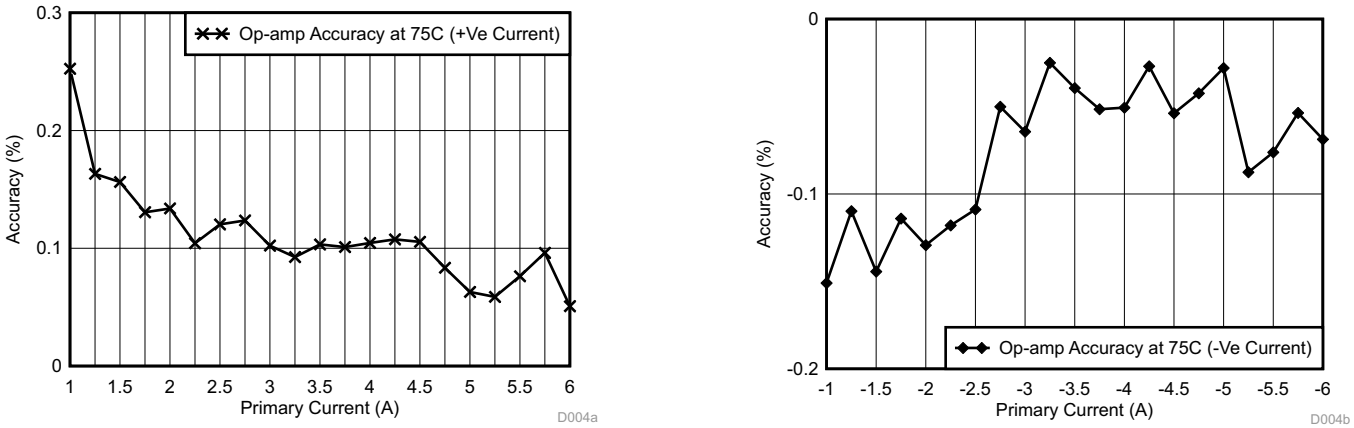


Figure 32. Op-Amp Accuracy at 75°C (Left) for Positive Current (Right) for Negative Current

Figure 33 shows accuracy of signal at the output of ADS7253 at 25°C and Figure 34 shows accuracy of ADC at 75°C. It includes the linearity and gain error from the ADC itself.

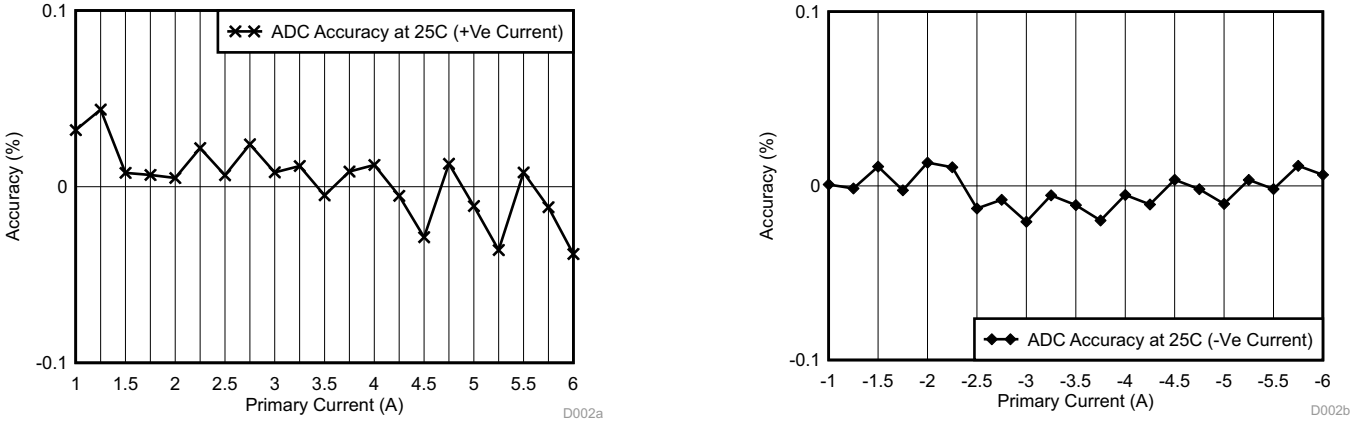


Figure 33. ADC Accuracy at 25°C (Left) for Positive Current (Right) for Negative Current

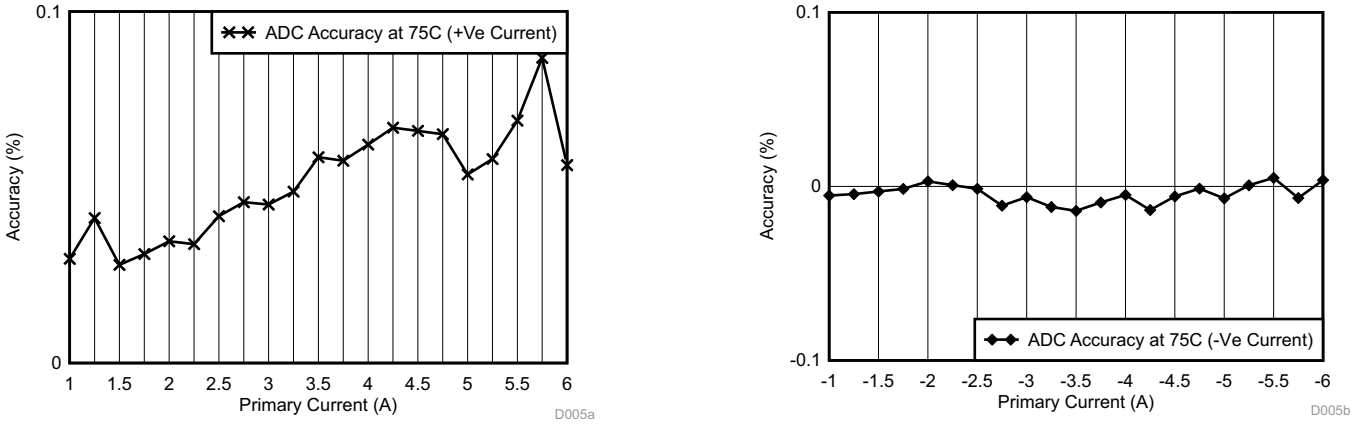


Figure 34. ADC Accuracy at 75°C (Left) for Positive Current (Right) for Negative Current

Figure 35 shows accuracy of signal for the entire signal chain (FDA + ADC) at 25°C and Figure 36 shows the total accuracy at 75°C. Note that in a typical drive application, the current sensor would be used from 30% to 100% of its nominal current rating so the accuracy should be considered for primary current from ±1.75A to ±6A.

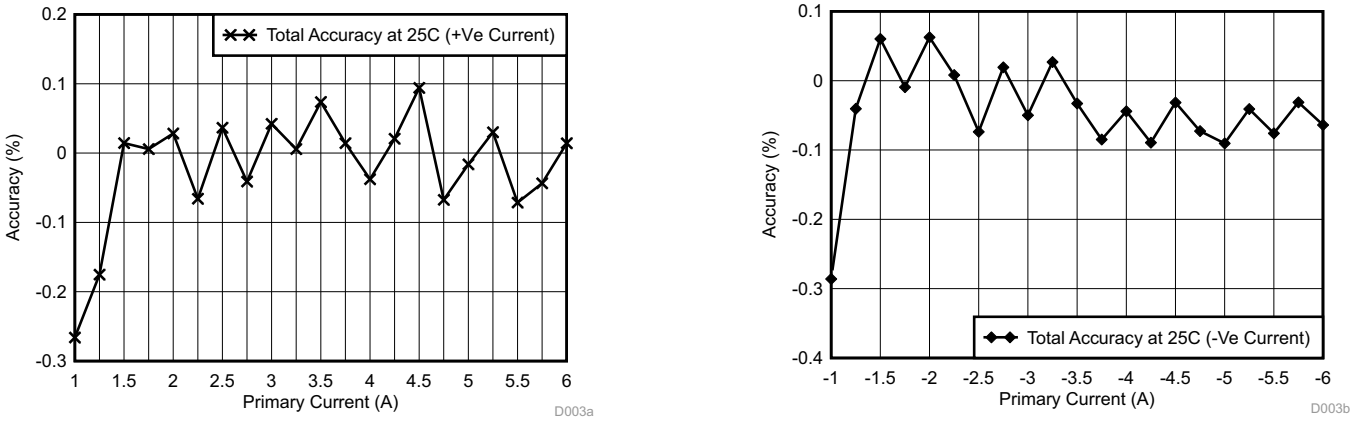


Figure 35. Total Accuracy at 25°C (Left) for Positive Current (Right) for Negative Current

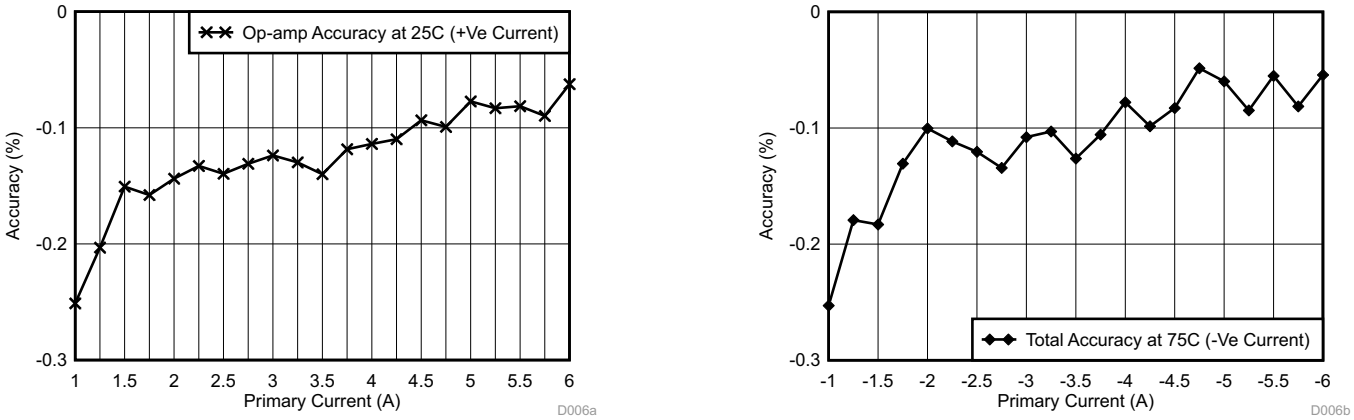


Figure 36. Total Accuracy at 75°C (Left) for Positive Current (Right) for Negative Current

9.5 DC Accuracy Tests Using Piccolo 28027 Internal ADC (on LaunchPad)

The accuracy of Internal ADC of Piccolo 28027 controller is measured along with the fluxgate-based reference design. Figure 37 shows the screenshot capture of ADC output code GUI. The total accuracy curve is as shown in Figure 38.

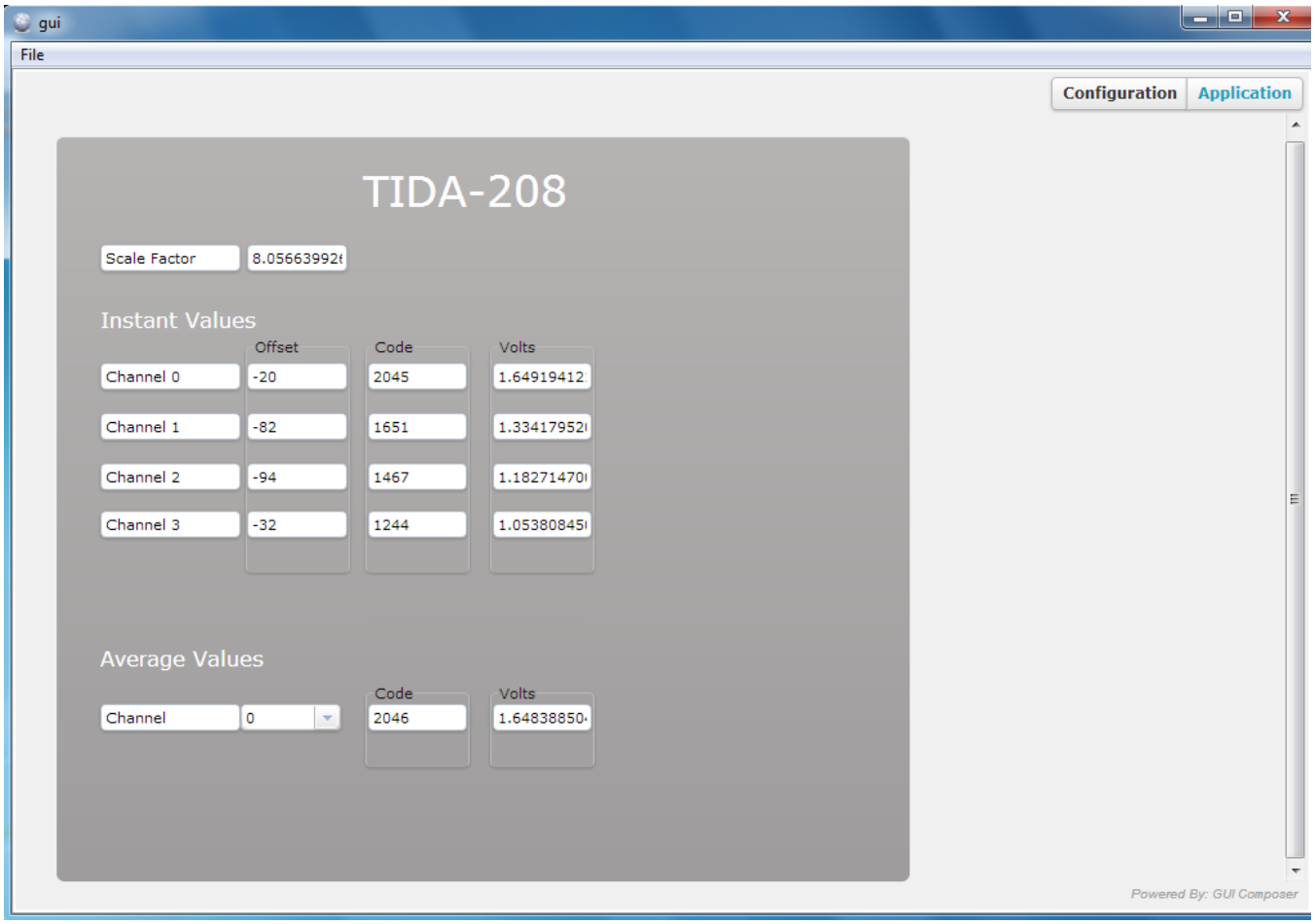


Figure 37. Screenshot of Internal ADC GUI for Piccolo Controller

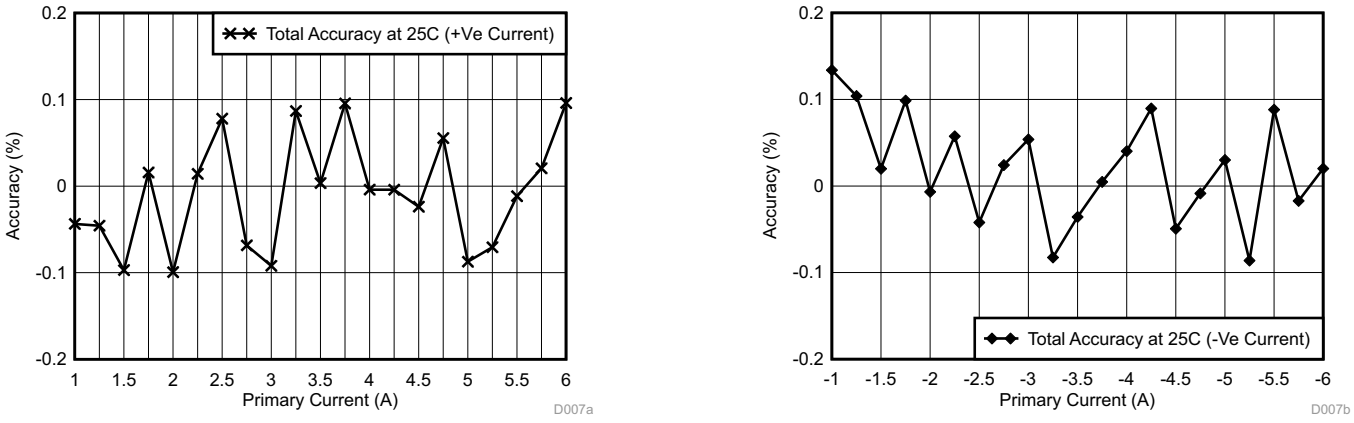


Figure 38. Total Accuracy While Using Internal ADC of Piccolo 28027 Controller (Left) for Positive Current (Right) for Negative Current

9.5.1 AC (or Dynamic) Performance Using Piccolo 28027 Internal ADC

For an AC current of 4.5 V_{RMS} at a frequency of 50 Hz, the conditioned voltage signal (at the output of OPA4322) is captured, and the FFT of the system is also taken using the Piccolo 28027 LaunchPad. Figure 39 shows the captured signal. Note the time period X2-X1 (= 20.05457026 ms), which corresponds to the 49.86-Hz frequency.

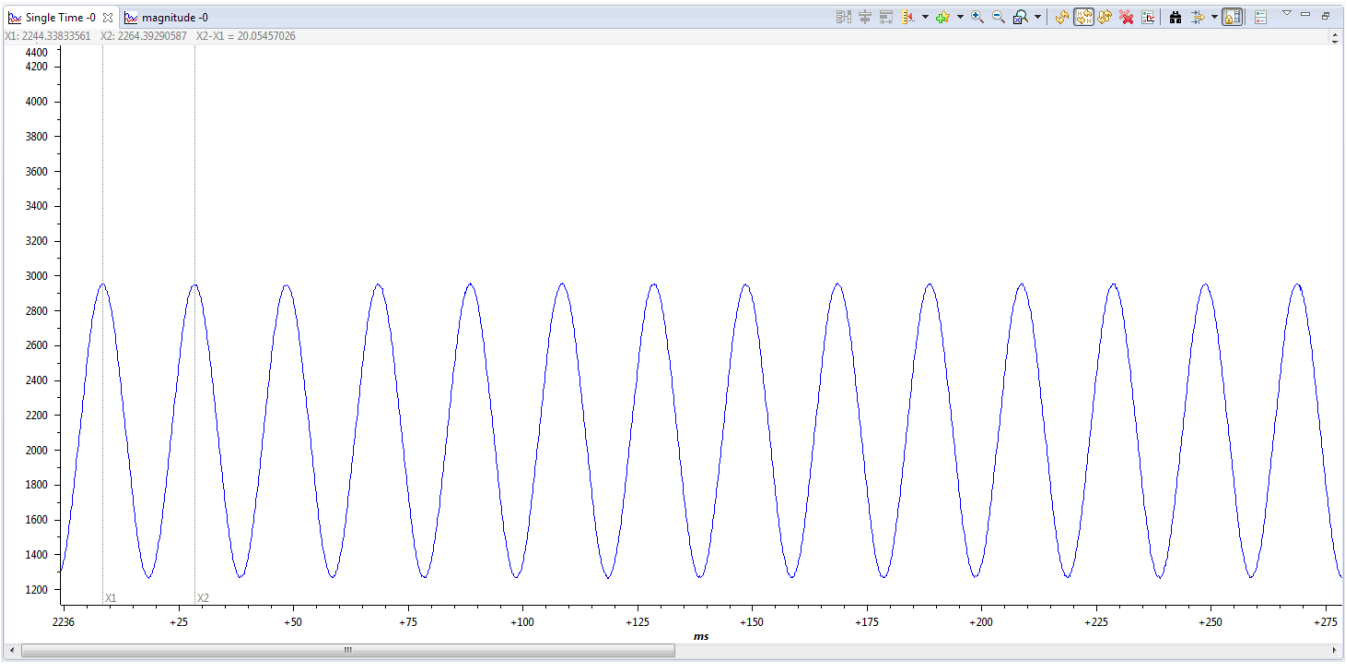


Figure 39. Signal Capture Using Piccolo 28027 LaunchPad

9.6 Power Supply and Reference Circuit Functionality Tests

The power supply circuit is tested for functionality and ripple measurement. Figure 40 shows the output of TPS7A4700 set at 5 V.

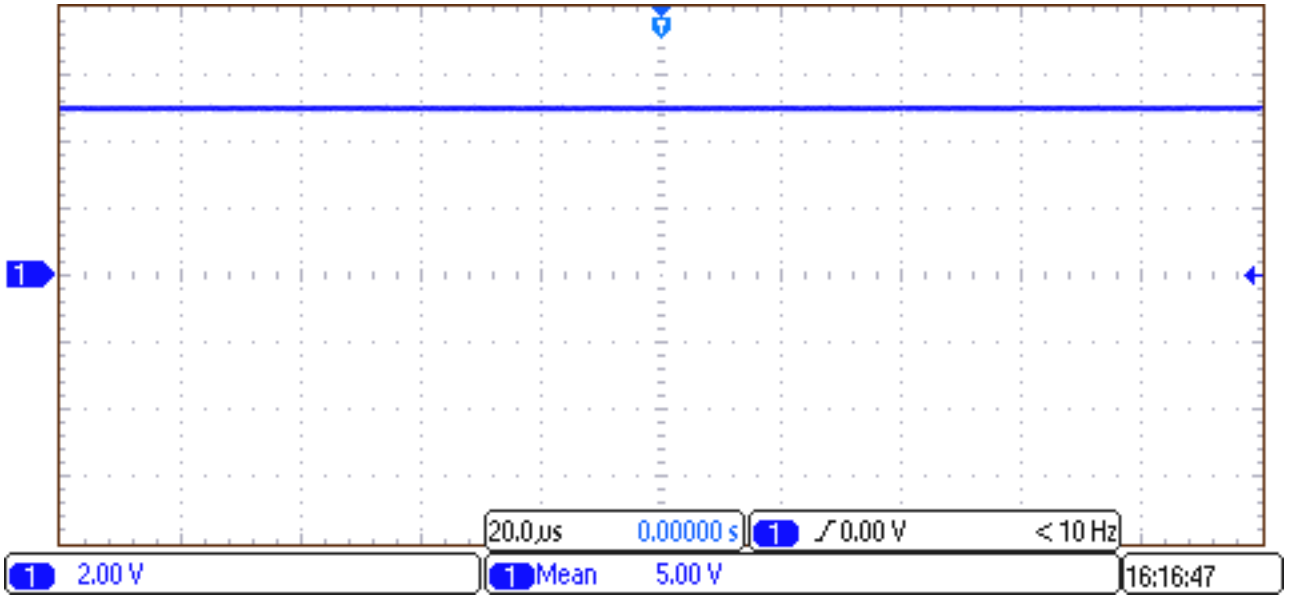


Figure 40. 5-V Signal From TPS7A4700

Figure 41 shows the 3.3-V digital supply voltage generated using TLV70033.

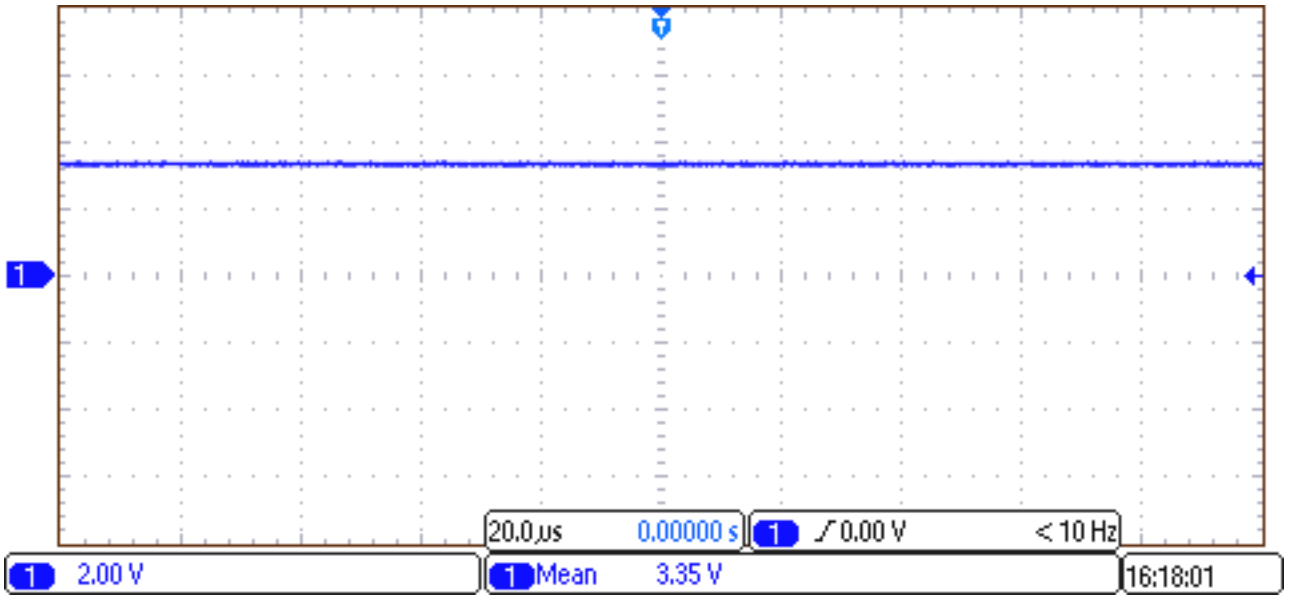


Figure 41. 3.3-V Reference Signal Generated by TLV70033

Figure 42 shows the output of REF5025 set internally at 2.5 V.

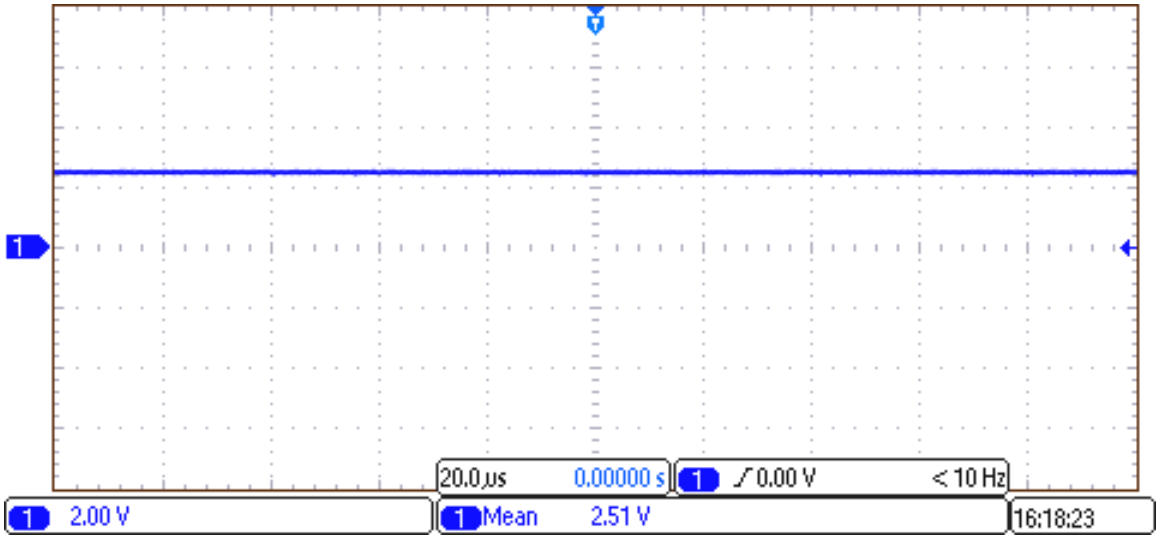


Figure 42. 2.5-V Reference Signal Generated by REF5025

Figure 43 and Figure 44 show the two outputs of REF2033 set internally at 3.3 V and 1.65 V, respectively.

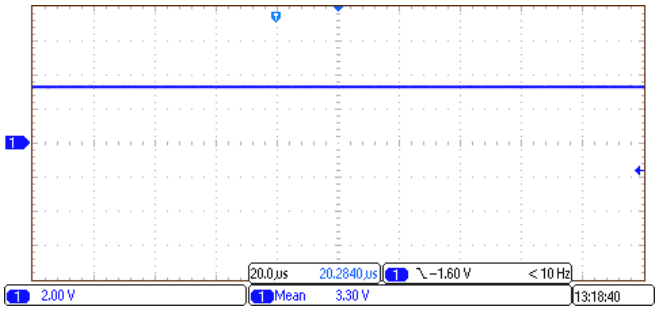


Figure 43. 3.3-V Reference Signal Generated by REF2033

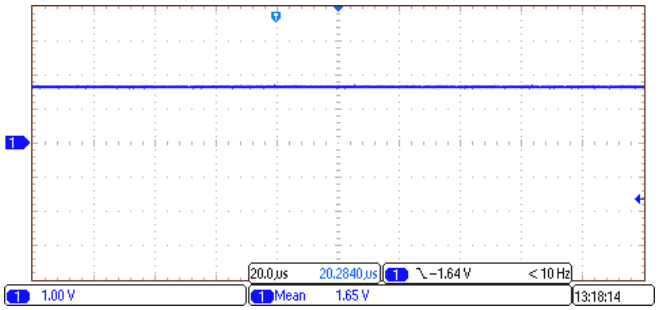


Figure 44. 1.65-V Reference Signal Generated by REF2033

9.7 Overcurrent and Earth Fault Detection Tests

The overcurrent and earth fault circuit are tested at 300% of the nominal current of the fluxgate sensors. The waveforms shown in Figure 45 and Figure 46 indicate the sensing of the overcurrent condition at VTH (pos), which requires 98 nanoseconds to detect.

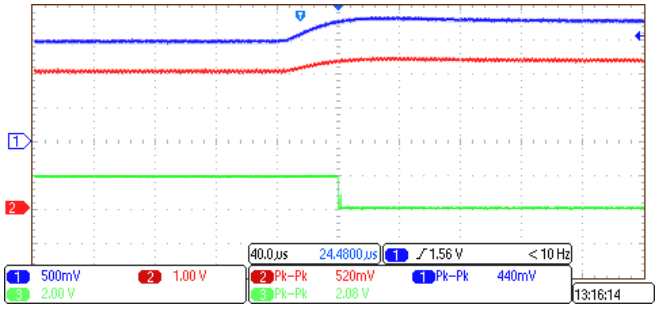


Figure 45. Overcurrent Detection at VTH (pos)

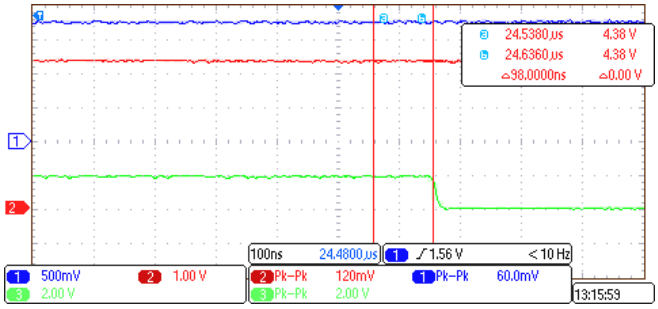


Figure 46. Overcurrent Detection at VTH (pos) — Zoomed

The waveforms shown in Figure 47 and Figure 48 indicate the sensing of the overcurrent condition at VTH (neg). The time required for the detection of the signal is 87.2 nanoseconds.

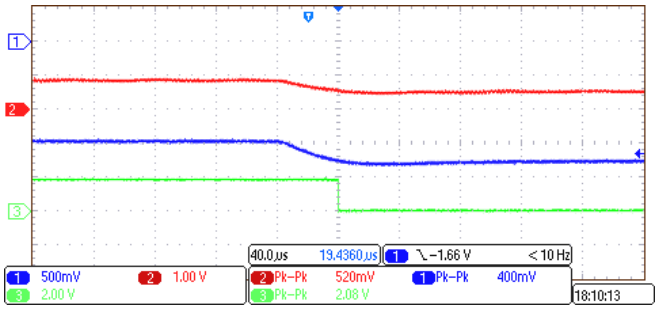


Figure 47. Overcurrent Detection at VTH (neg)

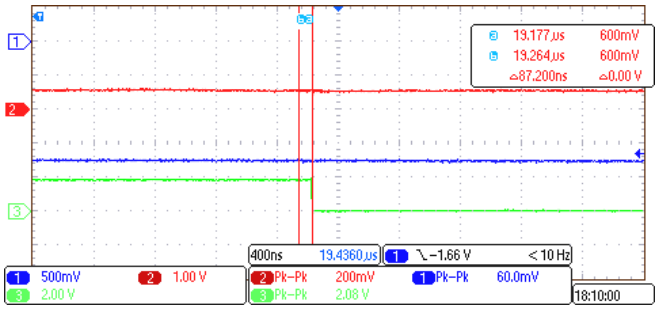


Figure 48. Overcurrent Detection at VTH (neg) — Zoomed

The waveforms shown in Figure 49 and Figure 50 indicate the sensing of earth fault condition at VTH (pos). The time required for the detection of the signal is 92 nanoseconds.

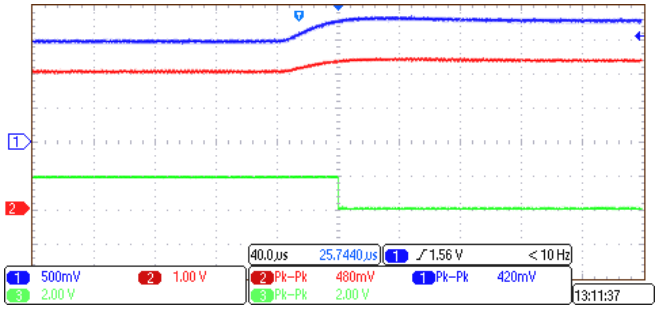


Figure 49. Earth Fault Detection at VTH (pos)

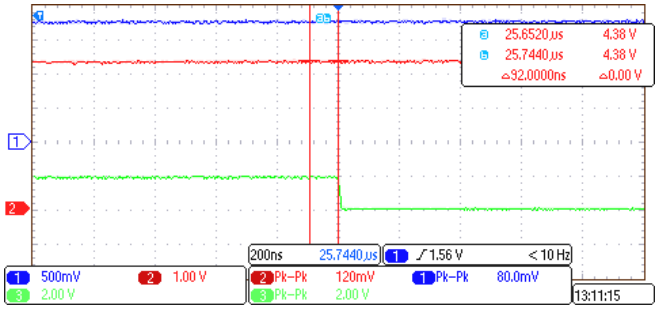


Figure 50. Earth Fault Detection at VTH (pos) — Zoomed

The waveforms shown in Figure 51 and Figure 52 indicate the sensing of earth fault condition at VTH (neg). The time required for the detection of the signal is 98 nanoseconds.

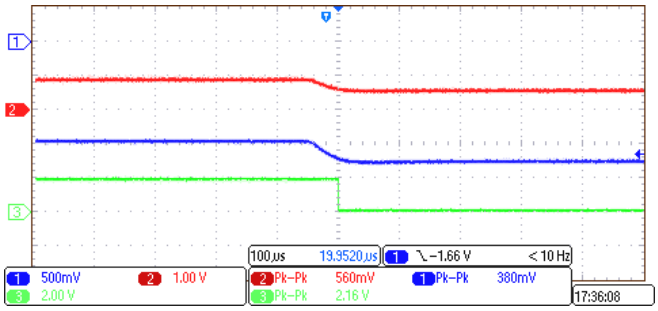


Figure 51. Earth Fault Detection at VTH (neg)

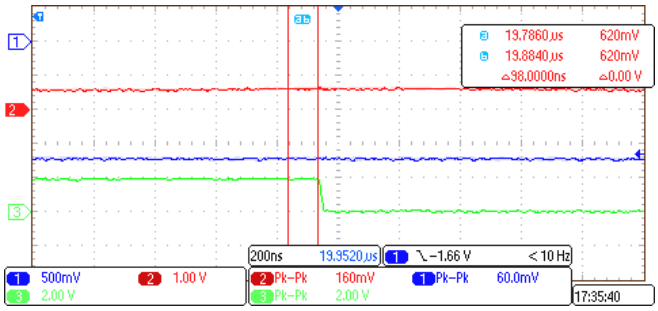


Figure 52. Earth Fault Detection at VTH (neg) — Zoomed

The comparators used in the protection circuits are open-drain outputs. The pull-up resistors are connected to 3.3 V (which is typically equal to digital supply of the MCU or FPGA) so that the high and low levels of the comparator outputs are within the sensing range of the MCU or FPGA.

10 Design Files

10.1 Schematics

To download the schematics, see the design files at TIDA-00208.

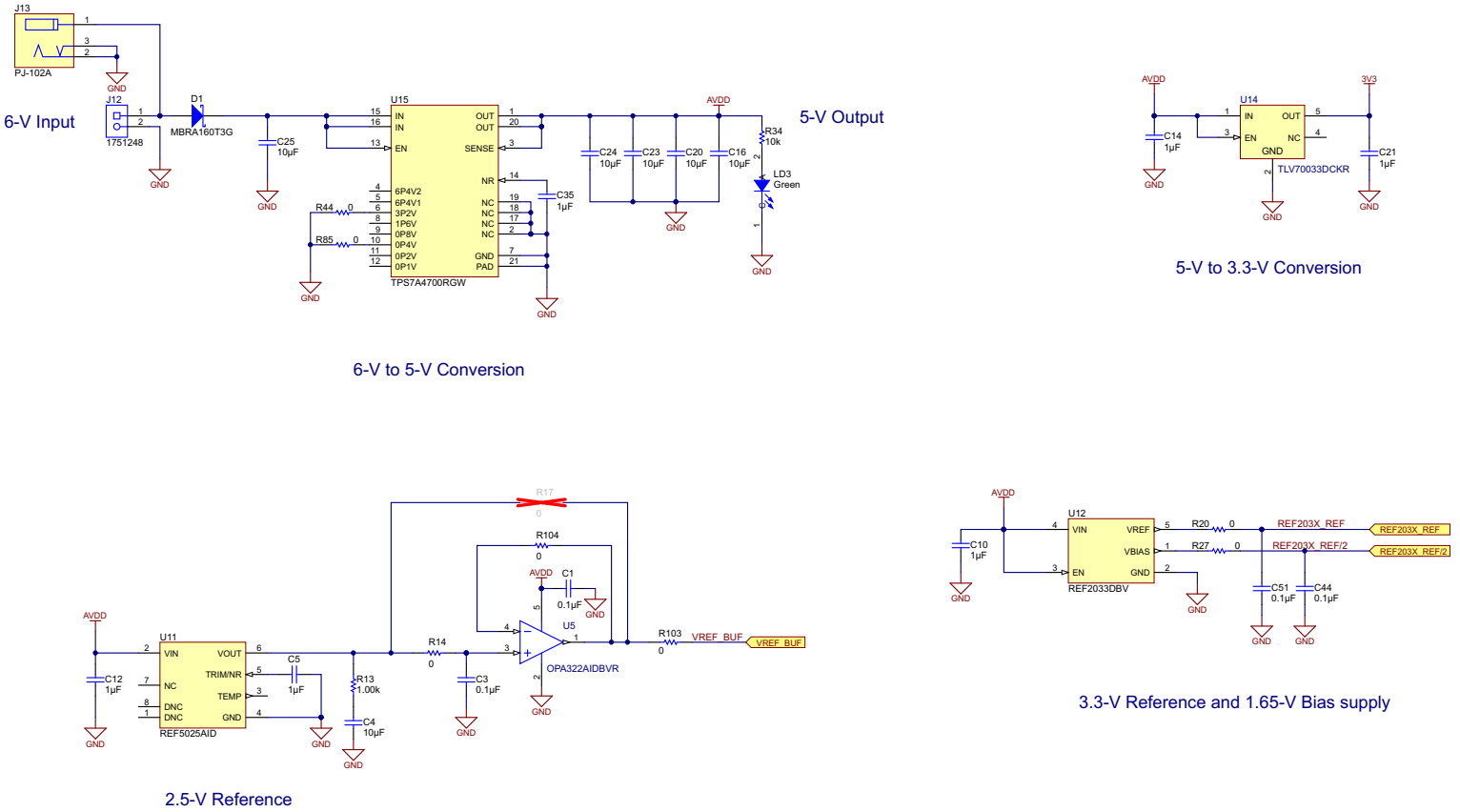
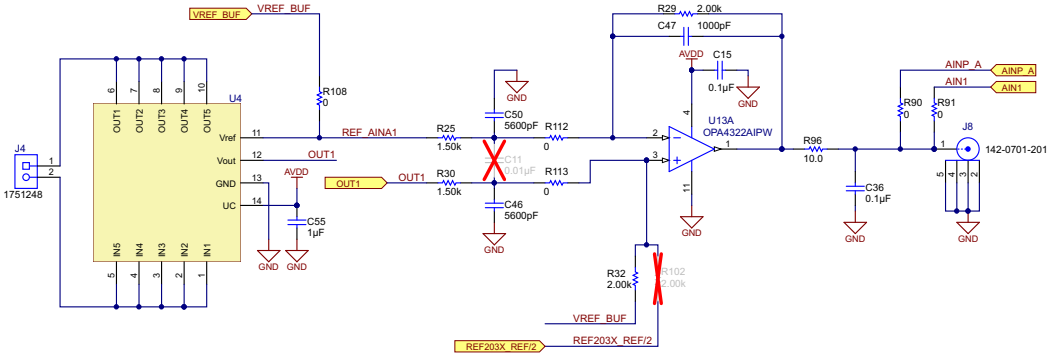
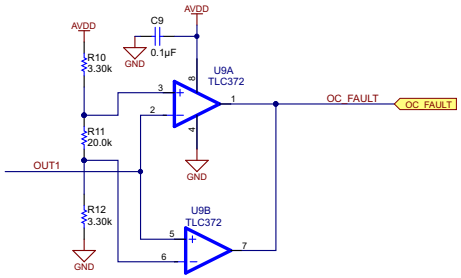


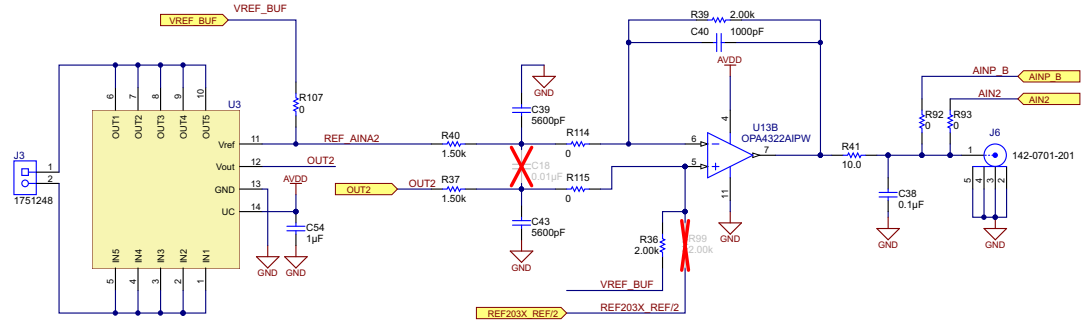
Figure 53. Schematics Page 1



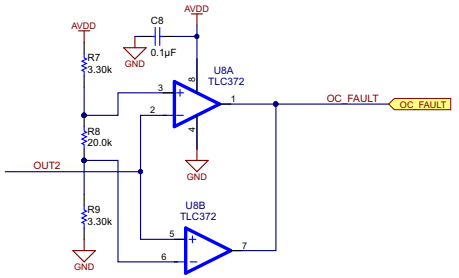
CH1 SIGNAL CONDITIONING



CH1 OVERCURRENT FAULT DETECTION

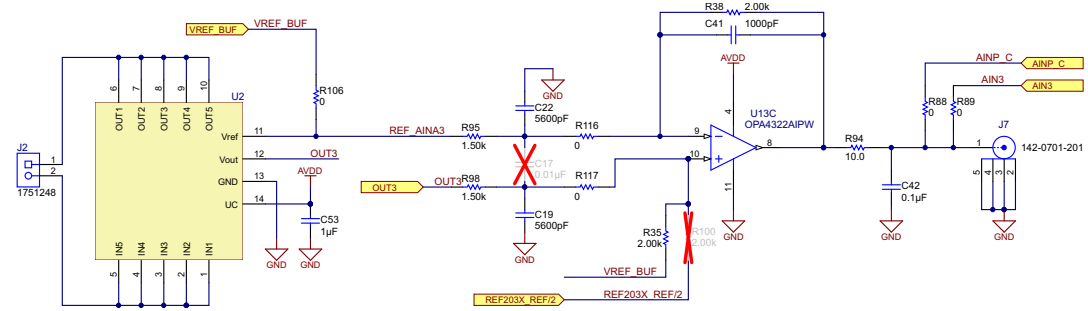


CH2 SIGNAL CONDITIONING

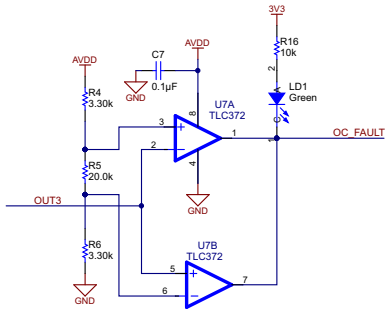


CH2 OVERCURRENT FAULT DETECTION

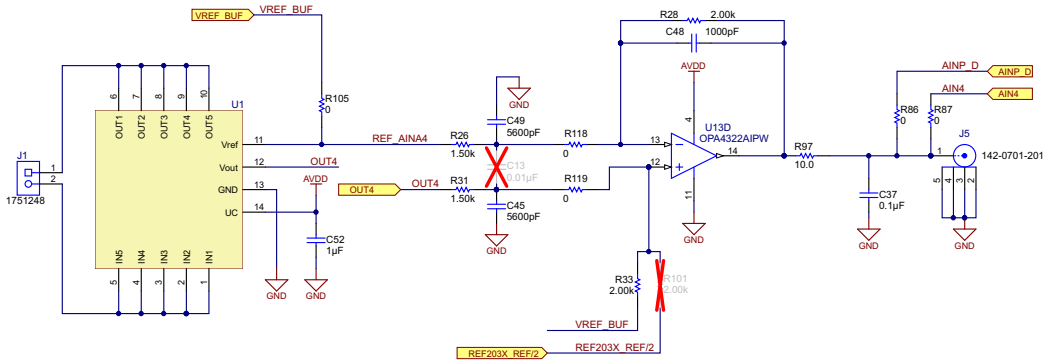
Figure 54. Schematics Page 2



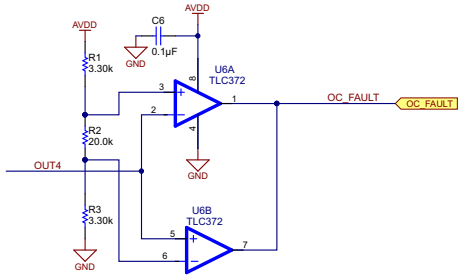
CH3 SIGNAL CONDITIONING



CH3 OVERCURRENT FAULT DETECTION



CH4 SIGNAL CONDITIONING



CH4 OVERCURRENT FAULT DETECTION

Figure 55. Schematics Page 3

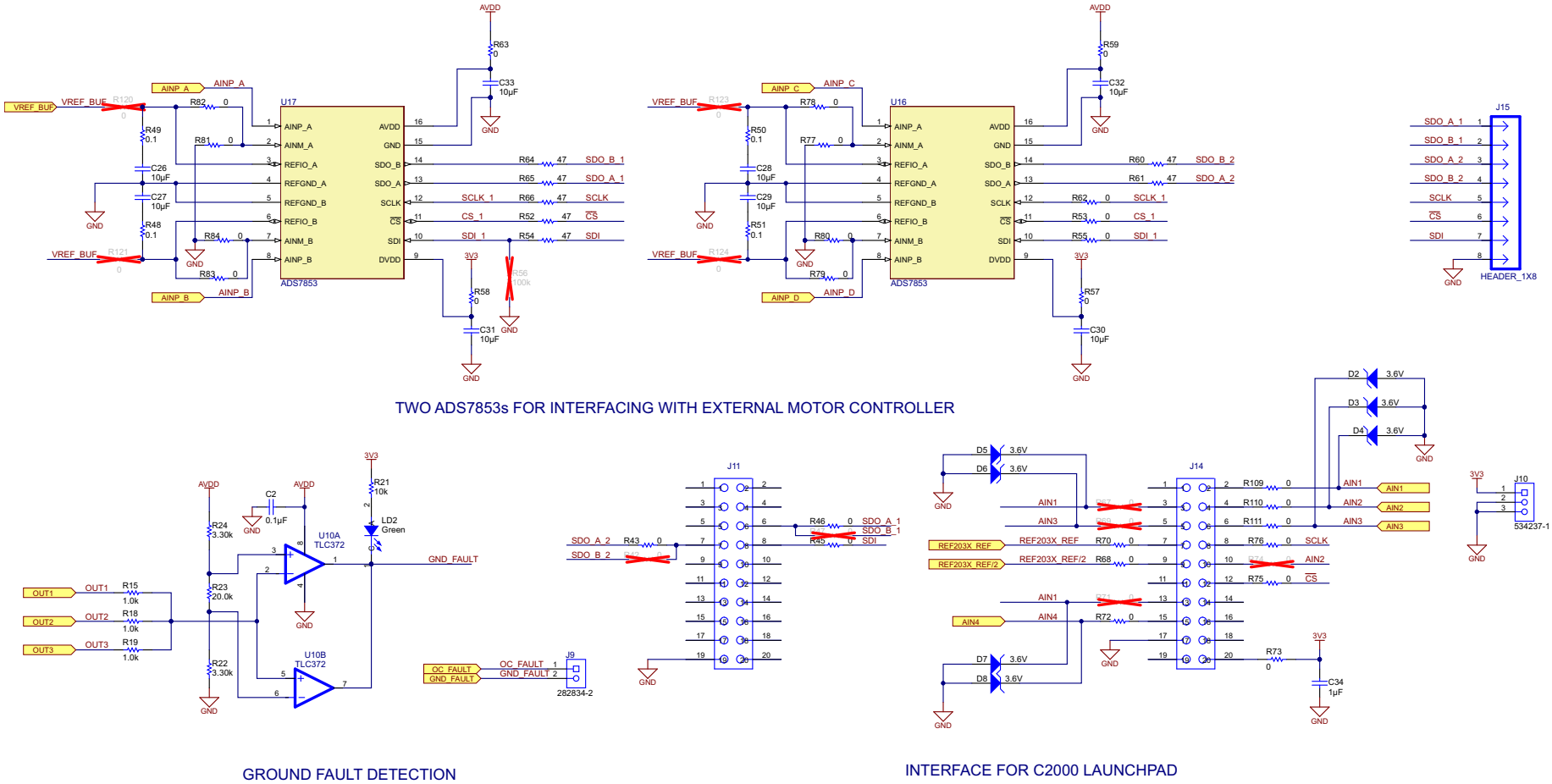


Figure 56. Schematics Page 4

10.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00208.

Table 8. BOM

QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER	MANUFACTURER PARTNUMBER	PCB FOOTPRINT	NOTE
1	!PCB	Printed Circuit Board	Any	TIDA-00208		Fitted
1	C4	CAP, CERM, 10 µF, 16 V, ±20%, X5R, 0603	Taiyo Yuden	EMK107BBJ106MA-T	0603	Fitted
1	D1	Diode, Schottky, 60 V, 1 A, SMA	ON Semiconductor	MBRA160T3G	SMA	Fitted
1	J10	Receptacle, 100 mil, 3×1, TH	TE Connectivity	534237-1	Receptacle, 100 mil, 3×1	Fitted
1	J13	Connector, DC Jack 2.1×5.5 mm, TH	CUI Inc.	PJ-102A	Power Jack, 14.4×11×9 mm	Fitted
1	J15	Header, Male 8-pin, 100-mil spacing	Sullins	PEC08SAAN	0.100 inch × 8	Fitted
1	J9	Terminal Block, 2×1, 2.54 mm, TH	TE Connectivity	282834-2	Terminal Block, 2×1, 2.54 mm, TH	Fitted
1	LBL1	Thermal Transfer Printable Labels, 0.650" W × 0.200" H - 10,000 per roll	Brady	THT-14-423-10	PCB Label 0.650" H × 0.200" W	Fitted
1	R13	RES, 1.00 kΩ, 1%, 0.1 W, 0603	Yageo America	RC0603FR-071KL	0603	Fitted
1	U11	Low-Noise, Very Low Drift, Precision Voltage Reference, 2.5 V, D008A	Texas Instruments	REF5025AID	D0008A	Fitted
1	U12	Dual Output Voltage Reference 3.3 V, DBV0005A	Texas Instruments	REF2033DBV	DBV0005A	Fitted
1	U13	20 MHz, Low Noise, RRIO, CMOS Operational Amplifier, 1.8 to 5.5 V, –40°C to 125°C, 14-pin SOP (PW0014A), Green (RoHS and no Sb/Br)	Texas Instruments	OPA4322AIPW	PW0014A	Fitted
1	U14	Single Output LDO, 200 mA, Fixed 3.3-V Output, 2 to 5.5-V Input, with Low IQ, 5-pin SC70 (DCK), –40°C to 125°C, Green (RoHS and no Sb/Br)	Texas Instruments	TLV70033DCKR	DCK0005A	Fitted
1	U15	36-V, 1-A, 4.17-μV_{RMS}, RF LDO Voltage Regulator, RGW0020A	Texas Instruments	TPS7A4700RGW	RGW0020A	Fitted
1	U5	20 MHz, Low Noise, RRIO, CMOS Operational Amplifier with Shutdown, 1.8 to 5.5 V, –40°C to 125°C, 5-pin SOT23 (DBV0005A), Green (RoHS and no Sb/Br)	Texas Instruments	OPA322AIDBVR	DBV0005A	Fitted
10	R1, R3, R4, R6, R7, R9, R10, R12, R22, R24	RES, 3.30 kΩ, 1%, 0.1 W, 0603	Yageo America	RC0603FR-073K3L	0603	Fitted
11	C1, C2, C6, C7, C8, C9, C15, C36, C37, C38, C42	CAP, CERM, 0.1 µF, 16 V, ±5%, X7R, 0603	Kemet	C0603C104J4RACTU	0603	Fitted

Table 8. BOM (continued)

QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER	MANUFACTURER PARTNUMBER	PCB FOOTPRINT	NOTE
2	J11, J14	CONN RCPT 20POS .100 DL STR SMD	FCI	89898-310ALF		Fitted
2	U16, U17	IC ADC 12BIT 1MSPS DUAL 16TSSOP	Texas Instruments	ADS7853	16TSSOP	Fitted
3	C3, C44, C51	CAP, CERM, 0.1 µF, 10 V, ±10%, X7R, 0603	Kemet	C0603C104K8RACTU	0603	Fitted
3	LD1, LD2, LD3	LED SmartLED Green 570NM	OSRAM	LG L29K-G2J1-24-Z	0603	Fitted
3	R15, R18, R19	RES, 1.0 kΩ, 5%, 0.1 W, 0603	Vishay-Dale	CRCW06031K00JNEA	0603	Fitted
3	R16, R21, R34	RES, 10 kΩ, 5%, 0.1 W, 0603	Vishay-Dale	CRCW060310K0JNEA	0603	Fitted
4	C40, C41, C47, C48	CAP, CERM, 1000 pF, 25 V, ±5%, C0G/NP0, 0603	MuRata	GRM1885C1E102JA01D	0603	Fitted
4	J5, J6, J7, J8	Connector, TH, SMA	Emerson Network Power	142-0701-201	SMA	Fitted
4	R41, R94, R96, R97	RES, 10.0 Ω, 0.1%, 0.1 W, 0603	Yageo America	RT0603BRD0710RL	0603	Fitted
4	R48, R49, R50, R51	RES, 0.1 Ω, 1%, 0.1 W, 0603	Panasonic	ERJ-3RSFR10V	0603	Fitted
4	U1, U2, U3, U4	Sensor Current 50 A, 5 V, MOD	LEM USA Inc	CKSR X-NP	Module	Fitted
5	C16, C20, C23, C24, C25	CAP, CERM, 10 µF, 16 V, ±10%, X5R, 0805	MuRata	GRM21BR61C106KE15L	0805	Fitted
5	C34, C52, C53, C54, C55	CAP, CERM, 1 µF, 25 V, ±10%, X7R, 0603	MuRata	GRM188R71E105KA12D	0603	Fitted
5	H1, H2, H3, H5, H6	Machine Screw, Round, #4-40 × 1/4, Nylon, Philips panhead	BandF Fastener Supply	NY PMS 440 0025 PH	Screw	Fitted
5	H4, H7, H8, H9, H10	Standoff, Hex, 0.5"L #4-40 Nylon	Keystone	1902C	Standoff	Fitted
5	J1, J2, J3, J4, J12	Conn Term Block, 2POS, 3.5 mm, TH	Phoenix Contact	1751248	11×8.5×7.3 mm	Fitted
5	R2, R5, R8, R11, R23	RES, 20.0 kΩ, 1%, 0.1 W, 0603	Vishay-Dale	CRCW060320K0FKEA	0603	Fitted
5	U6, U7, U8, U9, U10	IC, Dual Differential Comparators, 2 to 36 Vin	Texas Instruments	TLC372	SO-8	Fitted
54	R14, R20, R27, R43, R44, R45, R46, R53, R55, R57, R58, R59, R62, R63, R68, R70, R72, R73, R75, R76, R77, R78, R79, R80, R81, R82, R83, R84, R85, R86, R87, R88, R89, R90, R91, R92, R93, R103, R104, R105, R106, R107, R108, R109, R110, R111, R112, R113, R114, R115, R116, R117, R118, R119	RES, 0 Ω, 5%, 0.1 W, 0603	Vishay-Dale	CRCW06030000Z0EA	0603	Fitted
6	C5, C10, C12, C14, C21, C35	CAP, CERM, 1 µF, 10 V, ±10%, X7R, 0805	Kemet	C0805C105K8RACTU	0805	Fitted

Table 8. BOM (continued)

QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER	MANUFACTURER PARTNUMBER	PCB FOOTPRINT	NOTE
6	FID1, FID2, FID3, FID4, FID5, FID6	Fiducial mark. There is nothing to buy or mount.	N/A	N/A	Fiducial	Fitted
7	D2, D3, D4, D5, D6, D7, D8	Diode, Zener, 3.6 V, 500 mW, SOD-123	Diodes Inc.	MMSZ5227B-7-F	SOD-123	Fitted
7	R52, R54, R60, R61, R64, R65, R66	RES, 47 Ω, 5%, 0.1 W, 0603	Vishay-Dale	CRCW060347R0JNEA	0603	Fitted
8	C19, C22, C39, C43, C45, C46, C49, C50	CAP, CERM, 5600 pF, 25 V, ±5%, C0G/NP0, 0603	TDK	C1608C0G1E562J	0603	Fitted
8	C26, C27, C28, C29, C30, C31, C32, C33	CAP, CERM, 10 µF, 25 V, ±20%, X5R, 0603	TDK	C1608X5R1E106M080AC	0603	Fitted
8	R25, R26, R30, R31, R37, R40, R95, R98	RES, 1.50 k, 1%, 0.1 W, 0603	Vishay-Dale	CRCW06031K50FKEA	0603	Fitted
8	R28, R29, R32, R33, R35, R36, R38, R39	RES, 2.00 k, 1%, 0.1 W, 0603	Vishay-Dale	CRCW06032K00FKEA	0603	Fitted
0	C11, C13, C17, C18	CAP, CERM, 0.01 µF, 25 V, ±5%, C0G/NP0, 0603	Kemet	C0603H103J3GACTU	0603	Not Fitted
0	R17, R42, R47, R67, R69, R71, R74, R120, R121, R123, R124	RES, 0 Ω, 5%, 0.1 W, 0603	Vishay-Dale	CRCW06030000Z0EA	0603	Not Fitted
0	R56	RES, 100 kΩ, 1%, 0.1 W, 0603	Vishay-Dale	CRCW0603100KFKEA	0603	Not Fitted
0	R99, R100, R101, R102	RES, 2.00 k, 1%, 0.1 W, 0603	Vishay-Dale	CRCW06032K00FKEA	0603	Not Fitted

10.3 PCB Layout

To download the layer plots, see the design files at TIDA-00208.

NOTE: The total dimension of the board is 120 × 100 mm.

10.3.1 Layout Guidelines

Layout of Amplifier Section

The OPA4322 is a wideband amplifier. To realize the full operational performance of the device:

1. Follow good high-frequency PCB layout practices.
2. Connect the bypass capacitors between each supply pin and ground as close to the device as possible.
3. Design the bypass capacitor traces for minimum inductance.

Layout of ADC Section

The most important considerations in designing the PCB layout are as follows:

1. Keep the length of traces from the reference buffer circuit (REF and OPA) to the REFP input pin of the ADC as small as possible to minimize the trace inductance that can lead to instability and potential issues with the accurate settling of the reference voltage.
2. Locate the input driver circuit as close as possible to the inputs of the ADC to minimize loop area, making the layout more robust against EMI/RFI rejection. Similarly, keep the resistors and capacitor of the anti-aliasing filter at the inputs of the ADC close together and close to the inputs of the ADC to minimize the loop area.
3. Use a ground plane underneath the device and partition the PCB into analog and digital sections. Avoid crossing digital lines with the analog signal path and keep the analog input signals and the reference input signals away from noise sources.
4. Keep the power sources to the device clean and well-bypassed. Use 10-µF, ceramic bypass capacitors in close proximity to the analog (AVDD) and digital (DVDD) power-supply pins. Avoid placing vias between the AVDD and DVDD pins and the bypass capacitors. Connect all ground pins to the ground plane using short, low impedance paths.
5. Bypass the REFIO-A and REFIO-B reference inputs and outputs with 10-µF, X7R-grade, 0805-size, 16-V rated ceramic capacitors (CREF-x). Place the reference bypass capacitors as close as possible to the reference REFIO-x pins and connect the bypass capacitors using short, low-inductance connections. Avoid placing vias between the REFIO-x pins and the bypass capacitors. Use small 0.1-Ω to 0.2-Ω resistors (RREF-x) in series with the reference bypass capacitors to improve stability.
6. Place the fly-wheel RC filters immediately next to the input pins. Among ceramic surface-mount capacitors, COG (NPO) ceramic capacitors provide the best capacitance precision. The type of dielectric used in COG (NPO) ceramic capacitors provides the most stable electrical properties over voltage, frequency, and temperature changes.

10.3.2 Layout Plots

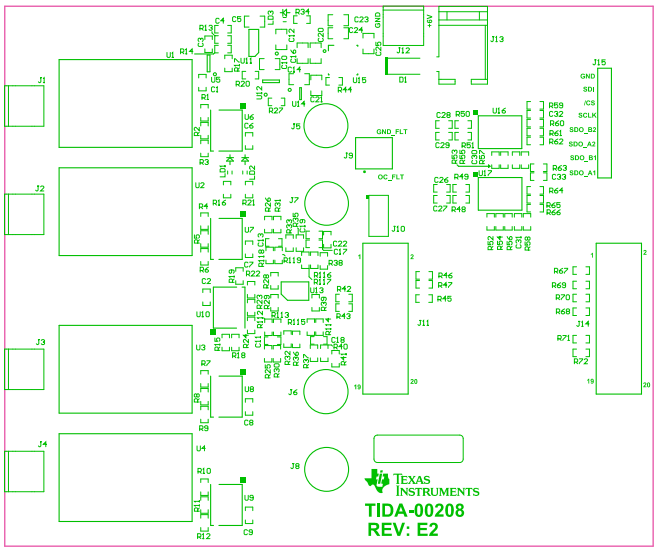


Figure 57. Top Overlay

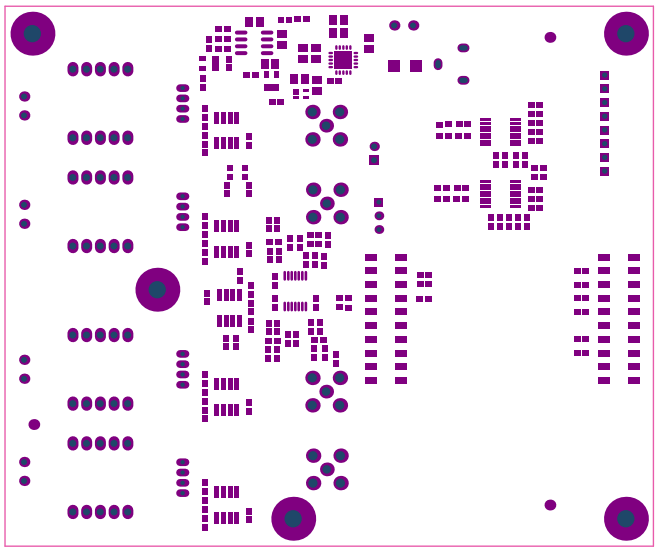


Figure 58. Top Solder

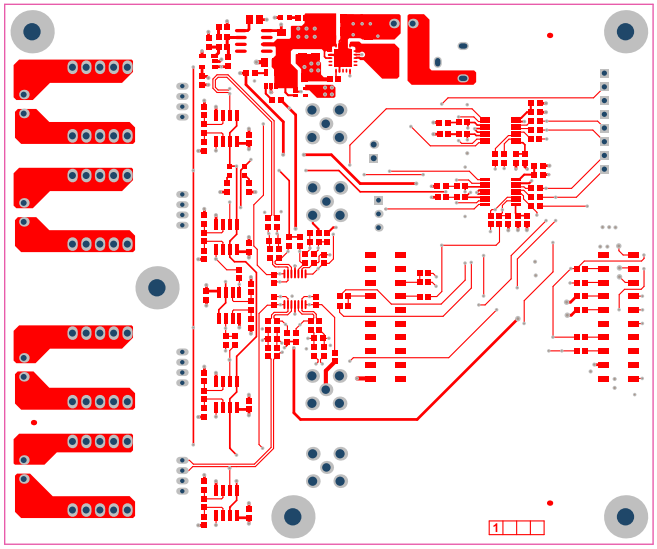


Figure 59. Top Layer

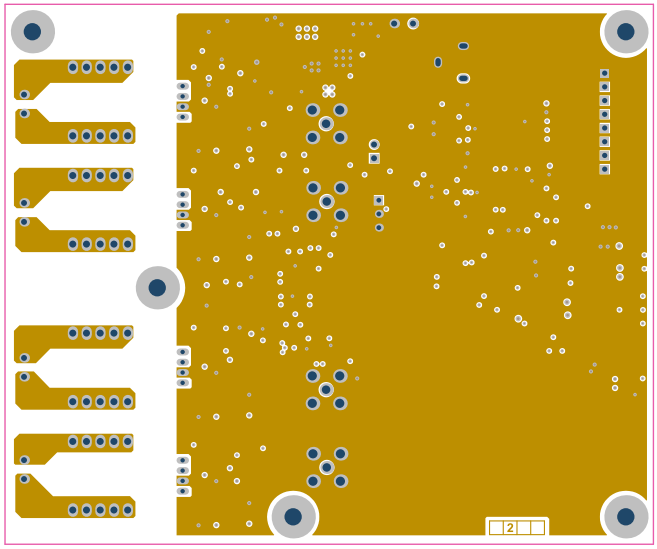


Figure 60. Mid1 Layer

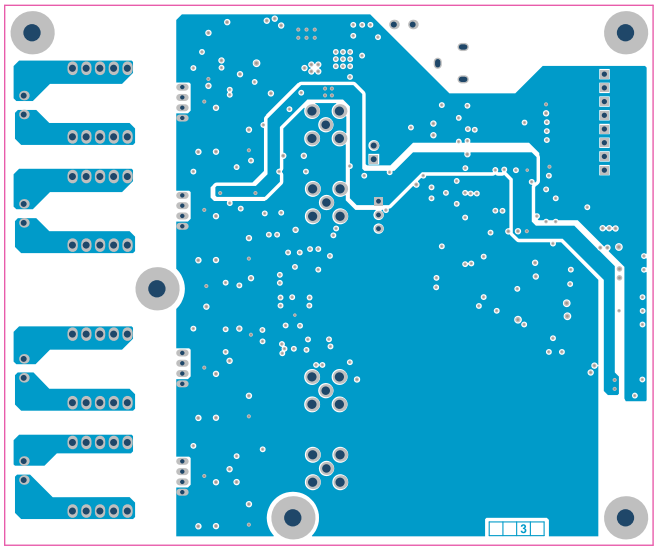


Figure 61. Mid2 Layer

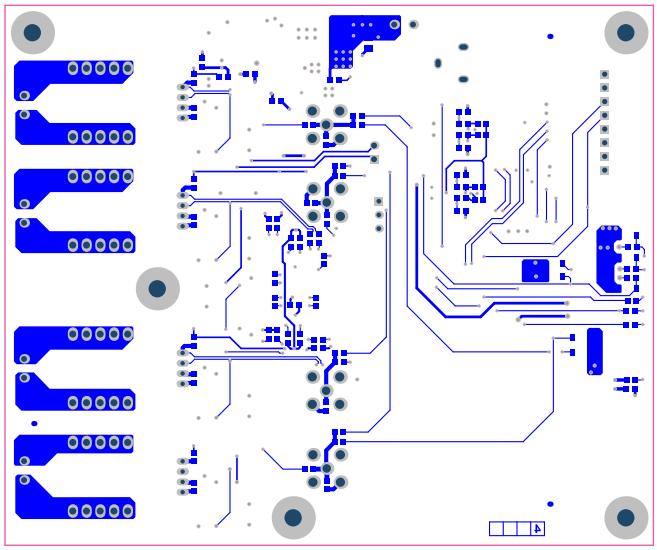


Figure 62. Bottom Layer

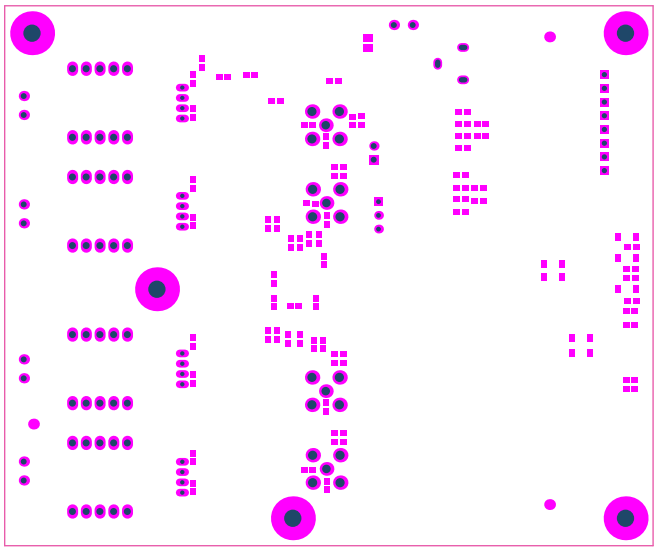


Figure 63. Bottom Solder

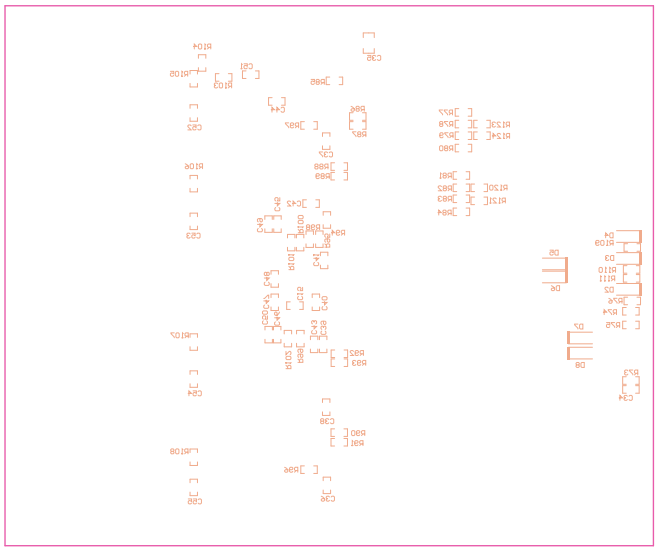


Figure 64. Bottom Overlay

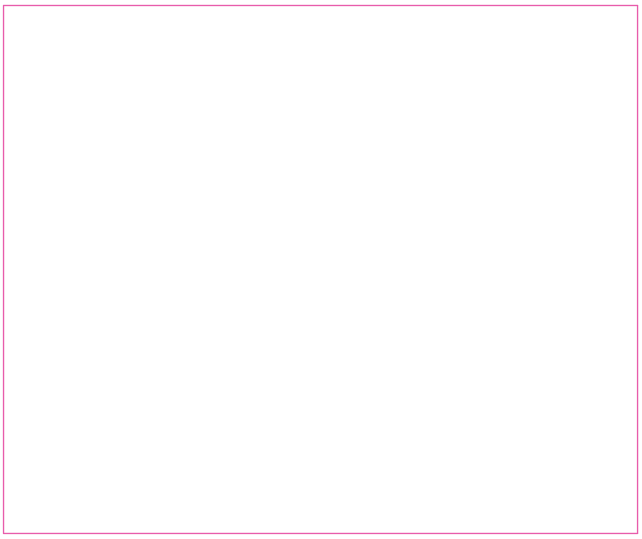


Figure 65. M1 Board Outline

10.4 Altium Project

To download the Altium project files, see the design files at TIDA-00208.

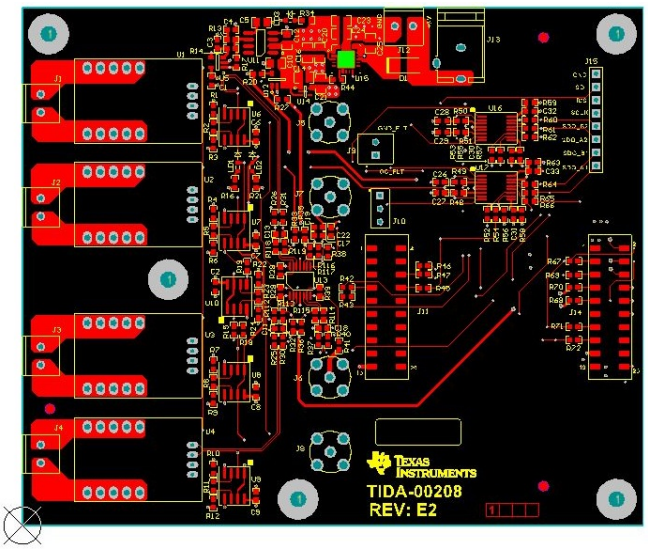


Figure 66. Top Layer

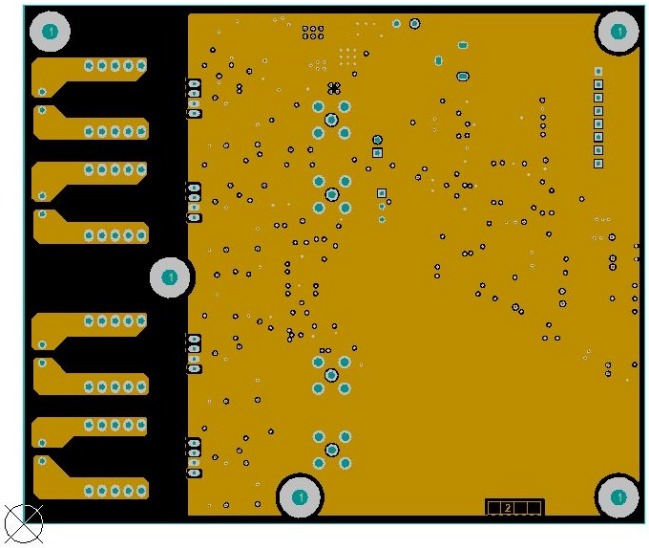


Figure 67. GND Layer

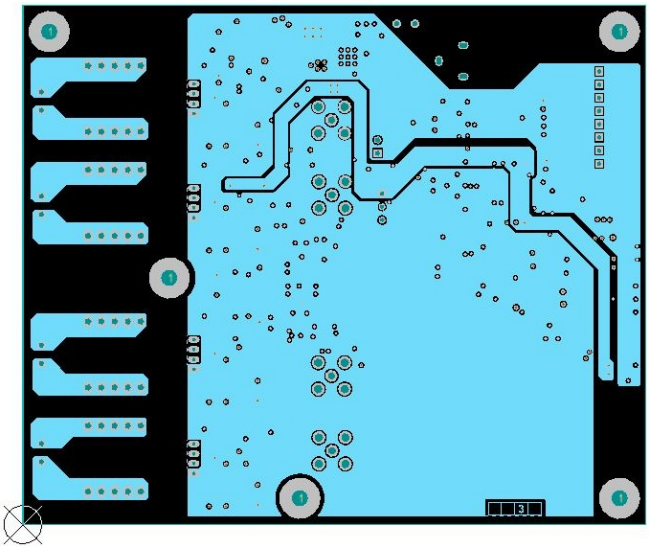


Figure 68. PWR Layer

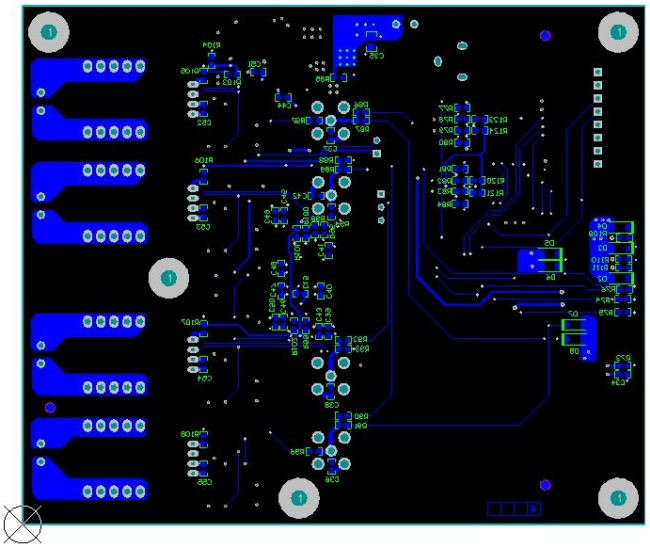


Figure 69. Bottom Layer

10.5 Gerber Files

To download the Gerber files, see the design files at TIDA-00208.

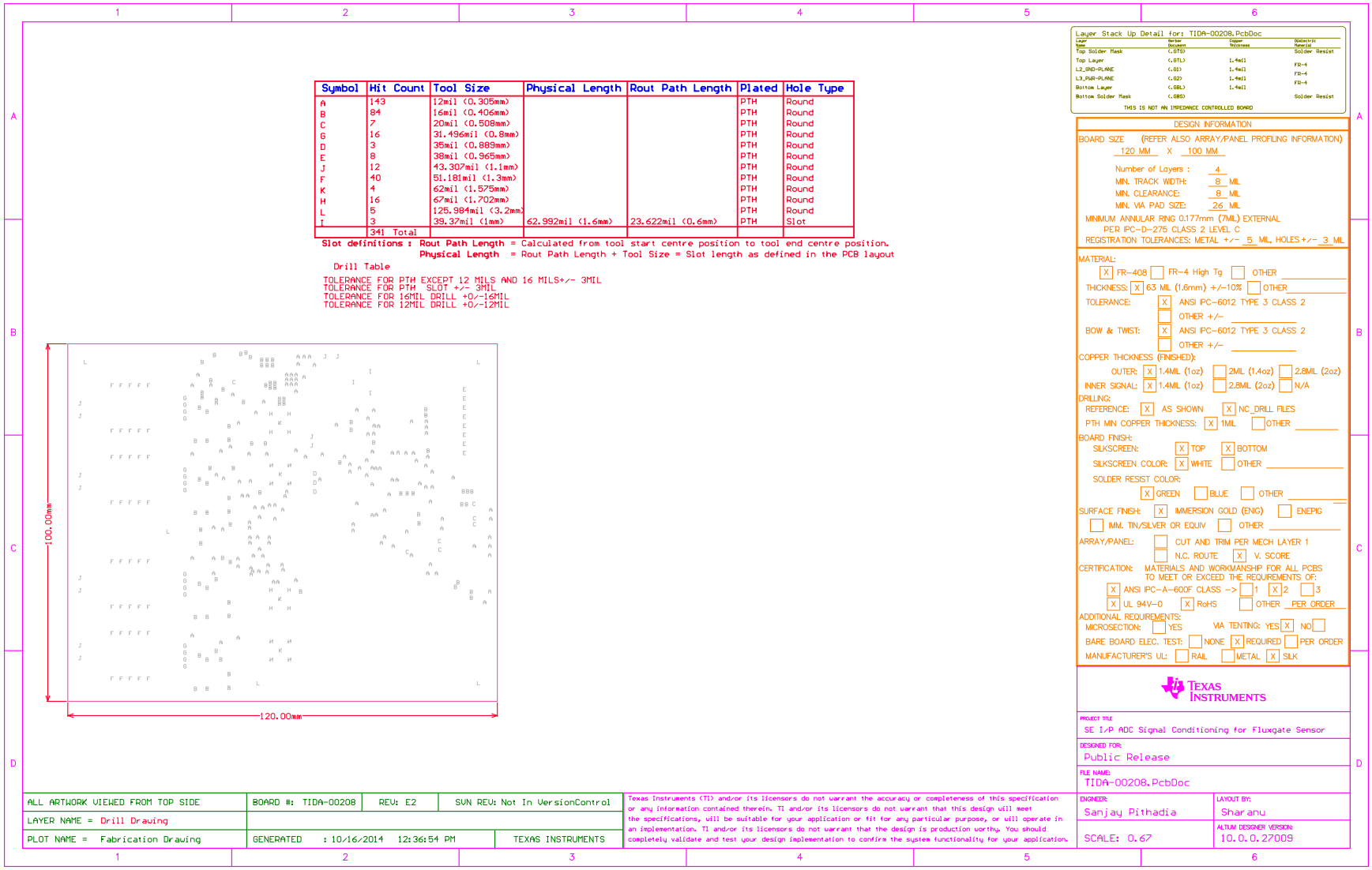


Figure 70. Fabrication Drawing

10.6 Assembly Drawings

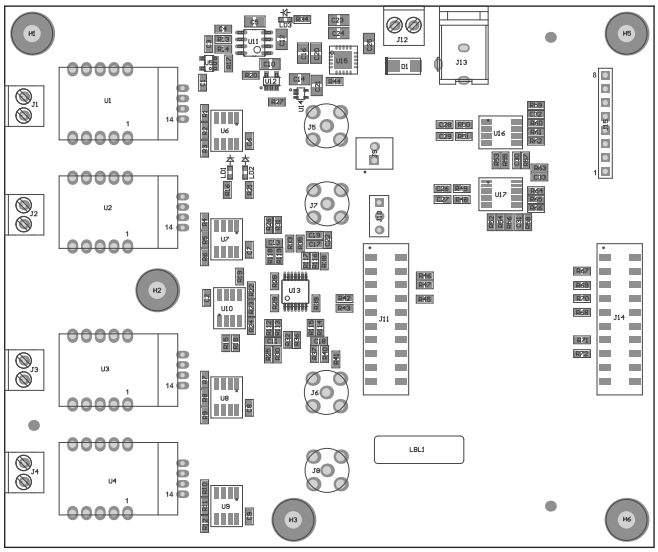


Figure 71. Top Assembly Drawing

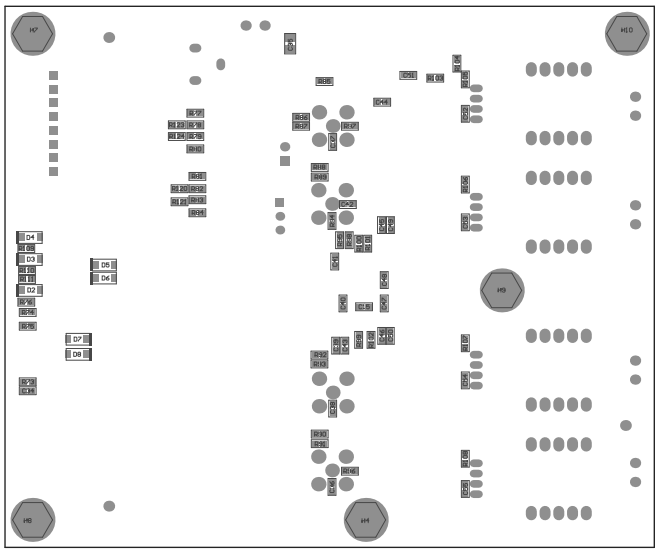


Figure 72. Bottom Assembly Drawing

10.7 Software Files

To download the software files, see the design files at TIDA-00208.

11 References

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2. Dominggus Yosua Suitella, Dr. Ir. Djoko Windarto, MT. *High Precision Fluxgate Current Sensor* (PDF)
3. Krzysztof Iniewski, ed. *Smart Sensors for Industrial Applications*. CRC Press, 2013.
4. Vaibhav Kumar. *18-Bit, 1MSPS Data Acquisition Block (DAQ) Optimized for Lowest Distortion and Noise*, Texas Instruments (SLAU515)
5. FilterPro™ Software (Tool Folder)
6. *LAUNCHXL-F28027 C2000 Piccolo LaunchPad Experimenter Kit*, Texas Instruments (SPRUHH2)

12 About the Author

SANJAY PITHADIA is a systems engineer at Texas Instruments where he is responsible for developing subsystem design solutions for the Industrial Motor Drive segment. Sanjay has been with TI since 2008 and has been involved in designing products related to energy and smart grid. Sanjay brings to this role his experience in analog design, mixed signal design, industrial interfaces, and power supplies. Sanjay earned his bachelor of technology in electronics engineering at VJTI, Mumbai.

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