TI Designs

EN55011-Compliant, Industrial Temperature 10/100-Mbps Ethernet PHY Brick

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Design Resources

TIDA-00207	Tool Folder Containing Design Files
DP83848K	Product Folder
TPD4E1U06	Product Folder
TPS75433	Product Folder
TPS71518	Product Folder
CDCE913	Product Folder
CDCLVC1102	Product Folder
EK-TM4C1294XL	MCU LaunchPad™ Tool Folder

TI E2E™ Community

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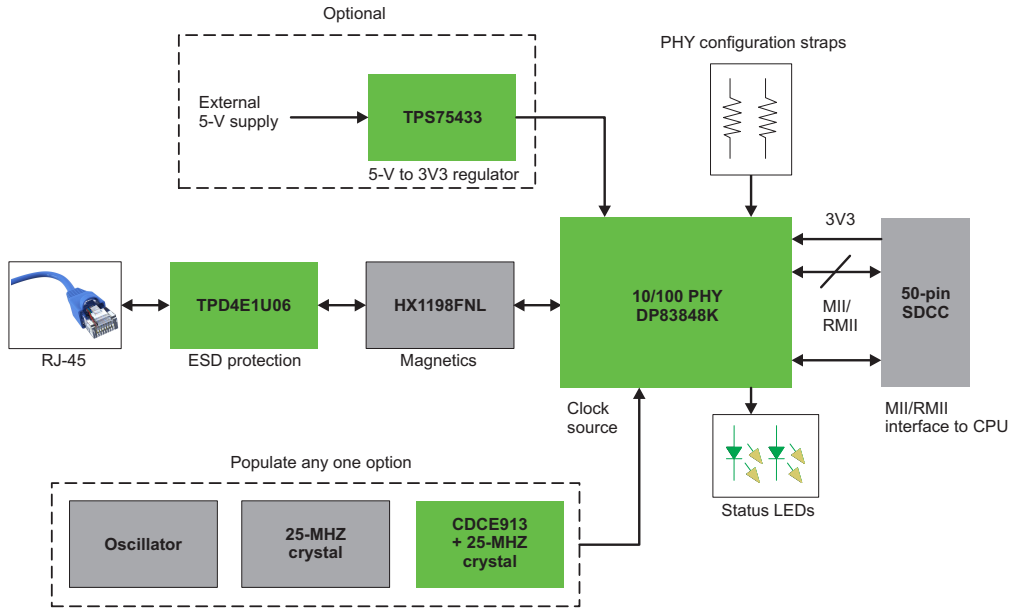
Design Features

- Low Power Consumption: 264 mW
- Meets EN55011 Class-A Radiated Emission Requirements
- Meets IEC61000-4-2 Level-4 Criterion B
- DP83848K Ethernet PHY Configured for MII Interface
- Programmable LED Support for Link and Activity
- External Isolation Transformer with Common-Mode Choke on PHY Side for Improved EMI and EMC performance
- HBM ESD Protection on RD± and TD± of 4 kV for DP83848K

Featured Applications

- Industrial Applications: Circuit Breakers, Protection Relays, Smart Meters (AMI), Panel-Mount Multi-Function Power and Energy Meters
- Substation Automation Products like RTU, Protection Relay, IEDs, Gateways, and Serial Converters
- Drives and Motion Control
- Industrial Remote Monitoring: Remote I/O and Data Loggers



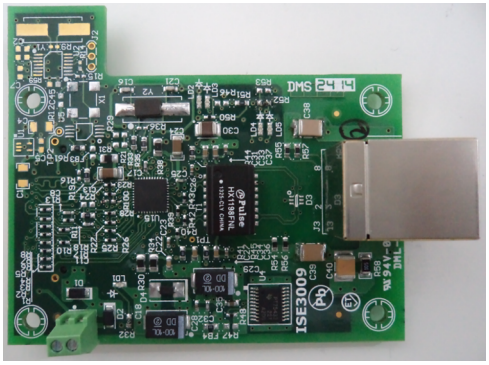


Figure 1. Top View

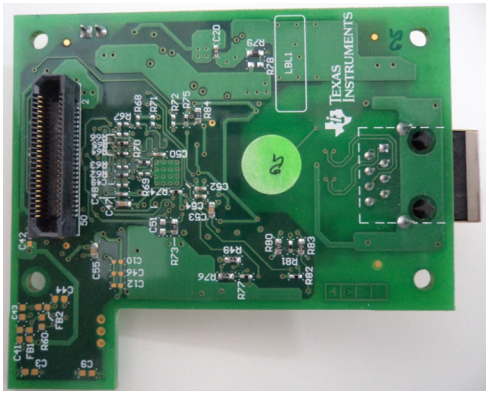


Figure 2. Bottom View

An IMPORTANT NOTICE at the end of this TI reference design addresses authorized use, intellectual property matters and other important disclaimers and information.

1 System Description

Ethernet has greatly expanded its scope over the years. A simple and effective design makes Ethernet the most popular networking solution at both the physical and data-link layers of the Open Systems Interconnection (OSI) model. The low cost of Ethernet hardware makes it an attractive option for industrial networking applications. Ethernet is also flexible because of the variety of media types and high speed options. The opportunity to use open protocols (such as TCP/IP over Ethernet networks) offers a high level of standardization and interoperability. The result has been an ongoing shift to the use of Ethernet for industrial control and automation applications from traditional serial field busses and proprietary communications.

A typical Ethernet application is shown in Figure 3.

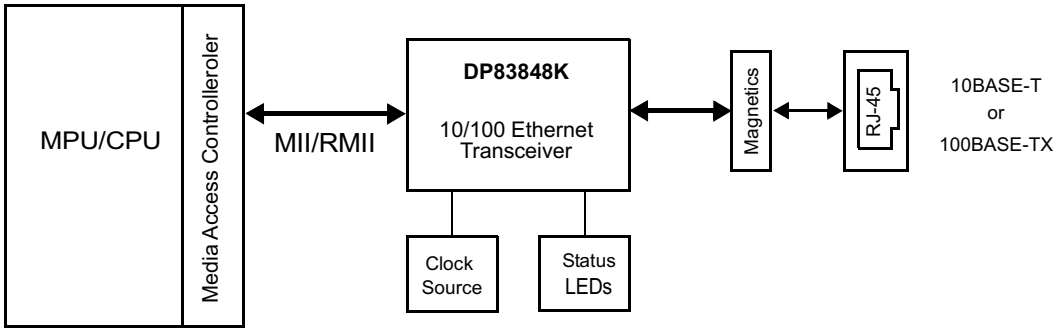


Figure 3. Typical Ethernet Application

This Ethernet PHY brick reference design enables TI's customers to quickly evaluate and design systems using TI's industrial Ethernet PHY transceiver devices. The design is compliant with EN55011 Class-A EMI requirements and immune to ESD up to ±15 kV (contact and air gap discharge), which helps reduce the time to test and release the systems to market. This design provides a 50-terminal interface to a 32-bit Cortex M4 processor-based controller board and is tested with TI's TIVA™ controller. The compact board design (2 × 3 inches) allows adoption to a variety of products with minimal efforts. In short, this reference design is an easily adaptable design platform for multiple industrial Ethernet end applications.

The reference design platform demonstrates the advanced performance and features of the DP83848K Ethernet PHY transceiver device. The design supports 10/100 Base-T and is compliant with the IEEE 802.3 standard. The device uses a single power supply (5 V with an onboard regulator of 3.3 V or 3.3 V directly coming from the 50-terminal interface). All other voltages required for the Ethernet PHY transceiver are internally generated within the device.

2 Design Features

The primary objective of this design is to create a platform that helps evaluate DP83848K in a compact form-factor board. The DP8384K addresses the quality and reliability for space sensitive applications in systems operating in the industrial temperature range. The DP83848K also offers performance exceeding the IEEE specifications with superior interoperability. The design features for this reference design are given in Table 1.

Table 1. Design Features

DEVICE	DESCRIPTION
Ethernet PHY	DP83848K Ethernet PHY features: • Media Independent Interface (MII) or Reduced Media Independent Interface (RMII): resistor strapping options • Configurable PHY addresses: resistor strapping options • Single register access for complete PHY status • Industrial temperature rating: –40°C to 85°C • IEEE 802.3u autonegotiation and parallel detection • IEEE 802.3u ENDEC, 10BASE-T transceivers and filters • IEEE 802.3u PCS, 100BASE-TX transceivers and filters • Tiny 6×6-mm LLP 40-pin Package
Power Supply	DP83848K is a low-power device that can operate with single 3.3-V ± 0.3-V supply Possible power input options are: • 5 V from external 2-terminal connector • 5-V DC input from MII interface connector and onboard regulator to generate 3.3 V • 3.3-V DC input from MII interface with no onboard regulator
Power Consumption	264 mW
MAC—Controller Interface	50-terminal MII interface connector
Clock	The design has three options to provide clock to DP83848K: • 25-MHz crystal with internal oscillator • External oscillator to generate the clock (not populated) • Using TI's CDCE913PW and a 25-MHz crystal to generate the clock over I2C lines (not populated)
Status LEDs	Two LEDs (link and activity with option to configure as pull-up or pull-down)
ESD	IEC61000-4-2: Level 4, Criterion B
Radiated Emission	EN55011, Class A

3 Block Diagram

This reference design is intended for all industrial applications where Ethernet PHY transceiver is used. The design files include schematics, bill of materials (BOM), layer plots, Altium files, Gerber files, and test results (see Section 8). Figure 4 shows the system block diagram of this reference design. The 10/100 Ethernet PHY is connected to an RJ-45 connector through an isolation amplifier. On the interface side, the design is connected to 50-pin connector to interface with a controller. Two status LEDs indicate a link and activity. The PHY is configured using different strap options. The PHY can be powered from the MII connector or using an external 5-V supply. Currently, the PHY is provided a clock signal using a crystal, but other options also available for clocking.

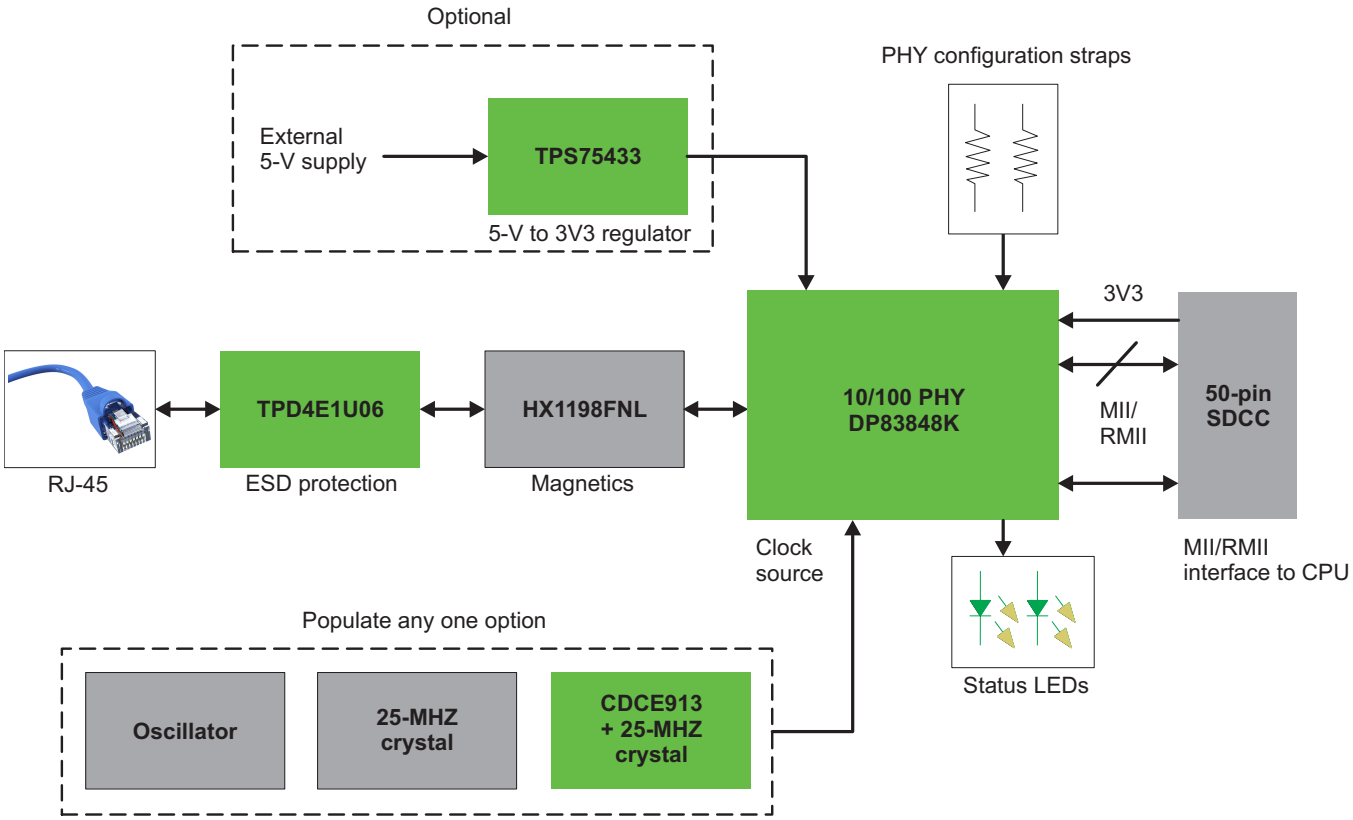


Figure 4. System Block Diagram

4 Ethernet PHY Features

4.1 DP83848K Ethernet PHY

The Ethernet PHY used in this reference design is the DP83848K. The DP83848K addresses the quality, reliability, and small form factor required for space sensitive applications in embedded systems operating in the industrial temperature range. The DP83848K outperforms the IEEE specifications with superior interoperability and an industry-leading performance beyond 137 m of Cat-V cable. The DP83848K also offers Auto-MDIX to remove cabling complications. DP83848K has superior ESD protection, greater than 4-KV Human Body Model, providing extremely high reliability and robust operation, ensuring a high-level performance in all applications. DP83848K offers two flexible LED indicators: one for link and the other for speed. In addition, both MII and RMII are supported to ensure the ease and flexibility of this design. The DP83848K is offered in a tiny 6×6-mm LLP 40-pin package and is ideal for industrial controls, building or factory automation, transportation, test equipment, and wireless base stations.

- Low-power 3.3-V, 0.18-µm CMOS technology
- Auto-MDIX for 10/100 Mbps
- Energy detection mode
- 3.3-V MAC interface
- RMII Rev. 1.2 interface (configurable)
- MII interface
- MII serial management interface (MDC and MDIO)
- IEEE 802.3u autonegotiation and parallel detection
- IEEE 802.3u ENDEC, 10BASE-T transceivers and filters
- IEEE 802.3u PCS, 100BASE-TX transceivers and filters
- Integrated ANSI X3.263 compliant TP-PMD physical sub-layer with adaptive equalization and baseline wander compensation
- Error-free operation beyond 137 m
- ESD protection greater than 4-KV Human body model
- Configurable LED for link and activity
- Single register access for complete PHY status
- 10/100 Mbps packet built in self test (BIST)
- 40-pin LLP package (6 × 6 × 0.8 mm)

4.2 MAC Data Interface

The DP83848K supports two modes of operation using the MII interface pins: MII and RMII. The modes of operation can be selected by strap options or register control. RMII mode is required to use the strap option, since it requires a 50-MHz clock instead of the normal 25 MHz. In the each of these modes, the IEEE 802.3 serial management interface is operational for device configuration and status. The serial management interface of the MII allows for the configuration and control of multiple PHY devices, gathering of status, error information, and the determination of the type and capabilities of the attached PHYs. In this reference design, the Ethernet PHY is interfaced to MAC through MII (Media Independent Interface).

The DP83848K incorporates the MII as specified in Clause 22 of the IEEE 802.3u standard. This interface may be used to connect PHY devices to a MAC in 10/100-Mbps systems. This section describes the nibble-wide MII data interface. The nibble-wide MII data interface consists of a receive bus and a transmit bus each with control signals to facilitate data transfer between the PHY and the upper layer (MAC). Figure 5 shows the signaling for MII.

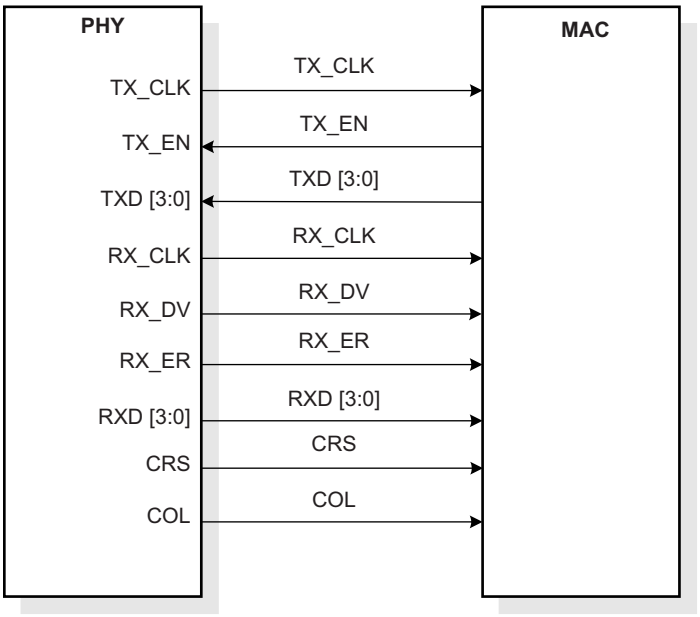


Figure 5. MII Signaling

The MII is a synchronous 4-bit wide nibble data interface that connects the PHY to the MAC in 100B-TX and 10B-T modes. The MII is fully compliant with IEEE802.3-2002 clause 22. The MII signals are summarized here:

- Transmit data signals: TXD[3:0]
- Transmit enable signal: TX_EN
- Receive data signals: RXD[3:0]
- Receive data valid signal: RX_DV
- Line status carrier sense signal: CRS

5 Getting Started

5.1 Clock Circuitry

The DP83848K supports an external CMOS-level oscillator source or a crystal resonator device. This design has three different options to generate the clock signal for DP83848K:

- 25-MHz crystal with internal oscillator
- External oscillator to generate the clock (not populated)
- Using TI's CDCE913PW and a 25-MHz crystal to generate the clock over I2C lines (not populated)

If an external clock source is used, X1 should be tied to the clock source and X2 should be left floating. The CMOS oscillator specifications for MII mode and RMII mode are provided in the datasheet for DP83848K.

Use a 25-MHz, parallel, 20-pF load crystal resonator if a crystal source is desired. The specifications for 25-MHz crystal is listed in Table 2 (taken from the datasheet for DP83848K).

Table 2. 25-MHz Crystal Specification

PARAMETER	MIN	TYP	MAX	UNITS	CONDITION
Frequency		25		MHz	
Frequency Tolerance			±50	ppm	Operational temperature
Frequency Stability			±50	ppm	1-year aging
Load Capacitance	25		40	pF	

Figure 6 shows the connection of a crystal resonator circuit with the DP83848K. The oscillator circuit is designed to drive a parallel resonance AT cut crystal with a minimum drive level of 100 µW and a maximum of 500 µW. In case a crystal is specified for a lower drive level, place a current limiting resistor in series between X2 and the crystal. This design uses load capacitors equal to 33 pF and series resistors equal to 0 Ω.

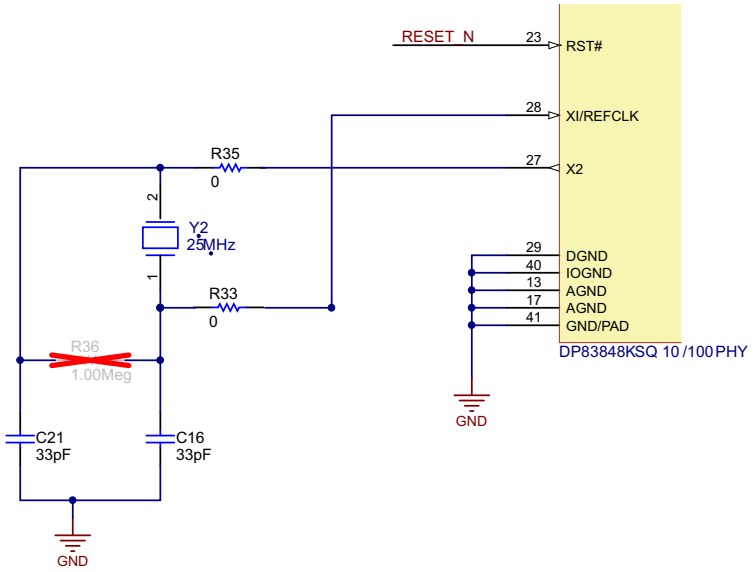


Figure 6. Crystal Oscillator Circuit for DP83848K

5.2 Twisted Pair Interface (TPI) Network Circuit

This reference design uses a shielded RJ-45 connector without internal isolation transformer. RJ-45 is the standard cable used for all the Ethernet and LAN applications. The standard color coding and signals for RJ-45 connector is shown in Figure 7.

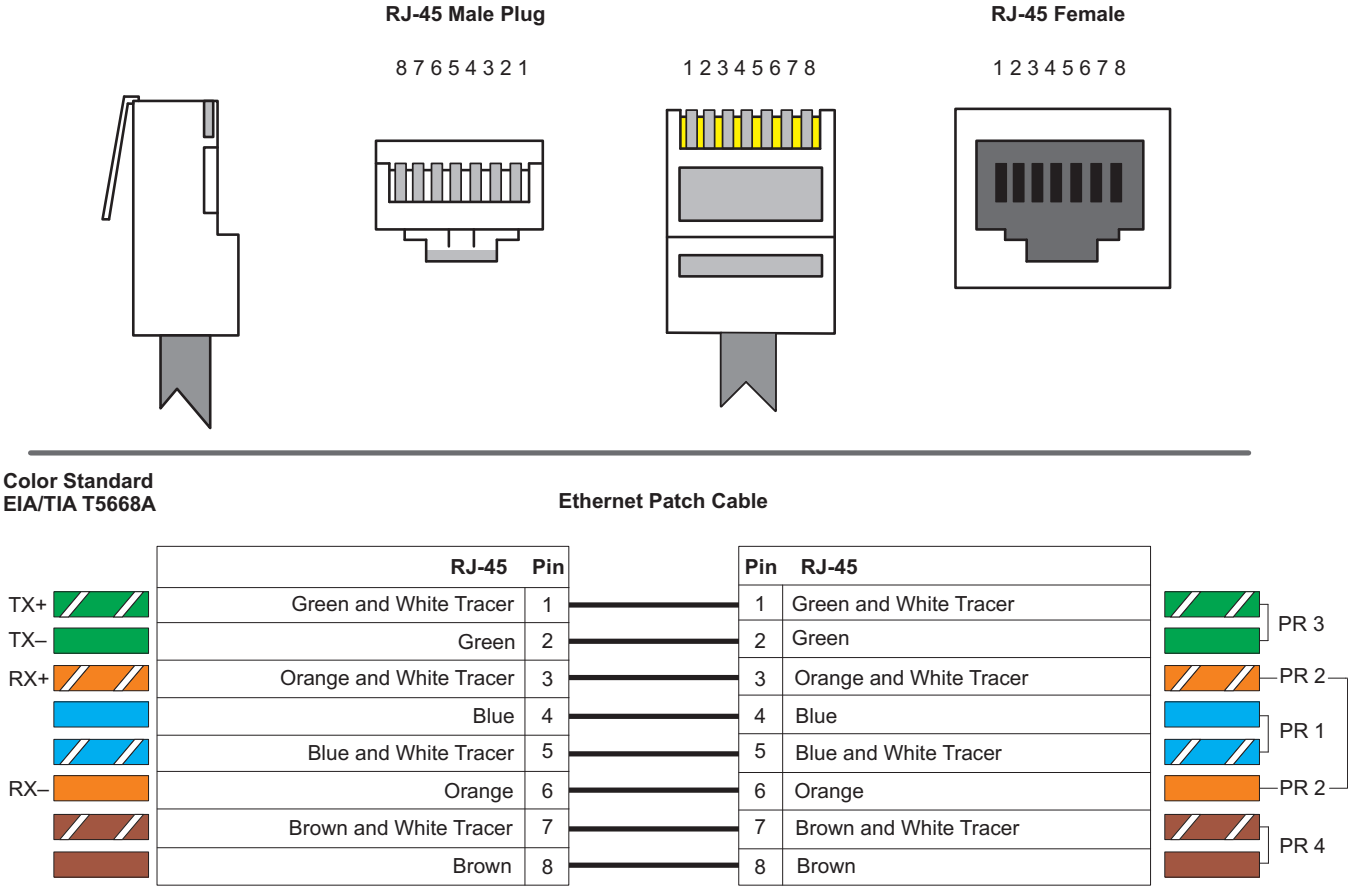


Figure 7. RJ-45 Cable Details

An external isolation transformer is interfaced. The design uses HX1198FNL from Pulse Electronics, a 1:1 transformer with an isolation of 1.5 kV_{RMS} (for 60 seconds). Based on the application, it may be necessary to connect a common-mode choke along with the isolation transformer. HX1198FNL already has an integrated common-mode transformer. Figure 8 shows the internal schematic of HX1198FNL.

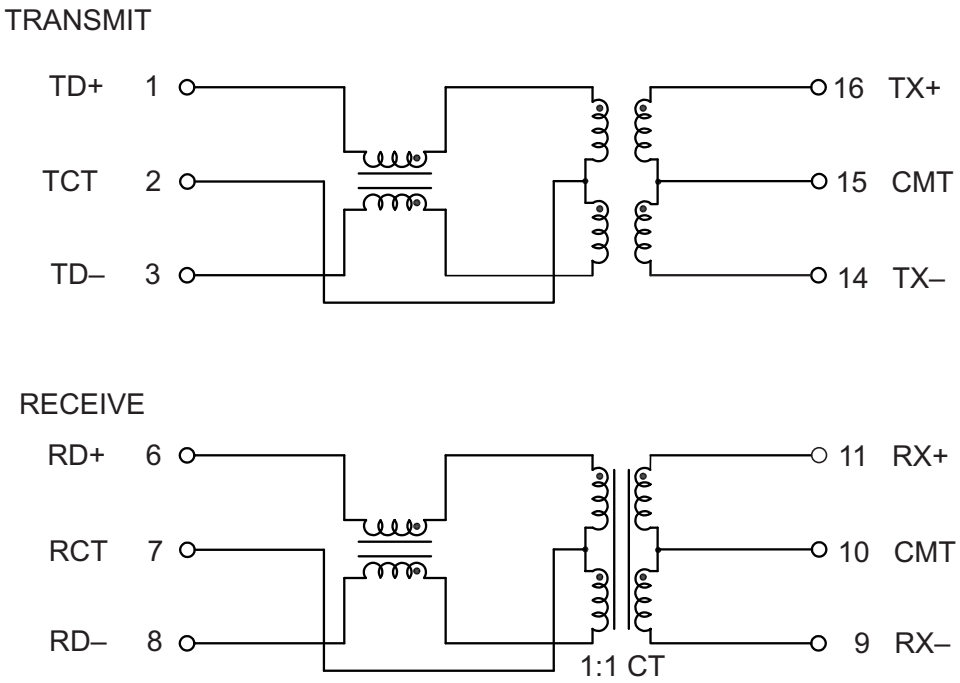


Figure 8. Internal Schematic of HX1198FNL

External 10BASE-T filters are not required when using the DP83848K, as the required signal conditioning is integrated into the device. Only isolation transformers and impedance matching resistors are required for the 10BASE-T transmit and receive interface. The internal transmit filtering ensures that all the harmonics in the transmit signal are attenuated by at least 30 dB. The TPI for this reference design is shown in Figure 9. The DP83848K datasheet recommends that the termination resistors R43, R39, R42 and R40 (of value 49.9Ω) and capacitors C26, C31, C23 and C27 should be placed very close to the device. The capacitors connected to the transformer center-taps (C33, C34, C36, and C37) should also be placed close to the taps. To get the best performance, all the components used in the TPI network should be of ±1% tolerance.

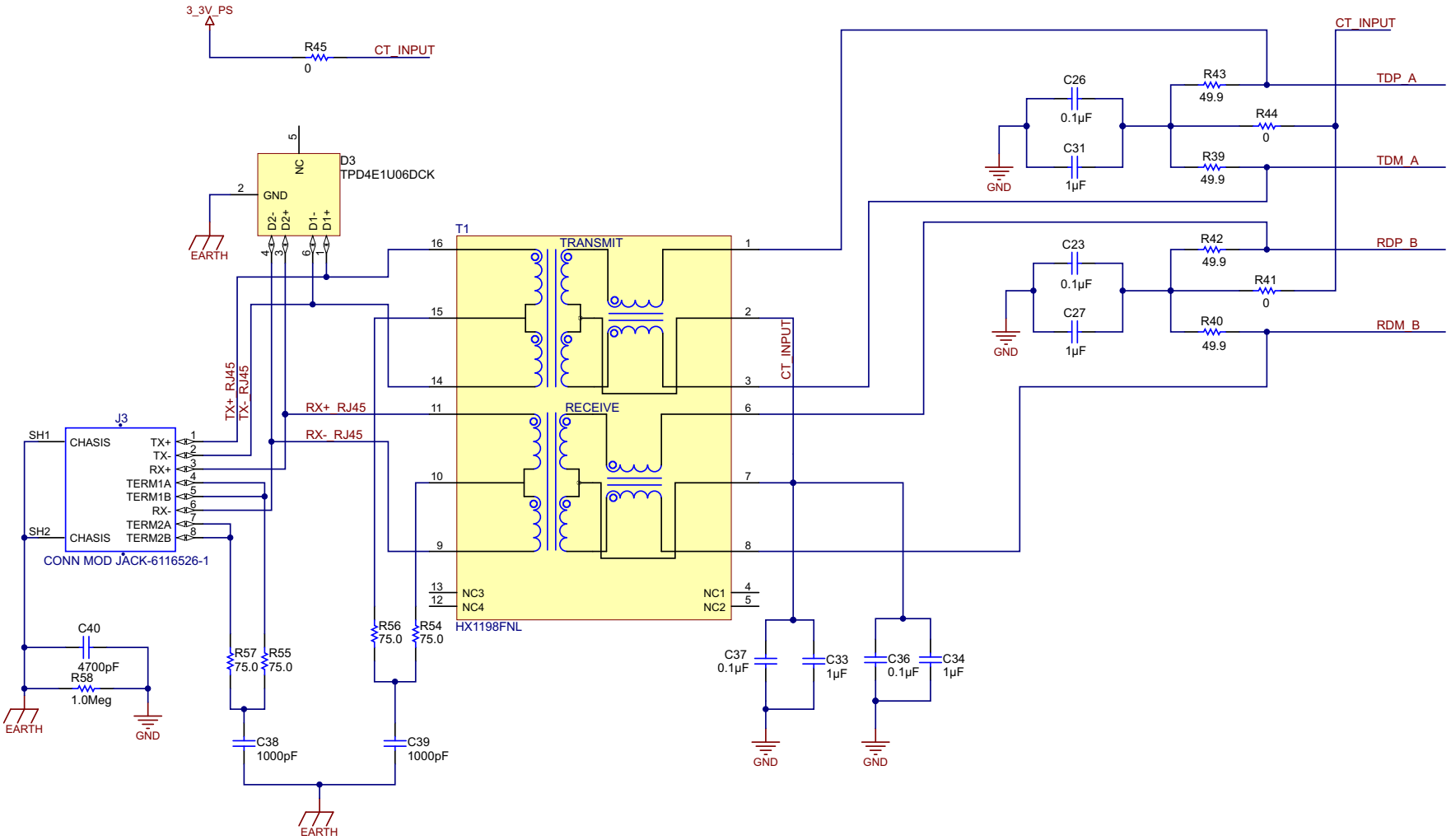


Figure 9. TPI Connection

5.3 Power Supply and Filtering

The Ethernet PHY is powered by a single 3.3-V as shown in Figure 10.

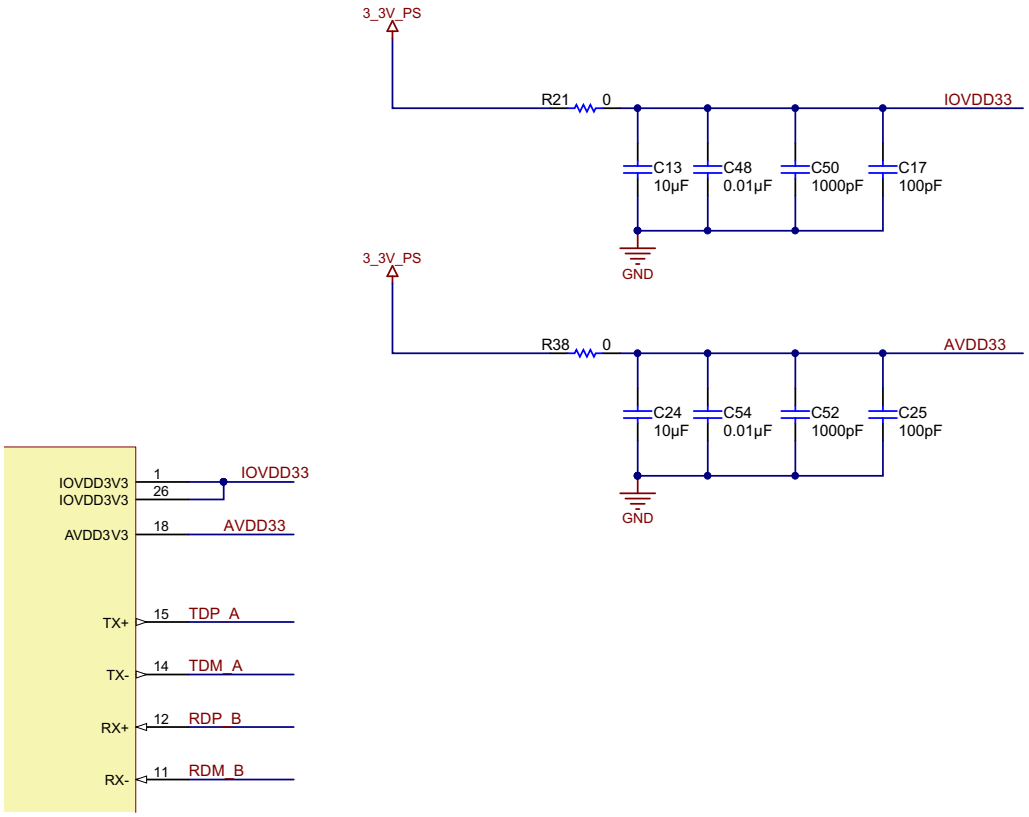


Figure 10. Power Connections for Single Supply Operation

This reference design board can be powered by any one of the following three methods:

1. By an external 5-V
2. By using 5 V from controller board on a 50-terminal MII connector as shown in Figure 11

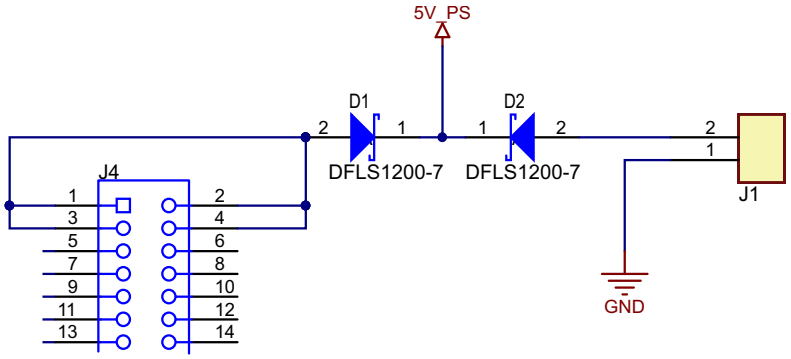


Figure 11. 5-V Input Supply Connection

3. By using 3.3 V from the controller board as shown in Figure 12

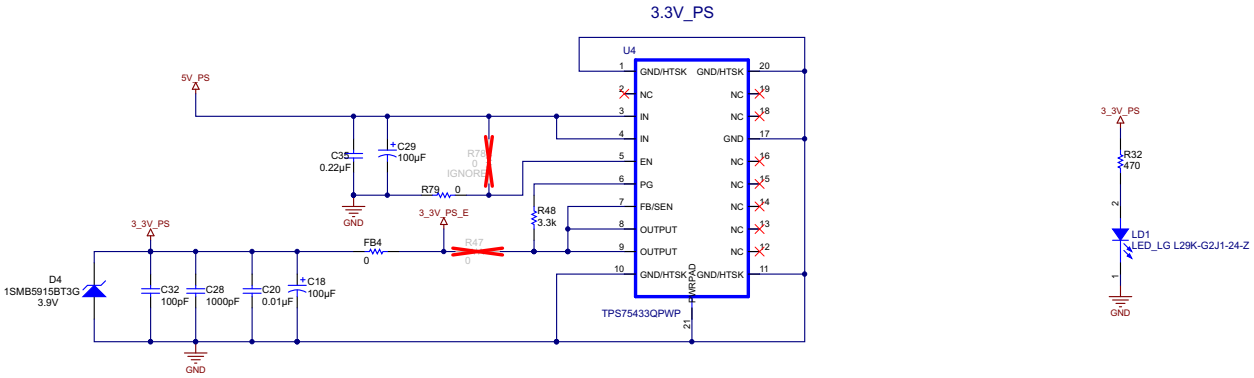


Figure 12. 3.3-V Power Supply Connection

It is important to bypass the power rails with the low-impedance surface-mount capacitors with values of 10 µF, 10 nF, 1 nF, and 100 pF. To reduce EMI, place the capacitors as close as possible to the VDD supply pins of the DP83848K. The preferred placement of these capacitors is between the supply terminals and the vias connecting to the power plane. Also, give the PCB at least one solid ground plane and one solid VDD plane to provide a low impedance power source to the component. The planes also provide a low-impedance return path for non-differential digital MII and clock signals. Place a 10-µF capacitor near the PHY device for local bulk bypassing between the VDD and the ground planes. The rise time of the VDD should be typically 500 µS.

5.4 Reset Operation of DP83848K

The DP83848K includes an internal power-on reset (POR) function and does not need to be explicitly reset for normal operation after power up. If required during normal operation, the device can be reset by a hardware or software reset.

5.4.1 Hardware Reset

A hardware reset is accomplished by applying a low pulse (TTL level), with a duration of at least 1 µs, to the RESET_N. This pulse resets the device, reinitialize all registers to default values, and re-latch the hardware configuration values into the device (similar to the power-up/reset operation). This reference design has an option to perform a hardware reset by populating R16 on the board as shown in Figure 13.

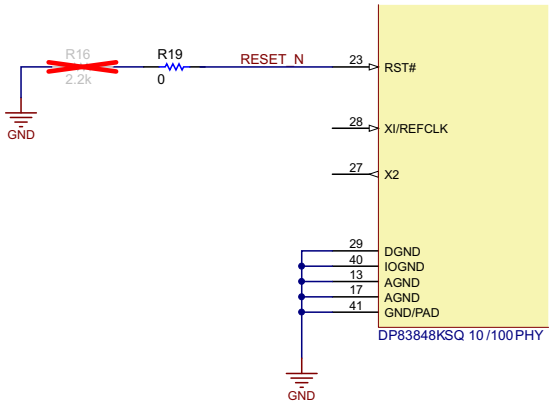


Figure 13. Hardware Reset Option

5.4.2 Software Reset

A software reset is accomplished by setting the reset bit (bit 15) of the Basic Mode Control Register (BMCR). The period from the point in time when the reset bit is set to the point in time when software reset has concluded is approximately 1 µs. This function resets the device to restore all registers to default values.

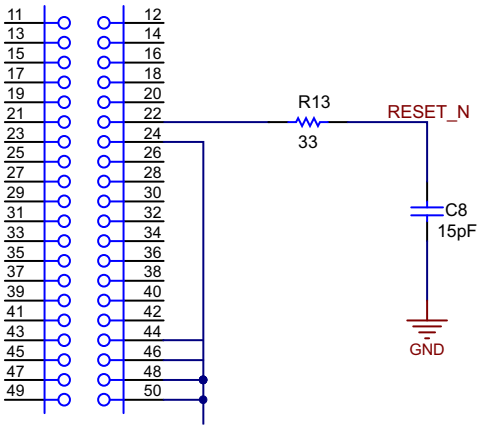


Figure 14. Software Reset Option

5.5 Power Down and Energy Detect Modes

The device can be put in a power-down mode by setting bit 11 (power down) in the BMCR, address 0x00h. When energy detect (ED) is enabled and the cable has no activity, the DP83848K remains in a low-power mode while monitoring the transmission line. Activity on the line causes the DP83848K to go through a normal power-up sequence. Regardless of cable activity, the DP83848K occasionally wakes up the transmitter to put ED pulses on the line, but otherwise draws as little power as possible. Energy detect functionality is controlled through the Energy Detect Control Register (EDCR), address 0x1Dh.

5.6 Power Feedback Circuit

The datasheet of DP83848K recommends power feedback capacitors to ensure correct operation for the device. Place parallel caps with values of 10 µF (Tantalum) and 0.1 µF close to pin 19 (PFBOUT) of the device. Pin 16 (PFBIN1) and pin 30 (PFBIN2) must be connected to pin 19 (PFBOUT); each pin requires a small capacitor (0.1 µF). See Figure 15 for proper connections.

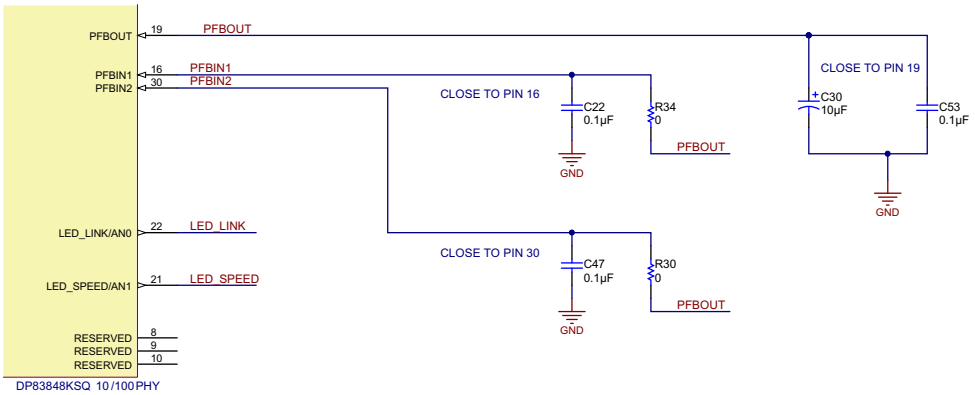


Figure 15. Power Feedback Circuit

5.7 ESD Protection

Typically, ESD precautions are predominantly in effect when handling the devices or board before being installed in a system. In those cases, implement strict handling procedures during the manufacturing process to greatly reduce the occurrences of catastrophic ESD events. After the system is assembled, internal components are less sensitive from ESD events. The ESD rating for DP83848K is 4 kV (at RZAP = 1.5 kΩ and CZAP = 120 pF). The network or Medium Dependent Interface (MDI) connection is through the transmit (TX+ and TX–) and receive (RX+ and RX–) differential pair terminals. The transmit and receive terminals connect to a termination network, then to a 1:1 magnetics (transformer), then to ESD protection devices and an RJ-46 connector. This design uses TPD4E1U06 as ESD diodes in between the RJ-45 connector and the isolation transformer as shown in Figure 16. The TPD4E1U06 is a quad-channel ultra-low cap ESD protection device. It offers a ±15-KV IEC air-gap and ±15-KV contact ESD protection compliant to IEC61000-4-2.

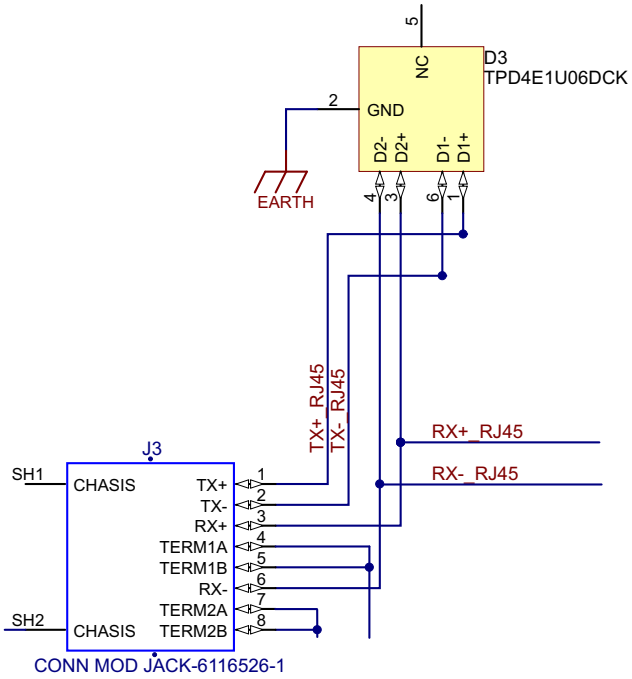


Figure 16. ESD Protection Device (TPD4E1U06DCK) Connected to MDI Connection

5.8 Controller Interface

This reference design is interfaced and tested with TM4C129XNCZAD 32-bit ARM® Cortex™-M4F MCU controller board, EK-TM4C1294XL. The drivers required to interface the DP83848K device to the MCU are available in the product folder of TIDA-00207. The controller interface is shown in Figure 17:

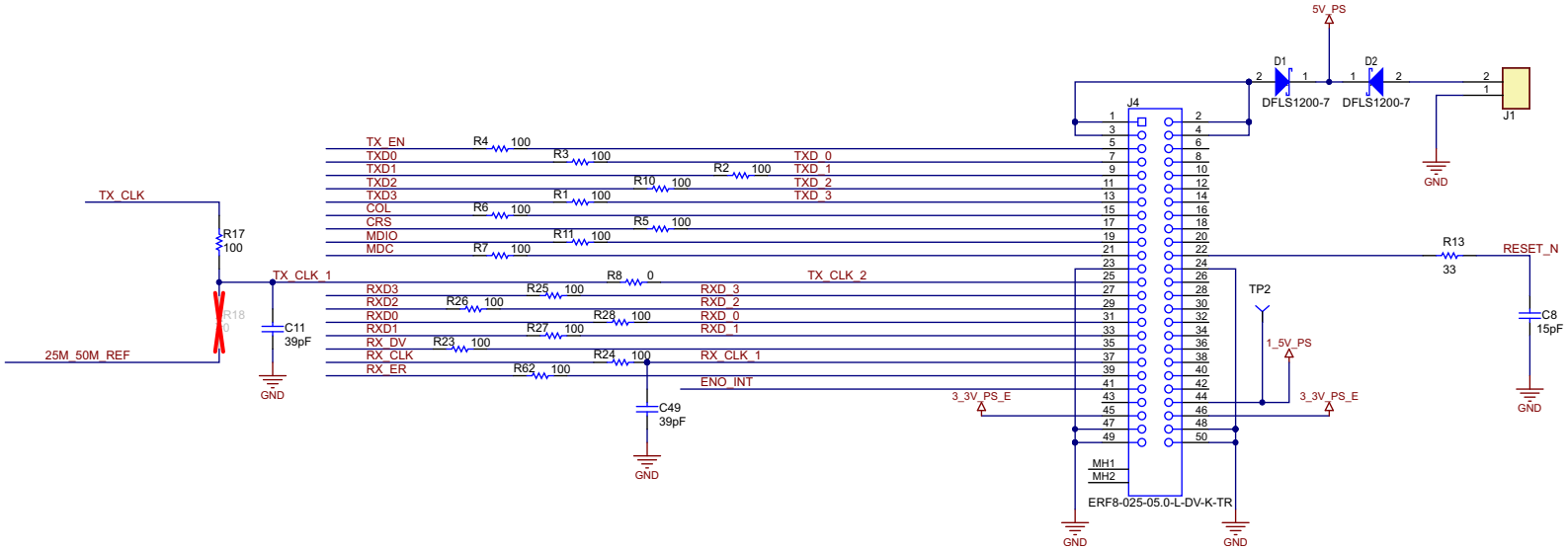


Figure 17. Controller Interface

Figure 18 shows how the Ethernet brick board will mount on the TIVA board.

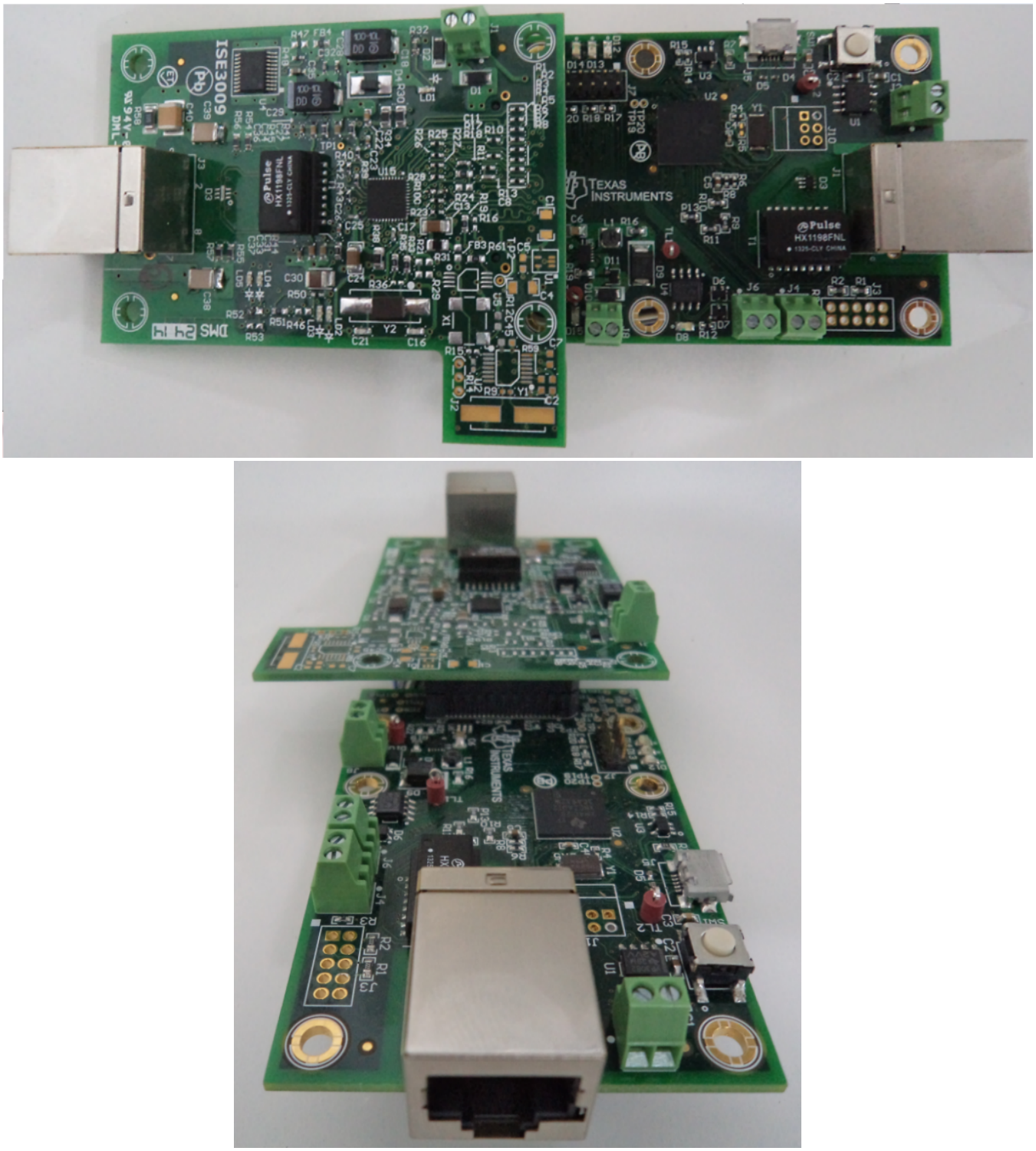


Figure 18. DP83848K Brick Mounted on TIVA Board

5.9 Strap Options

The DP83848K uses many functional pins as strap options. The values of these pins are sampled during reset and used to strap the device into specific modes of operation. The strap option pin assignments are defined in Table 3. The functional pin name is indicated in parentheses. A 2.2-kΩ resistor should be used for pull-down or pull-up to change the default strap option. If the default option is required, then there is no need for external pull-up or pull down resistors. Because these pins may have alternate functions after reset is de-asserted, the pins should not be connected directly to VCC or GND. Figure 19 shows the strap options used in this reference design.

Table 3. Strap Option Pins on DP83848K

TYPE	SIGNAL NAME	PIN #	COMPONENTS ON TIDA-00207 BOARD
PHY ADDRESS set-up	PHYAD0 (COL)	35	R63
	PHYAD1 (RXD_0)	36	R64
	PHYAD2 (RXD_1)	37	R65
	PHYAD3 (RXD_2)	38	R66
	PHYAD4 (RXD_3)	39	R67
Advertised mode selection	ANO (LED_LINK)	22	R46, R51
	AN1 (LED_SPEED)	21	R52, R53
MII mode selection	MII_MODE (RX_DV)	32	R100
LED Configuration	LED_CFG (CRS/CRS_DV)	33	R69
MDIX Enable	MDIX_EN (RX_ER)	34	R70

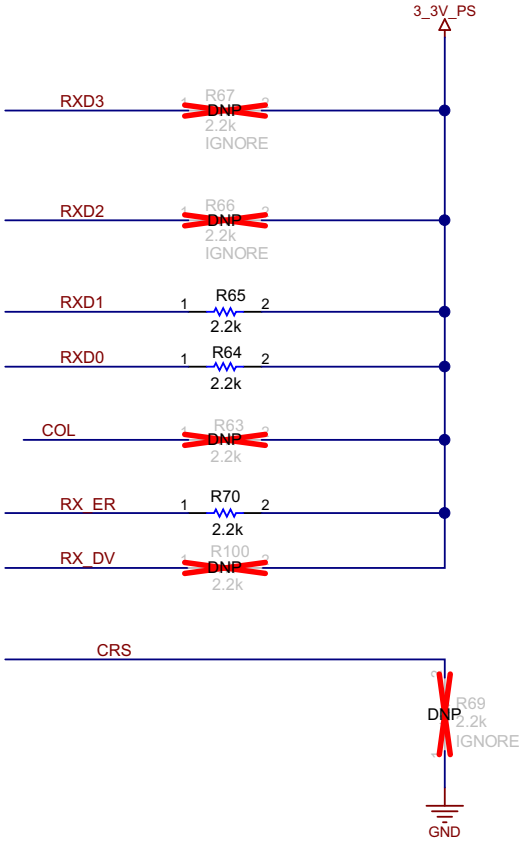


Figure 19. Strap Options in the Schematic

5.9.1 PHY Address Selection

The DP83848K provides five PHY address pins, the states of which are latched into the PHYCTRL register at system Hardware-Reset. The DP83848K supports PHY address strapping values 0 (<00000>) through 31 (<11111>). PHYAD0 pin has a weak internal pull-up resistor. PHYAD[4:1] pins have weak internal pull-down resistors. Currently, the PHY address is set-up at value of 6 (<00110>) as shown in Figure 19.

5.9.2 Advertised Mode Selection

These input pins control the advertised operating mode of the device according to the Table 4. The values on these pins are set by connecting them to GND (0) or VCC (1) through 2.2-kΩ resistors. Do not ever connect these pins directly to GND or VCC. The value set at this input is latched into the DP83848K at Hardware-Reset. The float or pull-down status of these pins is latched into the BMCR and the Auto-Negotiation Advertisement Register during Hardware-Reset. The default for DP83848K is 11 because these pins have an internal pull-up. Since these autonegotiation strap options share the LED output pins, the external components required for strapping and LED usage must be considered to avoid contention. Specifically, when the LED output is used to drive the LED directly, the active state of the output driver is dependent on the logic level sampled by the AN input upon power-up/reset. For example, if the AN input is resistively pulled low, then the corresponding output will be configured as an active high driver. Conversely, if the AN input is resistively pulled high, then the corresponding output will be configured as an active low driver. See Figure 19 for connection details.

Table 4. Advertised Mode Selection

AN1	AN0	ADVERTISED MODE
0	0	10BASE-T, Half/Full-Duplex
0	1	100BASE-TX, Half/Full-Duplex
1	0	10BASE-T, Half-Duplex 100BASE-TX, Half Duplex
1	1	10BASE-T, Half/Full-Duplex 100BASE-TX, Half/Full-Duplex

5.9.3 MII Mode Selection

MII_MODE (RX_DV) strapping option determines the operating mode of the MAC Data Interface. Default operation (no pull-up) enables the normal MII mode of operation. Strapping MII_MODE high causes the device to be in an RMII mode of operation. Since the pin includes an internal pull-down, the default value is 0. Table 5 details the configuration:

Table 5. Interface Mode Selection for DP83848K

MII_MODE	MAC INTERFACE MODE
0	MII Mode
1	RMII Mode

Figure 19 shows the same configuration.

5.9.4 LED Configuration

This strapping option determines the mode of operation of the LED pins. The default is Mode 1. Mode 1 and Mode 2 can be controlled through the strap option. All modes are configurable through register access. Refer to Section 5.10 and Table 6 for more details.

5.9.5 MDIX Enable

The default is to enable MDIX. This strapping option disables Auto-MDIX. An external pull-down will disable Auto-MDIX mode. A 2.2-kΩ resistor (R70) is connected to pull-up this pin.

5.10 LED Configuration

The DP83848K supports configurable light emitting diode (LED) pins for configuring the link and speed. The PHY Control Register (PHYCR) for the LED can also be selected through address 19h, bit [5]. See Table 6 for the LED mode selection for the DP83848K.

Table 6. LED Configuration

MODE	LED_CFG [0] (bit 5) OR (pin33)	LED_LINK	LED_SPEED
1	1	ON for Good Link OFF for No Link	ON in 100Mbps OFF in 10Mbps
2	0	ON for Good Link BLINK for Activity	ON in 100Mbps OFF in 10Mbps

The LED_LINK pin in Mode 1 indicates the link status of the port. In 100BASE-T mode, link is established due to input receive amplitude compliant with the TPPMD specifications which will result in internal generation of signal detect. A 10-Mbps link is established as a result of the reception of at least seven consecutive normal-link pulses or the reception of a valid 10BASE-T packet. This link causes LED_LINK to assert. The LED_LINK de-asserts in accordance with the link loss timer as specified in the IEEE 802.3 specification. The LED_LINK pin in Mode 1 will be off when no link is present. The LED_LINK pin in Mode 2 will be on to indicate link is good and blink to indicate activity is present on either transmit or receive activity. The LED_SPEED pin in DP83848K indicates a 10- or 100-Mbps data rate of the port. The functionality of this LED is independent of the mode selected. Because these LED pins are also used as strap options, the polarity of the LED depends on whether the pin is pulled up or down.

Since the autonegotiation strap options share the LED output pins, the external components required for strapping and LED usage must be considered to avoid contention. Specifically, when the LED output is used to drive the LED directly, the active state of the output driver is dependent on the logic level sampled by the AN input upon power-up/reset. For example, if the AN input is resistively pulled low then the corresponding output will be configured as an active high driver. Conversely, if the AN input is resistively pulled high, then the corresponding output will be configured as an active low driver.

Figure 20 below shows the connection of LED_LINK and LED_SPEED pins to external components.

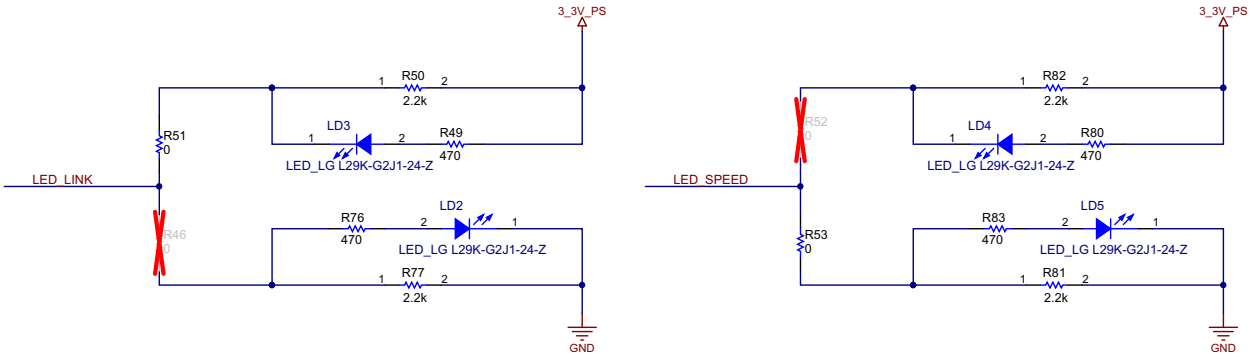


Figure 20. LED_LINK and LED_SPEED Pin Configurations

6 Software Description

Table 7. Software Configuration

FUNCTIONALITY	DESCRIPTION
Hardware Reset	A hardware reset is accomplished by applying a low pulse (TTL level), with a duration of at least 1 µs, to RESET_N. This pulse resets the device such that all registers are reinitialized to default values, and the hardware configuration values are re-latched into the device (similar to the power-up/reset operation). The time from the point when the reset terminal is de-asserted to the point when the reset has concluded internally is approximately 200 µs.
External MII PHY Initialization	Set the external PHY address. (All the read and write requests to the PHY shall use the configured external PHY address). To reset the MII PHY: 1. Set the BMCR (0x00) register bit 15 to one. 2. Set the BMCR (0x00) register to auto negotiation enable and auto negotiation restart by setting bit 12 and bit 8 to one. 3. Poll the BMSR (0x01) register bit 5 to check if auto negotiation is complete.
MII_MODE	The MII_MODE is selected by pin 32 (RX_DV). This terminal has internal weak pull down defaults to MII mode. An external pull-up makes the PHY to operate in RMII mode.
PHY ID	The PHY ID is decided by the pull-up resistors (see Section 5.9). Care must be taken that appropriate PHY ID is used for appropriate hardware bootstrap configuration (as per pull-up resistors). The values of terminals 35, 36, 37, 38, 39 (PHYAD0/COL, PHYAD1/RXD_0, PHYAD2/RXD_1, PHYAD3/RXD_2, PHYAD4/RXD_3) are latched into an internal register at hardware reset.
LED Configuration	Pin 21 and pin 22 can be used for LED configuration either as pull-up or pull-down. Pin 21 (LED_LINK) indicates a link status (fully lit) by default and activity is indicated by blinking that same LED. Pin 22 (LED_SPEED) in DP83848K indicates 10- or 100-Mbps data rate of the port (see Section 5.10).
Testing DP83848K	Assuming the hardware is connected to Ethernet cable and the other end of the Ethernet cable is connected to the PC, the TX clock and RX clock can be probed and measured (after PHY is powered up and not in reset state). Initiate a ping request with an IP address that is within the PC's subnet. (Example: 192.16.0.100 is PC IP address, 255.255.255.0 is the subnet mask) Initiate a ping command (Example: ping 192.16.0.1 –t), and TX[0:3] and RX[0:3] will show some data patterns. Ping will create traffic at every plug in of Ethernet cable. After sometime, when the destination host is unreachable message is seen, there may not be a further Ethernet message on the wire.

7 Test Setup and Test Results

7.1 Functional Test Results for DP83848K—Clock and Data

Figure 21 shows the clock signal at the crystal output. The signal has a frequency of 25 MHz.

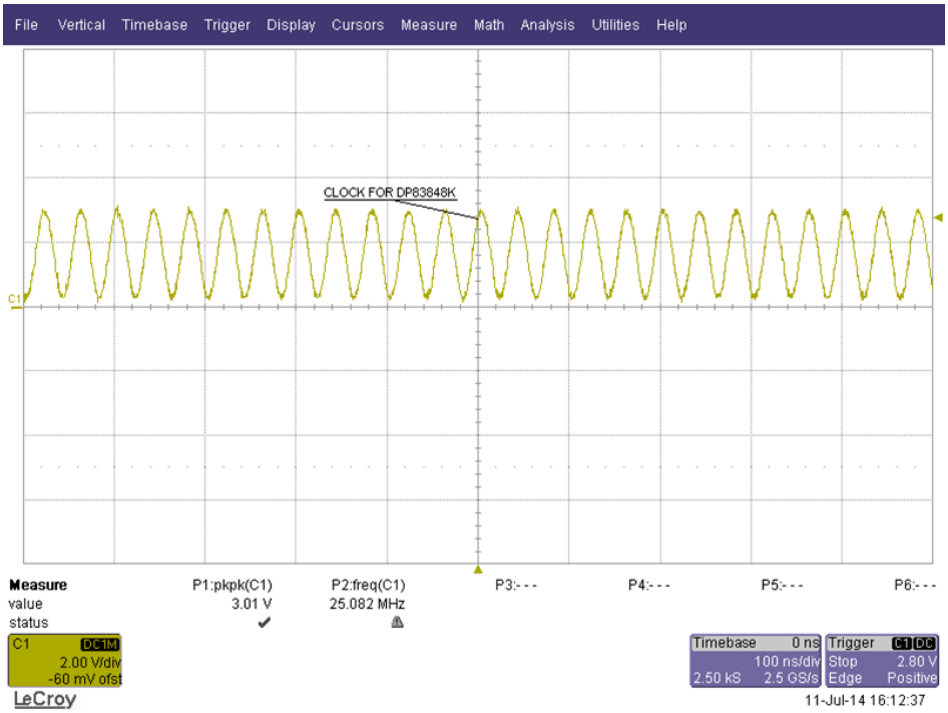


Figure 21. Clock for DP83848K

Figure 22 and Figure 23 show the data signals on TX+ and TX– lines as well as on RX+ and RX– lines. Each graph shows the differential signal.

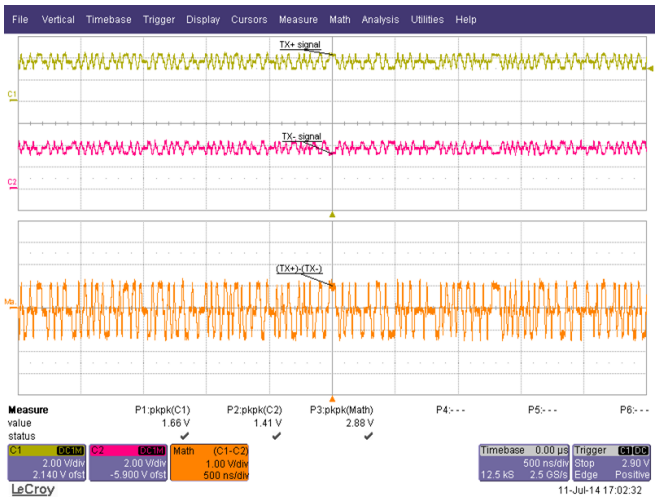


Figure 22. TX+ and TX– Signals

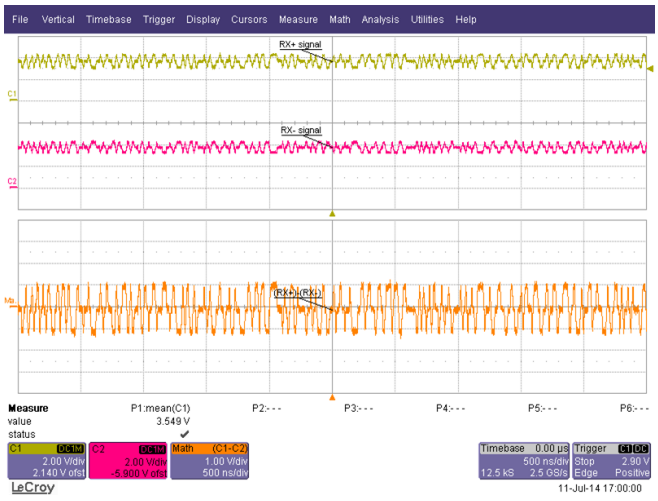


Figure 23. RX+ and RX– Signals

7.2 Power Supply to DP83848K

The power supply signal on the 3.3V_PS signal (in Figure 12) is captured along with the ripple on the same. Figure 24 and Figure 25 show the signals.

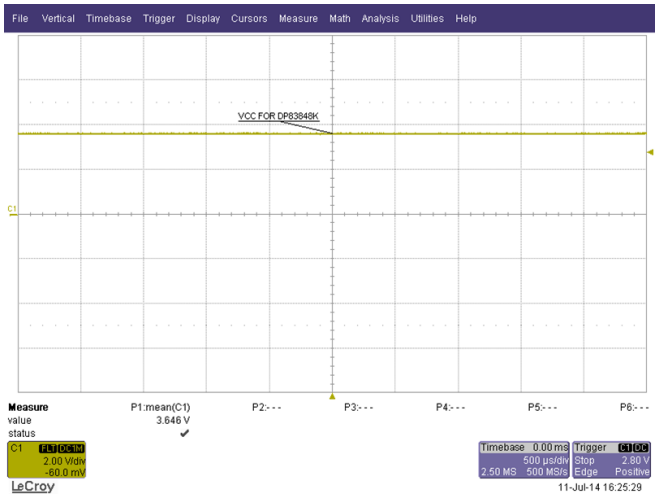


Figure 24. 3.3V_PS Signal

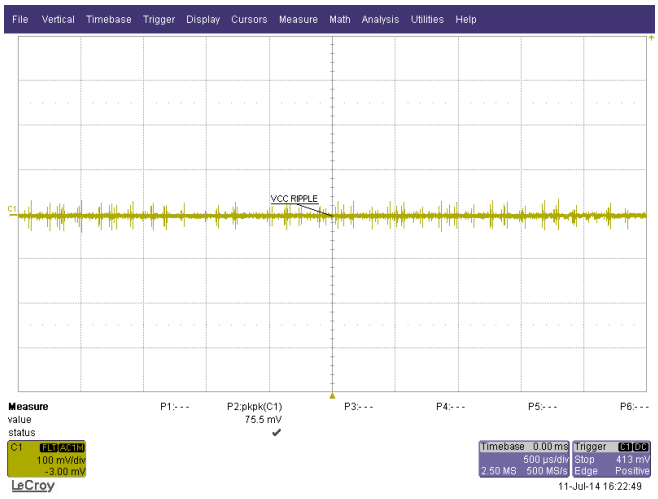


Figure 25. Ripple on 3.3V_PS

7.3 Communication Interface Testing (Computer to Device)—Ping Test

The ping test is done while both the boards connected together as shown in Figure 18. On the TIVA controller board, connector J2 is powered with 5.5 V and LEDs D8 and D15 are glowing. On the Ethernet brick board, LD1, LD3, and LD4 are glowing.

Network connection settings for ping test are:

1. Go to *Network Connections.*
2. Go to *Local Area Connection.*
3. Right click for *Properties.*
4. Select *Internet Protocol Version 4 (TCP/IPv4).*
5. Go to *Properties.*
6. Select *Use the following IP Address.*
7. Enter the IP address "192.16.0.100" and click on *Subnet Mask* (It should show "255.255.255.0").
8. Click *OK.*
9. Click *Close.*

Go to *Start*→*Run*→Type "cmd"→Type "ping 192.16.0.1" and click the *Enter* key to show four replies (Figure 26).

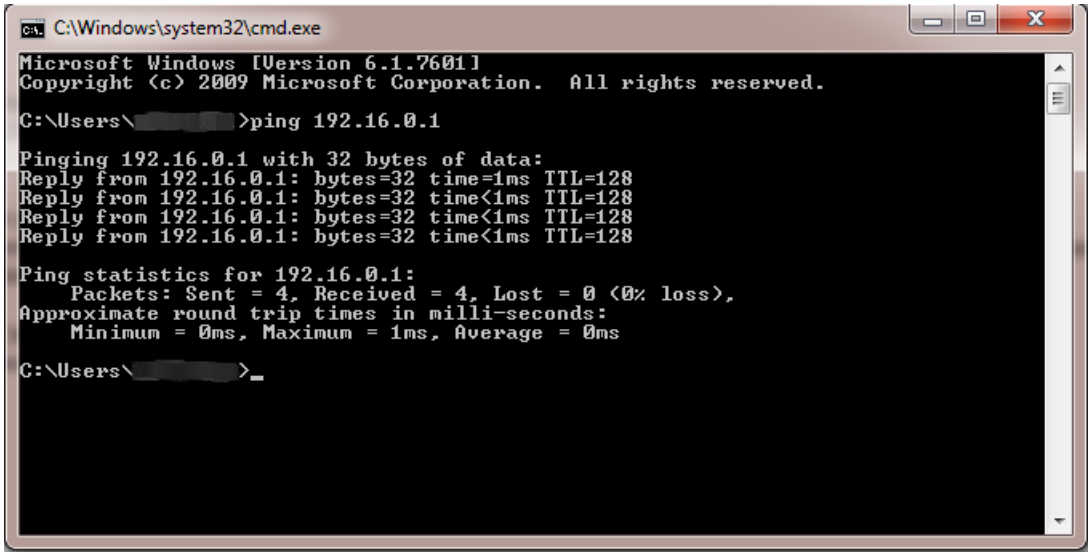


Figure 26. Ping Test

For continued replies, type “ping 192.16.0.1 –t” and click *Enter* key to show continuous replies for the ping (Figure 27).

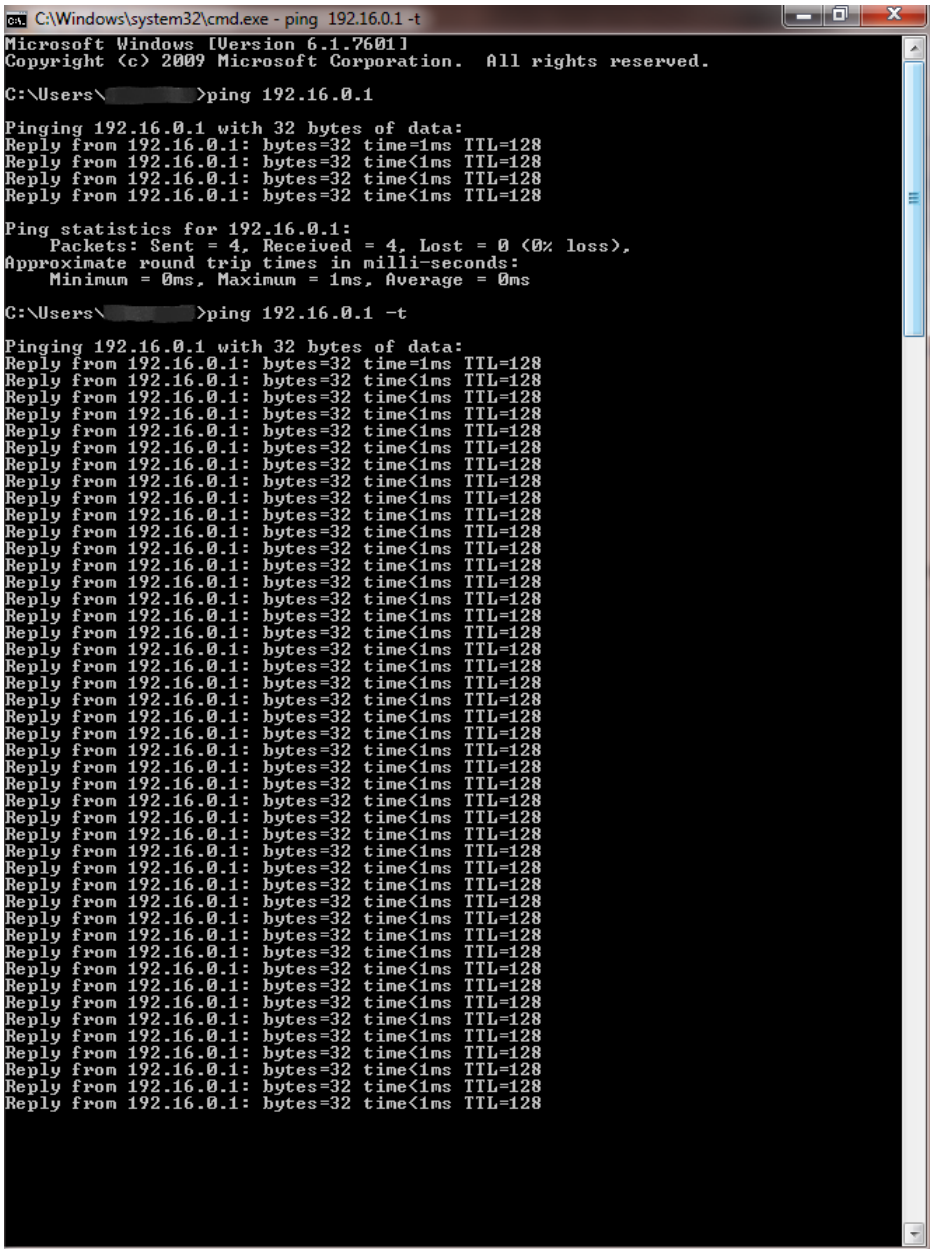


Figure 27. Ping Test (for Continuous Replies)

To stop the replies, type *CTRL+C* or close the command prompt window to stop the replies (Figure 28).

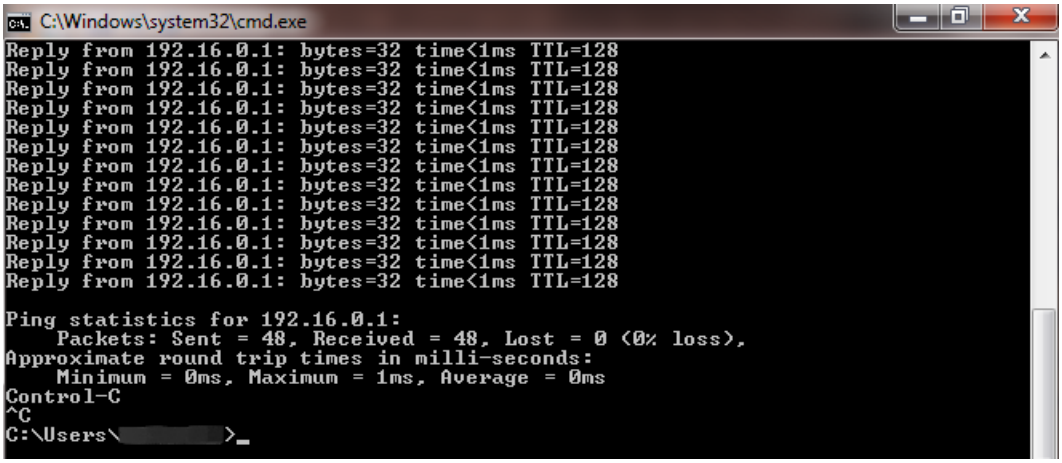


Figure 28. Ping Test Stopped

The data traffic can also be monitored using the Wireshark tool. For use this tool, open the Wireshark software, select the network *Local Area Connection*, go to the *Capture* menu, and click on *Start*. The window will show the requests and replies as shown in Figure 29.

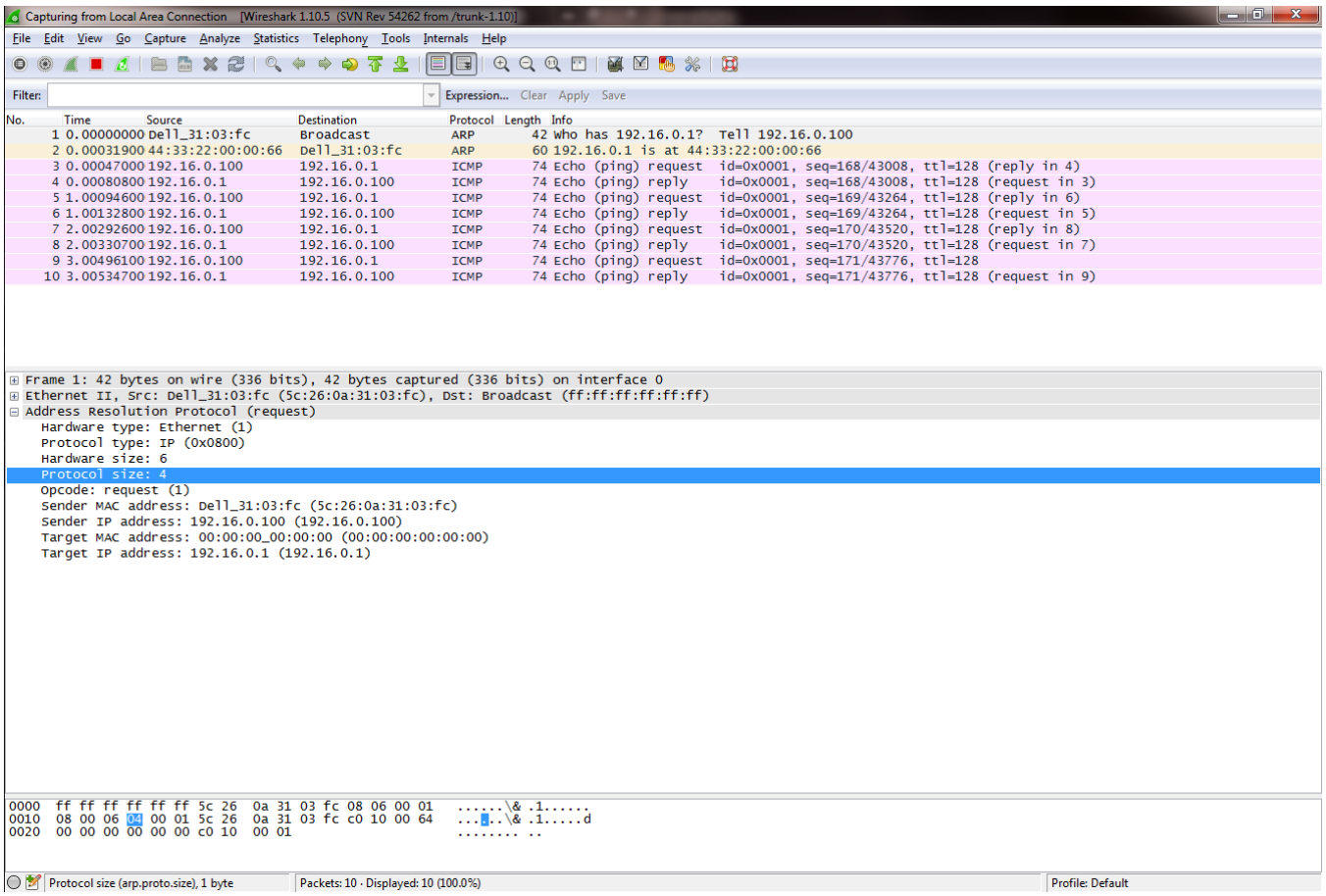


Figure 29. Wireshark Showing Data Traffic

7.4 Communication Interface Testing (Computer to Device)—Web Server Test

The web server test is done while both the boards are connected together as shown in Figure 18. On TIVA controller board, connector J2 is powered with 5.5 V and LEDs D8 and D15 are glowing. On the Ethernet brick board, LD1, LD3, and LD4 are glowing.

Settings for web server test are:

1. Go to *Internet Explorer.*
2. Go to *Tools.*
3. Click on *Internet Options* tab.
4. Go to *Connections* tab.
5. Go to *LAN Settings.*
6. Unclick *Use automatic configuration script* and click *Automatically detect settings.*
7. Click *OK* and then *OK* again.

Type the IP address "http://192.16.0.1/" in the browser and click *Enter* to show the following window (Figure 30).

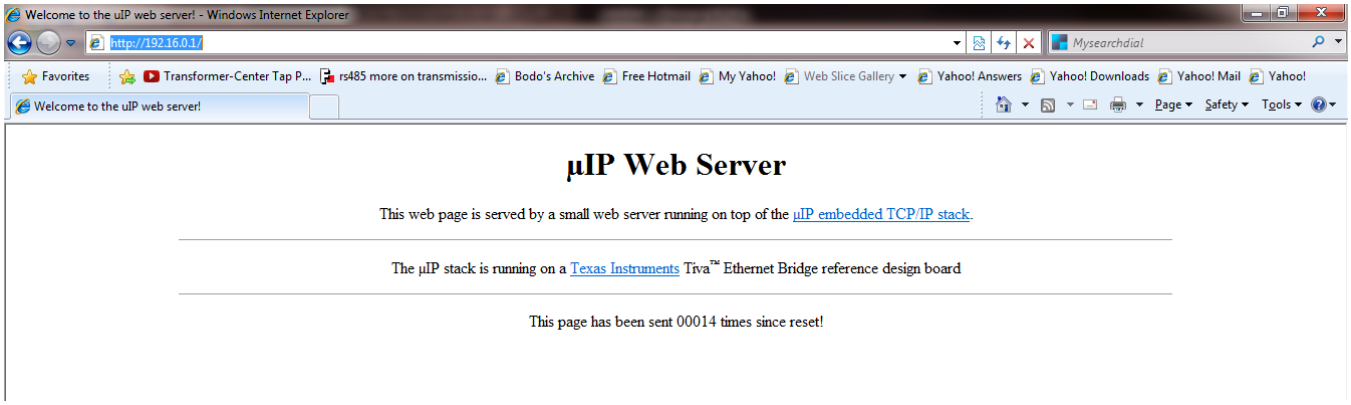


Figure 30. Web Server Test

The message "This page has been sent [number] times since reset!" will show number of times the *F5* key has been pressed on the keyboard. For example, the example window in Figure 30 shows that *F5* has been pressed 14 times.

The data traffic can also be monitored using the Wireshark tool. For use this tool, open the Wireshark software, select the network *Local Area Connection*, go to the *Capture* menu, and click on *Start*. The window will show the requests and replies as shown in Figure 31.

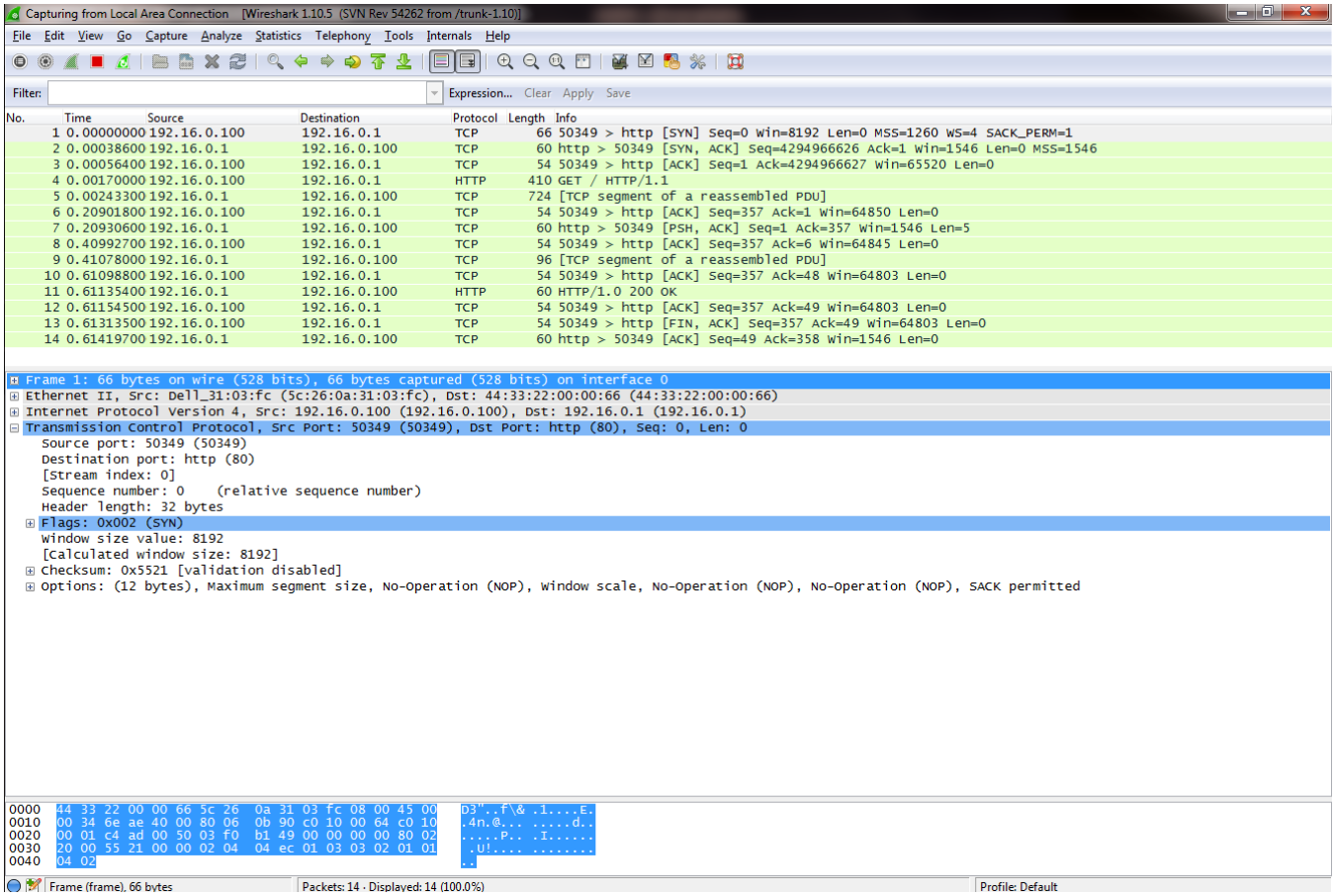


Figure 31. Data Traffic Capture for Web Server Test

7.5 EMI-Radiated Emissions

MII signals are critical to pass the radiated emission test. Therefore, proper routing of those signals with defined characteristic impedance with less vias are crucial. Series termination resistors need to be placed close to the source. Connect capacitors from the termination resistor to the ground to act as an RC filter to round off sharp edges from the MII signals. TX_CLK and RX_CLK are continuous signals, which have nearly equal emissions from their peak and quasi peak amplitudes. Therefore, those signals play a critical role in passing the RE test. The values of the termination resistor and capacitor need to be adjusted based on the test results.

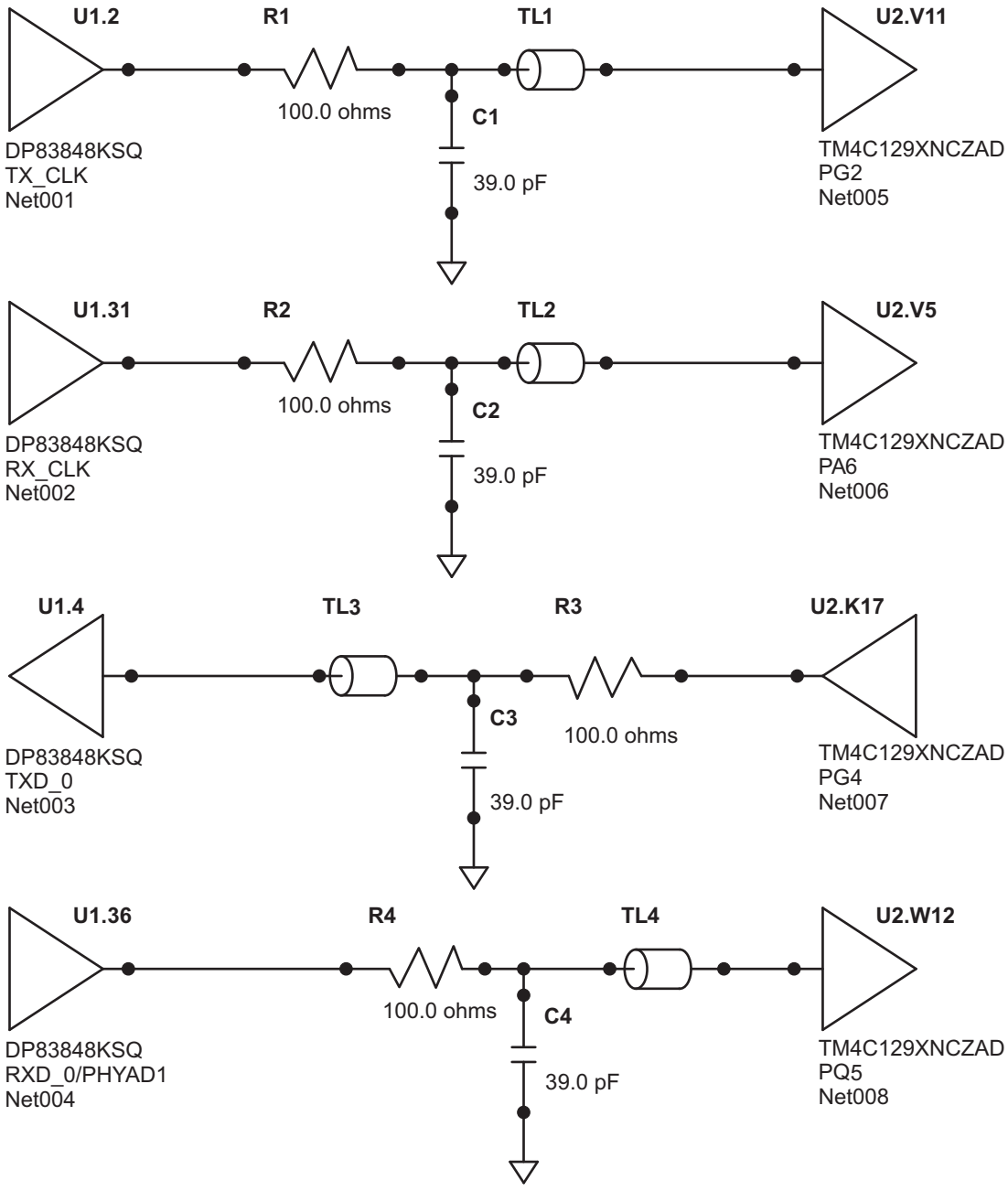


Figure 32. RC Terminations for MII Signals

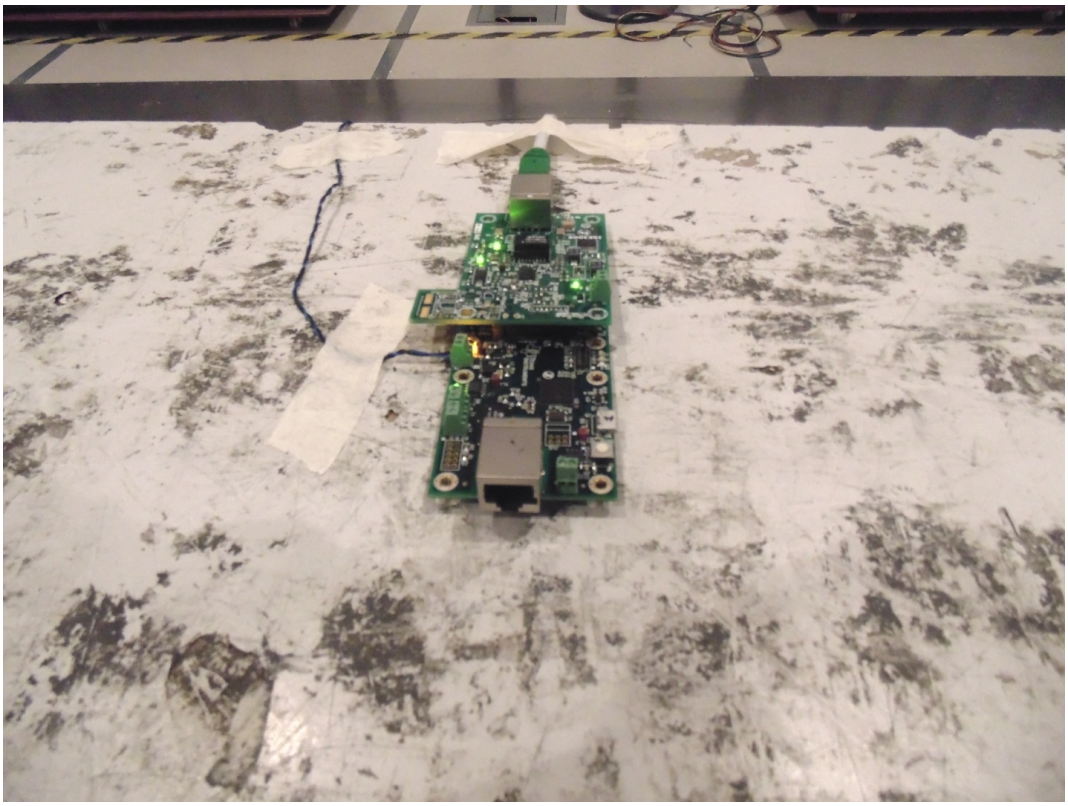


Figure 33. Ethernet PHY with Controller during RE Test

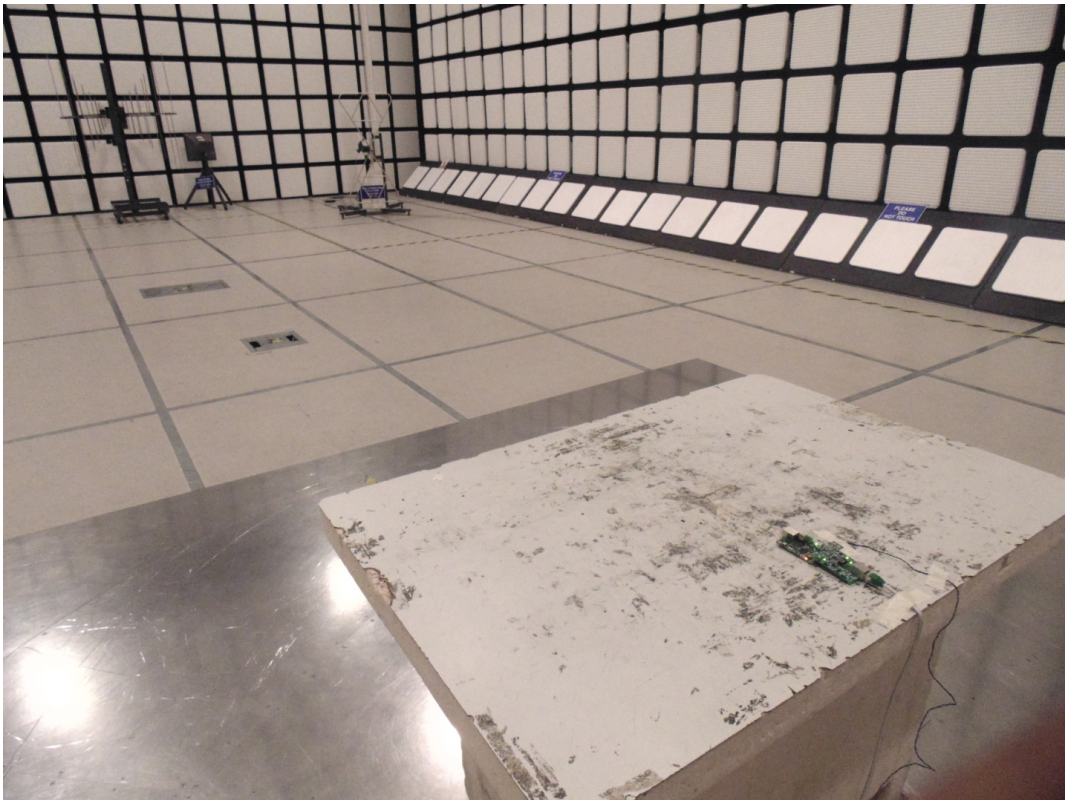


Figure 34. RE Test in 10-m Chamber

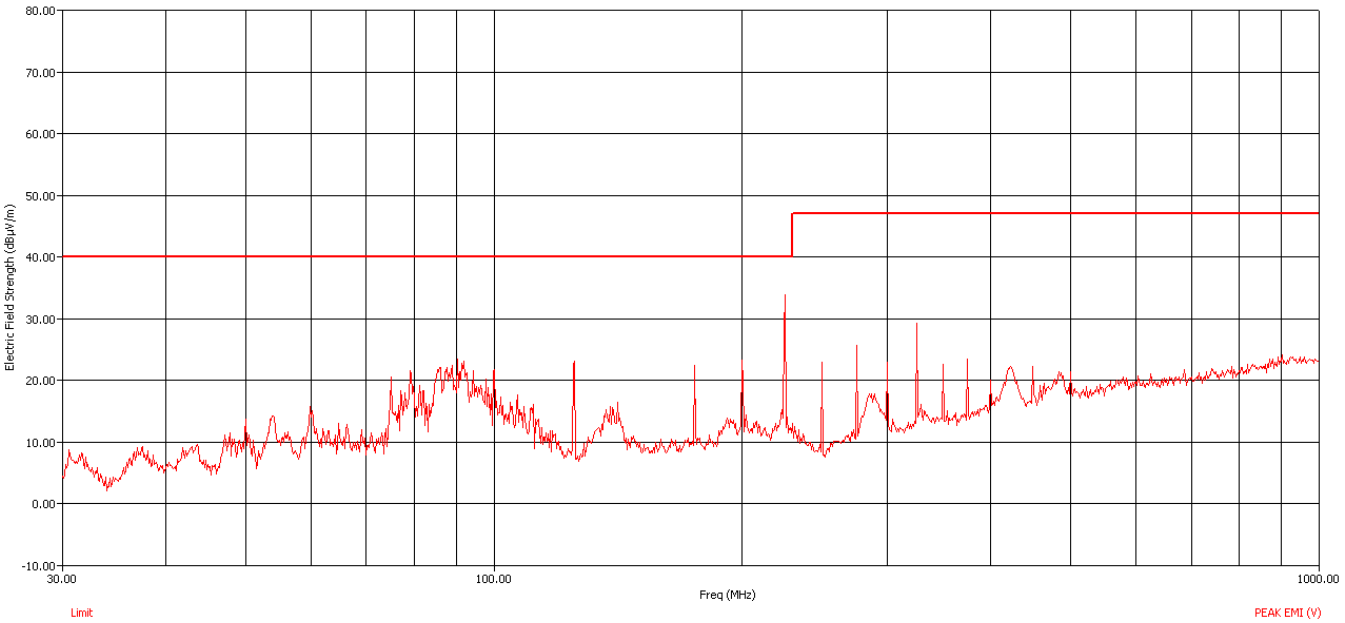


Figure 35. Peak Measurements in Vertical Polarization

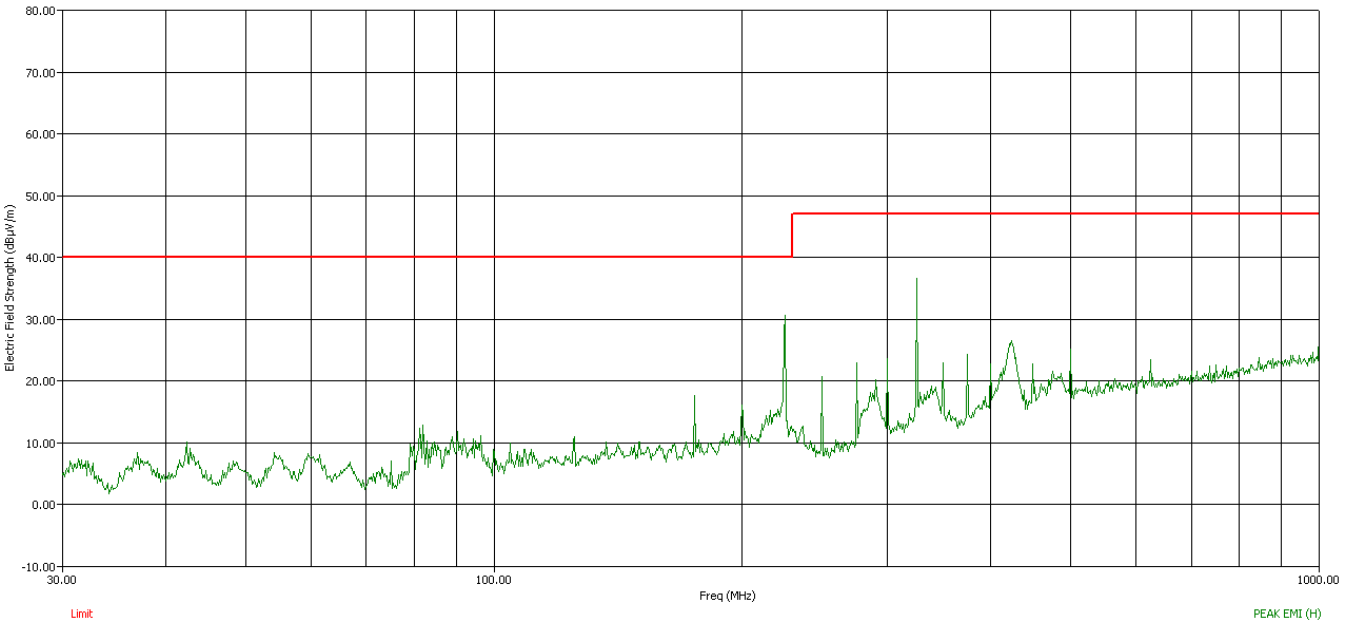


Figure 36. Peak Measurements in Horizontal Polarization

Table 8. 360° at 15° step size, 1-to-4 Meter, Quasi Peak Table

FREQ (MHz)	MAX FREQ (MHz)	POL	EUT Ttbl AGL (DEG)	TWR HT (cm)	(QP) TRACE (dBµV)	CABLE (dB)	TRANSDUCER (dB)	PREAMP (dB)	(QP) EMI (dBµv/m)	LIMIT (dBµv/m)	(QP) MARGIN (dB)
90.40	90.37	V	125.30	302.00	38.95	1.83	8.16	32.11	16.83	40.00	–23.17
125.00	124.99	V	156.30	103.00	42.18	2.15	11.00	32.07	23.26	40.00	–16.74
200.00	200.00	V	347.80	361.00	38.47	2.70	13.07	32.00	22.24	40.00	–17.16
225.00	224.99	H	144.20	388.00	48.53	2.88	11.75	31.97	31.19	40.00	–8.81
225.00	225.00	V	326.60	100.00	50.73	2.88	11.75	31.97	33.38	40.00	–6.62
325.00	324.99	H	241.30	278.00	50.69	3.45	13.96	31.90	36.19	47.00	–10.81
423.56	423.63	H	122.00	208.00	36.10	3.94	16.18	31.93	24.30	47.00	–22.70
1000.00	999.92	H	53.70	101.00	23.24	6.12	22.45	30.68	21.14	47.00	–25.86

The Ethernet PHY brick has passed the Class-A limit by a 6.6-dB margin.

7.6 ESD Test Results

The design is tested for ESD and passes IEC61000-4-2 Level 4, Criterion B.

8 Design Files

8.1 Schematics

To download the schematics, see the design files at TIDA-00207.

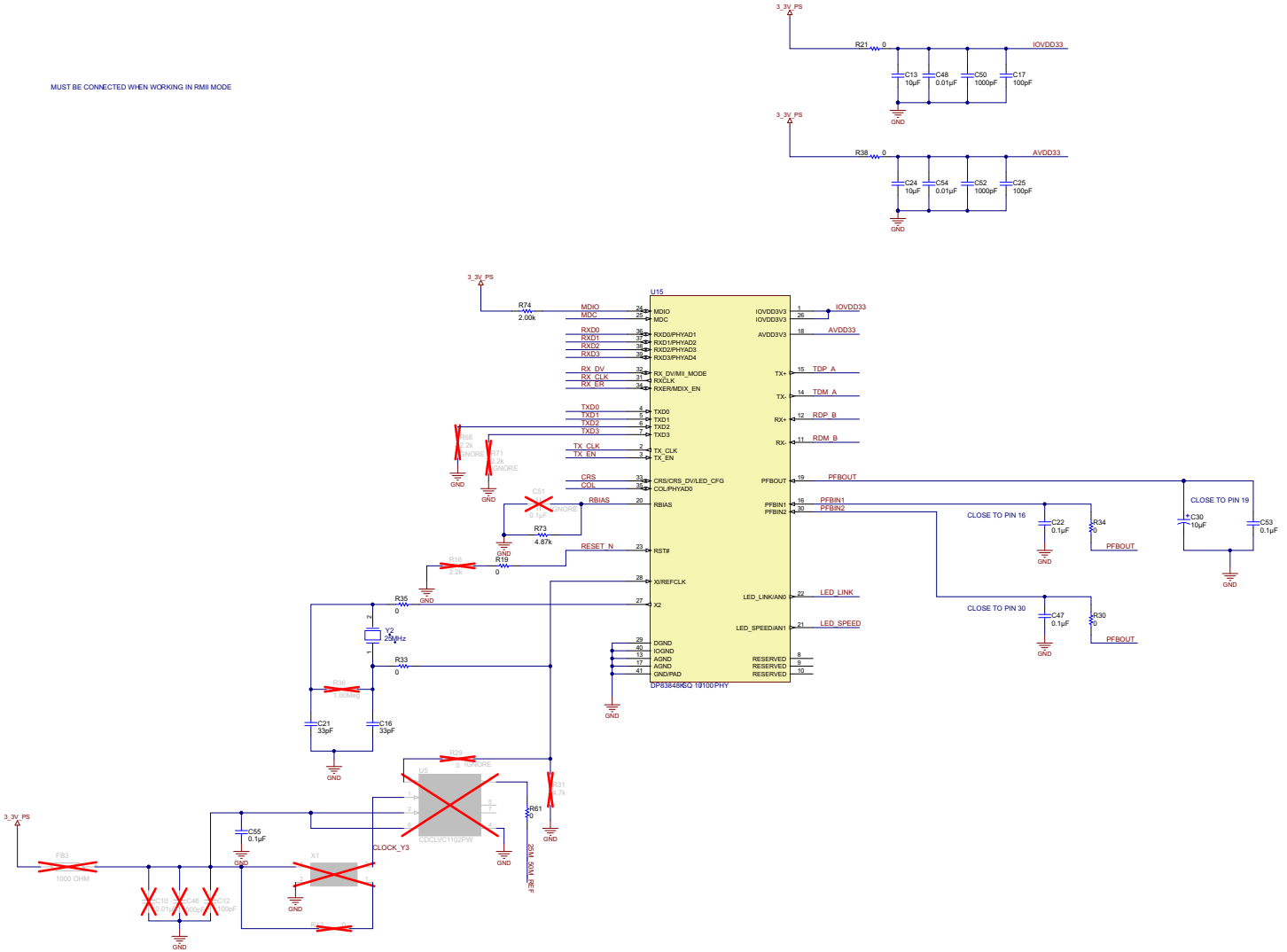


Figure 37. 10/100 Ethernet PHY Schematic

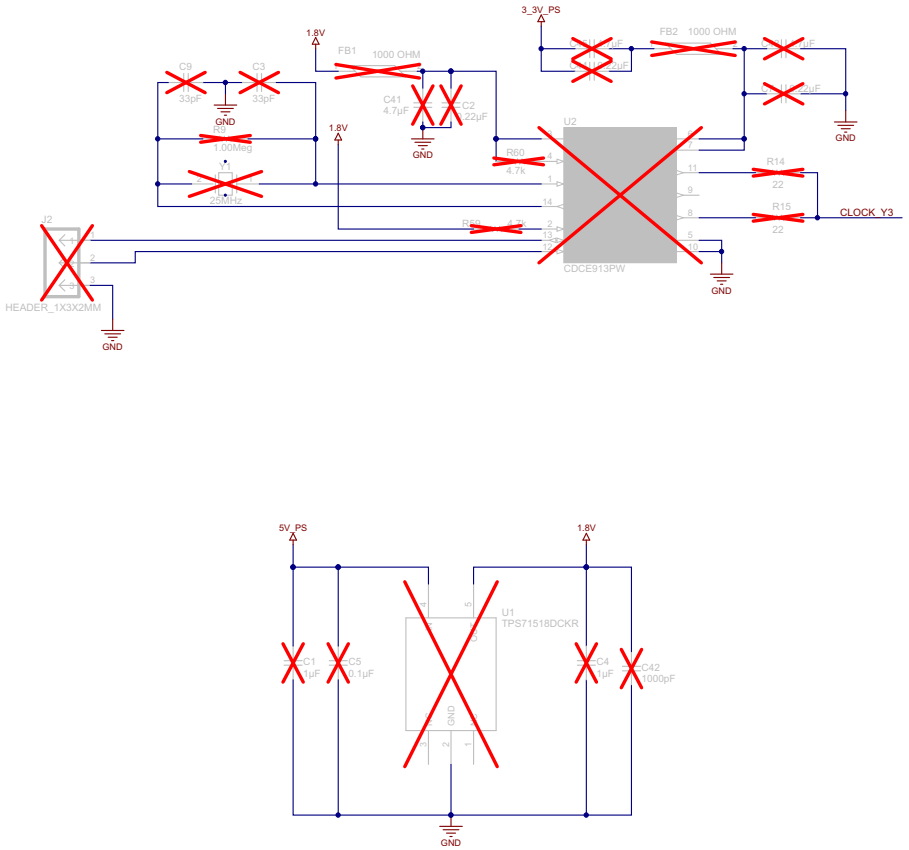


Figure 38. Clock Generator Schematic

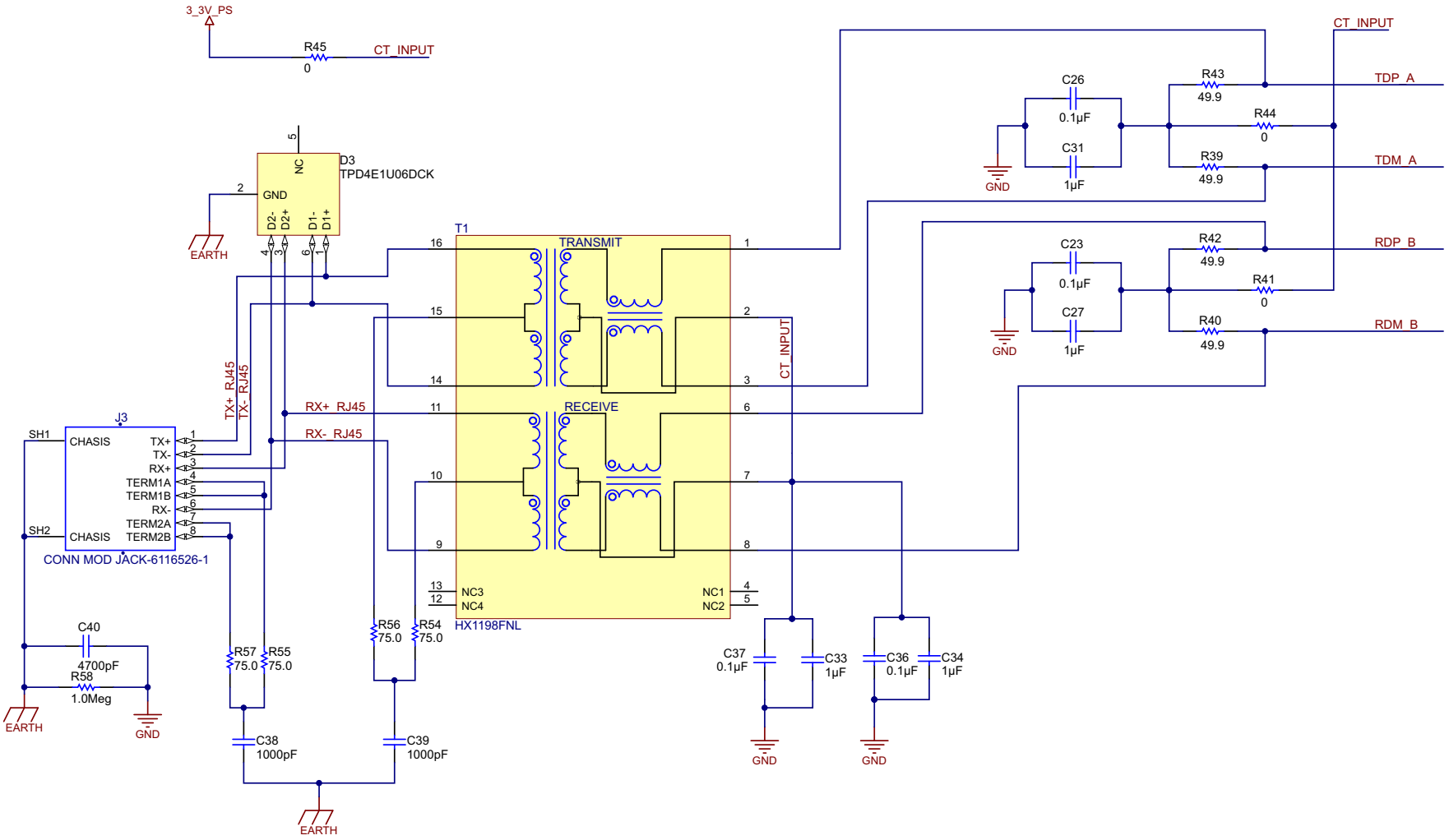


Figure 39. RJ-45 Connector Schematic

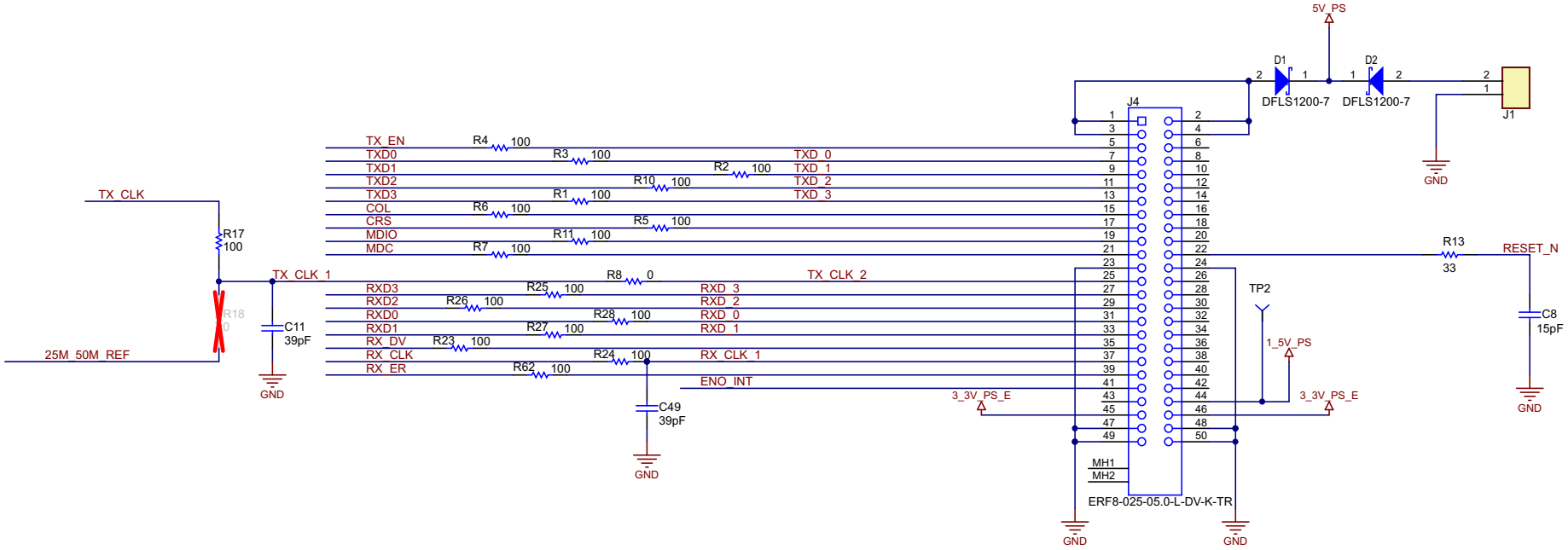


Figure 40. MII/RMII Interface Schematic

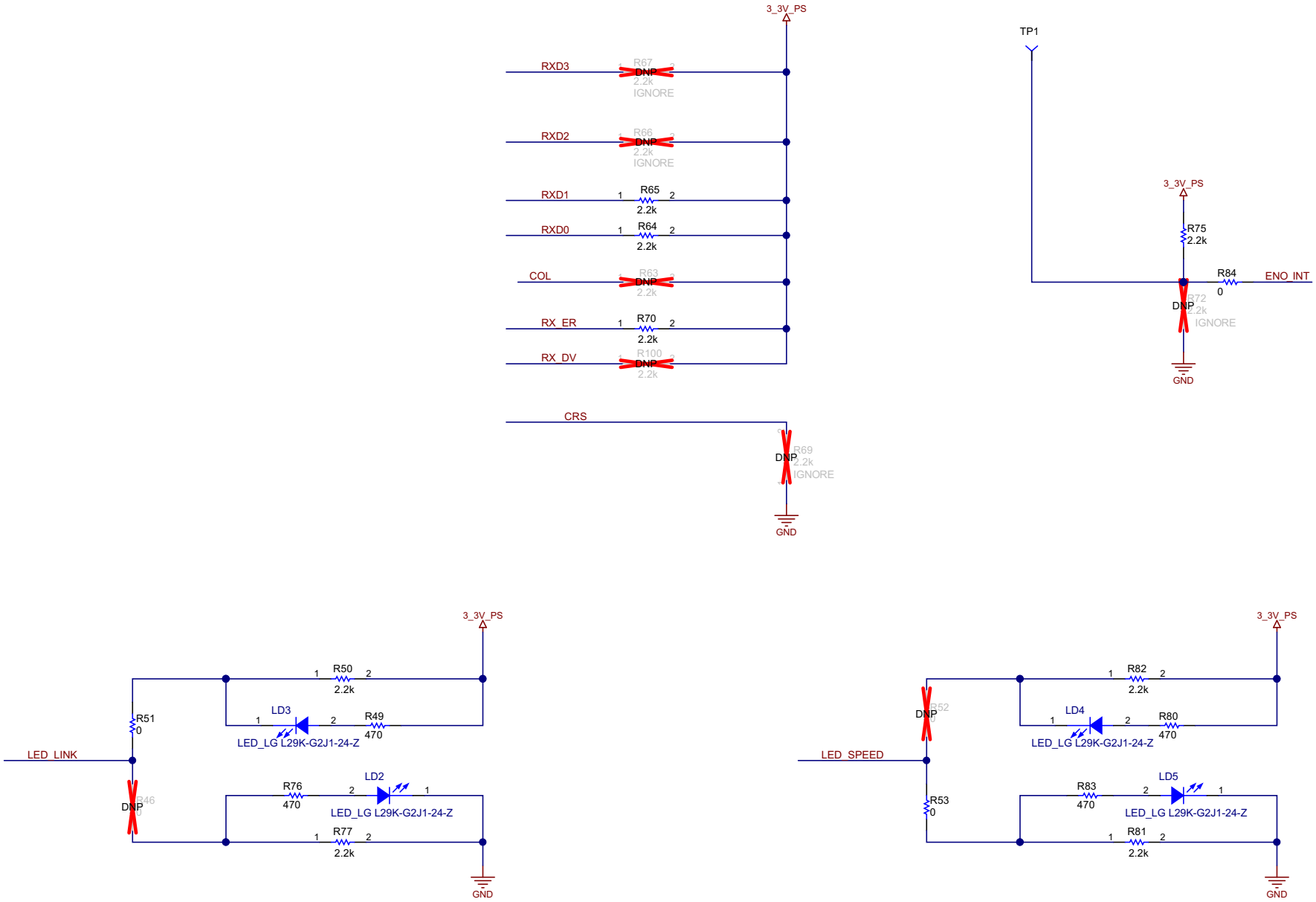


Figure 41. PHY Configuration Schematic

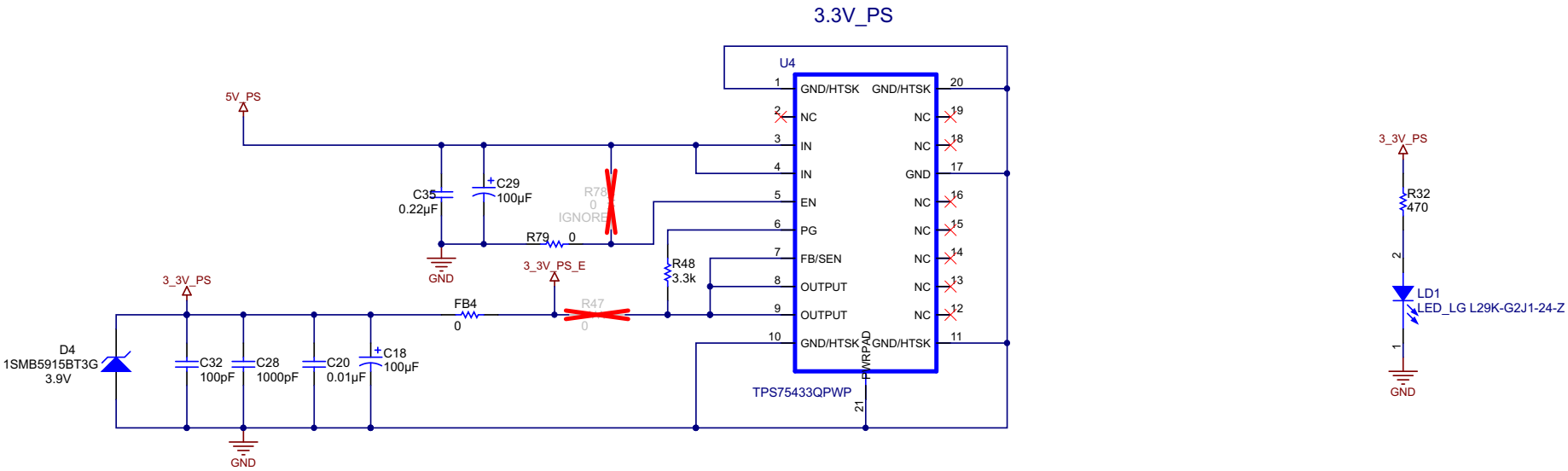


Figure 42. Power Supply Schematic

8.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00207.

Table 9. BOM

QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER	MANUFACTURER PARTNUMBER	PCB FOOTPRINT	NOTE
0	C1, C4	CAP CER 1UF 16V 10% X5R 1206	Murata Electronics	GRM31MR61C105KA0	1206	Not Fitted
0	C2, C7, C44	CAP CER 0.22UF 6.3V 10% X7R 0603	Kemet	C0603C224K9RACTU	0603	Not Fitted
0	C3, C9	CAP, CERM, 33pF, 50V, +/-5%, C0G/NP0, 0603	AVX	06035A330JAT2A	0603	Not Fitted
0	C5	CAP, CERM, 0.1uF, 16V, +80/-20%, Y5V, 0603	Kemet	C0603C104Z4VACTU	0603	Not Fitted
1	C8	CAP CER 15PF 50V 5% NP0 0402	TDK Corporation	C1005C0G1H150J050BA	0402	Fitted
0	C10	CAP, CERM, 0.01uF, 50V, +/-10%, C0G/NP0, 0402	MuRata	GCM155R71H103KA55D	0402	Not Fitted
2	C11, C49	CAP, CERM, 39pF, 25V, +/-5%, C0G/NP0, 0402	MuRata	GRM1555C1E390JA01D	0402	Fitted
0	C12	CAP, CERM, 100pF, 50V, +/-10%, X7R, 0402	Yageo America	CC0402KRX7R9BB101	0402	Not Fitted
2	C13, C24	CAP, CERM, 10uF, 35V, +/-10%, X7R, 1206	Taiyo Yuden	GMK316AB7106KL	1206	Fitted
2	C16, C21	CAP, CERM, 33pF, 50V, +/-5%, C0G/NP0, 0603	AVX	06035A330JAT2A	0603	Fitted
3	C17, C25, C32	CAP, CERM, 100pF, 50V, +/-10%, X7R, 0402	Yageo America	CC0402KRX7R9BB101	0402	Fitted
2	C18, C29	CAP, TA, 100uF, 10V, +/-20%, 0.6 ohm, SMD	Vishay-Sprague	293D107X0010D2TE3	7343-31	Fitted
3	C20, C48, C54	CAP, CERM, 0.01uF, 50V, +/-10%, C0G/NP0, 0402	MuRata	GCM155R71H103KA55D	0402	Fitted
4	C22, C47, C53, C55	CAP, CERM, 0.1uF, 16V, +/-10%, X7R, 0603	Kemet	C0603C104K4RACTU	0603	Fitted
4	C23, C26, C36, C37	CAP, CERM, 0.1uF, 10V, +/-10%, X5R, 0402	TDK	C1005X5R1A104K	0402	Fitted
4	C27, C31, C33, C34	CAP, CERM, 1uF, 6.3V, +/-10%, X5R, 0603	MuRata	GRM185R60J105KE26D	0603	Fitted
3	C28, C50, C52	CAP, CERM, 1000pF, 25V, +/-10%, X5R, 0402	MuRata	GRM155R61E102KA01D	0402	Fitted
1	C30	CAP, TA, 10uF, 16V, +/-10%, 2 ohm, SMD	Vishay-Sprague	293D106X9016B2TE3	3528-21	Fitted
1	C35	CAP, CERM, 0.22uF, 16V, +/-10%, X7R, 0603	MuRata	GRM188R71C224KA01D	0603	Fitted
2	C38, C39	CAP, CERM, 1000pF, 2000V, +/-10%, X7R, 1812	AVX	1812GC102KA1	1812	Fitted

Table 9. BOM (continued)

QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER	MANUFACTURER PARTNUMBER	PCB FOOTPRINT	NOTE
1	C40	CAP, CERM, 4700pF, 2000V, +/-10%, X7R, 1812	AVX	1812GC472KA1	1812	Fitted
0	C41, C43, C45	CAP, CERM, 4.7uF, 6.3V, +/-10%, X5R, 0603	Kemet	C0603C475K9PACTU	0603	Not Fitted
0	C42, C46	CAP, CERM, 1000pF, 25V, +/-10%, X5R, 0402	MuRata	GRM155R61E102KA01D	0402	Not Fitted
0	C51	CAP, CERM, 0.1uF, 16V, +/-10%, X7R, 0603	Kemet	C0603C104K4RACTU	0603	Not Fitted
2	D1, D2	Diode, Schottky, 200V, 1A, PowerDI123	Diodes Inc.	DFLS1200-7	powerDI123	Fitted
1	D3	Quad Channel High Speed ESD Protection Device, DCK0006A	Texas Instruments	TPD4E1U06DCK	DCK0006A_N	Fitted
1	D4	Diode, Zener, 3.9V, 550mW, SMB	ON Semiconductor	1SMB5915BT3G	SMB	Fitted
0	FB1, FB2, FB3	FERRITE CHIP 1000 OHM 300MA 0603	TDK Corporation	MMZ1608B102C	FB0603	Not Fitted
12	FB4, R19, R33, R35, R41, R44, R45, R51, R53, R61, R79, R84	RES, 0 ohm, 5%, 0.1W, 0603	Vishay-Dale	CRCW06030000Z0EA	0603	Fitted
0	FID1, FID2, FID3, FID4, FID5, FID6	Fiducial mark. There is nothing to buy or mount.	N/A	N/A	Fiducial10-20, Fiducial10-20, Fiducial10-20, Fiducial10-30, Fiducial10-30, Fiducial10-30	Fitted
1	J1	CONN TERM BLOCK 2.54MM 2POS PCB	On Shore Technology Inc	OSTVN02A150	CN2_MTB_P100_PD80_D1.1_S5.54X6.5_STACK	Fitted
0	J2	CONN HEADER 3POS 2MM VERT T/H	3M	951103-8622-AR	HEADER_1X3X2MM	Not Fitted
1	J3	CONN MOD JACK R/A 8P8C SHIELDED	TE Connectivity	6116526-1	TE_6116526-1	Fitted
1	J4	Receptacle, 0.8mm, 25x2, SMT	Samtec	ERF8-025-05.0-L-DV-K-TR	CONN_ERF8-025-05_0-L-DV-L-TR	Fitted
0	LBL1	Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll	Brady	THT-14-423-10	Label_650x200	Not Fitted
5	LD1, LD2, LD3, LD4, LD5	LED SmartLED Green 570NM	OSRAM	LG L29K-G2J1-24-Z	LED0603AA	Fitted
4	MH1, MH2, MH3, MH4	Mountin hole, NPTH Drill 3.2mm	N/A	N/A	MH3.2_H5_W6_KO8_STAR HEAD	Fitted
16	R1, R2, R3, R4, R5, R6, R7, R10, R11, R23, R24, R25, R26, R27, R28, R62	RES, 100 ohm, 5%, 0.063W, 0402	Vishay-Dale	CRCW0402100RJNED	0402	Fitted
1	R8	RES, 0 ohm, 5%, 0.063W, 0402	Vishay-Dale	CRCW04020000Z0ED	0402	Fitted
0	R9, R36	RES, 1.00Meg ohm, 1%, 0.063W, 0402	Vishay-Dale	CRCW04021M00FKED	0402	Not Fitted
0	R12, R18, R29, R46, R47, R52, R78	RES, 0 ohm, 5%, 0.1W, 0603	Vishay-Dale	CRCW06030000Z0EA	0603	Not Fitted

Table 9. BOM (continued)

QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER	MANUFACTURER PARTNUMBER	PCB FOOTPRINT	NOTE
1	R13	RES, 33 ohm, 5%, 0.063W, 0402	Vishay-Dale	CRCW040233R0JNED	0402	Fitted
0	R14, R15	RES, 22 ohm, 5%, 0.063W, 0402	Vishay-Dale	CRCW040222R0JNED	0402	Not Fitted
0	R16, R63, R66, R67, R68, R69, R71, R72	RES, 2.2k ohm, 5%, 0.063W, 0402	Vishay-Dale	CRCW04022K20JNED	0402	Not Fitted
1	R17	RES, 100 ohm, 5%, 0.1W, 0603	Vishay-Dale	CRCW0603100RJNEA	0603	Fitted
4	R21, R30, R34, R38	RES, 0 ohm, 5%, 0.125W, 0805	Yageo America	RC0805JR-070RL	0805_HV	Fitted
0	R31, R59, R60	RES, 4.7k ohm, 5%, 0.1W, 0603	Yageo America	RC0603JR-074K7L	0603	Not Fitted
5	R32, R49, R76, R80, R83	RES, 470 ohm, 1%, 0.1W, 0603	Yageo America	RC0603FR-07470RL	0603	Fitted
4	R39, R40, R42, R43	RES, 49.9 ohm, 1%, 0.063W, 0402	Vishay-Dale	CRCW040249R9FKED	0402	Fitted
1	R48	RES, 3.3k ohm, 5%, 0.063W, 0402	Vishay-Dale	CRCW04023K30JNED	0402	Fitted
1	R100	RES, 2.2k ohm, 5%, 0.063W, 0402	Vishay-Dale	CRCW04022K20JNED	0402	Not Fitted
8	R50, R64, R65, R70, R75, R77, R81, R82	RES, 2.2k ohm, 5%, 0.063W, 0402	Vishay-Dale	CRCW04022K20JNED	0402	Fitted
4	R54, R55, R56, R57	RES, 75.0 ohm, 1%, 0.1W, 0603	Yageo America	RC0603FR-0775RL	0603	Fitted
1	R58	RES, 1.0Meg ohm, 5%, 0.25W, 1206	Vishay-Dale	CRCW12061M00JNEA	1206	Fitted
1	R73	RES, 4.87k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW06034K87FKEA	0603	Fitted
1	R74	RES, 2.00k ohm, 1%, 0.063W, 0402	Vishay-Dale	CRCW04022K00FKED	0402	Fitted
1	T1	TRANSFORMER, MDL, XFMR SGL ETHR LAN, SOIC-16	PULSE ELECTRONICS	HX1198FNL	XFMR_ HX1198FNL	Fitted
2	TP1, TP2	Test Point 40mil pad 20mil drill	STD	STD	TP1_PD40_D0.5_S50	Fitted
0	U1	IC REG LDO 1.8V 50MA SC70-5	TI	TPS71518DCKR	SOP_5P.65MM(DCK)	Not Fitted
0	U2	Programmable 1-PLL VCXO Clock Synthesizer With 1.8-V, 2.5-V, and 3.3-V Outputs, PW0014A	Texas Instruments	CDCE913PW	PW0014A_N	Not Fitted
1	U4	IC, Low Dropout Voltage Regulator, 3.3 V, 2.0 A	Texas Instruments	TPS75433QPWP	PWP20	Fitted
0	U5	3.3 V and 2.5 V LVCMOS High-Performance Clock Buffer Family, PW0008A	Texas Instruments	CDCLVC1102PW	PW0008A_N	Not Fitted
1	U15	TI DP83848J 10/100 PHY	Texas Instruments	DP83848KSQ/NOPB	QFN50P600X600X80-40N	Fitted
0	X1	OSC 25.00 MHZ 3.3V HIGH STAB SMD	EPSON	HG-2150CA 25.000M-BXC3	OSC_HG-2150CA	Not Fitted
0	Y1	CRYSTAL 25.0MHZ 18PF SMD	CTS-Frequency Controls	445I23D25M00000	XTAL_ATS250BSM-1E_1	Not Fitted
1	Y2	CRYSTAL 25.0MHZ 18PF SMD	CTS-Frequency Controls	445I23D25M00000	XTAL_ATS250BSM-1E_1	Fitted

8.3 PCB Layout

To download the layer plots, see the design files at TIDA-00207.

NOTE: The total dimension of the board is 75 × 50 mm.

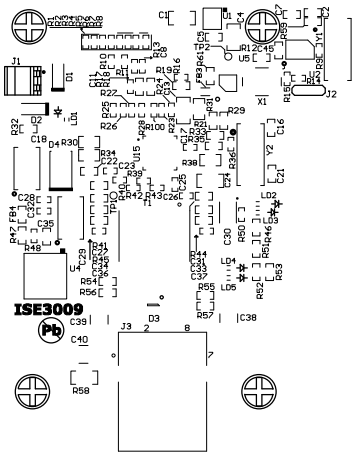


Figure 43. Top Overlay

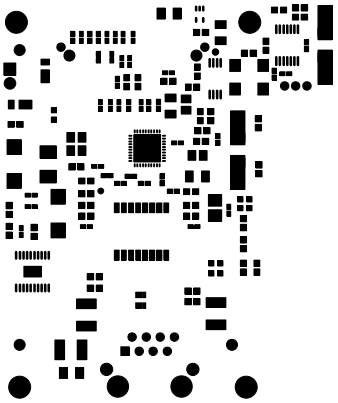


Figure 44. Top Solder Mask

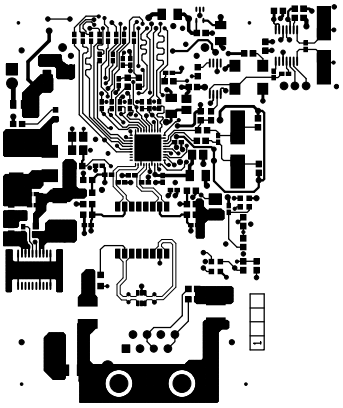


Figure 45. Top Layer

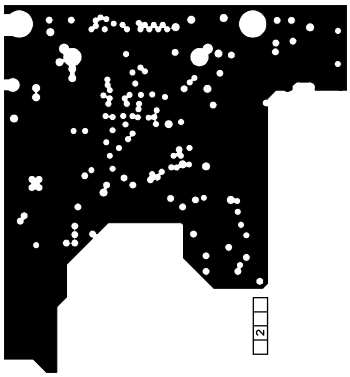


Figure 46. L2_P1

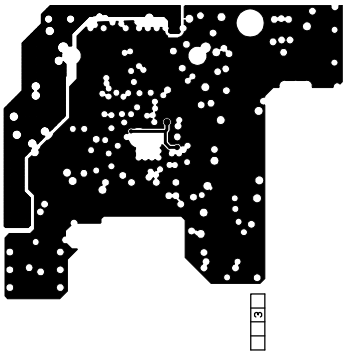


Figure 47. L3_P2

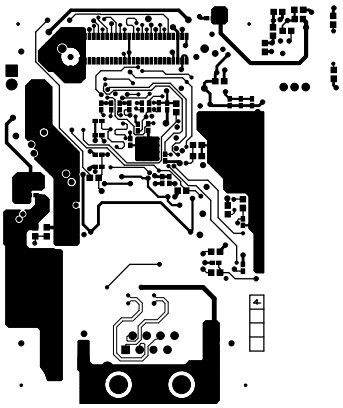


Figure 48. Bottom Layer

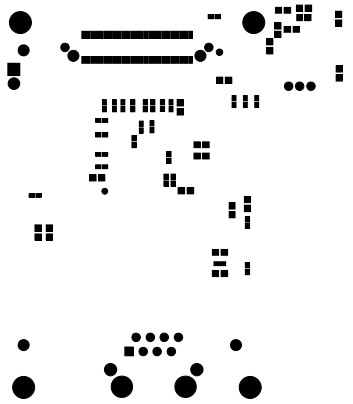


Figure 49. Bottom Solder Mask

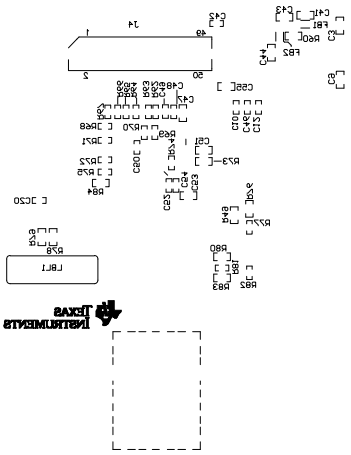


Figure 50. Bottom Overlay

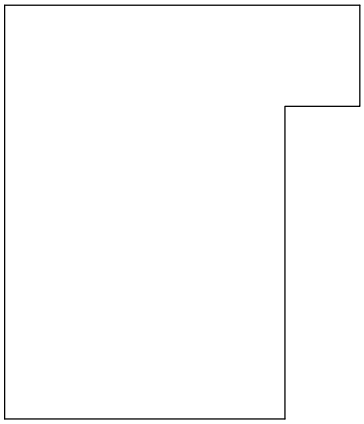


Figure 51. M1 Board Outline

8.4 Altium Project

To download the Altium project files, see the design files at TIDA-00207.

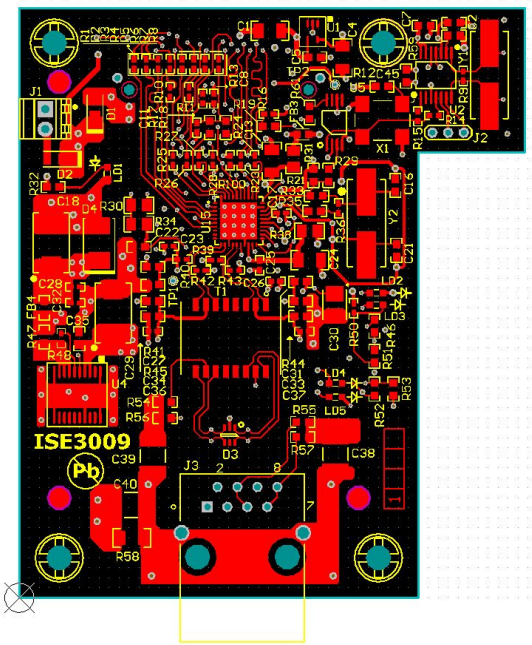


Figure 52. Top Layer

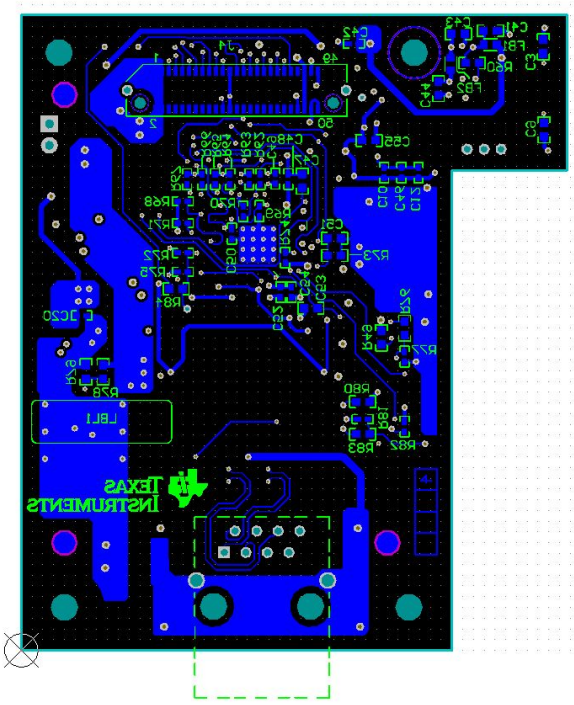


Figure 53. Bottom Layer

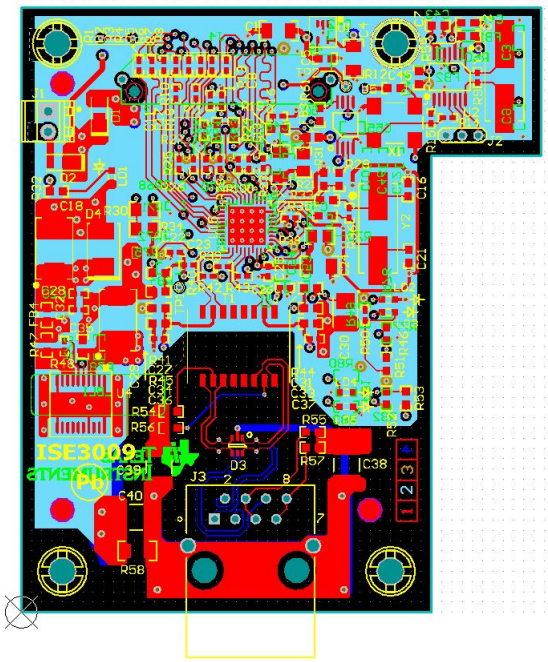


Figure 54. All Layers

8.5 Gerber Files

To download the Gerber files, see the design files at TIDA-00207.

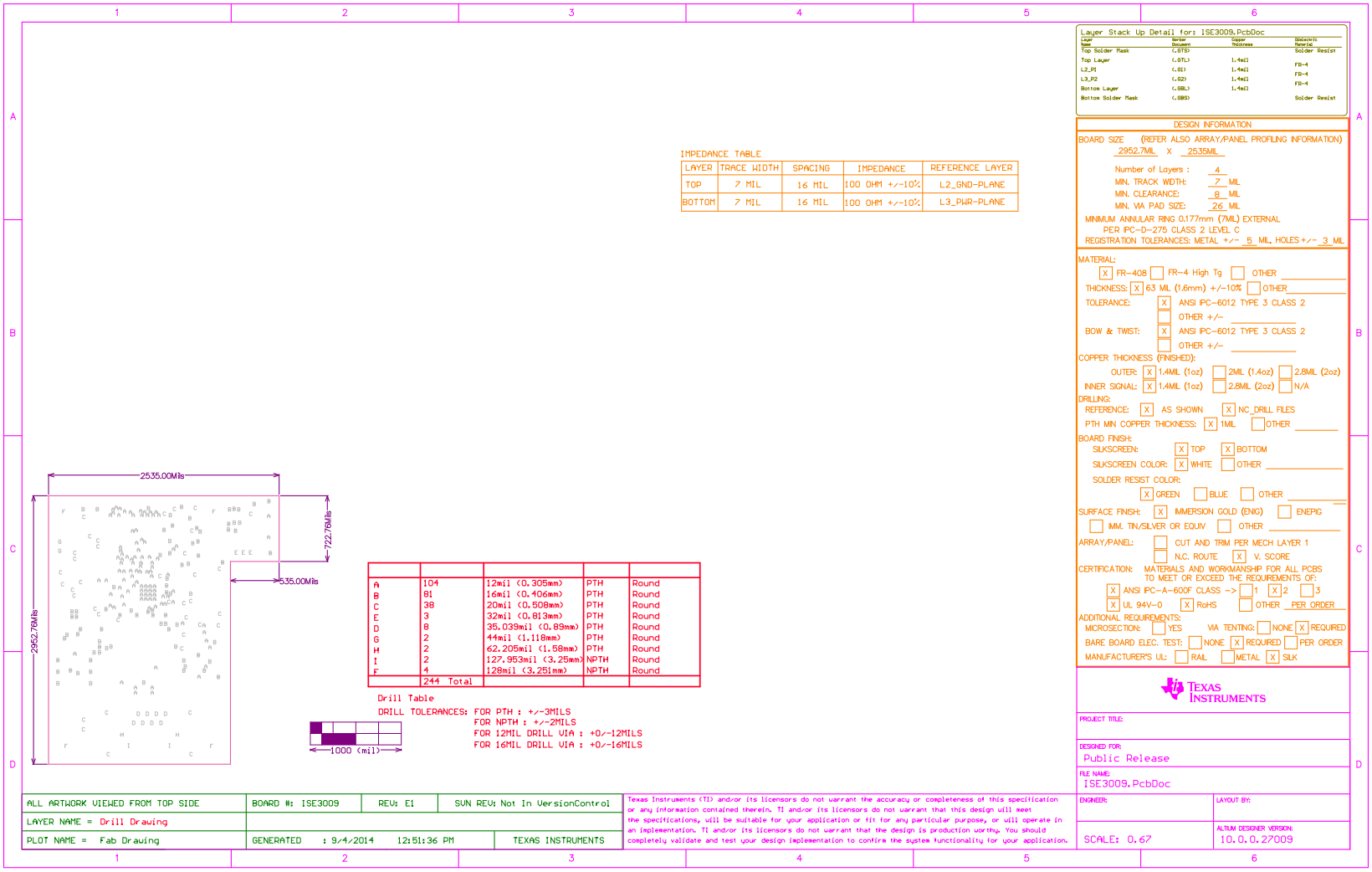


Figure 55. Fabrication Drawing

8.6 Assembly Drawings

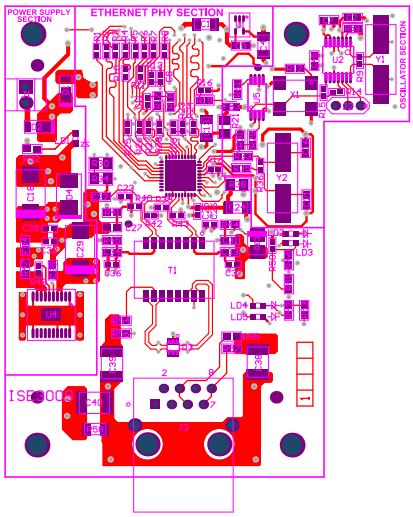


Figure 56. Assembly Top

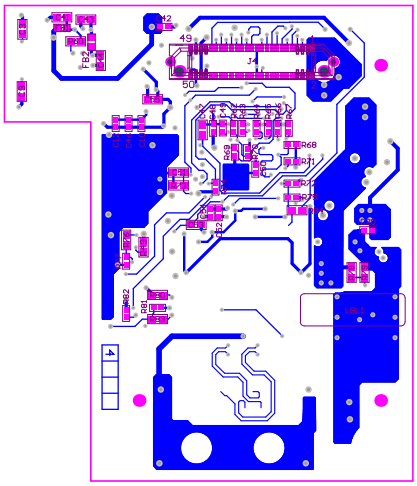


Figure 57. Assembly Bottom

9 References

1. PHYTER® Mini LS Industrial Temperature Single Port 10 100 Mbs Ethernet Transceiver (Link)
2. *DP8384K PHYTER Mini LS Industrial Temperature Single Port 10/100 Ethernet Transceiver* (SNLS251D)
3. Tiva C Series TM4C1294 Connected LaunchPad (Tool Folder)
4. *AN-1540 Power Measurement of Ethernet Physical Layer Products* (SNLA089B)
5. *32-Bit ARM Cortex-M4F MCU-Based Small Form factor Serial-to-Ethernet Converter* (TIDU348)

10 About the Author

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Revision History

Changes from Original (September 2014) to A Revision	Page
• Added third bullet	1
• Added "for DP83848K" to final bullet	1
• Changed from Level 3	3
• Changed 5-V to 3V3 regulator from TPS65433	4
• Changed Configuration Pins schematic	17
• Added *ESD Test Results*	31

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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