TI Designs

Isolated Current Shunt and Voltage Measurement Kit

TI Designs

TI Designs provide the foundation that you need including methodology, testing and design files to quickly evaluate and customize the system. TI Designs help *you* accelerate your time to market.

Design Resources

TIDA-00171	Tool Folder Containing Design Files
AMC1304M05	Product Folder
AMC1304M25	Product Folder
CDCE906	Product Folder
SN6501	Product Folder
TPS7A3001	Product Folder
TLV70450	Product Folder
OPA211AI	Product Folder
INA826	Product Folder
TPS55340	Product Folder
LP38798	Product Folder
TPS54232	Product Folder
REF3012	Product Folder
DAC8564	Product Folder
TMS320F28377D	Product Folder

TI E2E™ Community

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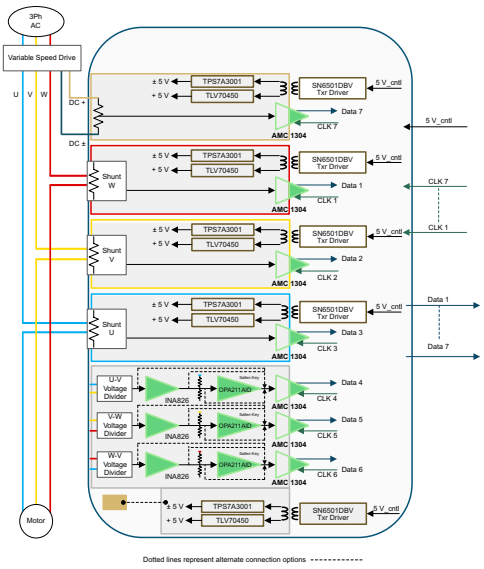
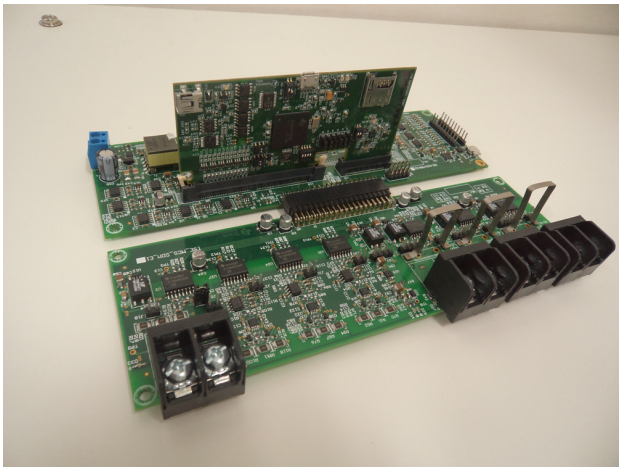
Design Features

- Isolated Shunt Feedback Measurements of 3-Phase Motor Currents and Voltages Using Isolated, Delta-Sigma Modulator AMC130x
- Integrated Sinc^3 Digital Filters using new C2000™ F2837xD Dual-Core Delfino™ Microcontroller
- Uncalibrated Accuracy of <2% at 25°C
- Calibrated Accuracy of ±0.2%
- <4-µS Response Time for Protection
- Option of Powering Board from Bootstrap Power Supply from Inverter for System Level Testing
- 16-Bit DAC for Real-Time Signal Regeneration for Analysis
- Onboard Isolated Power Supply
- Run-Time GUI for Complete Performance Analysis of Modulator Clock, Sinc Filter Parameters, and Current and Voltage Waveforms
- Tested for IEC61800 (EMC Requirement)

Featured Applications

- AC Motor Drives
- Uninterruptible Power Supplies
- Solar Inverters





1 System Description

1.1 Introduction to Measurement in Variable Frequency Drives

Government regulations around the world are calling for higher efficiency of industrial motor drives because they account for a considerable amount of our total energy consumption. Higher efficiency requires optimization of the torque and rotor speed, depending on the actual demand of the system, which can be achieved in part by increasing the accuracy of the motor current and voltage measurements.

Current measurement is an inherent part of any inverter-driven application. For speed and torque control in electrical drive systems, the converter output current has to be captured for online calculation of the PWM pattern. The current loop regulator typically works between 1 and 8 kHz. The signal used for this control loop must contain information from 10 to 40 kHz with a required resolution from 12 to 16 bits.

To increase the reliability and reduce the cost of the drive, a great effort has been made to eliminate the shaft speed or position sensor in most high performance induction motor drive applications. Rotor-speed estimators for induction motor drives use stator voltage and current measurements along with motor parameters for estimation. Dynamic performance of induction motor field-oriented controllers strongly depends on model parameter accuracy, which again depends on the measurement accuracy.

Both motor control and grid applications use the rotating-reference frame to control currents in the so-called d–q rotating coordinate system. Regulation of the currents of the d and q axes requires at least two phase current measurements. The current components become quasi-DC and the control are simplified to a low requirement in bandwidth. The more accurate current and voltage measurements improve the performance of motor drives by reducing torque ripple on the motor shaft.

One industry trend that is gaining more traction is to use delta-sigma modulation for measuring current and voltage levels. The primary reason for this shift is that delta-sigma modulation reduces overall system cost while providing high performance.

Traditionally, Hall effect sensors are used for the current and voltage measurement as they offered important electrical isolation. The hall effect sensor can be replaced with a current shunt resistor and isolated delta-sigma modulator, a more accurate and less expensive option, and provide direct measurement of current and voltage. A delta-sigma modulator converts an analog input signal into a high-frequency stream of single bits with out-off band noise. The advantage of moving the quantization noise to higher frequency bands include simple anti-aliasing filtering, low-cost solution by eliminating cost on drivers, and filters and scalable performance.

TI's latest isolated delta-sigma modulator, the AMC130x, is designed specifically for direct connection to current shunt resistors and has a galvanic isolation barrier. The AMC130x device is a second-order, delta-sigma modulator that is reinforced and isolated, which is ideal for motor control. It has two variants with 50-mV and 250-mV inputs. A 50-mV variant is used to measure current and a 250-mV variant is used to measure voltage. By having a low-input voltage of 50 mV, the power dissipation in the shunt resistor can be reduced significantly. A block diagram of the new approach is shown in Figure 1 and Figure 2.

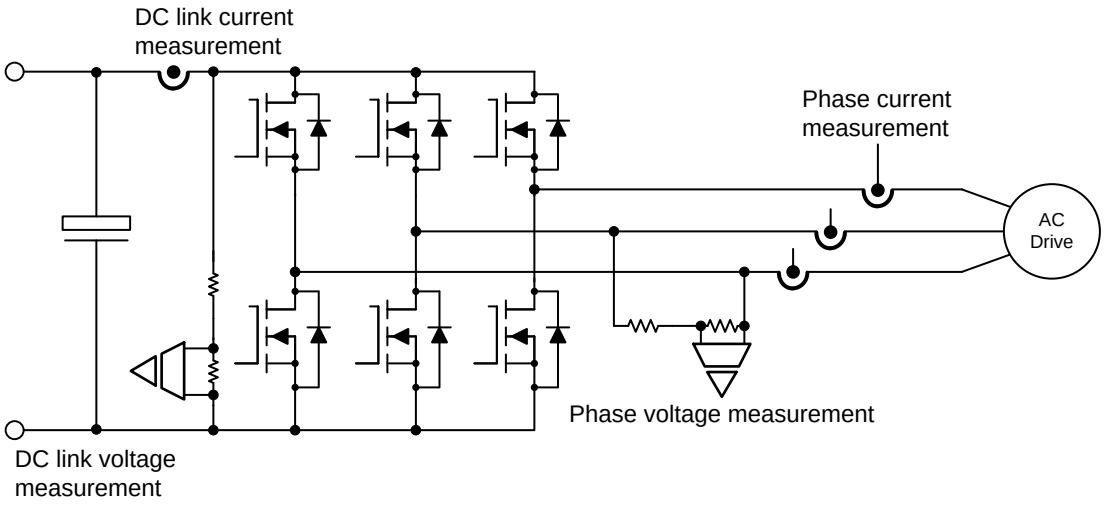


Figure 1. Current and Voltage Measurement in 3-Phase Inverters

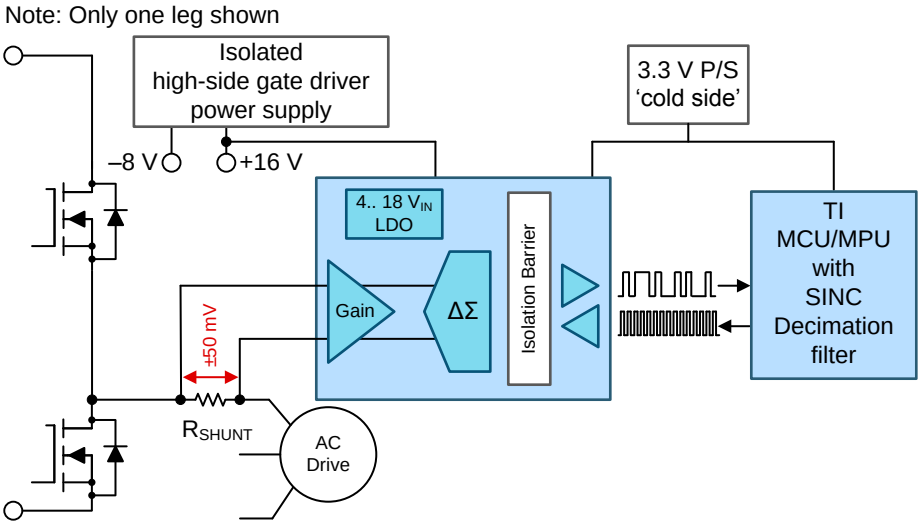


Figure 2. Delta-Sigma Modulator in Three-Phase Inverter

In motor control, up to eight signals need to be monitored. Therefore, it is most important to keep the costs for the sensors and their analog-to-digital conversion low. The cheapest method to measure currents is adding a resistor (shunt) into the current path and to measure the voltage drop across the resistor. A delta-sigma modulator is used to convert this voltage drop into a bit-stream. AMC130x converts the shunt voltage (equal approximately current) across the shunt resistor into a digital high frequency (20 MHz) bit stream, which can be filtered using $Sinc^3$ filter built into TI Delfino controllers. Similarly a cost effective method for measurement of the DC link or inverter voltage is to use a resistive divider to step down the voltage to a level acceptable by the delta-sigma modulator.

When measuring current by using shunts we can minimize the power loss ($P = I \times V$) in the shunt by using the AMC1304M05 part with ±50-mV input. Hence the voltage drop across the shunts remains as small as possible. AMC1304 delta-sigma modulators are very robust in respect to noise and offset. Even such low voltages can be converted to high resolutions. Also, the shunt and the modulator are often at a floating potential, so that the digital output (bit-stream) of the modulator must be galvanically isolated. AMC1304 has reinforced isolation, this provides the galvanic isolation for functioning of the application and required safety aspect to protect the user. The bit-stream is a two wire interface, a data and a clock signal. A high-resolution signal is extracted from the bit-stream with an appropriate low pass filter – $Sinc^K$ filters. The filter structure can be adjusted to the applications needs in respect of resolution and speed.

This reference design based on AMC130x along with TI Delfino controller provides provisions to measure currents and voltage as follows.

- Three motor currents
- DC link voltage
- Three inverter voltages (phase and line voltages)

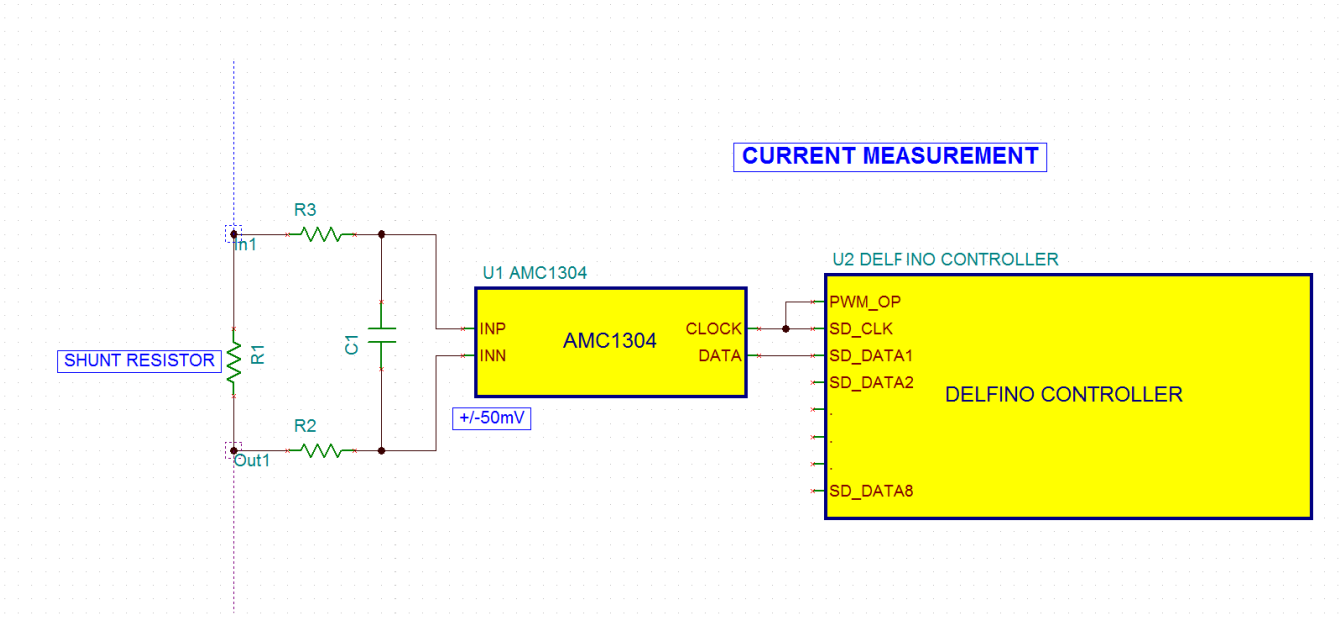


Figure 3. Current Measurement Using AMC130x and Delfino Controller

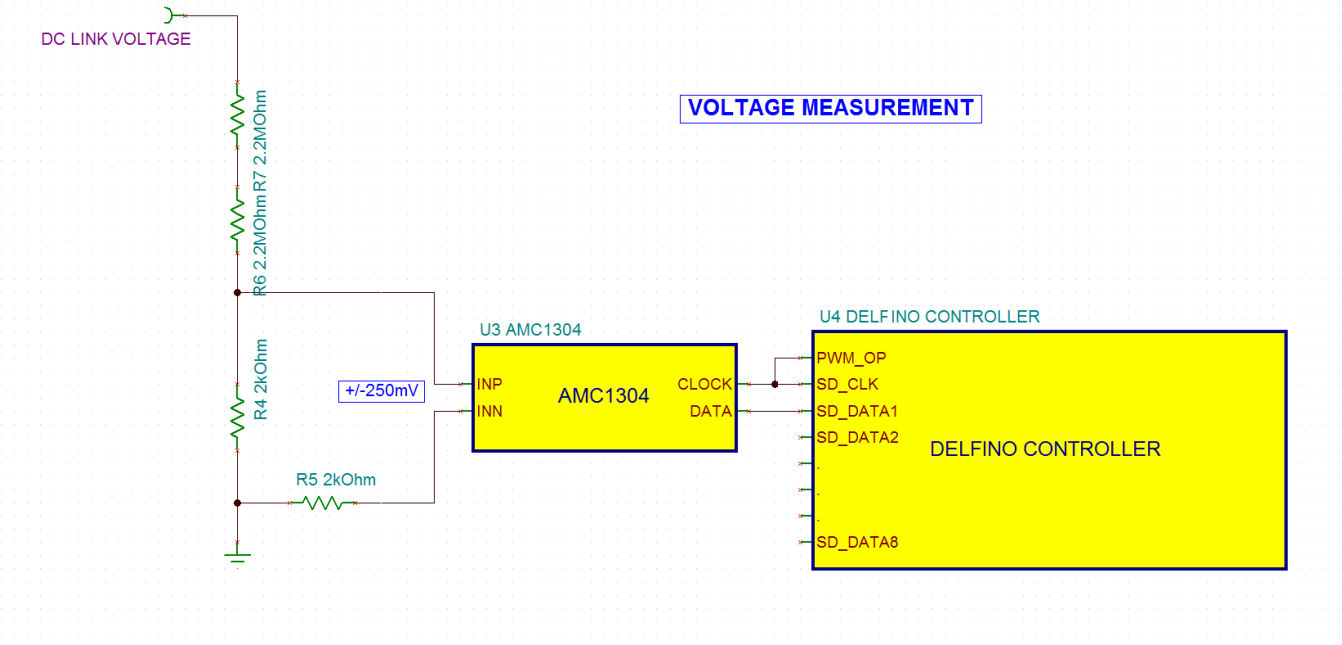


Figure 4. Voltage Measurement Using AMC130x and Delfino Controller

1.2 AMC130x Delta-Sigma Modulator

The AMC130x is a family of single-channel, second-order delta-sigma modulators designed for medium- to high-resolution analog-to-digital conversions. The analog input signal is continuously sampled by the modulator and compared to an internal voltage reference. The isolated output of the converter (DATA) provides a stream of digital ones and zeroes. The time average of this serial output is proportional to the analog input voltage.

A differential input signal of 0 V ideally produces a stream of ones and zeroes that are high 50% of the time and low 50% of the time. The relation between ones and zeroes changes with the input signal. A positive input voltage of 250 mV (specified full-scale range) for a ±250-mV part results in a bit stream with 90% ones, whereas a signal at negative full-scale (–250 mV) is only high 10% of the time. This specified FSR is also the linear range of the modulator with the performance as specified in the data sheet.

The range between the specified FSR (±250 or ±50 mV) and the absolute FSR (±312.5 or ±62.5 mV) is the non-linear range of the modulator. The output of the modulator clips with a stream of only zeros with an input less than or equal to the minimum value of the absolute FSR value or with a stream of only ones with an input greater than or equal to the positive value of the absolute FSR. The input voltage versus the output modulator signal is shown in Figure 6.

The system clock of the AMC1304 device is provided externally at the CLKIN pin. The data are synchronously provided at f_{CLKIN} at the DATA output pin. The data are changing at the falling edge of CLKIN.

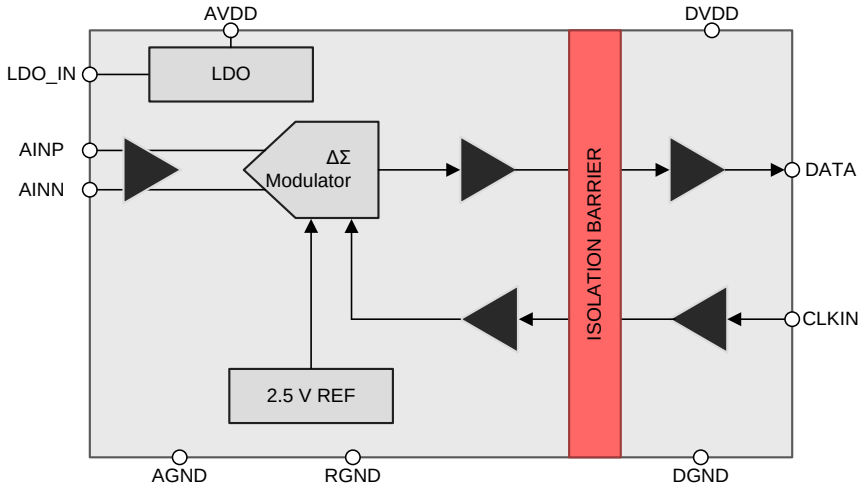


Figure 5. AMC1304 Block Diagram

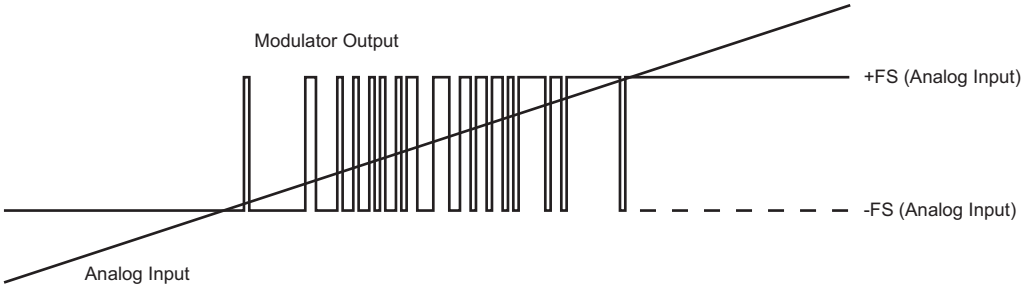


Figure 6. AMC130x Input Voltage versus Output

Benefits of using AMC130x are:

- Galvanic barrier provides EMI immunity and robust isolation barrier lifetime
- Wide clock range provides sample rate flexibility to customer
- Reduced input voltage range enables higher shunt currents

1.3 Sinc (CIC) Filters

Cascaded Integrator-Comb (CIC) filters are multi-rate filters often used for implementing large sample rate changes in digital systems. They are typically employed in applications that have a large excess sample rate. That is, the system sample rate is much larger than the bandwidth occupied by the processed signal. Implementations of CIC filters have structures that use only adders, subtractors, and delay elements. These structures make CIC filters appealing for their hardware-efficient implementations of multirate filtering.

There are two sections to the CIC decimator filter:

1. An integrator section with N integrator stages that processes input data samples at sampling rate fs
2. A comb section that operates at the lower sampling rate fs / R

This comb section consists of N comb stages with a differential delay of M samples per stage. The down sampling operation decimates the output of the integrator section by passing only every R^{th} sample to the comb section of the filter.

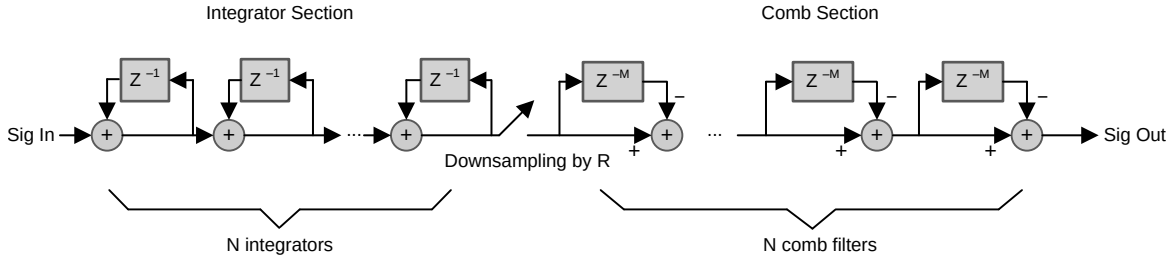


Figure 7. CIC Filter Structure

1.3.1 CIC Integrator Stage

The block diagram of a CIC integrator stage is illustrated in Figure 8. The difference equation that describes the integrator stage is given by:

$$y(n) = x(n) + y(n-1) \quad (1)$$

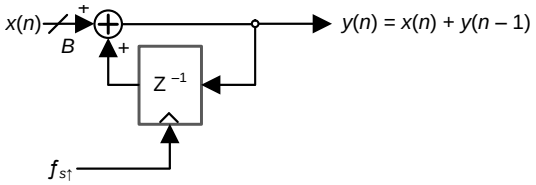


Figure 8. CIC Integrator Section

The corresponding z-transform and transfer function is given by Equation 2.

$$Y_{(z)} = X_{(z)} + z^{-1} Y(z)$$

$$H_{I(z)} = \frac{Y_{(z)}}{X_{(z)}}$$

$$H_{I(z)} = \frac{1}{1 - z^{-1}} \quad (2)$$

The N section cascade of integrators is given by Equation 3.

$$\left[H_I(z)\right]^N = \left[\frac{1}{1 - z^{-1}}\right]^N \quad (3)$$

1.3.2 CIC Comb Filter Stage

Figure 9 illustrates the general form of the comb filter architecture where the parameter *M* specifies the programmable comb filter differential delay. The output sequence generated by this structure is given by the difference in Equation 4.

$$y(n) = x(n) - x(n - M) \tag{4}$$

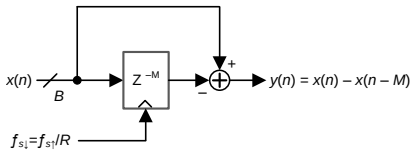


Figure 9. CIC Comb Filter Section

Although *M* could take on many possible values, the best CIC filter performance is generally obtained by limiting *M* to be equal to either 1 or 2.

Take the *Z* transform of both sides of the equation to obtain Equation 5.

$$Y(z) = (1 - z^{-M})\, X(z) \tag{5}$$

Define the transfer function as Equation 6.

$$H_C(z) = \frac{Y(z)}{X(z)}$$

$$H_C(z) = \left(1 - z^{-M}\right) \tag{6}$$

To obtain the frequency response of a discrete-time system expressed in the *Z* domain, make the substitution $Z = re^{j\omega}$.

Since the evaluation takes place on the unit circle, the magnitude *r* equals unity; therefore, $Z = re^{j\omega}$.

Make this substitution into Equation 6 to get Equation 7.

$$H_C(z)\big|_{z=e^{j\omega}} = \left(1 - e^{-j\omega M}\right) = \left(1 - e^{-j2\pi M f_{\downarrow}}\right) \tag{7}$$

The composite CIC filter response is composed of both the comb frequency response $H_C(z)$ and the integrator frequency response $H_I(z)$ in cascade. The composite frequency response is given by $H(z) = HI(z)H_C(z)$ for a single stage filter. Each of these two frequency response components operate at different sample rates. However, in order to discuss the composite CIC filter frequency response, reference the frequency response of the comb filter sections relative to the high sample rate of the integrator. Derive this high rate reference by substituting the high rate frequency in Equation 8.

$$H_C(z)\big|_{z\,=\,e^{j\omega}} = \left(1 - e^{-j2\pi RMf_{\downarrow}}\right) \tag{8}$$

The corresponding z-transform of the comb filter referenced to the high sample rate is expressed as Equation 9.

$$H_C(z) = \left(1 - z^{-RM}\right) \tag{9}$$

1.3.3 CIC Filter

Because the comb sections and integrator sections are in cascade with one another, the z-transform of the composite CIC filter can then be expressed as Equation 10.

$$H(z)=\left[H_C(z)\right]^N\left[H_I(z)\right]^N=\left[\frac{\left(1-z^{-RM}\right)}{\left(1-z^{-1}\right)}\right]^N \tag{10}$$

Evaluate Equation 10 on the unit circle in the z-plane by replacing the complex variable, *z*, with the complex exponential $Z = e^{j\omega}$ as shown in Equation 11.

$$H_C(z)\big|_{z=e^{j\omega}}=H\left(e^{j\omega}\right)=\left[\frac{1-e^{-j\omega RM}}{1-e^{-j\omega}}\right]^N \tag{11}$$

For a third-order CIC filter with differential delay of 1 (N = 3, M = 1), Equation 11 can be rewritten as Equation 12.

$$H\left(e^{j\omega}\right)=\left[\frac{1-e^{-j\omega R}}{1-e^{-j\omega}}\right]^3 \tag{12}$$

In a Sinc^3 filter response, the location of the first notch occurs at the frequency of output data rate $f_{DATA} = f_{CLK} / R$. The –3-dB point is located at $f_{DATA} / 4$.

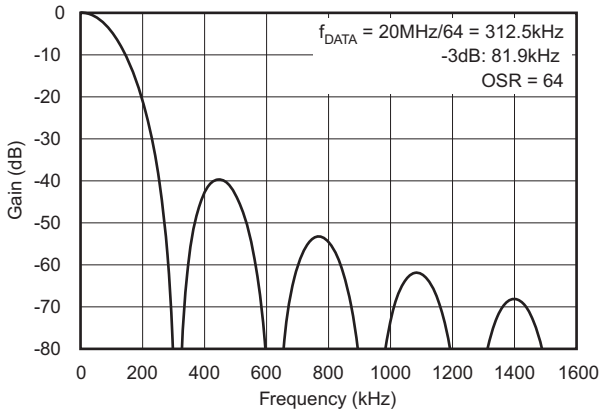


Figure 10. Magnitude versus Frequency Response of the Sinc^3 Filter

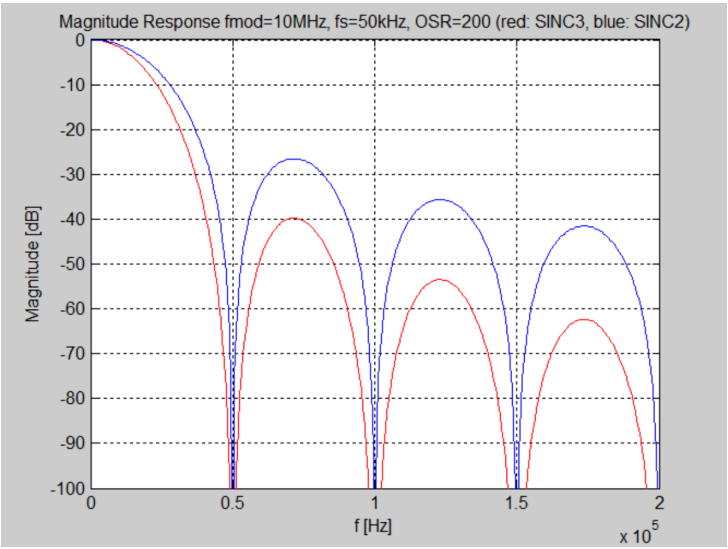


Figure 11. Magnitude versus Frequency Response of Sinc^2 Compared to Sinc^3 Filter

Thumb rules refers to the relationship between the modulator clock (or sampling frequency f_S), output data rate (or first-notch frequency), and the decimation ratio *R* is given by:

- Date rate = Fs / R
- A $Sinc^3$ filter –3-dB response point is 0.262 times the data rate
- For the third-order Sinc filter, the step function response requires three clock periods

Using the $Sinc^3$ decimation filter architecture, the output signal update rate depends on the modulator clock frequency and the decimation ratio. Using a 20-MHz modulator in conjunction with a decimation ratio of 256, the current signal will be updated every 12.8 µs. This conversion delay is acceptable for carrier based PWM control schemes as long as this delay is significantly smaller than the PWM sub-cycle time duration (TPWM / 2). For a 16-kHz PWM frequency, this configuration provides four current samples.

According to Figure 12, the TI modulator, AMC1304, provides an OSR of 128 and a $Sinc^3$ filter result of 14-bit precision. Decreasing the OSR to 64 would reduce the precision by two bits to only 12 bits. Increasing the OSR to 256 is not significantly increasing the precision; however, that value increases the conversion settling time.

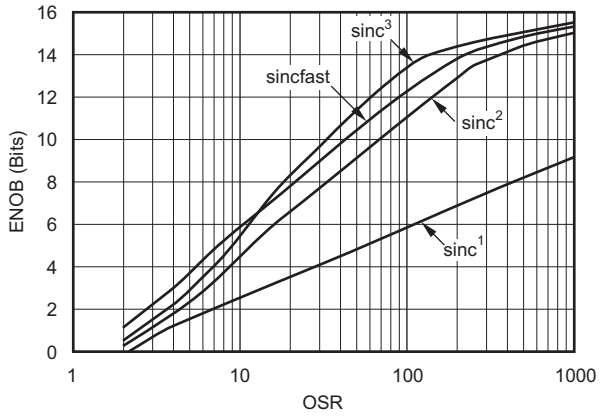


Figure 12. Measured Effective Number of Bits versus Oversampling Ratio

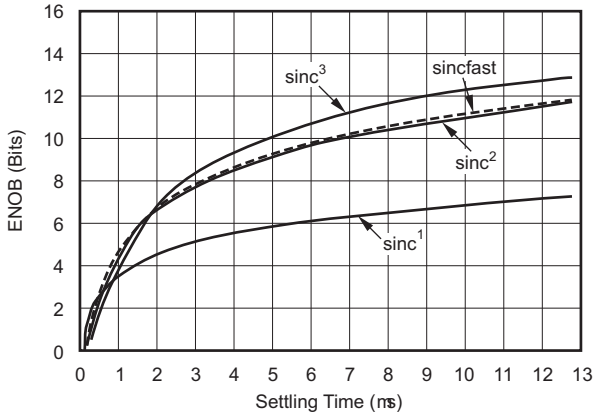


Figure 13. Measured Effective Number of Bits versus Settling Time

2 Design Features

The following are the design specifications of the *Isolated Current Shunt and Voltage Measurement Kit* reference design:

Table 1. TIDA-00171 Design Specifications

PARAMETER	SPECIFICATIONS and FEATURES
Measurement Parameter	3-phase motor currents 3-phase inverter voltage DC link voltage (Seven total channels)
Current	7 A_{RMS}
Voltage	550-V DC for DC link measurement 390-V AC for inverter voltage measurement
Measurement Accuracy, Post Calibration	±0.2% over the temperature range: –25°C to 75°C
Resolution	16 bit
Module Calibration	Offset and gain calibration of the AMC
Power Supply Range	18-V to 32-V DC
Isolation	Reinforced, IEC60747-5-2
ESD Immunity	**IEC 61000-4-2:** ±4-KV contact discharges ±8-KV air discharges
EFT Immunity	**IEC 61000-4-4:** ±4 KV at 5 KHz on U, V, W
Surge Transient Immunity	**IEC 61000-4-5:** ±4 KV CM, DM on U, V, W Inputs
Operating Temperature Range	–25°C to 75°C
Modules	Delta-sigma Module, filter module board, Delfino control card These three boards are integrated by appropriate board-to-board connectors

3 System Configuration and Block Diagram

Implementation of current and voltage measurement system has been split into three boards to have modularity.

1. The filter module board, or FMB, incorporates the power supply, slot to mount the Delfino control card, digital-to-analog converter (DAC), PLL, and Sallen-Key filters.
   - A 24-V input is converted into the 5 V and 3.3 V required to operate the circuit.
   - The PLL generates the required clock for the delta-sigma modulators
   - The DAC outputs the measured current and voltage
   - A provision of Sallen-Key filters converts the one-bit data stream from delta-sigma modulators back into analog domain
2. The delta-sigma module, or DSM, comprises of the entire signal chain for current and voltage sensing. The board has three channels for motor current sensing, three channels for inverter voltage sensing, and one channel to measure the DC link voltage. Each of the channels is provided with ESD protection diodes and a low-pass RC filter. The filtered signal is converted into a one-bit modulated stream by AMC130xM05 (±50-mV max input) or AMC130xM25 (±250-mV max input). This bit stream is then demodulated by a Sinc filter implemented within the C2000 processor of the Delfino control card.
3. The Delfino control card consists of a Delfino microcontroller along with associated peripherals. The control card has USB connectivity to interface with PCs, for programming, and for debugging.

   The three PCBs are integrated by the board-to-board connectors form the Isolated Current Shunt and Voltage Measurement Kit as shown in Figure 14.

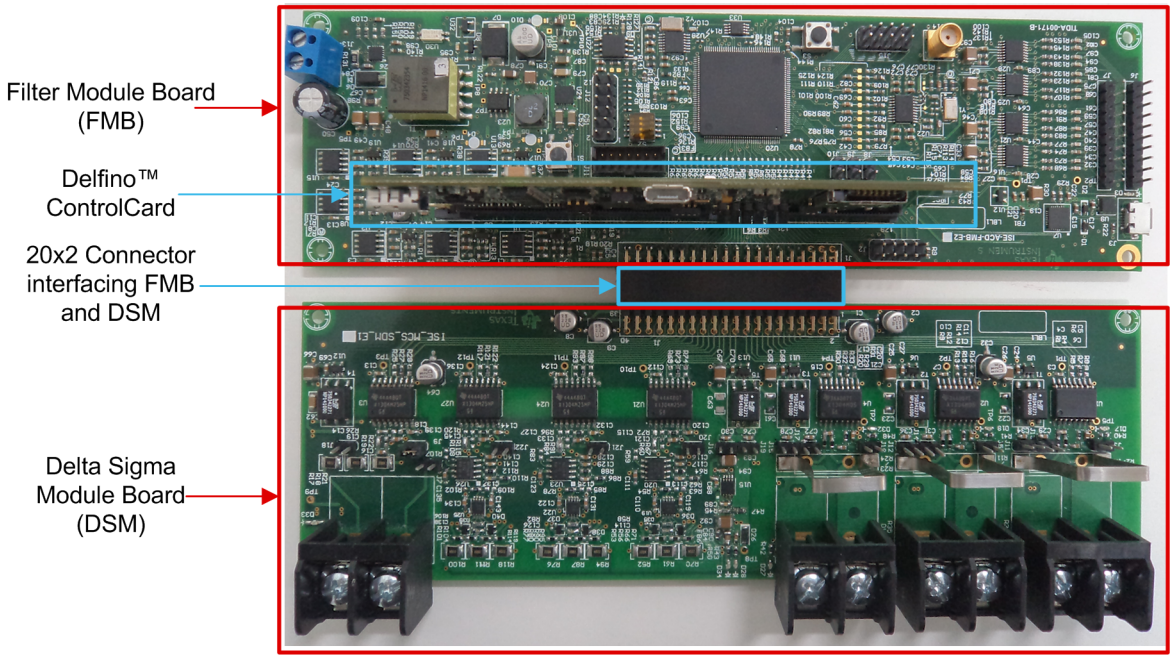


Figure 14. Picture of Isolated Current and Voltage Measurement Kit

3.1 DSM Board

The high-level block diagram of the DSM board is shown in Figure 15.

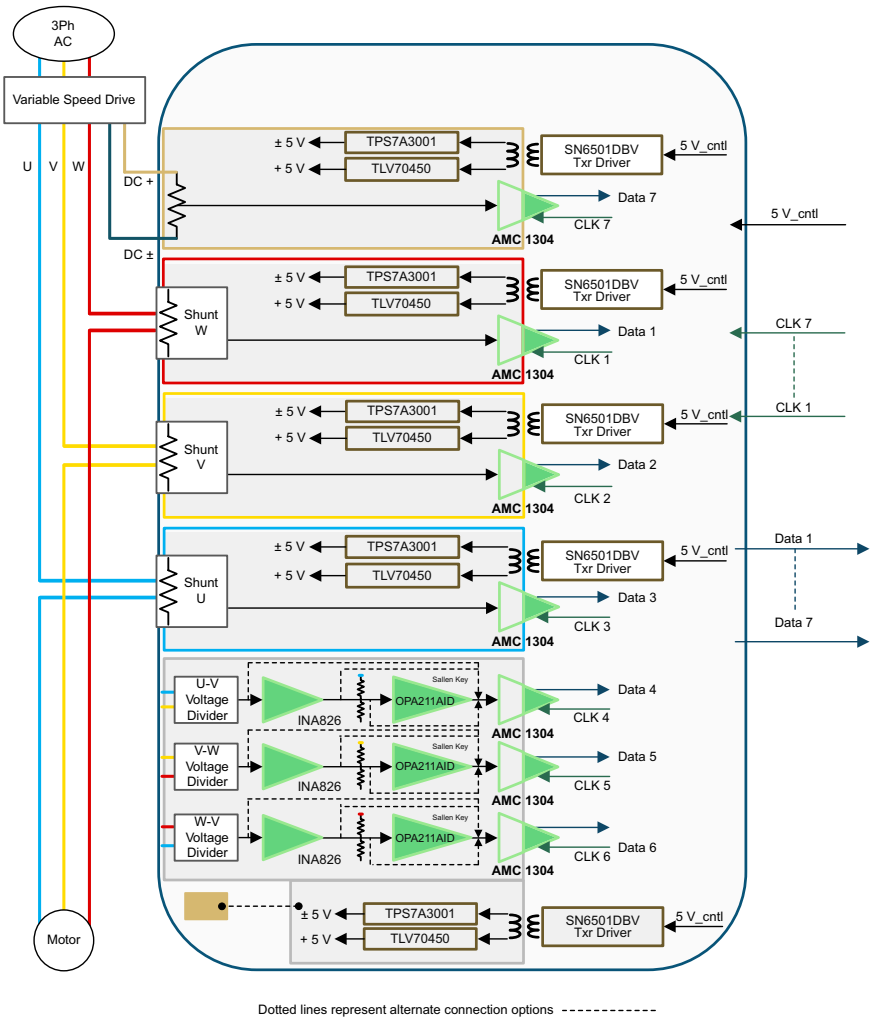


Figure 15. Block Diagram of DSM

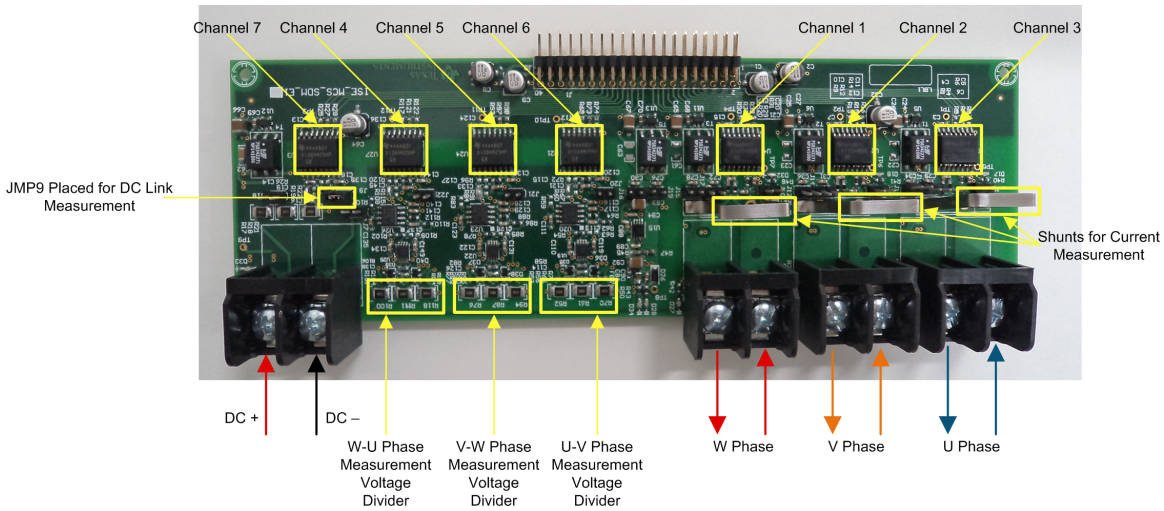


Figure 16. DSM Board

The DSM board features the following:

1. **Isolated Power Supply:** As shown in Figure 15, five isolated DC power supplies power the high side of the AMC1304 device. Each of the three current channels is provided with separate isolated 5-V to 5-V DC converters. The option is also provided to power the AMC130x device using gate-drive power supplies. The AC voltage measurement channels are provided with a common isolated 5-V DC. The DC link voltage measurement channel has its own isolated 5-V DC power supply.
2. **Inverter Measurements:** The AC motor is driven from a 3-phase inverter. The inverter voltage and motor current are measured by the isolated delta-sigma convertor AMC130xM25 and AMC130xM05. Each of the seven AMC130x isolated digital output (DOUT) converters of the modulator provide a stream of digital ones and zeroes that is synchronous to the clock source, provided at CLKIN pin, with a frequency in the range of 5 to 20.1 MHz. The time average of this serial bit-stream output is proportional to the analog input voltage.
   - **Inverter Voltage Measurement:** The PWM output voltages on the U, V, and W lines are scaled down through resistive dividers and then filtered for attenuating the noise. Options are provided to include or bypass an additional Sallen-Key filtering. The filtered output is provided to each of the three AMC1304M25 devices. The Sallen-Key filter attenuates frequencies above 20 Khz. This device can measure up to ±250 mV, which corresponds to 389-V_{RMS} of phase-to-phase AC voltage. For a wider range, the potential divider circuit needs to be modified accordingly.
   - **Motor Current Measurement:** The currents through motor windings are measured as voltage across 5-mΩ shunts. This voltage is then measured by AMC1304M05. This device can measure up to ±50 mV, which corresponds with up to 7-A_{RMS} AC current. For a higher measurement range, the shunt resistance may be reduced accordingly.

     NOTE: The accuracy of the shunt and the PCB layout are critical factors in the overall measurement accuracy. Use a four-wire shunt for a highly accurate system.

   - **DC Link Voltage Measurement:** The DC link voltage is stepped down to 250 mV through a resistive divider and is measured using AMC130xM25. The maximum DC voltage that can be measured is ±550-V DC.
3. **Connectors:** The DSM board has connectors to interfaces with the FMB board as well as with the drive and motor. Jumpers provide some specific, optional functions. The footprint of connectors is as highlighted in Table 2.

Table 2. Connectors on DSM Board

CONNECTOR on DSM	FUNCTION	CONNECTOR TYPE
J1	DSM to FMB	2×20 pins, right angle, female, board-to-board
J2, J4, J8	U,V,W Inputs or outputs	4×1, terminal block, 2.54-mm pitch
J6	DC link input	4×1, terminal block, 2.54-mm pitch
J3, J5, J9, J10, J20, J21, J22	Jumper to connect AVDD pin of AMC1304 to external AVDD (gate drive power supply)	2 pin, male header
J11, J12, J13, J14, J15, J16, J17, J18, J19	Jumper to enable or disable the isolated ±5 V to the corresponding LDOs	2 pin, male header

3.2 Filter Module Board

The high level block diagram of the FMB is shown in Figure 17 and Figure 18.

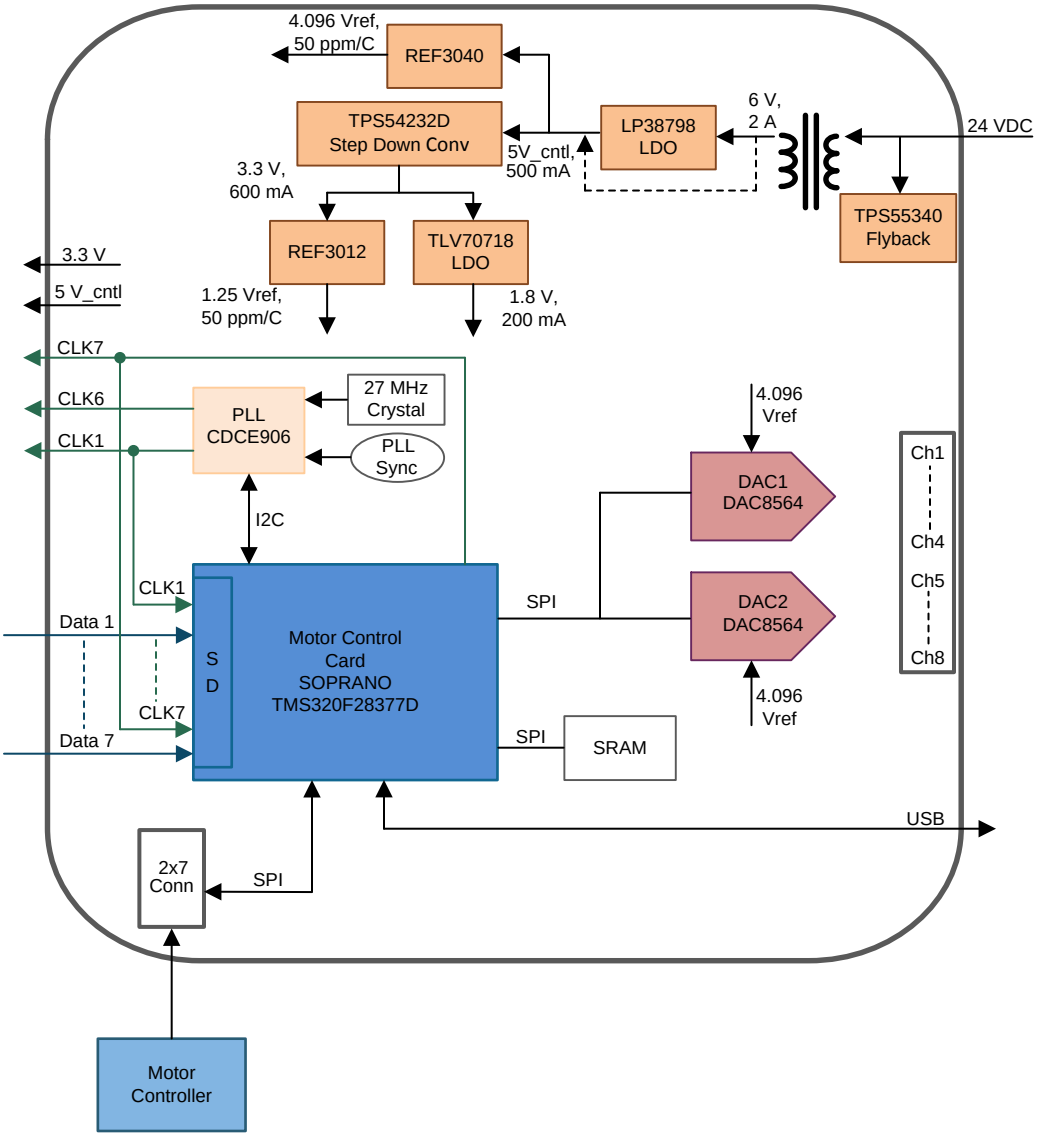


Figure 17. Block Diagram of FMB Subsystem

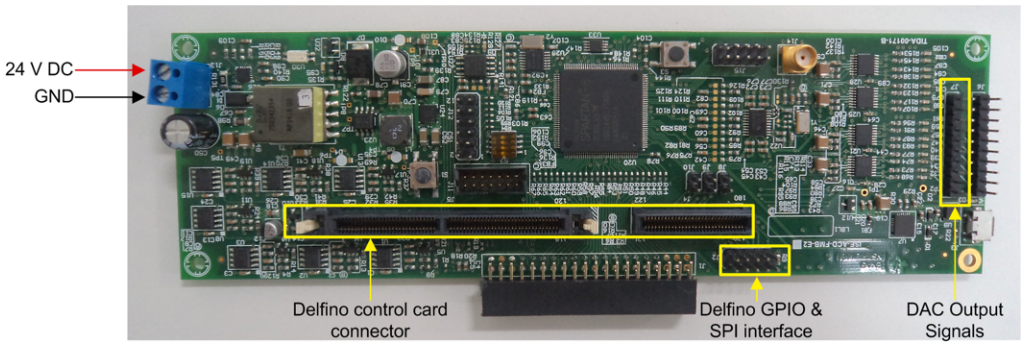


Figure 18. FMB

The subsystem PCBA consists of the following:

- **Power Supply:** 24-V DC to 6-V isolated DC-DC convertor based on flyback topology employing TI's TPS55340 device. The subsequent rails of 5 V and 3.3 V and analog references are generated by using TI's TPS54232 (step-down convertor), TLV70718 (LDO), REF3040, REF3012, and the optional LP38798 (LDO). The designs are provided with sufficient buffer to allow customers to load and add more functions without changing the power supply ICs.

  The power consumption estimated for each of the rails are shown in Table 3.

Table 3. Power Consumption Estimates of Rails

LOAD or RAIL	5 V	3.3 V	1.2-V REF	4.096-V REF
AMC1304s on FMB	100 mA	NA	NA	NA
Control card	200 mA	NA	NA	NA
Clock CDCE906	NA	125 mA	NA	NA
DACs on FMB	50 mA	NA	NA	25-mA max,75 PPM/C
Amplifier or filters	5 mA	NA	25-mA max, 75 PPM/C	NA
Further expansion	150 mA	375 mA	NA	NA
Total	500 mA	600 mA	50-µA max, 50 PPM/C	50-µA max, 50 PPM/C

- **Clocks:** The modulator on the DSM board requires up to 20 MHz of clock to generate a synchronized bit stream of up to 16-bit accurate measurement. The FMB generates clock by using the PLL synthesizer, CDCE906. The CDCE906 device can take high accuracy clock input from either a local crystal or an external clock source through the SMA connector (J14). The output from CDCE906 is sourced to the Delfino controller as well as to the DSM. Six clock outputs from the PLL are used by the six modulators meant for motor current and inverter voltage measurement. The seventh modulator (DC link measurement) is supplied with the clock generated by the Delfino controller.
- **DACs:** The measured voltage and currents can be displayed simultaneously by two DAC8564 devices, which make a 16-bit quad-channel voltage output DAC.
- **Amplifiers and Sallen-Key Filters:** These filters are provided as an option to convert the digital stream back from modulators to analog, which can be processed by the SAR ADC for motor control loops.
- **Connectors:** The FMB is provided with connector interfaces to the DSM board, control card, clock input, JTAG, and DAC. The functions of the connectors is as highlighted in Table 4.

Table 4. Connectors on FMB

CONNECTOR on FMB	FUNCTION	CONNECTOR TYPE
J1	FMB to DSM	2×20 pins, right angle, male, board-to-board
J2, J15	SPI interface	2×5 pins, male
J3	USB (not used currently)	USB micro type AB
J4	FMB to control card	60 pin, high-speed card edge
J5	FMB to control card	120 pin, high-speed card edge
J8, J9, J10	Controller GPIO	2×5 pins, male
J13	24-V DC input	2 pin
J14	External clock input	SMA female jack

3.3 Delfino Control Card

TI' Delfino F28377D controlCARD (TMDSCNCD28377D) provides a great way to learn and experiment with the F2837x device family and within TI's C2000 family of microcontrollers (MCUs). This 180-pin control card is intended to provide a well-filtered, robust design capable of working in most industrial environments.

3.4 F28377D controlCARD Features

- **Delfino F28377D MCU** – A high-performance C2000 microcontroller located on the control card
- **180-Pin HSEC8 Edge Card Interface** – Allows for compatibility with all of the C2000 180-pin control card application kits and control cards. Compatibility with 100-pin control cards can be accomplished using the TMDSADAP180TO100 adapter card (sold separately).
- **Built-In Isolated JTAG Emulation** – An XDS100v2 emulator that provides a convenient interface to Code Composer Studio™ without additional hardware. Flipping a switch allows an external JTAG emulator to be used.
- **Connectivity** – The control card contains connectors that allow the user to experiment with a USB, a microSD card, and isolated UART/SCI when working with the F2837x MCU devices.
- **Key Signal Breakout** – Most GPIO, ADC, and other key signals routed to hard gold connector fingers.
- **Robust Power Supply Filtering** – Requires a single 5-V input supply, On-card 3.3-V LDO. All MCU inputs are then decoupled using LC filters near the device.
- **ADC Clamping** – ADC inputs clamped by protection diodes.
- **Anti-Aliasing Filters** – Noise filters (small RC filters) can be easily added on several ADC input pins.

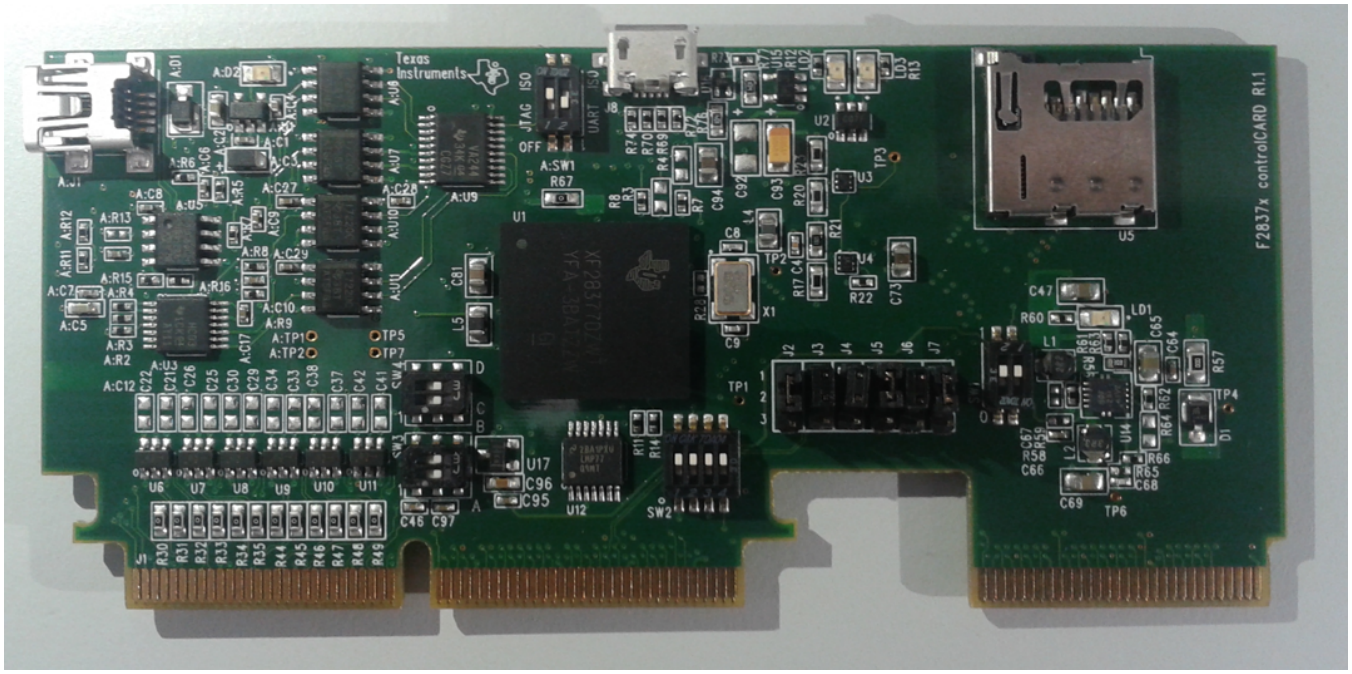


Figure 19. Delfino Control Card

4 Circuit Design and Component Selection

The Isolated Current and Voltage Measurement Kit is designed in a modular way to give customers greater flexibility in evaluating AMC130x for AC motor drive systems. Each of the subsystem modules in the design is explained in this section.

4.1 DSM

The DSM is comprised of the signal conditioning circuits, modulators, and isolated power supplies. The inputs to this board are the motor terminal voltage and corresponding motor winding current. The AMC1304 converts these inputs into a bit stream. The bit stream is transmitted to the Delfino control card, which is demodulated and filtered to obtain data.

4.1.1 AMC1304

The AMC1304 family is a precision DSM with an output isolated from the input circuitry by a capacitive isolation barrier that is highly resistant to magnetic interference. This barrier has been certified to provide reinforced isolation of up to 7000 V_{Peak}, according to UL1577 and IEC60747-5-5. Used in conjunction with isolated power supplies, this device prevents noise currents on a high common-mode voltage line from entering the local ground and interfering with, or damaging sensitive circuitry.

The input of the AMC1304 is optimized for direct connection to shunt resistors or other low voltage level signal sources. The unique low-input voltage range of the device allows significant reduction of the power dissipation through the shunt while supporting excellent AC and DC performance.

The simplified schematic is shown in Figure 20.

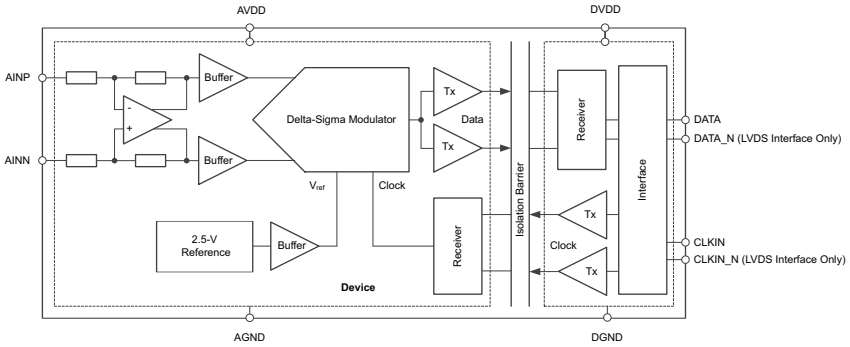


Figure 20. AMC1304 Pin Outs

The AMC1304 device incorporates front-end circuitry that contains a differential amplifier and sampling stage, followed by the DSM.

There are two restrictions on the analog input signals VINP and VINN:

1. If the input voltage exceeds the range AGND –6 V to AVDD 0.3 V, the input current must be limited to 10 mA, because the input protection diodes on the front end of the converter begin to turn on.
2. The linearity and the noise performance of the device are ensured only when the differential analog input voltage remains within ±250 mV for AMC1304M25 or ±50 mV for AMC1304M05.

The differential amplifier stage gains the differential input signal V_{IN} = (VINP – VINN) by a factor of four, in case of derivatives, with specified input voltage range of ±250 mV (AMC1304M25), or by a factor of 20 in devices with a ±50-mV input voltage range (AMC1304M05).

In this reference design, AMC1304M05 is used for current-shunt measurement, and AMC1304M25 is used for the voltage measurement.

The differential input impedance is 5 k for AMC1304M05 and 25 kΩ for AMC1304M25. The input impedance becomes a consideration in designs with high-input signal source impedance. This high impedance may cause degradation in gain (reduced by calibration on the system level), linearity, and THD.

4.1.1.1 AMC1304M25 for Current Measurement—Signal Chain Design

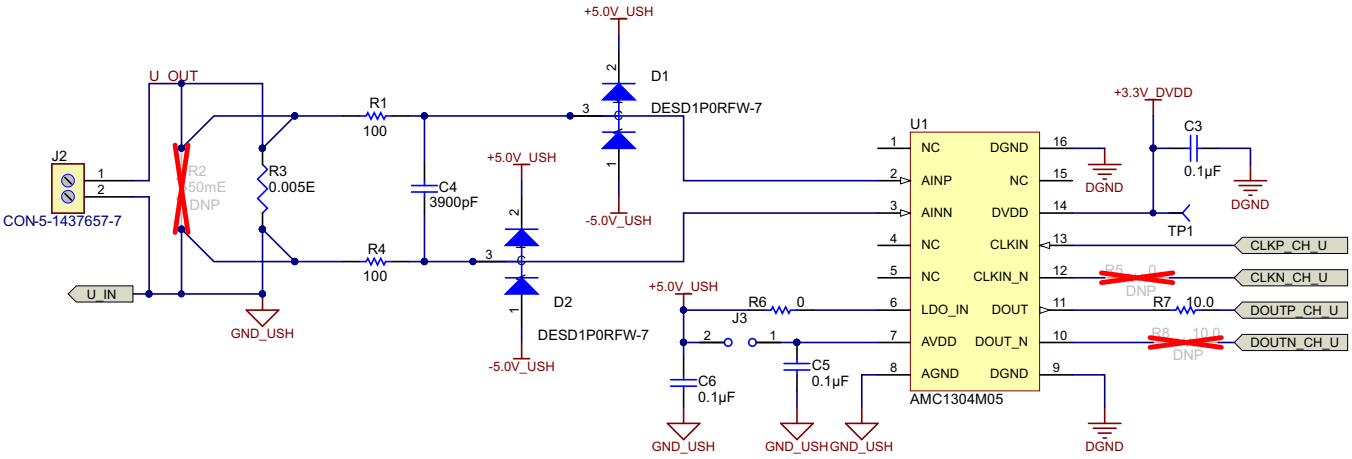


Figure 21. AMC1304 AC Interface

The shunt resistor value is selected based on the drive requirements. Consider a 0.55 kw / 3ø-230-V drive with a continuous output current of 3.5 A. Typically, the drives can deliver up to 200% overload for short durations, which necessitates measuring up to 7-A_{RMS}. For an AMC1304 50-mV part, the shunt value is calculated by Equation 13.

$$R_S = \frac{50\,mV}{7 \times 1.414} = 5m\Omega \tag{13}$$

Other criteria to consider while selecting the shunt resistor include:

- Resistor with sufficient power rating [in this example, 0.25 W(7^2*0.005)]
- Resistors having less change in nominal resistance value due to self-heating
- Low inductance resistors, good tolerance (<1%) and low temperature coefficient
- Two-terminal current-sense resistors for lower-cost applications
- Four-terminal current-sense resistors for higher-accuracy applications

The selected shunt is 5 mΩ, 5 W, 1%.

The footprint for the shunt provided on the board supports up to 10 W of power, which helps in scaling the measured current.

The RC filter provides the required low-pass filtering to improve the SNR. The TVS diodes DESD1P0RFW-7 clamp the transient pulses to typically 4 V. This voltage is safe for the AIN and AINN pins of the AMC.

In the event of a transient pulse, to have no or minimum impact on the 5.0 V_xx and –5.0 V_xx rails, have a sufficient value of decoupling capacitor placed on the corresponding planes to provide or absorb the sudden charge rush due to the clamping action of the diodes.

4.1.1.2 AMC1304M25 for DC Link Voltage Measurement—Signal Chain Design

DC link voltage needs to be measured for multiple functionalities like detection of under voltage, detection of over voltage, to turn on brake resistors, and to estimate inverter output voltage. Consider using an AMC1304 250-mV part for voltage measurements.

Considering the 200- to 240-V AC 3-phase input drive, the DC link voltage can be as high as 450 V. With a margin of an additional 100 V, the DC link measurement circuit should be able to read up to 550-V DC.

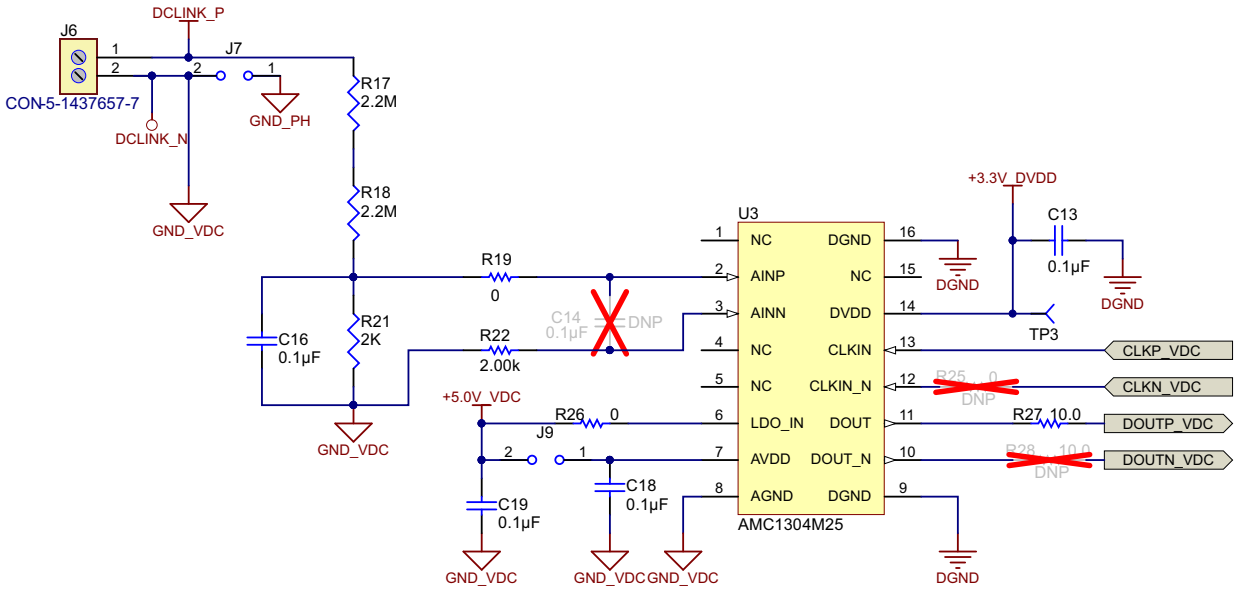
The resistor divider network is chosen so as to step down this 550-V DC to 250 mV. Assuming R21 = 2 K in Figure 22, the value of the divider network is calculated with Equation 14.

$$R = \left(\frac{V_{dc}}{250\,mV} - 1 \right) R21 \tag{14}$$

$$R = \left(\frac{550\,V}{250\,mV} - 1 \right) 2K\Omega = 4.4M\Omega \tag{15}$$

R17 and R18 are shown in Figure 22.

4.4 MΩ is split into two resistors of 2.2 MΩ, which can withstand up to 300-V DC.



The jumper (J7) needs to be disconnected to perform this measurement.

Figure 22. DC Link Measurement

AMC1304M25 is optimized for use with very low-impedance shunt resistors at its input. Use of signal sources with higher and miss-matched input impedance causes systematic offset and gain error due to input current.

Effect of Bias Current of AMC1304

AMC1304 contains PGA to gain input voltage and drive the modulator. An input bias current flows out of the input terminals due to resistive feedback network (R1, R2; approximately 31.25 µA each), which causes an offset voltage across the shunt resistor. This bias current is negligible for current measurements but starts playing a role for voltage measurements, creating an offset error. The effect of this bias current can be compensated by implementing an additional resistor (R22) in the negative signal path, which has the same value as R21.

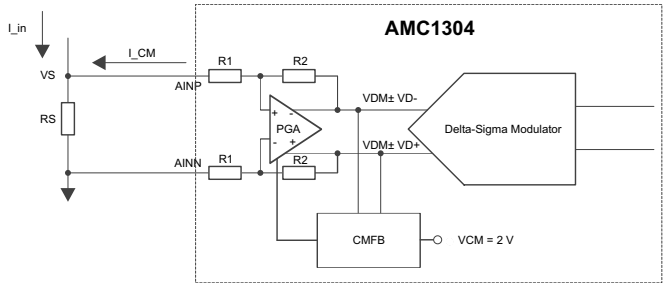


Figure 23. AMC1304 Input Block Diagram

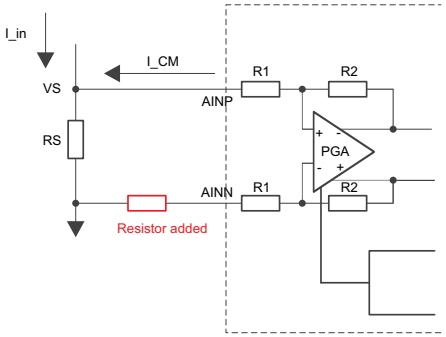


Figure 24. AMC1304 Input Offset Compensation Due to Bias Current

Effect of Input Impedance of AMC1304

AMC1304M25 input preamplifier contains a fully differential op-amp with a 50-kΩ feedback and 12.5-kΩ input resistors leading to 62.5 kΩ in total feedback. Because the negative input of the differential amplifier is grounded in the application through 2 kΩ, the input impedance seen is 12.5 kΩ. The 12.5-kΩ input impedence, in parallel with R21, leads to a gain error, which can be compensated for by using the correct value of resistor (2 kΩ || 12.5 kΩ) for voltage calculation.

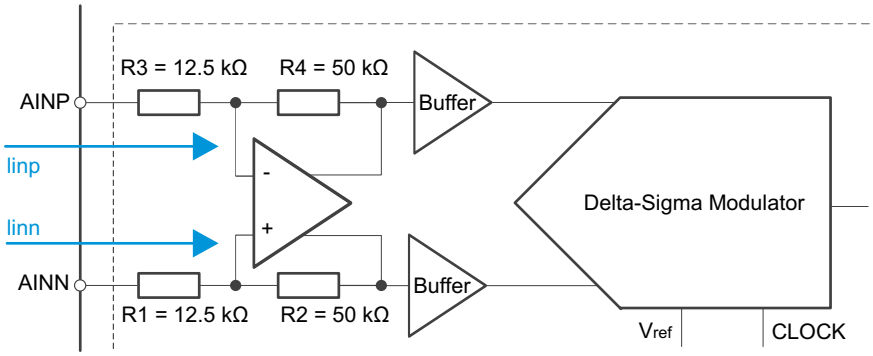


Figure 25. AMC1304 Input Amplifier

4.1.1.3 AMC1304M25 for AC Voltage Measurement—Signal Chain Design

The AMC1304M25 device is used for measuring AC voltages. This reference design can be used to measure phase-to-phase voltage or phase-to-DC_MINUS voltage measurement.

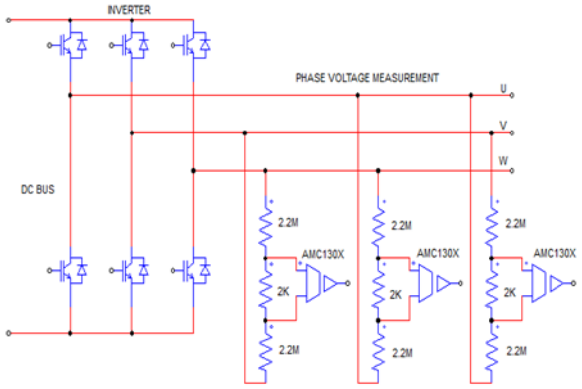


Figure 26. AMC1304 for Phase-to-Phase Voltage Measurement

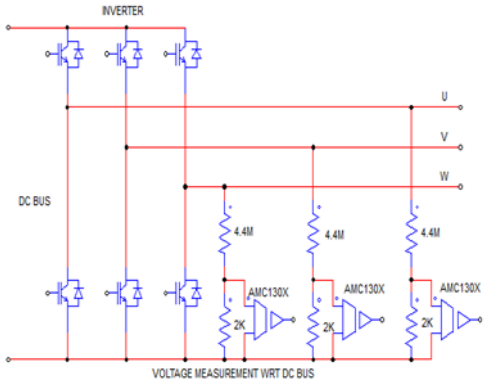


Figure 27. AMC1304 for Phase-to-DC_MINUS Voltage Measurement

The resistor divider network converts the AC voltage to a maximum of ±250 mV (peak). This reference design targets measurement of an RMS voltage of up to 390 V. The value of the component in the resistor divider network has been chosen so as to drop 390-V_{RMS} to 250 mV (peak).

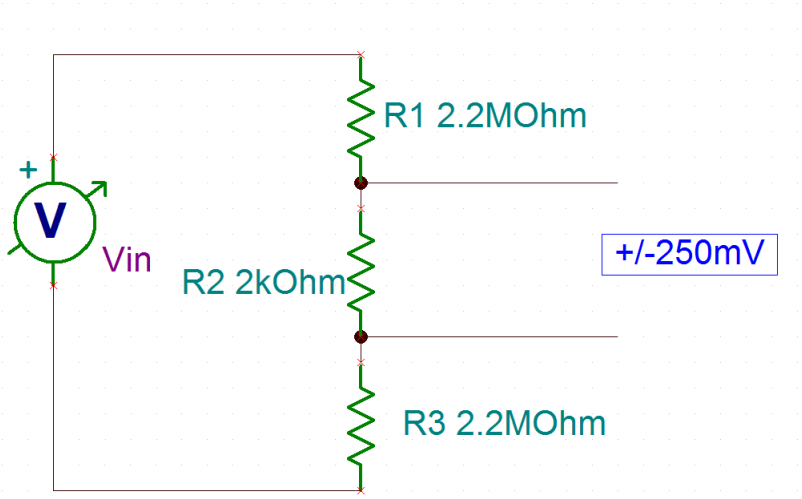


Figure 28. Phase-to-Phase Resistor Divider

$$R2 \times \frac{V_{IN}}{R1+R2+R3} = 250\,mV \tag{16}$$

Therefore, the values of R1, R2, and R3 are chosen to be

- R1 = R3 = 2.2 MΩ
- R2 = 2 kΩ

Phase-to-Phase Measurement

The phase-to-phase measurement can be done in any of the following ways:

1. *Direct Measurement:* The BOM for this reference design is, by default, configured for the direct differential phase-to-phase measurement.

Table 5. Direct Measurement Configuration

OPTIONAL COMPONENTS	CONNECTED
R57, R65, R81, R89, R105, R113	Yes
R67, R91, R107	No
R54, R78, R102	No
R63, R85, R109	No
R51, R75, R99	No
R59, R83, R107	No
R58, R82, R106	No

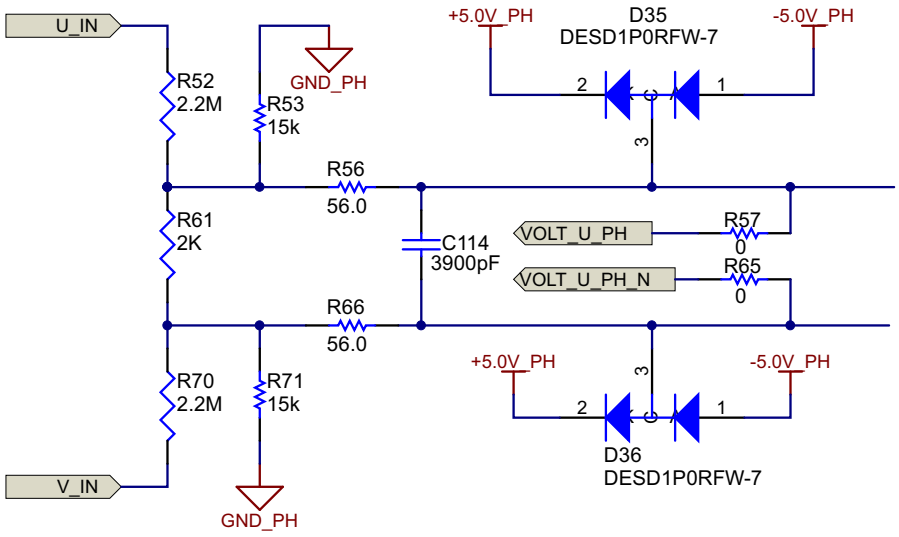


Figure 29. Phase-to-Phase AC Voltage Direct Measurement

The nets *VOLT_x_PH* and *VOLT_x_PH_N* are directly connected to the AMC1304M25 device. The internal impedance of AMC1304M25 (25 kΩ) would be in parallel with 2 kΩ, which needs to be considered while calculating the scale factor.

The 56-Ω and 25-kΩ internal to AMC1304 with 3.9 nF provide the low-pass filter with a –3-dB bandwidth at 22 kHz. Therefore, the PWM frequency from the motor drive will be attenuated accordingly. Based on the PWM frequency, this filter may be tuned further to improve the SNR of the measured voltage.

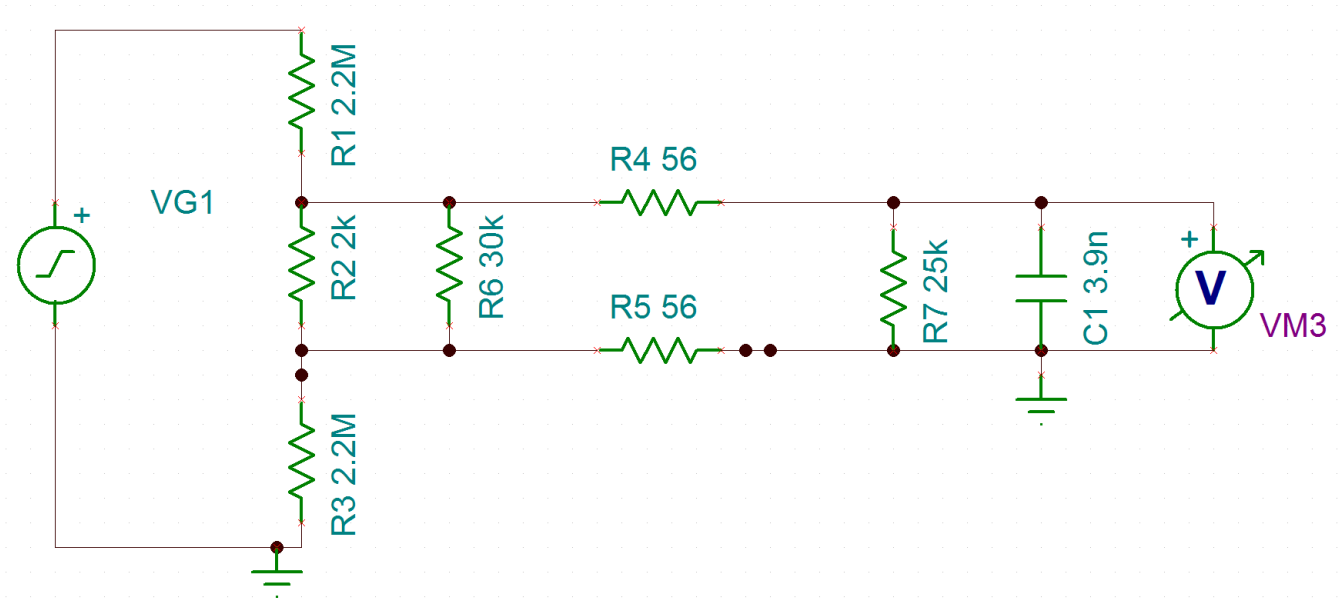


Figure 30. Direct Measurement Filter Simulation

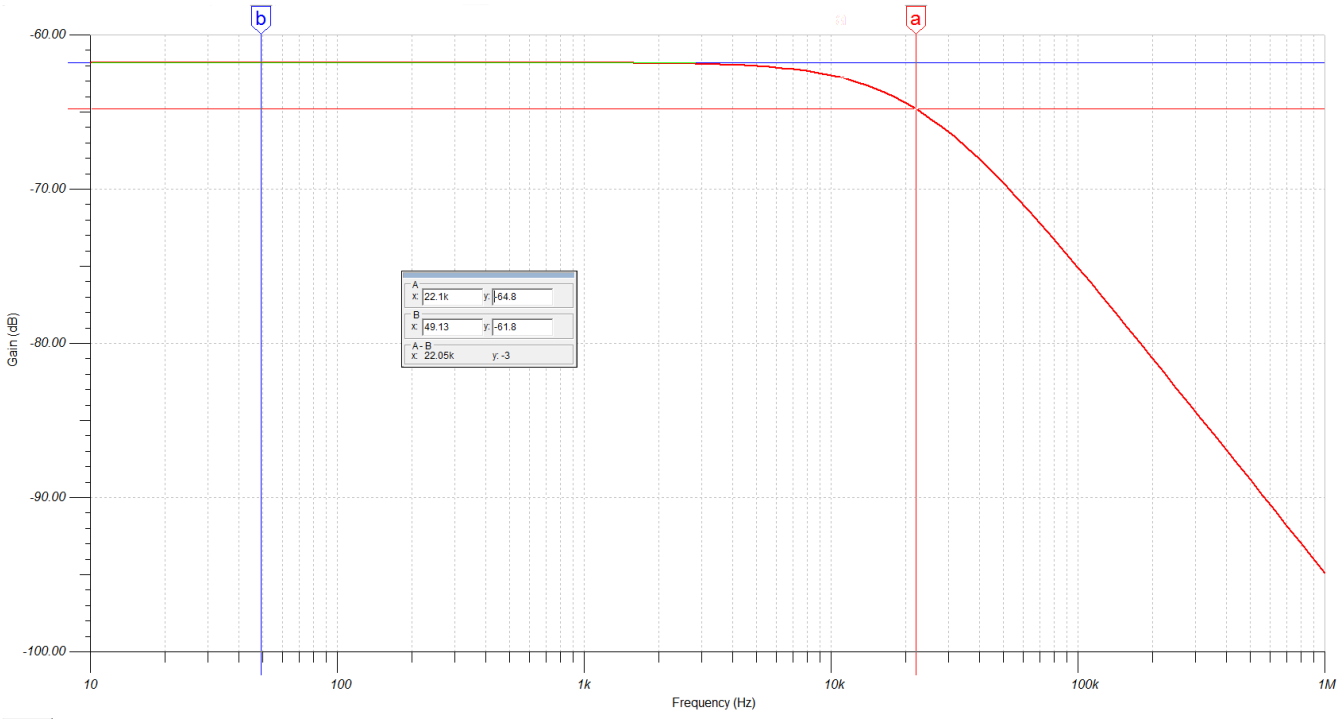


Figure 31. Simulation Results

2. *Measurement through In-Amp:* The in-amp provided on the board gains signals, gives a low impedance source to AMC130x, and acts as a high CMRR to the common mode noise. In many cases, an in-amp is not required and AMC130x can be directly connected to the resistive divider.

   To configure the circuit to use in-amps, follow the component modifications in Table 6:

Table 6. Circuit Modifications for In-Amp Use

OPTIONAL COMPONENTS	CONNECTED
R57, R65, R81, R89, R105, R113	No
R67, R91, R107	Yes
R54, R78, R102	Yes
R63, R85, R109	No
R51, R75, R99	No
R59, R83, R107	No
R58, R82, R106	No

3. *Measurement with Sallen-Key Filter:* The addition of a Sallen-Key filter after in-amp provides a further improvement in SNR. With a Sallen-Key based low-pass filter, the PWM frequency noise that passes by the in-amp is further attenuated. To make this configuration, the following component modifications are needed:

Table 7. Component Modifications for Sallen-Key Measuring

OPTIONAL COMPONENTS	CONNECTED
R57, R65, R81, R89, R105, R113	No
R67, R91, R107	Yes
R54, R78, R102	No
R63, R85, R109	Yes
R51, R75, R99	No
R59, R83, R107	Yes
R58, R82, R106	No

Phase-to-DC_MINUS Measurement

This reference design allows an option for performing a phase-to-DC_MINUS voltage measurement. This reference design targets to measure an RMS voltage of 390 V. The input impedance of the AMC1304M25 in this configuration is 12.5 kΩ, and the scale factor needs to be calculated accordingly.

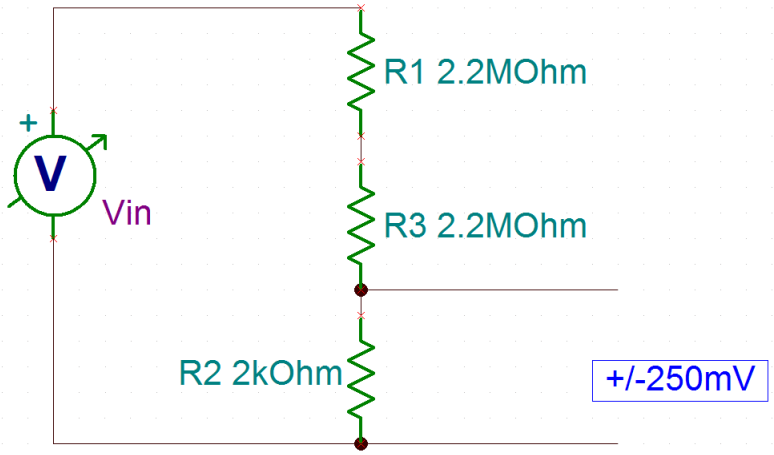


Figure 32. Phase-to-DC_MINUS Resistor Divider

$$R2 \times \frac{V_{IN}}{R1+R2+R3} = 250\,mV \quad (17)$$

To make this configuration, follow these component modifications:

Table 8. Component Modifications to Use Phase-to-DC_MINUS Resistor Divider

OPTIONAL COMPONENTS	CONNECTED
R57, R65, R81, R89, R105, R113	No
R67, R91, R107	Yes
R54, R78, R102	No
R63, R85, R109	No
R51, R75, R99	Yes
R59, R83, R107	Yes
R58, R82, R106	No

By providing the Sallen-Key based active filter, the board gets an attenuation of up to and beyond 3 dB for PWM frequencies of 20 kHz. The attenuation versus frequencies is shown in the TINA-TI-V9 simulation (Figure 33 and Figure 34).

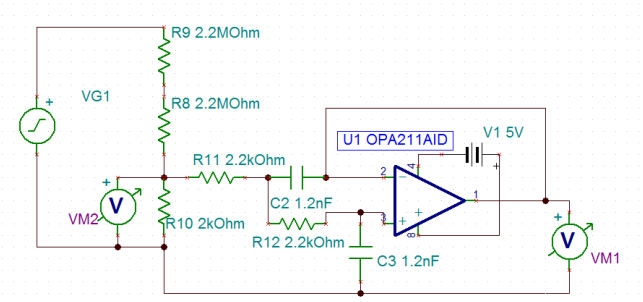


Figure 33. Phase-to-DC_MINUS Sallen-Key Simulation

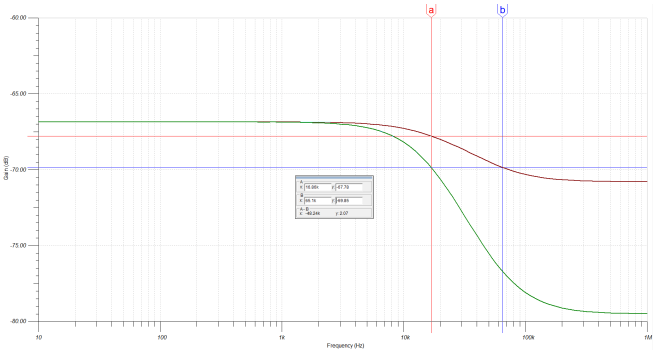


Figure 34. Simulation Results

NOTE: Connect Jumper J7 before setting up this configuration.

4.1.2 Isolated Power Supply

AMC130x has reinforced isolation. Therefore, the power for high-side (AVDD) and low-side (DVDD) sections need to be isolated.

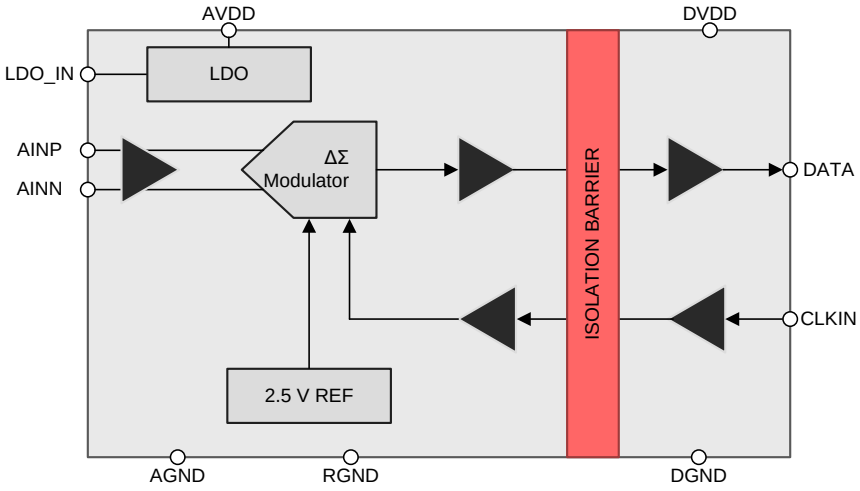


Figure 35. Block Diagram for AMC1304

The AVDD for the device can be derived from the power supply of the upper-gate driver or through a dedicated reinforced isolated power supply. The AMC1304 device has a built-in LDO, which can be fed directly with a gate-drive supply voltage up to 18 V. AMC1305 does not have inbuilt LDO, and the power for it can be derived by using simple external Zener diode or with an LDO.

The evaluation module has three current channels and four voltage channels. Power supplies for the entire current channel are isolated from each other. Voltage channels used for inverter-voltage measurement share one common power supply, and the DC link voltage measurement section has its own power supply. The SN6501 Transformer Driver is used to generate isolated power supplies. SN6501 converts the 5-V input from the control board to isolated 6 V and –6 V.

The SN6501 is a monolithic oscillator and power-driver, specifically designed for small form factor, isolated power supplies in isolated interface applications. The SN6501 drives a low-profile, center-tapped transformer primary from a 5-V DC power supply. A transformer with a 1:64:1 turns ratio is used in the design to obtain ±6 V.

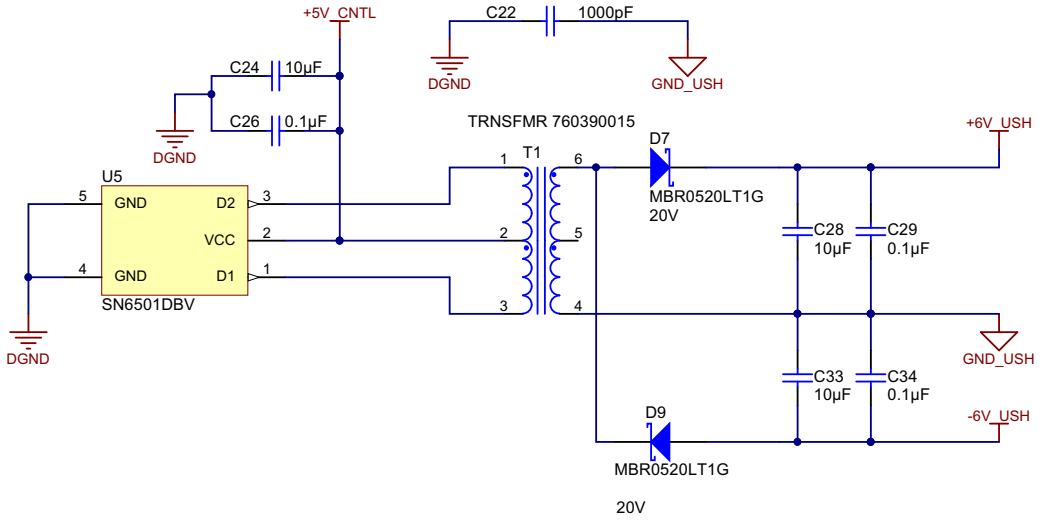


Figure 36. SN6501-Based Power Isolation

TLV70450DBV, an ultra-low I_q, high V_{IN} low-dropout regulator (LDO), is used to convert 6 V to the 5 V required for the modulator operation. Provision has been made to feed this regulator from gate-drive power supply through J13.

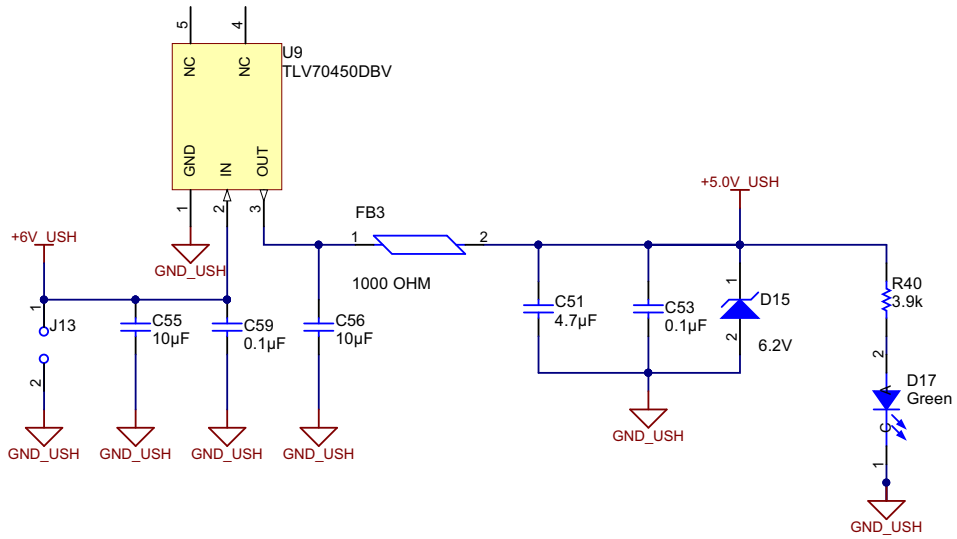


Figure 37. 5-V LDO

TPS7A3001DGNR, a negative, high-voltage, ultra-low-noise linear regulator, is used to convert the –6 V to –5 V. This supply is used only for protection purposes, and the modulator does not need this supply for its operation.

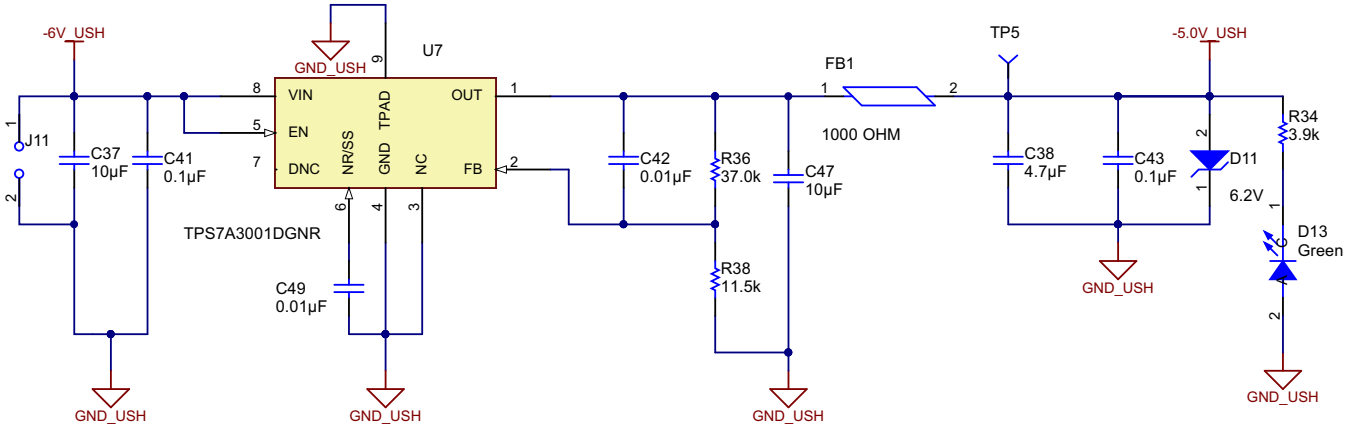
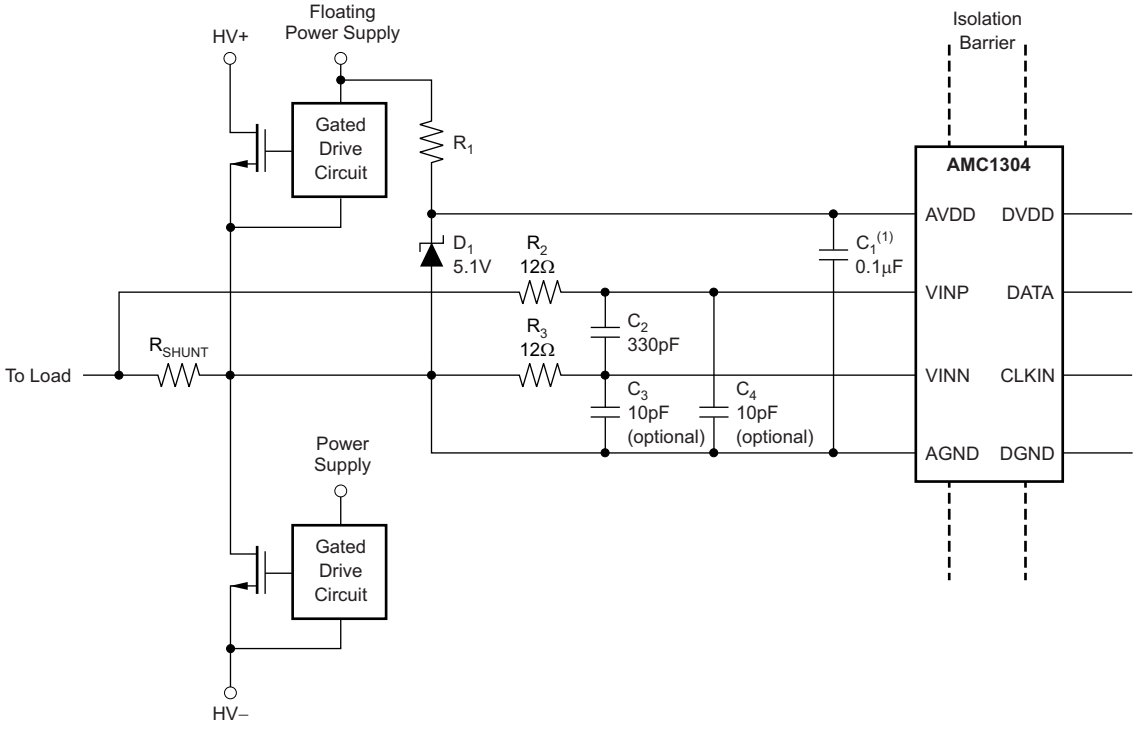


Figure 38. –5V LDO

For the lowest cost, a Zener diode can be used to limit the voltage to 5 V at ±10%. Use a decoupling capacitor of 0.1 µF for filtering this power-supply path. This capacitor (C1) should be placed as close as possible to the AVDD pin for best performance. If better filtering is required, an additional 1-µF to 10-µF capacitor can be used. The floating ground reference (AGND) is derived from the end of the shunt resistor, which is connected to the negative input (VINN) of the device.

Alternatively, Figure 39 shows AMC1304 biasing from power supply to gate-drive power supply. This method can be used if three individual gate-drive power supplies are already present in the application.



(1) Place C_1 close to the AMC1304

Figure 39. AMC1304 Biasing from Gate-Drive Power Supply

4.1.3 Connectors

4.1.3.1 Input Terminal Connectors

The terminal connectors for U, V, W, and DC link interface are J2, J4, J8, and J6, respectively.

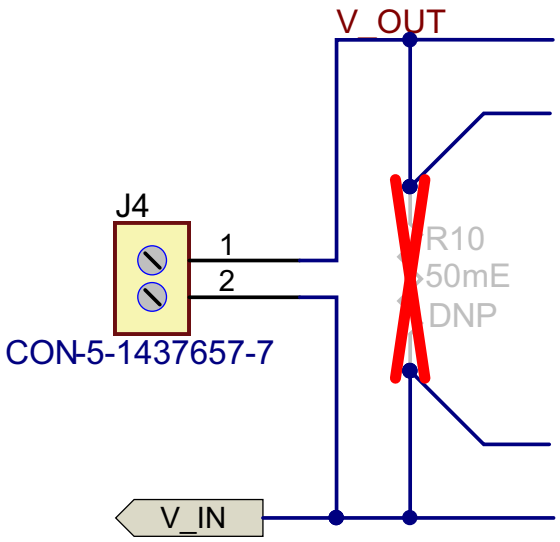


Figure 40. Terminal Connector

Current Measurement Connections

The U, V, and W phases should be connected to the motor windings through the connectors at J2, J4, and J8, respectively.

AC Voltage Measurement

- Phase-to-phase measurement: The 3-phase wire should be connected as:
  - J2-2 for looping in U.
  - J4-2 for looping in V.
  - J8-2 for looping in W.
- Phase-to-DC_MINUS measurement: The 3-phase and DC_MINUS wire should be connected as:
  - J2-2 for U
  - J4-2 for V
  - J8-2 for W
  - J6-2 for DC_MINUS

NOTE: Connect Jumper (J7) in this configuration.

DC Voltage Measurement

- The DC link voltage provided to the invertor should be connected as:
  - J6-1 for DC link
  - J6-2 for DC_MINUS

NOTE: Disconnect Jumper (J7) in this configuration.

4.1.3.2 Board-to-Board Connector

The 40-pin interface connector consists of:

- Differential or single-ended clock for all seven modulators
- Differential or single-ended DOUT signal from the seven modulators
- 3.3 V for operation of digital-side functioning of seven modulators
- 5 V to generate an isolated 5 V and –5 V for isolated modulator operation and protection

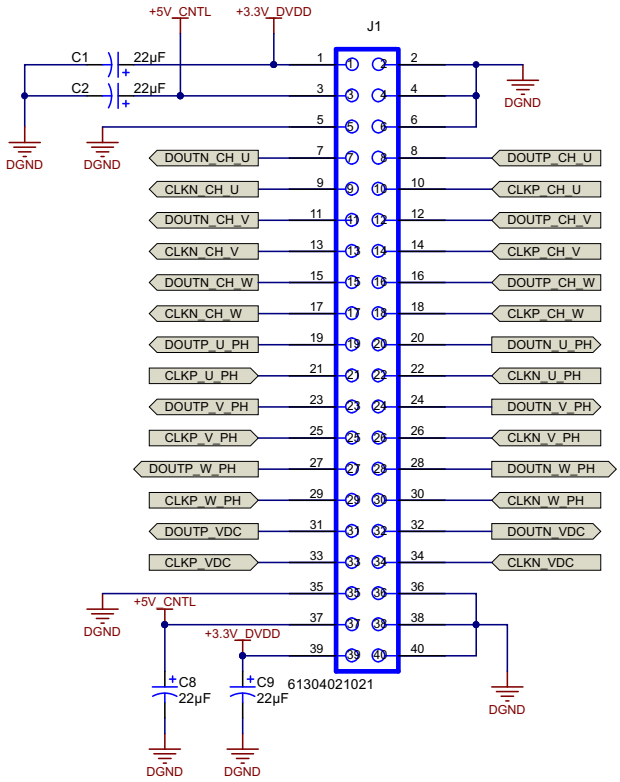


Figure 41. Board-to-Board Connector

4.2 FMB

The FMB acts as a base board to house the Delfino control card along with a power supply circuit.

4.2.1 Input Polarity Protection

The DC input to the Isolated Current Shunt and Voltage Measurement Kit is protected against any accidental wrong wiring. The diode (D23) provides this polarity protection with a peak-current capability of 4 A. Due to the input capacitors of close to 125 µF, the inrush current can be high initially for milliseconds, limited only by the 24-V DC bus and source impedance.

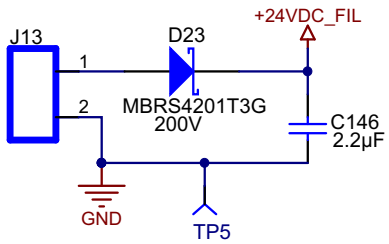


Figure 42. Input Polarity Protection

4.2.2 24- to 6-V DC Flyback Convertor

In practical Industrial conditions, the 24-V DC can vary up to ±20%, so the DC-DC convertor IC chosen for this reference design is the TPS55340 device, which has a maximum continuous-input voltage of 32 V. The switching frequency is externally set at a nominal 350 kHz. The 40-V, 5-A, low-side MOSFET is incorporated inside the TPS55340 package along with the gate-drive circuitry. The low drain-to-source on resistance of the MOSFET allows the TPS55340 to achieve high efficiencies. The compensation components are external to the integrated circuit.

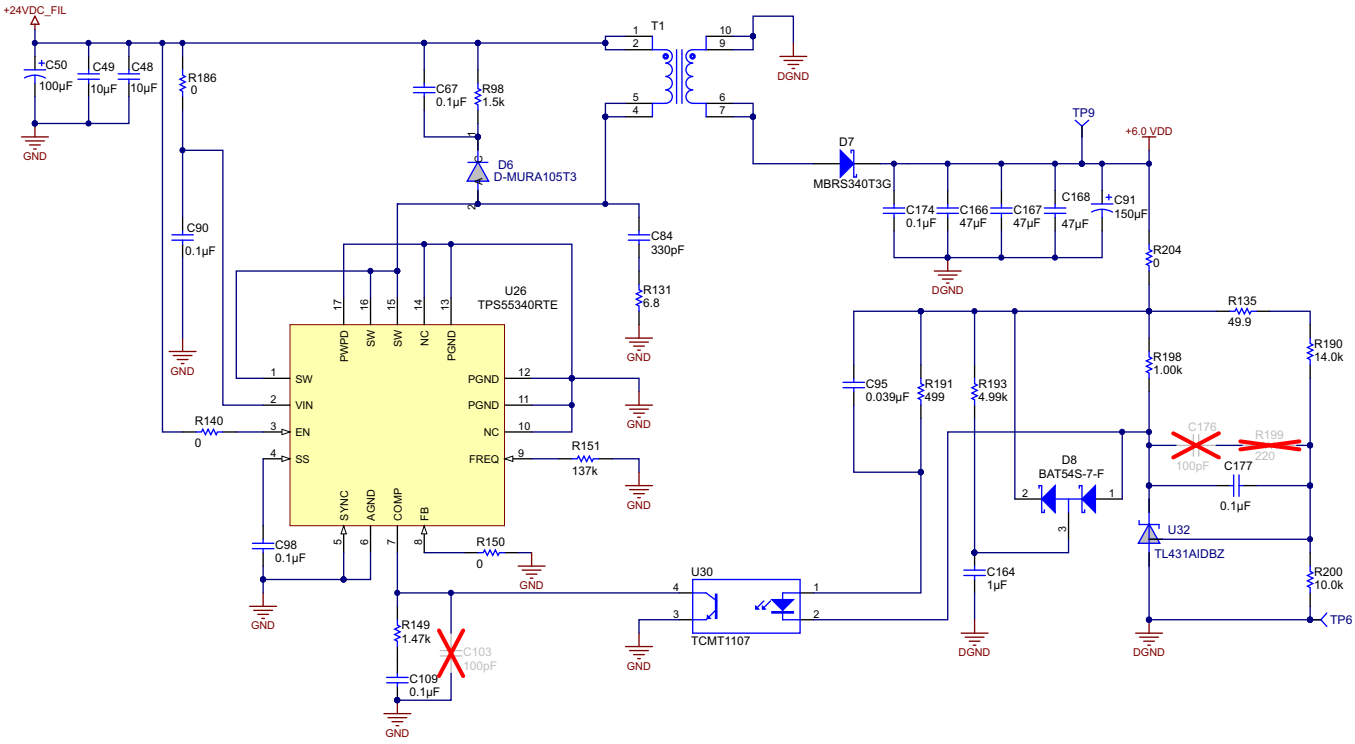


Figure 43. 24-V DC to 6-V DC Flyback Convertor

Output Voltage Selection

The output voltage required is 6 V. So, using TL431 and V_{ref} as 2.495 V, the values of R190 and R200 are selected as 14 kΩ and 10 kΩ, respectively.

$$R190 = R200 x \left(\frac{V_{out}}{V_{ref}} \right) - 1$$

where

- V_{out} = 6 V
- V_{ref} = 2.495 V (18)

Set the Switching Frequency

The resistance of R151 has to be calculated for desired switching frequency.

$$R_{FREQ}(k\Omega) = 57500 \times fsw(kHz) - 1.03$$

where

- fsw = 350KHz

therefore,

- R151 = 137 kΩ (19)

Efficiency

The efficiency of this design peaks at a load current of about 1.5 A at 24 V input, then decreases as the load current increases toward full load. Figure 44 shows the efficiency in general and Figure 45 shows the light-load efficiency by using a semi-log scale.

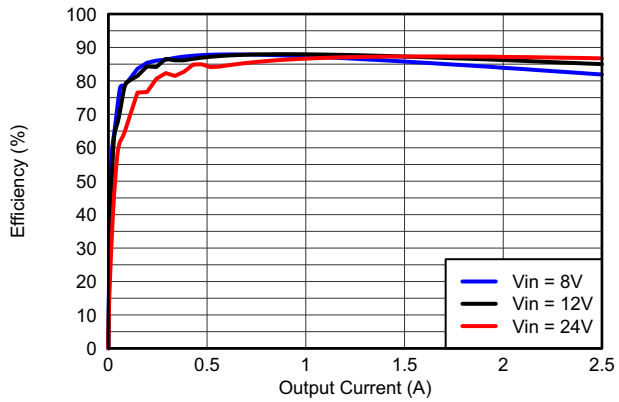


Figure 44. Efficiency

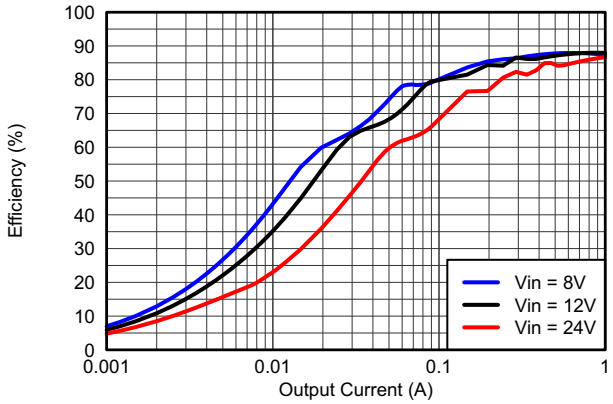


Figure 45. Light Load Efficiency

4.2.3 6- to 3.3-V Switching Regulator

The 3.3 V is generated by this step-down convertor based on the TPS54232 device. The 3.3 V is required for the PLL synthesizer CDCE906 device. Further, there is an option for up to 385 mA of expansion. This is useful if the user wants to interface another 3.3-V operated host controller.

The switching frequency is internally set at a nominal 1000 KHz. The high-side MOSFET is incorporated inside the TPS54232 package along with the gate-drive circuitry. The low drain-to-source on resistance of the MOSFET allows the TPS54232 to achieve high efficiencies and helps keep the junction temperature low at high output currents. The compensation components are external to the integrated circuit (IC), and an external divider allows for an adjustable output voltage. Additionally, the TPS54232 provides adjustable slow start and under-voltage lockout inputs.

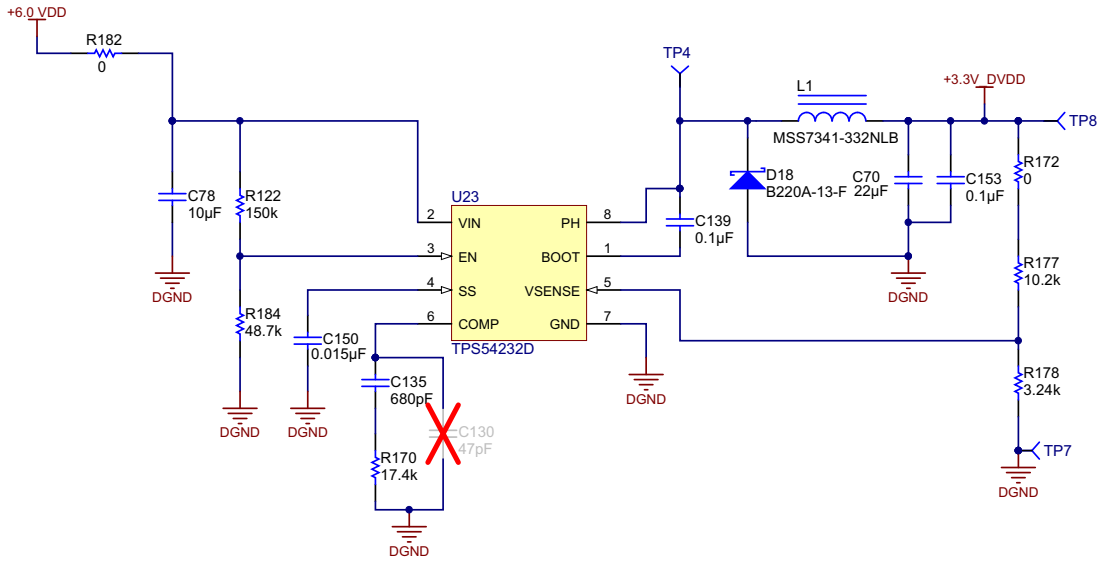


Figure 46. 6- to 3.3-V Step Down Convertor

4.2.4 Reference Voltages

The V_{ref} voltages are provided as a stable and noiseless voltage references for the analog circuits.

4.2.4.1 1.2 V_{ref}

The 1.2 V_{ref} is to provide a stable reference to the op-amp based filter circuits as shown in Figure 46. The REF3012 is a precision low-power, low-voltage dropout voltage reference in a SOT23-3 package. Other key specifications include:

- High accuracy: 0.2%
- Low Drift: 75 PPM/C from –75°C to 125°C
- High output current: 25 mA

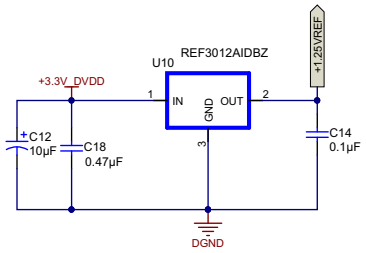


Figure 47. 1.2 V_{ref}

4.2.4.2 4.096 V_{ref}

The 4.096 V_{ref} provides a stable external voltage reference to the DAC8564. This is provided as an option, if the user needs a DAC output of maximum 4 V. The DAC8564 has an interval V_{ref} of 2.5 V; therefore, with an internal V_{ref} activated, the maximum DAC output shall be 2.5 V.

The REF3040 is a precision low-power, low-voltage dropout voltage reference in a SOT23-3 package.

Other key specifications include:

- High accuracy: 0.2%
- Low Drift: 75 PPM/C from –75°C to 125°C
- High output current: 25 mA

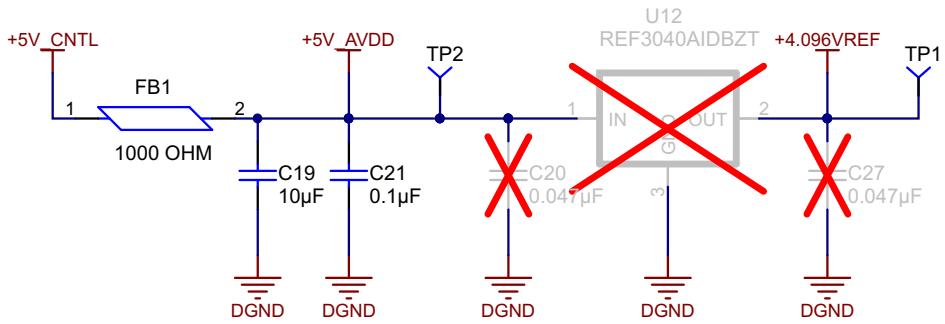


Figure 48. 4.096 V_{ref}

4.2.5 PLL Synthesizer CDCE906-Based Programmable Clock

The CDCE906 device is one of the smallest and most powerful PLL synthesizer/multiplier/divider available today. Despite its small physical outlines, the CDCE906 is the most flexible. It has the capability to produce an almost independent output frequency from a given input frequency.

The input frequency can be derived from a LVCMOS, a differential input clock, or a single crystal. The appropriate input waveform can be selected through the SMBus data interface controller.

To achieve an independent output frequency, the reference divider (M) and the feedback divider (N) for each PLL can be set to values from 1 up to 511 for the M-Divider and from 1 up to 4095 for the N-Divider. The PLL-VCO (voltage controlled oscillator) frequency is then routed from the free, programmable output-switching matrix to any of the six outputs. The switching matrix includes an additional 7-bit post-divider (1-to-127) and an inverting logic for each output.

The deep M/N divider ratio allows the generation of zero ppm clocks from, for example, a 27-MHz reference input frequency.

The CDCE906 device includes three PLLs. Of the three PLLs, one supports SSC (spread-spectrum clocking). PLL1, PLL2, and PLL3 are designed for frequencies up to 300 MHz and optimized for zero-ppm applications with wide divider factors.

PLL2 also supports center-spread and down-spread spectrum clocking (SSC). This is a proven method to effectively reduce the energy for the selected frequency range. The electro-magnetic interference (EMI) will be significantly reduced. Also, the slew-rate controllable (SRC) output edges minimize EMI noise. Based on the PLL frequency and the divider settings, the internal loop filter components will be automatically adjusted to achieve high stability and optimized jitter-transfer characteristic of the PLL.

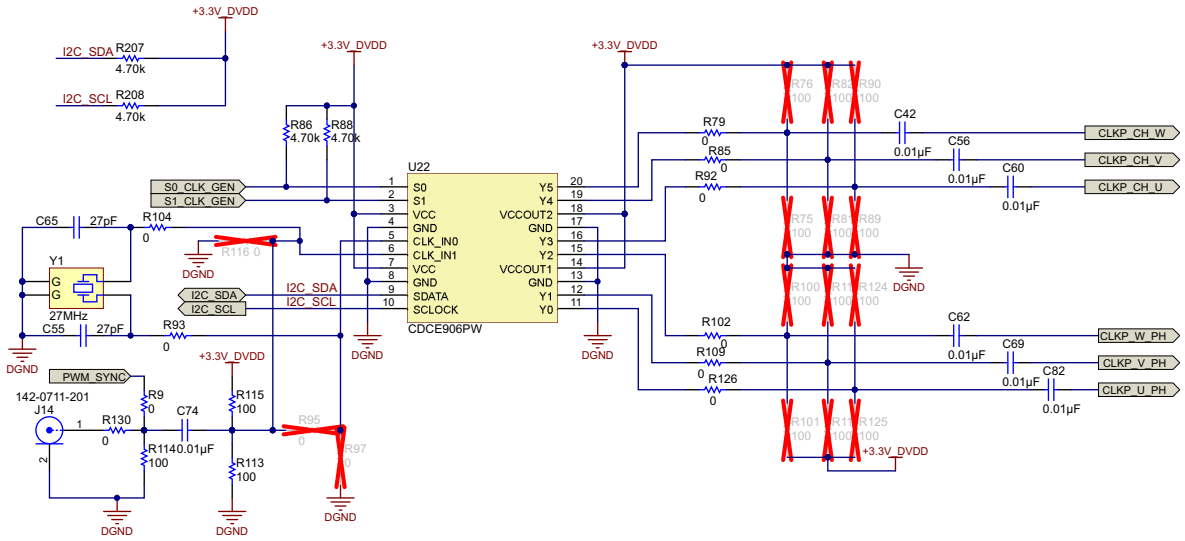


Figure 49. PLL Generation

In this reference design, the PLL is used to generate the reference clock for AMC1304. When the clock rate is higher, the higher the OSR; therefore, the accuracy is better. The AMC can operate at a maximum of 20.1 MHz.

4.2.6 DAC8564

The two DAC8564 devices provide a provision to replicate the analog input signal to the AMC1304 device.

DAC8564 is a 16-bit, high-resolution, quad-channel, and serial-input DAC with a built-in 2.5-V internal reference that is enabled by default. This DAC has a serial interface to communicate with the host microprocessor.

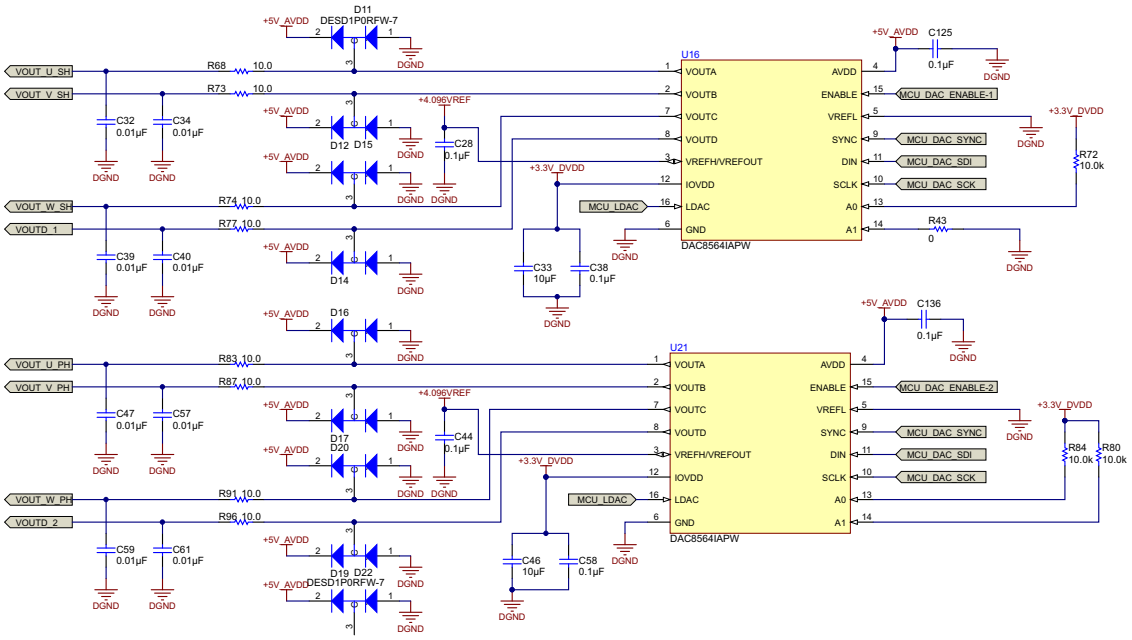


Figure 50. 16-Bit DAC Output

4.2.7 Amplifiers and Filters

This reference design features an amplifier and filter section to provide an option to interface the digital bit stream from each AMC1304 device to an SAR ADC.

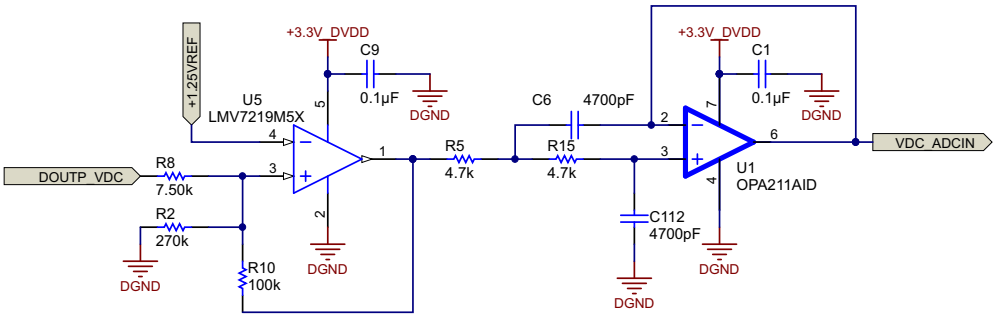


Figure 51. Amplifier and Sallen-Key Filter

4.2.8 Connectors

The FMB is provided with connectors to interface the 24-V DC input, Delfino control card, and DSM. There are more connectors to provide diagnostics functionality.

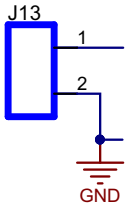


Figure 52. 24-V DC Input

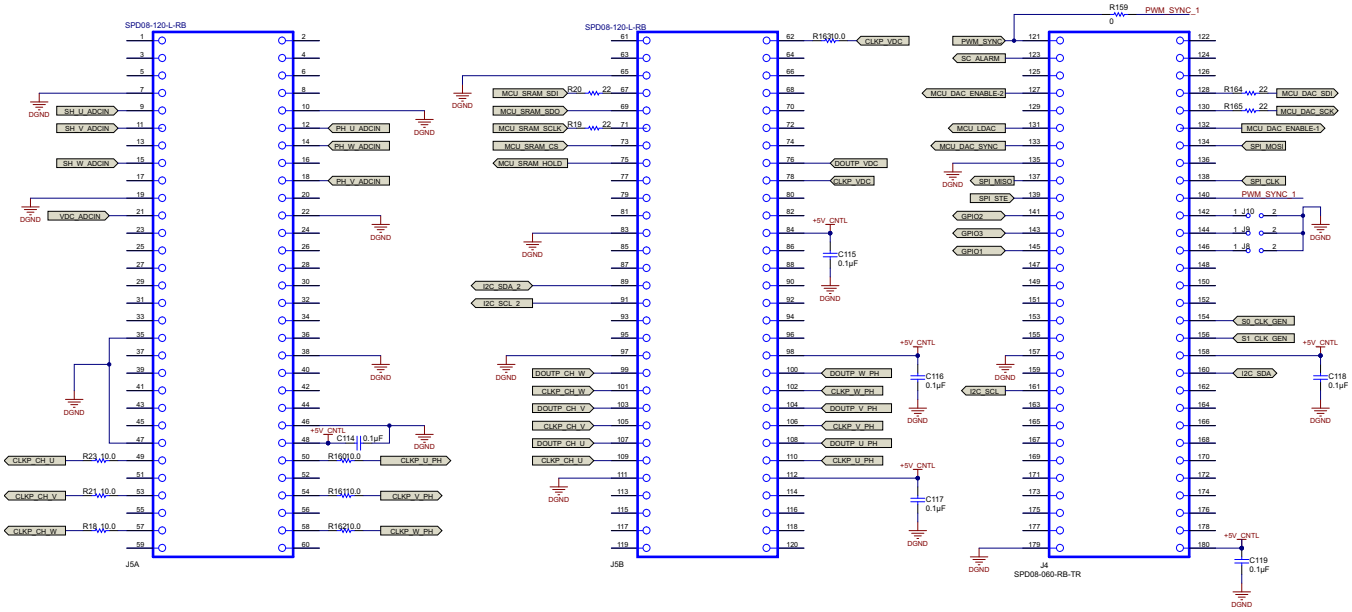


Figure 53. 120- and 60-Pin Connector to Delfino Base Control Card

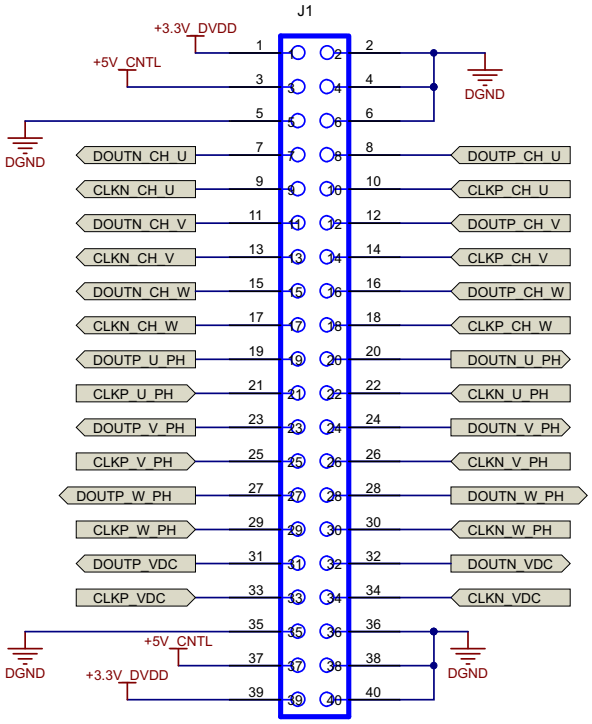


Figure 54. 2×20-Pin Connector to DSM Board

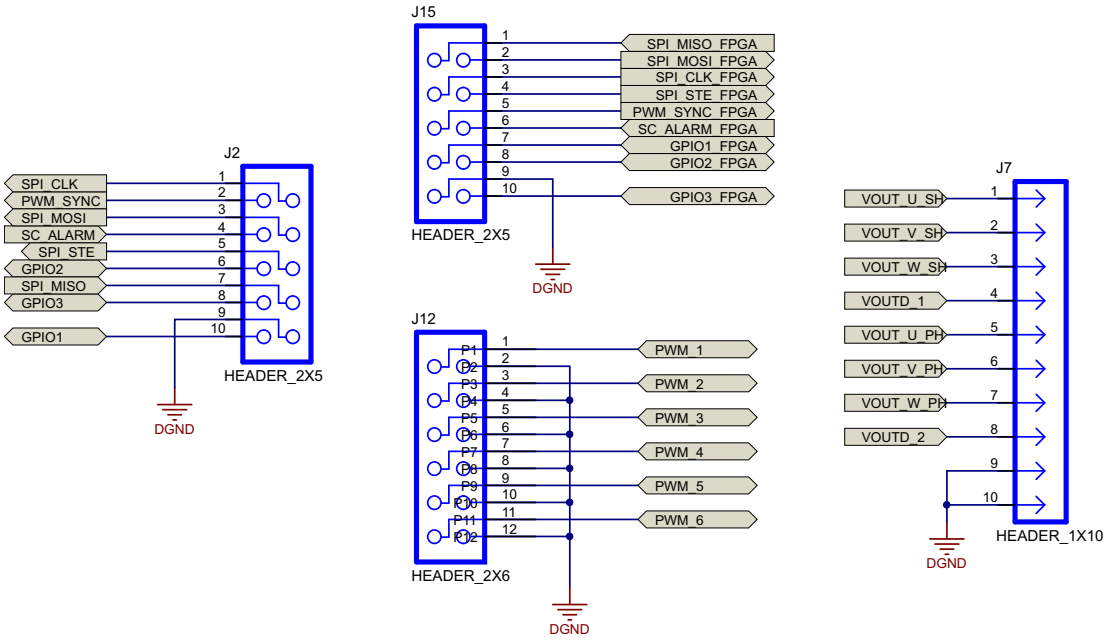


Figure 55. Miscellaneous Connectors: DAC, JTAG

4.3 Delfino Control Card

The microcontroller on the Delfino-based control card board is TMS320F28377D, a dual-core Delfino of the C2000 family of microcontrollers. Figure 56 gives an overview of the device and integrated peripherals.

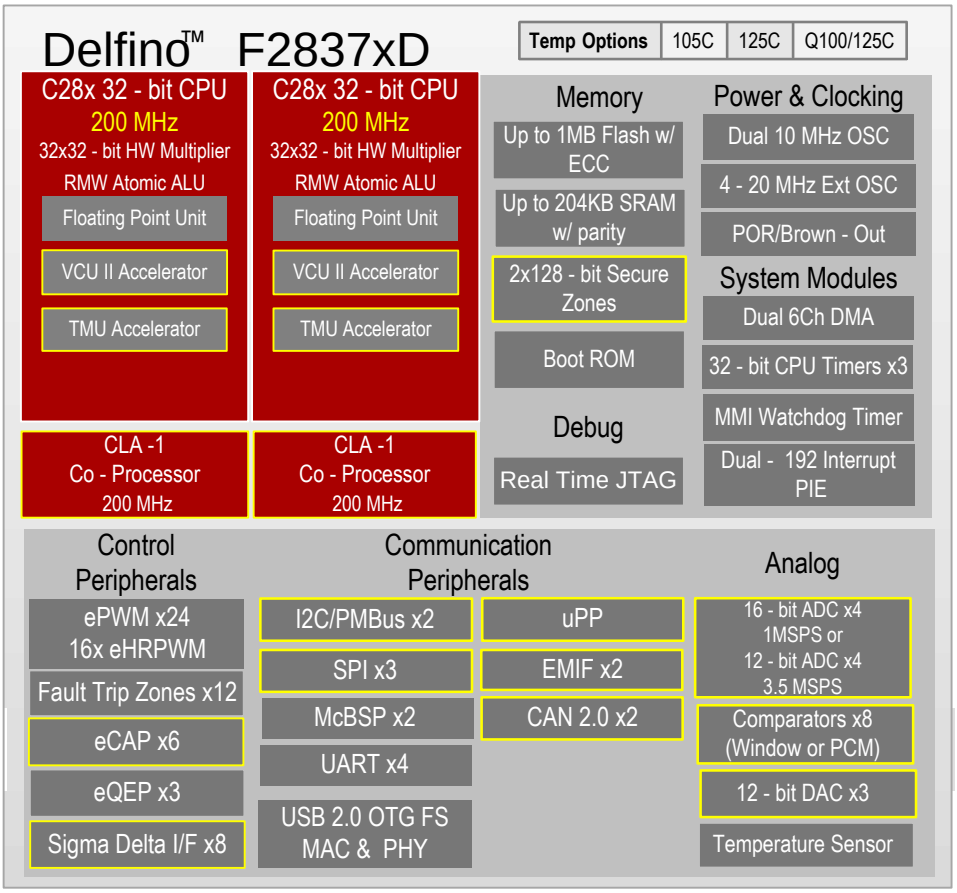


Figure 56. TMS320F28377D Overview

Table 9 lists the peripherals used on the controller and the master allocated to the peripheral.

Table 9. List of Peripherals

MCU RESOURCE	MASTER CPU	USED FOR
Sigma-Delta Filter Modules (SDFM1 and SDFM2)	CPU1	Interface with AMC1304
USB	CPU1	Interface with PC GUI
ePWM8	CPU1	Generates clock for the AMC1304, interfaced on the third channel of the SDFM2
ePWM1, ePWM2, ePWM3, ePWM4, ePWM5, ePWM7	CPU1	Optional clock source for other AMC1304 interfaced on SDFM1 and ADFM2(1)
SPI-B	CPU2	Interface with DAC8564
SPI-C	CPU2	Interface to external controller
I^2C-A	CPU1	Interface with CDCE906 PLL synthesizer

(1) Indicates resource allocated on the hardware, not used for GUI firmware.

4.3.1 SDFM Peripheral

The controller has two integrated Sigma-Delta Filter Modules (SDFM1, SDFM2). Each SDFM module supports four channels of delta-sigma demodulation. The eight channels available on the controller are used for sampling three current inputs, three voltage inputs, and one DC link voltage monitoring.

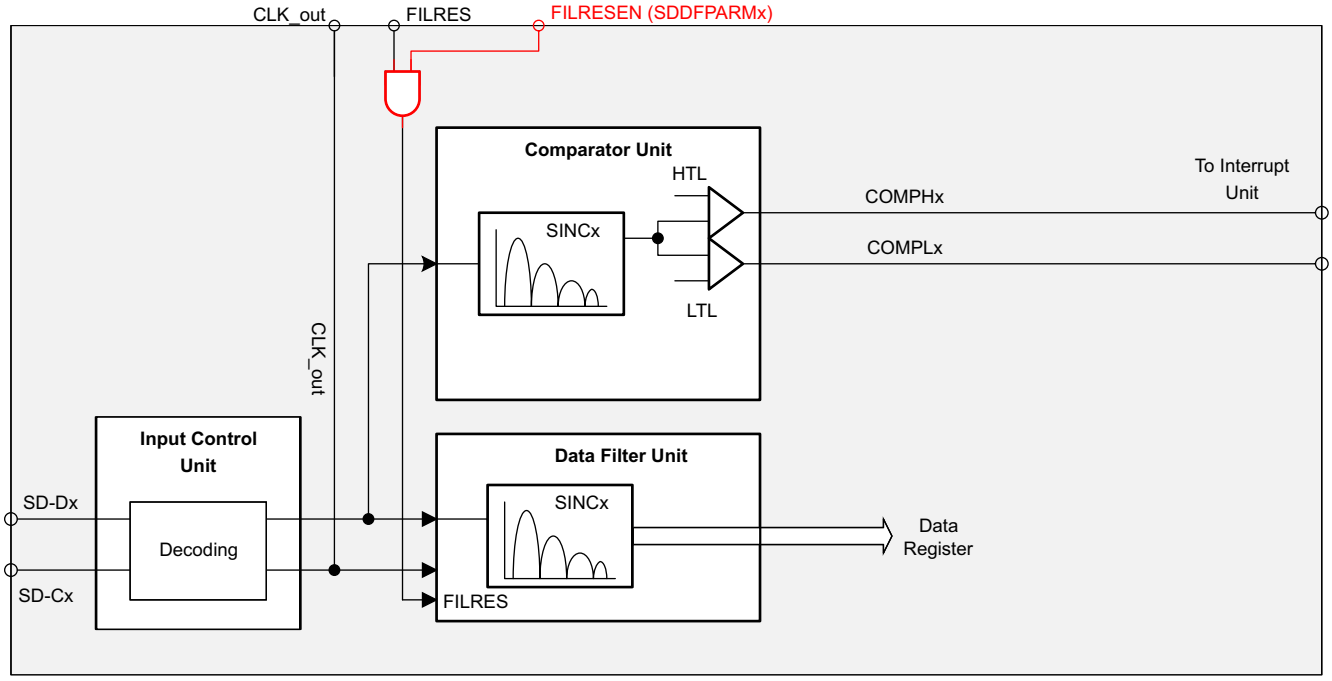


Figure 57. Block Diagram of One Filter Module

Figure 57 shows filter module for one channel available in the SDFM. Each SDFM peripheral has four filter modules. The main sub-modules within the SDFM are the data-filter unit, input-control unit, and the comparator unit. Refer to the TMS320F28377D TRM to learn more about the different blocks in the peripheral device.

The input-control block supports different types of bit stream. The input-control block supports bit streams, which may operate at the same rate as the clock input, twice the clock input, half the clock-input rate, or Manchester encoded bit streams. AMC1304 gives a data rate equal to the clock input. The required configuration for input-control bocks in modulator mode is Mode 0.

The data-filter unit implements Sinc filters in hardware; this converts the bit stream. The conversion result is obtained in the result registers. The data filter unit supports $Sinc^1$, $Sinc^2$, $Sinc^3$, and Sincfast filter structures with OSR of 1 to 256. GUI provides features to set modulator and Sinc structures as required.

Sampling rate of the filter is given as Equation 20.

$$f_{DATA}\,(\text{Sinc filter output rate}) = \frac{\text{Modular data rate}}{\text{SOSR}} \tag{20}$$

NOTE: SOSR: over sampling rate of the Sinc filter

In a motor drive application the minimum requirement is to have one sample with in one gate-drive PWM period, or one sample every alternating PWM period. The application can also require more than two samples per PWM period. Table 10 lists gate-drive switching frequency and some examples of sampling frequency with respect to the clock and OSR settings.

Table 10. Standard Motor Drive Switching Frequency with Respect to Sampling Rate for Required OSR Settings and Clock Inputs

GATE-DRIVE SWITCHING FREQUENCY	SAMPLING RATE	CLOCK FREQUENCY	OSR
10 kHz	20 Ksps	5.120 MHz	256
16 kHz	32 Ksps	8.192 MHz	256

The Sinc filter unit output register is 32 bits wide, and a 16-bit mode is provided and is used. The 16-bit mode the output, which is 32 bits, is right-shifted to a 16-bit representation in the complement of two. The SH filed in SDFIPARM is used to control the right-shift operation during the conversion. The position of the MSb in 32-bit mode depends on the filter structure and the OSR. When obtaining the 16-bit data, set SH to a value to obtain the MSB of the data in the MSB of the register.

Data-bit width depends on the Sinc structure and the OSR. Table 11 shows the result range. $Sinc^3$ filter types with a maximum OSR of 256 provides a resolution of 24 bits. $Sinc^3$ and 256 OSR provided the best resolution.

Table 11. Peak Data Values for Different DOSR/Filter Combinations

DOSR	$Sinc^1$	$Sinc^2$	$Sinc^3$	Sincfast
x	x	x^2	x^3	$2x^2$
4	–4 to 4	–16 to 16	–64 to 64	–32 to 32
8	–8 to 8	–64 to 64	–512 to 512	–128 to 128
16	–16 to 16	–256 to 256	–4096 to 4096	–512 to 512
32	–32 to 32	–1024 to 1024	–32,768 to 32,768	–2048 to 2048
64	–64 to 64	–4096 to 4096	–262,144 to 262,144	–8192 to 8192
128	–128 to 128	–16,384 to 16.384	–2,097,152 to 2,097,152	–32,768 to 32,768
256	–256 to 256	–65,536 to 35,536	–16,177,216 to 16,177,216	–131,072 to 131,072

The modulator frequency is chosen as 2 × Inverter switching frequency × OSR.

The frequency response of the filter structure is given in Figure 58. Notice that Sinc^3 provides higher attenuation and higher noise rejection. Therefore, a Sinc^3 filter is best suited for accuracy.

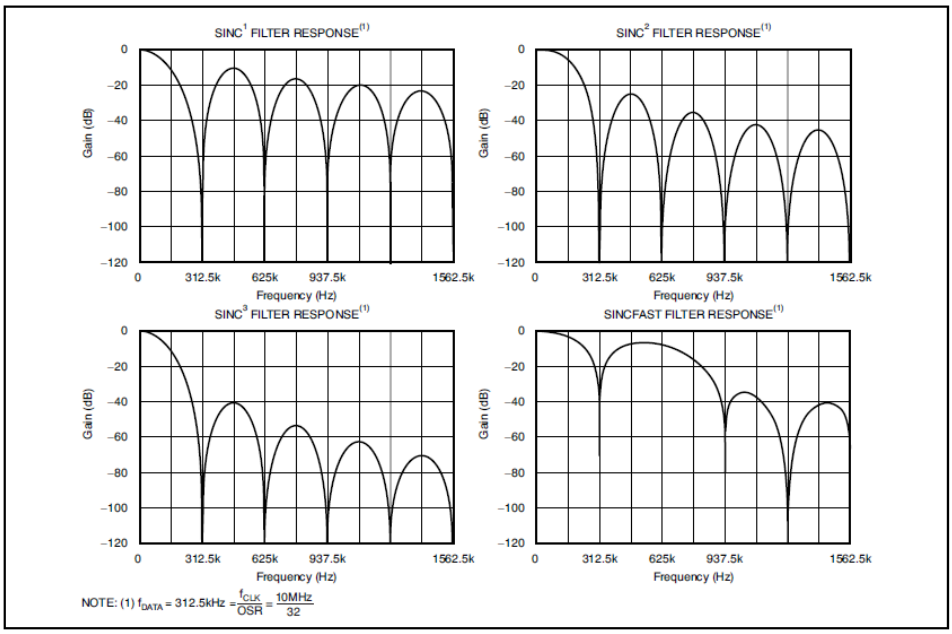


Figure 58. Frequency Response of Various Sinc Filters

The comparator unit implements a second Sinc filter. The conversion result digitally compared to threshold values in the threshold registers (SDFCMPHx and SDFCMPLx registers). The comparator unit is used for over voltage and short circuit detection. In each filter module, the comparator is used for overvoltage and short-circuit detection.

4.4 Short Circuit Detection

Protecting IGBT is one of the main tasks in inverter control. Inverter fault conditions, like phase-to-phase shorts or ground faults, need to be detected and rectified as quickly as possible before IGBT is destroyed. Typically, IGBT under short circuit needs to be turned off within 10 µs or less. This mandates the use of very fast AD conversion in protecting the IGBT in case of a short circuit.

The data filter unit, which is used for getting the conversion result, has a conversion delay. This delay depends on the OSR and the type of Sinc filter. The meet-accuracy requirement chosen is a higher OSR and higher-order Sinc filter; however, for the short circuit response time, a lower OSR and Sinc filter was chosen. This response time necessitates the use of the comparator unit, which works in parallel with the data filter unit. To meet such short-circuit detection requirements using AMC1304, the comparator oversampling ratio is typically set between 8 and 32, with a filter structure of Sinc^1 or Sincfast.

The comparator filter structure has been fixed for Sinc^1, with an OSR of 32 in firmware. Sinc^1 gives a better response time, and the OSR of 32 gives a 5-bit output-width resolution to set the threshold values. The format of the threshold register is an unsigned integer. The fault flags are set on crossing the threshold values; this triggers an interrupt, and within the interrupt, the firmware signals this event on a GPIO. The event is also stored in the MCU for the GUI or external controller to read. The threshold values can be calculated as shown in these examples:

- *Example 1:* Consider a 50-mV part with SDFCMPHx = 32, SDFCMPLx = 0. The threshold values are 62.5 mV and –62.5 mV; if the shunt value is 50 mΩ, this corresponds to (62.5 mV) / 50 mΩ = 1.25 A and (–62.5 mV) / 50 mΩ = –1.25 A.
- *Example 2:* Similarly for the shunt value of 5 mΩ, this corresponds to (62.5 mV) / 5 mΩ = 12.5 A and (–62.5 mV) / 5 mΩ = –12.5 A.

4.5 Scale Factor

The GUI obtains raw counts from the Delfino controller. The GUI calculates the applied voltage or current by multiplying the raw counts by a scale factor. First, calculate the intended scale factor. This is called the theoretical scale factor. Once the theoretical scale factor is known, calibration should be performed. Follow these steps for calibration:

Scale Factor for Motor Current Measurement

The part used for the current measurement is ±50 mV. The total full-scale deflection for the part from AMC1304M05 datasheet is 62.5 mV to –62.5 mV. This corresponds to a range of 32767 to –32768 for a 16-bit result register. The resolution is shown in Equation 21.

$$\frac{62.5\,\text{mV} - (-62.5)\,\text{mV}}{32767 - (-32768)} = 0.0019073\,\text{mV / count} \tag{21}$$

Considering the shunt used is 5 mΩ, the Scale factor in amps per division is shown in Equation 22.

$$\frac{0.00190734\,\text{mV}}{5\,\text{m}\Omega} = 3.8146 \times 10^{-4}\ \text{A / count} \tag{22}$$

Scale Factor for Inverter Voltage Phase-to-phase Direct Measurement

The part used for the DC link voltage is ±250 mV the total full-scale deflection for the part from data sheet is 312.5 to –312.5 mV. This corresponds to a range of 32767 to –32768 for a 16-bit result register. The resolution is

$$\frac{312.5\,\text{mV} - (-312.5)\,\text{mV}}{32767 - (-32768)} = 0.0095367\,\text{mV / count} \tag{23}$$

To calculate the voltage divider ratio, consider that AMC1304 has input impedance of 12.5 kΩ on each input terminal. Considering the circuit is configured as differential ended and in parallel to this is two 15 kΩ in series. Therefore, the total impedance at the AMC1304 terminal is (2 kΩ || 25 kΩ || 30 kΩ). The voltage divider ratio calculated from Figure 28 is

$$\frac{4.4\,\text{M}\Omega + (2\,\text{k}\Omega \,||\, 25\,\text{k}\Omega \,||\, 30\,\text{k}\Omega)}{(2\,\text{k}\Omega \,||\, 25\,\text{k}\Omega \,||\, 30\,\text{k}\Omega)} = 2523.66 \tag{24}$$

The scale factor AC voltage phase-to-phase direct measurement is 2523.66 × 0.0095367 = 0.024067 V/div

Scale Factor AC Voltage Phase-to-Phase with In-Amp

The part used for the AC voltage is ±250 mV the total full-scale deflection for the part from data sheet is 312.5 to –312.5 mV. This corresponds to a range of 32768 to –32768 for a 16-bit result register. The resolution is

$$\frac{312.5\,\text{mV} - (-312.5)\,\text{mV}}{32767 - (-32768)} = 0.0095367\,\text{mV / count} \tag{25}$$

The in-amp has very high input impedance with unity gain. Therefore, to calculate the voltage divider ratio, the voltage divider ratio provided from Figure 28 is

$$\frac{4.4\,\text{M}\Omega + (2\,\text{k}\Omega)}{(2\,\text{k}\Omega)} = 2201 \tag{26}$$

The scale factor AC voltage phase-to-phase direct measurement is 2201 × 0.0095367 = 0.02099 V/count

Scale Factor for AC Voltage Phase-to-Phase with In-Amp and Sallen Key

The scale factor is same as the case for phase-to-phase measurement with only in-amp, as the addition of Sallen Key does not change the voltage divider and has no effect on the input impedance. The Sallen Key provides a low-pass filter whether the gain at low frequency is unity.

Scale Factor for AC Voltage Phase-to-DC_MINUS In-Amp

The scale factor is same as the case for phase-to-phase measurement with only in-amp; here, the Sallen Key provides filtering and unit gain at lower frequency. The voltage divider is same as in the case of phase-to-phase measurement with only in-amp.

Scale Factor DC Link Voltage Measurement

The part used for the DC link voltage is ±250 mV the total full-scale deflection for the part from data sheet is 312.5 to –312.5 mV. This corresponds to a range of 32767 to –32768 for a 16-bit result register. The resolution is

$$\frac{312.5\,\text{mV} - (-312.5)\,\text{mV}}{32767 - (-32768)} = 0.0095367\,\text{mV / div} \tag{27}$$

To calculate the voltage divider ratio, consider that the AMC1304 has input impedance of 12.5 kΩ on each input terminal. Considering the circuit is configured as single ended hence total input impedance is 12.5 kΩ. The voltage divider ratio provided by for the DC link voltage from Figure 21 is

$$\frac{4.4\,\text{M}\Omega + (2\,\text{k}\Omega \,||\, 12.5\,\text{k}\Omega)}{(2\,\text{k}\Omega \,||\, 12.5\,\text{k}\Omega)} = 2533 \tag{28}$$

The scale factor for DC link voltage is 2533 × 0.0095367 = 0.024347 V/div

4.6 Calibration

The scale factor from the previous section is theoretical and produces errors in performance testing from expected reading. The reasons for this are:

- Offset error of AMC130x
- Gain error of AMC130x
- Tolerance of the sense resistors

In case of 2-wire shunts the soldering resistance adds to the shunt value and deviates the reading. For the current channel, this necessitates gain compensation.

In AC voltage measuring, the error seen depends on the tolerance of the components used for voltage divider. Uncalibrated error percentage error is approximately equal to tolerance of the parts. Also, the calculation depends on the AMC1304 input impedance this can vary from device to device. Calibration also compensates for AMC1304 input impedance, which does vary from device to device. The offset errors are negligible in AC voltage measuring configuration and is not required.

Because the DC link measurement the circuit configuration is single-ended, this causes an unequal bias on the input terminal and results in a DC-offset voltage appear at input terminal and is seen in conversion result of the SDFM peripheral of Delfino. Even with the compensation method explained in Section 4.1.1.2, it is not possible to completely remove the offset bias as it is not possible to have an exactly matched resistor. Therefore, after an offset compensation in hardware, further offset correction is done in software for the DC link measurement.

4.6.1 Calibration Procedure

Depending on the channel that is being calibrated the setup is made same as the Section 7.2.3 if it is current measurement, Section 7.1.1 if it is AC voltage measurement, Section 7.1.3. if it is DC link measuring section In all cases the calibration is done with respect to a reference meter.

Table 12 has steps to perform a two-point calibration. First, obtain the two readings. The readings may correspond to the maximum and minimum of the range from two readings if they are formatted in following:

Table 12. Two-Point Calibration Formatting

METER READING	READING FROM PC GUI
Xa	Ya
Xb	Yb

The gain calibration can be done by modifying the scale factor calculated previously as new scale factor = (Xa – Xb) / (Ya – Yb) × Old scale factor.

For offset calibration we calculate the required offset in raw counts as = (YbXa – YaXb) / Old scale factor.

Once the new scale factor value and the offset value is found this can be updated as explained in Section 6.5.

5 Software Description

The firmware was developed using the device support package for F2837xD contained in controlSUITE, which provides the register definitions for the device, peripheral driver libraries, and USB libraries. The libraries can be found in the installation directory of controlSUITE. The purpose of the firmware is to configure the Sinc filters, set the PLL frequency, receive data from Sinc filters, and interface to the PC's GUI to help user to validate the AMC1304 performance. The firmware supports configuration changes to Sinc filter parameters in the Delfino controller. The firmware is composed of the GUI interface, the DAC8564 interface, SDFM1 and SDFM2 interfacing to AMC1304, interfacing to CDCE906 for clock generation, ePWM to generate clock, and fault detection.

The SDFM1 and SDFM2 peripherals in the Delfino controller is interfaced with AMC130x. Firmware supports updating the filter type, the OSR value fault detection thresholds. The SDFM1 and SDFM2 channel are renamed on the GUI to have a common naming convention. The naming convention is "channel1" to "channel7" and is shown in Figure 15.

On start up, the firmware configures the controller for fault detection using the SDFM's comparator unit with default threshold values. The GUI can be used to update the threshold settings. When overload is detected, the event is logged inside the interrupt routine and also GPIO1 on the header J2 is set. The GUI reads periodically from the firmware if any faults have occurred.

The GUI interface is implemented using the integrated USB in F28377D. The device is configured for device mode as a raw bulk device. Raw bulk device was chosen as it provided a convenient interface to the Labview GUI. The raw bulk descriptor and configuration is the same as the controlSUITE example by the name "usb_dev_bulk". A custom application protocol was implemented for interaction between the USB device and GUI. Implementation of this protocol can be seen in files "GUI.h" and "GUI.c" for its internal working.

See CDCE906 (SCAS814I) data sheet for the Devices configuration registers and definition. The Delfino interfaces to the clock synthesizer CDCE906 on the I^2C bus. After power on the firmware sets up CDCE906 to minimum clock output of 1 MHz, the clock output can be changed from the GUI. When the user updates the switching frequency in the GUI, the GUI calculates the new clock frequency and internally calculates the required configuration values to be written into the CDCE906. The Delfino receives the clock configuration from the GUI and updates the register settings in CDCE906 through the I^2C interface.

ePWM8 is used to generate a clock only for the modulator monitoring the DC link voltage on the board. The board requires seven independent clocks; six are provided by the clock synthesizer CDCE906. The clock for the last channel is provided by the ePWM peripheral. The output clock generated is fixed at 5 MHz for this channel.

The two DAC8564 is used for debugging purpose. The Delfino updates the DAC's output to represent the conversion result by the SDFM peripheral. The user can then view the waveform on the oscilloscope. DAC8564 is interfaced on SPI-B, and the CPU2 is made master of SPI-B. See DAC8564 (SBAS403D) for the SPI frame format. To update one channel of the DAC, write a 24-bit word, the first 8 bits containing the DAC addressing, channel addressing, and the load command and the next 16 bits is the DAC value in 16-bit straight binary.

The firmware uses immediate load for all channels, and the DAC address and channel address are chosen appropriately. LDAC feature is not used. The firmware sets up the DAC8564 to use an internal 2.5-V reference. CPU1 passes the SDFM results to CPU2 by writing the results to a shared RAM. The address location is hard code in both CPU1 and CPU2 and maintained same. The output from the SDFM is configured to a 16-bit signed output, ranging from –32768 to 32767. This output is converted to 16-bit straight binary by adding 32767 to SDFM output. That is, 1.25 V from DAC represents 0, 2.5 V represent 32767, and 0 V represents –32768 from the SDFM peripheral.

Figure 59 shows the firmware flow graph and arrangement of tasks between CPU1 and CPU2.

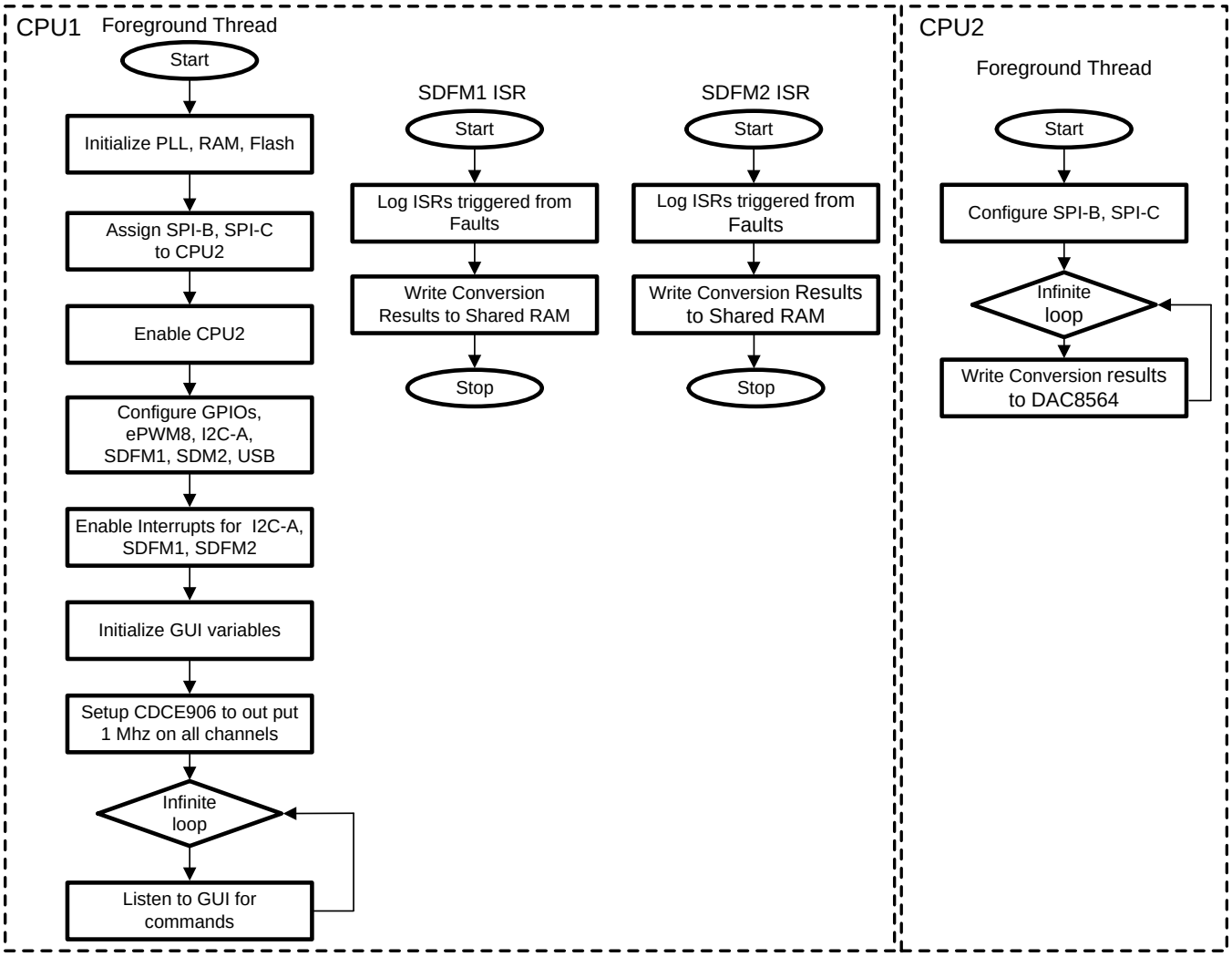


Figure 59. Firmware Flow Graph

6 GUI User Guide

This section describes the functionality of the isolated current and voltage measurement test bench.

6.1 GUI Software Installation

The following section explains the location and the procedure for installing the software properly. The GUI assumes that CPU1 and CPU2 of the Delfino controller has been programmed with firmware found at TIDA-00171.

6.1.1 Installing Run-Time Engine

The LabVIEW run-time engine must be downloaded and installed to use the IVIM Test Bench.

1. Click on the link to install the LabVIEW Run-Time Engine 2010 SP1 (32-bit Standard RTE). http://www.ni.com/download/labview-run-time-engine-2010-sp1/2292/en/
2. Run LVRTE2010_SP1f5std.exe to install the LabVIEW 2010 SP1 Run-Time Engine (32-bit).
3. Follow the installation wizard and complete the installation.

The installation files for the run-time engine are automatically extracted to a directory on disk. The installer does not remove the files after installing. If you want to remove these files from the disk, be sure to note their location during the unzipping process.

6.1.2 Installing VISA

The VISA driver must be downloaded and installed to communicate with the device.

1. Click the link to install the NI-VISA 5.0.3. http://www.ni.com/download/ni-visa-5.0.3/2251/en/
2. Run visa503full_downloader.exe.
3. Follow the installation wizard and complete the installation.

6.1.3 Installing IVIM Test Bench

The GUI can be found at TIDA-00171.

1. Select the *Destination Directory* for IVIM Test Bench and click *Next*.

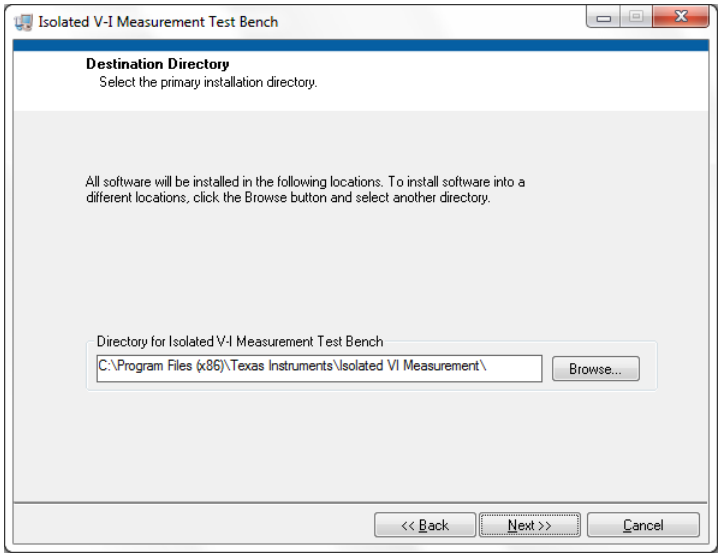


Figure 60. The Destination Directory Selection Window for IVIM Test Bench

2. Figure 61 shows the list of files that will be added or modified with this installation. Click *Next.*

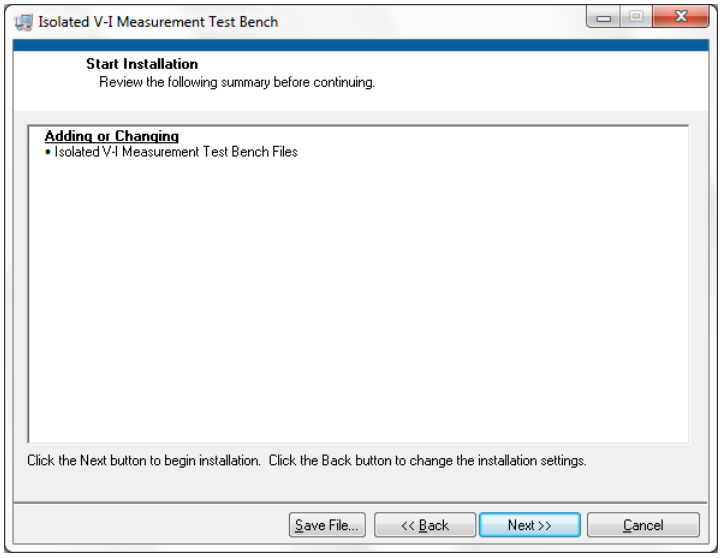


Figure 61. List of Files Added or Modified With Installation

3. Once the installation starts and finishes as shown in Figure 3, click *Finish.*

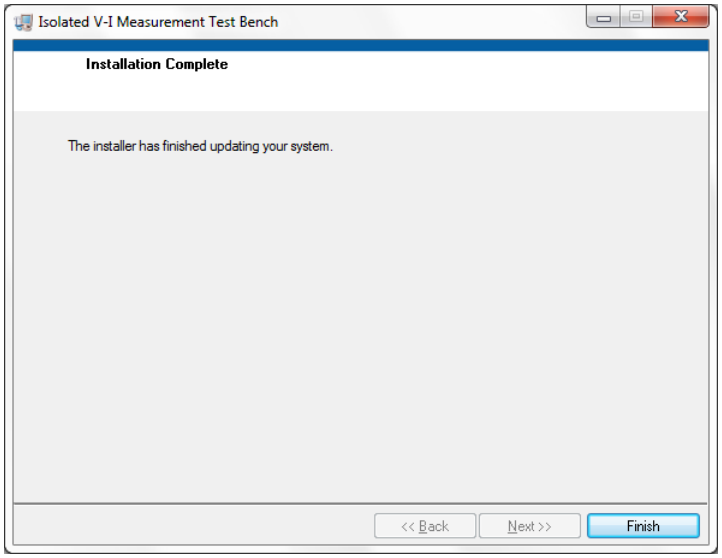


Figure 62. Window After Successful Installation

6.2 Launching IVIM Test Bench

Follow these steps to launch the IVIM Test Bench.

1. Locate the IVIM Test Bench through any of these approaches:
   - Desktop shortcut
   - Start menu shortcut
   - Installed folder location. Default location is Win 7: C:\Program Files (x86)\Texas Instruments\Isolated VI Measurement\
2. Double click on Isolated V-I Measurement.exe

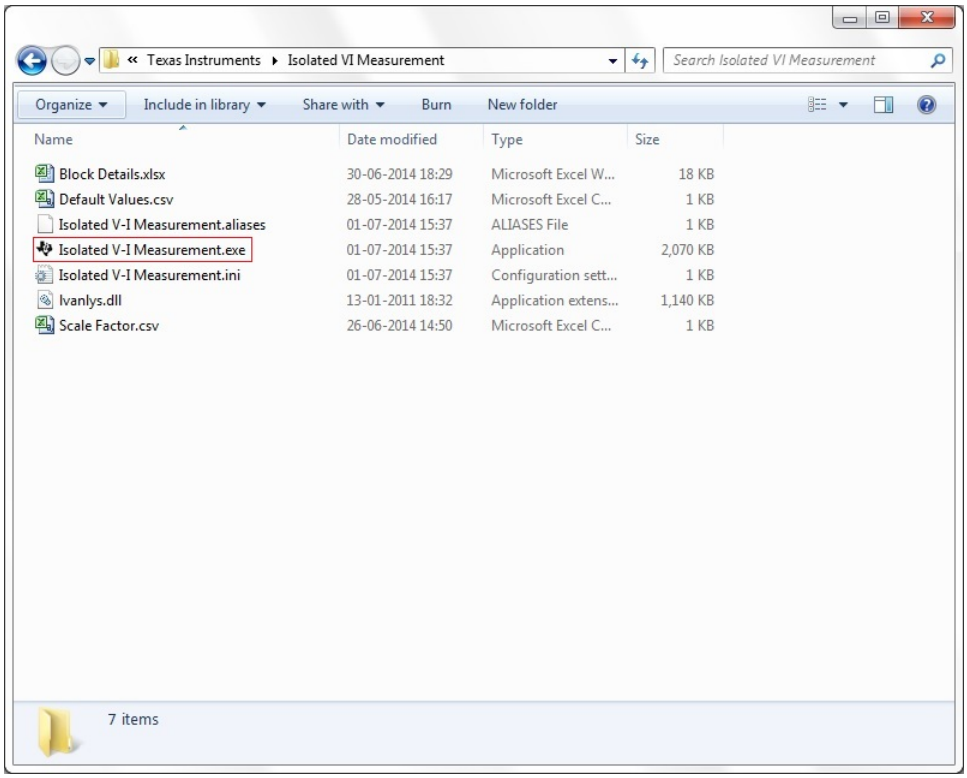


Figure 63. Isolated VI Measurement Folder Structure

6.3 Mode Selection

The *Select a Mode* dialog box pops up as the application is launched (Figure 5). Select the MCU and the corresponding VISA resource name.

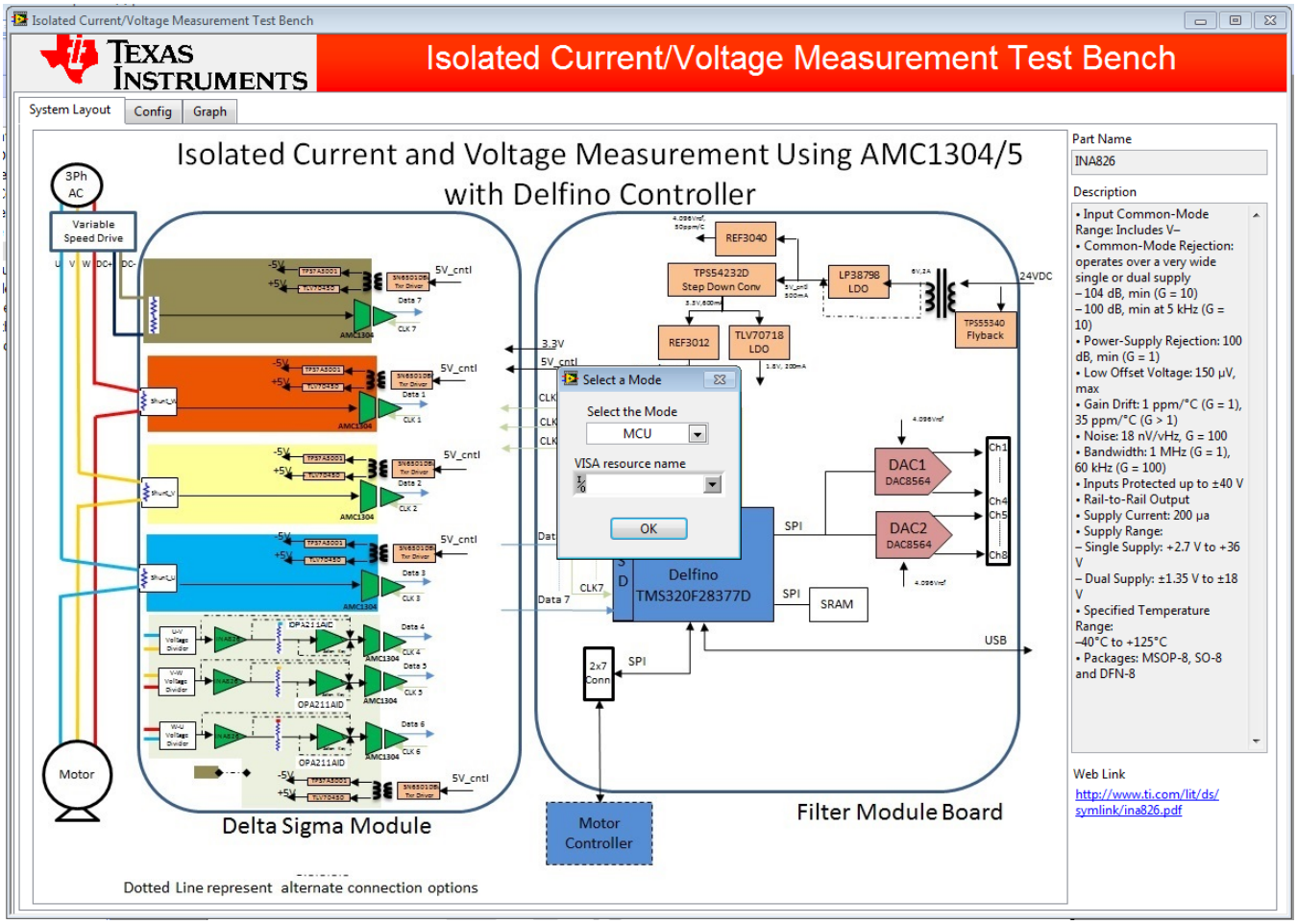


Figure 64. Mode Selection

As soon as the user selects the mode, the GUI starts to initialize.

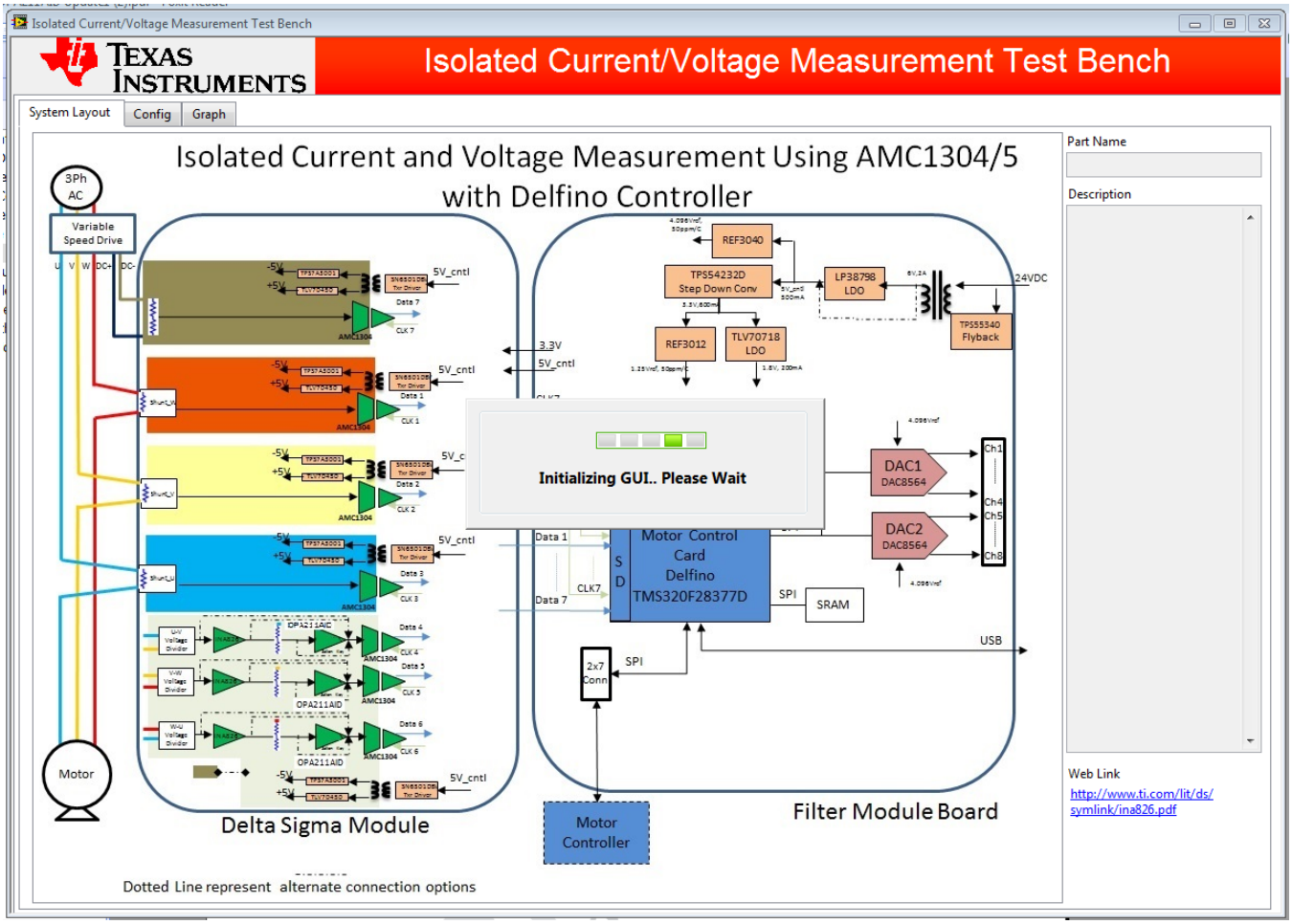


Figure 65. GUI Initialization

Proceed to use the GUI after the initialization completes.

6.4 IVIM Pages

IVIM Test Bench has three pages:

1. System layout
2. Config page
3. Graph page

6.4.1 System Layout

The system layout page has the block diagram with description of the parts used in Isolated current and voltage measurement. Moving the mouse pointer over any of the blocks shows the description of the same on the right side of the page with web links for reference. Refer to Figure 66.

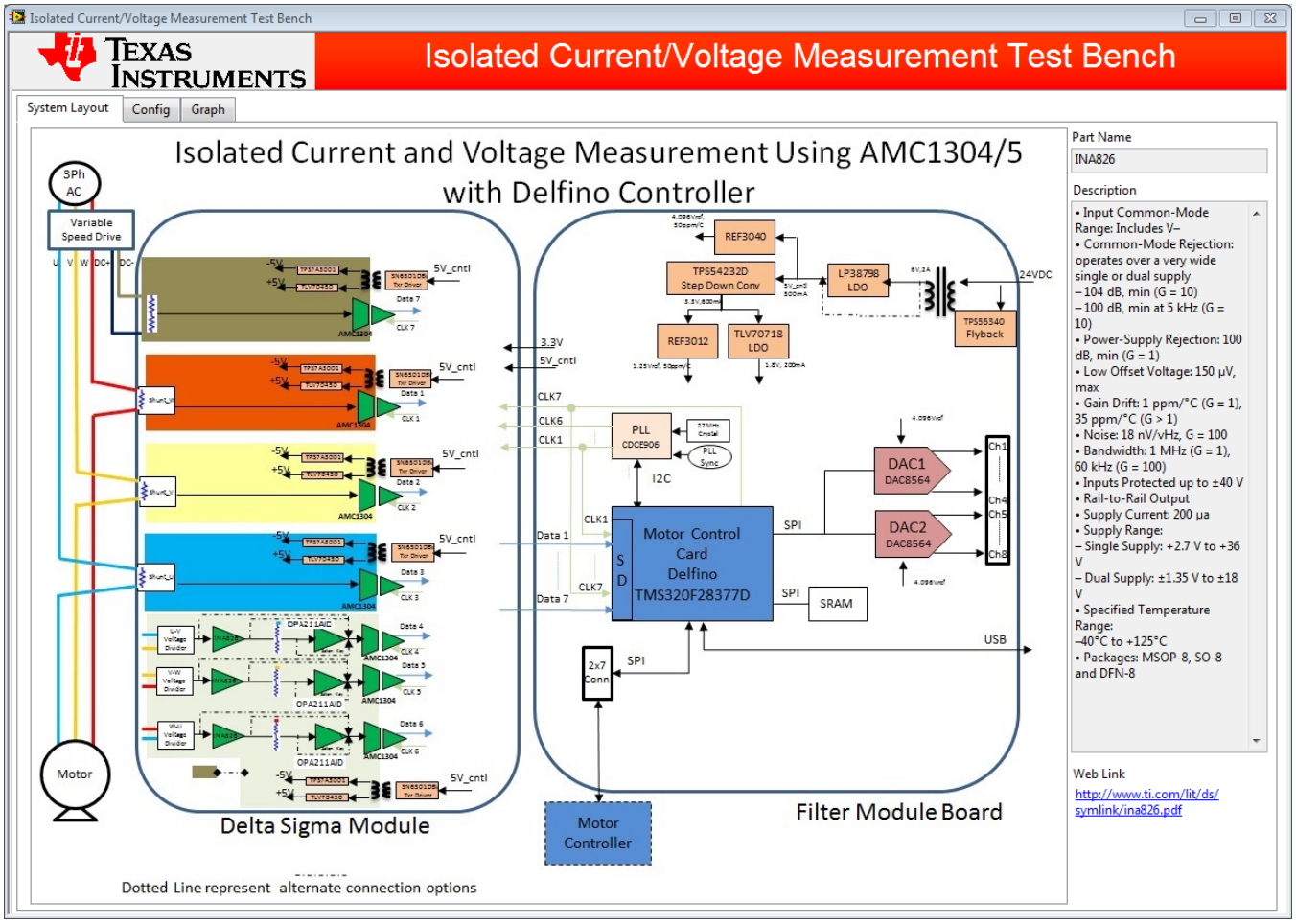


Figure 66. System Layout

- **Block Diagram:** The block diagram gives the detailed description of the parts used for isolated voltage and current measurement
- **Part Name:** This box displays the part name selected.
- **Description Box:** This box displays a brief description about the part in the block diagram.
- **Web Link Box:** This box displays the web reference of the part.

6.4.2 Config Page

This page allows the user to configure the delta-sigma filter parameters.

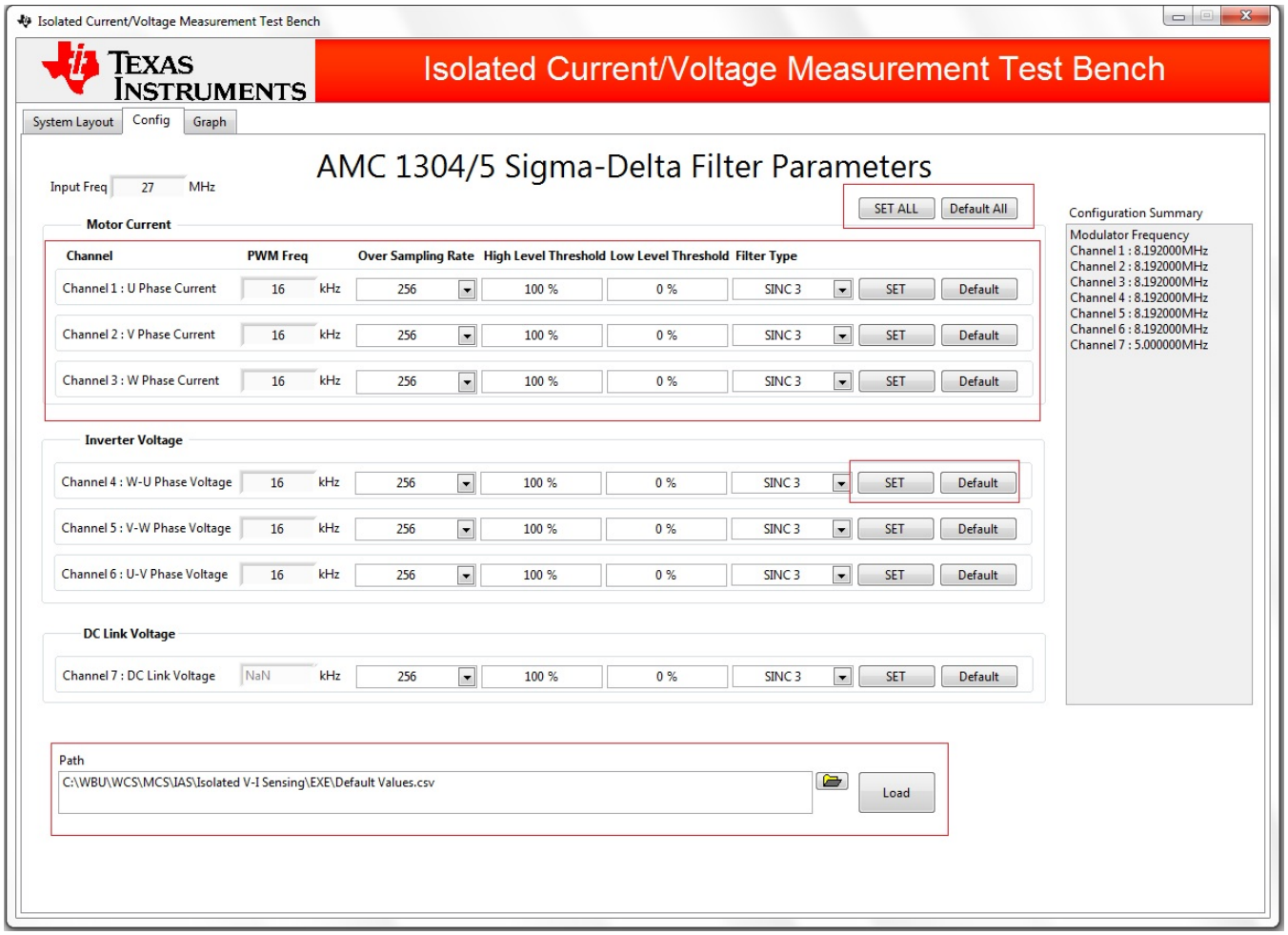


Figure 67. Config Page

- **Motor Current:** This option contains the settings for three channels to be configured for respective phase current.
- **Inverter Voltage:** This option contains the settings for three channels to be configured for respective phase voltage.
- **DC Link Voltage:** This option contain the setting for a channel to be configured for DC link voltage.
- **Set:** This button sets the configured settings for the corresponding row.
- **Set All:** This button sets the configured value for all channels.
- **Default All:** This button sets the default values for all channels.
- **Load:** This button loads the values for each parameter form the file specified in the in the path dialog box.
- **Configuration Summary:** This option displays the modulated frequency for each of the channels.

6.4.2.1 Setting PWM Frequency and Oversampling Rate

- **PWM Frequency:** The frequency value can be entered in the given text box in kHz.
- **Oversampling Rate:** The oversampling rate can be selected from the list.

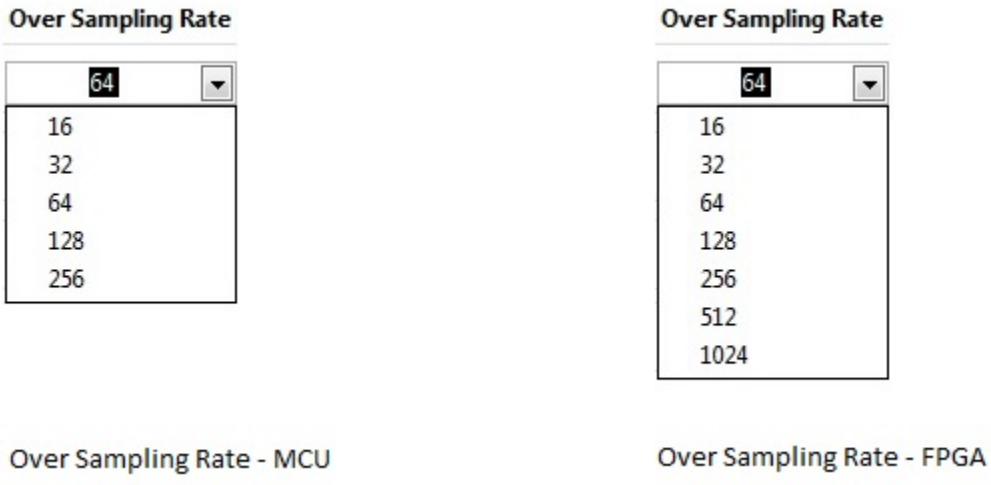


Figure 68. Over Sampling Rate Selection

- **Modulator Frequency:** The modulator frequency depends on the PWM frequency and over sampling rate. The modulator frequency is limited to 20 MHz.

6.4.2.2 Setting the Filter Type

The filter type for each channel can be set from the list (shown in Figure 69).

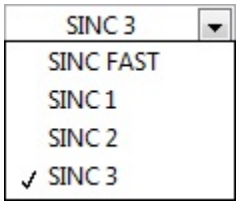


Figure 69. Channel Filter Type

6.4.2.3 Setting Default Value

Each channel can be configured to their default values using the *Default* button provided for each channel. The user can also use the *Default All* button to set default values to all the channels.

6.4.2.4 Configuration Summary

The configuration summary box gives the calculated modulator frequency for each channel. The modulator frequency has a limit of 5 to 20 MHz. When the set values exceed the limit, the values are coerced and the summary box indicates the error with a notification as shown in Figure 70.

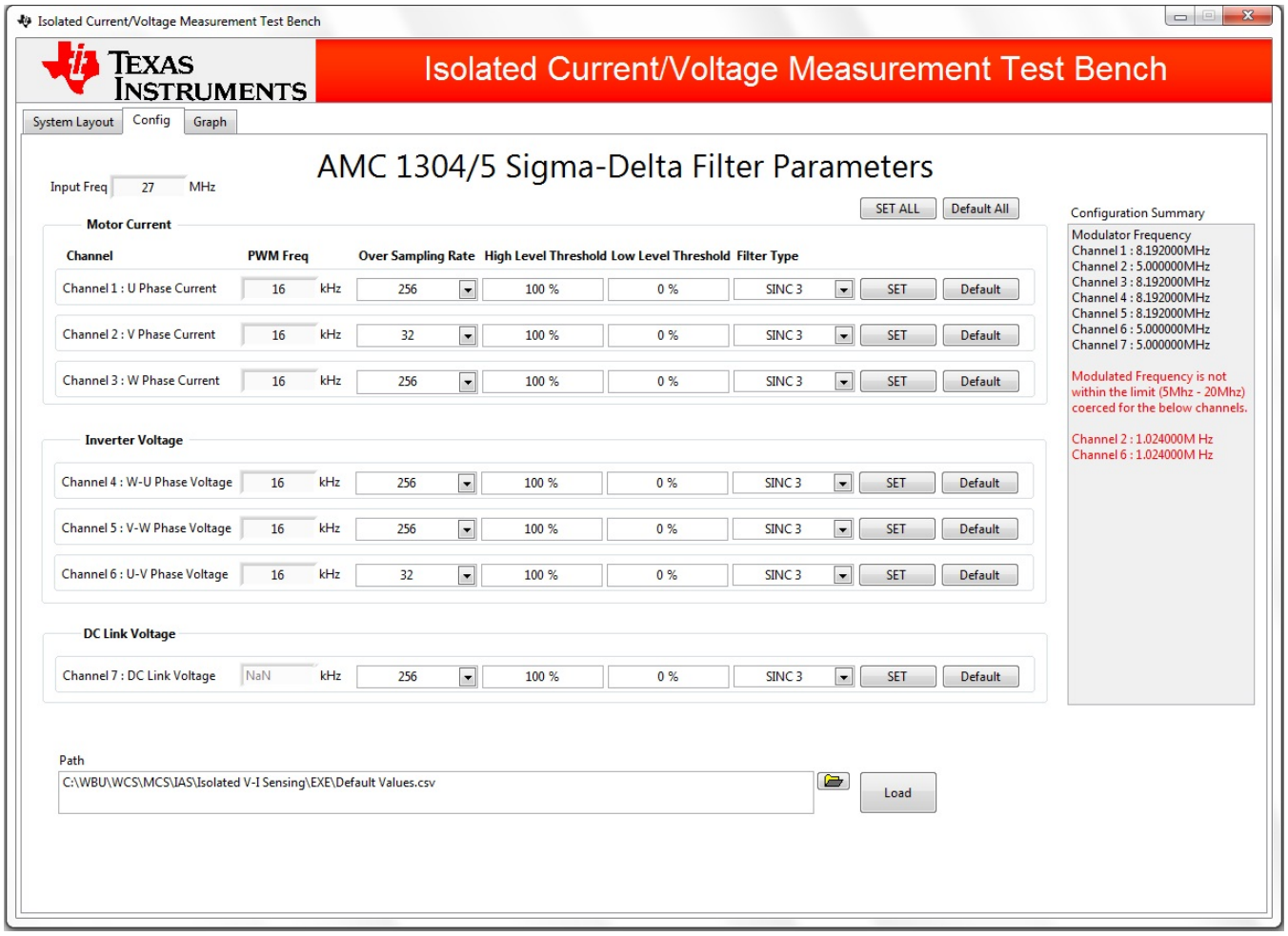


Figure 70. Configuration Summary

6.4.2.5 Loading the Default Value File

Select the default value file using the path control available. Click on the *Load* button to load the settings to the user interface.

Figure 71. Load Default Values File

6.4.2.6 Setting Configuration

Set the final channel configuration using the *Set* buttons provided with each channel or can use *Set All* button to set all channels configuration. When the *Set All* button is pressed, all the details in the config page is sent to the MCU as previously selected.

6.4.3 Graph Page

The graph page is the result display and processing page. The captured values are displayed as graphs in this page as either in time domain or frequency domain.

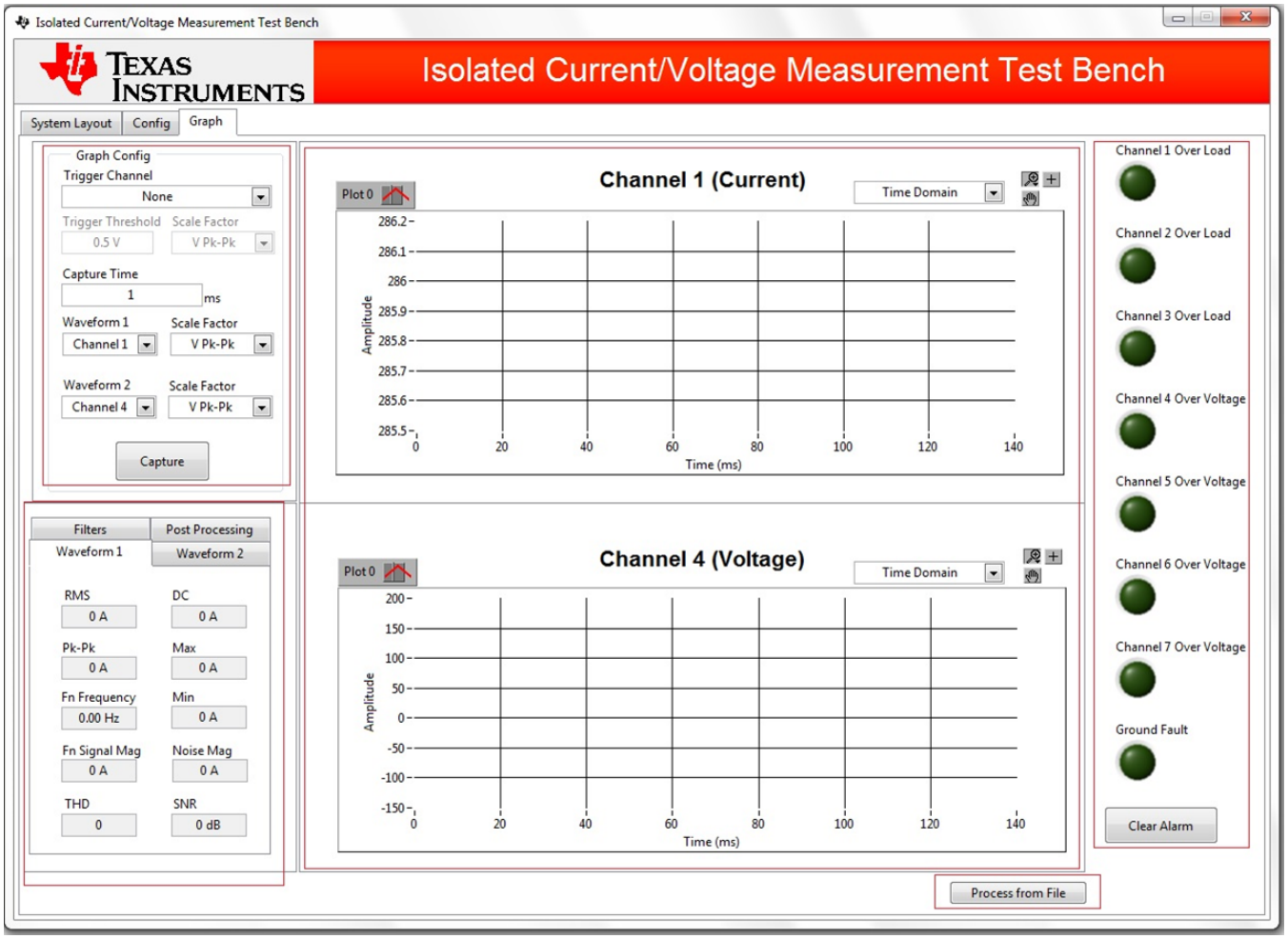


Figure 72. Graph Page

- **Graph Config:** This pane sets the trigger modes and select waveforms to display.
- **Waveform Parameter:** This pane displays the parameters of the selected waveform.
- **Graph Pane:** The captured data is plotted in the form of graph in this pane.
- **Error Indicators:** The graph page has eight indicators to detail the error. *Clear Alarm* erases the indications.
- **Process from File:** This button plots the data from the file in a graph.

6.4.3.1 Setting the Trigger Channel

The trigger channel can be set using the *Trigger Channel* control. Select any of the channels available.

Set the trigger threshold of the selected channel in *Trigger Threshold* control, and select the scale factor from the *Scale Factor* control.

Set the capture time in milliseconds (ms) in the *Capture Time* control.

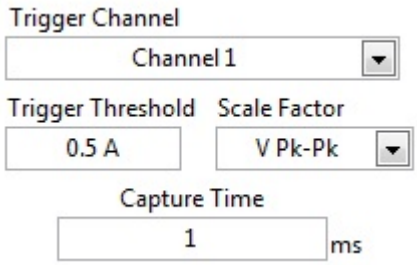


Figure 73. Trigger Configuration

6.4.3.2 Selecting the Waveform and Scale Factor

The waveform to be displayed and its corresponding scale factors can be selected from the *Waveform 1* and *Waveform 2* control. The scale factors are selected from their respective controls.

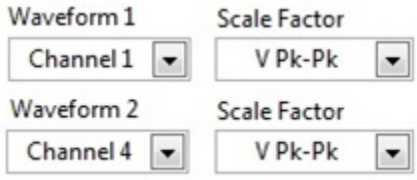


Figure 74. Waveform Settings

6.4.3.3 Selecting the Filter

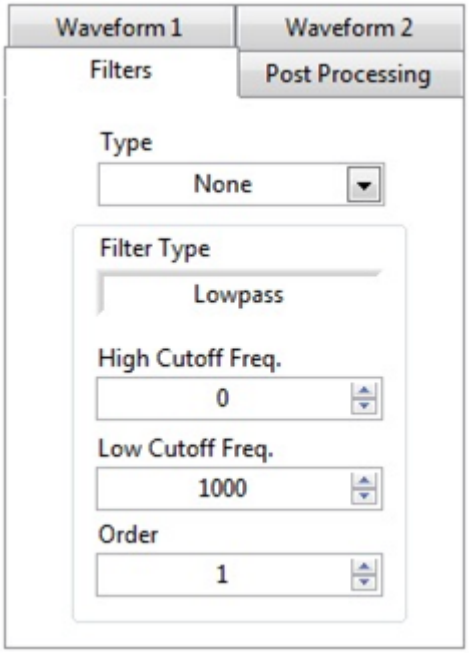


Figure 75. Filter Selection

The filter can be selected from the *Type* control.

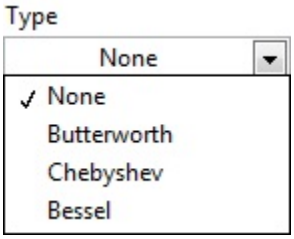


Figure 76. Filter Type Selection

The filter characteristics can be set using the *Filter Type*, *High* and *Low Cutoff Freq.*, and *Order* controls.

6.4.3.4 FFT Window Selection

FFT windows can be selected using the *FFT-Window* control in *Post Processing* tab.

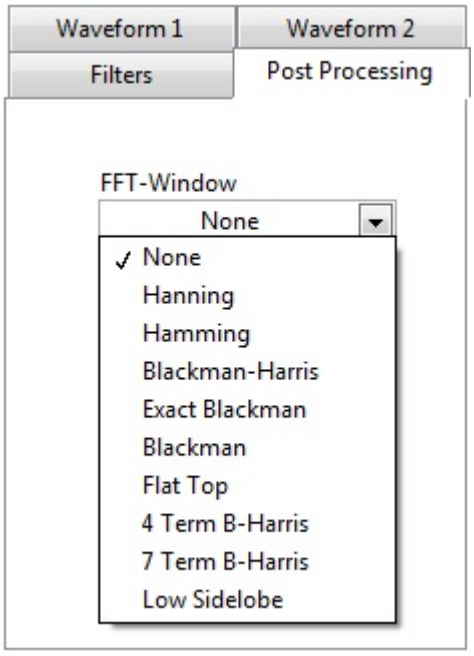


Figure 77. FFT Window Selection

6.4.3.5 Waveform Parameter Display

The parameters of the selected channel waveform can be noted from the waveform page as in Figure 78.

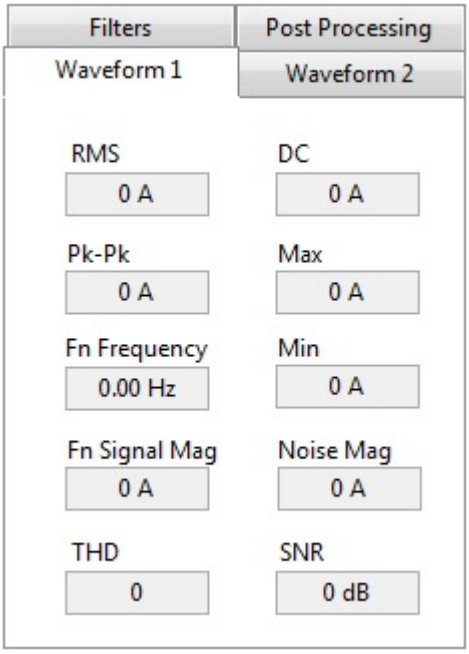


Figure 78. Waveform Parameter Display

6.4.3.6 Data Capture

Click on the data captures shown in Figure 79 to obtain the results.

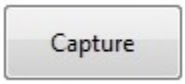


Figure 79. Data Capture Button

Capture mode sends the corresponding settings to MCU, gets the data for the time specified, and displays it in the graph once.

6.4.3.7 Selecting the Domain

Select the graph domain using control provided for each graphs and the *Time/Frequency* domain using this control (see Figure 17).

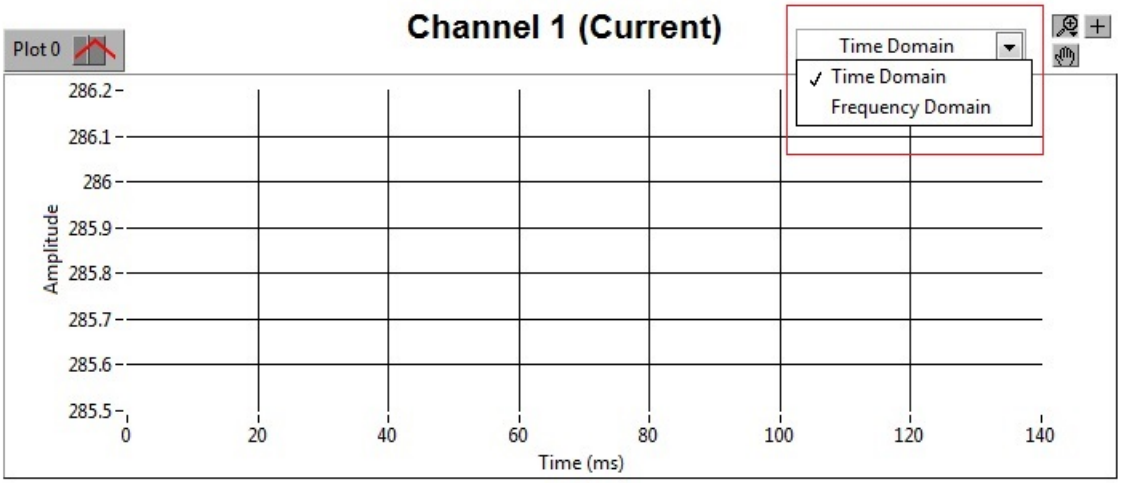


Figure 80. Graph Domain Selection

6.4.3.8 Emergency Indicators

The emergency indicators activate during overload and overvoltage conditions. The user can clear these indicators by pressing the *Clear Alarm* button available in the user interface.

6.5 Editing the Scale Factor

The scale factor values are read from the *Scale Factor.csv* file and then loaded to the user interface.

The scale factor file is placed in the same folder of the executable.
For Win 7: C:\Program Files (x86)\Texas Instruments\Isolated VI Measurement\

- The scale factor is the value used to convert the raw data into the equivalent voltage/current specified by the user.
- Offset is the value used to calibrate the fixed offset errors. This value will be subtracted from the raw value received from MCU.

The structure of the scale factor file is as shown in Table 13:

Table 13. Scale Factor Structure

SCALE LABEL	SCALE FACTOR	OFFSET
V Pk-Pk	0.023103	0
V at APC	0.00021	0
Current	3.81E-05	0
V_Inamp	0.021437137	0
Raw	1	0
CH1 CAL	3.83E-05	0
CH2 CAL	3.81E-05	0

User can give a suitable Scale Label and the corresponding Scale Factor and Offset value.

NOTE: Do not change the structure of the file by adding or deleting any columns. The user can only add or delete the rows.

6.6 Editing Default Values

The default value for each channel is read from the *Default Values.csv* file. The structure of this file is as shown in Table 14:

Table 14. Default Value Structure

CHANNEL NAME	MODULATOR CLOCK FREQUENCY	OSR	HIGH-LEVEL THRESHOLD	LOW-LEVEL THRESHOLD	FILTER TYPE
1	16	256	100	0	SINC 3
2	16	256	100	0	SINC 3
3	16	256	100	0	SINC 3
4	16	256	100	0	SINC 3
5	16	256	100	0	SINC 3
6	16	256	100	0	SINC 3
7	16	256	100	0	SINC 3

The user can edit the necessary field and save the changes.

NOTE: Do not change the structure of the file by adding or deleting any columns or rows.

7 Test Results

The board was tested for claimed performance with respect to accuracy for 3-phase motor voltage, DC link voltage, and AC current measurements. The results of the test are given here. For the 3-phase AC, the test was conducted for both phase-to-phase and phase-to-DC_MINUS voltage configuration. Additionally, graphs form functionally testing on power supply, DACs, clocks, data, and EMC test are given here.

7.1 Voltage Measurement Accuracy

7.1.1 Test Setup for AC Voltage Accuracy

The diagram of the test set up for validating the AC voltage measurement is shown in Figure 71. The Isolated Current Shunt and Voltage Measurement Kit is placed in a thermal chamber. The test is performed using Agilent's 6 ½ digit-multimeter (34401A) as the reference meter. The first reading is taken at 25°C. The results calculated using the theoretical scale factor are discussed in Section 4.5.

For AC voltage measurement, gain correction was performed. The reading was taken at 25°C, –25°C, and 75°C. The board provides flexibility to add in-amp and Sallen-Key filter to the signal chain. The test was performed for four of the possible configurations: phase-to-phase voltage measurement using a voltage divider connected directly to AMC1304; phase-to-phase voltage measurement using an in-amp; phase-to-phase voltage measurement using an in-amp and Sallen-Key filter; and phase-to-DC_MINUS voltage measurement using an in-amp and Sallen-Key filter. Figure 81 describes the modification required on the board to enable each of these configurations.

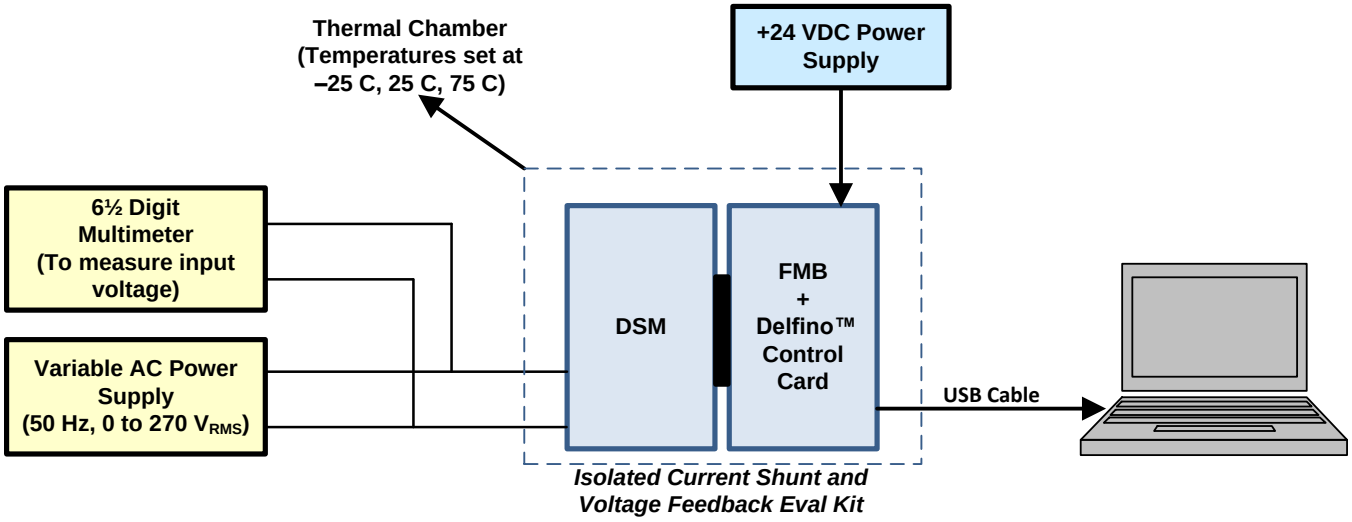


Figure 81. Test Setup for AC Voltage Measurement Accuracy

7.1.2 Results

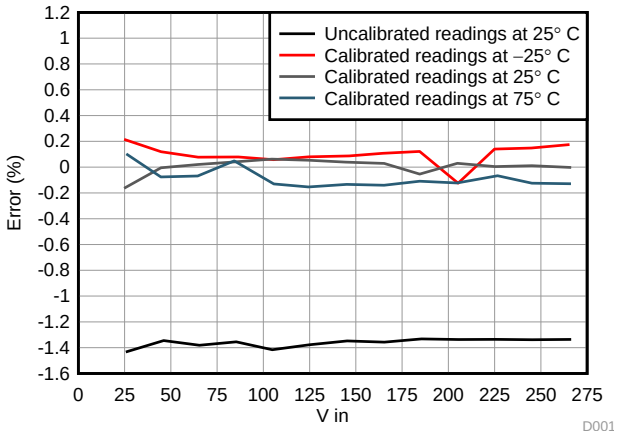


Figure 82. Phase-to-Phase Voltage versus Error

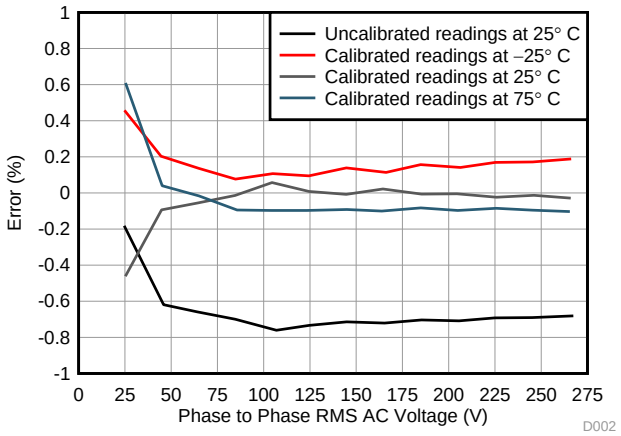


Figure 83. Phase-to-Phase Voltage versus Error with In-Amp

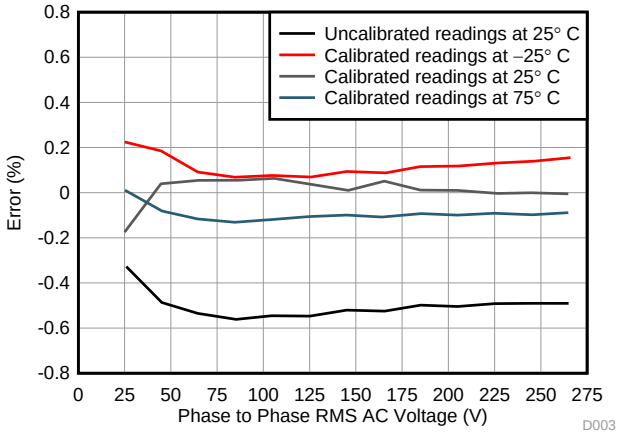


Figure 84. Phase-to-Phase Voltage versus Error with In-Amp and Sallen Key

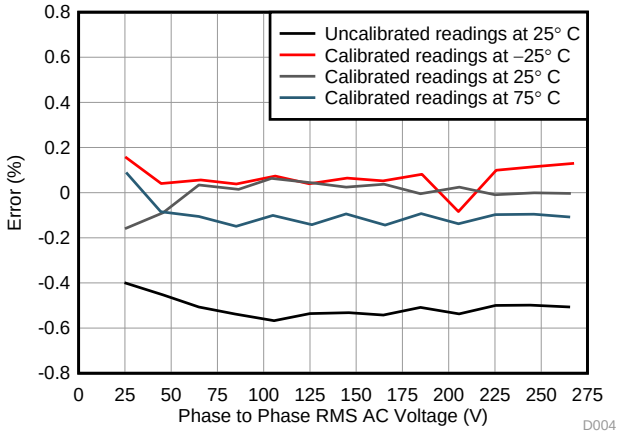


Figure 85. Phase-to-DC_MINUS versus Error with Sallen Key

AMC130X with INL of just 4LSBs, having a smaller temperature drift (20 ppm per degree) in gain error along with integrated SINC digital filter (TMS320F2837x) to decimate the bit stream, enables the system to achieve 16-bit of resolution with 13 bit 13 ENOB leading to a 0.2% accuracy across temperatures from –25°C to 75°C.

7.1.3 Test Setup for DC Link Voltage Measurement Accuracy

The diagram of the test set up for validating the DC link voltage measurement is shown in Figure 86. The Isolated Current Shunt and Voltage Measurement Kit is placed in the thermal chamber. Agilent's 6 ½ digital-multimeter (34401A) was used as reference to calculate error. The first reading is taken at 25°C. The results calculated using the theoretical scale factor are discussed in Section 4.5. For the DC link measurement, both offset error correction and gain correction were performed. The reading was taken at 25°C, –25°C, and 75°C.

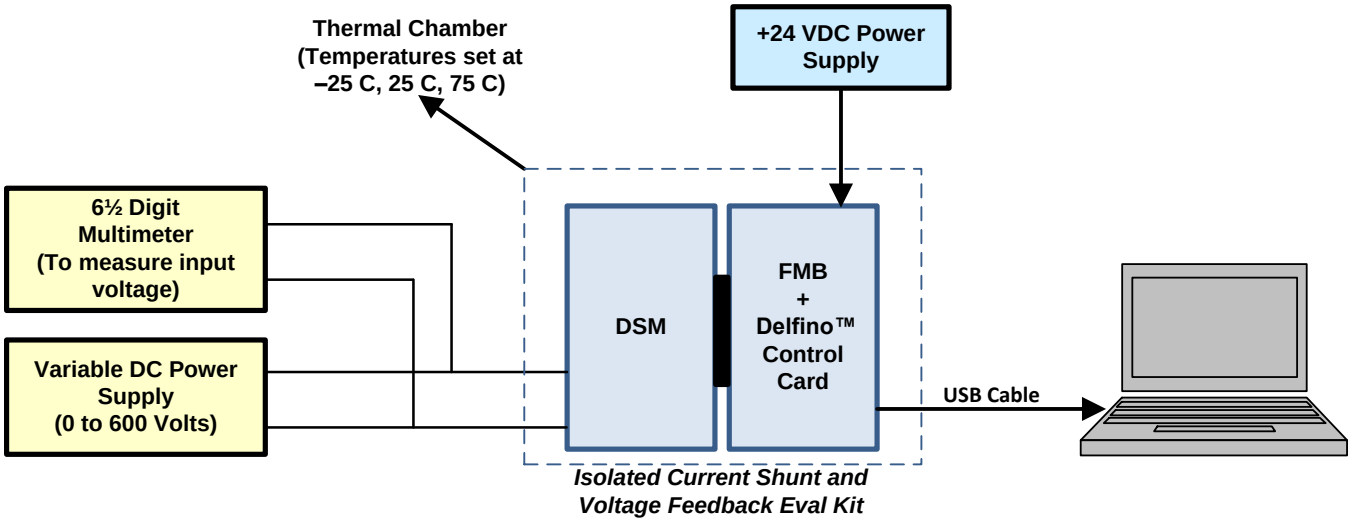


Figure 86. Test Setup for DC Link Voltage Measurement Accuracy

7.1.4 Results

Figure 87 and Figure 88 show the error versus applied DC link voltage. The uncalibrated error at a lower voltage is due to an offset error.

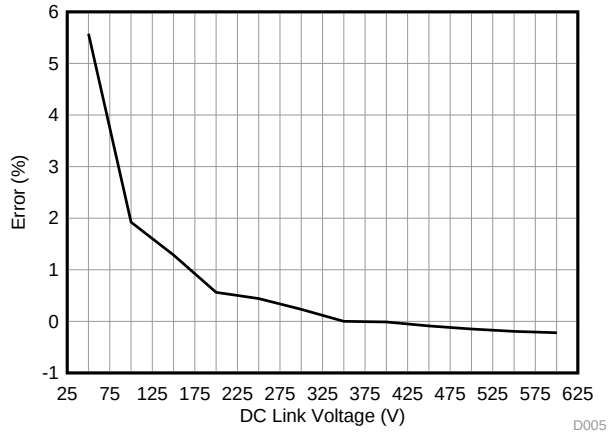


Figure 87. Uncalibrated Readings at 25°C

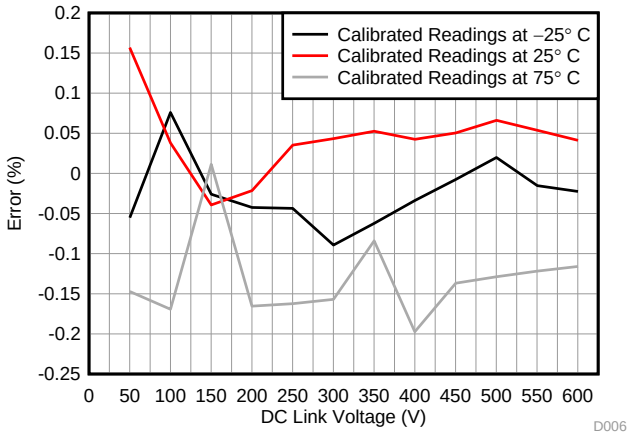


Figure 88. DC Link Voltage versus Error

7.2 Current Measurement Accuracy

7.2.1 Test Setup DC Measurement Accuracy

The diagram of the test set up for validating the DC measurement is shown in Figure 89. The Isolated Current Shunt and Voltage Measurement Eval Kit is placed in the thermal chamber. The DC source used is Keithley 2420. Two sources are used in parallel to get the desired maximum current. This source has a precision metering inbuilt, which is used as a reference. The first reading is taken at 25°C. The results calculated using the theoretical scale factor are discussed in Section 4.5. For DC measurement, a gain correction was performed. The reading was taken at 25°C, –25°C, and 75°C. While performing this test, Agilent's 6 ½ Digit-multimeter (34401A) measured the shunt voltage. The shunt voltage and shunt current was used to calculate the shunt impedance. The results are given in Table 15.

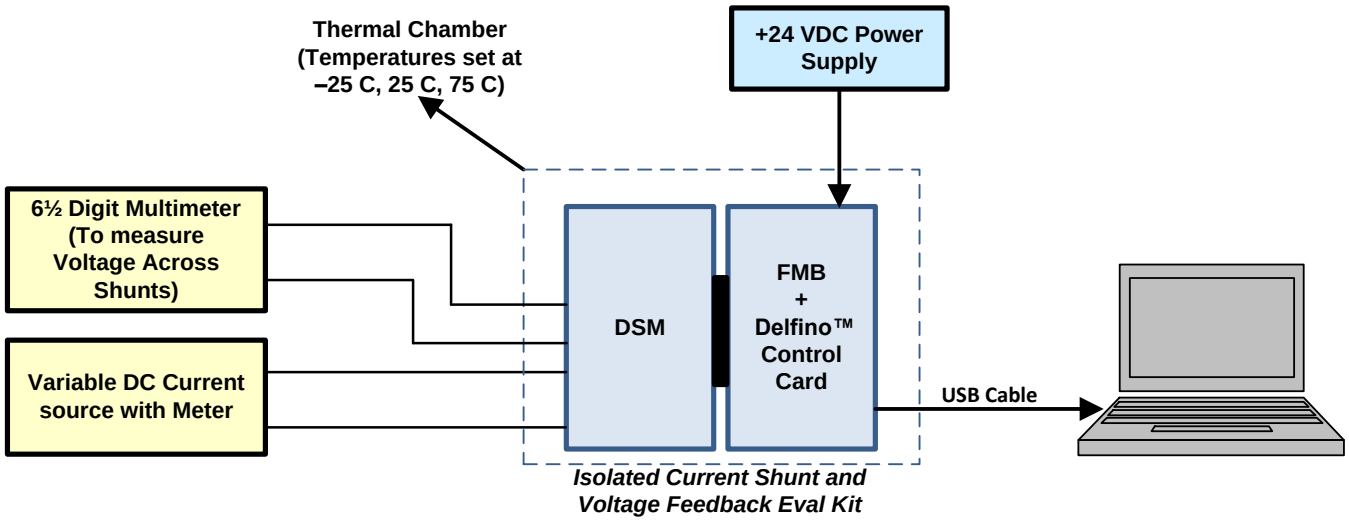


Figure 89. Test Setup for DC Measurement Accuracy

7.2.2 Results

Table 15. Effective Shunt Resistance

TEST	VALUE
Effective Shunt Resistance at –25°C	5.131 mΩ
Effective Shunt Resistance at 25°C	5.2104 mΩ
Effective Shunt Resistance at 75°C	5.2865 mΩ

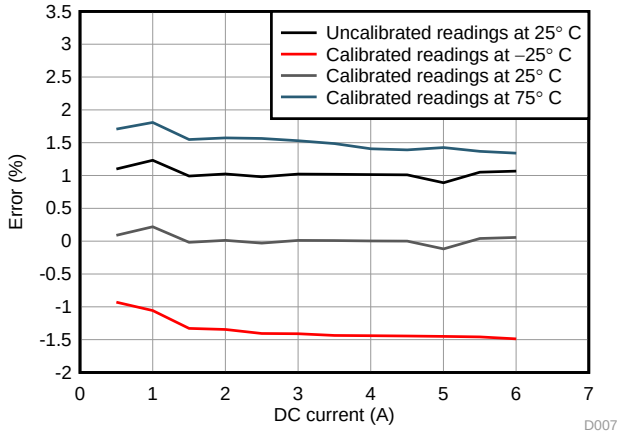


Figure 90. DC Current versus Error

NOTE: A higher error is noticed due to change in resistance of the solder joint in the shunt resistor. With proper routing or with use of a 4-wire shunt, the calibrated accuracy will be within 0.2% across temperatures from –25°C to 75°C.

7.2.3 Test Setup for AC Measurement Accuracy

The diagram of the test set up for validating the AC measurement is shown in Figure 91. The Isolated Current Shunt and Voltage Measurement Eval Kit is placed in the thermal chamber. The AC is measured using Agilent's 6 1/2 Digit-multimeter (34401A), which is used as the reference. The first reading is taken at 25°C. The results calculated using the theoretical scale factor are discussed in Section 4.5. For AC measurement, a gain correction was performed. The reading was taken at 25°C, –25°C and 75°C.

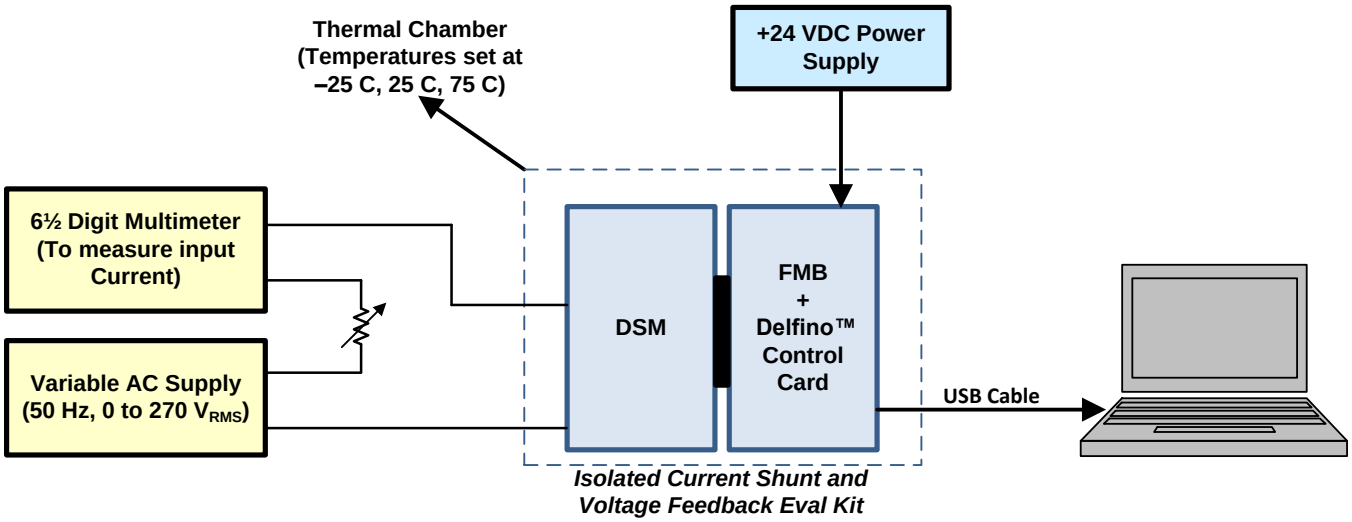


Figure 91. Test Setup for AC Current Measurement Accuracy

7.2.4 Results

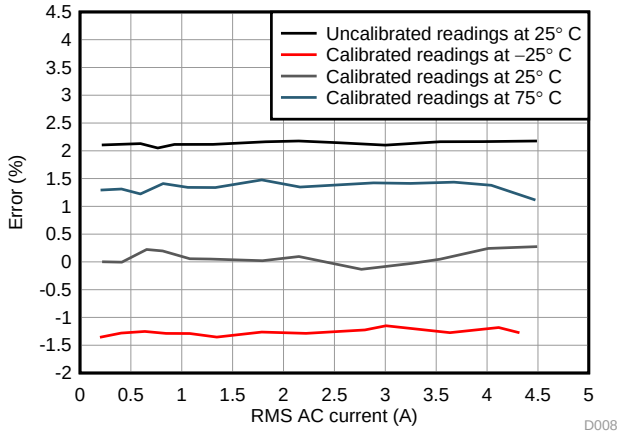


Figure 92. AC Current versus Error

NOTE: A higher error is noticed due to change in resistance of the solder joint in the shunt resistor. With proper routing or with use of a 4-wire shunt, the calibrated accuracy will be within 0.2% across temperatures from –25°C to 75°C.

7.3 Test with Motor Drive and Load Setup

7.3.1 Test Setup

The diagram of the test set up for validating the AC measurement on a motor drive setup is shown in Figure 93. The same calibration data obtained for in the previous test were retained for while conducting test on the motor.

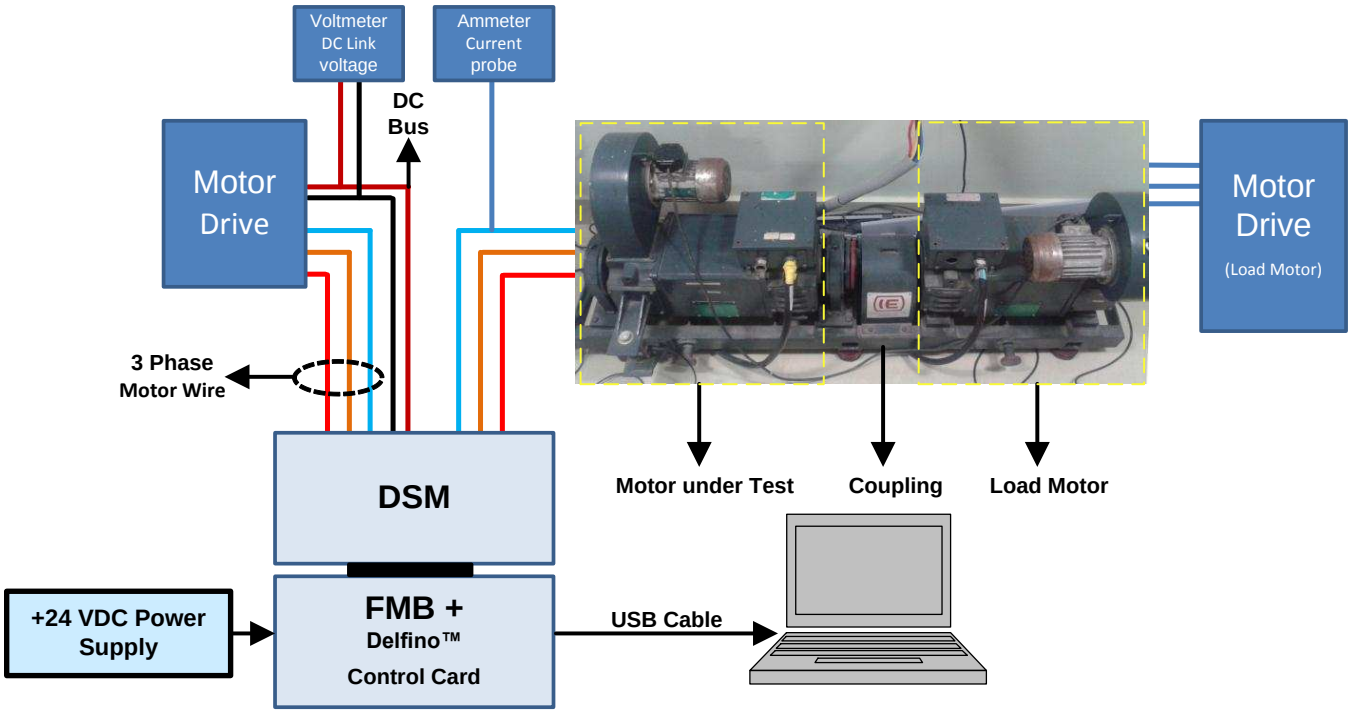


Figure 93. Test with Motor Drive and Load Setup

7.3.2 Results

The error versus motor current shown in Figure 94 and error versus DC link voltage are Figure 95. Notice there is no trend in the error; the max error lies within a ±0.2% error band.

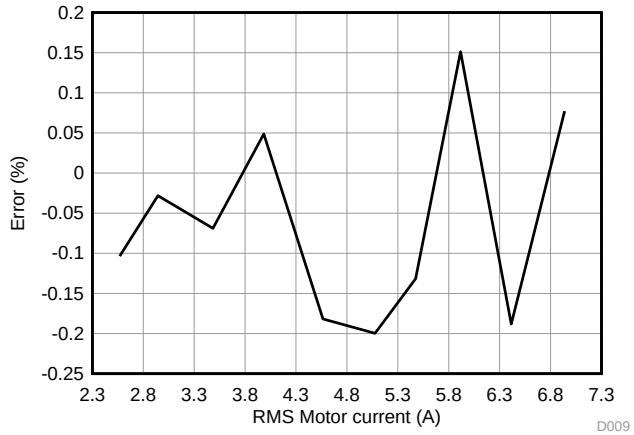


Figure 94. Motor Current versus Error, Tested with Motor Drive and Load Setup

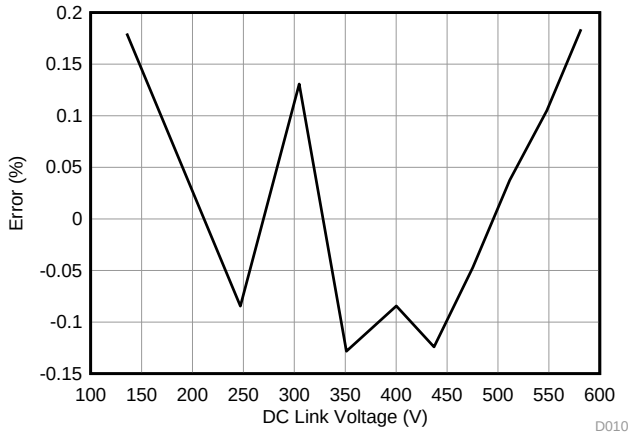


Figure 95. DC Link Voltage versus Error, Tested with Motor Drive and Load Setup

7.4 Short Circuit Accuracy and Response Time

The shunts used to validate the short circuit alarm are 50 mΩ. The threshold was set to 1.25 A as discussed in Section 4.4. The test setup for short circuit test is shown in Figure 96. The PC GUI is used to set the threshold settings and modulator clock frequency to 8.192-MHz. The initial current in the circuit is set below the threshold value. Upon closing the switch, the current in circuit exceeds 1.25 A.

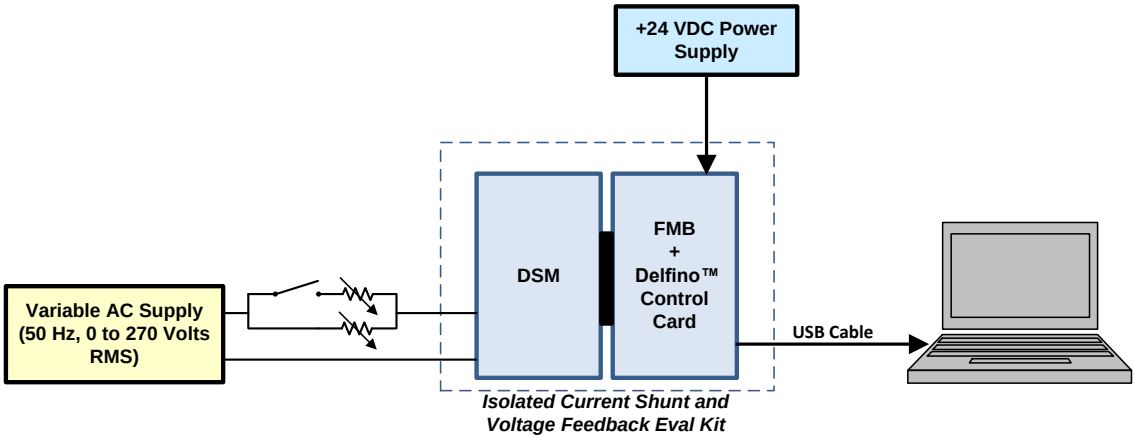


Figure 96. Test Setup for Short Circuit Testing

Figure 97 shows the current waveform captured on an oscilloscope by a current probe when the switch is closed. This waveform is shown in yellow. The second wave form in red is from a GPIO on Jumper J2.10. On the FMB, this GPIO is used to signal the short circuit event. A current probe provides the isolation while measuring signal from different ground references and is needed for conducting this test safely. A modified firmware was used to set the GPIO on high whenever the instantaneous current is above the threshold. This firmware provided a convenient way of checking the short circuit detection for accuracy. To compare the accuracy of the short circuit detection on the graph, the value 1.110 A represents 1.25 A because the current probe had attenuation.

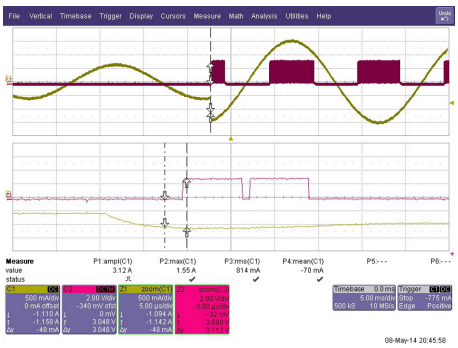


Figure 97. Short Circuit Current Waveform (Yellow) and Signal From MCU (Red) on GPIO1 Pin 10 on J2 Header on FMB Board

In this method, it is difficult to ascertain the exact point where the short circuit event occurred. The waveform shape did change when switch was closed, but at this point the current at the input has not reached the threshold. Do not include the time it takes to reach the threshold value in the external circuit as part of the short circuit response time. Therefore, the design needs an ideal waveform from the source, which provides an instantaneous jump from a low value to above the threshold value. This limitation was overcome by removing the AC source and the shunt and using a signal generator. The signal generator is used to apply a signal at the AMC input representing a short circuit condition. A signal generator is set to a square form with peaks crossing ±62.5 mV to represent an equivalent voltage of 1.25 A.

Figure 98 shows the waveform capture. The blue waveform is from the signal generator, and the yellow waveform is the short circuit signal at GPIO generated by the controller. The edge of the square wave signal from the generator represents the initiation of short circuit. The time difference from the falling edge of the signal generator to the event being detected is 4.4 µs. The theoretical time delay is equal to the time taken to cpmplete one sample conversion by the comparator module in the SDFM peripheral. The oversampling rate set for the comparator is 32; therefore, the time delay is calculated as the time taken to complete 32 modulator clock cycles at 8.192 MHz for a sinc1 filter. This is 1 / (32 × 8.192 Mhz) = 3.8 µs. The additional delay is due to the GPIO rise time and ISR execution time.

Note the input signal and the GPIO signal are on different grounds and can be at different potentials. In the above test, both probes need isolation to test safely. Otherwise, using normal probes on the board cause a short between the two different ground points on the board through the probes. The oscilloscope used in the above test had isolation between channels.

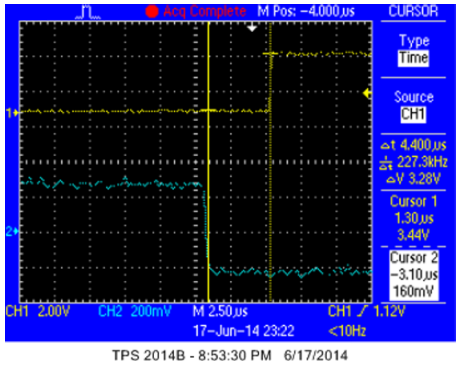


Figure 98. Short Circuit Signal Applied to AMC1304 (Blue) and Signal From MCU (Yellow) on GPIO1 Pin 10 on J2 Header on FMB Board

7.5 Functional Tests

7.5.1 Test Setup

This reference design can be used in combination with the High Voltage Motor Control and PFC Developer's Kit (TMDSHVMTRPFCKIT) from TI to drive a corresponding motor and evaluate this design functionally. This kit has a GUI for the control motor with a speed input.

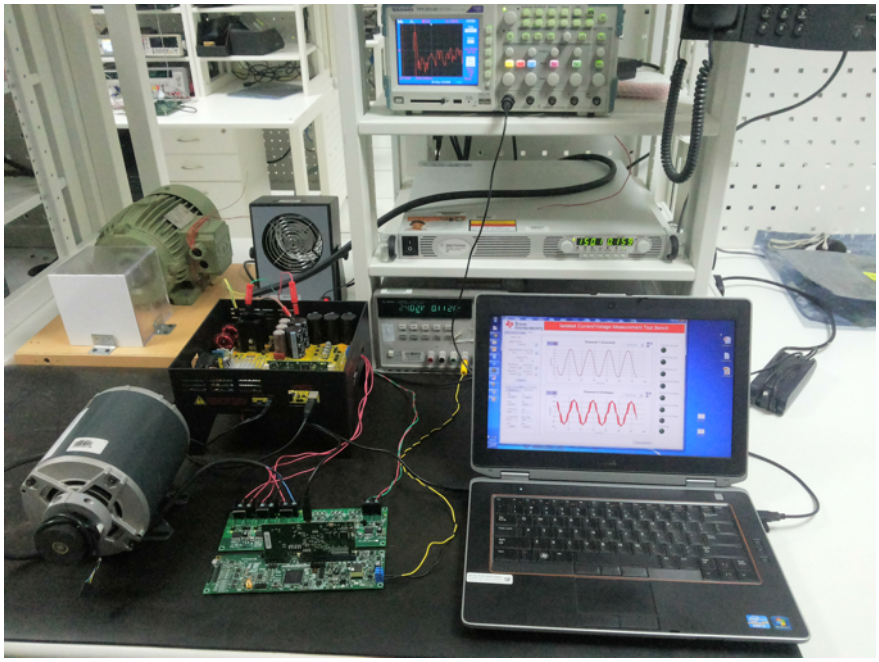


Figure 99. Isolated Current Shunt and Voltage Measurement Eval Kit with HV Invertor Kit and AC Motor

7.5.2 Power Supply

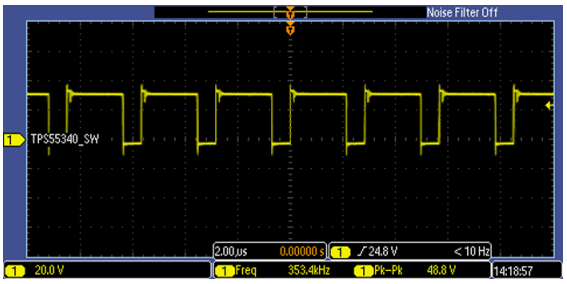


Figure 100. Switch Node Wave Form for TPS5534 24 V to 6 V, DC-DC Converter

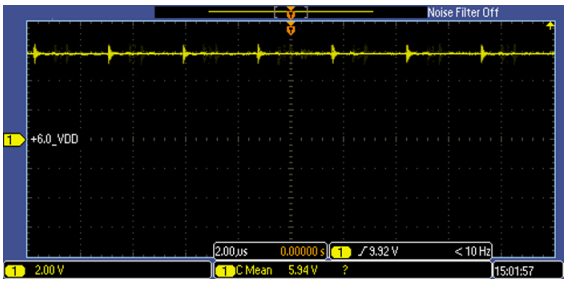


Figure 101. 6.0_VDD Power Rail on FMB Board

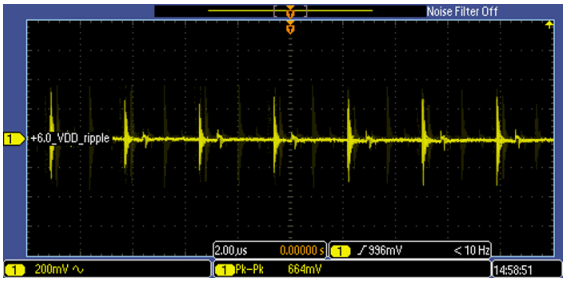


Figure 102. Ripple on 6.0_VDD Power Rail, FMB Board

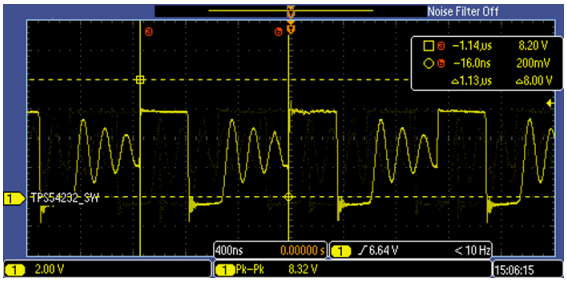


Figure 103. Switch Node Waveform for TPS54232, 6-V to 3.3-V DC-DC Converter, on FMB Board

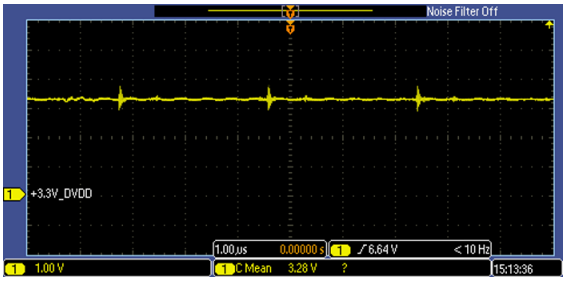


Figure 104. 3.3V_DVDD Power Rail, on FMB Board

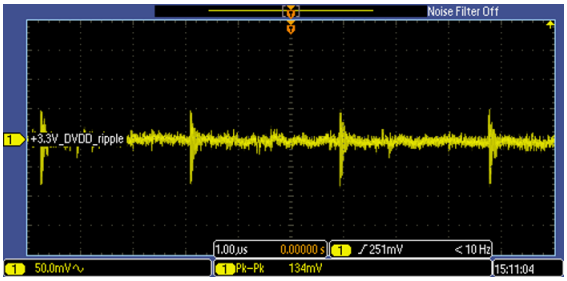


Figure 105. Ripple on 3.3V_DVDD Power Rail, on FMB Board

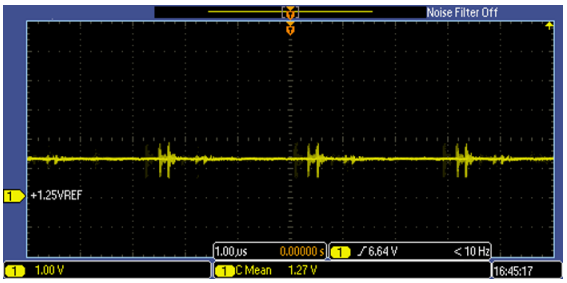


Figure 106. 1.25-V Reference Voltage from REF3012, on FMB Board

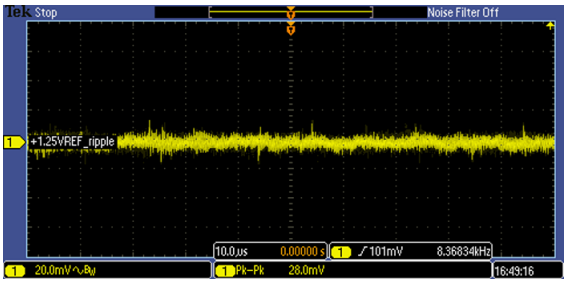


Figure 107. Ripple on 1.25-V Reference Voltage from REF3012, on FMB Board

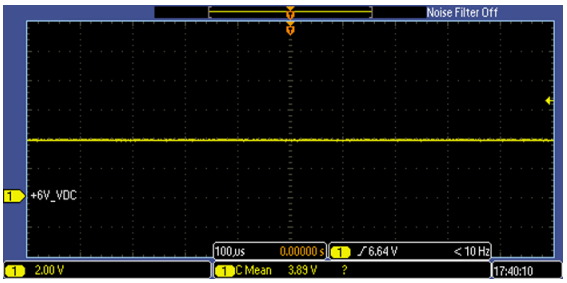


Figure 108. 6V_VDC Power Rail on DSM Board, Measured Across Capacitor C73

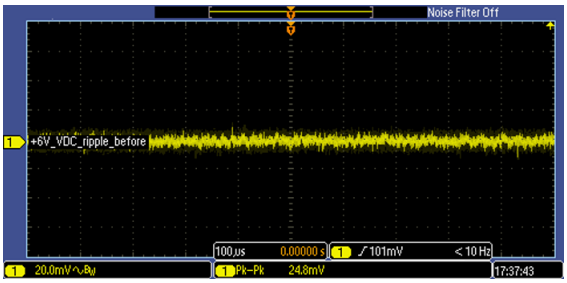


Figure 109. Ripple on 6.0V_VDC Power Rail on DSM Board, Measured Across Capacitor C73, with Motor Turned Off

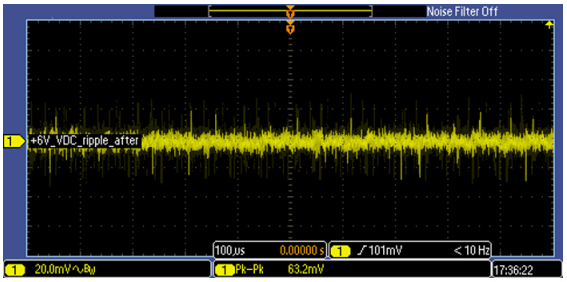


Figure 110. Ripple on 6.0V_VDC Power Rail on DSM Board, Measured Across Capacitor C73, with Motor Turned On

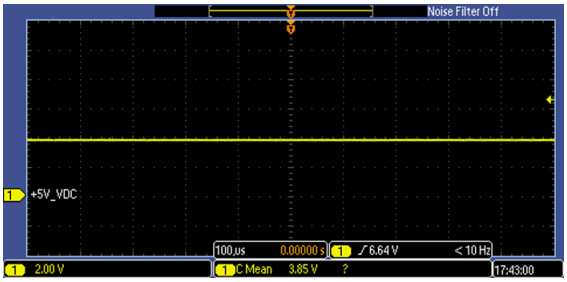


Figure 111. 5.0V_VDC Power Rail on DSM Board

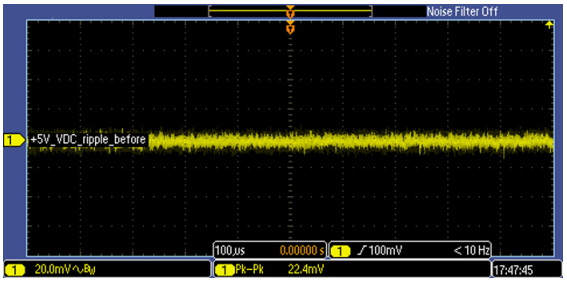


Figure 112. Ripple on 5.0V_PH Power Rail on DSM Board, Measured Across Capacitor C96, with Motor Turned Off

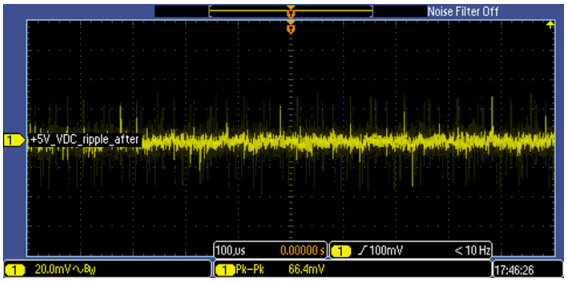


Figure 113. Ripple on 5.0V_PH Power Rail on DSM Board, Measured Across Capacitor C96, with Motor Turned On

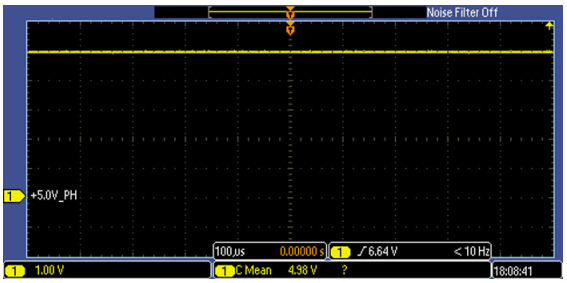


Figure 114. 5.0V_PH Power Rail on DSM Board, Measured Across Capacitor C103, with Motor Turned On

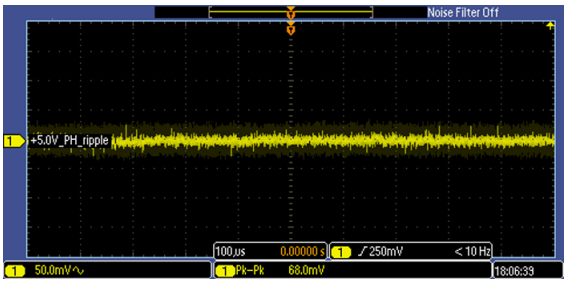


Figure 115. Ripple on 5.0V_PH Power Rail on DSM Board, Measured Across Capacitor C103, with Motor Turned On

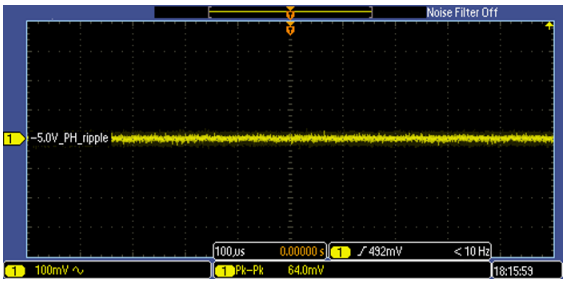


Figure 116. –5.0V_PH Power Rail on DSM Board, Measured Across Capacitor C84, with Motor Turned On

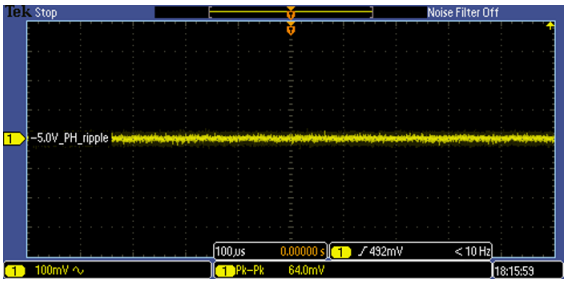


Figure 117. Ripple on –5.0V_PH Power Rail on DSM Board, Measured Across Capacitor C84, with Motor Turned On

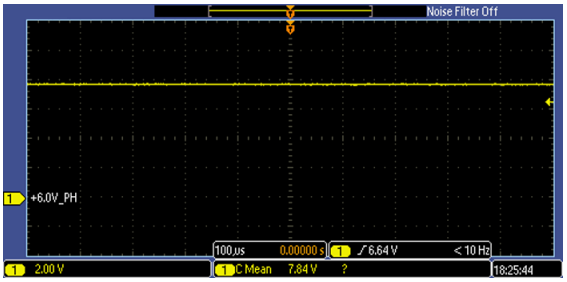


Figure 118. 6.0V_PH Power Rail on DSM Board, Measured Across Capacitor C107, with Motor Turned On

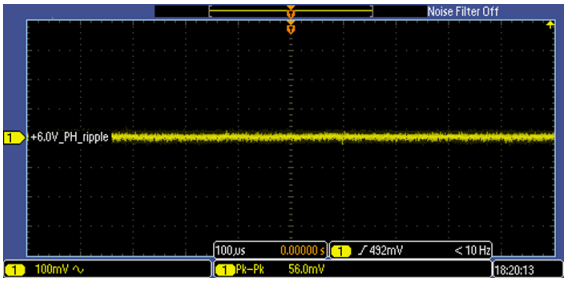


Figure 119. Ripple on 6V_PH Power Rail on DSM Board, Measured Across Capacitor C107, with Motor Turned On

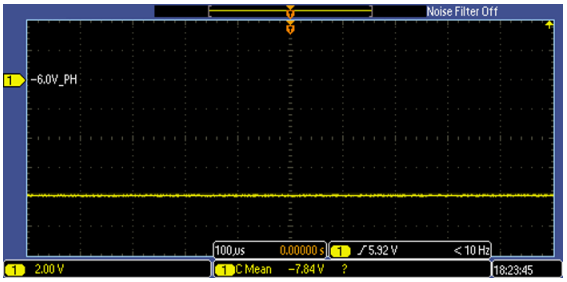


Figure 120. –6.0V_PH Power Rail on DSM Board, Measured Across Capacitor C83, with Motor Turned On

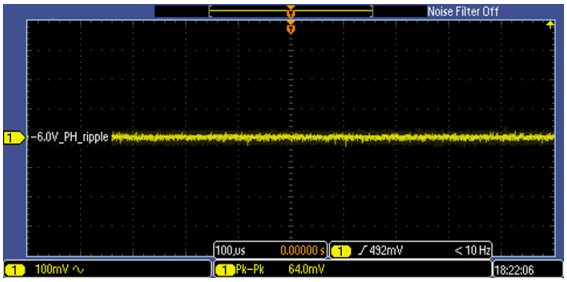


Figure 121. Ripple on –6V_PH Power Rail on DSM Board, Measured Across Capacitor C83, with Motor Turned On

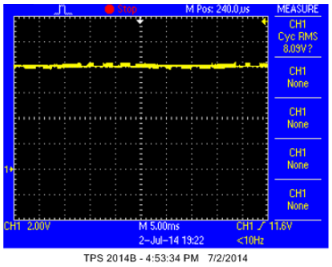


Figure 122. 6V_USH Power Rail on DSM Board, Measured Across Capacitor C28, with Motor Turned On

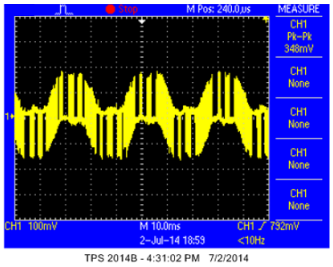


Figure 123. Ripple on 6.0V_USH Power Rail on DSM Board, Measured Across Capacitor C28, with Motor Turned On

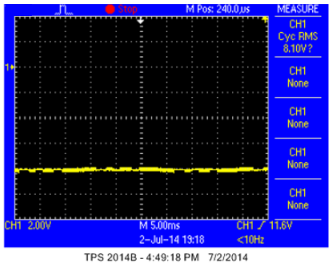


Figure 124. –6.0V_USH Power Rail on DSM Board, Measured Across Capacitor C33, with Motor Turned On

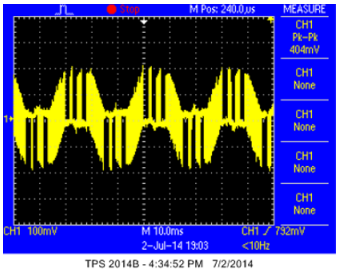


Figure 125. Ripple on –6.0V_USH Power Rail on DSM Board, Measured Across Capacitor C33, with Motor Turned On

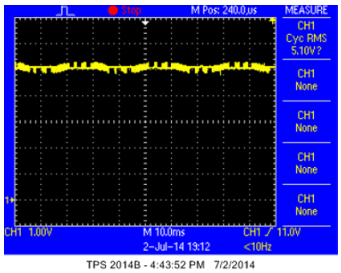


Figure 126. 5.0V_USH Power Rail on DSM Board, Measured Across Capacitor C38, with Motor Turned On

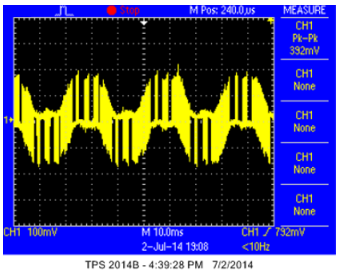


Figure 127. Ripple on 5.0V_USH Power Rail on DSM Board, Measured Across Capacitor C38, with Motor Turned On

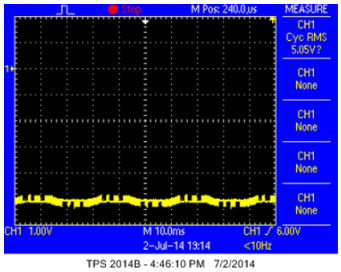


Figure 128. –5.0V_USH Power Rail on DSM Board, Measured Across Capacitor C51, with Motor Turned On

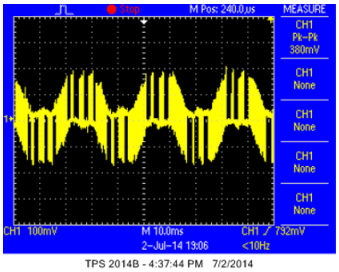


Figure 129. Ripple on –5.0V_USH Power Rail on DSM Board, Measured Across Capacitor C51, with Motor Turned On

7.5.3 AMC1304 Clock and Data Graphs

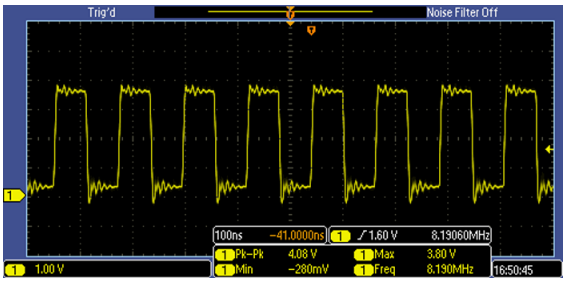


Figure 130. Input Clock to AMC1304

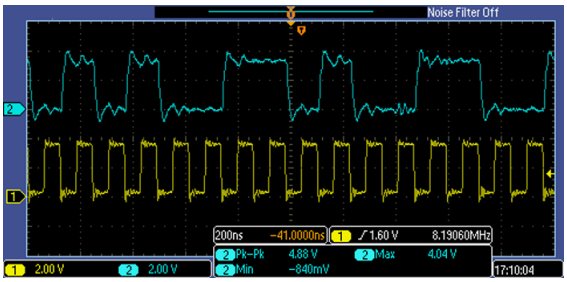


Figure 131. Data out of AMC1304 (Blue Wave Form) and Input Clock (Yellow Wave Form)

7.5.4 DAC Output Signal

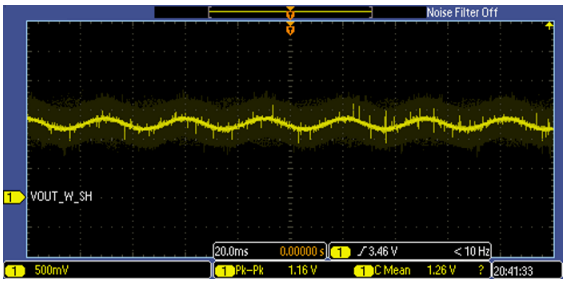


Figure 132. DAC Output, VOUT_W_SH, with Shunt Value of 5 mΩ

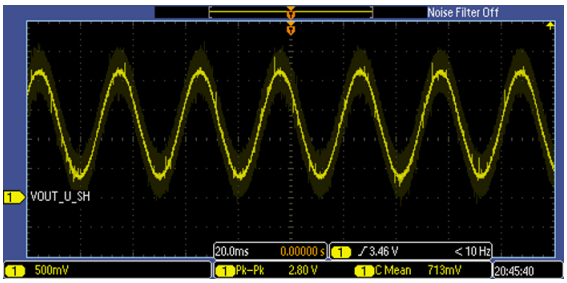


Figure 133. DAC Output, VOUT_U_SH, with Shunt Value of 50 mΩ

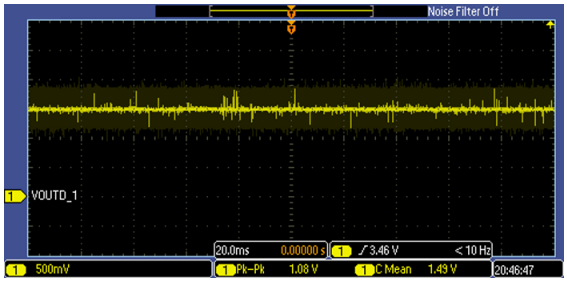


Figure 134. DAC Output, VOUTD_1; Represents the DC Link Voltage; DC Link Voltage was 150 V

7.6 EMC Test Results

The design was tested according to IEC61800-3 standards for ESD, EFT, and Surge with reference to IEC61000-4-2, IEC61000-4-4. and IEC61000-4-5 standards, respectively. See EMC test results document at TIDA-00171.

8 Design Files

8.1 Schematics

To download the schematics, see the design files at TIDA-00171.

8.1.1 DSM

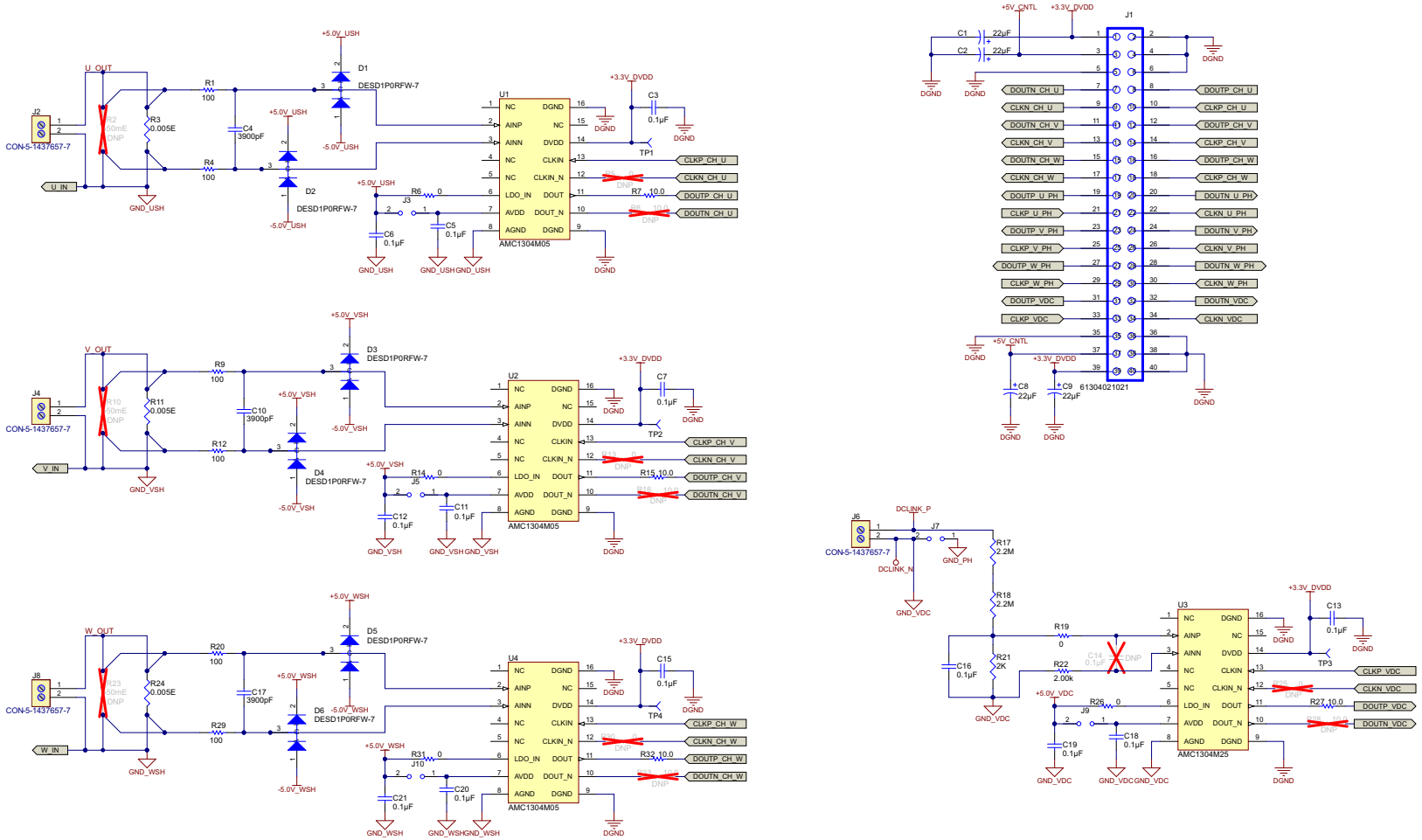


Figure 135. Current Sense Schematic

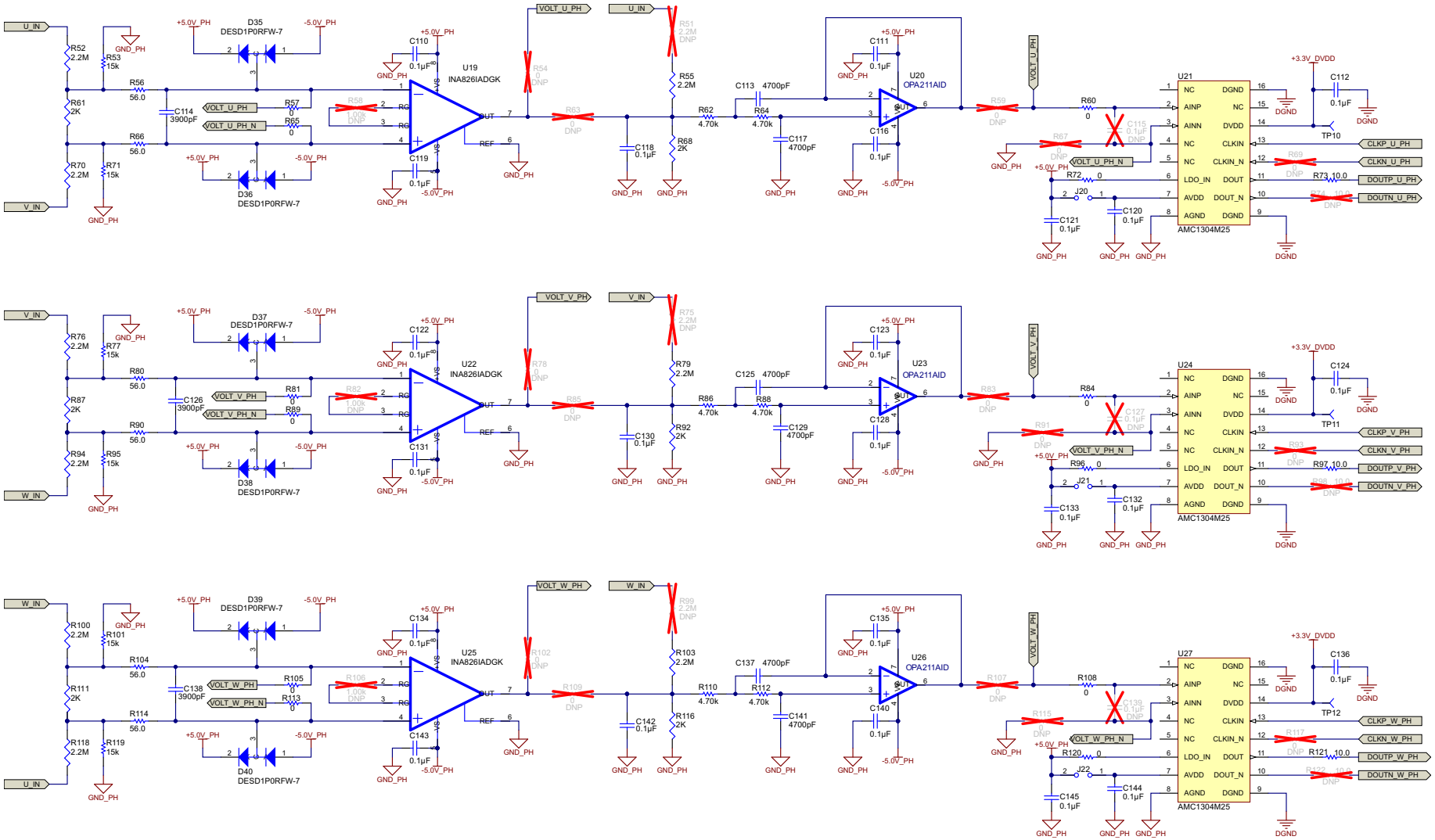


Figure 136. Voltage Conditioning Schematic

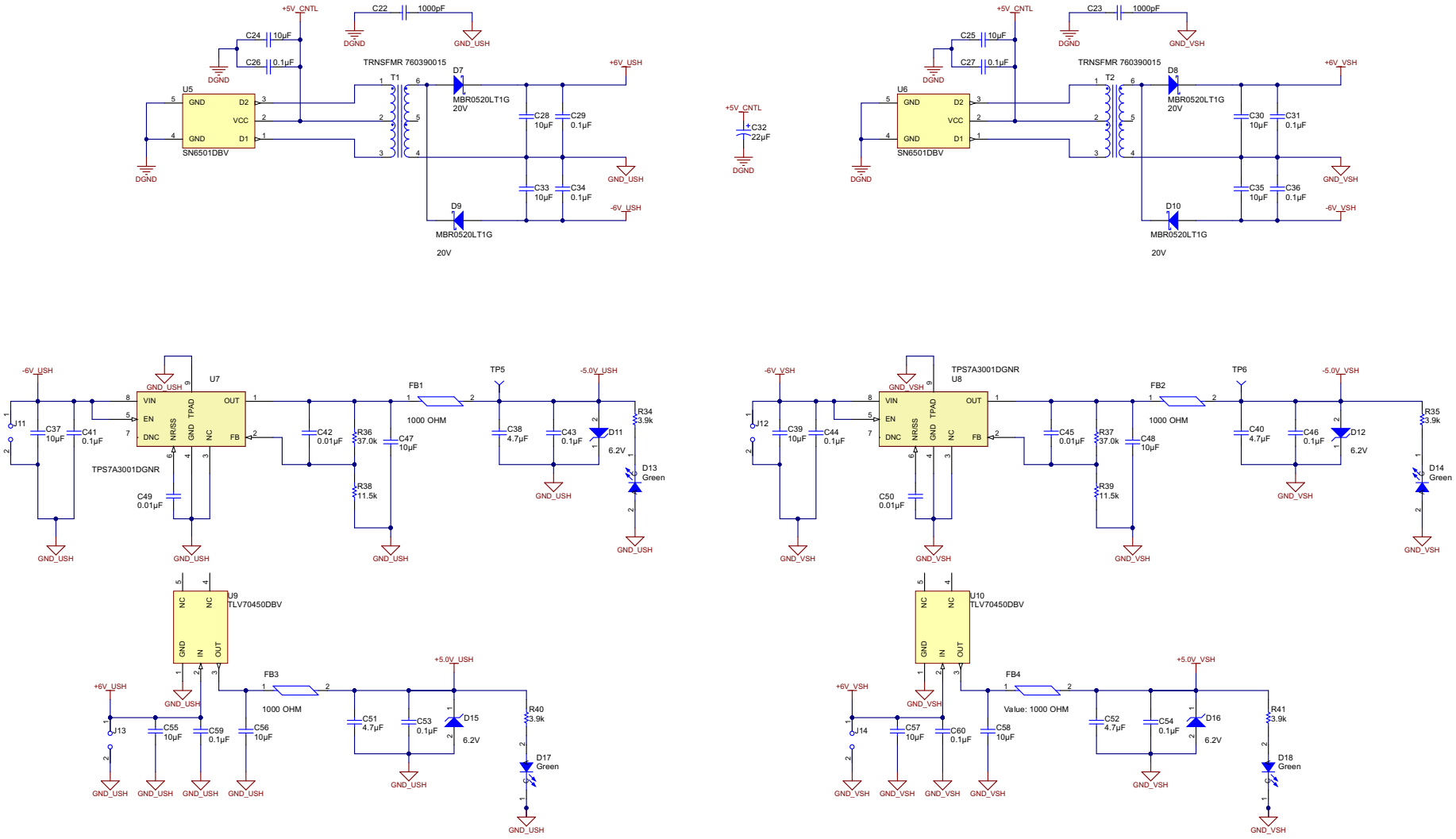


Figure 137. Power Supply 1 Schematic

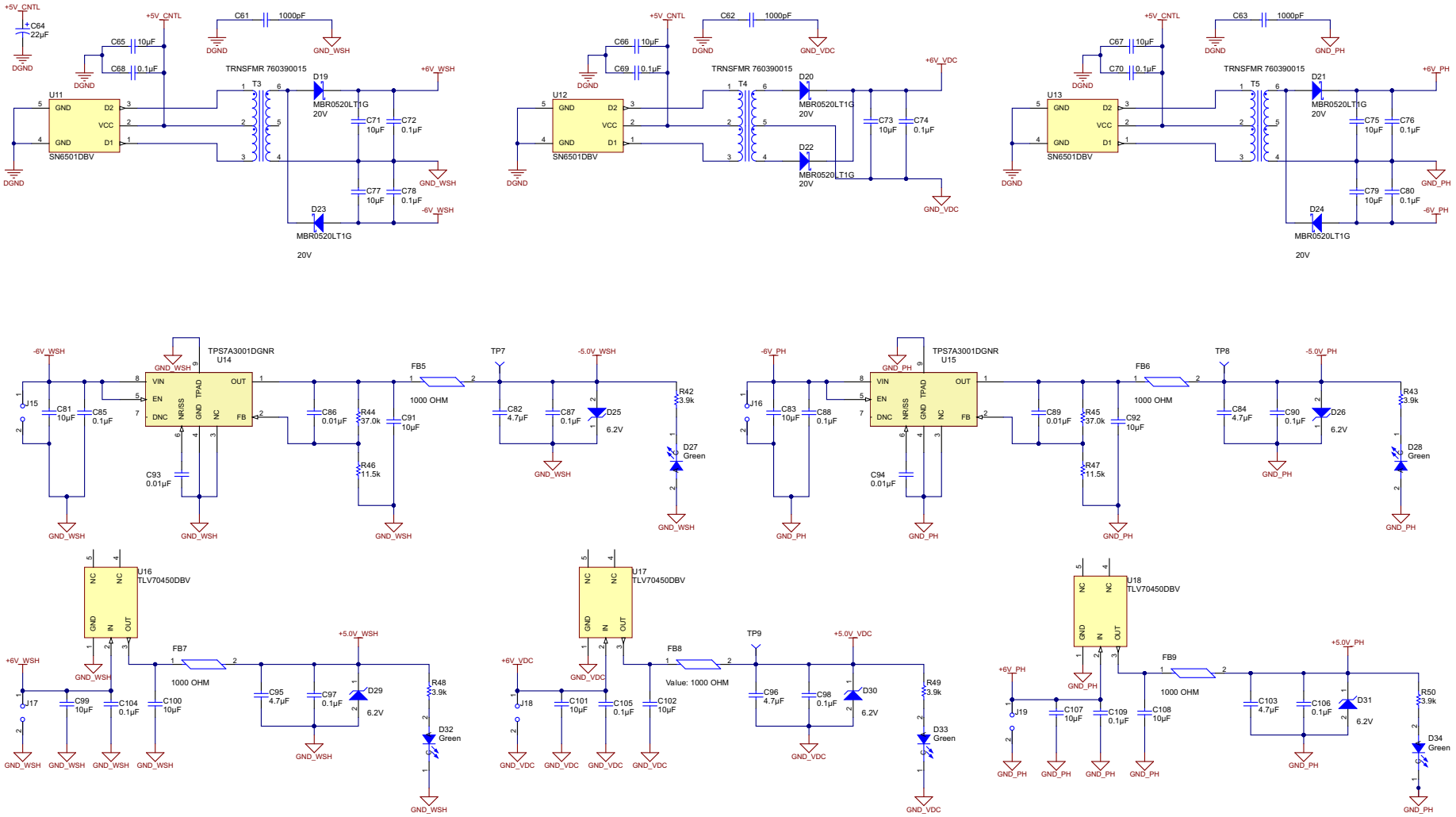


Figure 138. Power Supply 2 Schematic

8.1.2 FMB

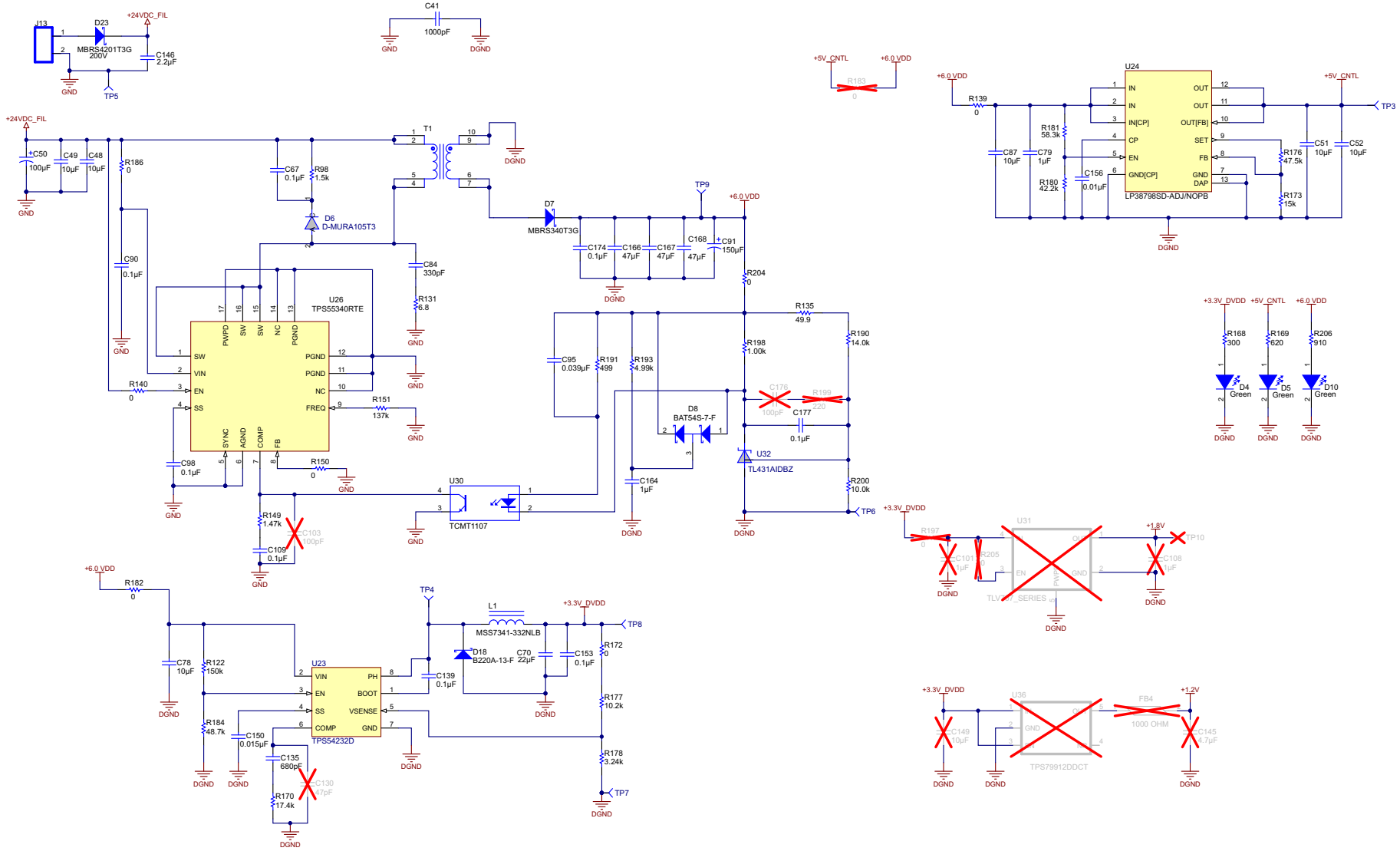


Figure 139. Power Supply Schematic

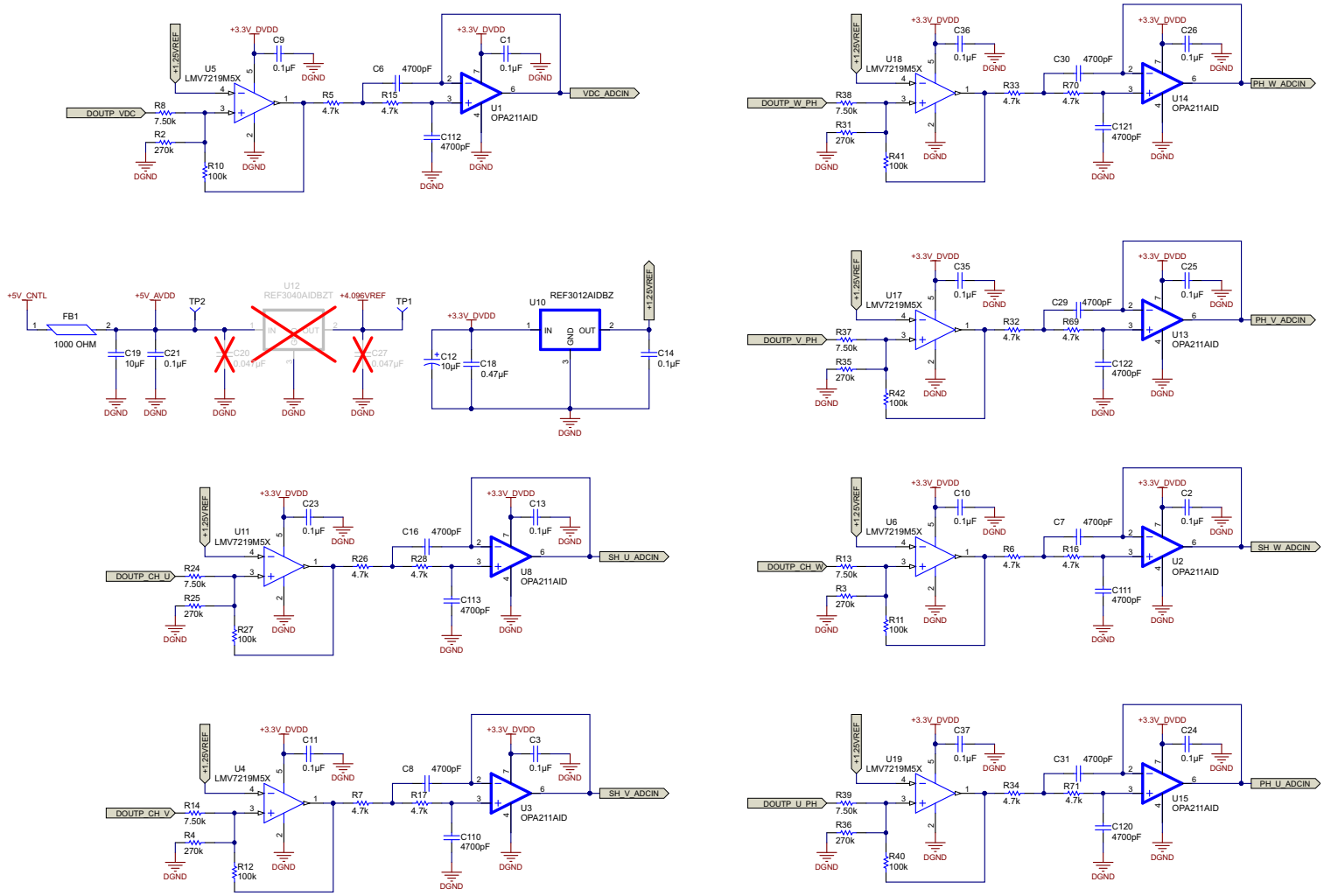


Figure 140. SDM OP Filtering Schematic

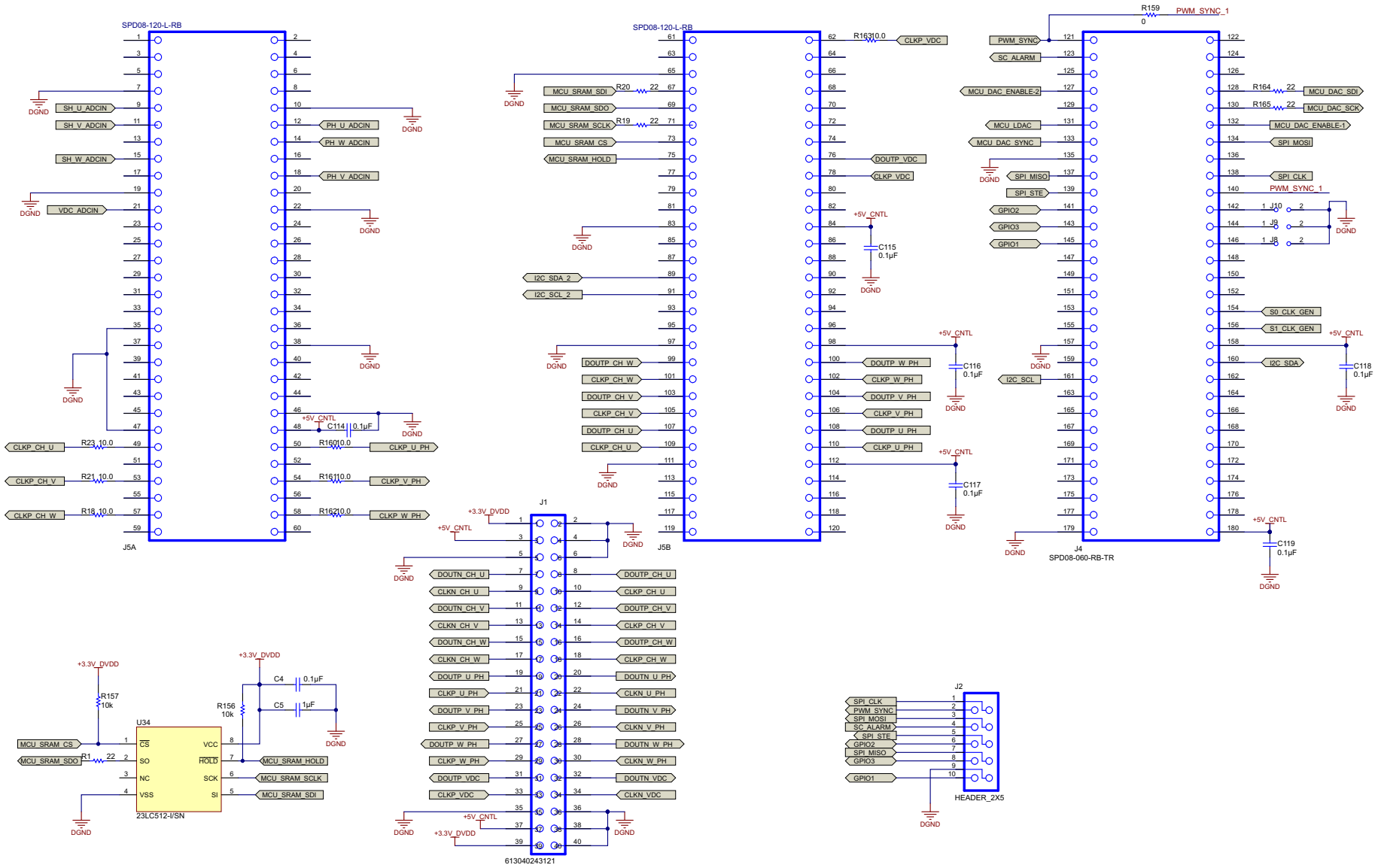


Figure 141. Control Card Connector

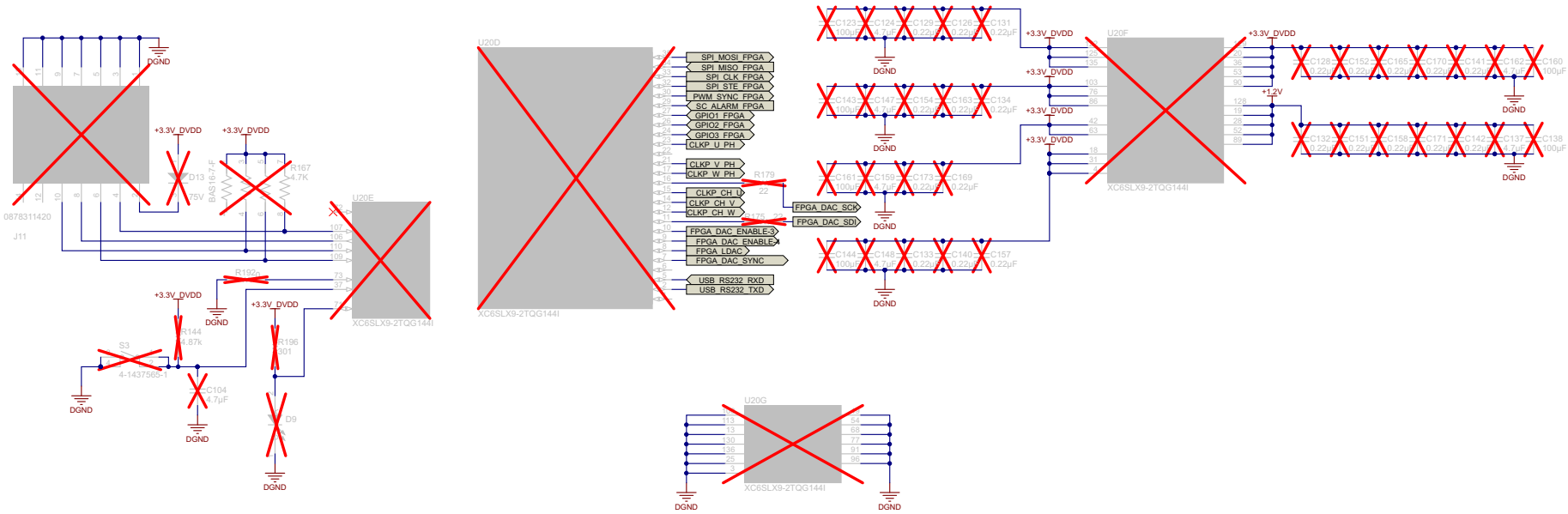


Figure 142. FGPA Power Schematic

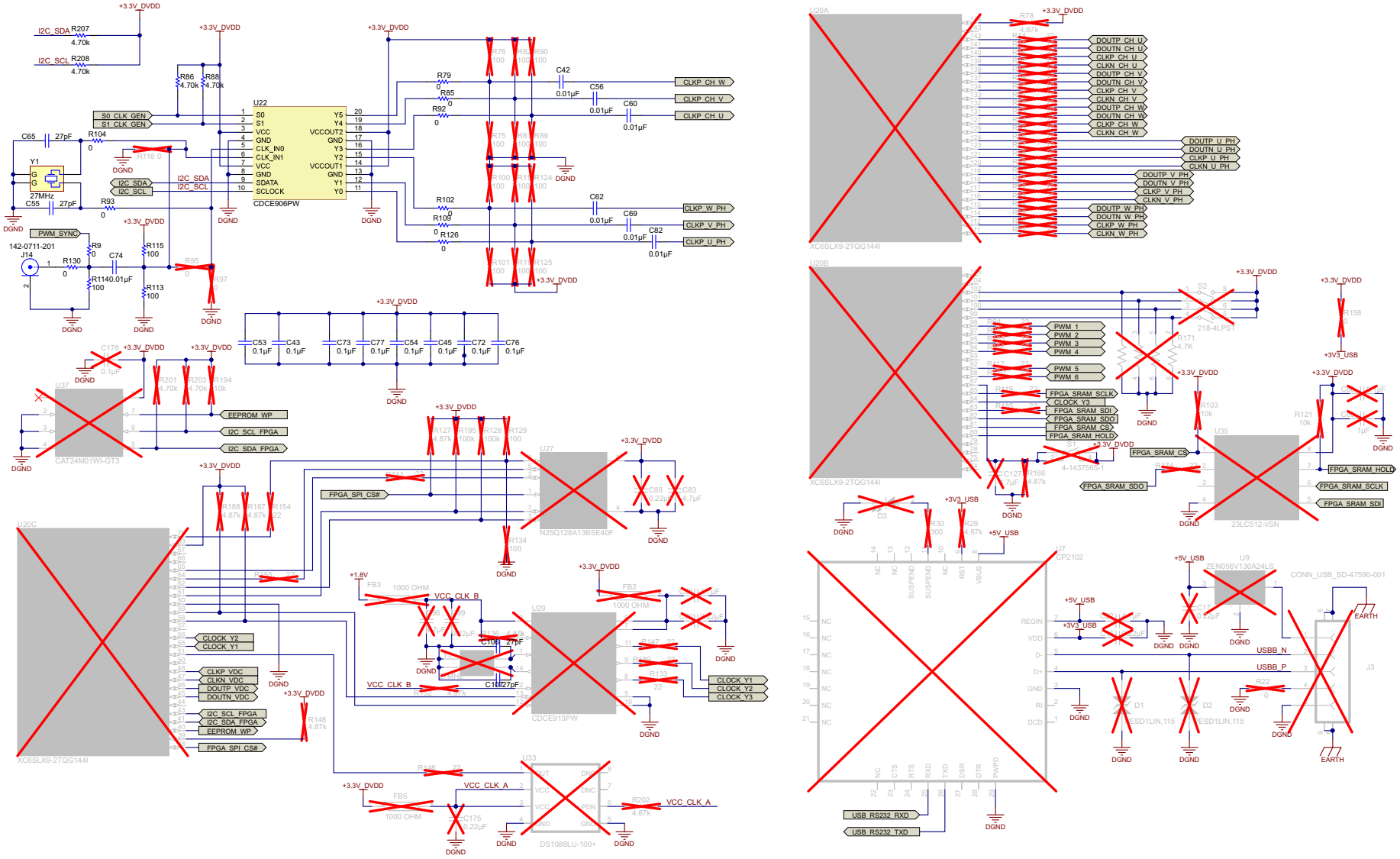


Figure 143. FGPA Clock USB Schematic

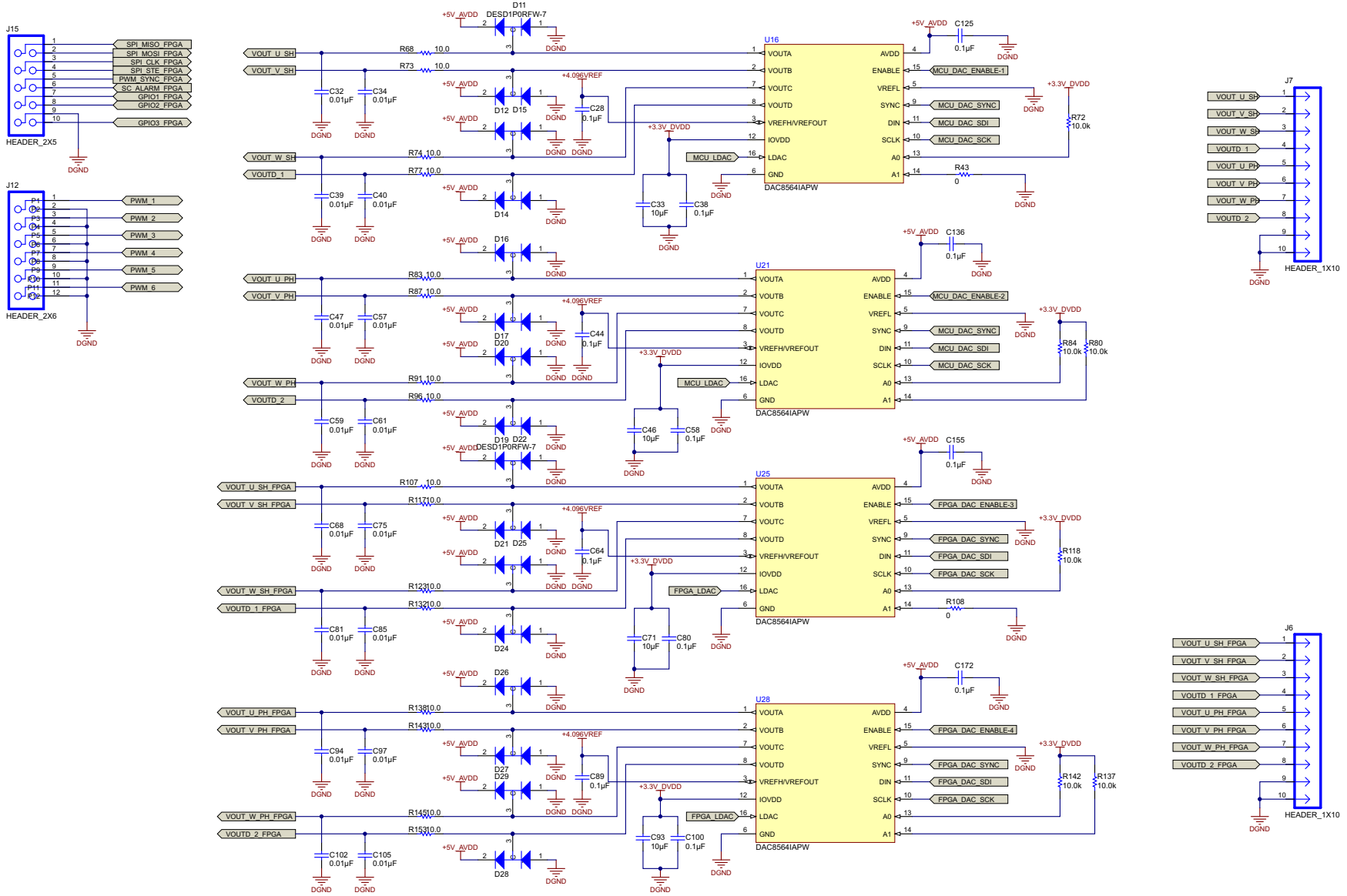


Figure 144. DAC Schematic

8.2 BOM

To download the bill of materials (BOM), see the design files at TIDA-00171.

Table 16. DSM Bill of Materials

QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER	MANUFACTURER PN	PCB FOOTPRINT	NOTE
6	C1, C2, C8, C9, C32, C64	CAP, AL, 22 µF, 25 V, ±20%, 0.76 Ω, SMD	Nichicon	UUD1E220MCL1GS	5x5.8	Fitted
7	C3, C7, C13, C15, C112, C124, C136	CAP, CERM, 0.1 µF, 25 V, ±5%, X7R, 0603	AVX	06033C104JAT2A	0603	Fitted
6	C4, C10, C17, C114, C126, C138	CAP, CERM, 3900 pF, 25 V, ±5%, C0G/NP0, 0603	TDK	C1608C0G1E392J	0603	Fitted
62	C5, C6, C11, C12, C16, C18, C19, C20, C21, C26, C27, C29, C31, C34, C36, C41, C43, C44, C46, C53, C54, C59, C60, C68, C69, C70, C72, C74, C76, C78, C80, C85, C87, C88, C90, C97, C98, C104, C105, C106, C109, C110, C111, C116, C118, C119, C120, C121, C122, C123, C128, C130, C131, C132, C133, C134, C135, C140, C142, C143, C144, C145	CAP, CERM, 0.1 µF, 50 V, ±10%, X7R, 0603	Kemet	C0603C104K5RACTU	0603	Fitted
5	C22, C23, C61, C62, C63	CAP, CERM, 1000 pF, 2 KV 10% X7R 1206	Johanson Dielectrics Inc	202R18W102KV4E	1206	Fitted
32	C24, C25, C28, C30, C33, C35, C37, C39, C47, C48, C55, C56, C57, C58, C65, C66, C67, C71, C73, C75, C77, C79, C81, C83, C91, C92, C99, C100, C101, C102, C107, C108	CAP, CERM, 10 µF, 35 V, ±20%, X7R, 1210	Taiyo Yuden	GMK325AB7106MM-T	1210	Fitted
9	C38, C40, C51, C52, C82, C84, C95, C96, C103	CAP, CERM, 4.7 µF, 50 V, ±10%, X5R, 0805	TDK	C2012X5R1H475K125AB	0805	Fitted
8	C42, C45, C49, C50, C86, C89, C93, C94	CAP, CERM, 0.01 µF, 100V, ±5%, X7R, 0603	AVX	06031C103JAT2A	0603	Fitted
6	C113, C117, C125, C129, C137, C141	CAP, CERM, 4700 pF, 100 V, ±10%, X7R, 0603	AVX	06031C472KAT2A	0603	Fitted
2	D1, D2	Diode, P-N, 70 V, 0.2 A, SOT-323	Diodes Inc	DESD1P0RFW-7	SOT-323	Fitted
10	D3, D4, D5, D6, D35, D36, D37, D38, D39, D40	Diode, P-N, 70 V, 0.2 A, SOT-323	Diodes Inc	DESD1P0RFW-7	SOT-323	Fitted
10	D7, D8, D9, D10, D19, D20, D21, D22, D23, D24	Diode, Schottky, 20 V, 0.5 A, SOD-123	ON Semiconductor	MBR0520LT1G	SOD-123	Fitted
9	D11, D12, D15, D16, D25, D26, D29, D30, D31	Diode, Zener, 6.2 V, 1 W, PowerDI123	Diodes Inc.	DFLZ6V2-7	PowerDI123	Fitted

Table 16. DSM Bill of Materials (continued)

QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER	MANUFACTURER PN	PCB FOOTPRINT	NOTE
9	D13, D14, D17, D18, D27, D28, D32, D33, D34	LED SmartLED Green 570NM	OSRAM	LG L29K-G2J1-24-Z	0603	Fitted
9	FB1, FB2, FB3, FB4, FB5, FB6, FB7, FB8, FB9	Ferrite Chip 1000 Ω 300 MA 0603	TDK Corporation	MMZ1608B102C	0603	Fitted
5	FID4, FID5, FID6, FID7, FID8	Fiducial mark. There is nothing to buy or mount.	N/A	N/A	Fiducial	Fitted
1	J1	Connector, Right Angle 2×20 pin, 100-mil spacing	WURTH ELEKTRONIK	61304021021		Fitted
4	J2, J4, J6, J8	Terminal Block, 4×1, 2.54 mm, TH	TE Connectivity	5-1437657-7	TERM_BLK, 2pos, 2.54 mm	Fitted
17	J3, J5, J7, J9, J10, J11, J12, J13, J14, J15, J16, J17, J18, J19, J20, J21, J22	Header, Male 2-pin, 100-mil spacing,	Sullins	PEC02SAAN	0.100 inch × 2	Fitted
1	LBL1	Thermal Transfer Printable Labels, 0.650" W × 0.200" H - 10,000 per roll	Brady	THT-14-423-10	PCB Label 0.650"H × 0.200"W	Fitted
4	MH1, MH2, MH3, MH4	Mounting hole, NPTH Drill 3.2 mm			Screw	Fitted
6	R1, R4, R9, R12, R20, R29	RES, 100 Ω, 1%, 0.1 W, 0603	Yageo America	RC0603FR-07100RL	0603	Fitted
6	R56, R66, R80, R90, R104, R114	RES, 56.0 Ω, 1%, 0.1 W, 0603	Yageo America	RC0603FR-0756RL	0603	Fitted
3	R3, R11, R24	RES Metal .005 Ω, 5 W, 1% Radial	TT Electronics/IRC	OAR5R005FLF	Radial	Fitted
17	R6, R14, R19, R26, R31, R57, R60, R65, R72, R81, R84, R89, R96, R105, R108, R113, R120	RES, 0 Ω, 5%, 0.1 W, 0603	Vishay-Dale	CRCW06030000Z0EA	0603	Fitted
7	R7, R15, R27, R32, R73, R97, R121	RES, 10.0 Ω, 1%, 0.1 W, 0603	Vishay-Dale	CRCW060310R0FKEA	0603	Fitted
11	R17, R18, R52, R55, R70, R76, R79, R94, R100, R103, R118	RES 2.2 MΩ, 1/3 W 1% 1210	Rohm Semiconductor	KTR25JZPF2204	1210	Fitted
7	R21, R61, R68, R87, R92, R111, R116	RES 2 KΩ, 1/3 W, 1% 1210	Rohm Semiconductor	KTR25JZPF2001	1210	Fitted
1	R22	RES, 2.00 kΩ, 0.5%, 0.1 W, 0603	Yageo America	RT0603DRE072KL	0603	Fitted
9	R34, R35, R40, R41, R42, R43, R48, R49, R50	RES, 3.9 kΩ, 5%, 0.1 W, 0603	Vishay-Dale	CRCW06033K90JNEA	0603	Fitted
4	R36, R37, R44, R45	RES, 37.0 kΩ, 0.1%, 0.1 W, 0603	Yageo America	RT0603BRD0737KL	0603	Fitted
4	R38, R39, R46, R47	RES, 11.5 kΩ, 1%, 0.1 W, 0603	Vishay-Dale	CRCW060311K5FKEA	0603	Fitted
6	R53, R71, R77, R95, R101, R119	RES 15.0 kΩ, 1/10 W, .1% SMD 0603	Yageo America	RT0603BRD0715KL-ND	0603	Fitted
6	R62, R64, R86, R88, R110, R112	RES, 4.70 kΩ, 1%, 0.1 W, 0603	Yageo America	RC0603FR-074K7L	0603	Fitted

Table 16. DSM Bill of Materials (continued)

QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER	MANUFACTURER PN	PCB FOOTPRINT	NOTE
5	T1, T2, T3, T4, T5	Transformer 475 µH SMD	Wurth Electronics Midcom	750342271	10.05-mm L × 6.73-mm W	Fitted
12	TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP11, TP12	Test Point, 0.040 Hole	STD	STD		Fitted
4	U3,U21,U24,U27	20 MHz, Isolated Delta-Sigma Modulator, CMOS interface	Texas Instruments	AMC1304M25	DW0016A	Fitted
3	U1,U2,U4	20 MHz, Isolated Delta-Sigma Modulator, CMOS interface	Texas Instruments	AMC1304M05	DW0016A	Fitted
5	U5, U6, U11, U12, U13	Transformer Driver for Isolated Power Supplies, DBV0005A	Texas Instruments	SN6501DBV	DBV0005A	Fitted
4	U7, U8, U14, U15	–36 V, –200 mA, Ultralow-Noise, Negative Linear Regulator	Texas Instruments	TPS7A3001DGNR	MSOP-PowerPAD (DGN) | 8	Fitted
5	U9, U10, U16, U17, U18	Regulator, LDO, 5 V, 0.15 A, SOT23-5	Texas Instruments	TLV70450DBV	DBV0005A	Fitted
3	U19, U22, U25	IC, Precision, 200 µA, 36-V Supply Instrument Amplifier.	Texas Instruments	INA826IADGK	MSOP-8	Fitted
3	U20, U23, U26	IC, 1.1-nV/vHz Noise, Low Power, Precision Op-Amp	Texas Instruments	OPA211AID	SO	Fitted
0	C14, C115, C127, C139	CAP, CERM, 0.1 µF, 50 V, ±10%, X7R, 0603	Kemet	C0603C104K5RACTU	0603	Not Fitted
0	FID1, FID2, FID3	Fiducial mark. There is nothing to buy or mount.	N/A	N/A	Fiducial	Not Fitted
0	R2, R10, R23	RES 50 mΩ, 3 W, .5% TO-247 TH	ISOTEK	PBH-R050-F1-0.5	TO-247	Not Fitted
0	R5, R13, R25, R30, R54, R59, R63, R67, R69, R78, R83, R85, R91, R93, R102, R107, R109, R115, R117	RES, 0 Ω, 5%, 0.1 W, 0603	Vishay-Dale	CRCW06030000Z0EA	0603	Not Fitted
0	R8, R16, R28, R33, R74, R98, R122	RES, 10.0 Ω, 1%, 0.1 W, 0603	Vishay-Dale	CRCW060310R0FKEA	0603	Not Fitted
0	R51, R75, R99	RES 2.2 MΩ, 1/3 W, 1% 1210	Rohm Semiconductor	KTR25JZPF2204	1210	Not Fitted
0	R58, R82, R106	RES, 1.00 kΩ, 1%, 0.1 W, 0603	Yageo America	RC0603FR-071KL	0603	Not Fitted

Table 17. FMB Bill of Materials

QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER	MANUFACTURER PN	PCB FOOTPRINT	NOTE
37	C1, C2, C3, C9, C10, C11, C13, C21, C23, C24, C25, C26, C28, C35, C36, C37, C38, C44, C58, C64, C67, C80, C89, C90, C100, C109, C114, C115, C116, C117, C118, C119, C125, C136, C155, C172, C177	CAP, CERM, 0.1 µF, 50 V, ±10%, X7R, 0603	Kemet	C0603C104K5RACTU	0603	Fitted
2	C4, C139	CAP, CERM, 0.1 µF, 16 V, ±5%, X7R, 0603	AVX	0603YC104JAT2A	0603	Fitted
1	C5	CAP, CERM, 1 µF, 16 V, ±10%, X5R, 0603	TDK	C1608X5R1C105K080AA	0603	Fitted
14	C6, C7, C8, C16, C29, C30, C31, C110, C111, C112, C113, C120, C121, C122	CAP, CERM, 4700 pF, 100 V, ±10%, X7R, 0603	AVX	06031C472KAT2A	0603	Fitted
1	C12	CAP, AL, 10 µF, 16 V, ±20%, 3 Ω, SMD	Panasonic	EEEFC1C100R	SMT Radial B	Fitted
9	C14, C43, C45, C53, C54, C72, C73, C76, C77	CAP, CERM, 0.1 µF, 25 V, ±5%, X7R, 0603	AVX	06033C104JAT2A	0603	Fitted
1	C18	CAP, CERM, 0.47 µF, 16 V, ±10%, X7R, 0805	AVX	0805YC474KAT2A	0805	Fitted
5	C19, C33, C46, C71, C93	CAP, CERM, 10 µF, 35 V, ±20%, X7R, 1210	Taiyo Yuden	GMK325AB7106MM-T	1210	Fitted
16	C32, C34, C39, C40, C47, C57, C59, C61, C68, C75, C81, C85, C94, C97, C102, C105	CAP, CERM, 0.01 µF, 100 V, ±5%, X7R, 0603	AVX	06031C103JAT2A	0603	Fitted
1	C41	CAP, CERM, 1000 pF, 2 KV, 10% X7R 1206	Johanson Dielectrics Inc	202R18W102KV4E	1206	Fitted
7	C42, C56, C60, C62, C69, C74, C82	CAP, CERM, 0.01 µF, 100 V, ±10%, X7R, 0603	AVX	06031C103KAT2A	0603	Fitted
2	C48, C49	CAP, CERM, 10 µF, 50 V, ±10%, X7R, 1210	MuRata	GRM32ER71H106KA12L	1210	Fitted
1	C50	CAP, AL, 100 µF, 50 V, ±20%, 0.17 Ω, TH	Nichicon	UHE1H101MPD1TD	8.0 × 10.5 mm	Fitted
3	C51, C52, C87	CAP, CERM, 10µF, 16 V, ±10%, X7R, 1206	MuRata	GRM31CR71C106KAC7L	1206	Fitted
4	C55, C65, C106, C107	CAP, CERM, 27 pF, 50 V, ±5%, C0G/NP0, 0603	AVX	06035A270JAT2A	0603	Fitted
1	C70	CAP, CERM, 22 µF, 10 V, ±20%, X5R, 1210	TDK	C3225X5R1A226M230AA	1210	Fitted
1	C78	CAP, CERM, 10 µF, 35 V, ±10%, X7R, 1206	Taiyo Yuden	GMK316AB7106KL-TR	1206	Fitted
1	C79	CAP, CERM, 1 µF, 25 V, ±10%, X7R, 1206	AVX	12063C105KAT2A	1206	Fitted
1	C84	CAP, CERM, 330 pF, 50 V, ±5%, C0G/NP0, 0603	AVX	06035A331JAT2A	0603	Fitted
1	C91	CAP, AL, 150 µF, 16 V, ±20%, 0.34 Ω, SMD	Nichicon	EEEFK1C151XP	6.3x7.7	Fitted
1	C95	CAP, CERM, 0.039 µF, 50 V, ±10%, X7R, 0603	MuRata	06035C393KAT2A	0603	Fitted
1	C98	CAP, CERM, 0.1 µF, 50 V, ±10%, X7R, 0603	AVX	06035C104KAT2A	0603	Fitted
1	C135	CAP, CERM, 680 pF, 25 V, ±5%, C0G/NP0, 0603	MuRata	MCMT18N681F250CT	0603	Fitted
1	C146	CAP, CERM, 2.2 µF, 100 V, ±10%, X7R, 1210	MuRata	GRM32ER72A225KA35L..	1210	Fitted
1	C150	CAP, CERM, 0.015 µF, 16 V, ±10%, X7R, 0603	MuRata	MC0603B153K160CT	0603	Fitted
2	C153, C174	CAP, CERM, 0.1 µF, 10 V, ±10%, X7R, 0603	Kemet	0603ZC104KAT2A	0603	Fitted
1	C156	CAP, CERM, 0.01 µF, 50 V, ±10%, X7R, 0805	AVX	08055C103KAT2A	0805	Fitted
1	C164	CAP, CERM, 1 µF, 16 V, ±10%, X5R, 0603	Kemet	C0603C105K4PACTU	0603	Fitted
3	C166, C167, C168	CAP, CERM, 47 µF, 10 V, ±10%, X5R, 1210	MuRata	GRM32ER61A476KE20L	1210	Fitted
3	D4, D5, D10	LED SmartLED Green 570 NM 0603	OSRAM Opto Semiconductors Inc	KPT-1608CGCK	0603	Fitted
1	D6	Rectifier, Ultrafast Power, 50 V, 1 A	On Semi	MURA105T3G	403D	Fitted
1	D7	Diode, Schottky, 40 V, 3 A, SMC	ON Semiconductor	MBRS340T3G	SMC	Fitted

Table 17. FMB Bill of Materials (continued)

QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER	MANUFACTURER PN	PCB FOOTPRINT	NOTE
1	D8	Diode, Schottky, 30 V, 0.2 A, SOT-23	Diodes Inc.	BAT54S-7-F	SOT-23	Fitted
16	D11, D12, D14, D15, D16, D17, D19, D20, D21, D22, D24, D25, D26, D27, D28, D29	Diode, P-N, 70 V, 0.2 A, SOT-323	Diodes Inc		SOT-323	Fitted
1	D18	Diode, Schottky, 20 V, 2 A, SMA	Diodes Inc.	B220A-13-F	SMA	Fitted
1	D23	Diode, Schottky, 200 V, 4 A, SMC	ON Semiconductor	MBRS4201T3G	SMC	Fitted
1	FB1	Ferrite Chip 1000 Ω, 300 MA 0603	TDK Corporation		0603	Fitted
1	J1	Connector, Right Angle, Male, 2×20 pin, 100-mil spacing	WURTH ELEKTRONIK			Fitted
2	J2, J15	Header, Male 2×5-pin, 100-mil spacing	Sullins		0.100 inch × 5 × 2	Fitted
1	J4	Conn High SPD Card Edge 60 POS	3M		28.6 × 7 mm	Fitted
1	J5	Conn High SPD Card Edge 120 POS	3M		7 × 56 mm	Fitted
2	J6, J7	Header, Male 10-pin, 100-mil spacing,	Sullins		0.100 inch × 10	Fitted
3	J8, J9, J10	Header, Male 2-pin, 100-mil spacing,	Sullins		0.100 inch × 2	Fitted
1	J12	Header, Male 2×6 pin, 100-mil spacing	Sullins		0.100 inch × 2 × 6	Fitted
1	J13	Terminal Block, 2-pin, 15-A, 5.1 mm	OST		0.40 × 0.35 inch	Fitted
1	J14	Connector, SMA Jack, Vertical, Gold, SMD	Emerson Network Power	142-0711-201	SMA	Fitted
1	L1	Inductor, Shielded Drum Core, Ferrite, 3.3 µH, 3.72 A, 0.02 Ω, SMD	Coilcraft	MSS7341-332NLB	MSS7341	Fitted
1	LBL1	Thermal Transfer Printable Labels, 0.650" W × 0.200" H - 10,000 per roll	Brady	THT-14-423-10	PCB Label 0.650"H × 0.200"W	Fitted
4	MH1, MH2, MH3, MH4	Mountin hole, NPTH Drill 3.2 mm			Screw	Fitted
5	R1, R19, R20, R164, R165	RES, 22 Ω, 5%, 0.063 W, 0402	Vishay-Dale	CRCW040222R0JNED	0402	Fitted
7	R2, R3, R4, R25, R31, R35, R36	RES, 270 kΩ, 1%, 0.1 W, 0603	Yageo America	RC0603FR-07270KL	0603	Fitted
14	R5, R6, R7, R15, R16, R17, R26, R28, R32, R33, R34, R69, R70, R71	RES, 4.7 kΩ, 5%, 0.1 W, 0603	Vishay-Dale	CRCW06034K70JNEA	0603	Fitted
7	R8, R13, R14, R24, R37, R38, R39	RES, 7.50 kΩ, 1%, 0.1 W, 0603	Vishay-Dale	CRCW06037K50FKEA	0603	Fitted
16	R9, R43, R79, R85, R92, R102, R108, R109, R126, R130, R139, R140, R150, R159, R186, R204	RES, 0 Ω, 5%, 0.1 W, 0603	Vishay-Dale	CRCW06030000Z0EA	0603	Fitted
7	R10, R11, R12, R27, R40, R41, R42	RES, 100 kΩ, 1%, 0.1 W, 0603	Vishay-Dale	CRCW0603100KFKEA	0603	Fitted
23	R18, R21, R23, R68, R73, R74, R77, R83, R87, R91, R96, R107, R117, R123, R132, R138, R143, R145, R153, R160, R161, R162, R163	RES, 10.0 Ω, 1%, 0.1 W, 0603	Vishay-Dale	CRCW060310R0FKEA	0603	Fitted
7	R72, R80, R84, R118, R137, R142, R200	RES, 10.0 kΩ, 1%, 0.1 W, 0603	Vishay-Dale	CRCW060310K0FKEA	0603	Fitted
4	R86, R88, R207, R208	RES, 4.70 kΩ, 1%, 0.1 W, 0603	Yageo America	RC0603FR-074K7L	0603	Fitted
2	R93, R104	RES, 0 Ω, 5%, 0.063 W, 0402	Vishay-Dale	CRCW04020000Z0ED	0402	Fitted
1	R98	RES, 1.5 kΩ, 5%, 0.25 W, 1206	Vishay-Dale	CRCW12061K50JNEA	1206	Fitted
3	R113, R114, R115	RES, 100 Ω, 5%, 0.1W, 0603	Vishay-Dale	CRCW0603100RJNEA	0603	Fitted
1	R122	RES, 150 kΩ, 1%, 0.1 W, 0603	Yageo America	RC0603FR-07150KL	0603	Fitted
1	R131	RES, 6.8 Ω, 5%, 0.25 W, 1206	Vishay-Dale	CRCW12066R80JNEA	1206	Fitted
1	R135	RES, 49.9 Ω, 1%, 0.1 W, 0603	Vishay-Dale	CRCW060349R9FKEA	0603	Fitted

Table 17. FMB Bill of Materials (continued)

QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER	MANUFACTURER PN	PCB FOOTPRINT	NOTE
1	R149	RES, 1.47 kΩ, 1%, 0.1 W, 0603	Yageo America	ERJ3EKF1471V	0603	Fitted
1	R151	RES, 137 kΩ, 1%, 0.1 W, 0603	Vishay-Dale	CRCW0603137KFKEA	0603	Fitted
2	R156, R157	RES, 10 kΩ, 5%, 0.1 W, 0603	Vishay-Dale	CRCW060310K0JNEA	0603	Fitted
1	R168	RES, 300 Ω, 5%, 0.1 W, 0603	Vishay-Dale	CRCW0603300RJNEA	0603	Fitted
1	R169	RES, 620 Ω, 1%, 0.1 W, 0603	Yageo America	MC0063W06031620R	0603	Fitted
1	R170	RES, 17.4 kΩ, 1%, 0.1 W, 0603	Vishay-Dale	CRCW060317K4FKEA	0603	Fitted
1	R172	RES, 0 Ω, 5%, 0.1 W, 0603	Yageo America	RC0603JR-070RL	0603	Fitted
1	R173	RES, 15 kΩ, 5%, 0.1 W, 0603	Vishay-Dale	CRCW060315K0JNEA	0603	Fitted
1	R176	RES, 47.5 kΩ, 1%, 0.1 W, 0603	Vishay-Dale	CRCW060347K5FKEA	0603	Fitted
1	R177	RES, 10.2 kΩ, 1%, 0.1 W, 0603	Vishay-Dale	CRCW060310K2FKEA	0603	Fitted
1	R178	RES, 3.24 kΩ, 1%, 0.1 W, 0603	Vishay-Dale	CRCW06033K24FKEA	0603	Fitted
1	R180	RES, 42.2 kΩ, 1%, 0.1 W, 0603	Yageo America	ERJ3EKF4222V	0603	Fitted
1	R181	RES, 58.3 kΩ, 0.1%, 0.1 W, 0603	Yageo America		0603	Fitted
1	R182	RES, 0 Ω, 5%, 0.25 W, 1206	Vishay-Dale	CRCW12060000Z0EA	1206	Fitted
1	R184	RES, 48.7 kΩ, 1%, 0.1 W, 0603	Vishay-Dale	CRCW060348K7FKEA	0603	Fitted
1	R190	RES, 14.0 kΩ, 1%, 0.1 W , 0603	Vishay-Dale	CRCW060314K0FKEA	0603	Fitted
1	R191	RES, 499 Ω, 1%, 0.1 W, 0603	Vishay-Dale	CRCW0603499RFKEA	0603	Fitted
1	R193	RES, 4.99 kΩ, 1%, 0.1 W, 0603	Vishay-Dale	CRCW06034K99FKEA	0603	Fitted
1	R198	RES, 1.00 kΩ, 1%, 0.1 W, 0603	Vishay-Dale	CRCW06031K00FKEA	0603	Fitted
1	R206	RES, 910 Ω, 0.1%, 0.1 W, 0603	Susumu Co Ltd	CPF0603B910RE1	0603	Fitted
1	T1	Transformer	Wurth Elektronik	750342354	17.75 × 12.7 × 13.46 mm	Fitted
2	TP1, TP2	Test Point, 0.040 Hole	STD			Fitted
7	TP3, TP4, TP5, TP6, TP7, TP8, TP9	Test Point, 0.020 Hole	STD			Fitted
7	U1, U2, U3, U8, U13, U14, U15	IC, 1.1-nV/vHz Noise, Low Power, Precision Op-Amp	Texas Instruments	OPA211AID	SO	Fitted
7	U4, U5, U6, U11, U17, U18, U19	7 nsec, 2.7-V to 5-V Comparator with Rail-to- Rail Output, 5-pin SOT-23	Texas Instruments	LMV7219M5	MF05A	Fitted
1	U10	IC, Voltage Reference, 50 ppm/°C Max, 50 µA	Texas Instruments	REF3012AIDBZT	SOT23	Fitted
4	U16, U21, U25, U28	16-Bit, Quad Channel, Ultra-Low Glitch, Voltage Output DAC with 2.5 V, 2-ppm/°C Internal Reference, PW0016A	Texas Instruments	DAC8564IAPW	PW0016A	Fitted
1	U22	Programmable 3-PLL Clock Synthesizer / Multiplier/Divider	Texas Instruments	CDCE906PW	TSSOP (PW) 20	Fitted
1	U23	Buck Step Down Regulator with 3.5- to 28-V Input and 0.8- to 25-V Output, –40°C to 150°C, 8-Pin SOIC (D), Green (RoHS and no Sb/Br)	Texas Instruments	TPS54232D	D0008A	Fitted
1	U24	Ultra Low Noise, 800-mA Linear Voltage Regulator for RF/Analog Circuits, DNT0012B	Texas Instruments	LP38798SDE-ADJ/NOPB	DNT0012B	Fitted
1	U26	Integrated 5-A 40-V Wide Input Range Boost/SEPIC/Flyback DC-DC Regulator, RTE0016C	Texas Instruments	TPS55340RTET	RTE0016C	Fitted

Table 17. FMB Bill of Materials (continued)

QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER	MANUFACTURER PN	PCB FOOTPRINT	NOTE
1	U30	Optocoupler, 3.75-kV RMS, SMT	Vishay-Semiconductor	TCMT1107	SOP-4	Fitted
1	U32	IC, Precision Adjustable Shunt Regulator	Texas Instruments	TL431AIDBZR	SOT23-3	Fitted
1	U34	IC SRAM 512-KB 20 MHZ 8SOIC	Microchip Technology		8-SOIC (0.154", 3.90-mm Width)	Fitted
1	Y1	Crystal, 10.000 MHz, 10 pF, SMD	TXC Corporation	7B-27.000MEEQ-T	5 × 0.9 × 3.2 mm	Fitted
0	C15, C17, C88, C92, C99, C126, C128, C129, C131, C132, C133, C134, C140, C141, C142, C151, C152, C154, C157, C158, C163, C165, C169, C170, C171, C173, C175	CAP, CERM, 0.22 µF, 6.3V, +/-10%, X7R, 0603	MuRata		0603	Not Fitted
0	C20, C27	CAP, CERM, 0.047 µF, 25 V, ±5%, X7R, 0603	AVX		0603	Not Fitted
0	C22, C83, C86, C96, C104, C124, C127, C137, C145, C147, C148, C159, C162	CAP, CERM, 4.7 µF, 6.3 V, ±10%, X5R, 0603	Kemet		0603	Not Fitted
0	C63	CAP, CERM, 1 µF, 16 V, ±10%, X5R, 0603	TDK		0603	Not Fitted
0	C66, C178	CAP, CERM, 0.1 µF, 16 V, ±5%, X7R, 0603	AVX		0603	Not Fitted
0	C101, C108	CAP, CERM, 1 µF, 10 V, ±10%, X7R, 0603	MuRata		0603	Not Fitted
0	C103, C176	CAP, CERM, 100 pF, 50 V, ±5%, C0G/NP0, 0603	TDK		0603	Not Fitted
0	C123, C138, C143, C144, C160, C161	CAP, CERM, 100 µF, 6.3 V, ±20%, X5R, 1206	MuRata		1206	Not Fitted
0	C130	CAP, CERM, 47 pF, 25 V, ±5%, C0G/NP0, 0402	MuRata		0402	Not Fitted
0	C149	CAP, CERM, 10 µF, 35 V, ±20%, X7R, 1210	Taiyo Yuden		1210	Not Fitted
0	D1, D2	Diode, TVS, Bi, 15 V, 160 W, SOD-323	NXP Semiconductor		SOD-323	Not Fitted
0	D3, D9	LED SmartLED Green 570 NM	OSRAM		0603	Not Fitted
0	D13	Diode, Ultrafast, 75 V, 0.3 A, SOT-23	Diodes Inc.		SOT-23	Not Fitted
0	FB2, FB3, FB4, FB5	Ferrite Chip 1000 Ω, 300 MA 0603	TDK Corporation		0603	Not Fitted
0	J3	Connector, USB Micro, Type AB	Molex		5.3 × 7.5 mm	Not Fitted
0	J11	Connector Header 14-Pos 2-mm Vert Gold	Molex Inc		2.00 mm	Not Fitted
0	R22, R158, R192	RES, 0 Ω, 5%, 0.1 W, 0603	Vishay-Dale		0603	Not Fitted
0	R29, R78, R127, R136, R144, R148, R152, R166, R187, R188, R202	RES, 4.87 kΩ, 1%, 0.1 W, 0603	Vishay-Dale		0603	Not Fitted
0	R30	RES, 300 Ω, 5%, 0.1 W, 0603	Vishay-Dale		0603	Not Fitted
0	R44, R45, R46, R47, R48, R49, R50, R51, R52, R53, R54, R55, R56, R57, R58, R59, R60, R61, R62, R63, R64, R65, R66, R67, R94, R99, R105, R106, R112, R119, R120, R133, R141, R146, R147, R154, R155, R174, R175, R179, R185, R189	RES, 22 Ω, 5%, 0.063 W, 0402	Vishay-Dale		0402	Not Fitted
0	R75, R76, R81, R82, R89, R90, R100, R101, R110, R111, R124, R125, R129, R134	RES, 100 Ω, 5%, 0.1 W, 0603	Vishay-Dale		0603	Not Fitted
0	R95, R97, R116	RES, 0 Ω, 5%, 0.063 W, 0402	Vishay-Dale		0402	Not Fitted
0	R103, R121	RES, 10 kΩ, 5%, 0.1 W, 0603	Vishay-Dale		0603	Not Fitted
0	R128, R195	RES, 100 kΩ, 1%, 0.1 W, 0603	Vishay-Dale		0603	Not Fitted
0	R167, R171	Resistor, Chip Array, 4.7 KΩ 4-RES 0612	Vishay		0612	Not Fitted
0	R183	RES, 0 Ω, 5%, 0.25 W, 1206	Vishay-Dale		1206	Not Fitted
0	R194	RES, 10 kΩ, 5%, 0.1 W, 0603	Yageo America		0603	Not Fitted

Table 17. FMB Bill of Materials (continued)

QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER	MANUFACTURER PN	PCB FOOTPRINT	NOTE
0	R196	RES, 301 Ω, 0.5%, 0.1 W, 0603	Yageo America		0603	Not Fitted
0	R197, R205	RES, 0 Ω, 5%, 0.1 W, 0603	Yageo America		0603	Not Fitted
0	R199	RES, 220 Ω, 1%, 0.1 W, 0603	Yageo America		0603	Not Fitted
0	R201, R203	RES, 4.70 kΩ, 1%, 0.1 W, 0603	Yageo America		0603	Not Fitted
0	S1, S3	Switch, Tactile, SPST-NO, 0.05 A, 12 V, SMT	TE Connectivity		SW, SPST 6×6 mm	Not Fitted
0	S2	Switch, Slide, SPST 4 poles, SMT	CTS Electrocomponents		SW, SMT Half Pitch 4SPST, 5.8×2.7×6.25 mm	Not Fitted
0	TP10	Test Point, 0.020 Hole	STD			Not Fitted
0	U7	IC, Single-Chip USB-to-UART Bridge	Silicon Labratories		QFN-28	Not Fitted
0	U9	Polyzen, 5.6 V, PPTC/Zener, SMD	TE		SMD 4 × 4 mm	Not Fitted
0	U12	Voltage Reference, SRS PREC 4.096 V SOT23-3	Texas Instruments		SOT23	Not Fitted
0	U20	IC FPGA SPARTAN, 102 I/O, 144TQFP	Xilinx		TQG-144	Not Fitted
0	U27	Single LVDS Transmitter	Micron Technology		SO8W	Not Fitted
0	U29	Programmable 1-PLL VCXO Clock Synthesizer With 1.8-V, 2.5-V, and 3.3-V Outputs, PW0014A	Texas Instruments		PW0014A	Not Fitted
0	U31	IC, 150 mA, Low IQ, LDO Regulator	Texas Instruments		uDFN	Not Fitted
0	U33	IC, 100 MHz, EconOscillator, 2.7-3.6 V, 8 uSOP	Maxim		8 uSOP	Not Fitted
0	U35	IC SRAM 512KB 20 MHZ 8SOIC	Microchip Technology		8-SOIC (0.154", 3.90-mm Width)	Not Fitted
0	U36	IC, Ultra-low Noise, High PSRR 200 mA, LDO, 1.2 V, 0.2 A 5SOT	Texas Instruments		SOT23-5	Not Fitted
0	U37	IC EEPROM 1 MB, 1 MHZ 8SOIC	ON Semiconductor		8-SOIC (0.154", 3.90-mm Width)	Not Fitted
0	Y2	Crystal, 10.000 MHz, 10 pF, SMD	TXC Corporation		5 × 0.9 × 3.2 mm	Not Fitted

8.3 Layer Plots

To download the layer plots, see the design files at TIDA-00171.

8.3.1 DSM

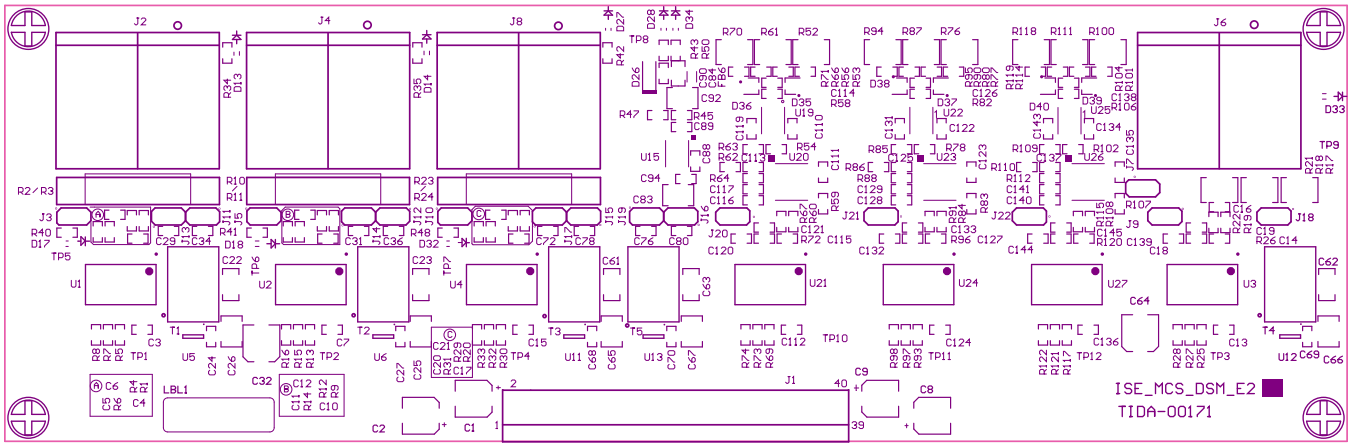


Figure 145. Top Overlay

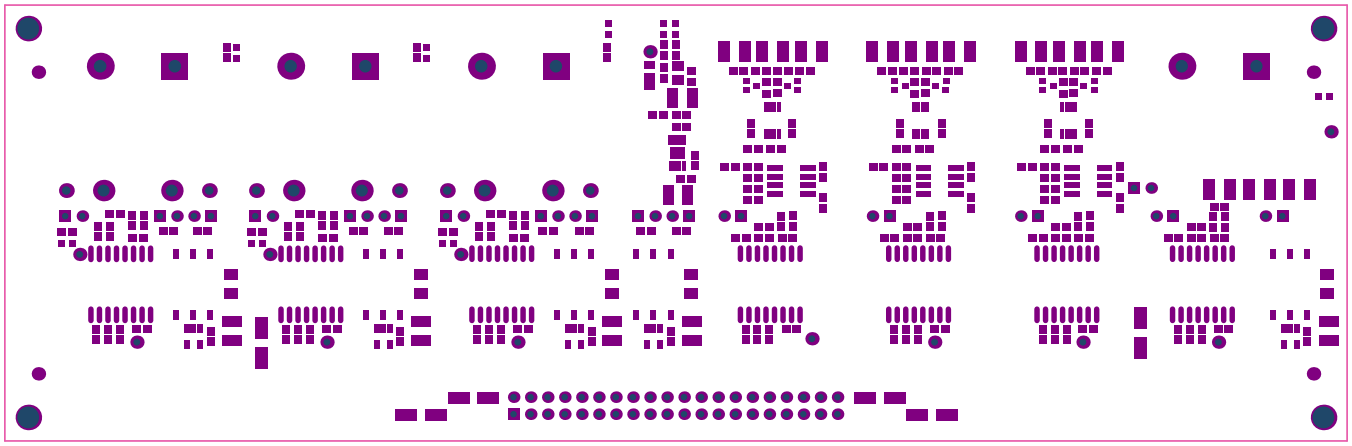


Figure 146. Top Solder

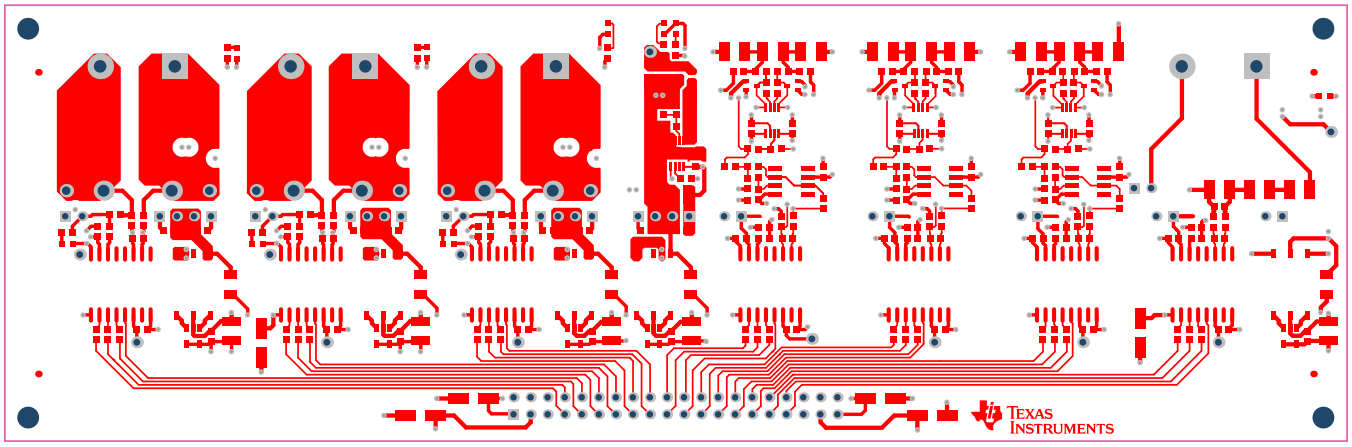


Figure 147. Top Layer

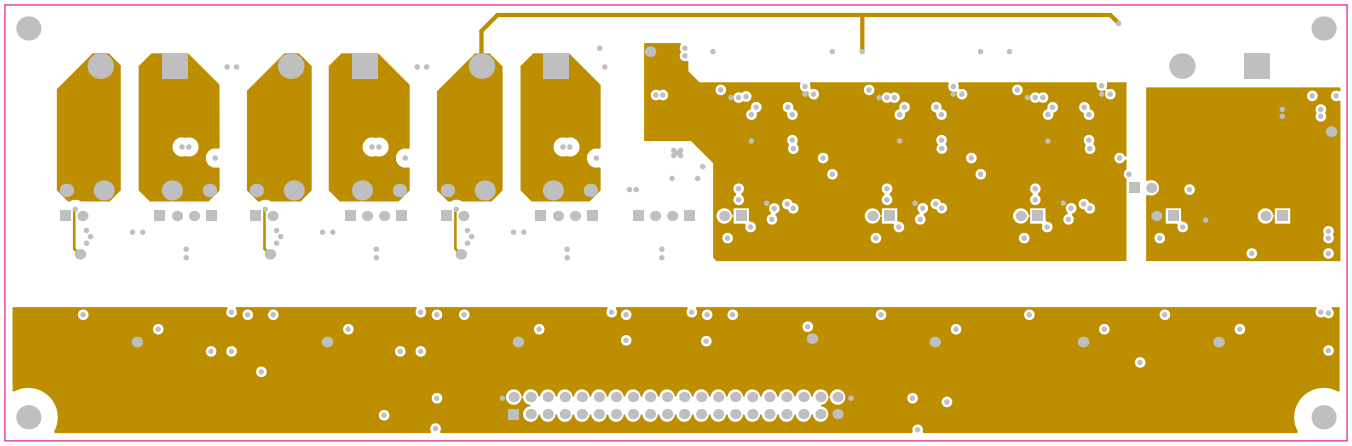


Figure 148. Mid Layer 1

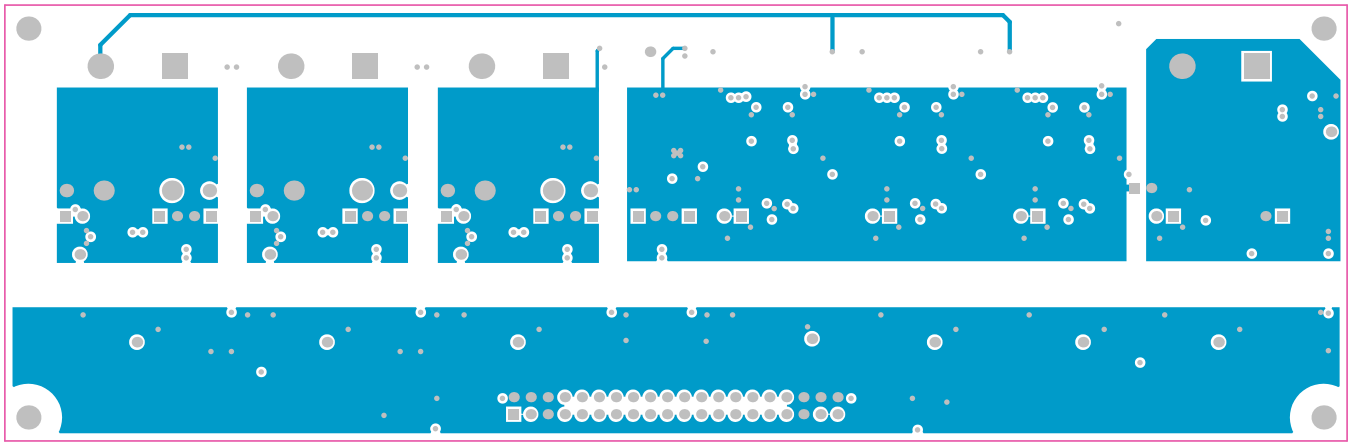


Figure 149. Mid Layer 2

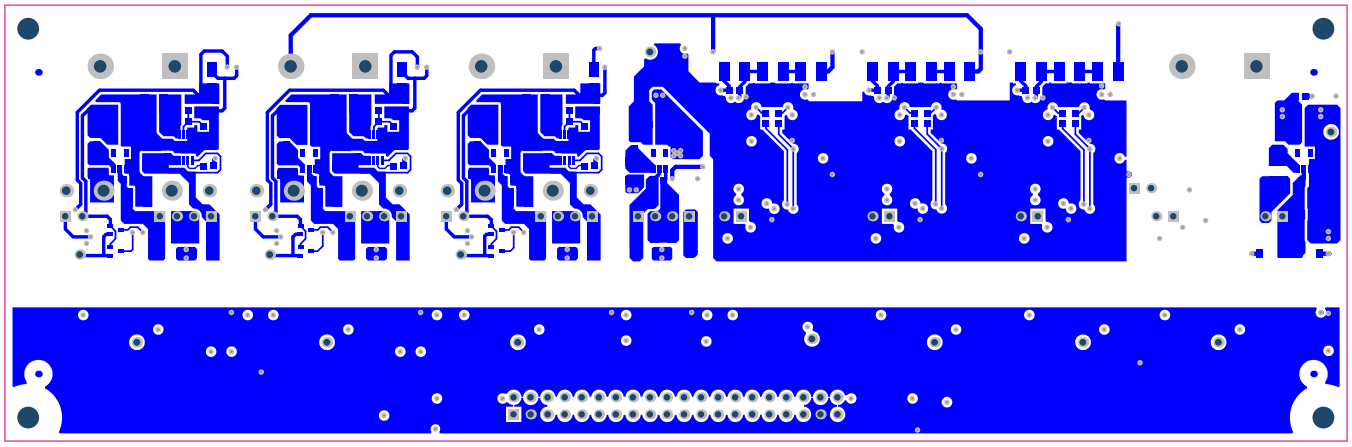


Figure 150. Bottom Layer

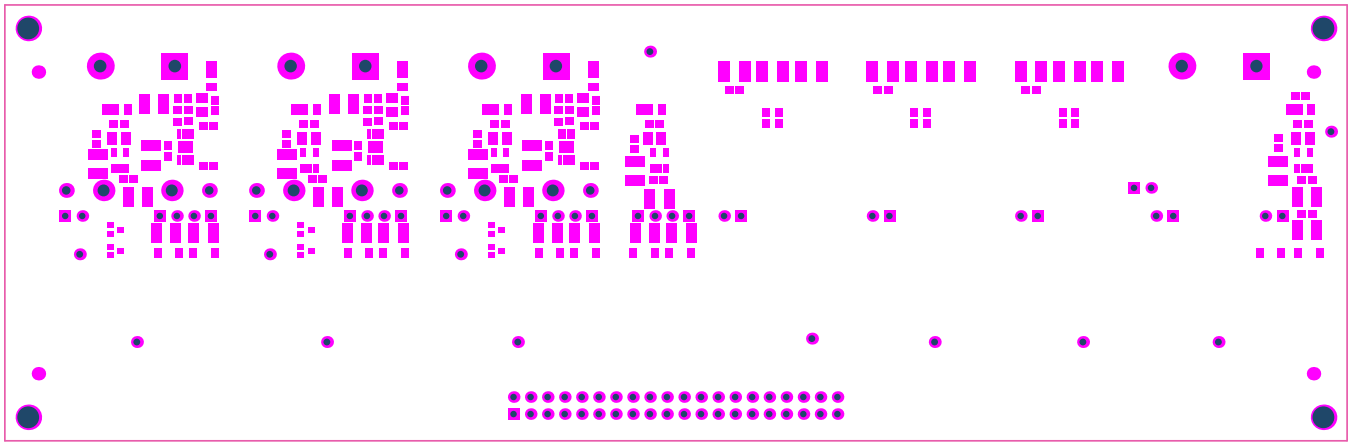


Figure 151. Bottom Solder

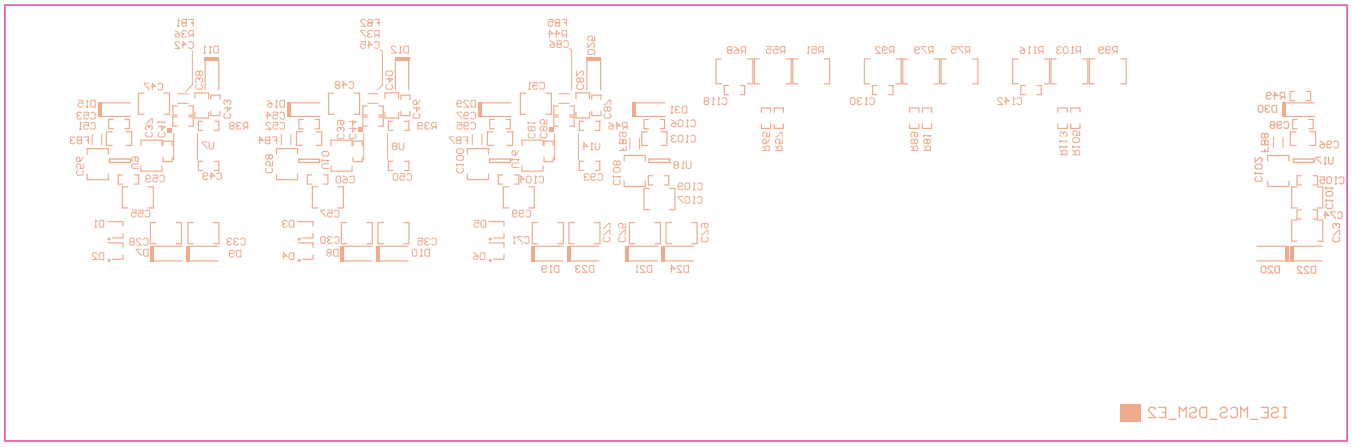


Figure 152. Bottom Overlay

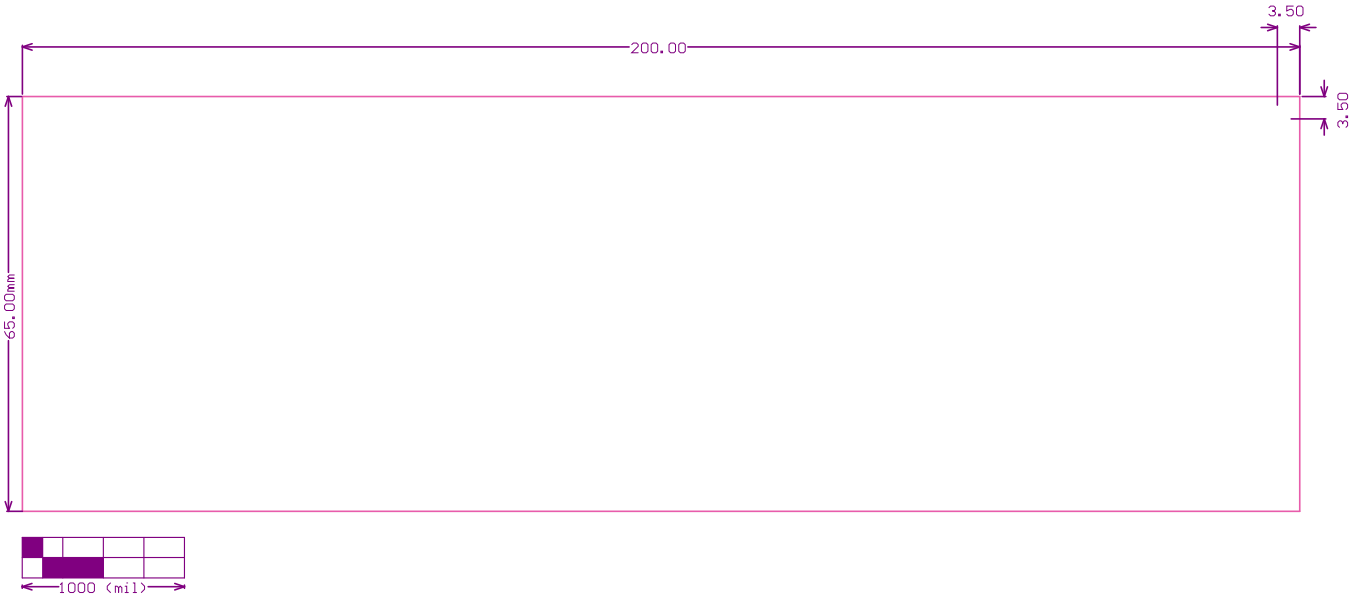


Figure 153. Board Dimensions

8.3.2 FMB

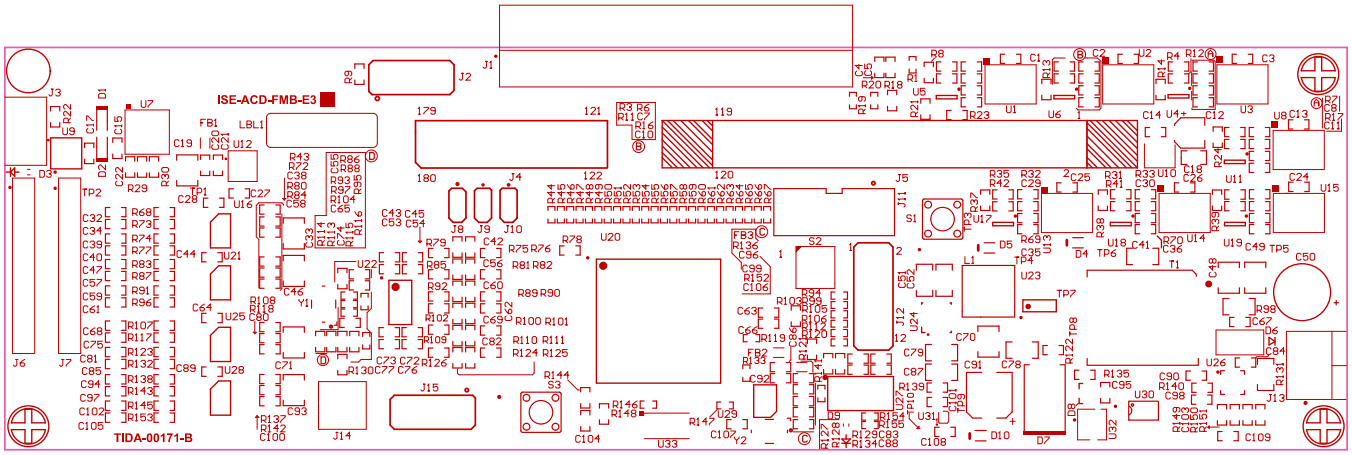


Figure 154. Top Overlay

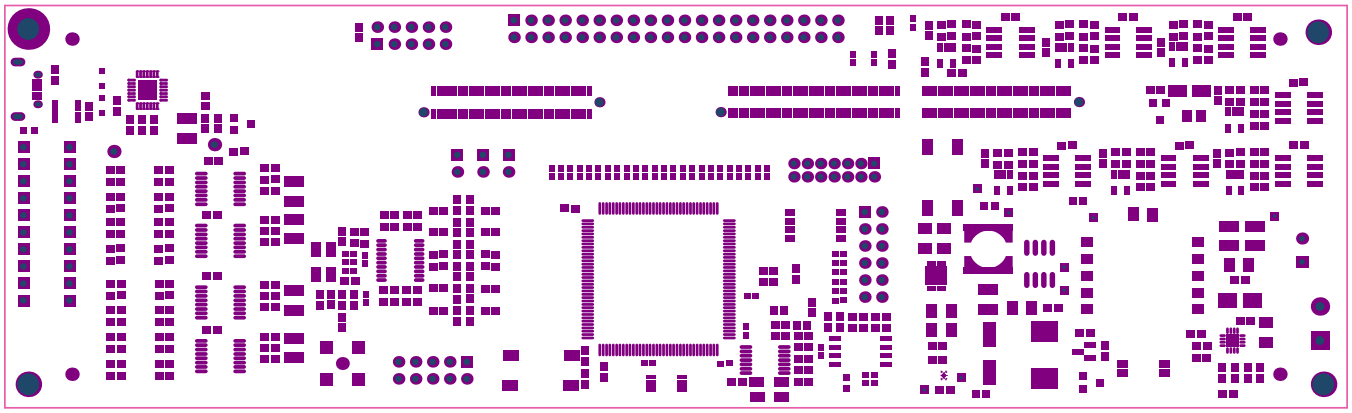


Figure 155. Top Solder

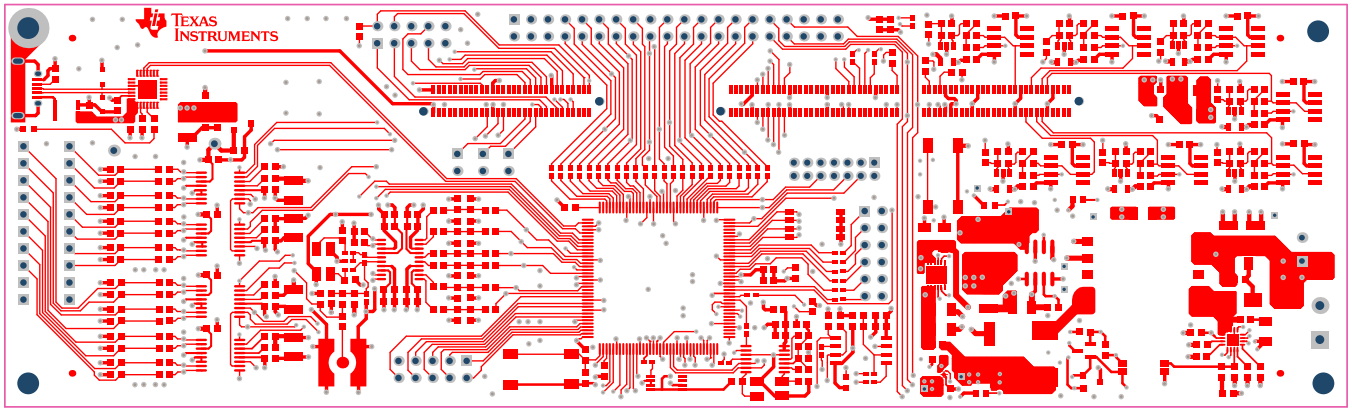


Figure 156. Top Layer

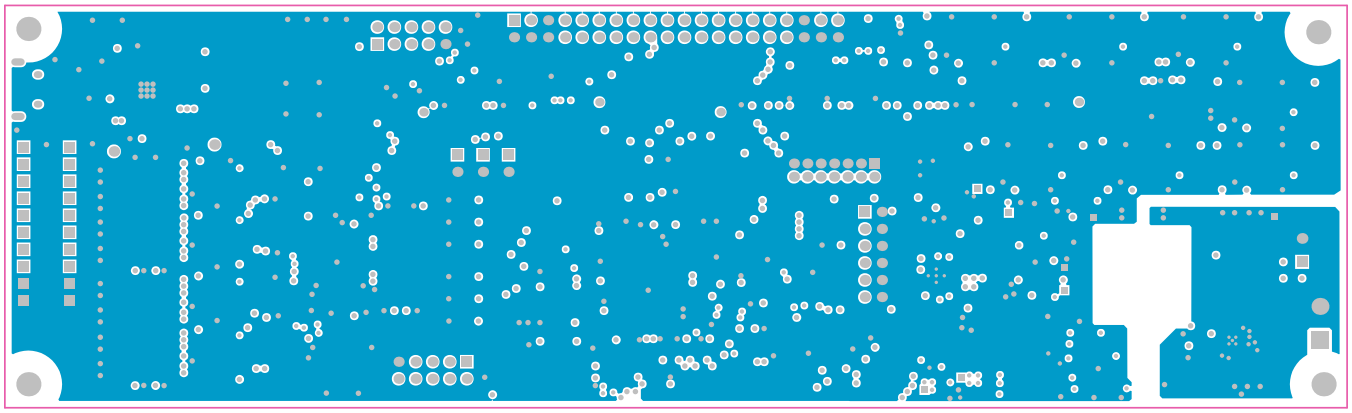


Figure 157. Mid Layer 1

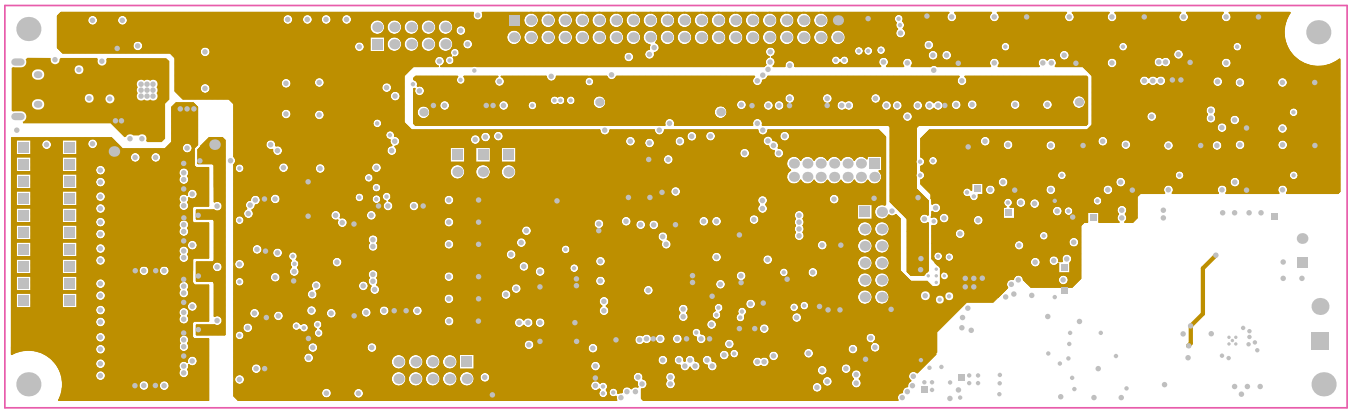


Figure 158. Mid Layer 2

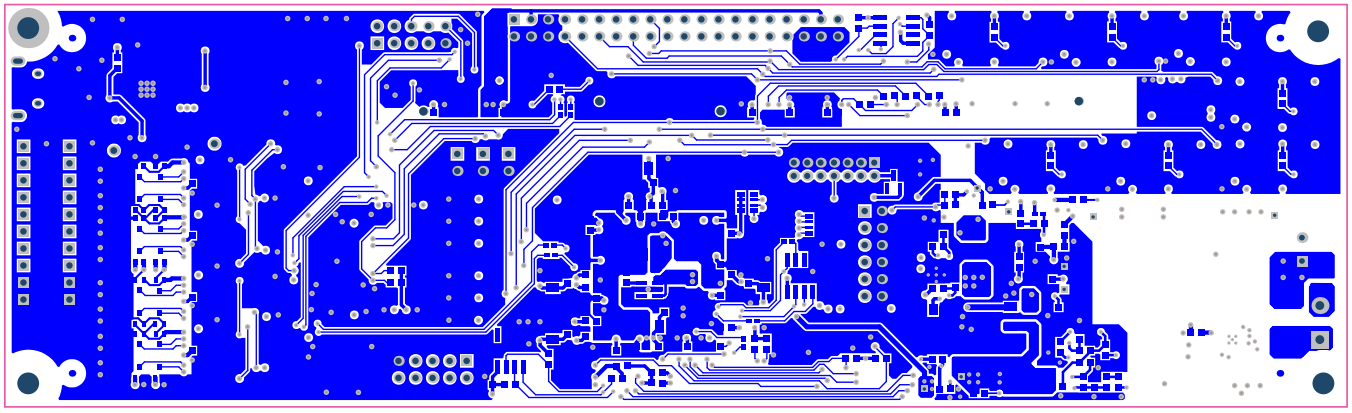


Figure 159. Bottom Layer

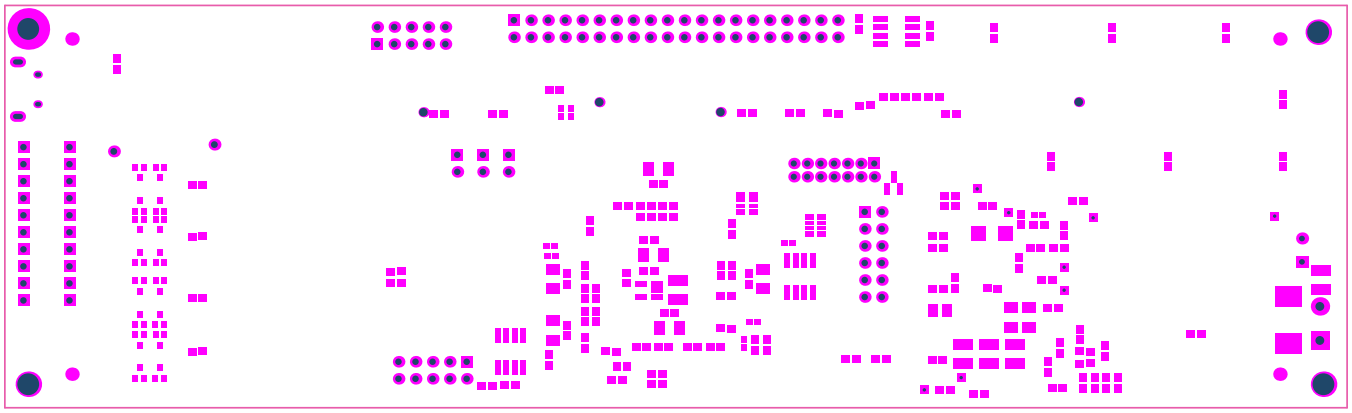


Figure 160. Bottom Solder

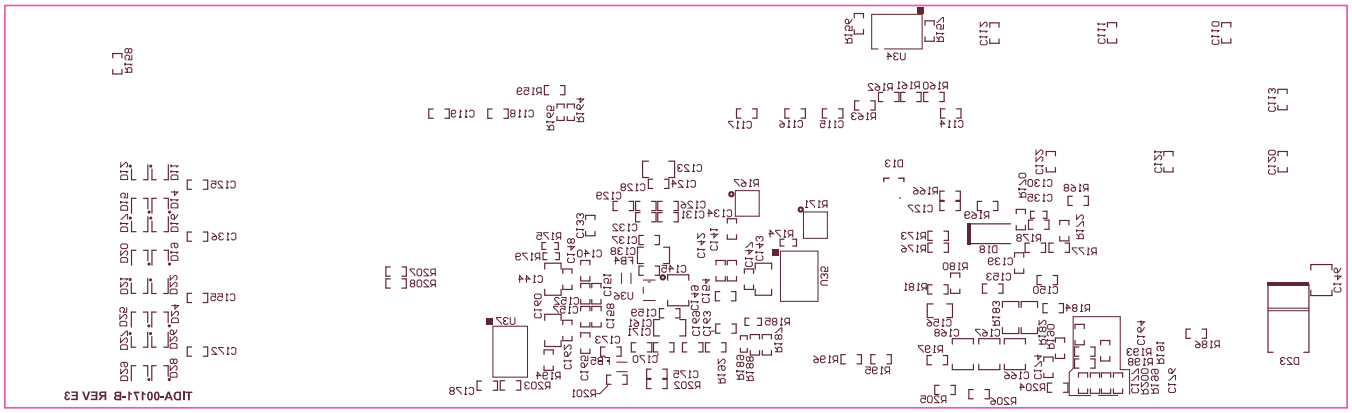


Figure 161. Bottom Overlay

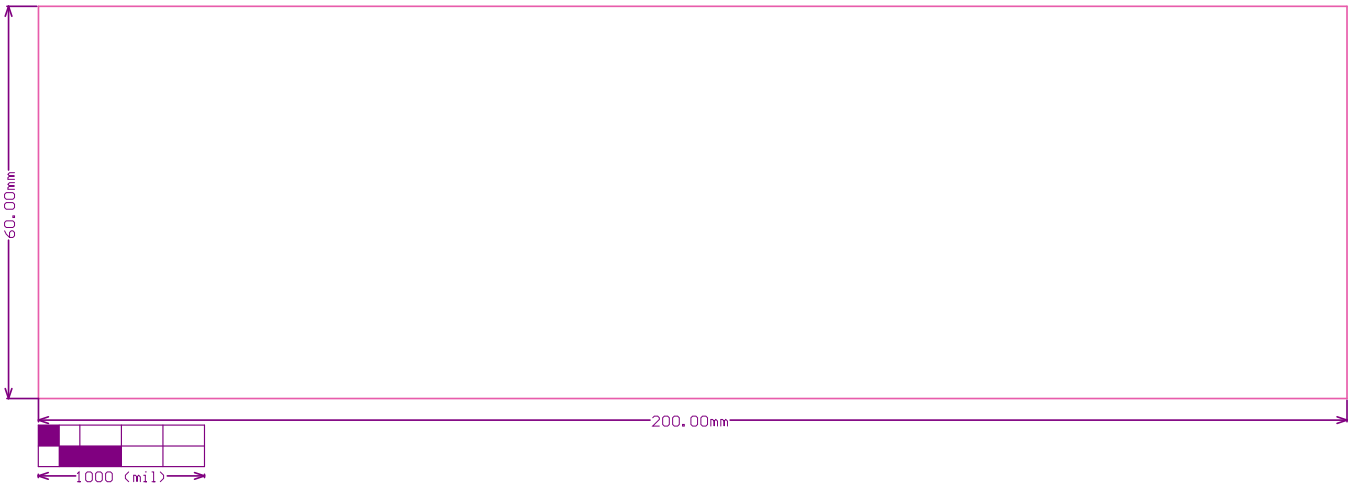


Figure 162. Board Dimensions

8.4 Altium Project Files

To download the Altium project files, see the design files at TIDA-00171.

8.4.1 DSM

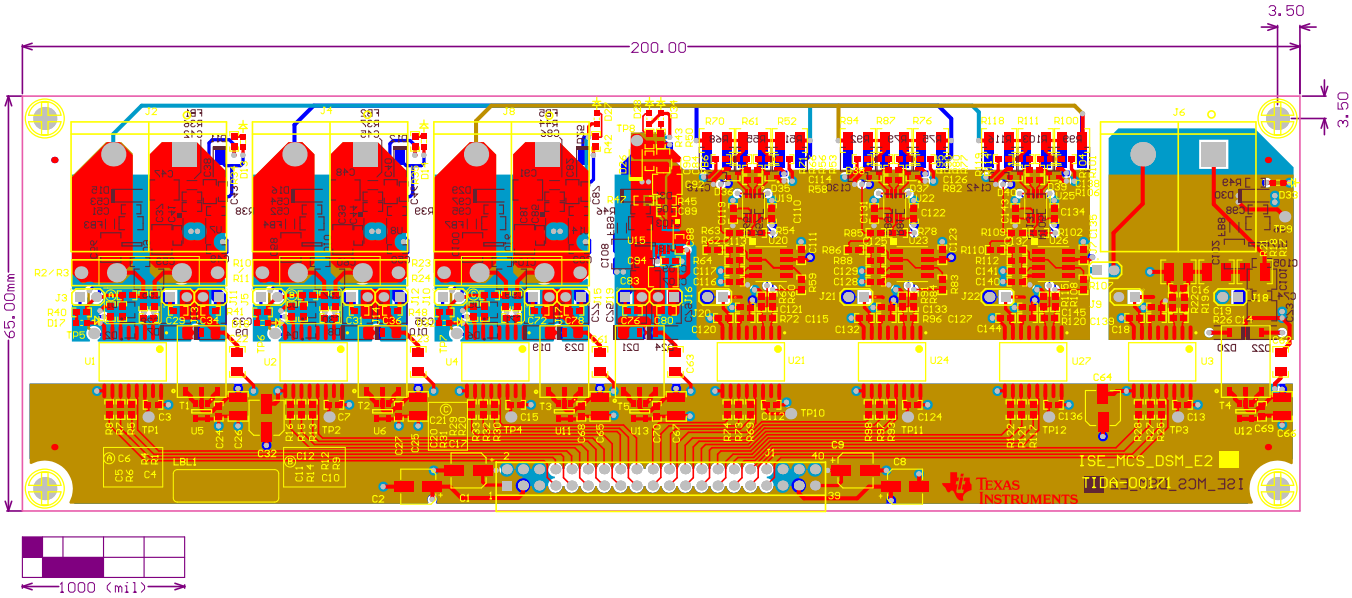


Figure 163. Multilayer Composite Print

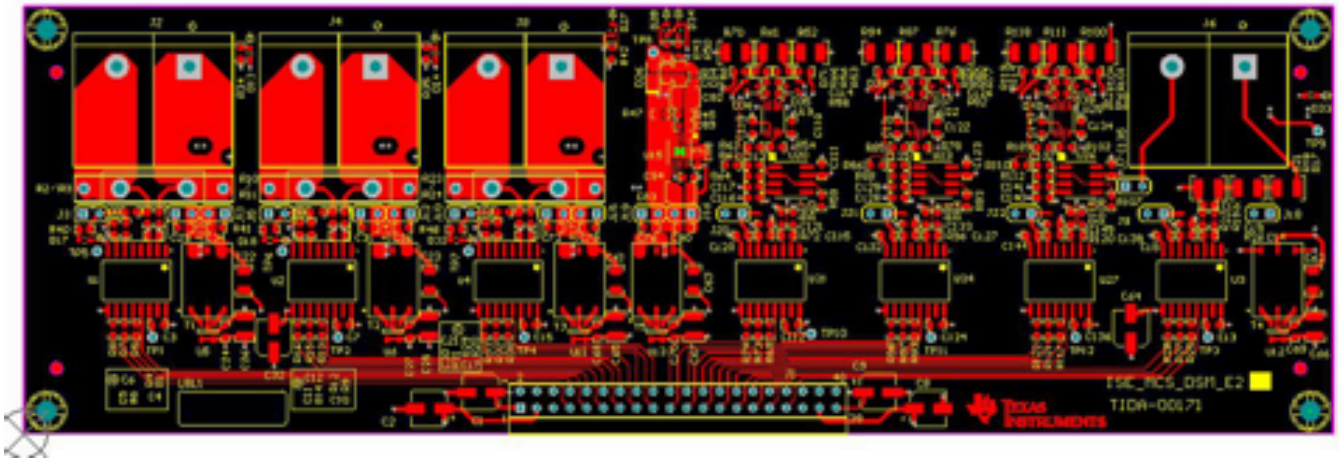


Figure 164. Top Layer

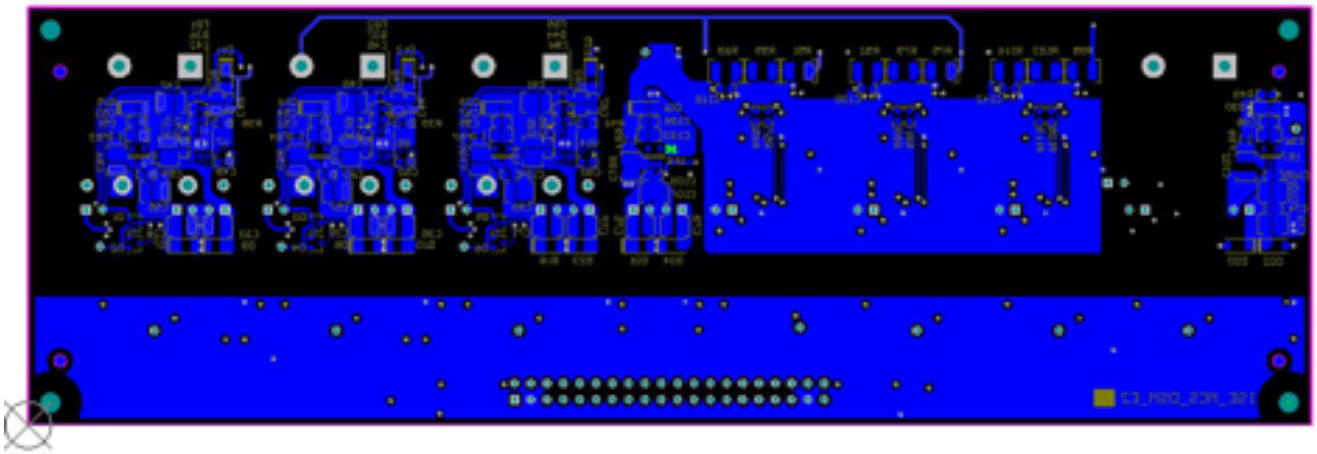


Figure 165. Bottom Layer

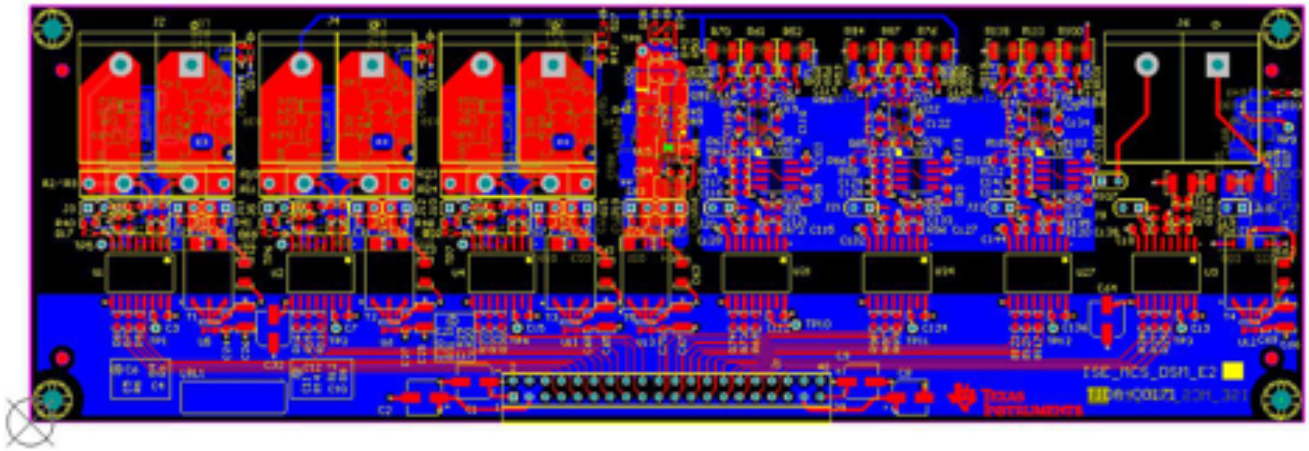


Figure 166. Top and Bottom Layers Combined

8.4.2 FMB

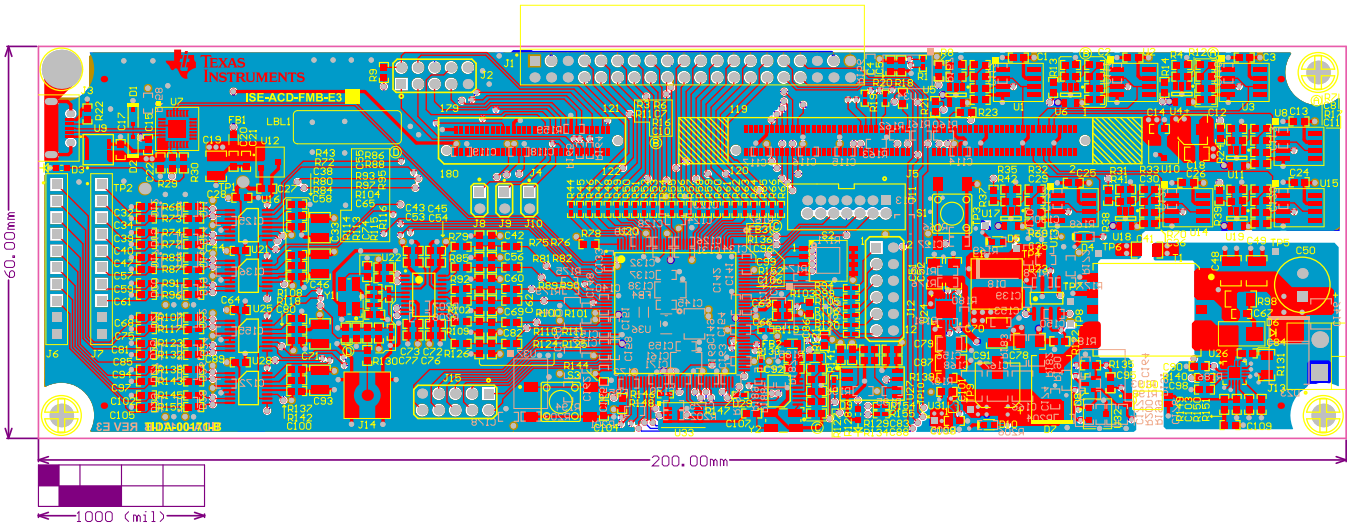


Figure 167. Multilayer Composite Print

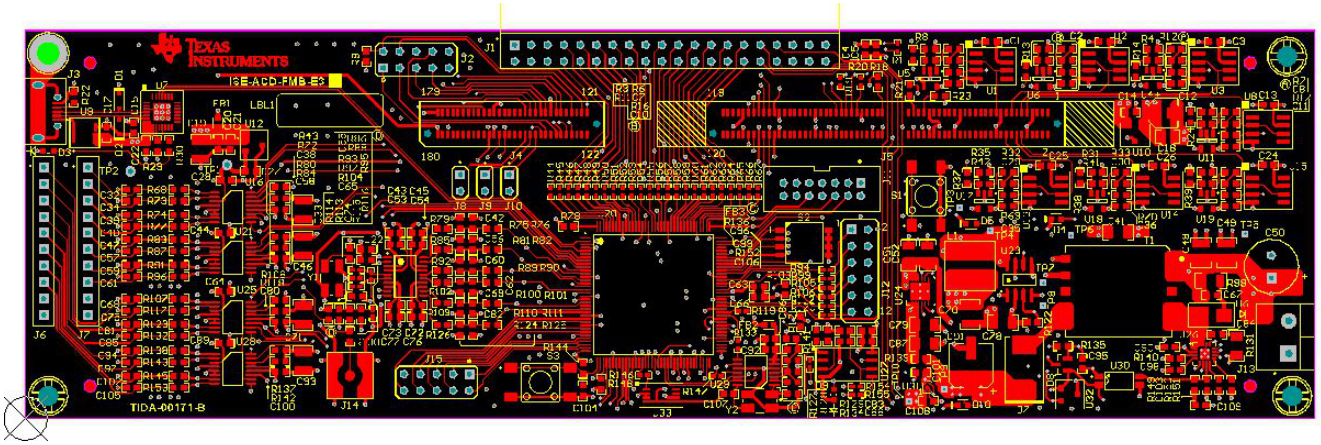


Figure 168. Top Layer

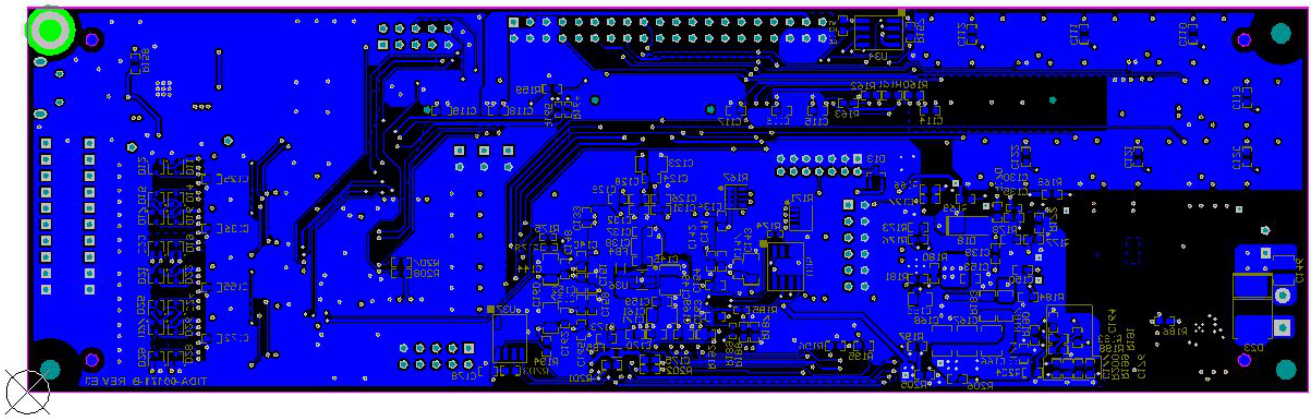


Figure 169. Bottom Layer

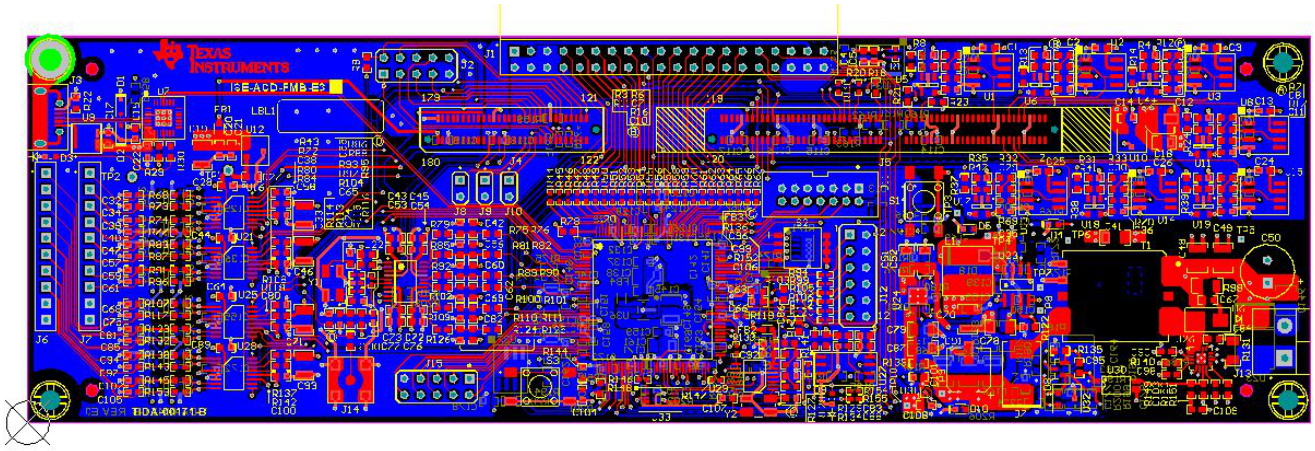


Figure 170. Top and Bottom Layers Combined

8.5 Gerber Files

To download the Gerber files, see the design files at TIDA-00171.

8.5.1 DSM

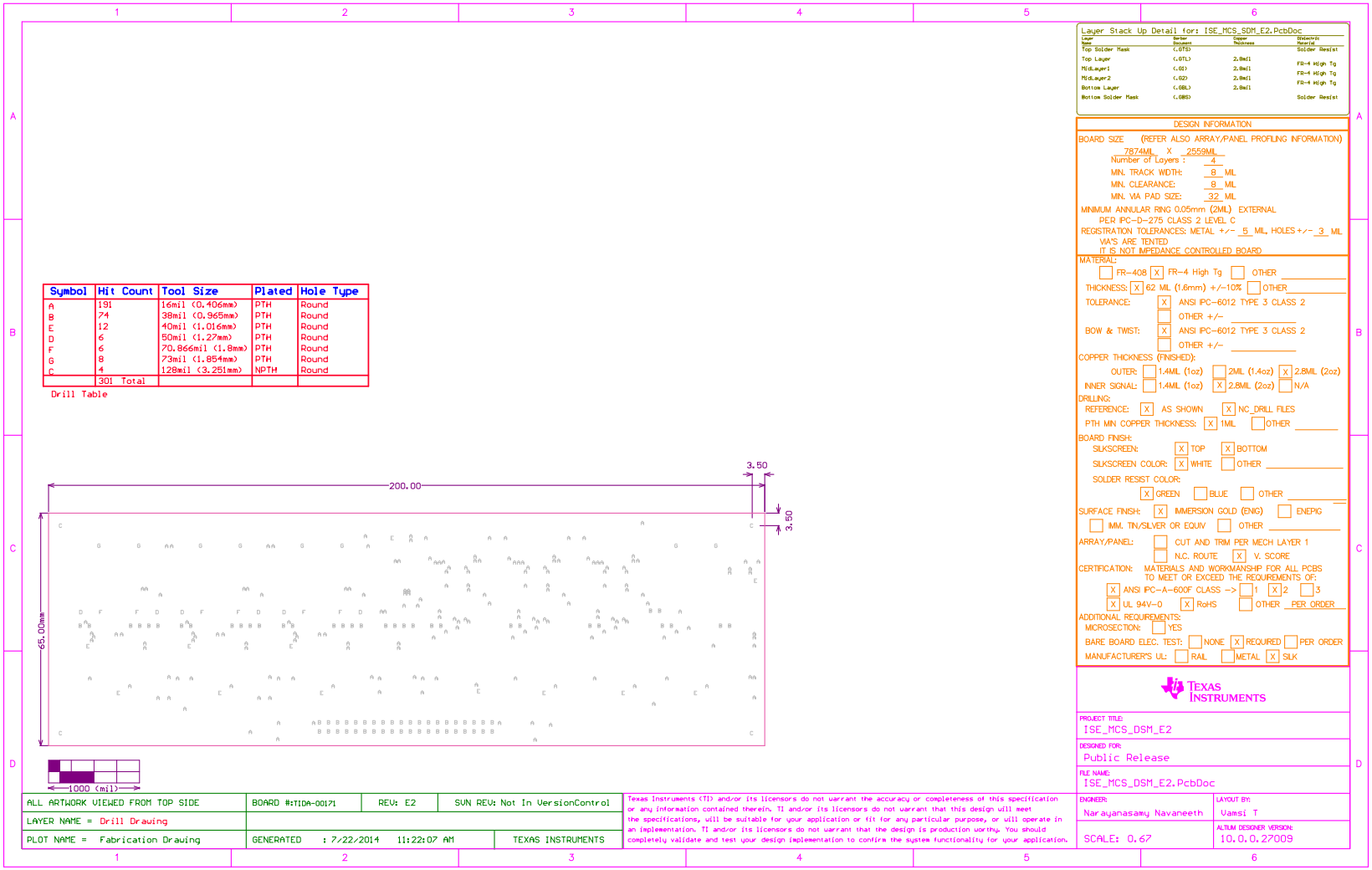


Figure 171. Fabrication Drawing

8.5.2 FMB

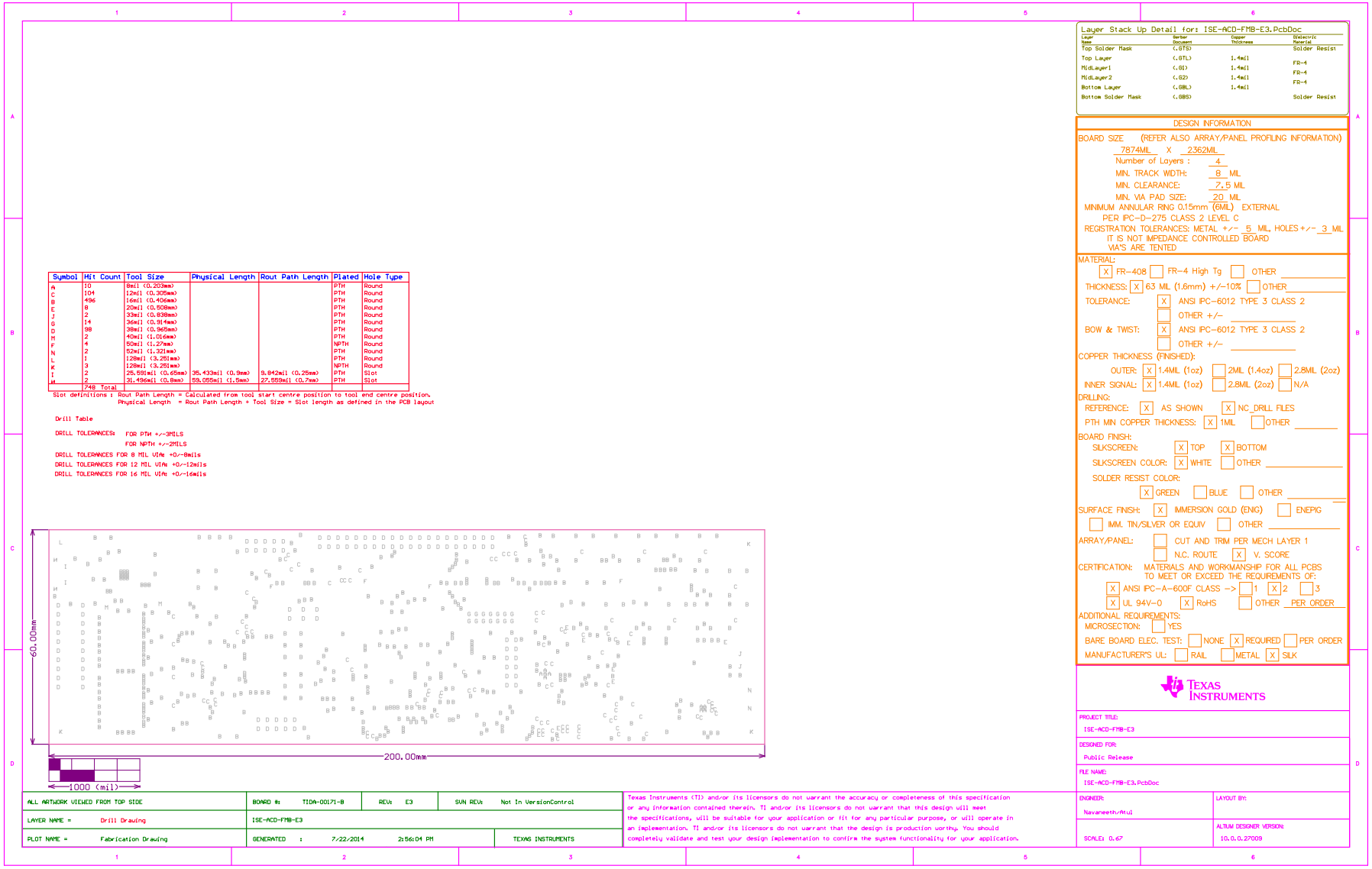


Figure 172. Fabrication Drawing

8.6 Assembly Drawings

8.6.1 DSM

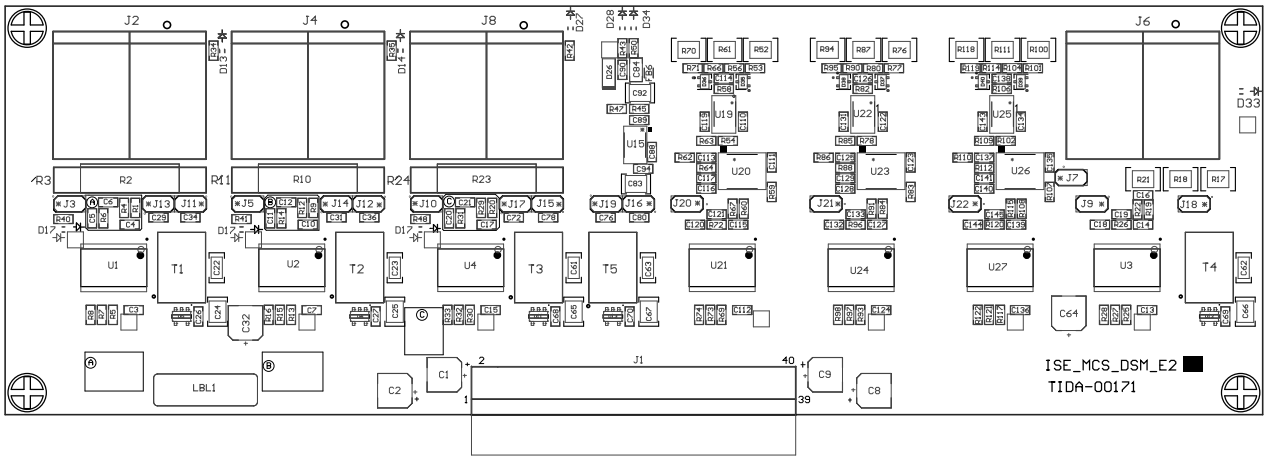


Figure 173. Top Assembly

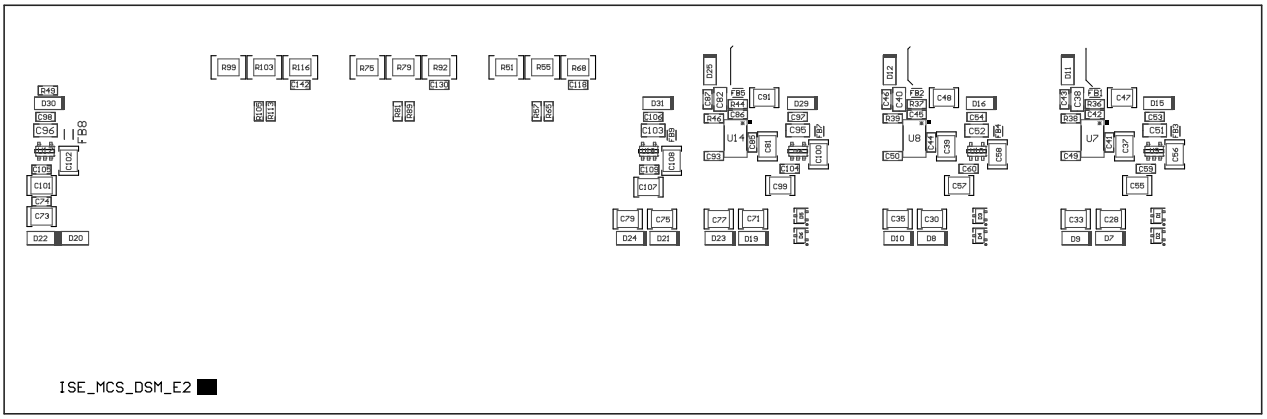


Figure 174. Bottom Assembly

8.6.2 FMB

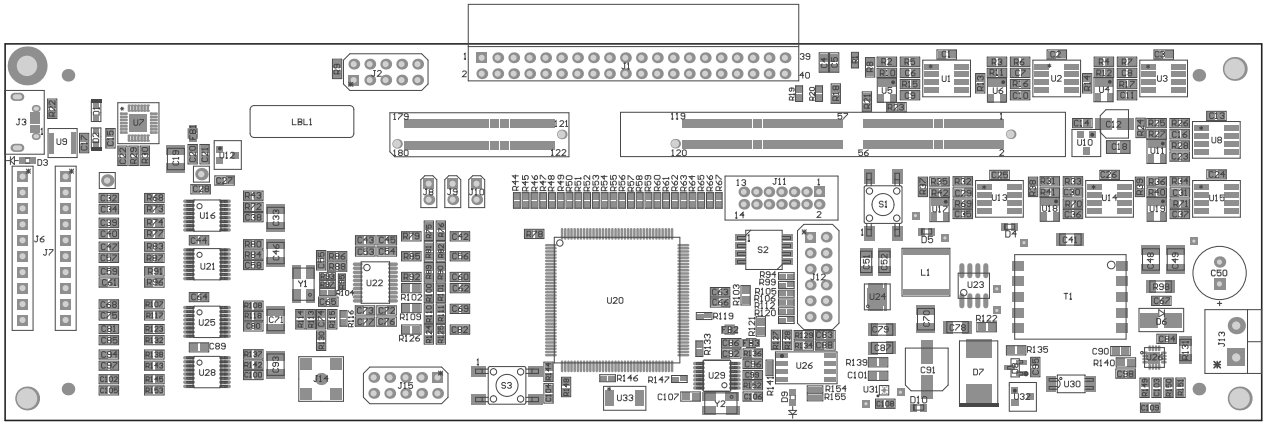


Figure 175. Top Assembly

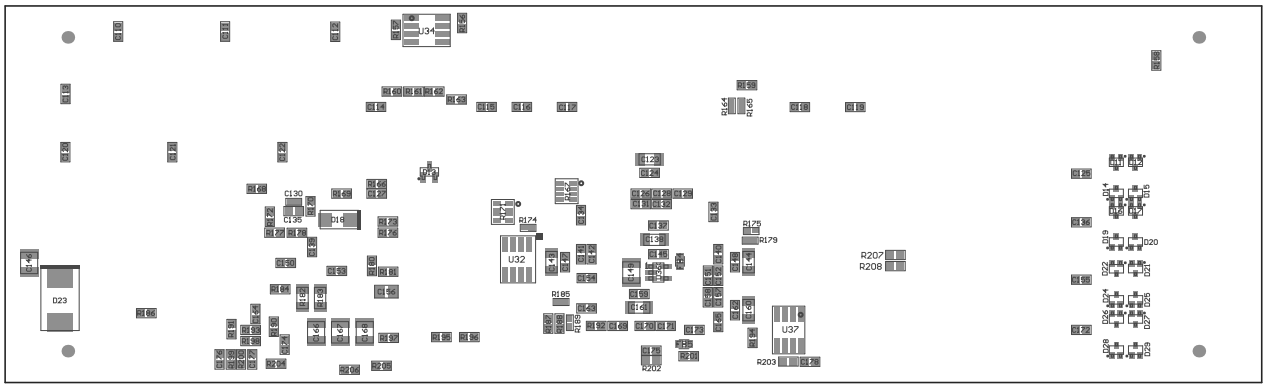


Figure 176. Bottom Assembly

9 References

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5. AMC1305 data sheet (SBAS654A)
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7. SPRUHM8A — TMS320F2837xD Delfino™ Microcontrollers Technical Reference Manual

10 About the Author

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Revision History

Changes from Original (October 2014) to A Revision	Page
• Changed from LVDS interface to CMOS interface	91
• Changed from LVDS interface to CMOS interface	91

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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